

# VERSION HISTORY

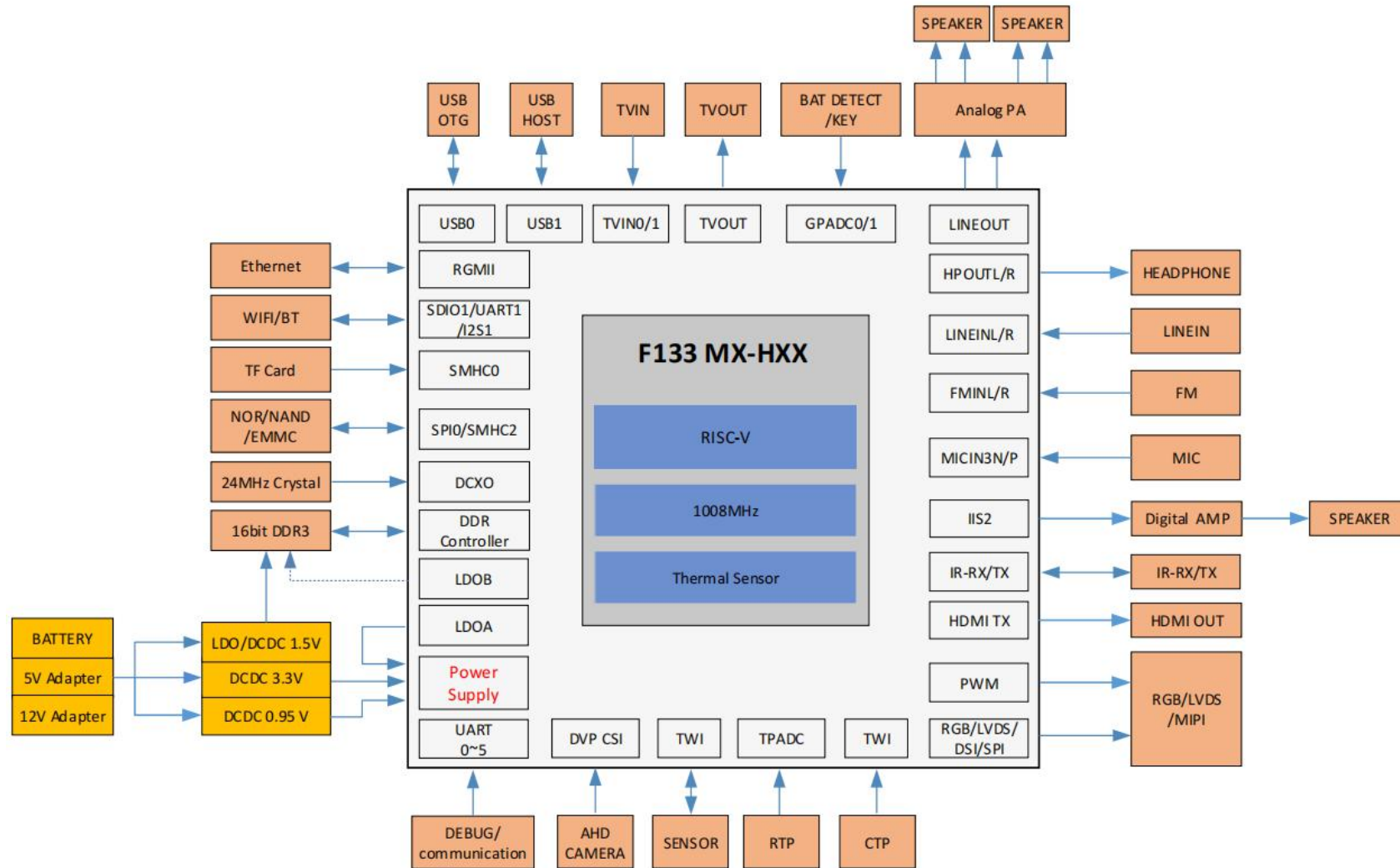
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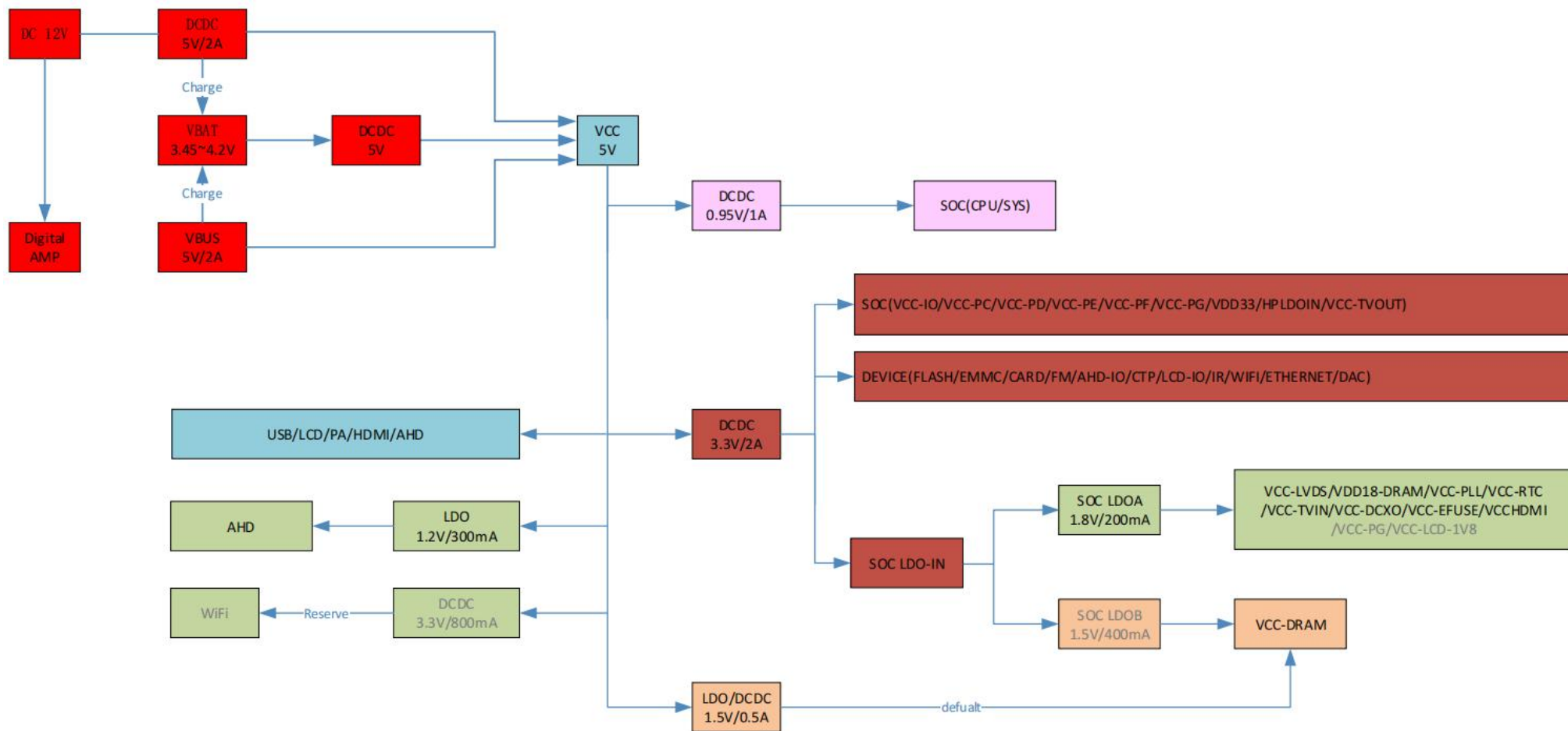
Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Release Version	2024-10-18			

	<b>AllWinner Technology Co., Ltd</b>		
	Design Name	F133 MX-HXX_STD_V1_0	
Size A3	Page Name	01 VERSION HISTORY	
Date:	Friday, November 01, 2024	Sheet	1 of 18

# BLOCK

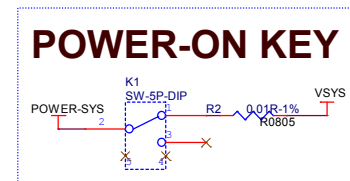
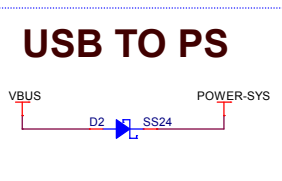
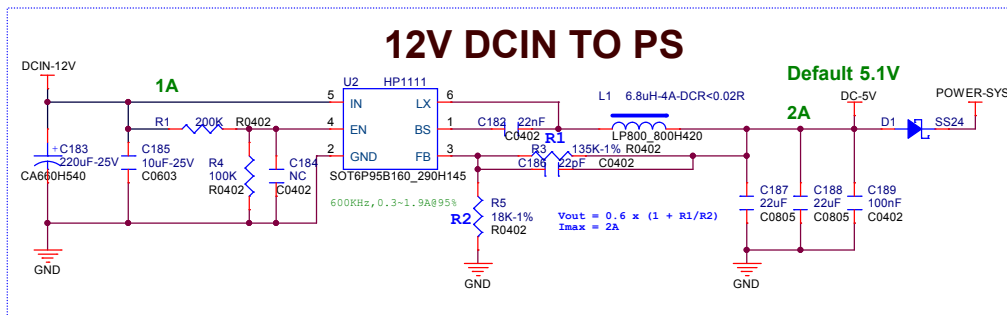
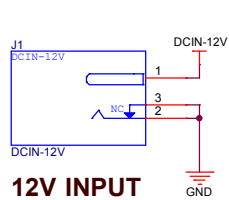


# F133 MX-HXX电源树

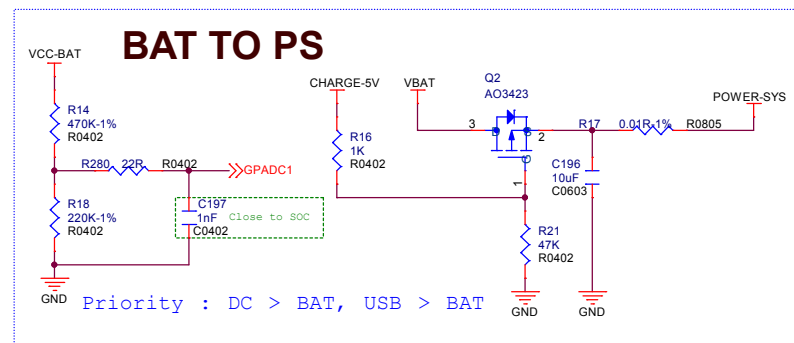
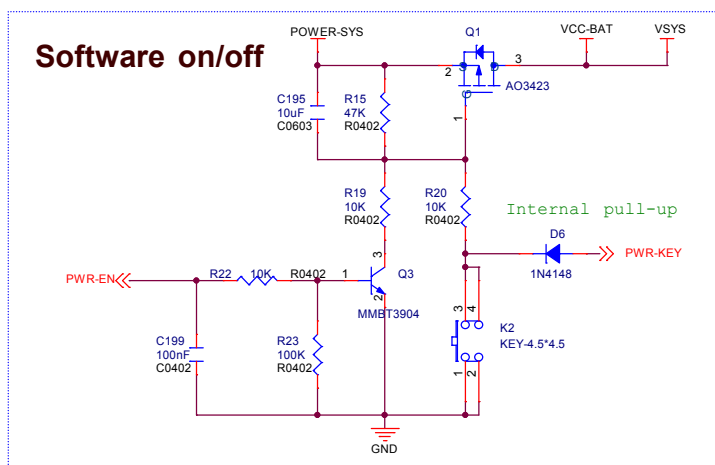
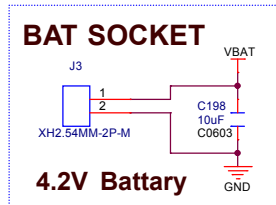
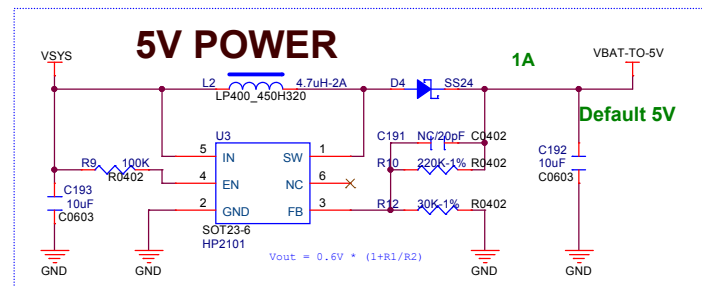
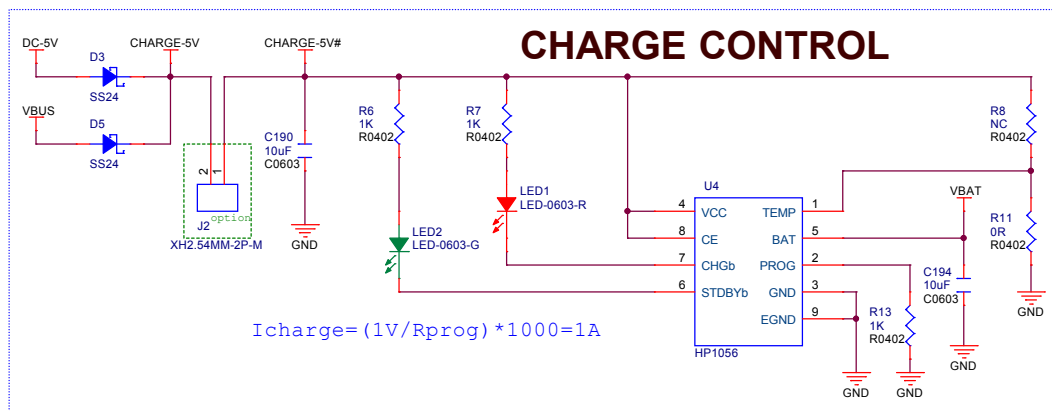


# POWER1

## DC-IN Programme

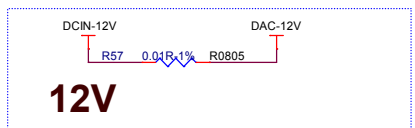
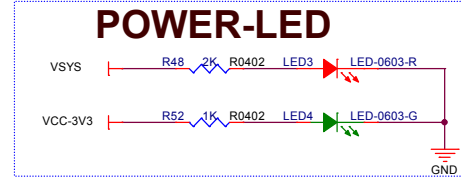
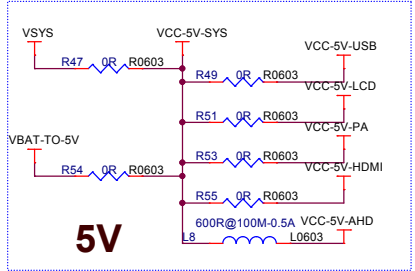
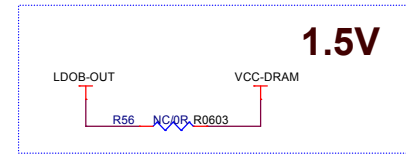
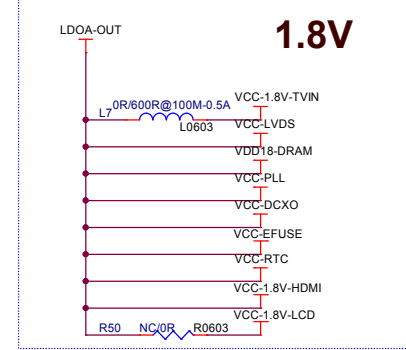
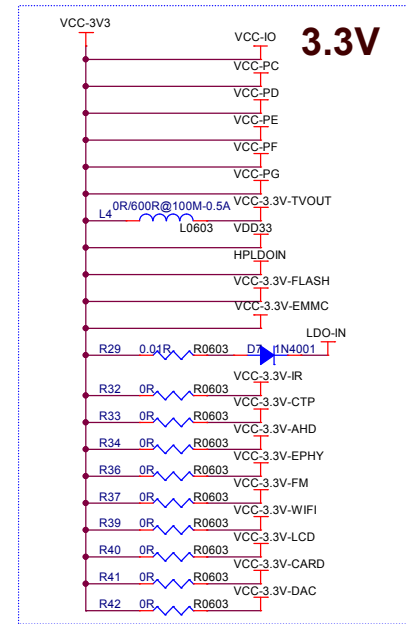
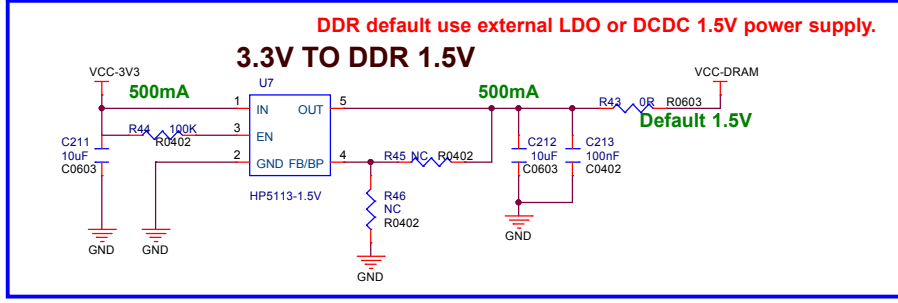
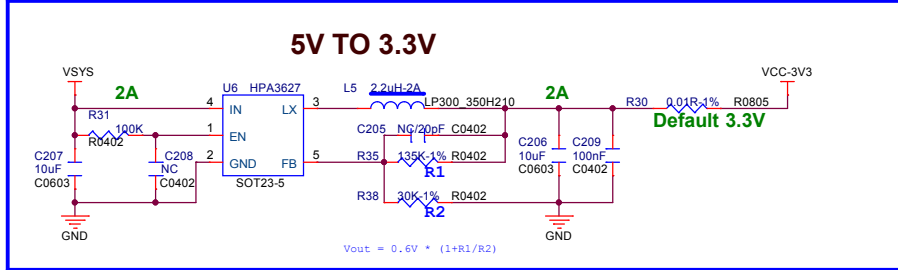
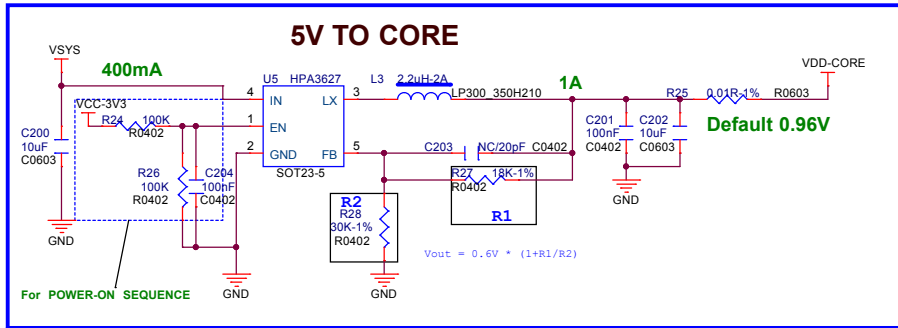


## Battery Programme



# POWER2

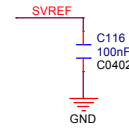
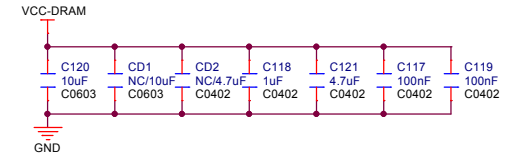
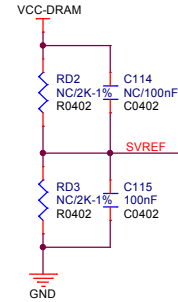
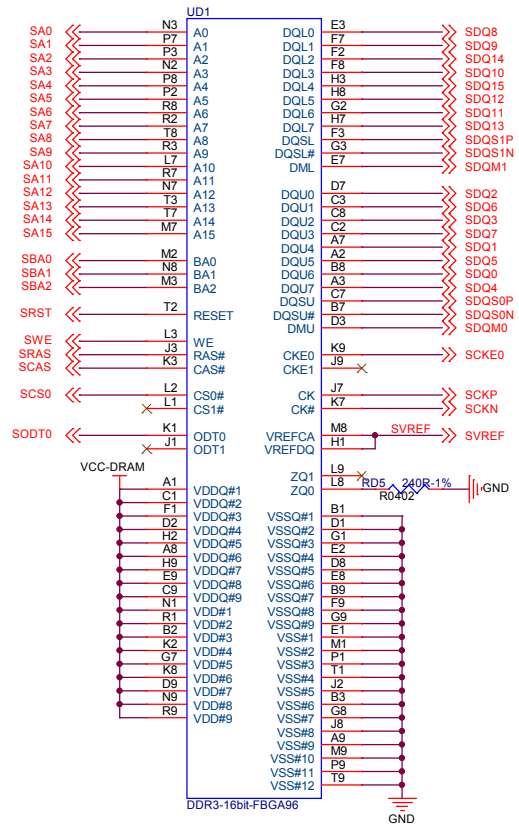
Place on bottom.





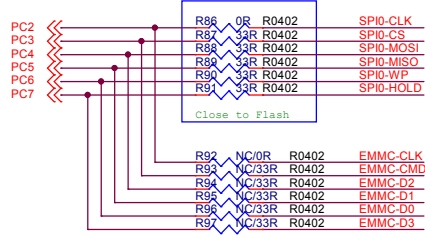
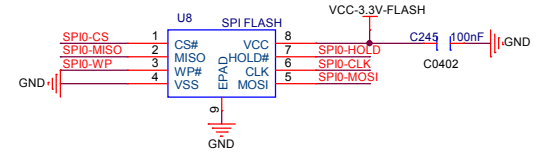
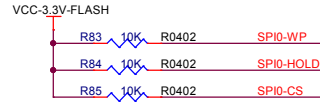


# DDR3

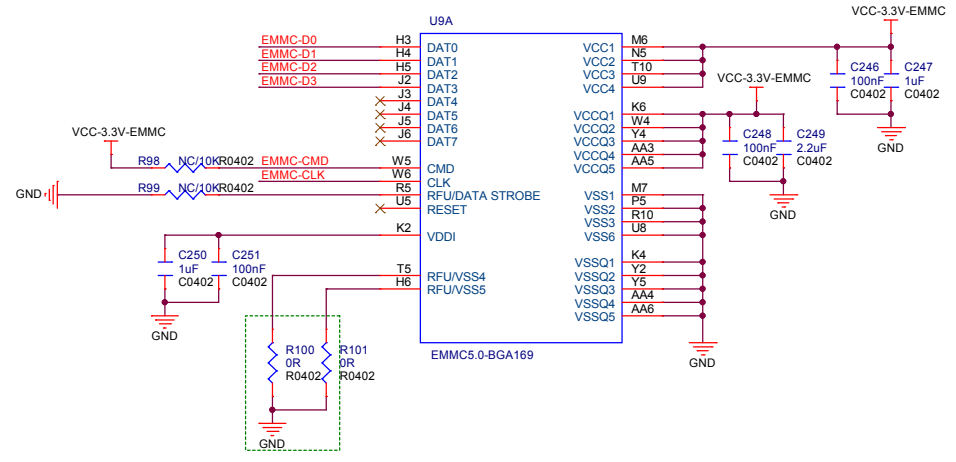
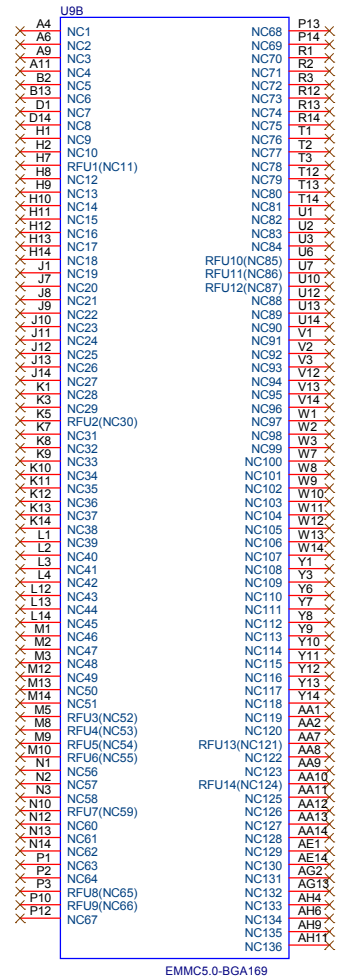


# Flash

# SPI FLASH



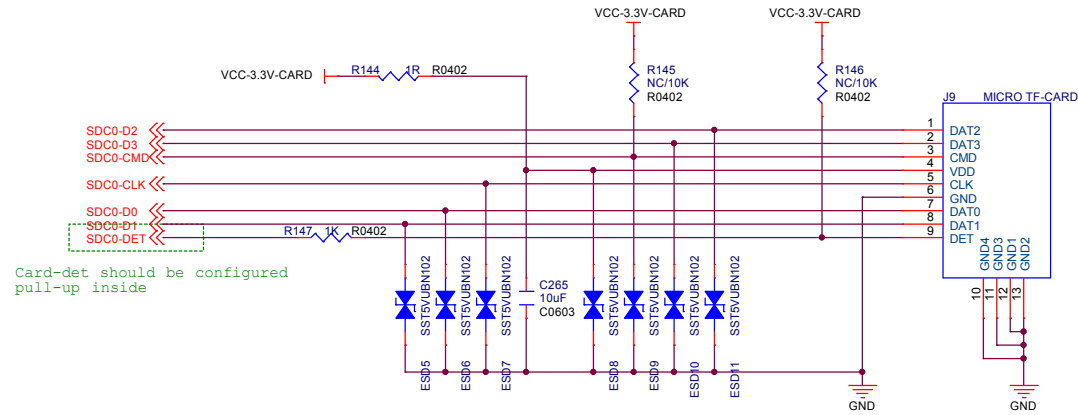
# EMMC



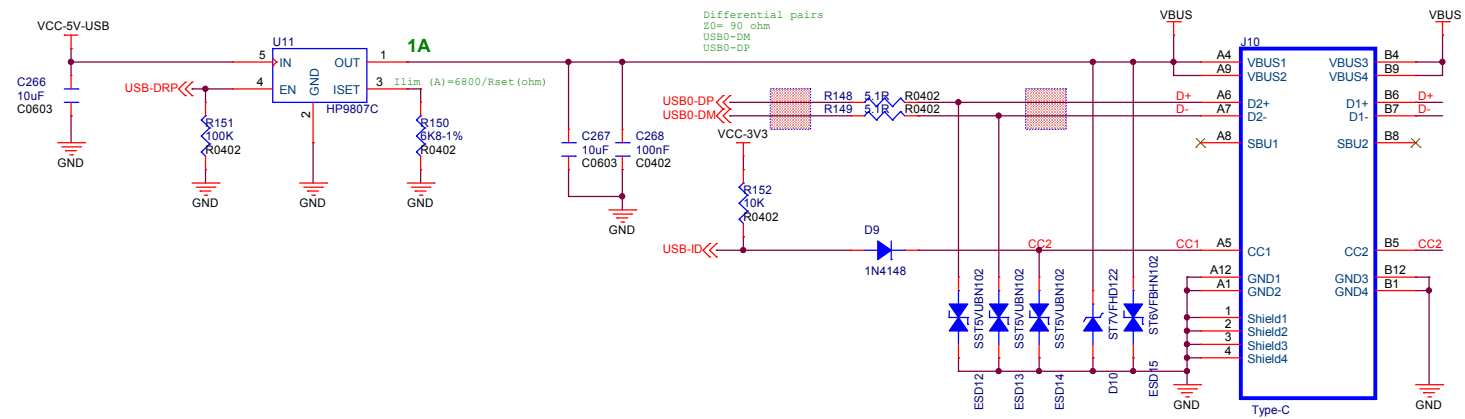
If EMMC is not v5.0/v5.1, then NC this two resistors.



# SD CARD



# USB

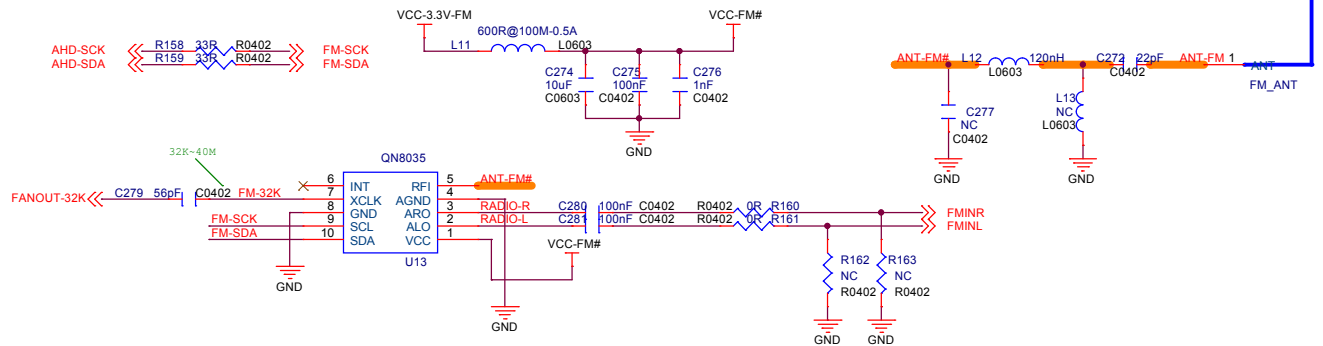


90 ohm

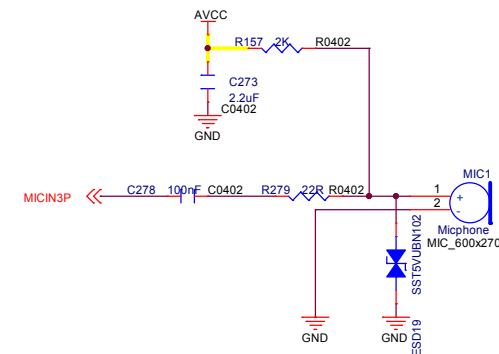


# FM

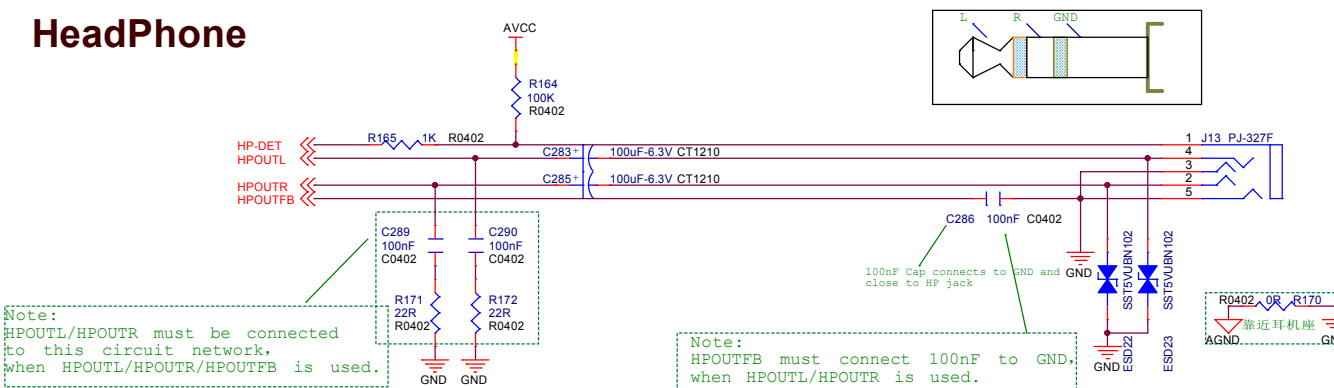
## Layout: RF 50ohm Line Width



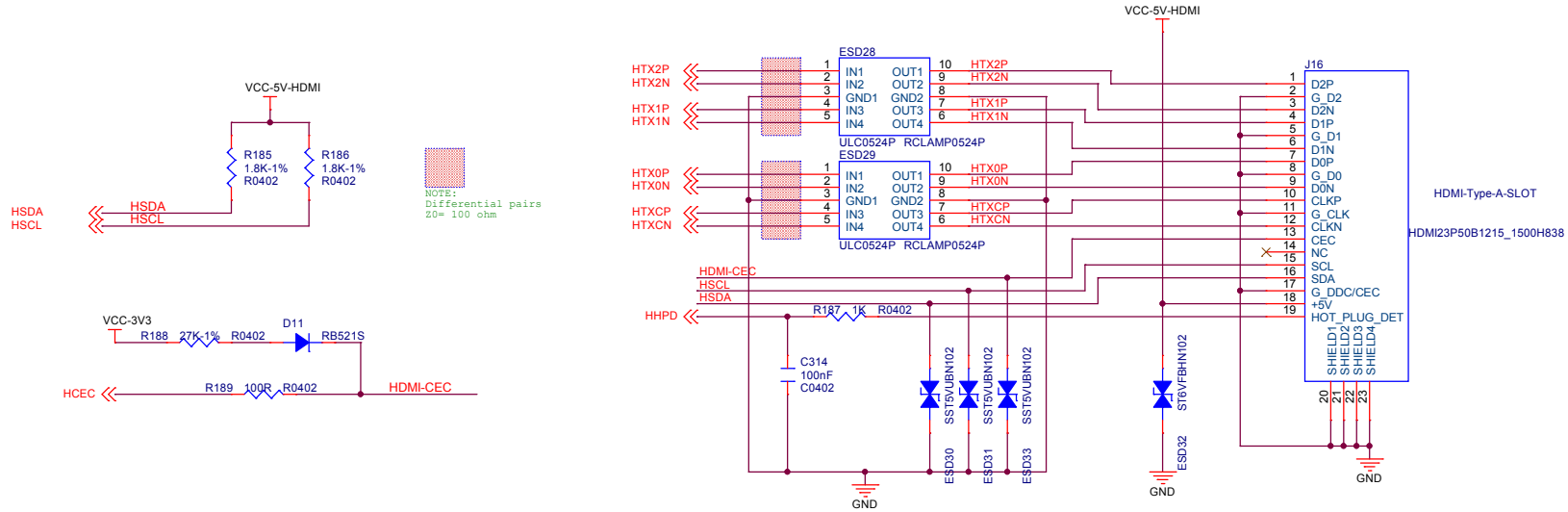
# MIC



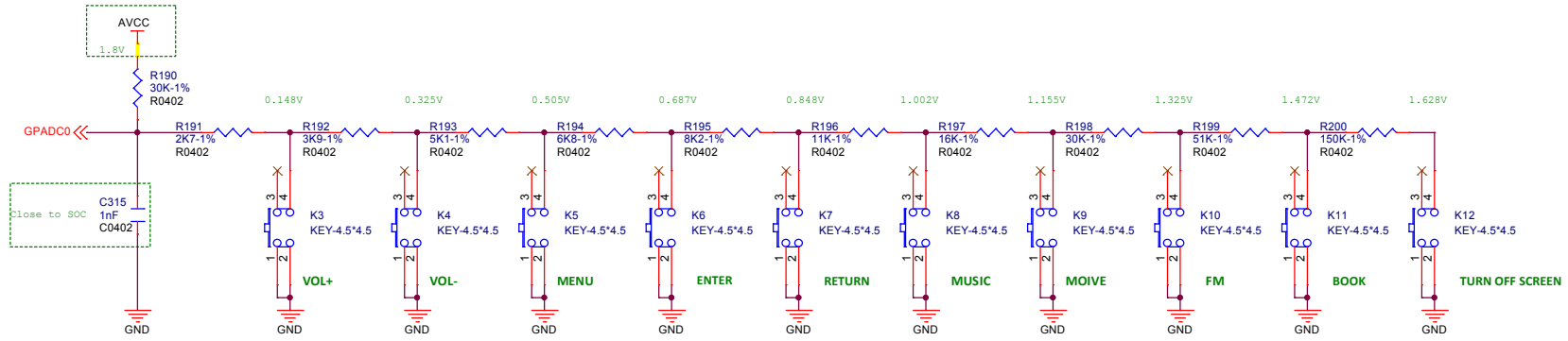
# HeadPhone



# HDMI



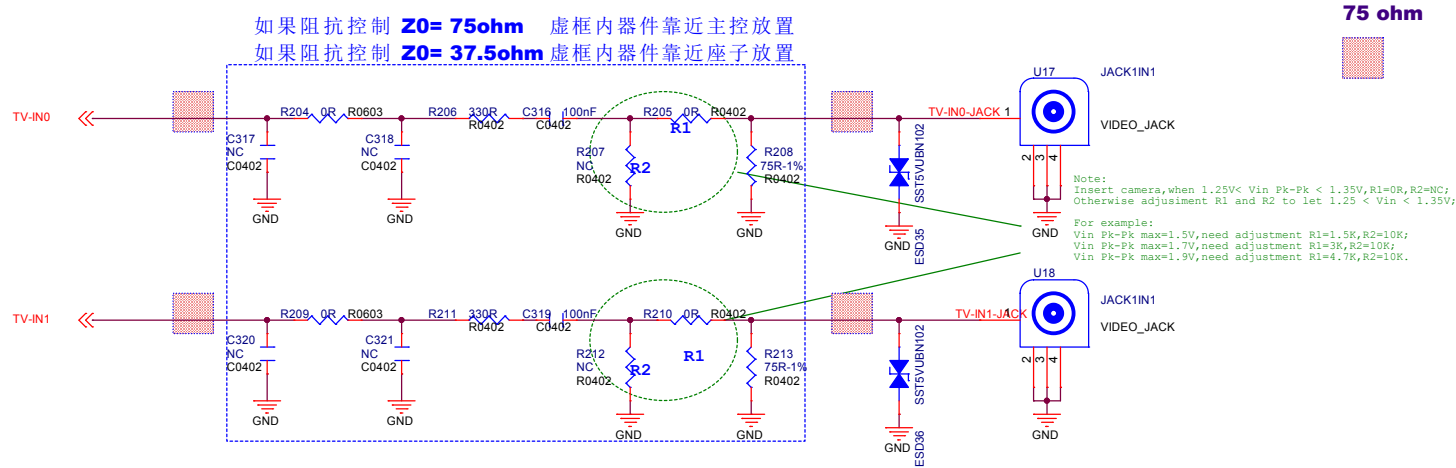
# KEY



# TV OUT

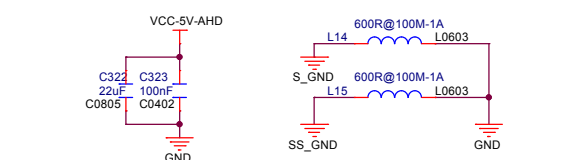


# TV IN

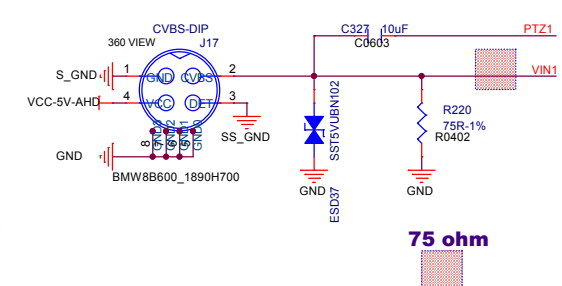


Note:  
Insert camera, when  $1.25V < V_{in} Pk-Pk < 1.35V$ ,  $R1=0R$ ,  $R2=NC$ ;  
Otherwise adjustment  $R1$  and  $R2$  to let  $1.25 < V_{in} < 1.35V$ ;  
For example:  
 $V_{in} Pk-Pk \text{ max}=1.5V$ , need adjustment  $R1=1.5K$ ,  $R2=10K$ ;  
 $V_{in} Pk-Pk \text{ max}=1.7V$ , need adjustment  $R1=3R$ ,  $R2=10K$ ;  
 $V_{in} Pk-Pk \text{ max}=1.9V$ , need adjustment  $R1=4.7K$ ,  $R2=10K$ .

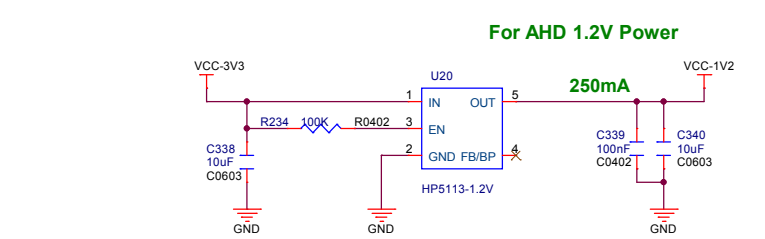
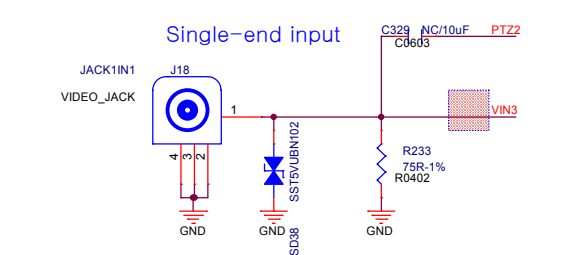
# AHD CAMERA



Single-end input

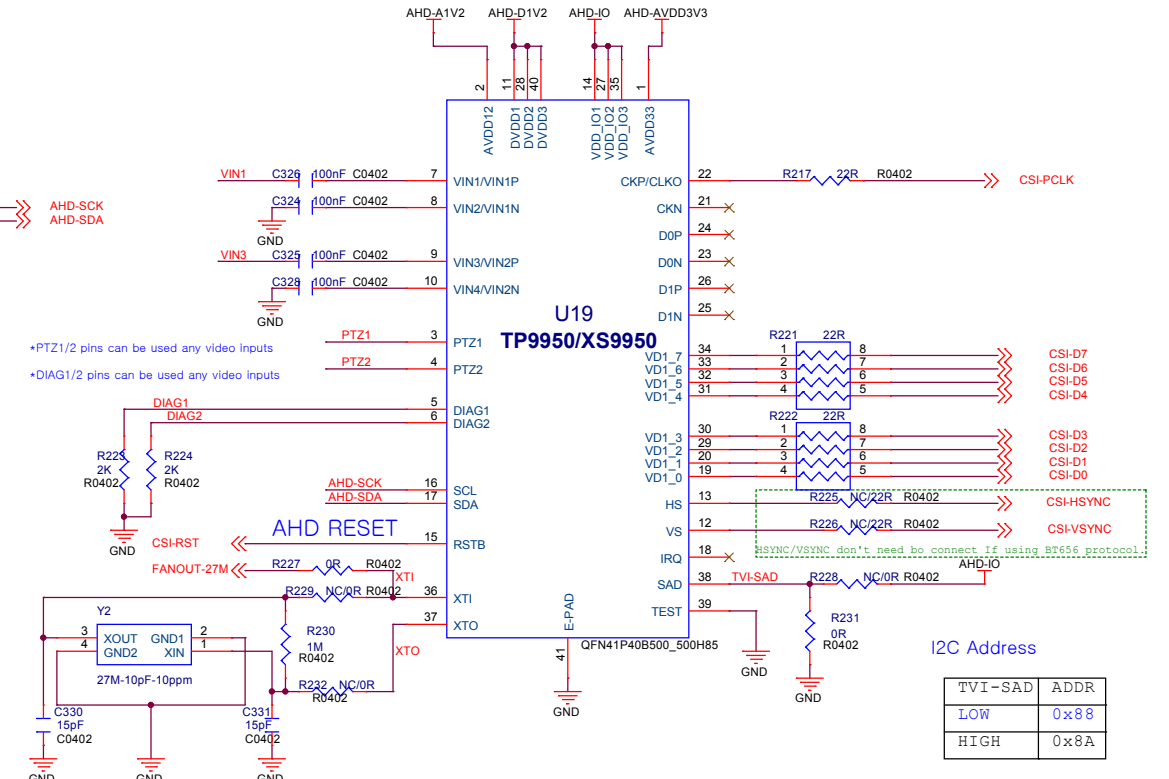
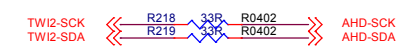
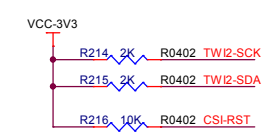


75 ohm



For AHD 1.2V Power

250mA

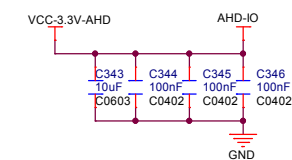
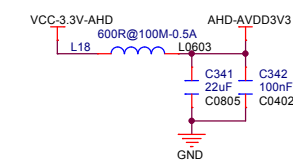
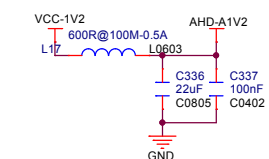
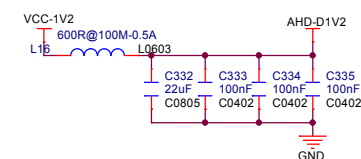


+PTZ1/2 pins can be used any video inputs  
+DIAG1/2 pins can be used any video inputs

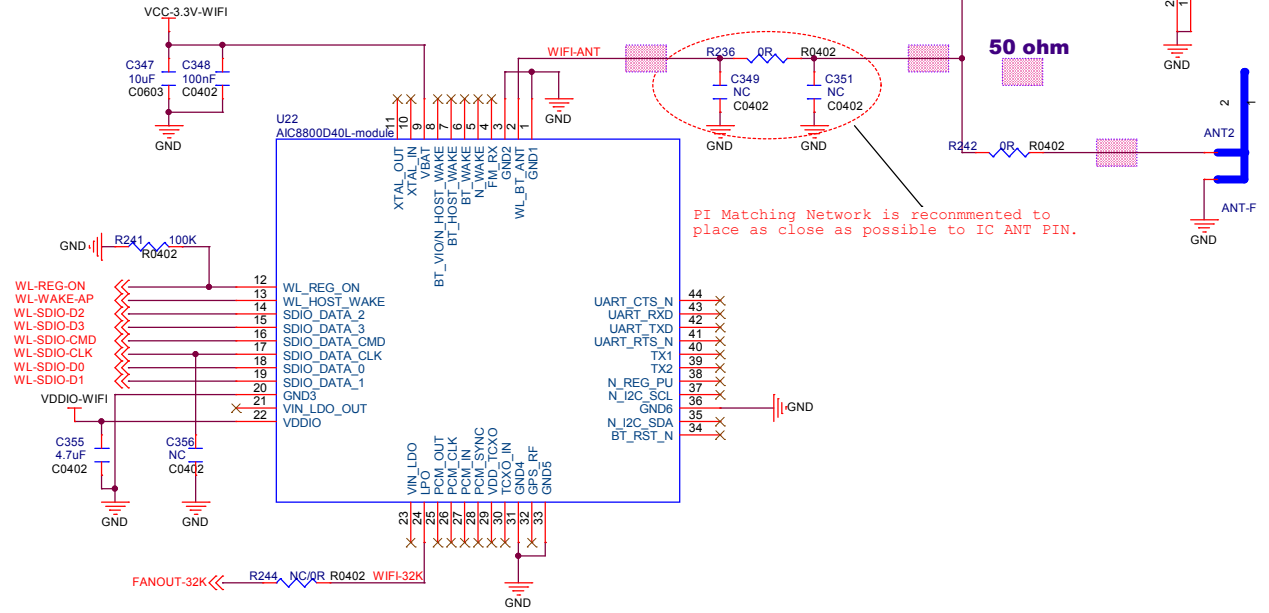
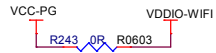
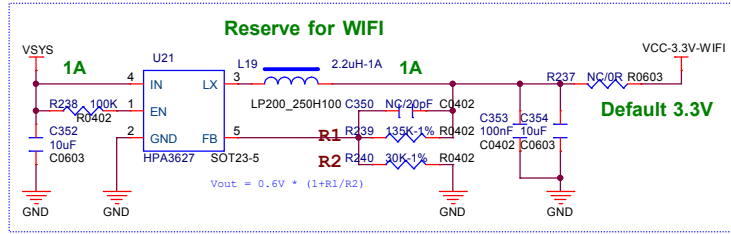
HSYNC/VSYNC don't need to connect if using BT656 protocol

I2C Address

TVI-SAD	ADDR
LOW	0x88
HIGH	0x8A

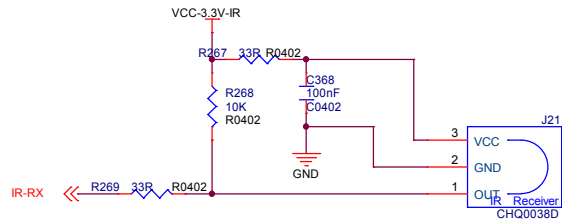


# WIFI MODULE





# IR-RX



# IIS DAC

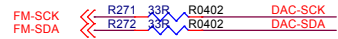
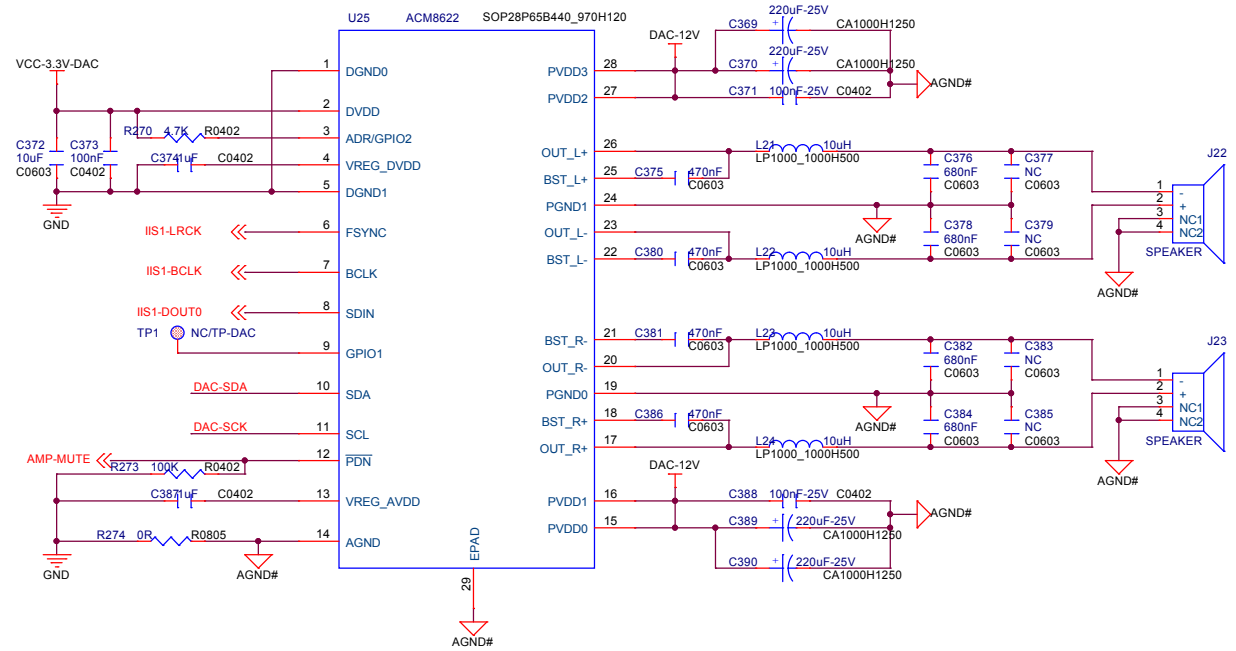
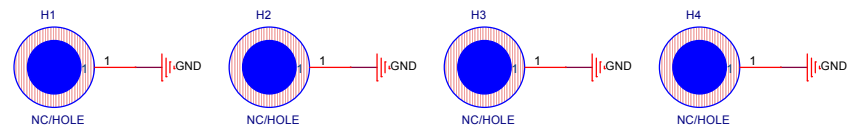
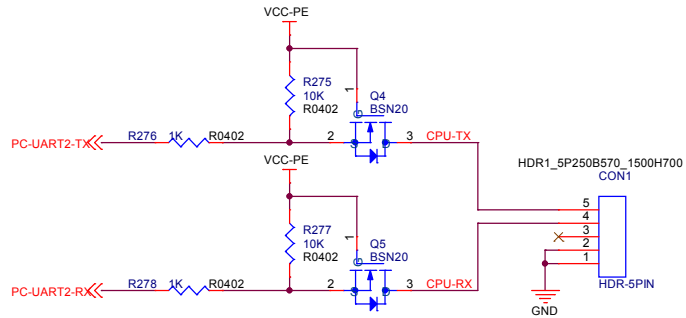


Table 5 I<sup>2</sup>C Device Address Configuration

ADR PIN Configuration	MSBs	User Define	LSB	Device Write Address
4.7kΩ to DVDD	0 0 0 1 1	0 0	R/W	0x18
15kΩ to DVDD	0 0 0 1 1	0 1	R/W	0x1a
47kΩ to DVDD	0 0 0 1 1	1 0	R/W	0x1c
120kΩ to DVDD	0 0 0 1 1	1 1	R/W	0x1e



# CPU DEBUG



	<b>AllWinner Technology Co., Ltd</b>	
	Design Name: <b>F133 MX-HXX_STD_V1_0</b>	
	Size: A3	Page Name: <b>18 IR IIS URAT</b>
	Date: Friday, November 01, 2024	Sheet: 18 of 18