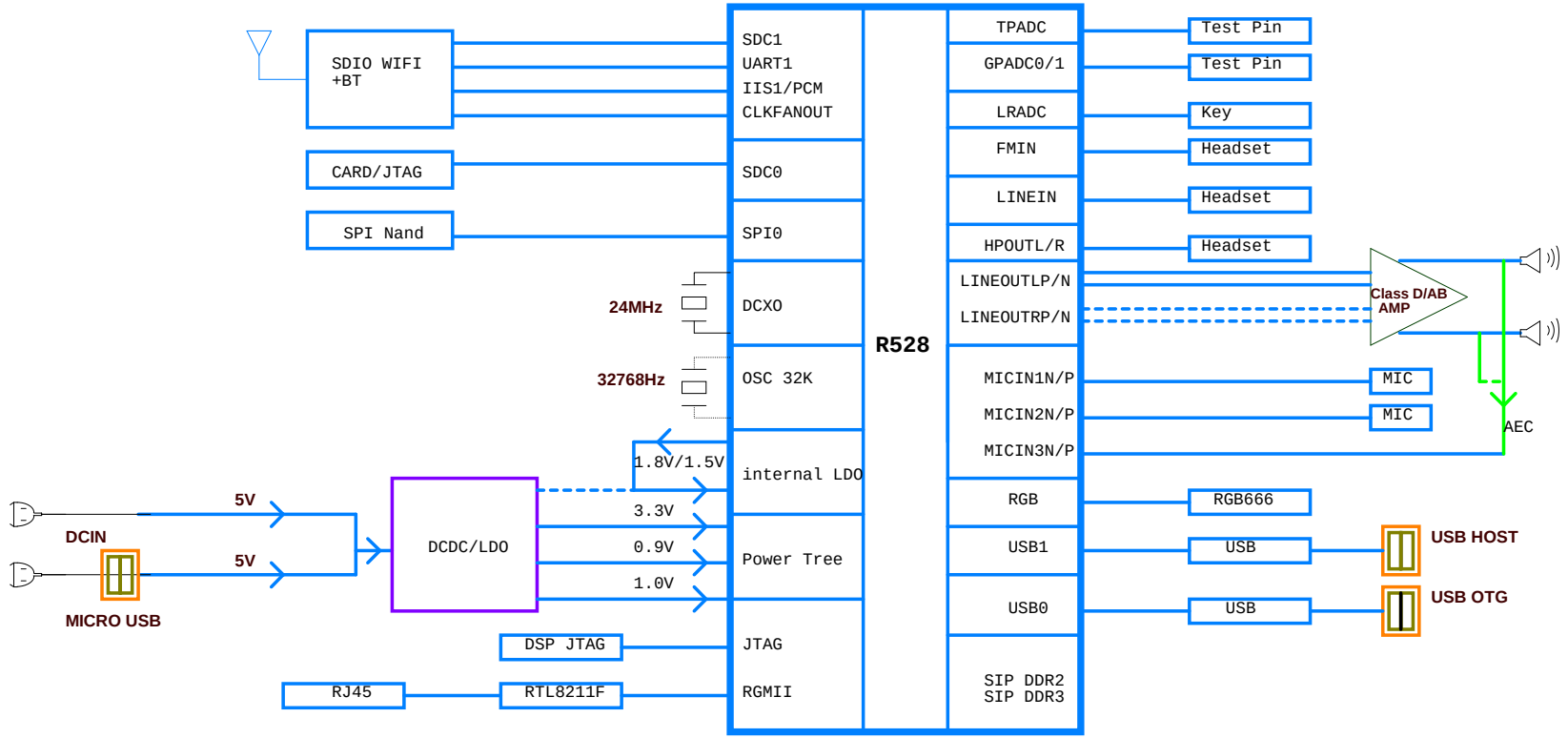
VERSION HISTORY

Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Releas version	2021-10-28			
Ver 1.1	Releas version	2022-03-24			
Ver 1.2	Releas version	2022-05-30			

Index:

Option

BLOCK

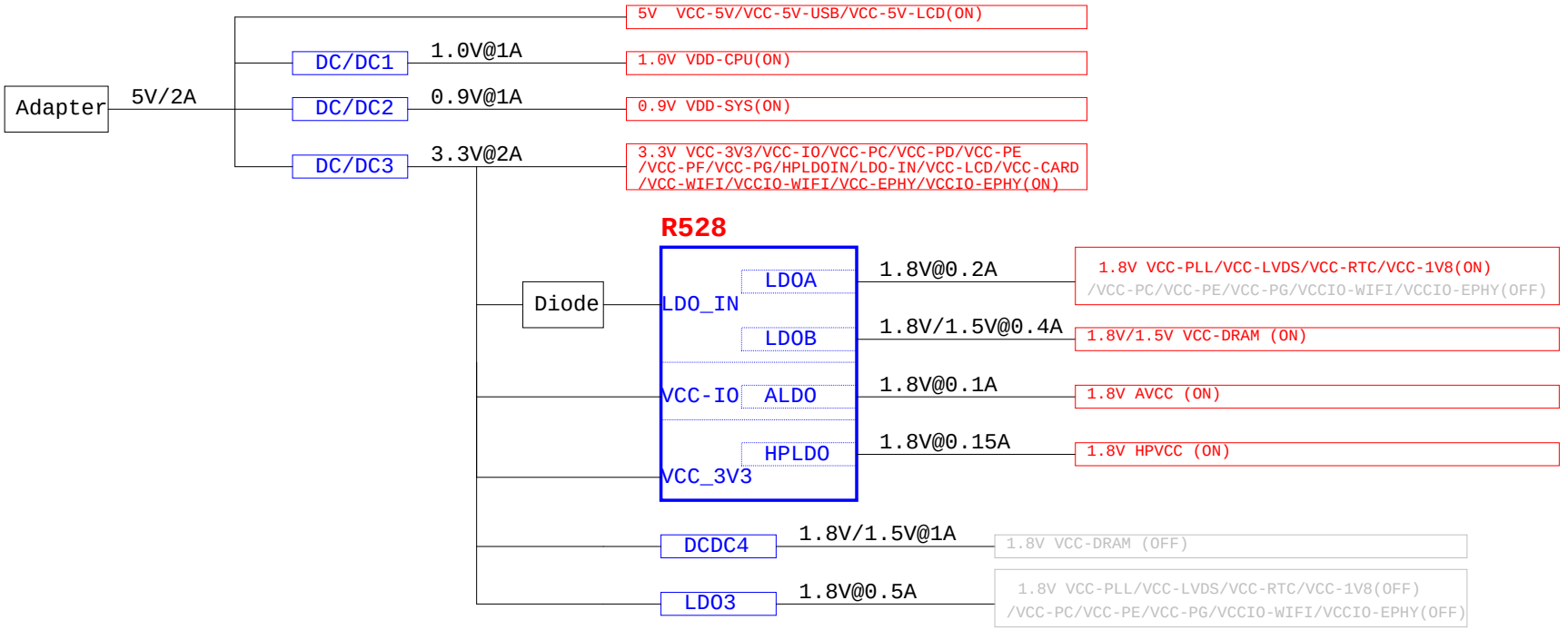


AllWinner Technology Co.,Ltd		
Design Name: R528_STD_V1_2		
Size: A3	Page Name: 02 BLOCK DIAGRAM	Rev
Date: Monday, May 30, 2022	Sheet 2 of 17	

POWER TREE

DEFAULT POWER ON

DEFAULT POWER OFF



AllWinner Technology Co.,Ltd		
Design Name: R528_STD_V1_2		
Size: A3	Page Name: 03 POWER TREE	Rev
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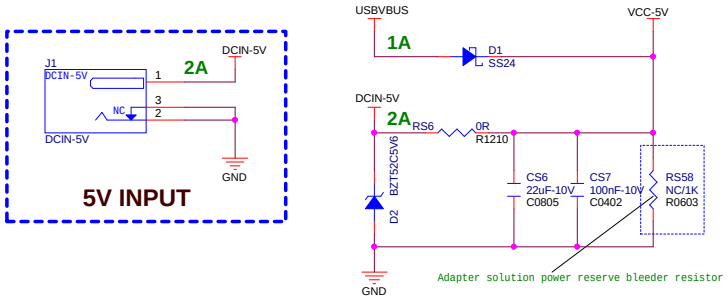
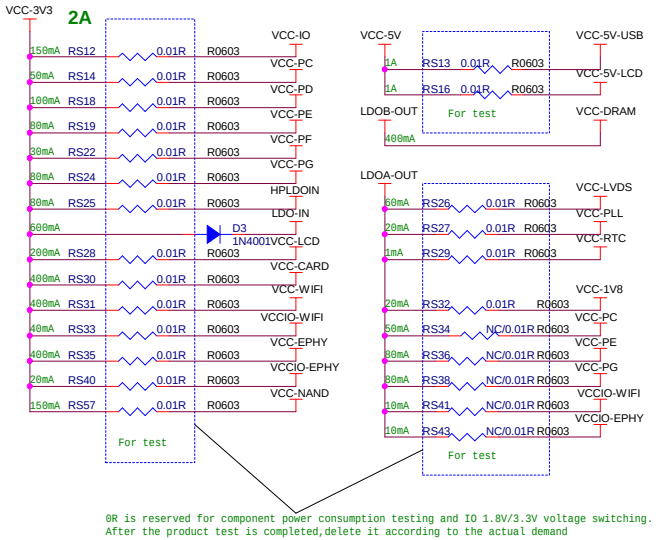
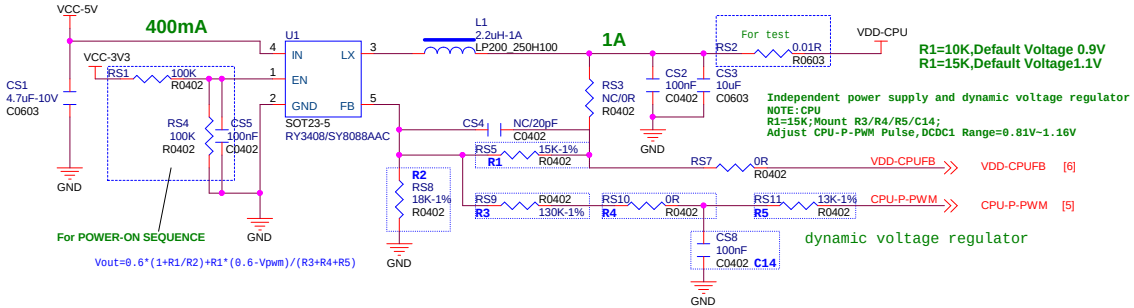
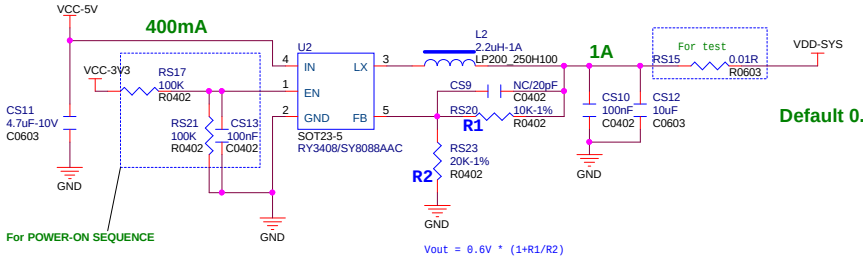
POWER

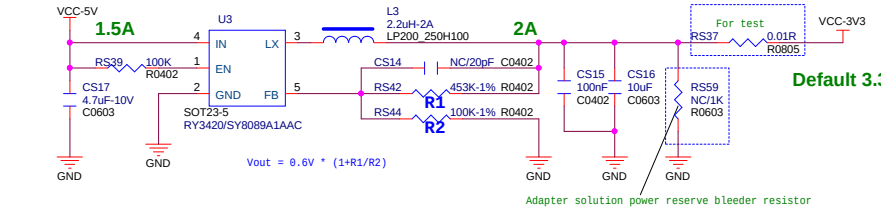




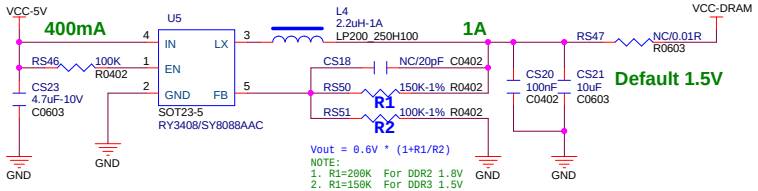


Notice
If PWM dynamic voltage regulation is not used,
please contact FAE to obtain the default voltage of VDD-CPU.

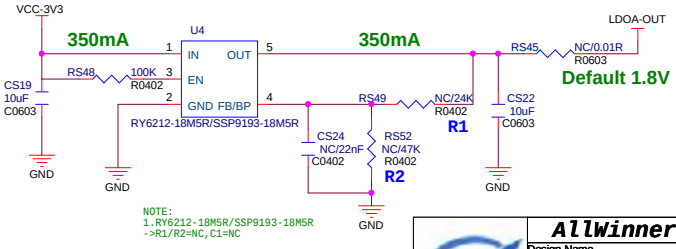




Option



Option



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SOC1

Notice:
The PC/PF port has Flash and SD Card functions.When Soc starts,it will try various media,and will send clock and command signals,etc;
When designing the schematic,do not place the enable or control signal of acoustics,optics,electricity on the PC/PF port to avoid uncontrolled peripherals,such as the LED flashes or the PA has pop sound.

U6C — PC

R528-BGA226

PC0/UART2_TX/TWI2_SCK/LEDC_DO/PC_EINT0	L3		UART2-TX	UART2-TX [14]
PC1/UART2_RX/TWI2_SDA/PC_EINT1	L2		UART2-RX	UART2-RX [14]
PC2/SPI0_CLK/SDC2_CLK/PC_EINT2	L1	R1 33R R0402	SPI0-CLK eMMC-CLK	
PC3/SPI0_CS0/SDC2_CMD/PC_EINT3	M3	close to soc	SPI0-CS0 eMMC-CMD	
PC4/SPI0_MOSI/SDC2_D2/BOOT_SEL0/PC_EINT4	M2		SPI0-MOSI eMMC-D2	
PC5/SPI0_MISO/SDC2_D1/BOOT_SEL1/PC_EINT5	N3		SPI0-MISO eMMC-D1	
PC6/SPI0_WP/SDC2_D0/UART3_TX/TWI3_SCK/DBG_CLK/PC_EINT6	N2		SPI0-WP eMMC-D0	
PC7/SPI0_HOLD/SDC2_D3/UART3_RX/TWI3_SDA/TCON_TRIG/PC_EINT7	N1		SPI0-HOLD eMMC-D3	
VCC_PC	F5		VCC-PC	

U6F — PF

R528-BGA226

PF0/SDC0_D1/JTAG_MS/R_JTAG_MS/I2S2_DOUT1/I2S2_DIN0/PF_EINT0	G1	SDC0-D1
PF1/SDC0_D0/JTAG_DI/R_JTAG_DI/I2S2_DOUT0/I2S2_DIN1/PF_EINT1	H3	SDC0-D0
PF2/SDC0_CLK/UART0_TX/TWI0_SCK/PF_EINT2	J3	SDC0-CLK
PF3/SDC0_CMD/JTAG_DO/R_JTAG_DO/I2S2_BCLK/PF_EINT3	J2	SDC0-CMD
PF4/SDC0_D3/UART0_RX/TWI0_SDA/PWM6/IR_TX/PF_EINT4	J1	SDC0-D3
PF5/SDC0_D2/JTAG_CK/R_JTAG_CK/I2S2_LRCK/PF_EINT5	K3	SDC0-D2
PF6/SPDIF_OUT/IR_RX/I2S2_MCLK/PWM5/PF_EINT6	K2	SDC0-DET
VCC_PF	E6	VCC-PF

U6B — PB

R528-BGA226

PB0/PWM3/IR_TX/TWI2_SCK/SPI1_WP/DBI_TE/UART0_TX/UART2_TX/SPDIF_OUT/PB_EINT0	D16	CTP-SCK	CTP-SCK [8]
PB1/PWM4/I2S2_DOUT3/TWI2_SDA/I2S2_DIN3/UART0_RX/UART2_RX/IR_RX/PB_EINT1	D17	CTP-SDA	CTP-SDA [8]
PB2/LCD0_D0/I2S2_DOUT2/TWI0_SDA/I2S2_DIN2/LCD0_D18/UART4_TX/PB_EINT2	M16	PA-SHDN	PA-SHDN [9]
PB3/LCD0_D1/I2S2_DOUT1/TWI0_SCK/I2S2_DIN0/LCD0_D19/UART4_RX/PB_EINT3	M17	USB0-DRVVBUS	USB0-DRVVBUS [11]
PB4/LCD0_D8/I2S2_DOUT0/TWI1_SCK/I2S2_DIN1/LCD0_D20/UART5_TX/PB_EINT4	M18	CTP-RST	CTP-RST [8]
PB5/LCD0_D9/I2S2_BCLK/TWI1_SDA/PWM0/LCD0_D21/UART5_RX/PB_EINT5	L16	CPU-P-PWM	CPU-P-PWM [4]
PB6/LCD0_D16/I2S2_LRCK/TWI3_SCK/PWM1/LCD0_D22/UART3_TX/CPUBIST0/PB_EINT6	L17	CTP-INT	CTP-INT [8]
PB7/LCD0_D17/I2S2_MCLK/TWI3_SDA/IR_RX/LCD0_D23/UART3_RX/CPUBIST1/PB_EINT7	K16	IR-RX	IR-RX [14]
PB8/DMIC_DATA3/PWM5/TWI2_SCK/SPI1_HOLD/DBI_DCX/DBI_WRX/UART0_TX/UART1_TX/PB_EINT8	D18	USB0-VBUSDET	USB0-VBUSDET [11]
PB9/DMIC_DATA2/PWM6/TWI2_SDA/SPI1_MISO/DBI_SDI/DBI_TE/DBI_DCX/UART0_RX/UART1_RX/PB_EINT9	C16	USB-ID	USB-ID [11]
PB10/DMIC_DATA1/PWM7/TWI0_SCK/SPI1_MOSI/DBI_SDO/CLK_FANOUT0/UART1_RTS/PB_EINT10	C18	LCD0-PIO0	
PB11/DMIC_DATA0/PWM2/TWI0_SDA/SPI1_CLK/DBI_SCLK/CLK_FANOUT1/UART1_CTS/PB_EINT11	C17	LCD0-PIO1	
PB12/DMIC_CLK/PWM0/SPI1_CS/DBI_CSX/CLK_FANOUT2/IR_RX/PB_EINT12	B18	USB-DRVVBUS1	USB-DRVVBUS1 [11]
VCC_IO	G13	VCC-IO	

SD Card function R2 close to soc
UART0 function R2 can delete

SPI0-CLK	SPI0-CLK [7]	SDC0-D1	SDC0-D1 [11]
SPI0-CS0	SPI0-CS0 [7]	SDC0-D0	SDC0-D0 [11]
SPI0-MOSI	SPI0-MOSI [7]	SDC0-CLK R2 33R R0402 S-SDC0-CLK	S-SDC0-CLK [11]
SPI0-MISO	SPI0-MISO [7]	SDC0-CMD	SDC0-CMD [11]
SPI0-WP	SPI0-WP [7]	SDC0-D3	SDC0-D3 [11]
SPI0-HOLD	SPI0-HOLD [7]	SDC0-D2	SDC0-D2 [11]
		SDC0-DET	SDC0-DET [11]
eMMC-CLK	eMMC-CLK [7]		
eMMC-CMD	eMMC-CMD [7]		
eMMC-D2	eMMC-D2 [7]	S-SDC0-CLK UART0-TX	UART0-TX [14]
eMMC-D1	eMMC-D1 [7]	SDC0-D3 UART0-RX	UART0-RX [14]
eMMC-D0	eMMC-D0 [7]		
eMMC-D3	eMMC-D3 [7]		

U6D — PD

R528-BGA226

PD0/LCD0_D2/LVDS0_V0P/DSI_D0P/TWI0_SCK/PD_EINT0	T12	DSI-D0P	LVDS0-V0P LCD0-D2
PD1/LCD0_D3/LVDS0_V0N/DSI_D0N/UART2_TX/PD_EINT1	U12	DSI-D0N	LVDS0-V0N LCD0-D3
PD2/LCD0_D4/LVDS0_V1P/DSI_D1P/UART2_RX/PD_EINT2	U13	DSI-D1P	LVDS0-V1P LCD0-D4
PD3/LCD0_D5/LVDS0_V1N/DSI_D1N/UART2_RTS/PD_EINT3	V13	DSI-D1N	LVDS0-V1N LCD0-D5
PD4/LCD0_D6/LVDS0_V2P/DSI_CKP/UART2_CTS/PD_EINT4	T14	DSI-CKP	LVDS0-V2P LCD0-D6
PD5/LCD0_D7/LVDS0_V2N/DSI_CKN/UART5_TX/PD_EINT5	U14	DSI-CKN	LVDS0-V2N LCD0-D7
PD6/LCD0_D10/LVDS0_CKP/DSI_D2P/UART5_RX/PD_EINT6	U15	DSI-D2P	LVDS0-CKP LCD0-D10
PD7/LCD0_D11/LVDS0_CKN/DSI_D2N/UART4_TX/PD_EINT7	V15	DSI-D2N	LVDS0-CKN LCD0-D11
PD8/LCD0_D12/LVDS0_V3P/DSI_D3P/UART4_RX/PD_EINT8	U16	DSI-D3P	LVDS0-V3P LCD0-D12
PD9/LCD0_D13/LVDS0_V3N/DSI_D3N/PWM6/PD_EINT9	V16	DSI-D3N	LVDS0-V3N LCD0-D13
PD10/LCD0_D14/LVDS1_V0P/SPI1_CS/DBI_CSX/UART3_TX/PD_EINT10	U17		LVDS1-V0P LCD0-D14
PD11/LCD0_D15/LVDS1_V0N/SPI1_CLK/DBI_SCLK/UART3_RX/PD_EINT11	U18		LVDS1-V0N LCD0-D15
PD12/LCD0_D18/LVDS1_V1P/SPI1_MOSI/DBI_SDO/TWI0_SDA/PD_EINT12	T17		LVDS1-V1P LCD0-D18
PD13/LCD0_D19/LVDS1_V1N/SPI1_MISO/DBI_SDI/DBI_TE/DBI_DCX/UART3_RTS/PD_EINT13	T18		LVDS1-V1N LCD0-D19
PD14/LCD0_D20/LVDS1_V2P/SPI1_HOLD/DBI_DCX/DBI_WRX/UART3_CTS/PD_EINT14	R16		LVDS1-V2P LCD0-D20
PD15/LCD0_D21/LVDS1_V2N/SPI1_WP/DBI_TE/IR_RX/PD_EINT15	R17		LVDS1-V2N LCD0-D21
PD16/LCD0_D22/LVDS1_CKP/DMIC_DATA3/PWM0/PD_EINT16	P17		LVDS1-CKP LCD0-D22
PD17/LCD0_D23/LVDS1_CKN/DMIC_DATA2/PWM1/PD_EINT17	P18		LVDS1-CKN LCD0-D23
PD18/LCD0_CLK/LVDS1_V3P/DMIC_DATA1/PWM2/PD_EINT18	N16		LVDS1-V3P LCD0-CLK
PD19/LCD0_DE/LVDS1_V3N/DMIC_DATA0/PWM3/PD_EINT19	N17		LVDS1-V3N LCD0-DE
PD20/LCD0_HSYNC/TWI2_SCK/DMIC_CLK/PWM4/PD_EINT20	V11		LVDS0-BL-EN0 LCD0-HSYNC
PD21/LCD0_VSYNC/TWI2_SDA/UART1_TX/PWM5/PD_EINT21	U11	DSI-RESET	LVDS1-BL-EN1 LCD0-VSYNC
PD22/SPDIF_OUT/IR_RX/UART1_RX/PWM7/PD_EINT22	T11	BL-PWM	
VCC_LVDS	K13	VCC-LVDS	
VCC_PD	H13	VCC-PD	

DSI option

DSI-D0P	DSI-D0P	[8]
DSI-D0N	DSI-D0N	[8]
DSI-D1P	DSI-D1P	[8]
DSI-D1N	DSI-D1N	[8]
DSI-CKP	DSI-CKP	[8]
DSI-CKN	DSI-CKN	[8]
DSI-D2P	DSI-D2P	[8]
DSI-D2N	DSI-D2N	[8]
DSI-D3P	DSI-D3P	[8]
DSI-D3N	DSI-D3N	[8]
DSI-RESET	DSI-RESET	[8]
BL-PWM	BL-PWM	[5,8]

LVDS option

LVDS0-V0P	LVDS0-V0P	[8]
LVDS0-V0N	LVDS0-V0N	[8]
LVDS0-V1P	LVDS0-V1P	[8]
LVDS0-V1N	LVDS0-V1N	[8]
LVDS0-V2P	LVDS0-V2P	[8]
LVDS0-V2N	LVDS0-V2N	[8]
LVDS0-CKP	LVDS0-CKP	[8]
LVDS0-CKN	LVDS0-CKN	[8]
LVDS0-V3P	LVDS0-V3P	[8]
LVDS0-V3N	LVDS0-V3N	[8]
LVDS0-BL-EN0	LVDS0-BL-EN0	[8]
BL-PWM	BL-PWM	[5,8]

Default RGB666

LCD0-D2	LCD0-D2	[8]
LCD0-D3	LCD0-D3	[8]
LCD0-D4	LCD0-D4	[8]
LCD0-D5	LCD0-D5	[8]
LCD0-D6	LCD0-D6	[8]
LCD0-D7	LCD0-D7	[8]
LCD0-D10	LCD0-D10	[8]
LCD0-D11	LCD0-D11	[8]
LCD0-D12	LCD0-D12	[8]
LCD0-D13	LCD0-D13	[8]
LCD0-D14	LCD0-D14	[8]
LCD0-D15	LCD0-D15	[8]
LCD0-D18	LCD0-D18	[8]
LCD0-D19	LCD0-D19	[8]
LCD0-D20	LCD0-D20	[8]
LCD0-D21	LCD0-D21	[8]
LCD0-D22	LCD0-D22	[8]
LCD0-D23	LCD0-D23	[8]
LCD0-CLK	LCD0-CLK	[8]
LCD0-DE	LCD0-DE	[8]
LCD0-HSYNC	LCD0-HSYNC	[8]
LCD0-VSYNC	LCD0-VSYNC	[8]
BL-PWM	BL-PWM	[5,8]
LCD0-PIO0	LCD0-PIO0	[8]
LCD0-PIO1	LCD0-PIO1	[8]

Notice:
When the differential pair of the PD port is used as a common GPIO:
If a pull-up resistor is added to the N pin, the corresponding P pin will have a 1V glitch
at the moment of power-on caused by leakage,and vice versa.
Pay attention when enabling sound and light peripherals such as LEDs.

U6E — PE

R528-BGA226

PE0/NCSI0_HSYNC/UART2_RTS/TWI1_SCK/LCD0_HSYNC/RGMII_RXCTRL/RMII_CRS_DV/PE_EINT0	V9		RGMII-RXCTL [12]
PE1/NCSI0_VSYNC/UART2_CTS/TWI1_SDA/LCD0_VSYNC/RGMII_RXD0/RMII_RXD0/PE_EINT1	U9		RGMII-RXD0 [12]
PE2/NCSI0_PCLK/UART2_TX/TWI0_SCK/CLK_FANOUT0/UART0_TX/RGMII_RXD1/RMII_RXD1/PE_EINT2	T9		RGMII-RXD1 [12]
PE3/NCSI0_MCLK/UART2_RX/TWI0_SDA/CLK_FANOUT1/UART0_RX/RGMII_TXCK/RMII_TXCK/PE_EINT3	T8		RGMII-TXCK [12]
PE4/NCSI0_D0/UART4_TX/TWI2_SCK/CLK_FANOUT2/D_JTAG_MS/R_JTAG_MS/RGMII_TXD0/RMII_TXD0/PE_EINT4	V7	D-JTAG-MS	RGMII-TXD0 [12]
PE5/NCSI0_D1/UART4_RX/TWI2_SDA/LEDC_DO/D_JTAG_DI/R_JTAG_DI/RGMII_TXD1/RMII_TXD1/PE_EINT5	U7	D-JTAG-DI	RGMII-TXD1 [12]
PE6/NCSI0_D2/UART5_TX/TWI3_SCK/D_JTAG_DO/R_JTAG_DO/RGMII_TXCTRL/RMII_TXEN/PE_EINT6	T7	D-JTAG-DO	RGMII-TXCTL [12]
PE7/NCSI0_D3/UART5_RX/TWI3_SDA/SPDIF_OUT/D_JTAG_CK/R_JTAG_CK/RGMII_CLKIN/RMII_RXER/PE_EINT7	U6	D-JTAG-CK	RGMII-CLKIN [12]
PE8/NCSI0_D4/UART1_RTS/PWM2/UART3_TX/JTAG_MS/MDC/PE_EINT8	T6		RGMII-MDC [12]
PE9/NCSI0_D5/UART1_CTS/PWM3/UART3_RX/JTAG_DI/MDIO/PE_EINT9	V5		RGMII-MDIO [12]
PE10/NCSI0_D6/UART1_TX/PWM4/IR_RX/JTAG_DO/EPHY_25M/PE_EINT10	U5		EPHY-CLK-25M [12]
PE11/NCSI0_D7/UART1_RX/I2S0_DOUT3/I2S0_DIN3/JTAG_CK/RGMII_TXD2/PE_EINT11	T5		RGMII-TXD2 [12]
PE12/TWI2_SCK/NCSI0_FIELD/I2S0_DOUT2/I2S0_DIN2/RGMII_TXD3/PE_EINT12	U4		RGMII-TXD3 [12]
PE13/TWI2_SDA/PWM5/I2S0_DOUT0/I2S0_DIN1/DMIC_DATA3/RGMII_RXD2/PE_EINT13	T4		RGMII-RXD2 [12]
PE14/TWI1_SCK/D_JTAG_MS/I2S0_DOUT1/I2S0_DIN0/DMIC_DATA2/RGMII_RXD3/PE_EINT14	V3		RGMII-RXD3 [12]
PE15/TWI1_SDA/D_JTAG_DI/PWM6/I2S0_LRCK/DMIC_DATA1/RGMII_RXCK/PE_EINT15	U3		RGMII-RXCK [12]
PE16/TWI3_SCK/D_JTAG_DO/PWM7/I2S0_BCLK/DMIC_DATA0/PE_EINT16	V2		RGMII-RESET [12]
PE17/TWI3_SDA/D_JTAG_CK/IR_TX/I2S0_MCLK/DMIC_CLK/PE_EINT17	U2		WIFI-DIS [13]
VCC_PE	G6	VCC-PE	

D-JTAG-MS	TP1	D-JTAG-MS	
D-JTAG-DI	TP2	D-JTAG-DI	
D-JTAG-DO	TP3	D-JTAG-DO	
D-JTAG-CK	TP4	D-JTAG-CK	

DSP JTAG debug
If there is a series resistance in the wire,
the TP point may not be reserved to avoid
the bifurcation of the RGMI signal

SDC0-D1	JTAG-MS	TP10	JTAG-MS
SDC0-D0	JTAG-DI	TP11	JTAG-DI
SDC0-CMD	JTAG-DO	TP12	JTAG-DO
SDC0-D2	JTAG-CK	TP13	JTAG-CK

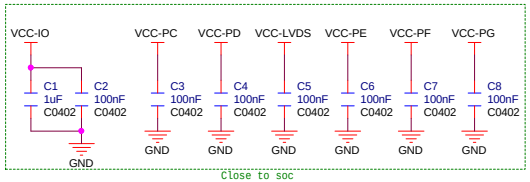
CPU JTAG debug
If there is a series resistance in the wire,
the TP point may not be reserved to avoid
signal bifurcation

U6G — PG

R528-BGA226

close to soc

PG0/SDC1_CLK/UART3_TX/RGMII_RXCTRL/RMII_CRS_DV/PWM7/PG_EINT0	A2	R3 33R R0402	SDC1-CLK	WL-SDIO-CLK [13]
PG1/SDC1_CMD/UART3_RX/RGMII_RXD0/RMII_RXD0/PWM6/PG_EINT1	C4		SDC1-CMD	WL-SDIO-CMD [13]
PG2/SDC1_D0/UART3_RTS/RGMII_RXD1/RMII_RXD1/UART4_TX/PG_EINT2	A3		SDC1-D0	WL-SDIO-D0 [13]
PG3/SDC1_D1/UART3_CTS/RGMII_TXCK/RMII_TXCK/UART4_RX/PG_EINT3	C3		SDC1-D1	WL-SDIO-D1 [13]
PG4/SDC1_D2/UART5_TX/RGMII_TXD0/RMII_TXD0/PWM5/PG_EINT4	B1		SDC1-D2	WL-SDIO-D2 [13]
PG5/SDC1_D3/UART5_RX/RGMII_TXD1/RMII_TXD1/PWM4/PG_EINT5	B2		SDC1-D3	WL-SDIO-D3 [13]
PG6/UART1_TX/TWI2_SCK/RGMII_TXD2/PWM1/PG_EINT6	E3		UART1-TX	BT-UART-RX [13]
PG7/UART1_RX/TWI2_SDA/RGMII_TXD3/PG_EINT7	E2		UART1-RX	BT-UART-TX [13]
PG8/UART1_RTS/TWI1_SCK/RGMII_RXD2/UART3_TX/PG_EINT8	E1		UART1-RTS	BT-UART-CTS [13]
PG9/UART1_CTS/TWI1_SDA/RGMII_RXD3/UART3_RX/PG_EINT9	F3		UART1-CTS	BT-UART-RTS [13]
PG10/PWM3/TWI3_SCK/RGMII_RXCK/CLK_FANOUT0/IR_RX/PG_EINT10	F2		WL-WAKE-AP	WL-WAKE-AP [13]
PG11/I2S1_MCLK/TWI3_SDA/EPHY_25M/CLK_FANOUT1/TCON_TRIG/PG_EINT11	G3		I2S1-MCLK	CLK-FANOUT1 [13]
PG12/I2S1_LRCK/TWI0_SCK/RGMII_TXCTRL/RMII_TXEN/CLK_FANOUT2/PWM0/UART1_TX/PG_EINT12	C2		I2S1-LRCK	BT-PCM-SYNC [13]
PG13/I2S1_BCLK/TWI0_SDA/RGMII_CLKIN/RMII_RXER/PWM2/LEDC_DO/UART1_RX/PG_EINT13	C1		I2S1-BCLK	BT-PCM-CLK [13]
PG14/I2S1_DIN0/TWI2_SCK/MDC/I2S1_DOUT1/SPI0_WP/UART1_RTS/PG_EINT14	D3		I2S1-DIN0	BT-PCM-DOUT [13]
PG15/I2S1_DOUT0/TWI2_SDA/MDIO/I2S1_DIN1/SPI0_HOLD/UART1_CTS/PG_EINT15	D2		I2S1-DOUT0	BT-PCM-DIN [13]
PG16/IR_RX/TCON_TRIG/PWM5/CLK_FANOUT2/LEDC_DO/PG_EINT16	G2		AP-WAKE-BT	AP-WAKE-BT [13]
PG17/UART2_TX/TWI3_SCK/PWM7/CLK_FANOUT0/IR_TX/UART0_TX/PG_EINT17	B4		BT-WAKE-AP	BT-WAKE-AP [13]
PG18/UART2_RX/TWI3_SDA/PWM6/CLK_FANOUT1/SPDIF_OUT/UART0_RX/PG_EINT18	A4		BT-RESETN	BT-RESETN [13]
VCC_PG	E5	VCC-PG		



AllWinner Technology Co.,Ltd		
Design Name	R528_STD_V1_2	
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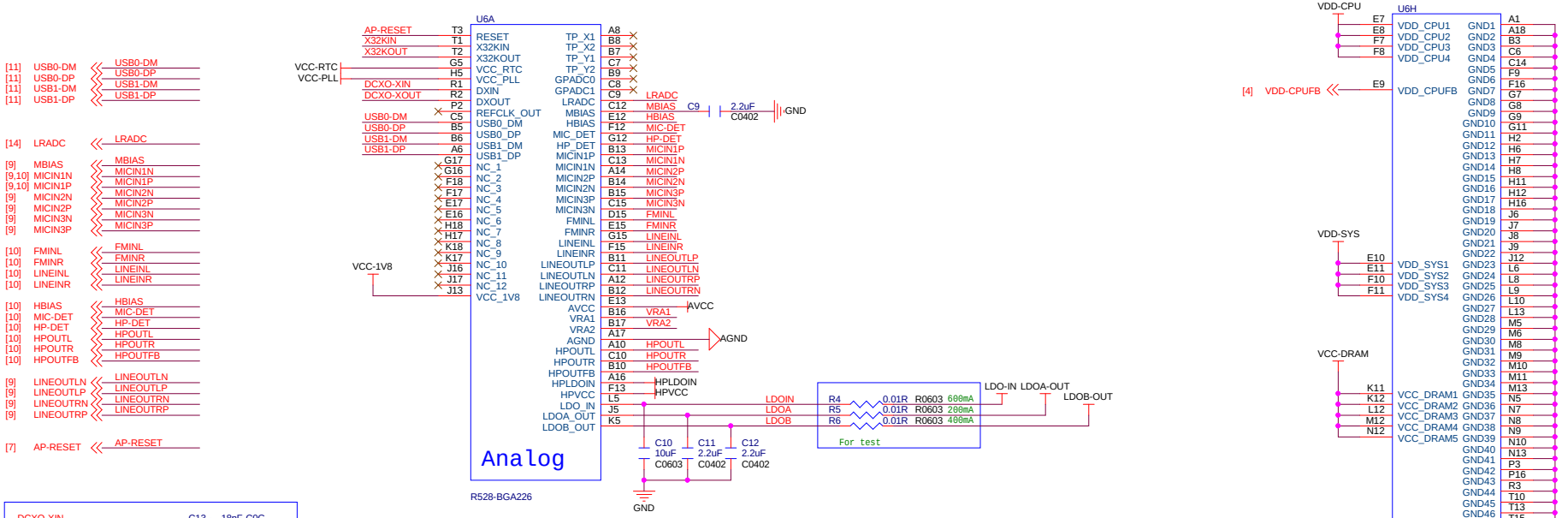
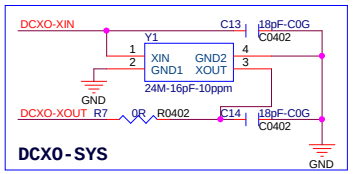
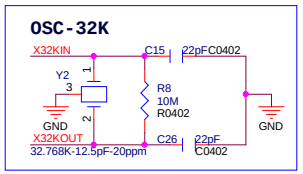
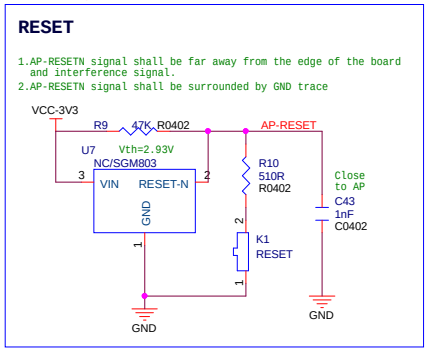
SOC2

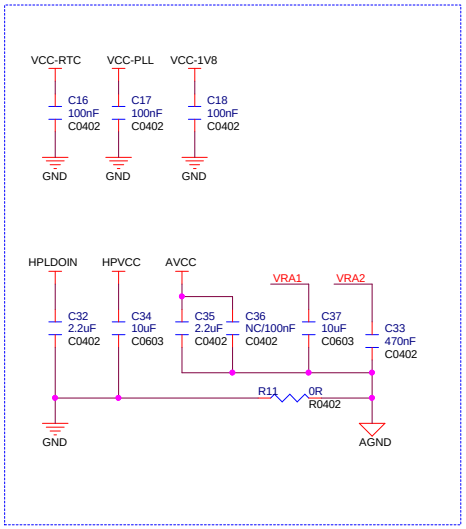


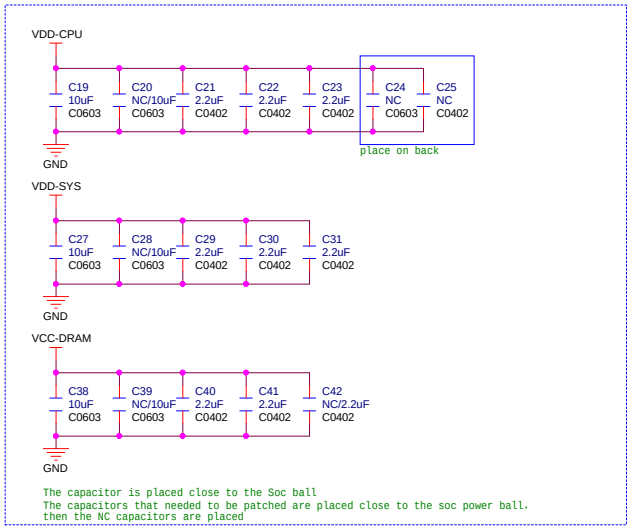




NOTE:RESET IC can NC ,
When Using SoC internal RESET Logic.







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Flash

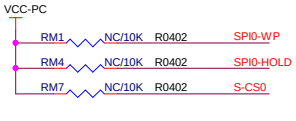
[5] SPI0-CLK — S-CLK
[5] SPI0-CS0 — S-CS0
[5] SPI0-MOSI — SPI0-MOSI
[5] SPI0-MISO — SPI0-MISO
[5] SPI0-WP — SPI0-WP
[5] SPI0-HOLD — SPI0-HOLD

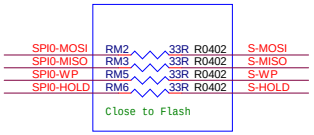
[5] eMMC-CLK — e-MMC-CLK
[5] eMMC-CMD — e-MMC-CMD
[5] eMMC-D2 — e-MMC-D2
[5] eMMC-D1 — e-MMC-D1
[5] eMMC-D0 — e-MMC-D0
[5] eMMC-D3 — e-MMC-D3

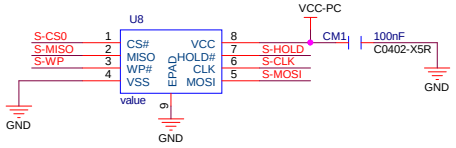
[6] AP-RESET — AP-RESET

SPI Nand

Default:use SPI NAND

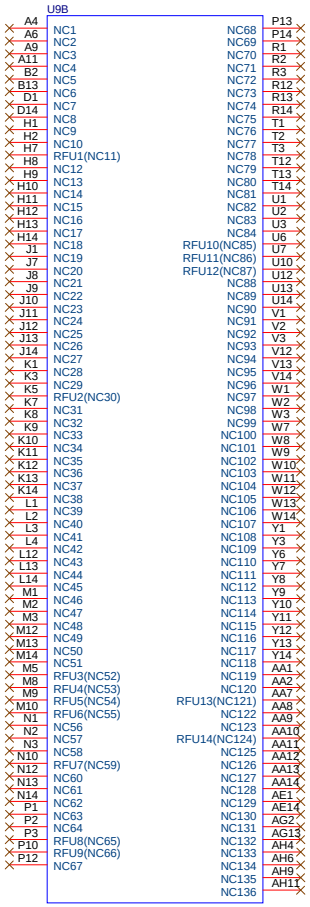


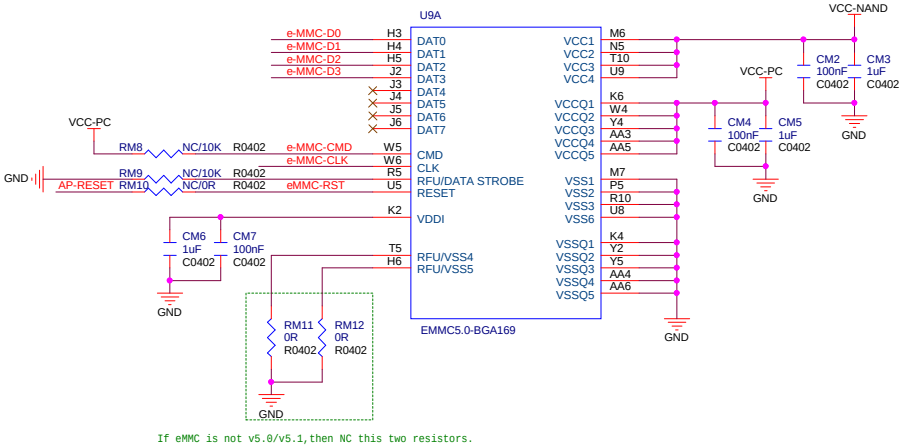




EMMC

OPTION





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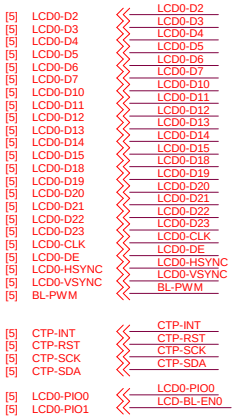
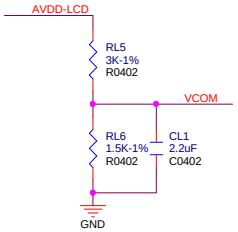
RGB666

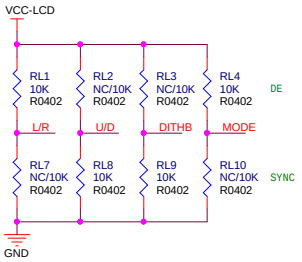


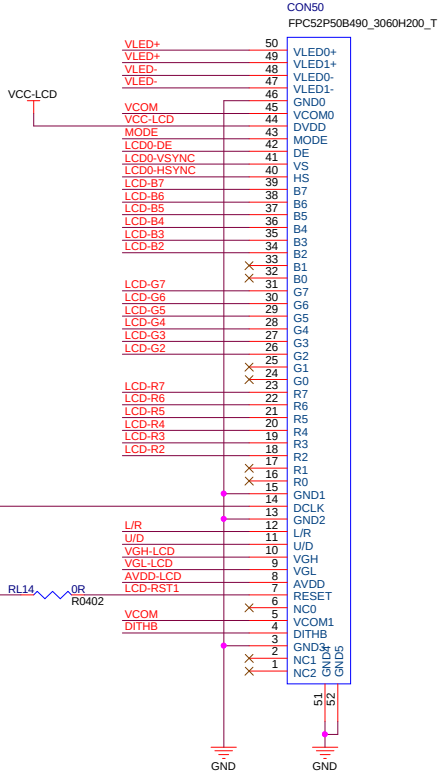
LCD0-D2	LCD-B2
LCD0-D3	LCD-B3
LCD0-D4	LCD-B4
LCD0-D5	LCD-B5
LCD0-D6	LCD-B6
LCD0-D7	LCD-B7
LCD0-D10	LCD-G2
LCD0-D11	LCD-G3
LCD0-D12	LCD-G4
LCD0-D13	LCD-G5
LCD0-D14	LCD-G6
LCD0-D15	LCD-G7
LCD0-D18	LCD-R2
LCD0-D19	LCD-R3
LCD0-D20	LCD-R4
LCD0-D21	LCD-R5
LCD0-D22	LCD-R6
LCD0-D23	LCD-R7
LCD0-PIO0	LCD-RST



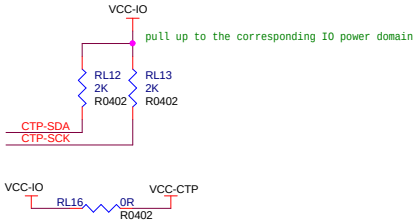
VCOM=[3.0V~3.6V]

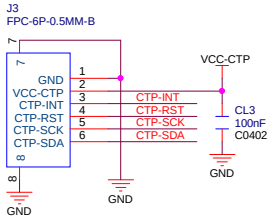
The VCOM voltage is subject to the specification voltage of the actual selected screen

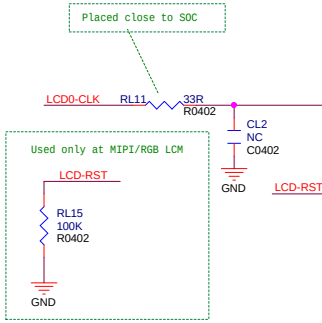




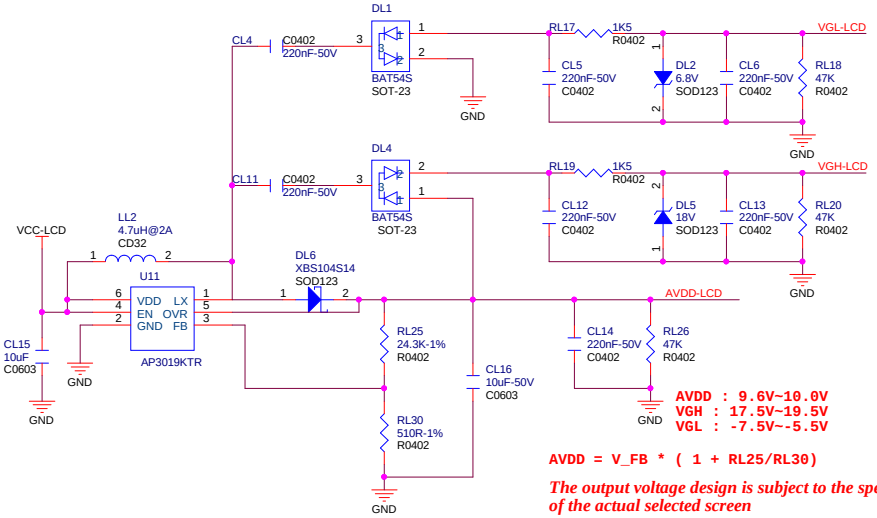
CTP







LCD POWER

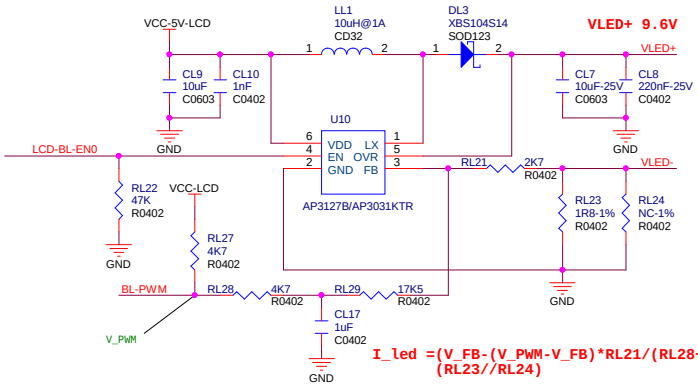


AVDD : 9.6V~10.0V
VGH : 17.5V~19.5V
VGL : -7.5V~-5.5V

AVDD = V_FB * (1 + RL25/RL30)

The output voltage design is subject to the specification voltage of the actual selected screen

BACKLIGHT



I_led =(V_FB-(V_PWM-V_FB)*RL21/(RL28+RL29))/(RL23//RL24)

The output voltage design is subject to the specification voltage of the actual selected screen

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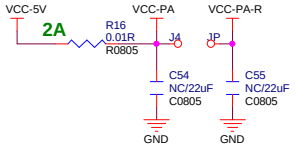
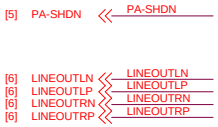
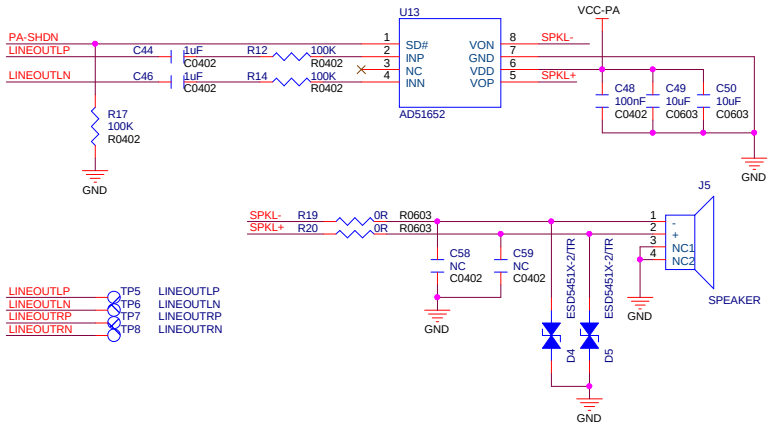
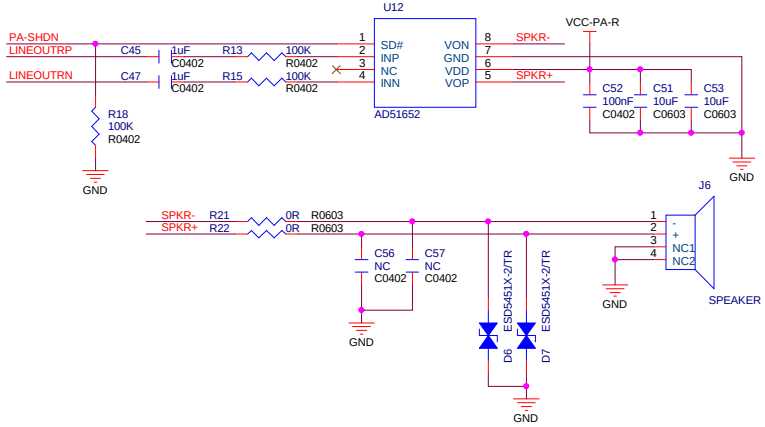
Audio



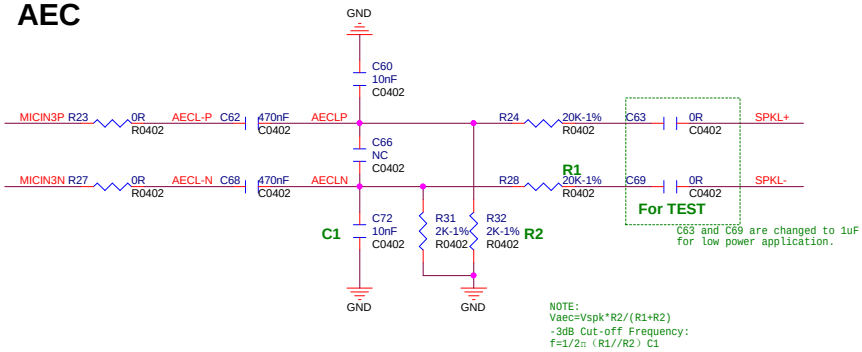


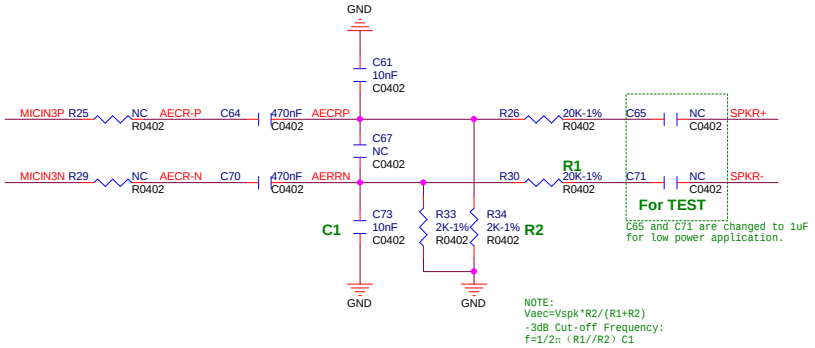
PA



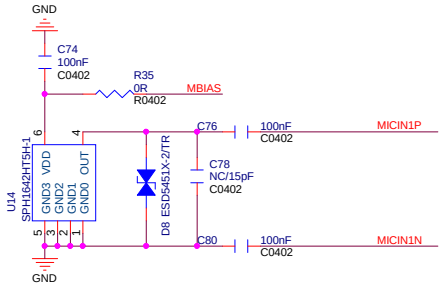


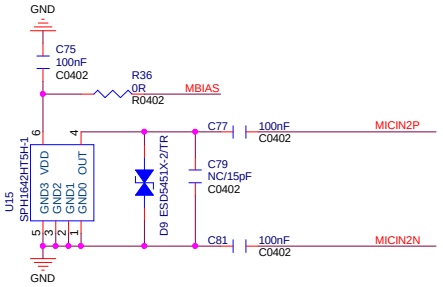
AEC





MIC





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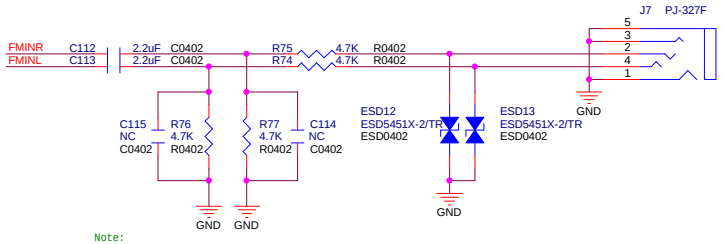
Audio

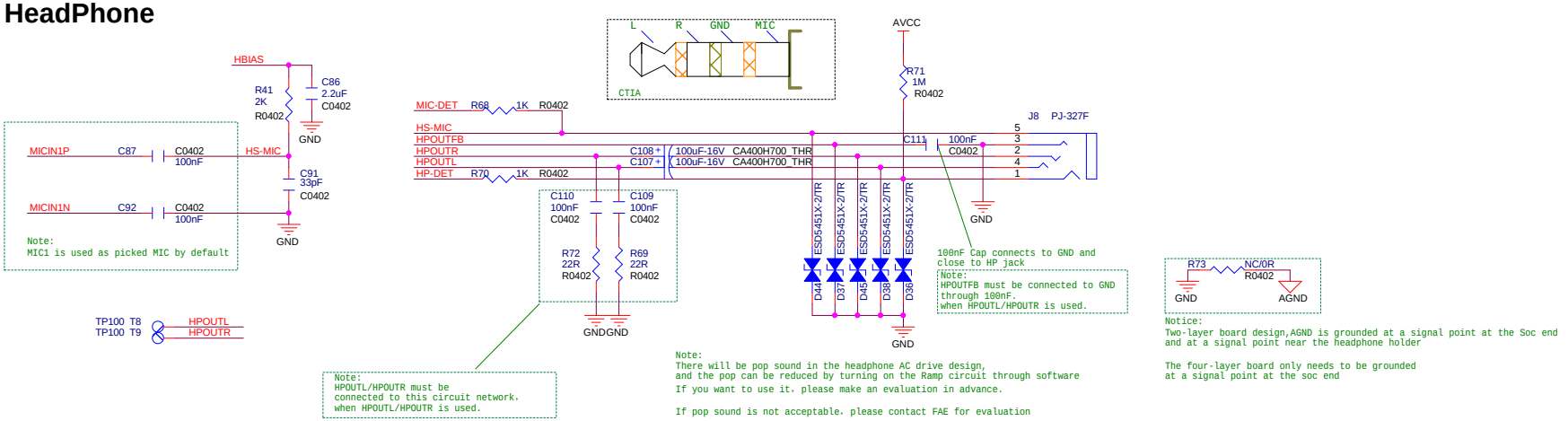
FMIN



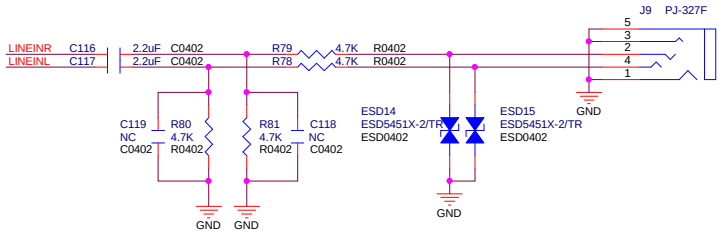
Note:
Voltage divider circuit reduces input signal amplitude

If the junction temperature of the product is over 90℃,
please contact FAE when using FMIN

HeadPhone



LINEIN



Note:
Voltage divider circuit reduces input signal amplitude

If the junction temperature of the product is over 90℃,
please contact FAE when using LINEIN

[6] FMINL
[6] FMINR
FMINL
FMINR

[6] MIC-DET
[6] HBIAS
[6,9] MICIN1N
[6,9] MICIN1P
[6] HP-DET
[6] HPOUTL
[6] HPOUTFB
[6] HPOUTR
MIC-DET
HBIAS
MICIN1N
MICIN1P
HP-DET
HPOUTL
HPOUTFB
HPOUTR

[6] LINEINL
[6] LINEINR
LINEINL
LINEINR

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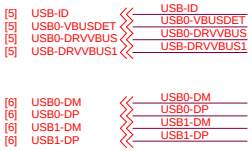
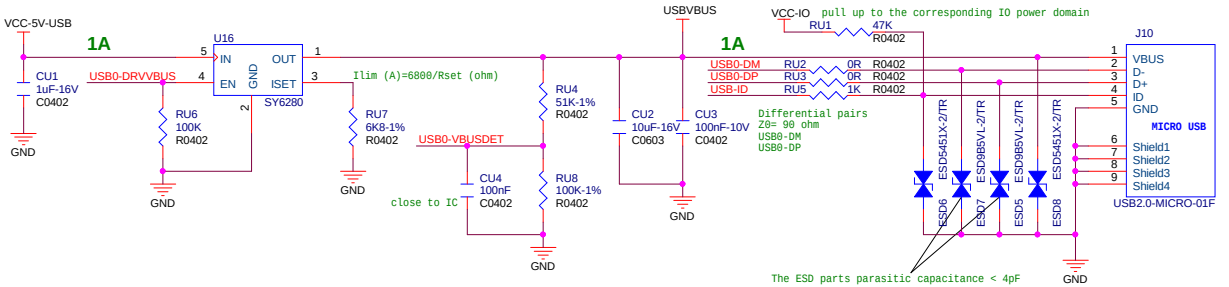
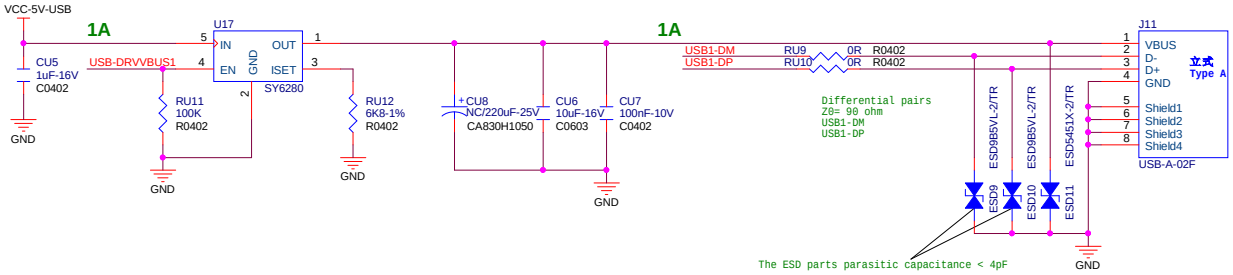
USB





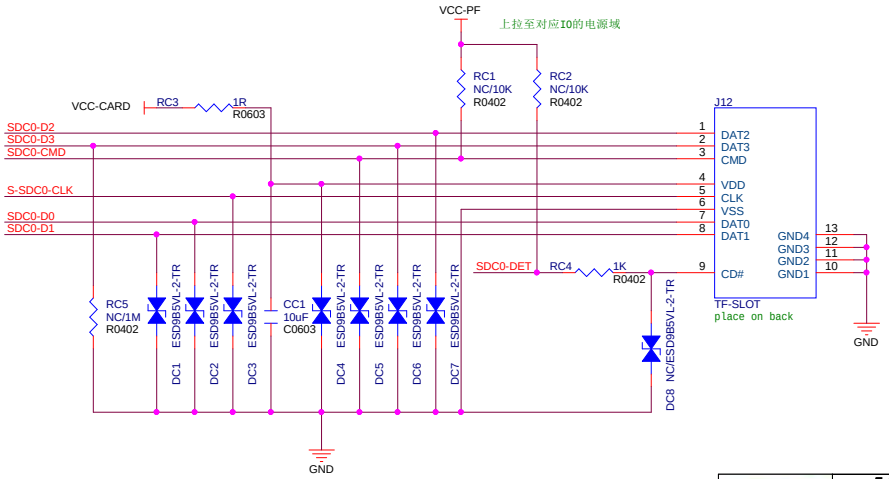


CARD

OPTION

The design defaults the PF port as the UART system debug port

If the design use SD Card ,need to move UART0 to other IO and update the software configuration



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EPHY

[5] RGMII-RXD3 — RGMII-RXD3
[5] RGMII-RXD2 — RGMII-RXD2
[5] RGMII-RXD1 — RGMII-RXD1
[5] RGMII-RXD0 — RGMII-RXD0
[5] RGMII-RXCK — RGMII-RXCK
[5] RGMII-RXCTL — RGMII-RXCTL
[5] RGMII-CLKIN — RGMII-CLKIN-125M
[5] RGMII-TXD3 — RGMII-TXD3
[5] RGMII-TXD2 — RGMII-TXD2
[5] RGMII-TXD1 — RGMII-TXD1
[5] RGMII-TXD0 — RGMII-TXD0
[5] RGMII-TXCK — RGMII-TXCK
[5] RGMII-TXCTL — RGMII-TXCTL
[5] RGMII-MDC — RGMII-MDC
[5] RGMII-MDIO — RGMII-MDIO

[5] RGMII-RESET — PHYRSTB
[5] EPHY-CLK-25M — EPHY-CLK-25M

VCC-EPHY
VCCIO-EPHY

VCC-EPHY: RE1 0.01R R0603; CE2 4.7uF C0402; CE3 100nF C0402; GND
Reserved for EMI. (optional)
Close to PHY PIN11 and PIN40 for Analog Power
RE5 0.01R R0603; CE5 100nF C0402; CE6 100nF C0402; GND
Close to PHY PIN29 for Digital Power & SWR

VCCIO-EPHY: RE6 0.01R R0603; CE13 100nF C0402; CE14 4.7uF C0402; GND

Note 1: RE6 is not needed for ONLY 3.3V RGMII application, and DVDDRG can be connected directly to DVDD33.
Note 2: DVDDRG must be short (or RE6 be mounted) to DVDD33 if the external RGMII 3.3V is selected.
Note 3: RE6 must be removed if the internal or external 2.5V/1.8V/1.5V RGMII is selected.
Note 4: CAPs must be closed to pin28 for EMI consideration.

RGMII TX Filter Network
RGMII-TXD3 RE10 0R R0402 TXD3
RGMII-TXD2 RE15 0R R0402 TXD2
RGMII-TXD1 RE16 0R R0402 TXD1
RGMII-TXD0 RE17 0R R0402 TXD0
RGMII-MDC RE12 0R R0402 MDC
RGMII-MDIO RE20 0R R0402 MDIO
RGMII-TXCTL RE13 0R R0402 TXCTL
RGMII-TXCK RE22 0R R0402 TXC
CE20 NC/22PF C0402-COG
Close to SOC. Reserved for EMI.(optional)

RGMII RX Filter Network
RGMII-RXCK RE23 0R R0402 RXC/PHYAD1
CE21 NC/22PF C0402-COG
RGMII-RXD3 RE24 0R R0402 RXD3/PHYAD0
RGMII-RXD2 RE25 0R R0402 RXD2/PLLOFF
RGMII-RXD1 RE26 0R R0402 RXD1/TXDLY
RGMII-RXD0 RE28 0R R0402 RXD0/RXDLY
RGMII-RXCTL RE31 0R R0402 RXCTL/PHYAD2
Close to PHY. Reserved for EMI.(optional)
Suggest that 15ohm for RTL8211FD-VX-CG, and 0ohm for RTL8211F/RTL8211FI/RTL8211FD/RTL8211FDI

RGMII-CLKIN-125M RE34 0R R0402 CLKOUT-125M
CE22 NC/22PF C0402-COG

DVDD33 PHY RESET/INTB
RE41 4.7K R0402 INTB
RE44 4.7K R0402 PHYRSTB
CE23 100nF C0402
DVDDRG GND
RE50 1.5K R0402 MDIO
RE51 2.49K-1% R0402 RSET

Enable/Disable PLL @ ALDPS
RE54 4.7K R0402 RXD2/PLLOFF RE55 NC/4.7K R0402
Pull-up to disable PLL @ ALDPS mode.

RGMII TXC/RXC Delay Config.
RE62 4.7K R0402 RXD1/TXDLY RE63 NC/4.7K R0402
RE64 NC/4.7K R0402 RXD0/RXDLY RE65 4.7K R0402
Pull-up for additional 2ns delay to TXC/RXC for data latching.

RGMII Voltage Config.
RE39 NC/4.7K R0402 LED0/CFG-EXT RE40 4.7K R0402
RE42 4.7K R0402 LED1/CFG-LDO0 RE43 NC/4.7K R0402
RE45 4.7K R0402 LED2/CFG-LDO1 RE46 NC/4.7K R0402

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V (default)	1'b1	2'b00
External 2.5V	1'b1	2'b01
External 1.8V	1'b1	2'b10
External 1.5V	1'b1	2'b11
Internal 2.5V	1'b0	2'b01
Internal 1.8V	1'b0	2'b10
Internal 1.5V	1'b0	2'b11

PHY Address Config.
RE56 NC/4.7K R0402 RXD3/PHYAD0 RE57 4.7K R0402
RE58 4.7K R0402 RXC/PHYAD1 RE59 NC/4.7K R0402
RE60 4.7K R0402 RXCTL/PHYAD2 RE61 NC/4.7K R0402

PHY Address	PHYAD[2:0]
0	3'b000
1 (default)	3'b001
2	3'b010
3	3'b011
4	3'b100
5	3'b101
6	3'b110
7	3'b111

A: 20mil RE3 NC/0R R0402 20mil
REGOUT 20mil L5 2.2uH-1A 20mil 20mil LP200_25DH100
CE9 NC/100nF/1uF C0402
CE10 4.7uF C0603-X7R B
CE11 100nF C0402
RE2 0R R0402
RE4 0R R0402
DVDD10
CE4 100nF C0402
AVDD10
CE7 100nF C0402
CE8 100nF C0402
CE12 100nF C0402
GND
For LDO mode
For SWR mode

Note 1: Bypass CAPs close to PHY DVDD10/AVDD10 power pins.
Note 2: Any inductance or bead except L5 is not allowed on the path from REGOUT to DVDD10/AVDD10.
Note 3: A is reserved to change the DVDD10/AVDD10 supply source to LDO mode (RTL8211FD).
Note 4: No design change of PCB model is needed if A is reserved. If only RTL8211FD used for particular PCB model, directly short REGOUT to DVDD10/AVDD10.
Note 5: If RTL8211FI is selected, the B should be replaced as 10uF X7R capacitor for industrial grade application. Please refer to the datasheet for other industrial grade information.
Note 6: The Trace length between L5 and PHY pin 30 must be within 0.5cm, CE8 and CE9 must be within 0.5cm.
Note 7:If RTL8211FD-VX is selected,the value of CE9 should be 1uF.

UE1
RTL8211Fxx
RTL8211F-CG/RTL8211FD-CG
AVDD33 40, RSET 39, AVDD10 38, XTAL-OUT 37, XTAL-IN 36, CLKOUT 35, LED2/CFG-LDO0 34, LED1/CFG-LDO0 33, LED0/CFG-EXT 32, INTB 31
41 EGND GND
MDI0+ 1, MDI0- 2, AVDD10 3, MDI1+ 4, MDI1- 5, MDI2+ 6, MDI2- 7, AVDD10 8, MDI3+ 9, MDI3- 10
REG_OUT 30 REGOUT, DVDD33 29 DVDD33, DVDD_RG 28 DVDDRG, RXC/PHYAD1 27 RXC/PHYAD1, RXCTL/PHYAD2 26 RXCTL/PHYAD2, RXD0/RXDLY 25 RXD0/RXDLY, RXD1/TXDLY 24 RXD1/TXDLY, RXD2/PLLOFF 23 RXD2/PLLOFF, RXD3/PHYAD0 22 RXD3/PHYAD0, DVDD10 21 DVDD10
AVDD33 11, PHYRSTB 12, MDC 13, MDIO 14, TXD3 15, TXD2 16, TXD1 17, TXD0 18, TXCTL 19, TXC 20

External Clock Case
EPHY-CLK-25M RE52 0R R0402 XTAL-OUT
RE53 0R R0402 XTAL-IN
GND
The XTAL_IN needs to be connected to GND if the external 25MHz clock used.

XTAL-IN CE24 NC/22pF-C0G C0402
YE1 XIN GND2 GND1 XOUT NC/25M-16pF-20ppm
XTAL-OUT RE66 NC/0R R0402 CE25 NC/22pF-C0G C0402
Crystal Case

D15 SPD9103W SOD130_175H101
D16 SPD9103W SOD130_175H101
D17 SPD9103W SOD130_175H101
D18 SPD9103W SOD130_175H101
GND CE1 NC/100nF C0402
J13 VCC GND MDI3- 8 TD3- MDI3+ 7 TD3+ MDI2- 5 TD2- MDI2+ 4 TD2+ MDI1- 6 TD1- MDI1+ 3 TD1+ MDI0- 2 TD0- MDI0+ 1 TD0+ 12 SHIELD-0 11 SHIELD-1
10/100/1000 MAGNETICS && RJ45
HFJ11-1G01E
CHASIS-GND
CE15 1000pF-2KV C1206
GND CHASIS-GND

MDI0- RE7 NC/49.9R-1% R0402 CE16 NC/1nF C0402 GND
MDI0+ RE8 NC/49.9R-1% R0402
MDI1- RE9 NC/49.9R-1% R0402 CE17 NC/1nF C0402 GND
MDI1+ RE14 NC/49.9R-1% R0402
MDI2- RE11 NC/49.9R-1% R0402 CE19 NC/1nF C0402 GND
MDI2+ RE18 NC/49.9R-1% R0402
MDI3- RE19 NC/49.9R-1% R0402 CE18 NC/1nF C0402 GND
MDI3+ RE21 NC/49.9R-1% R0402

LEDs Configuration
LED0/CFG-EXT Reserved for EMI 10M Link and Active
C99 NC/100PF C0402
RE27 NC/0R R0402
RE29 0R R0402
RE32 NC/510R R0402
D19 LED-0805-R
RE30 510R R0402
DVDD33
LED1/CFG-LDO0 Reserved for EMI 100M Link and Active
C100 NC/100PF C0402
RE33 0R R0402
RE35 NC/0R R0402
RE37 510R R0402
D20 LED-0805-R
RE36 NC/510R R0402
DVDD33
LED2/CFG-LDO1 Reserved for EMI 1000M Link and Active
C101 NC/100PF C0402
RE38 0R R0402
RE47 NC/0R R0402
RE49 510R R0402
D21 LED-0805-R
RE48 NC/510R R0402
DVDD33

LED Resistances Setting	
CFG-EXT=1'b1	RE27(NC), RE29, RE30, RE32(NC)
CFG-EXT=1'b0	RE27, RE29(NC), RE30(NC), RE32
CFG-LDO0=1'b1	RE33(NC), RE35, RE36, RE37(NC)
CFG-LDO0=1'b0	RE33, RE35(NC), RE36(NC), RE37
CFG-LDO1=1'b1	RE38(NC), RE47, RE48, RE49(NC)
CFG-LDO1=1'b0	RE38, RE47(NC), RE48(NC), RE49

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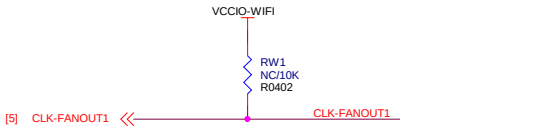
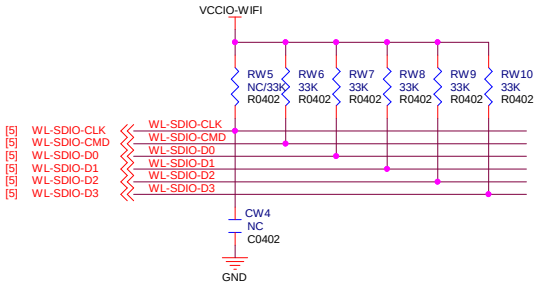
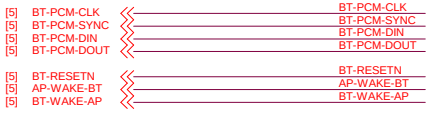
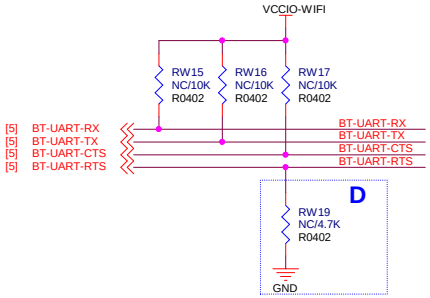
WIFI+BT

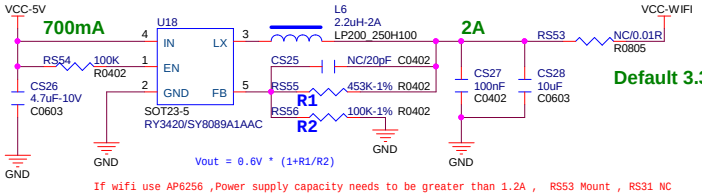


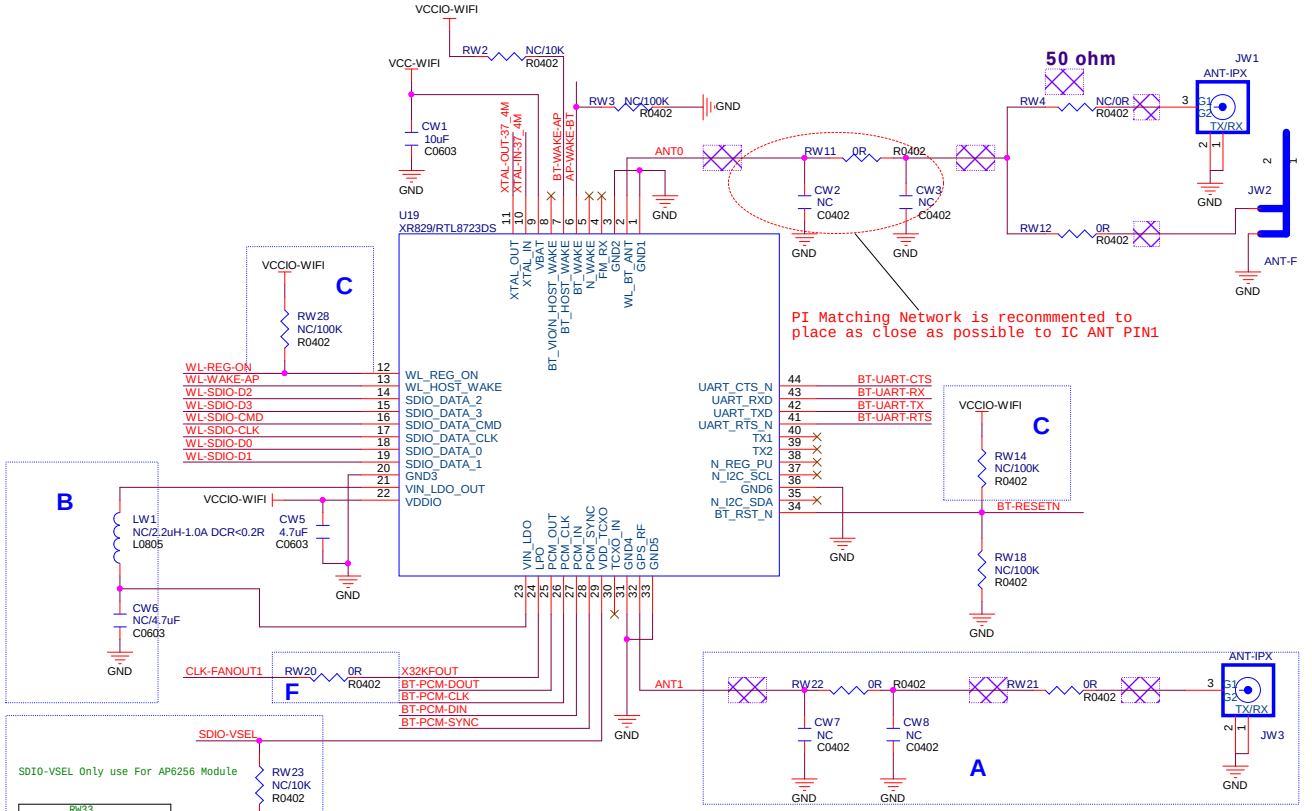






Option





NOTE	ANT	A	B	C	D	E	F
XR829 Module	single	NC	NC	NC	NC	NC	Mount
RTL8723DS Module	single	NC	NC	Mount	NC	NC	NC
RTL8723DS Module(no debugged)	double	Mount	NC	Mount	NC	NC	NC
RTL8821CS Module(no debugged)	single	NC	NC	Mount	Mount	NC	NC
AP6256 Module(no debugged)	single	NC	Mount	NC	NC	Mount	Mount

Please consult the module factory for the latest design advice

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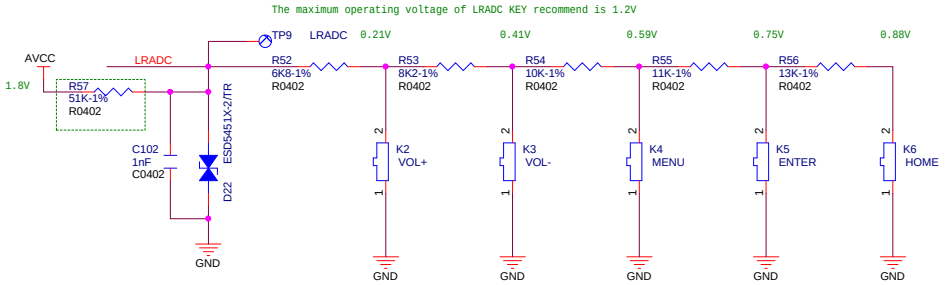
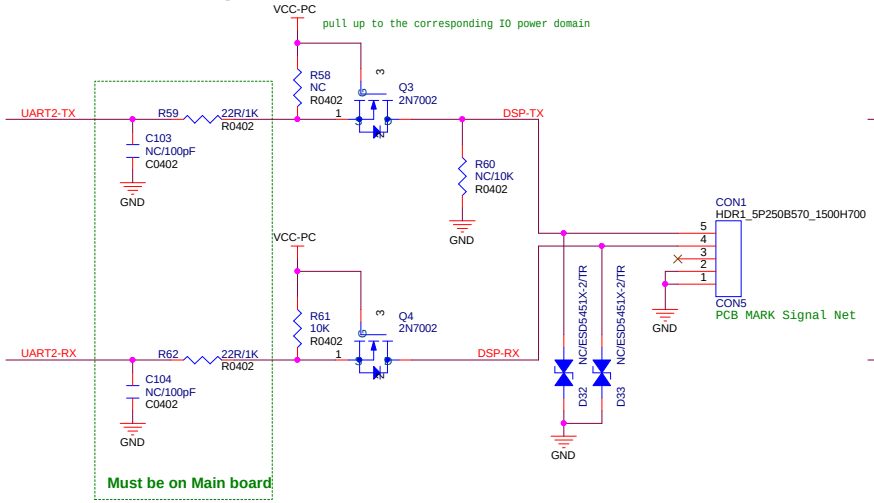
KEY ADC

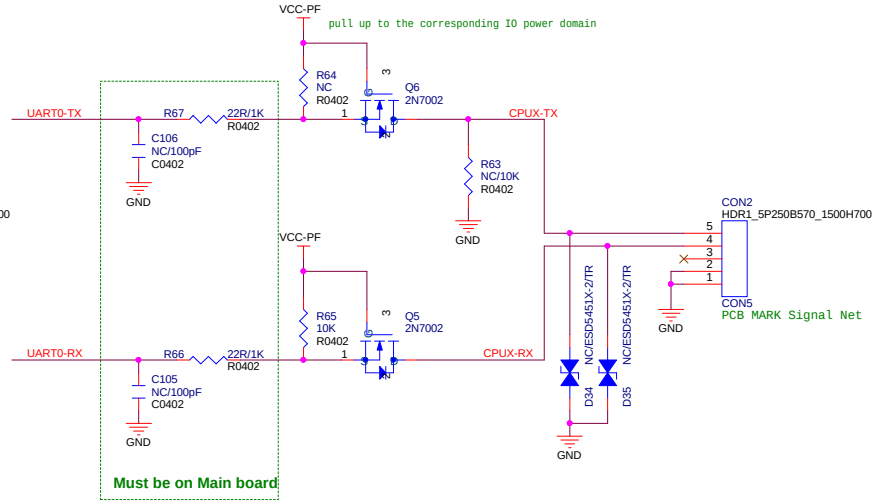


[6] LRADC <<< LRADC

UART Debug



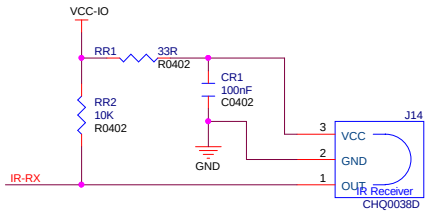
The isolation circuit must be reserved for debugging,otherwise it will cause abnormal power-on.
Cost-saving during production ,do not use UART debug,consider reducing isolation circuit NC.



The isolation circuit must be reserved for debugging,otherwise it will cause abnormal power-on.
Cost-saving during production ,do not use UART debug,consider reducing isolation circuit NC.

[5] UART2-TX <<< UART2-TX
[5] UART2-RX <<< UART2-RX
[5] UART0-TX <<< UART0-TX
[5] UART0-RX <<< UART0-RX

IR-RX



[5] IR-RX <<< IR-RX

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