Himax Display, Inc.

Application Note

(DOC No. AN-HX7033-AN01)

HX7033

320X240 0.28” LCOS Module

Version 01 November, 2010

Himax Display, Inc.
http://www.himaxdisplay.com

Revision History

Version	Eff. Date	Author	Modified Items
01	2010/11/09	Stanley	New Setup

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1 About This Document

This document is a preliminary version application note for HX7033 LCOS color sequential chipset. It is for customer’s reference only, and it subjects to change without notice.

2 General Description

The purpose of this application note is to offer several common usage sequences as a quick start for customers. Register values of the registers shown below will be generated by HDI Adjustment Tool. Please set these values according to HDI Adjustment Tool output file.

3 Serial Interface and Command Registers

HX7033 is controlled via a two-wired serial interface. The device is connected to this bus as slave device. HX7033 has a 7-bit slave address.

The seven bits identify numbers is **(1, 0, 0, 1, 0, 0, 0).**

3.1 Two-Wired Serial Bus Protocol Operates as Follows

(a) The master initiates data transfer by establishing a START condition, when a high-to-low transition on the SDI line occurs while SCL is high. The following byte is the address byte, which consists of the 7th bit slave address followed by an R/*W* bit (this bit determines whether data will be read from or written to the slave device).

The slave whose address corresponds to the transmitted address responds by pulling SDI low during the 9th clock pulse (this is the Acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its shift register.

(b) Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an Acknowledge bit). The transitions on the SDI line must occur during the low period of SCL and remain stable during the high period of SCL.

(c) When all data bits have been read or written to, a STOP condition is established. In Write/Read mode, the master will pull the SDI line high during the 10th clock pulse to establish a STOP condition. The master will then bring the SDI line low before the 10th clock pulse and then high during the 10th clock pulse to establish a STOP condition.

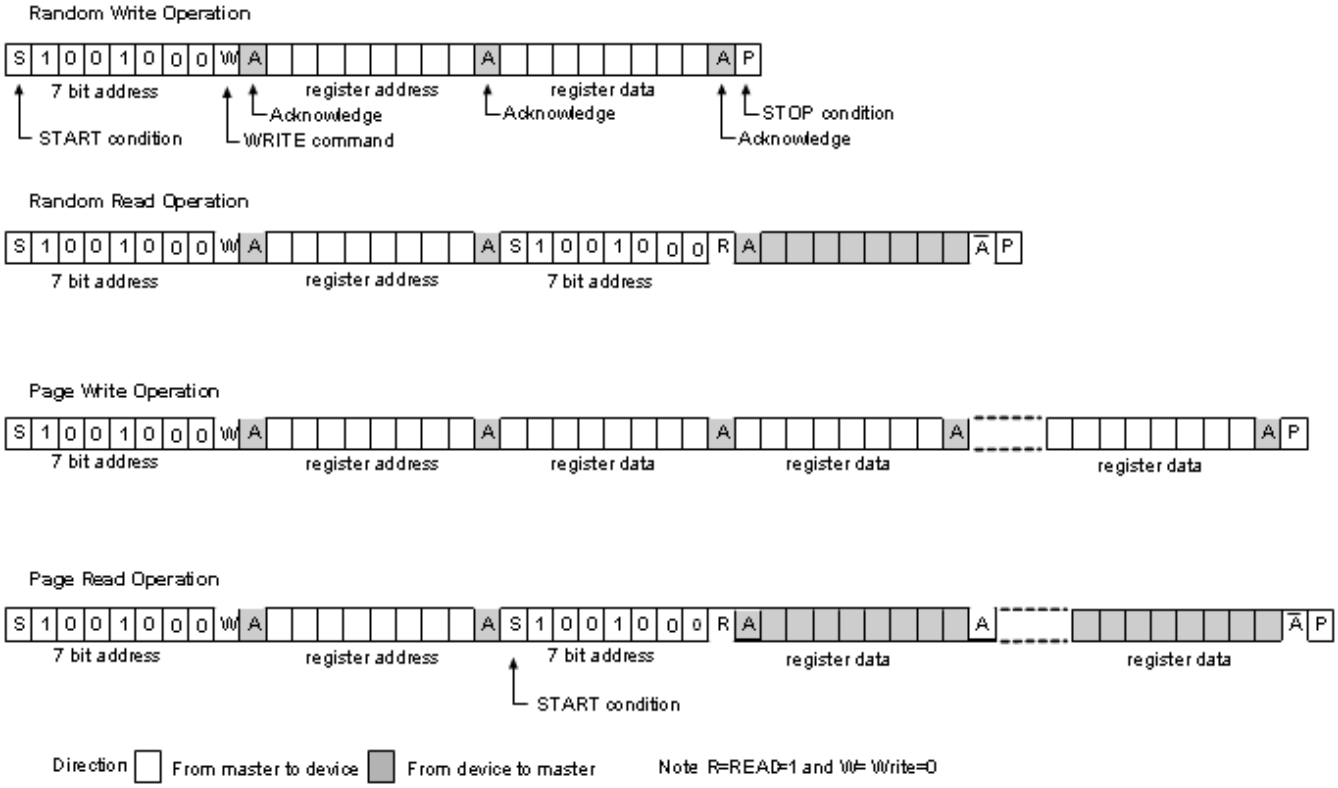

Figure 3.1 Two-Wired Serial Interface Read/Write Operation

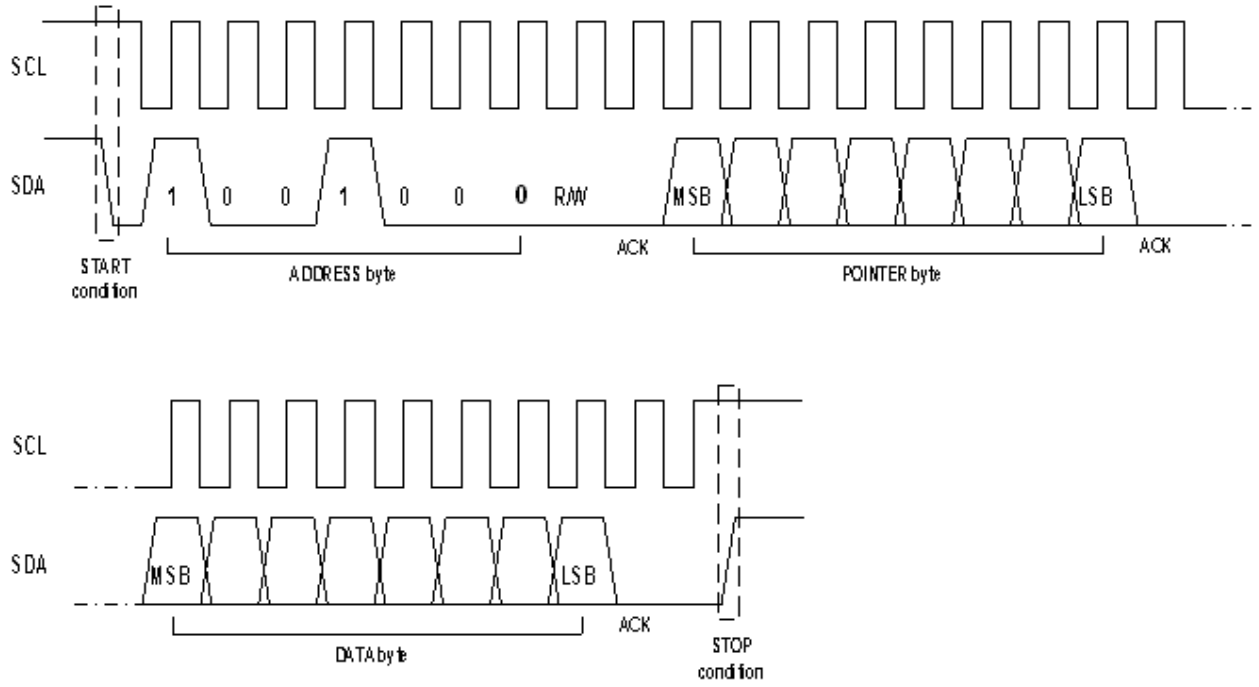

Figure 3.2 Two-Wired Serial Interface Timing Diagram

Table 3.1 Two-Wired Serial Interface Input Signal SCL, SDA Specification

Item	Symbol	Min	Typ.	Max	Unit
SCL clock frequency	FSCL	-	-	100	KHz
Bus free time	Tbuf	1.0	-	-	us
Start condition setup time	Tsu;start	1.0	-	-	us
Start condition hold time	Thd;start	0.5	-	-	us
SCL low time	Tlow	1.0	-	-	us
SCL high time	Thigh	1.0	-	-	us
SCL and SDA rise time	Tr	-	-	1.0	us
SCL and SDA fall time	Tr	-	-	0.3	us
Data setup time	Tsu;dat	250	-	-	ns
Data hold time	Thd;dat	250	-	-	ns
SCL low to data out valid	Tvd;dat	-	-	5.2	us
Stop condition setup time	Tsu;stop	1.0	-	-	us

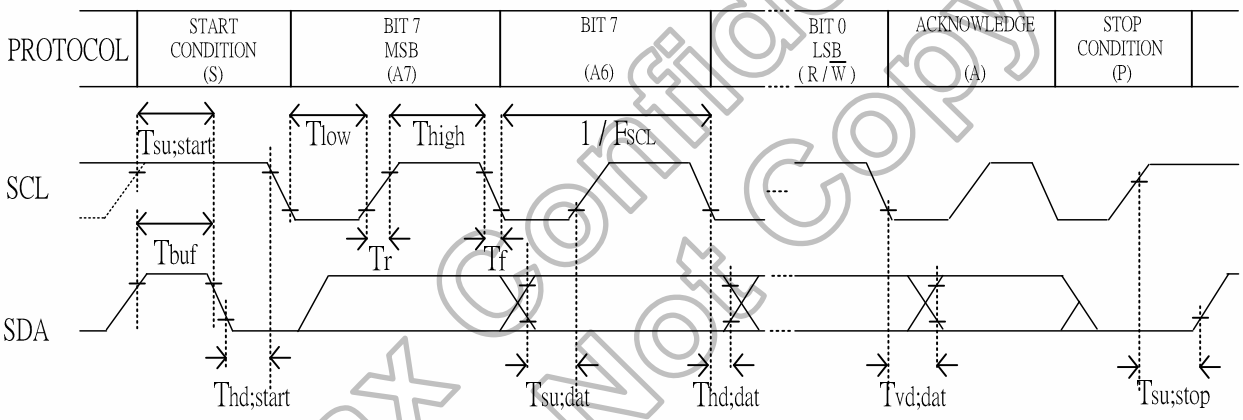

Figure 3.3 Two-Wired Serial Interface Waveform

3.2 Two-Wired Serial Interface Pull-up Circuit

The two-wired serial interface level of HX7033 could be 3.3V or 1.8V following the VDDD. If the master device is 3.3V supply voltage and HX7033 VDDD is 1.8V, it needs transfer the two-wired serial interface level to 1.8V.

The two-wired serial interface level shift circuit sees as below:

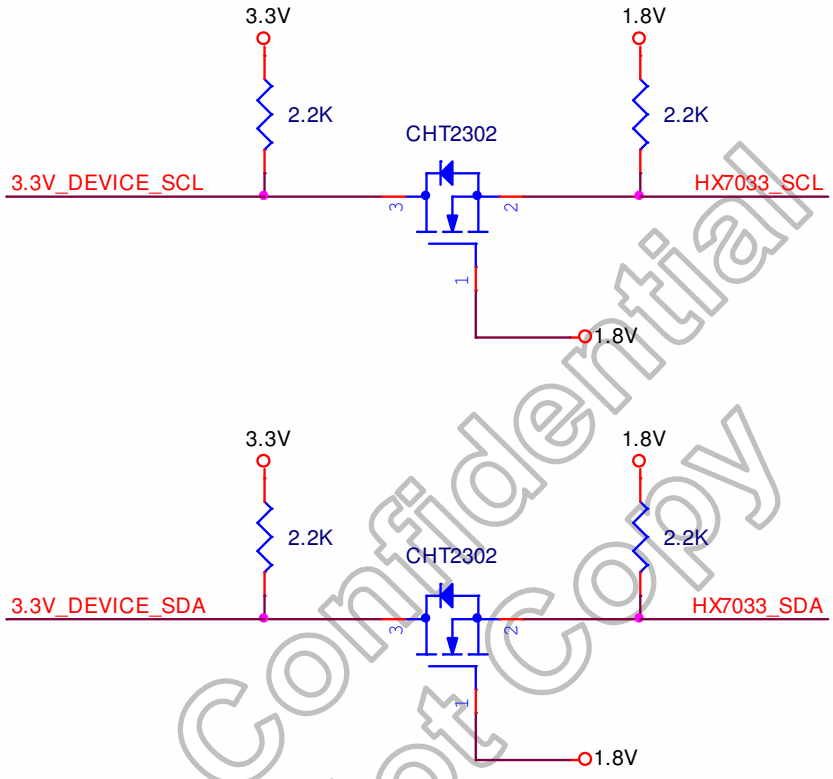

Figure 3.4 Two-Wired Serial Interface level shift Circuit

3.3 Initial Settings

After resetting HX7033, user could set some command registers to light on HX7033.

Table 3.2 Command Registers for HX7033 Initial Settings

Register NO.	*Register code definition*							
	D[7]	*D[6]*	*D[5]*	*D[4]*	*D[3]*	*D[2]*	*D[1]*	*D[0]*
R00h	LR	UD	0	1	0	1	1	0
R01h	SC_I2C	0	0	0	0	0	0	0
R03h	TRIGMA	1	0	1	0	0	0	0
R04h	1	0	0	0	0	RGB_EN	0	DEG_EN
R05h	1	1	1	1	0	1	0	1
R06h	0	1	0	1	0	1	0	1
R07h	0	1	0	1	0	1	0	1
R08h	0	1	0	1	0	1	0	1
R09h	0	1	0	1	0	1	0	1
R0Ah	1	1	1	1	0	1	1	0
R0Bh	COMPN	0	0	0	0	0	0	0

Table 3.3 Description of Control Setting

Register	Setting Description
LR	0, Display right to left
	1, Display left to right (Default)
UD	0, Display down to up
	1, Display up to down (Default)
SC_I2C	0, Disable single cell (Default)
	1, Enable single cell
TRIGMA	0, All refer to R gamma (Default)
	1, Enable R/G/B gamma select function
RGB_EN	0, Disable RGB666 interface
	1, Enable RGB666 interface (Default)
DEG_EN	0, Disable Dual-edge interface (Default)
	1, Enable Dual-edge interface
COMPN	1, COM range is 1/2VDDA~VDDA (Default)
	0, COM range is 0~1/2VDDA

R0Ah and R0Bh registers setting example :

- VDDA = 10V, => 1/2VDDA = 5V.

1. Setting COM voltage to 5.2V, the R0Bh is 80h. (COM voltage > 1/2VDDA)

$$V_{COM} = VDDA - \frac{VDDA * D}{510}$$, VCOM = 5.2V, VDDA = 10V

=> D = 244,

=> R0Ah = F4h.

2. Setting COM voltage to 4.8V, the R0Bh is 00h. (COM voltage < 1/2VDDA)

$$V_{COM} = \frac{VDDA}{2} - \frac{VDDA * D}{510}$$, VCOM = 4.8V, VDDA = 10V

=> D = 10,

=> R0Ah = 0Ah.

3.4 Gamma and COM suggest setting

See Table 3.4 is the gamma 2.2 and COM suggest settings

Table 3.4 Gamma 2.2 and COM Settings

Note	*Register NO.*	*Register Value*
COM	R0Ah	F2h
COMPN	R0Bh	80h
RGMAP1	R0Ch	00h
RGMAP2	R0Dh	51h
RGMAP3	R0Eh	8Ah
RGMAP4	R0Fh	B2h
RGMAP5	R10h	D8h
RGMAP6	R11h	E5h
RGMAN6	R12h	19h
RGMAN5	R13h	26h
RGMAN4	R14h	4Ch
RGMAN3	R15h	74h
RGMAN2	R16h	ADh
RGMAN1	R17h	FFh

Note : TRIGMA = 0.

4 VDDA/VDDD Power Input Circuit

HX7033 needed VDDA and VDDD power input, the reference circuit as below:

a. VDDA power input

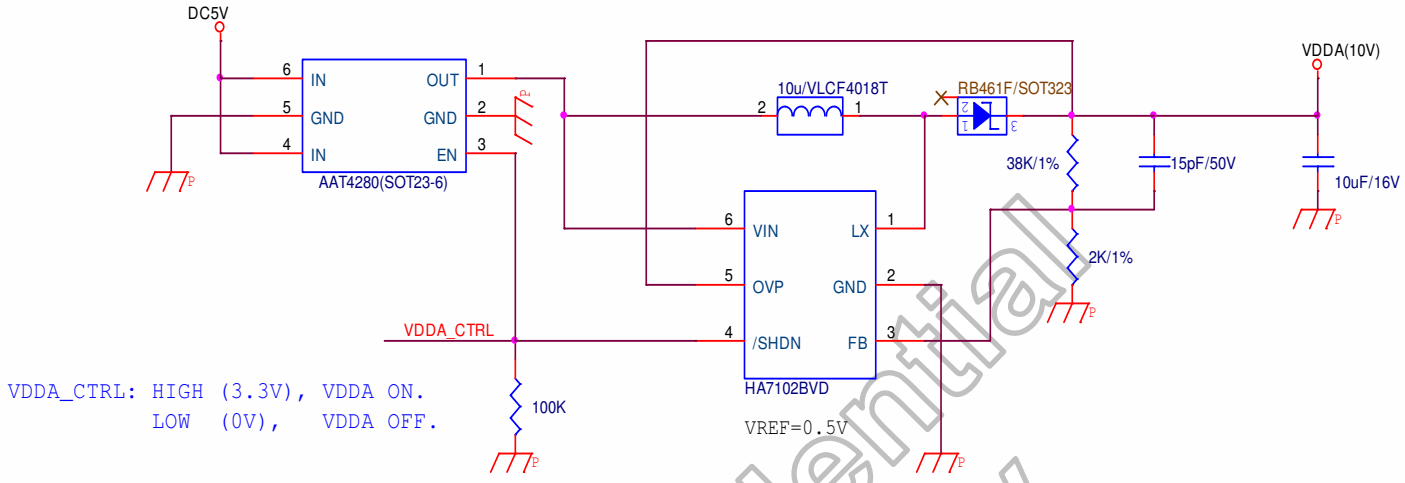

Figure 3.5 VDDA Power Input Circuit

b. VDDD power input

VDDD is 1.8V.

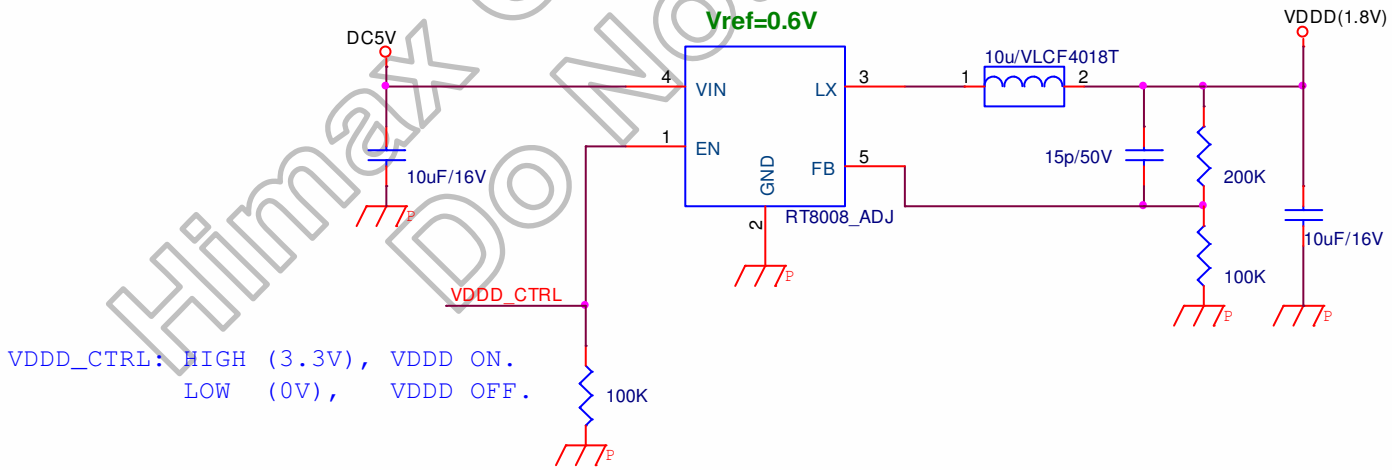

Figure 3.6 VDDD Power Input Circuit

c. HX7033 application circuit

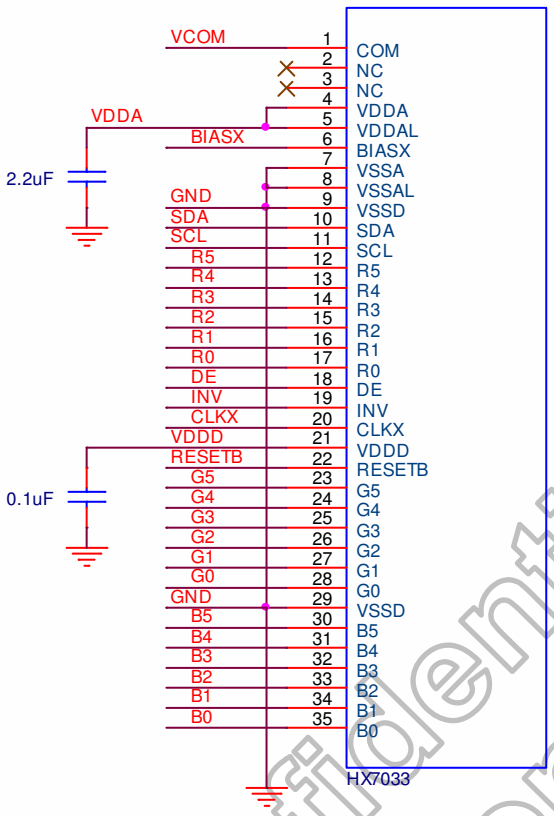

Figure 3.7 HX7033 Application Circuit

5 Common Sequences

5.1 Power on Sequence

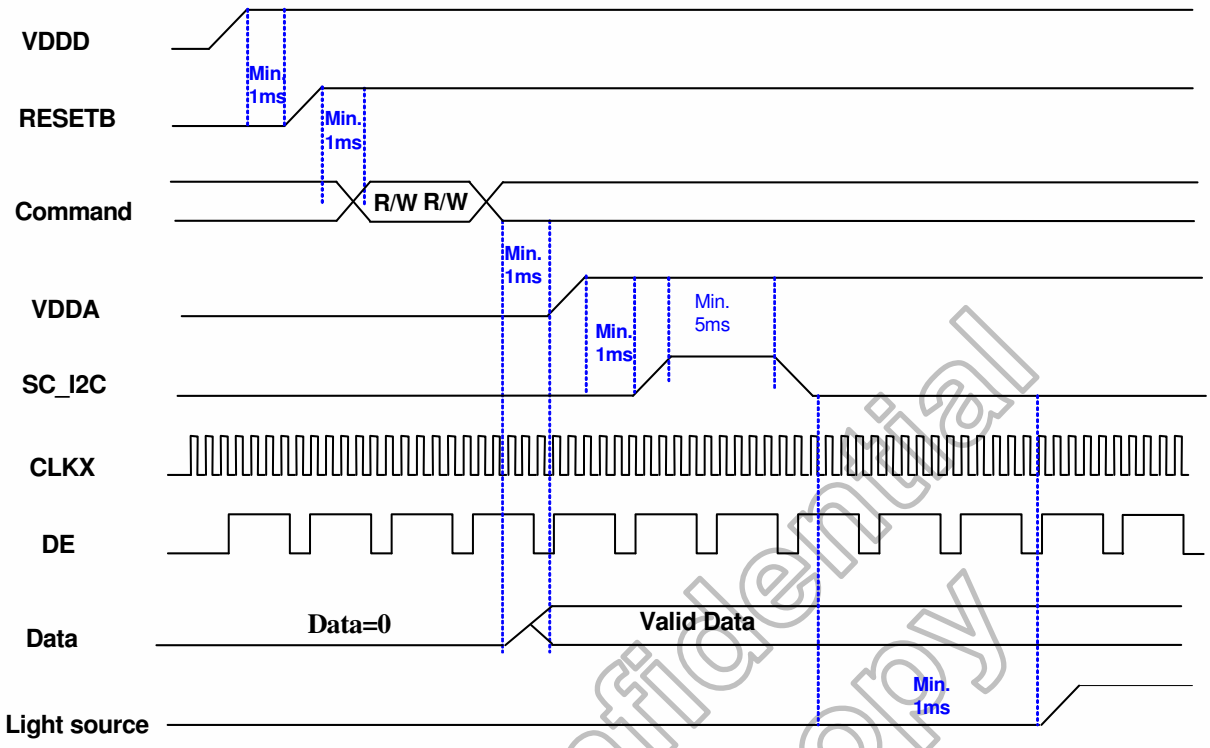

Figure 4.1 Timing Diagram for Power on Sequence

5.2 Power off Sequence

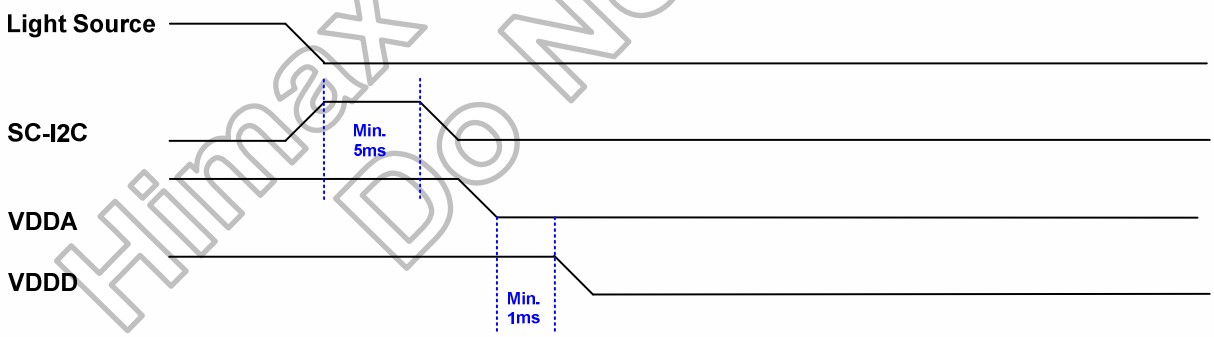

Figure 4.2 Timing Diagram for Power off Sequence

6 Firmware Flow

6.1 Power on Sequence Flow

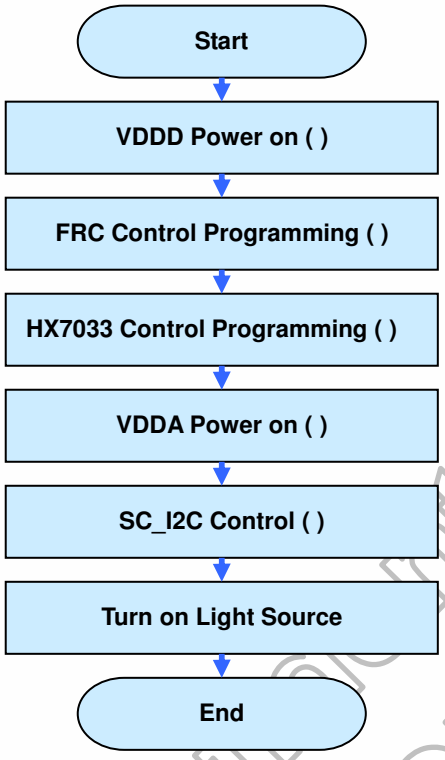

Figure 6.1 Power on Sequence Flow

6.2 Power off Sequence Flow

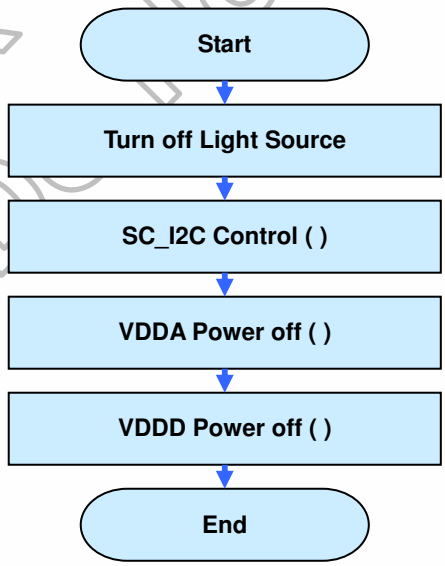

Figure 6.2 Power off Sequence Flow