1/10” VGA CMOS Image Sensor

GC0310

DataSheet

V1.0

2014-02-19

GalaxyCore Inc.

Revision History

Version V1.0 2014.02.19

- Document Release

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Content

1. Sensor Overview

1.1 General Description

The GC0310 features 640V x 480H resolution with 1/10-inch optical format, and 4-transistor pixel structure for high image quality and low noise variations. It delivers superior image quality by powerful on-chip design of a 10-bit ADC, and embedded image signal processor.

The full scale integration of high-performance and low-power functions makes the GC0310 best fit the design, reduce implementation process, and extend the battery life of cell phones, PDAs, and a wide variety of mobile applications.

The on-chip ISP provides a very smooth AE (Auto Exposure) and accurate AWB(Auto White Balance) control. It provides various data formats, such as Bayer RGB, RGB565, YCbCr 4:2:2. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor. It's also offer DVP, MIPI and SPI interface with BB.

1.2 Features

- Standard optical format of 1/10 inch
- Various output formats: YCbCr4:2:2, RGB565, Raw Bayer
- Interface support: DVP parallel, MIPI, SPI
- Power supply requirement: AVDD: 2.7~3.0V
  IOVDD: 1.7~3.0V
- Windowing support
- Horizontal/Vertical mirror
- Image processing module
- Package: CSP/COB

1.3 Application

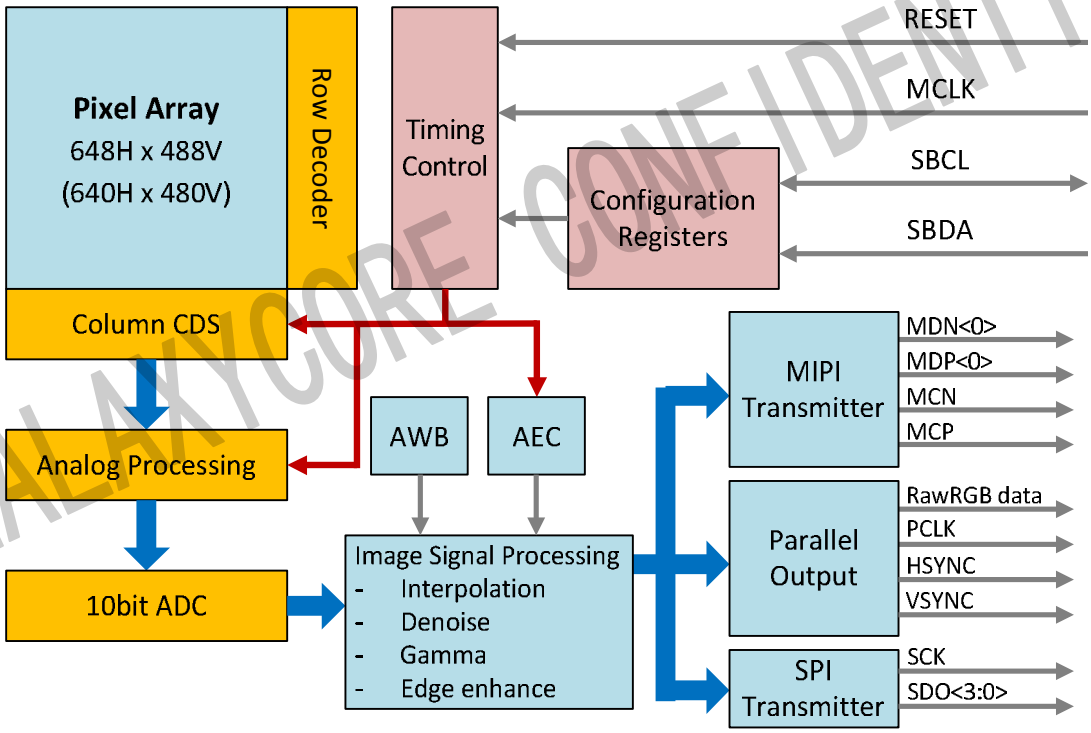
- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipments
- Security systems
- Industrial and environmental systems

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/10 inch
Pixel Size	2.25um x 2.25um
Active pixel array	648 x 488
ADC resolution	10 bit ADC
Max Frame rate	30fps@24Mhz,VGA
Power Supply	AVDD28: 2.7~3.0V IOVDD: 1.7~3.0V
Power Consumption	80mW @ 30fps VGA <50μA @ standby
SNR	TBD
Dark Current	TBD
Sensitivity	TBD
Operating temperature:	-20~70℃
Stable Image temperature	0~50℃
Optimal lens chief ray angle(CRA)	29° (linear)
Package type	CSP/COB

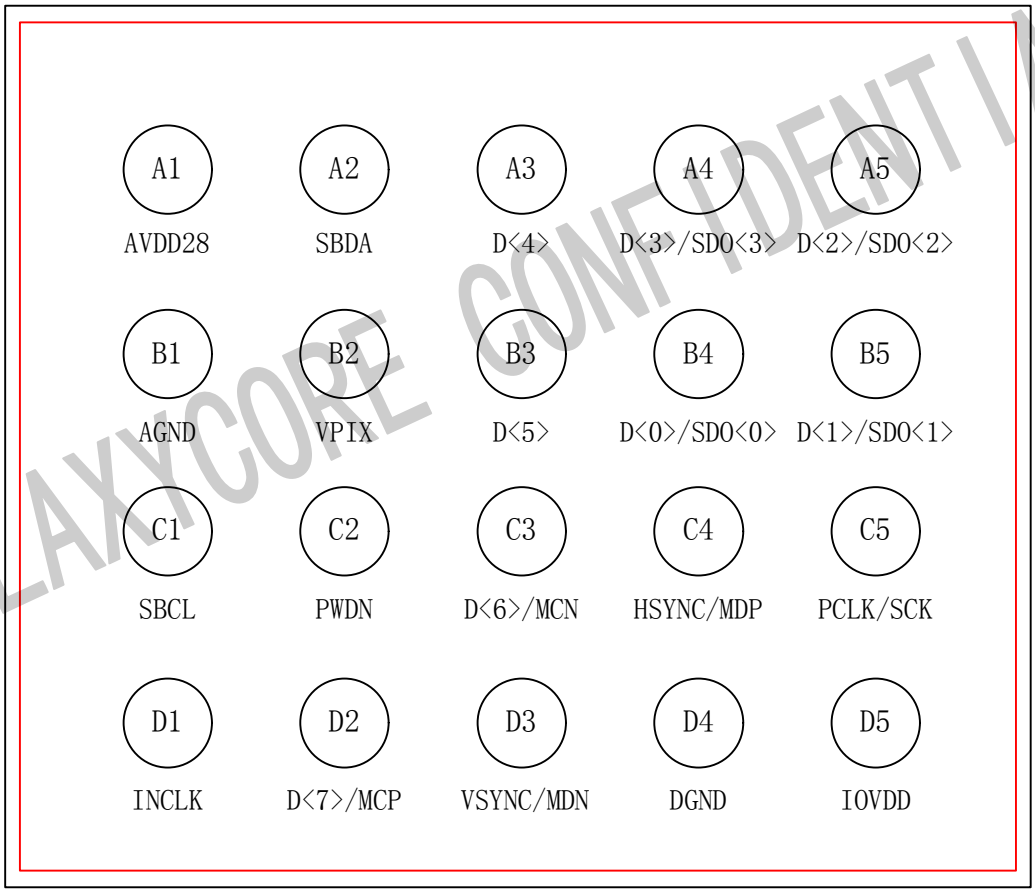
2. Block Diagram

2.1 Block Diagram



GC0310 has an active image array of 648x488 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bit A/D converter. The digital signals are processed in the ISP Block, including Bayer interpolation, denoise, color correction, gamma correction, data format conversion and so on. Users can easily control these functions via two-wire serial interface bus.

2.2 Pin Diagram



Top View

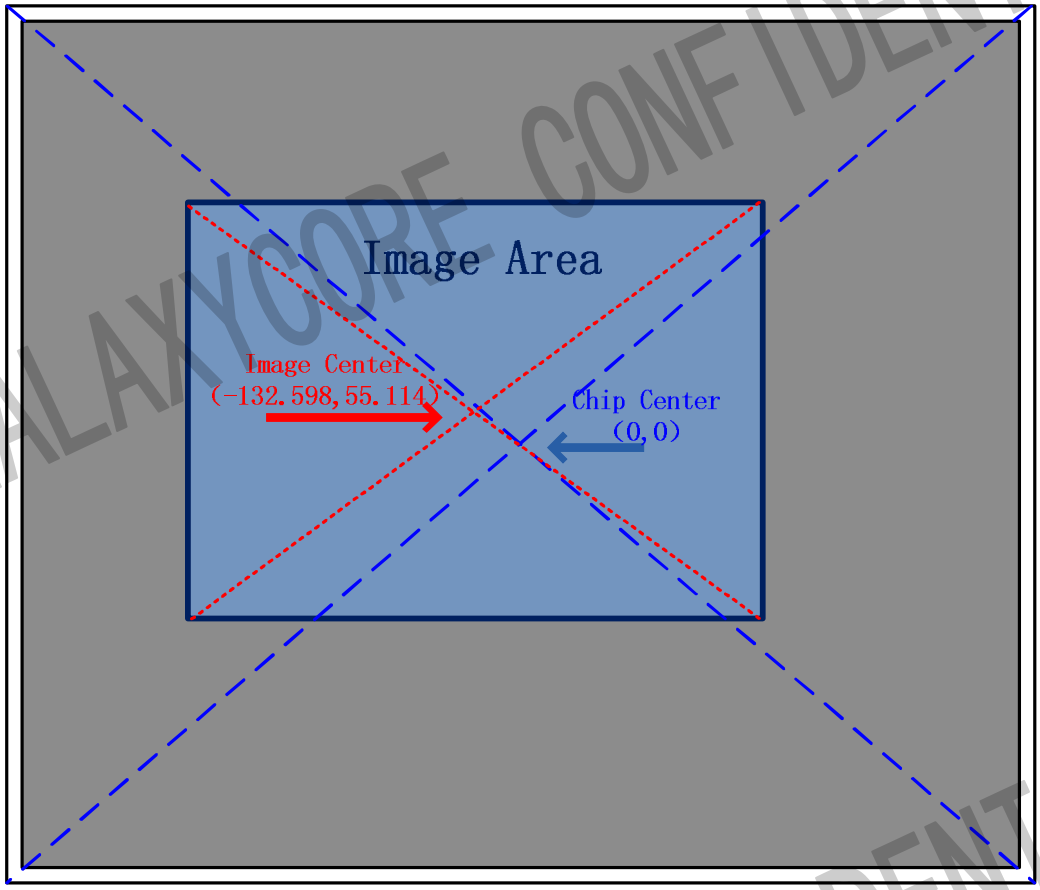
2.3 Signal Descriptions

Pin	Name	Pin Type	Function
A1	**AVDD28**	Power	Main power supply pin, 2.7~3.0V, please connect capacity to ground.
A2	**SBDA**	I/O	Two-wire serial bus, data
A3	**D<4>**	Output	YUV/RGB data output bit[4]
A4	**D<3>**	Output	YUV/RGB data output bit[3]
	SDO<3>		SPI data[3]
A5	**D<2>**	Output	YUV/RGB data output bit[2]
	SDO<2>		SPI data[2]
B1	**AGND**	Ground	AGND
B2	**VPIX**	Power	Internal Power, please connect capacity to ground.
B3	**D<5>**	Output	YUV/RGB data output bit[5]
B4	**D<0>**	Output	YUV/RGB data output bit[0]
	SDO<0>		SPI data[0]
B5	**D<1>**	Output	YUV/RGB data output bit[1]

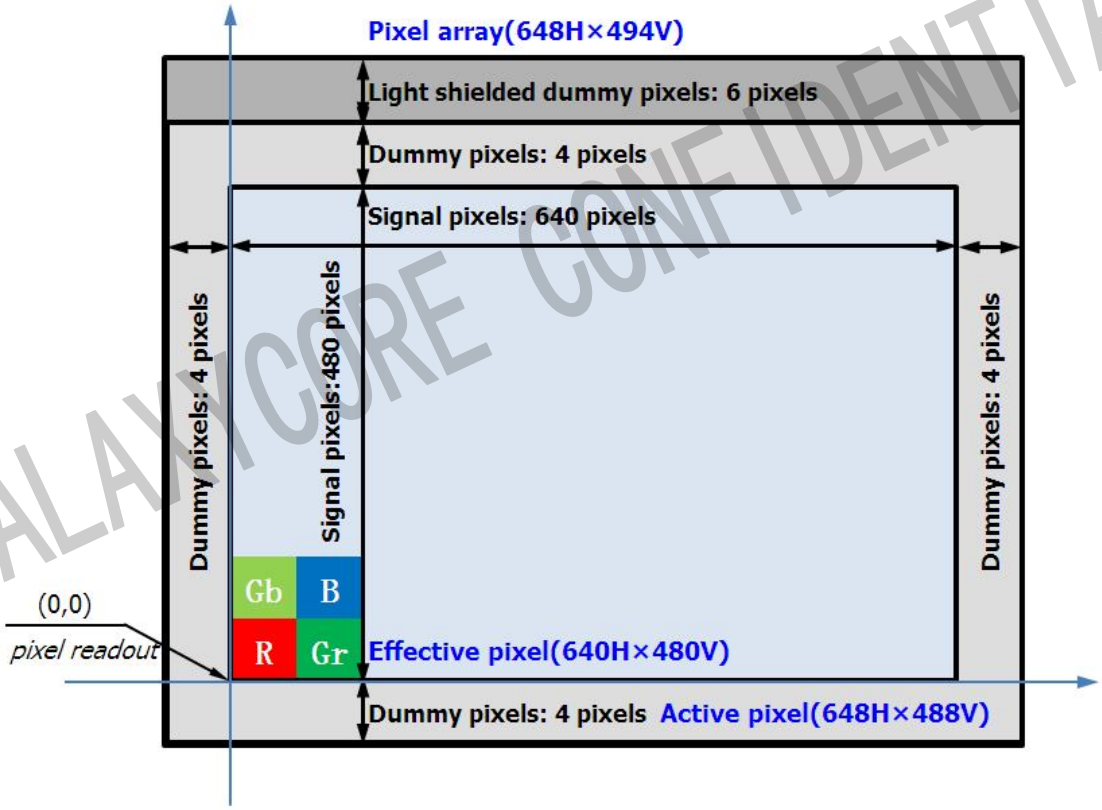
	SDO<1>		SPI data[1]
C1	**SBCL**	Input	Two-wire serial bus, clock
C2	**PWDN**	Input	Sensor power down control: 0: normal work 1: standby
C3	**D<6>**	Output	YUV/RGB data output bit[6]
	MCN		MIPI clock(-)
C4	**HSYNC**	Output	HSYNC output
	MDP		MIPI data(+)
C5	**PCLK**	Output	Pixel clock output
	SCK		SPI Clock
D1	**INCLK**	Input	Main clock
D2	**D<7>**	Output	YUV/RGB data output bit[7]
	MCP		MIPI clock(+)
D3	**VSYNC**	Output	VSYNC output
	MDN		MIPI data(-)
D4	**DGND**	Ground	DGND
D5	**IOVDD**	Power	Power Supply for I/O circuits, 1.7~3.0V, please connect capacity to ground.

3. Optical Specifications

3.1 Sensor Array Center



3.2 Pixel Array

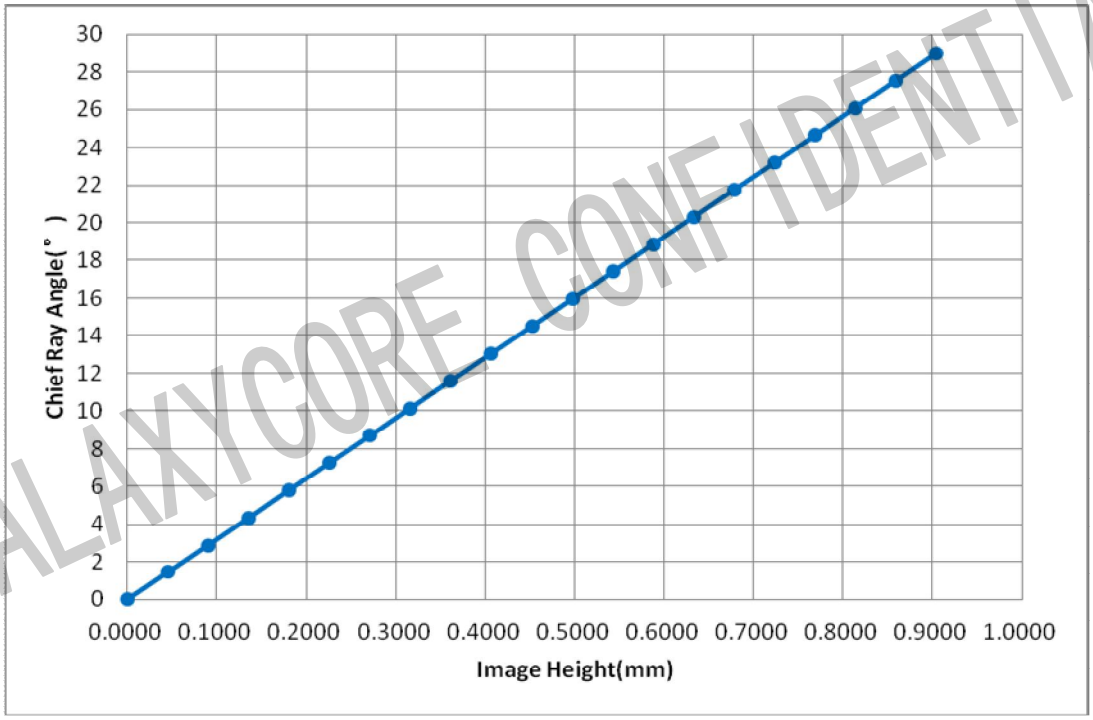


Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 647. If flip in column, column is read out from 647 to 0.

If no flip in row, row is read out from 0 to 487. If flip in row, row is read out from 487 to 0.

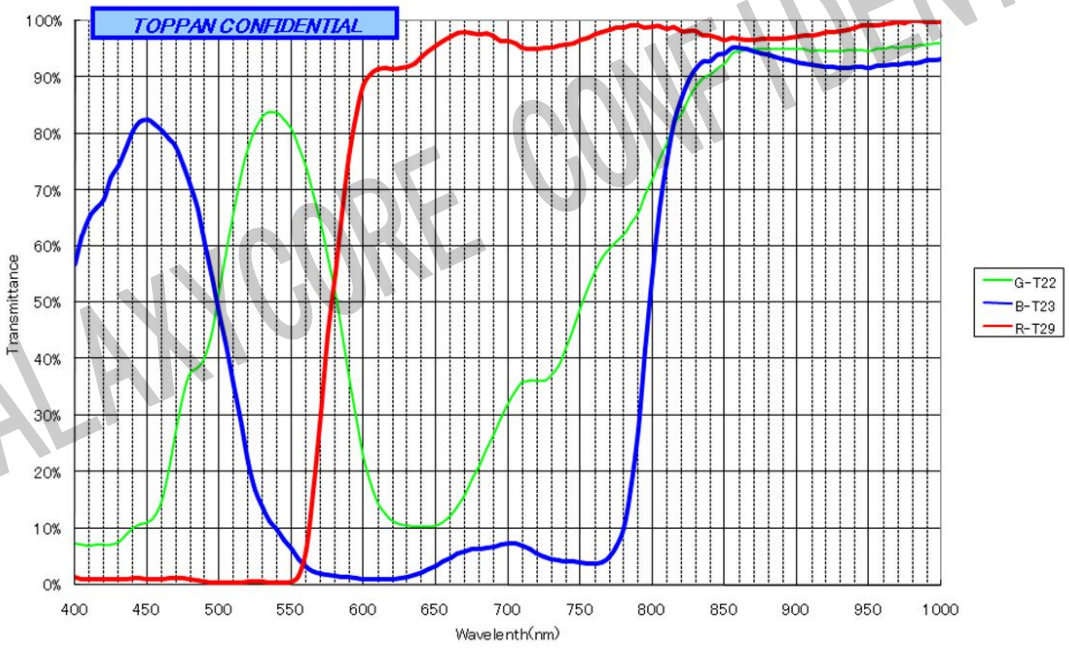
3.3 Lens Chief Ray Angle (CRA)



Field(%)	Image Height(mm)	CRA(degrees)
0	0.0000	0.0
5	0.0452	1.45
10	0.0904	2.90
15	0.1357	4.35
20	0.1809	5.80
25	0.2261	7.25
30	0.2713	8.70
35	0.3165	10.15
40	0.3618	11.60
45	0.4070	13.05
50	0.4522	14.50
55	0.4974	15.95
60	0.5426	17.40
65	0.5879	18.85
70	0.6331	20.30
75	0.6783	21.75
80	0.7235	23.20
85	0.7687	24.65
90	0.8140	26.10
95	0.8592	27.55
100	0.9044	29.00

3.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below:



4. Two-wire Serial Bus Communication

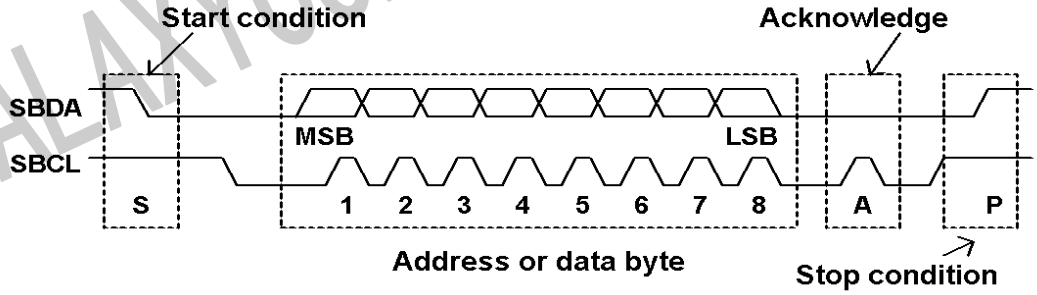
GC0310 Device Address:

serial bus write address = 0x42, serial bus read address = 0x43

4.1 Protocol

The host must perform the role of a communications master and GC0310 acts as either a slave receiver or transmitter. The master must do

- ◆Generate the **Start(S)/Stop(P)** condition
- ◆Provide the serial clock on **SBCL**.



Single Register Writing:

S	42H	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	42H	A	Register Address	A	Data(1)	A	.....	Data(N)	A	P

Single Register Reading:

S	42H	A	Register Address	A	S	43H	A	Data	NA	P

Notes:

From master to slave From slave to master

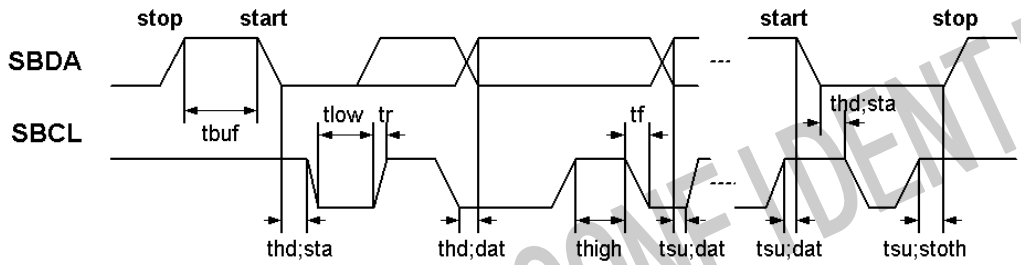
S: Start condition **P:** Stop condition

A: Acknowledge bit **NA:** No acknowledge

Register Address: Sensor register address

Data: Sensor register value

4.2 Serial Bus Timing

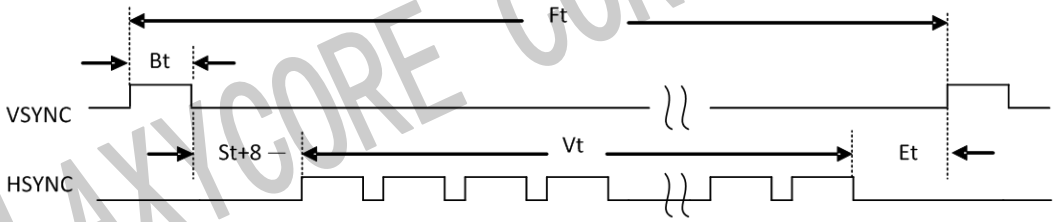


Parameter	Symbol	Min.	Max.	Unit
SBCL clock frequency	fscl	0	400	KHz
Bus free time between a stop and a start	tbuf	1.2	*	μs
Hold time for a repeated start	thd;sta	1.0	*	μs
LOW period of SBCL	tlow	1.2	*	μs
HIGH period of SBCL	thigh	1.0	*	μs
Set-up time for a repeated start	tsu;sta	1.2	*	ns
Data hold time	thd;dat	1.3	*	ns
Data Set-up time	tsu;dat	250	*	ns
Rise time of SBCL, SBDA	tr	*	250	ns
Fall time of SBCL, SBDA	tf	*	300	ns
Set-up time for a stop	tsu;sto	1.2	*	μs
Capacitive load of bus line (SBCL, SBDA)	Cb	*	*	pf

5. Application

5.1 DVP Timing

Suppose Vsync is low active and Hsync is high active, and output format is YCbCr/RGB565, then the timing of Vsync and Hsync is bellowing (take capture mode for example，preview mode is the same):



Ft =VB+ Vt +8 (unit is row_time)

VB = Bt + St + Et, Vblank/Dummy line, setting by register P0:0x07 and P0:0x08.

Ft -> Frame time, one frame time.

Bt -> Blank time, Vsync no active time.

St -> Start time, setting by register P0:0x12.

Et –> End time, setting by register P0:0x13.

Vt -> valid line time. VGA is 480, Vt = win_height-8, win_height is setting by register P0:0x0d and P0:0x0e.

When exp_time ≤ win_height+VB, Bt = VB – St - Et. Frame rate is controlled by window_height + VB.

When exp_time > win_height + VB, Bt = exp_time - win_height – St - Et. Frame rate is controlled by exp_time.

The following is row_time calculate:

row_time = Hb + Sh_delay + win_width /2+ 4.

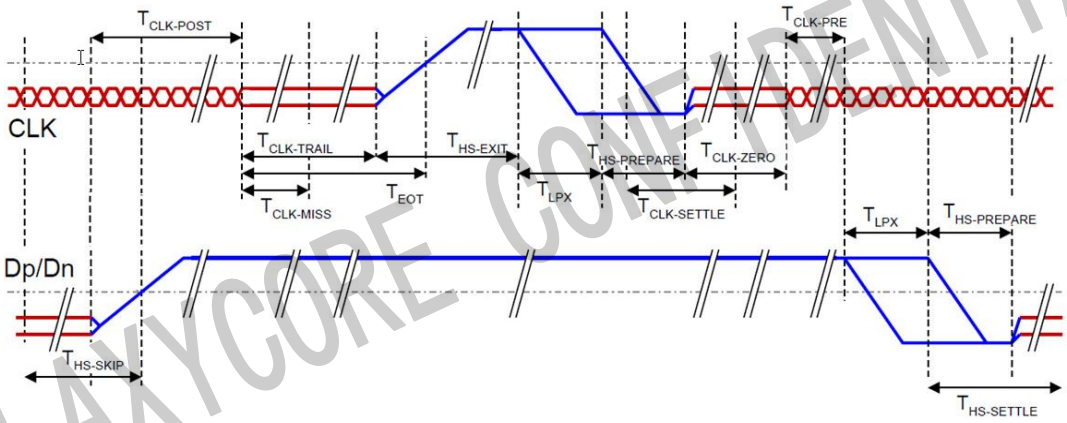
Hb –> HBlank or dummy pixel，Setting by register P0:0x05 and P0:0x06.

Sh_delay -> Setting by register P0:0x11.

win_width -> Setting by register P0:0x0f and P0:0x10, win_width = final_output_width + 8. So for VGA, we should set win_width as 648.

5.2 MIPI

5.2.1 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

  T_{CLK_PRE}: setting by Register P3: 0x24

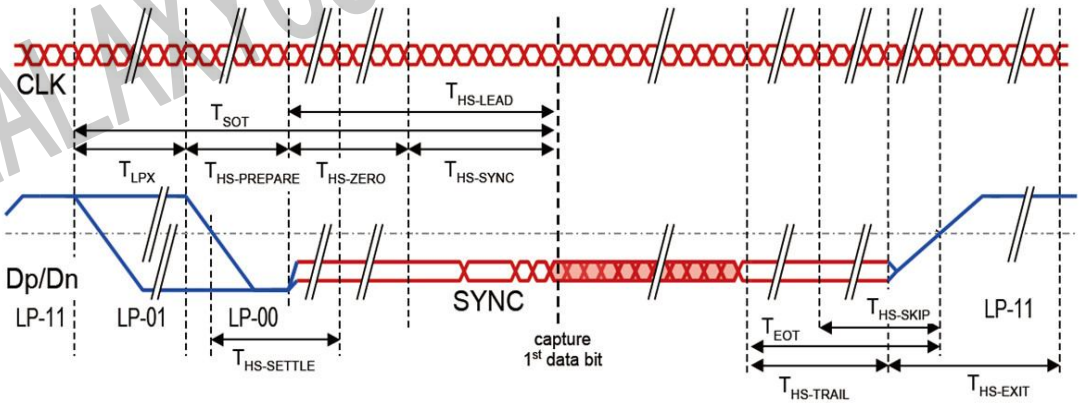
  $T_{CLK\_HS\_PRE}$: setting by Register P3: 0x22

  T_{CLK_POST} : setting by Register P3: 0x25

  T_{CLK_ZERO}: setting by Register P3: 0x23

  T_{CLK_TRAIL}: setting by Register P3: 0x26

5.2.2 Data Burst



Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

T_{LPX}: setting by Register P3:0x21

$T_{HS\_PREPARE}$: setting by Register P3: 0x29

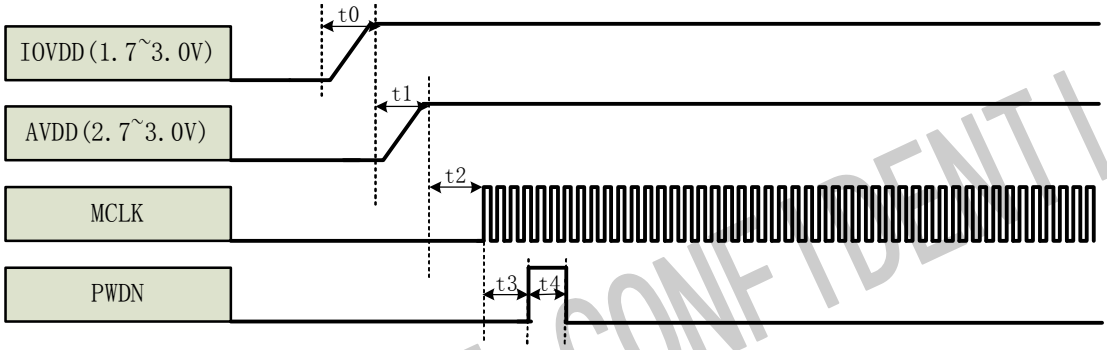
T_{HS_ZERO}: setting by Register P3: 0x2a

T_{HS_TRAIL}: setting by Register P3: 0x2b

T_{HS_EXIT}: setting by Register P3: 0x27

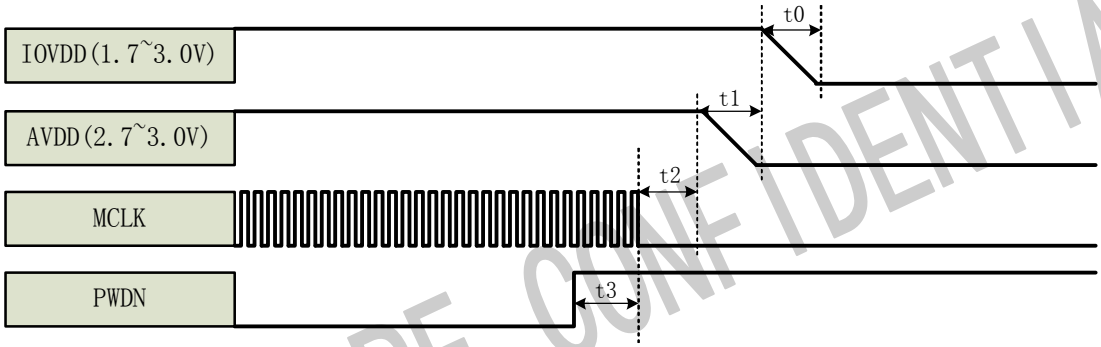
5.3 Power on/off sequence

5.3.1 Power On Sequence



Parameter	Description	Min.	Max.	Unit
t0	IOVDD rising time	50		us
t1	From IOVDD to AVDD	≥0		us
t2	From AVDD to MCLK applied	≥0		us
t3	From MCLK applied to PWDN pull high	≥0		us
t4	PWDN from pull high to pull low	>1		us

5.3.2 Power Off Sequence



Parameter	Description	Min.	Max.	Unit
t0	From AVDD to IOVDD falling time	≥0		us
t1	AVDD falling time	≥0		us
t2	From MCLK disable to sensor AVDD power down	≥0		us
t3	From sensor disable to MCLK disable	≥0		us

- **Recommended power on/off sequence is above.**
- **If you have special requirements in application, please contact with us to confirm.**

5.4 DC Parameters

Symbol		Parameter	Min	Typ	Max	Unit
Supply						
V_{AVDD28}		Power supply	2.7	2.8	3.0	V
V_{IOVDD}		Power Supply(Digital I/O)	1.7	1.8	3.0	V
I_{AVDD28}		Active(operating) current	-	10	20	mA
I_{IOVDD}	1.8V		-	18	25	mA
	2.8V		-	20	30	mA
I_{DDS_PWD}		Standby Current	-	30	50	uA
Digital Input(Typical conditions: AVDD28=2.8V，IOVDD=1.8V)						
V_{IH}		Input voltage HIGH	1.4			V
V_{IL}		Input voltage LOW			0.6	V
Digital Output(Typical conditions: AVDD28=2.8V，IOVDD=1.8V)						
V_{OH}		Output voltage HIGH	1.6			V
V_{OL}		Output voltage LOW			0.2	V

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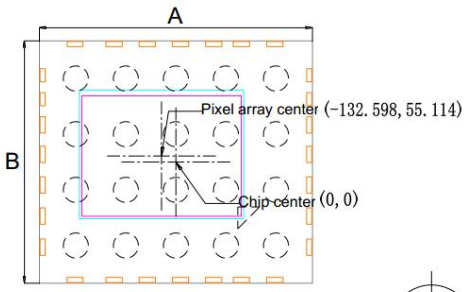
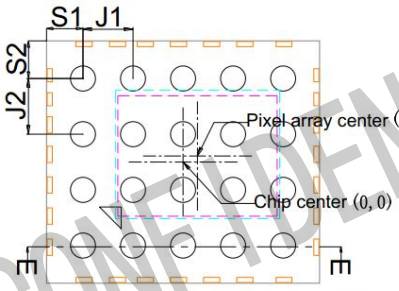
6. Package Specification



TOP VIEW(Image side)



BOTTOM VIEW(BGA side)

CROSS SECTION VIEW (E-E)

Notch

Unit:um
Package Size:2510*2220
Ball diameter:230
Ball pitch:X-460um,Y-510um

Parameter	Symbol	Nominal	Min.	Max.
		μm		
Package Body Dimension X	A	5620	5595	5645
Package Body Dimension Y	B	3740	3715	3765
Package Height	C	735	680	790
Ball Height	C1	175	145	205
Package Body Thickness	C2	560	525	595
Glass Thickness	C3	400	390	410
Cavity Height (glass to pixel distance)	C4	30	26	34
Cavity Wall + Epoxy Thickness (glass to the wafer bonding top point)	C5	32.5	27.5	37.5
Ball Diameter	D	350	320	380
Total Pin Count	N	28		
Pins Count X axis	N1	6		
Pins Count Y axis	N2	5		
Pins Pitch X axis	J1	800		
Pins Pitch Y axis	J2	750		
Edge to Pin Center Distance along X	S1	1083.645	1083.615	1083.675
Edge to Pin Center Distance along Y	S2	360	359.97	360.03

7. Register List

System Register

Address	Name	Width	Default Value	R/W	Description
0xf0	**Sensor_ID_high**	**8**	**0xa3**	**RO**	**Sensor_ID**
0xf1	**Sensor_ID_low**	**8**	**0x10**	**RO**	**Sensor_ID**
0xf2	mipi_pad_mode pad_vb_hiz_mode oen_flop_mode	8	0x01	RW	[7] mipi_pad_mode [3] pad_vb_hiz_mode [0] oen_flop_mode
0xf3	sync_output_en data_output_en	8	0x00	RW	[7:5] sync_output_en [7] pclk_en [6] hsync_en [5] vsync_en [4:0] data_output_en
0xf4	I2C_open_en up_dn pwd_dn	5	0x00		[4] I2C_open_en [3:2] up_dn 00: not pull 01: pull down 10: pull up 11: illegal [1] NA [0] PWD dn 0: pull down 1: not pull
0xf5	sck_delay_mode	3	0x00	RW	[2:0] sck_delay_mode
0xf6	sync_hiz data_hiz	8	0x00	RW	[7:5] sync_hiz [4:0] data_hiz
0xf7	PLL_mode1	8	0x10	RW	[7] dvp mode [6:4] serial_clk_div [3] clk_double [2] use pll [1] div2en [0] pll_en
0xf8	PLL_mode2	8	0x00	RW	[7] freq_div2_en [6] freq_div2_close frame mode

					[5:0] divx4
0xf9	cm_mode	8	0x00	RW	[7] regf clk enable [6] use internal clk [5] clk_3_2_div [4] sync_use pll [3] isp all clock enable [2] pll_lock [1] NA [0] not_use_pll
0xfa	clk_div_mode	8	0x00	RW	[7:4] +1 represent the frequency division number [3:0] represent the high level in one pulse after frequency division
0xfc	spi_pad_mode analog_pwc	8	0x03	RW	[7] SPI pad mode [6:4] NA [3:0] analog_pwc
0xfd	clk_div2_mode	8	0x11	RW	[7:4] divide_by [3:0] clock duty
0xfe	Reset related	8	0x00	RW	[7] soft_reset [6:5] NA [4] CISCTL_restart_n, restart CISCTL, effective low [3:2] NA [1:0] page_select

Analog & CISCTL

Address	Name	Width	Default Value	R/W	Description
P0:0x00	Reserved	8	0x01	RW	Reserved
P0:0x01	Reserved	8	0x03	RW	Reserved
P0:0x02	Reserved	8	0x44	RW	Reserved
P0:0x03	Exposure[11:8]	4	0x00	RW	[7:4] NA [3:0] Exposure[11:8], use row time as the unit
P0:0x04	Exposure[7:0]	8	0x10	RW	Exposure[7:0]
P0:0x05	HB[11:8]	4	0x00	RW	Horizontal blanking, unit pixel clock
P0:0x06	HB[7:0]	8	0x6a	RW	
P0:0x07	VB[11:8]	4	0x00	RW	Vertical blanking, if current exposure < (Vb + window Height) , frame rate will be (Vb + window Height); otherwise frame rate will be determined by
P0:0x08	VB[7:0]	8	0x6c	RW	

					exposure
P0:0x09	Row_start[8]	1	0x00	RW	Defines the starting row of the pixel array
P0:0x0a	Row_start[7:0]	8	0x00	RW	
P0:0x0b	Column_start[9:8]	2	0x00	RW	Defines the starting column of the pixel array
P0:0x0c	Column_start[7:0]	8	0x04	RW	
P0:0x0d	Window_height[8]	1	0x01	RW	[7:1] NA [0] Window height[8]
P0:0x0e	Window_height[7:0]	8	0xe8	RW	Window height[7:0]
P0:0x0f	Window_width[9:8]	2	0x02	RW	[7:2] NA [1:0] Window width[9:8]
P0:0x10	Window_width[7:0]	8	0x88	RW	window width[7:0]
P0:0x11	sh_delay	8	0x2a	RW	sh_delay
P0:0x12	Vs_st	8	0x09	RW	number of Row time from frame start to first HSYNC valid
P0:0x13	Vs_et	8	0x04	RW	number of Row time from last HSYNC valid to frame end Notice the relation with VB, VB > vs_st+vs_et
P0:0x14	Reserved	8	0xc0	RW	Reserved
P0:0x15	Reserved	8	0x01	RW	Reserved
P0:0x16	Reserved	7	0x10	RW	Reserved
P0:0x17	Mirror & Flip	8	0x00	RW	[7:2] Reserved [1] Flip [0] mirror
P0:0x18	Reserved	8	0x0a	RW	Reserved
P0:0x19	Reserved	8	0x05	RW	Reserved
P0:0x1a	Reserved	8	0x03	RW	Reserved
P0:0x1b	Reserved	8	0x44	RW	Reserved
P0:0x1c	Reserved	8	0x1c	RW	Reserved
P0:0x1e	Reserved	8	0x12	RW	Reserved
P0:0x1f	Reserved	8	0x00	RW	Reserved
P0:0x20	Reserved	8	0x00	RW	Reserved
P0:0x21	Reserved	8	0x00	RW	Reserved
P0:0x22	Reserved	8	0xba	RW	Reserved
P0:0x23	Reserved	8	0x05	RW	Reserved

P0:0x24	PAD_drv	8	0x15	RW	[7:6]data_low_drv [5:4] sync_drv [3:2] data_high_drv [1:0] pclk_drv
P0:0x25	Reserved	8	0x00	RW	Reserved
P0:0x27	Reserved	8	0x00	RW	Reserved
P0:0x34	Reserved	8	0x00	RW	Reserved

BLK

Address	Name	Width	Default Value	R/W	Description
P0:0x26	Blk_mode	8	0x23	RW	[7:2] Reserved [1] dark_current_en [0] offset_en
P0:0x28	BLK_limit_value	8	0xff	RW	When Dark data big than it, while get this to replace it for protect dark data. low align 11bits
P0:0x29	global_offset	8	0x00	RW	low align 11bits
P0:0x2a	Current_G1_offset	8		RO	Current_G1_offset
P0:0x2b	Current_R1_offset	8		RO	Current_R1_offset
P0:0x2c	Current_B2_offset	8		RO	Current_B2_offset
P0:0x2d	Current_G2_offset	8		RO	Current_G2_offset
P0:0x2e	current_G1_dark_current	8		RO	current_G1_dark_current
P0:0x2f	current_R1_dark_current	8		RO	current_R1_dark_current
P0:0x30	current_B2_dark_current	8		RO	current_B2_dark_current
P0:0x31	current_G2_dark_current	8		RO	current_G2_dark_current
P0:0x32	Exp_rate_darkc	8	0x00	RW	Exp_rate_darkc
P0:0x33	offset_ratio	6	0x18	RW	[5:0] offset ratio of G1 channel, 1.5 bits
P0:0x35	Reserved	8	0x80	RW	Reserved
P0:0x37	dark_current_ratio	6	0x20	RW	[5:0] dark current ratio of G1 channel, 1.5bits

P0:0x38	offset_X_inv_ratio	6	0x08	RW	[5:0] offset_X_inv_ratio, 1.5bits
P0:0x47	Reserved	8	0x27	RW	Reserved
P0:0x1d	Reserved	8	0xff	RW	Reserved
P0:0x4e	select_row_bits	8	0x66	RW	select_row_bits
P0:0xa8	Reserved	2	0x02	RW	Reserved
P0:0xa9	Reserved	8	0x88	RW	Reserved

ISP Related

Address	Name	Width	Default Value	R/W	Description
P0:0x40	Block_enable_1	8	0xff	RW	[7] Reserved [6] gamma enable [5] CC_en [4] EE_en [3] INTP_en [2] DN_en [1] DD_en [0] LSC_en
P0:0x41	Block_enable_2	8	0xfd	RW	Reserved
P0:0x42	AAAA_enable	8	0x18	RW	[7:2] Reserved [1] AWB enable [0] Reserved
P0:0x43	special_effect	8	0x00	RW	[7:3] NA [2] edge_map [1] CrCb_fixed_en [0] Inverse color
P0:0x44	Output_format	8	0x02	RW	[7] YUV420_row_switch [6] YUV420_col_switch [5] 420 legacy mode [4:0] output data mode, check details in out 5'h00 Cb Y Cr Y 5'h01 Cr Y Cb Y 5'h02 Y Cb Y Cr 5'h03 Y Cr Y Cb 5'h04 LSC bypass, C/Y 5'h05 LSC bypass, Y/C 5'h06 RGB 565

GALAXYCORE CONFIDENTIAL

					5'h0f bypass 11bits 5'h17 switch odd/even column /row to controls output bayer pattern 5'h18 DNDD_bypass 5'h19 LSC_bypass 5'h1a pregain
P0:0x45	Reserved	8	0x53	RW	Reserved
P0:0x46	sync_mode	8	0x0f	RW	Reserved
P0:0x48	ANALOG_COL_gain, col_code	4	0x00	RO	[7:4] ANALOG_COL_gain [2:0] col_code
P0:0x49	bypass_mode	8	0x03	RW	[7:4] Reserved [3] is_8bit_bypass [2] is_10bit_bypass [1:0] bypass which 8bits from 11bit, in is_8bit_bypass mode
P0:0x4a	Reserved	8	0x83	RW	Reserved
P0:0x4b	debug_mode1	8	0x8e	RW	Reserved
P0:0x4c	debug_mode2	8	0x00	RW	[7:3] Reserved [2] input_test_image [1] LSC_test_image [0] test_image after EEINTP
P0:0x4d	debug_mode3	8	0x05	RW	[7:4] test_image_fix_value [3:0] Reserved
P0:0x50	win_mode	1	0x01	RW	[0] Crop out Window mode
P0:0x51	out_win_y1[8]	1	0x00	RW	[1:0] out_win_y1[8]
P0:0x52	out_win_y1[7:0]	8	0x00	RW	out _win_y1[7:0]
P0:0x53	out_win_x1[9:8]	2	0x00	RW	[1:0] out_win_x1[9:8]
P0:0x54	out_win_x1[7:0]	8	0x00	RW	out_win_x1[7:0]
P0:0x55	out_win_height[8]	1	0x01	RW	Out window height[8]
P0:0x56	out_win_height[7:0]	8	0xe0	RW	Out window height[7:0]
P0:0x57	out win_width[9:8]	2	0x02	RW	Out window width[9:8]
P0:0x58	out win_width[7:0]	8	0x80	RW	Out window width[7:0]
P0:0x5a	Reserved	8	0x84	RW	Reserved

GALAXYCORE CONFIDENTIAL

P0:0x5b	Reserved	8	0xc6	RW	Reserved
P0:0x5c	Reserved	8	0xeb	RW	Reserved
P0:0x5d	Reserved	8	0x0f	RW	Reserved

AUTO GAMMA

Address	Name	Width	Default Value	R/W	Description
P0:0x5f	Gamma_0	8	0x0d	RW	Knee0=0
P0:0x60	Gamma_1	8	0x24	RW	Knee1=8
P0:0x61	Gamma_2	8	0x36	RW	Knee2=16
P0:0x62	Gamma_3	8	0x45	RW	Knee3=24
P0:0x63	Gamma_4	8	0x4f	RW	Knee4=32
P0:0x64	Gamma_5	8	0x5b	RW	Knee5=40
P0:0x65	Gamma_6	8	0x65	RW	Knee6=48
P0:0x66	Gamma_7	8	0x76	RW	Knee7=64
P0:0x67	Gamma_8	8	0x86	RW	Knee8=80
P0:0x68	Gamma_9	8	0x94	RW	Knee9=96
P0:0x69	Gamma_10	8	0xa1	RW	Knee10=112
P0:0x6a	Gamma_11	8	0xad	RW	Knee11=128
P0:0x6b	Gamma_12	8	0xba	RW	Knee12=144
P0:0x6c	Gamma_13	8	0xc4	RW	Knee13=160
P0:0x6d	Gamma_14	8	0xd9	RW	Knee14=192
P0:0x6e	Gamma_15	8	0xed	RW	Knee15=224
P0:0x6f	Gamma_16	8	0xff	RW	Knee16=256
P0:0xb1	Reserved	8	0x38	RW	Reserved
P0:0xb2	Reserved	8	0x40	RW	
P0:0xb3	Reserved	8	0x20	RW	Reserved
P0:0xb4	Reserved	8	0x24	RW	

GLOBAL/PRE/POSTGAIN

Address	Name	Width	Default Value	R/W	Description
P0:0x70	Global_gain	8	0x40	RW	Global_gain
P0:0x71	Auto_pregain	8	0x20	RO	Auto_pregain
P0:0x72	Auto_postgain	8	0x40	RO	Auto_postgain
P0:0x73	Channel_gain_R	8	0x80	RW	Channel_gain_R
P0:0x74	Channel_gain_G1	8	0x80	RW	Channel_gain_G1

P0:0x75	Channel_gain_G2	8	0x80	RW	Channel_gain_G2
P0:0x76	Channel_gain_B	8	0x80	RW	Channel_gain_B
P0:0x77	AWB_R_gain	8	0x50	RO	AWB_R_gain
P0:0x78	AWB_G_gain	8	0x40	RO	AWB_G_gain
P0:0x79	AWB_B_gain	8	0x48	RO	AWB_B_gain
P0:0x7a	R_ratio	8	0x80	RW	R_ratio
P0:0x7b	G_ratio	8	0x80	RW	G_ratio
P0:0x7c	B_ratio	8	0x80	RW	B_ratio
P0:0x7d	Reserved	1	0x00	RW	Reserved

DNDD/DITHER

Address	Name	Width	Default Value	R/W	Description
P0:0x80	DN_mode_en	8	0xc1	RW	Reserved
P0:0x81	DD_mode_en	4	0x08	RW	Reserved
P0:0x82	Reserved	6	0x08	RW	Reserved
P0:0x83	Reserved	7	0x10	RW	Reserved
P0:0x84	DD_dark_TH	6	0x0a	RW	DD_dark_TH
P0:0x86	Reserved	8	0x50	RW	Reserved
P0:0x87	Reserved	6	0x30	RW	
P0:0x88	Reserved	8	0x15	RW	
P0:0x89	ASDE_low_luma_value_DD_th2	8	0x20	RW	ASDE_low_luma_value_DD_th
P0:0x8a	ASDE_low_luma_value_DD_th3	8	0x18	RW	
P0:0x8b	ASDE_low_luma_value_DD_th4	8	0x10	RW	
P0:0x8c	Reserved	6	0x08	RW	Reserved
P0:0x8d	Reserved	7	0x10	RW	Reserved

INTPEE （Interpolation and Edge Enhancement）

Address	Name	Width	Default Value	R/W	Description
P0:0x8f	Reserved	8	0x55	RW	Reserved

P0:0x90	EEINTP mode 1	8	0xac	RW	[7] LP_edge_en [6:4] Reserved [3] LP_intp_en [2:0] Reserved
P0:0x91	EEINTP mode 2	8	0x00	RW	[7] HP_mode1 [6] HP_mode2 [5] only 2 direction [4] LP_intp_share [3] only_defect_map [2] map_dir [0] edge_level
P0:0x92	direction_TH1	8	0x05	RW	[5:0] Direction THreshold
P0:0x93	Diff_HV_TI_TH	5	0x00	RW	[4:0] Diff_HV_TI_TH
P0:0x94	Direction diff TH	4	0x05	RW	[5] NA [4:0] Direction diff TH
P0:0x95	Edge1 effect Edge2 effect	8	0x45	RW	[7:4] edge1 effect [3:0] edge2 effect
P0:0x96	Edge_max Edge_th	8	0x82	RW	[7:4] edge max [3:0] edge threshold

RGB gamma

Address	Name	Width	Default Value	R/W	Description
P0:0xbf	RGB_Gamma_0	8	0x10	RW	Each out value of knee_i. Knee0=0
P0:0xc0	RGB_Gamma_1	8	0x20	RW	Knee1=8
P0:0xc1	RGB_Gamma_2	8	0x38	RW	Knee2=16
P0:0xc2	RGB_Gamma_3	8	0x4e	RW	Knee3=24
P0:0xc3	RGB_Gamma_4	8	0x63	RW	Knee4=32
P0:0xc4	RGB_Gamma_5	8	0x76	RW	Knee5=40
P0:0xc5	RGB_Gamma_6	8	0x87	RW	Knee6=48
P0:0xc6	RGB_Gamma_7	8	0xa2	RW	Knee7=64
P0:0xc7	RGB_Gamma_	8	0xb8	RW	Knee8=80

	8				
P0:0xc8	RGB_Gamma_9	8	0xca	RW	Knee9=96
P0:0xc9	RGB_Gamma_10	8	0xd8	RW	Knee10=112
P0:0xca	RGB_Gamma_11	8	0xe3	RW	Knee11=128
P0:0xcb	RGB_Gamma_12	8	0xeb	RW	Knee12=144
P0:0xcc	RGB_Gamma_13	8	0xf0	RW	Knee13 =160
P0:0xcd	RGB_Gamma_14	8	0xf8	RW	Knee14 = 192
P0:0xce	RGB_Gamma_15	8	0xfd	RW	Knee15 = 224
P0:0xcf	RGB_Gamma_16	8	0xff	RW	Knee16 = 256

YCP

Address	Name	Width	Default Value	R/W	Description
P0:0xd0	Global saturation	8	0x40	RW	Global saturation
P0:0xd1	saturation_Cb	8	0x20	RW	Cb saturation
P0:0xd2	saturation_Cr	8	0x20	RW	Cr saturation
P0:0xd3	luma_contrast	8	0x40	RW	Luma_contrast
P0:0xd4	Contrast_center	8	0x80	RW	Contrast center value
P0:0xd5	Luma_offset	8	0x00	RW	Add offset on luma value
P0:0xd6	skin_Cb_center	8	0xe8	RW	Cb criteria for skin detection
P0:0xd7	skin_Cr_center	8	0x20	RW	Cr criteria for skin detection
P0:0xd8	Reserved	6	0x18	RW	Reserved
P0:0xd9	Reserved	8	0xe3	RW	Reserved
P0:0xda	Fixed_Cb	8	0x00	RW	Fixed_Cb
P0:0xdb	Fixed_Cr	8	0x00	RW	Fixed_Cr
P0:0xdd	Reserved	8	0x38	RW	Reserved
P0:0xde	Reserved	6	0x38	RW	Reserved

AEC

Address	Name	Width	Default Value	R/W	Description
P0:0x4f	AEC_EN	1	0x00	RW	[0] AEC_en
P1:0x01	Reserved	3	0x00	RW	Reserved
P1:0x05	AEC_center_x1	8	0x20	RW	[7:0] AEC_center_x1
P1:0x06	AEC_center_x2	8	0x40	RW	[7:0] AEC_center_x2
P1:0x07	AEC_center_y1	8	0x40	RW	[7:0] AEC_center_y1
P1:0x08	AEC_center_y2	8	0x60	RW	[7:0] AEC_center_y2
P1:0x09	Reserved	8	0x00	RW	Reserved
P1:0x0a	AEC_mode1	8	0x01	RW	[7:3] Reserved [2] gain mode [1:0] skip mode
P1:0x0b	AEC_mode2	8	0x21	RW	[7] fix target [6:4] AEC take action every N frame [3:0] Reserved
P1:0x0c	AEC_mode3	8	0x01	RW	[7] Reserved [6:4] center weight mode [3:2] skin weight mode [1] NA [0] Reserved
P1:0x0d	AEC_mode4	8	0x00	RW	Reserved
P1:0x0e	Reserved	8	0x45	RW	Reserved
P1:0x0f	Reserved	8	0x65	RW	Reserved
P1:0x10	Reserved	8	0x65	RW	Reserved
P1:0x11	Reserved	8	0x40	RW	AEC outdoor slope
P1:0x12	Reserved	8	0x51	RW	Reserved
P1:0x13	AEC_target_Y	8	0x50	RW	expected luminance value
P1:0x14	Y_average	8	0x10	RO	Current frame luminance average
P1:0x15	Reserved	8	0x80	RW	Reserved
P1:0x16	Reserved	8	0xeo	RW	Reserved
P1:0x17	Reserved	8	0xe0	RW	Reserved
P1:0x18	AEC_mode	8	0x91	RW	[7:4] AEC slow margin [2:0] AEC slow speed
P1:0x19	AEC_mode	8	0x95	RW	[7:4] AEC fast margin [2:0] AEC fast speed
P1:0x1a	AEC_mode	8	0x96	RW	Gain change criteria
P1:0x1b	Reserved	8	0x01	RW	Reserved
P1:0x1c	Reserved	8	0x11	RW	Reserved
P1:0x1d	Reserved	7	0x07	RW	Reserved
P1:0x1e	Reserved	8	0x61	RW	Reserved

P1:0x1f	AEC_max_pre_dg_gain	8	0x30	RW	AEC_max_pre_dg_gain
P1:0x20	AEC_max_post_dg_gain	8	0xc0	RW	AEC_max_post_dg_gain
P1:0x21	Reserved	8	0x14	RW	Reserved
P1:0x22	Reserved	8	0x80	RW	Reserved
P1:0x23	Reserved	8	0x40	RW	Reserved
P1:0x24	Reserved	8	0x60	RW	Reserved
P1:0x25	AEC_anti_flicker_step[11:8]	4	0x01	RW	[7:4] NA [3:0] AEC anti flicker step[11:8]
P1:0x26	AEC_anti_flicker_step[7:0]	8	0x68	RW	AEC anti flicker step[7:0]
P1:0x27	AEC_exp_level_1[11:8]	4	0x04	RW	[7:4] NA [3:0] AEC exp level1[11:8]
P1:0x28	AEC_exp_level_1[7:0]	8	0x38	RW	AEC exp level1[7:0]
P1:0x29	AEC_exp_level_2[11:8]	4	0x05	RW	[7:4] NA [3:0] AEC exp level2[11:8]
P1:0x2a	AEC_exp_level_2[7:0]	8	0xa0	RW	AEC exp level2[7:0]
P1:0x2b	AEC_exp_level_3[11:8]	4	0x09	RW	[7:4] NA [3:0] AEC exp level3[11:8]
P1:0x2c	AEC_exp_level_3[7:0]	8	0xd8	RW	AEC exp level_3[7:0]
P1:0x2d	AEC_exp_level_4[11:8]	4	0x0e	RW	[7:4] NA [3:0] AEC exp level 4[11:8]
P1:0x2e	AEC_exp_level_4[7:0]	8	0x10	RW	AEC exp level 4 [7:0]
P1:0x2f	AEC_exp_level_5[11:8]	4	0x00	RW	[7:4] NA [3:0] AEC exp level 5[11:8]
P1:0x30	AEC_exp_level_5[7:0]	8	0xe0	RW	AEC exp level 5 [7:0]
P1:0x31	AEC_exp_level_6[11:8]	4	0x0c	RW	[7:4] NA [3:0] AEC exp level 6[11:8]
P1:0x32	AEC_exp_level_6[7:0]	8	0x20	RW	AEC exp level 6[7:0]
P1:0x33	AEC_exp_level_7[11:8]	4	0x0c	RW	[7:4] NA [3:0] AEC exp level7[11:8]
P1:0x34	AEC_exp_level_7[7:0]	8	0x20	RW	AEC exp level 7[7:0]
P1:0x35	AEC_max_dg_gain1	8	0x40	RW	5.3bits, AEC max dg gain1,x8

P1:0x36	AEC_max_dg_gain2	8	0x40	RW	5.3bits, AEC max dg gain2,x8
P1:0x37	AEC_max_dg_gain3	8	0x40	RW	5.3bits, AEC max dg gain3,x8
P!:0x38	AEC_max_dg_gain4	8	0x40	RW	5.3bits, AEC max dg gain4,x8
P1:0x39	AEC_max_dg_gain5	8	0x40	RW	5.3bits, AEC max dg gain5,x8
P1:0x3a	AEC_max_dg_gain6	8	0x40	RW	5.3bits, AEC max dg gain6,x8
P1:0x3b	AEC_max_dg_gain7	8	0x40	RW	5.3bits, AEC max dg gain7,x8
P1:0x3c	AEC_max_exp_level AEC_exp_min_l [11:8]	6	0x20	RW	[5:4] Max level setting [3:0] exp min[11:8]
P1:0x3d	AEC_exp_min_l [7:0]	8	0x04	RW	AEC_exp_min_l[7:0]
P1:0x3e	Reserved	8	0x40	RW	Reserved
P1:0x3f	Reserved	6	0x5a	RW	Reserved
P1:0x40	Reserved	8	0x80	RW	Reserved
P1:0x41	Reserved	8	0xb5	RW	Reserved
P1:0x42	Reserved	8	0x00	RW	Reserved
P1:0x43	Reserved	8	0x6a	RW	Reserved
P1:0x04	Reserved	8	0xff	RW	Reserved
P1:0x03	Reserved	7	0x70	RW	Reserved
P1:0x44	Reserved	3	0x03	RW	Reserved

AWB

Address	Name	Width	Default Value	R/W	Description
P1:0x50	AWB_PRE_mode	8	0xc0	RW	Reserved
P1:0x51	AWB_Parametre	8	0x80	RW	AWB_Parametre
P1:0x52	AWB_Parametre	8	0x01	RW	
P1:0x53	AWB_Parametre	8	0x80	RW	AWB_Parametre
P1:0x54	AWB_Parametre	8	0x0f	RW	

P1:0x55	AWB_Parametre	8	0x00	RW	AWB_Parametre
P1:0x56	AWB_Parametre	8	0x00	RW	AWB_Parametre
P1:0x58	AWB_Parametre	8	0x00	RW	AWB_Parametre
P1:0x59	AWB_PRE_RGB_low	8	0x01	RW	RGB pixel low THD
P1:0x5a	AWB_PRE_RGB_high	8	0xf0	RW	RGB pixel high THD
P1:0x5b	AWB_Parametre	8	0x00	RW	AWB_Parametre
P1:0x5c	Reserved	8	0xf0	RW	Reserved
P1:0x5d	Reserved	8	0x01	RW	Reserved
P1:0x60	Reserved	4	0x00	RW	Reserved
P1:0x61	Reserved	8	0xdc	RW	Reserved
P1:0x62	Reserved	8	0xca	RW	Reserved
P1:0x63	Reserved	8	0x80	RW	Reserved
P1:0x64	Reserved	8	0xa0	RW	Reserved
P1:0x65	Reserved	8	0x40	RW	Reserved
P1:0x66	Reserved	4	0x04	RW	Reserved
P1:0x67	Reserved	8	0x04	RW	Reserved
P1:0x68	Reserved	8	0xc0	RW	Reserved
P1:0x69	Reserved	8	0x40	RW	Reserved
P1:0x6a	Reserved	8	0x20	RW	Reserved
P1:0x6b	Reserved	8	0x41	RW	Reserved
P1:0x6c	Reserved	8	0x00	RW	Reserved
P1:0x6d	AWB_every_N	8	0x12	RW	AWB_every_N
P1:0x6e	Reserved	8	0x00	RW	Reserved
P1:0x6f	Reserved	8	0xa0	RW	Reserved
P1:0x70	Reserved	8	0x50	RW	Reserved
P1:0x76	AWB_R_gain_limit	8	0x70	RW	Channel gain limit for R, G, B.
P1:0x77	AWB_G_gain_limit	8	0x58	RW	
P1:0x78	AWB_B_gain_limit	8	0x78	RW	
P1:0x79	AWB_R_gain_out_h_limit	8	0x50	RW	outdoor R high limit
P1:0x7a	AWB_G_gain_out_h_limit	8	0x58	RW	outdoor G high limit

P1:0x7b	AWB_B_gain_out_h_limit	8	0x46	RW	outdoor B high limit

LSC

Address	Name	Width	Default Value	R/W	Description
P1:0xc1	LSC_row_center	7	0x60	RW	LSC row center
P1:0xc2	LSC_col_center	8	0x80	RW	LSC col center
P1:0xc3	LSC_b4_sign	1	0x00	RW	[0] sign of b4
P1:0xc4	LSC_red_b2	8	0x20	RW	b2 for channel red
P1:0xc5	LSC_green_b2	8	0x20	RW	b2 for channel green
P1:0xc6	LSC_blue_b2	8	0x20	RW	b2 for channel blue
P1:0xc7	LSC_red_b4	8	0x20	RW	b4 for channel red
P1:0xc8	LSC_green_b4	8	0x20	RW	b4 for channel green
P1:0xc9	LSC_blue_b4	8	0x20	RW	b4 for channel blue
P1:0xdc	Reserved	8	0x20	RW	Reserved
P1:0xdd	Reserved	8	0x10	RW	Reserved
P1:0xdf	Reserved	4	0x08	RW	Reserved

Measure Window

Address	Name	Width	Default Value	R/W	Description
P1:0xcc	C_big_win_x0	8	0x04	RW	Window setting for AEC & AWB
P1:0xcd	C_big_win_y0	8	0x02	RW	
P1:0xce	C_big_win_x1	8	0x60	RW	
P1:0xcf	C_big_win_y1	8	0x90	RW	

AUTO_CC

Address	Name	Width	Default Value	R/W	Description
P1:0xd0	CC_CT1_11	8	0x40	RW	CC_CT1
P1:0xd1	CC_CT1_12	8	0x00	RW	
P1:0xd2	CC_CT1_13	8	0x00	RW	
P1:0xd3	CC_CT1_21	8	0x00	RW	
P1:0xd4	CC_CT1_22	8	0x40	RW	
P1:0xd5	CC_CT1_23	8	0x00	RW	
P1:0xd6	CC_CT2_11	8	0x40	RW	CC_CT2

P1:0xd7	CC_CT2_12	8	0x00	RW	
P1:0xd8	CC_CT2_13	8	0x00	RW	
P1:0xd9	CC_CT2_21	8	0x00	RW	
P1:0xda	CC_CT2_22	8	0x40	RW	
P1:0xdb	CC_CT2_23	8	0x00	RW	

CSI/PHY1.0

Address	Name	Width	Default Value	R/W	Description
P3:0x01	DPHY_analog_mode1	8	0x00	RW	[5] CTD_lane0 [4] CTD_clk [2] phy_lane1_en [1] phy_lane0_en [0] phy_clk_en
P3:0x02	DPHY_analog_mode2	8	0x00	RW	[6:4] lane0_diff [2:0] clk_diff
P3:0x03	DPHY_analog_mode3	8	0x00	RW	[7] NA [6] NA [5] lane0_delay [4] clk_delay [2] lpldo_en [1:0] lpldo_r
P3:0x04	fifo_prog_full_level[7:0]	8	0x01	RW	fifo full level[7:0]
P3:0x05	fifo_prog_full_level[9:8]	2	0x00	RW	[1:0] fifo full level[9:8]
P3:0x06	fifo_mode	8	0x0c	RW	[7] free clk mode [6] manual_CSI2_up_mode [4] fifo_rst_mode [3] write_gate_mode [2] data_odd_mode [1] switch_read [0] switch_write
P3:0x10	BUF_CSI2_mode	8	0x00	RW	[7] lane_enable [6] NA [5] ULP_mode [4] MIPI_enable [3] bit10_swicth [2] RAW8 [1] line_sync_mode [0] double_lane

P3:0x11	LDI_set	8	0x1e	RW	RAW10 2b RAW8 2a YUV422 1e
P3:0x12	LWC_set[7:0]	8	0x00	RW	LWC set 640x5/4 RAW10
P3:0x13	LWC_set[15:8]	8	0x05	RW	
P3:0x14	SYNC_set	8	0xb8	RW	SYNC set
P3:0x15	DPHY_mode	8	0x00	RW	[7:4] trigger mode [7] read_reday [6] half [5] full [4] prog [3:2] switch msb mode [1:0] clklane_mode
P3:0x16	LP_set	8	0x09	RW	[7:6] hi-Z [3:2] 1 [1:0] 0
P3:0x17	MIPI_wdiv_set	8	0x00	RW	[7:4] NA [3:0] MIPI_wdiv_set
P3:0x20	T_init_set	8	0x80	RW	T_init_set
P3:0x21	T_LPX_set	8	0x10	RW	T_LPX_set
P3:0x22	T_CLK_HS_PREPARE_set	8	0x05	RW	T_CLK_HS_PREPARE_set
P3:0x23	T_CLK_zero_set	8	0x30	RW	T_CLK_zero_set
P3:0x24	T_CLK_PRE_set	8	0x02	RW	T_CLK_PRE_set
P3:0x25	T_CLK_POST_set	8	0x10	RW	T_CLK_POST_set
P3:0x26	T_CLK_TRAIL_set	8	0x08	RW	T_CLK_TRAIL_set
P3:0x27	T_HS_exit_set	8	0x10	RW	T_HS_exit_set
P3:0x28	T_wakeup_set	8	0xa0	RW	T_wakeup_set
P3:0x29	T_HS_PREPARE_set	8	0x06	RW	T_HS_PREPARE_set
P3:0x2a	T_HS_Zero_set	8	0x0a	RW	T_HS_Zero_set
P3:0x2b	T_HS_TRAIL_set	8	0x08	RW	T_HS_TRAIL_set
P3:0x30	MIPI_Test	2	0x00	RW	[1:0]MIPI_Test
P3:0x31	MIPI_Test_data0	8	0x96	RW	MIPI_Test_data0

P3:0x32	MIPI_Test_data1	8	0x3a	RW	MIPI_Test_data1
P3:0x33	MIPI_Test_data2	8	0x87	RW	MIPI_Test_data2
P3:0x34	MIPI_Test_data3	8	0xb5	RW	MIPI_Test_data3
P3:0x3f	fifo_error log	8		RO	Fifo error log
P3:0x40	output_buf_mode1	8	0x09	RW	[7:4] start_mode [3] dummy_mode [2:1] delay_half [0] output_en
P3:0x41	output_buf_mode2	3	0x00	RW	[3] dummy pclk mode [2] clk gating [1] pclk_polarity [0] hsync_polarity
P3:0x42	buf_win_width [7:0]	8	0x76	RW	Buffer window width
P3:0x43	buf_win_width [10:8]	3	0x0d	RW	

SPI

Address	Name	Width	Default Value	R/W	Description
P3:0x51	spi_mode	8	0x00	RW	[7:1] NA [0] spi_enable
P3:0x52	spi_global_mode	8	0x80	RW	[7] msb_first [6] NA [5] ddr_mode [4] NA [3:2] trigger_depth [1] CPHA [0] CPOL
P3:0x53	spi_data_mode	8	0x20	RW	[7] add crc [6] line number mode [5] add_sync_sign [4] data_idle_status [3:2] data_bandwidth [1:0] data_sequnce
P3:0x54	spi_master_mode	8	0x20	RW	[7] pause_enable [6] pause_reg [5] master_outformat [4] ssn_polarity

					[3:0] NA
P3:0x55	spi_master_mode1	8	0x81	RW	[7] data_start_finish_mode [6] ddr_4line_mode [5] free clk_mode [4] ddr_switch_mode [3] status_tail_enable [2] allow_pause_timer [1] NA [0] high_bandwidth
P3:0x57	pause_number	8	0x20	RW	pause_number, once transfer numbers, then pause
P3:0x58	timer_number	8	0x20	RW	timer_number, pause number clock,then restart transfermation
P3:0x59	wordout_mode	4	0x00	RW	wordout_mode [3] data_size [2] line_number [1] height [0] width
P3:0x5a	sync_format	8	0x01	RW	sync_format
P3:0x5b	image_width[7:0]	8	0x80	RW	image_width[7:0]
P3:0x5c	image_width[15:8]	8	0x02	RW	image_width[15:8]
P3:0x5d	image_height[7:0]	8	0Xe0	RW	image_height[7:0]
P3:0x5e	image_height[15:8]	8	0x01	RW	image_height[15:8]
P3:0x60	SYNC_code0	8	0x01	RW	SYNC_code0
P3:0x61	SYNC_code1	8	0x02	RW	SYNC_code1
P3:0x62	SYNC_code2	8	0x40	RW	SYNC_code2
P3:0x63	SYNC_code3	8	0x00	RW	SYNC_code3
P3:0x64	hsync_delay_mode sck_always bt656_mode	4	0x04	RW	[3] bt656_mode [2] sck_always [1:0]hsync_delay_mode
P3:0x65	SYNC_HEADER[23:16]	8	0xff	RW	SYNC_HEADER[23:16]
P3:0x66	SYNC_HEADER[15: 8]	8	0xff	RW	SYNC_HEADER[15: 8]
P3:0x67	SYNC_HEADER[7: 0]	8	0xff	RW	SYNC_HEADER[7: 0]