# MT7981B HW Application Note

(Keywords: SCH, PCB, power, thermal, flash)



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# 1 Document Revision History

| No. | Description | Edited by | Date of Approval |
|---|---|---|---|
| 1.0 | Initial Draft | Kim Su | 2021/11/5 |
| 1.1 | Update MT7981B thermal characteristic | Randy Chou | 2021/11/30 |
| 1.2 | Update section 4.2.4 DDR layout constraint<br>Update section 4.2.6 SGMII 0/1 design notice | Randy Chou | 2021/12/20 |
| 1.3 | Update section 4.1 & 4.2 SCH/PCB design<br>Update section 4.2.4 DDR layout constraint | Randy Chou | 2022/1/19 |
| 1.4 | Update section 5. PHY test command | Jason Chiang | 2022/2/22 |
| 1.5 | [Remove]p.38 WF0 to WF4, each port's chip AIQ out to A die (MT7976) trace length should be kept the same (< 1.5mm) | Kim Su | 2022/3/10 |
| | | | |

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## 2 Important Notice

For the performance consideration, the critical components show, no-change & critical parts, in the application note please follow MTK QVL design.

1. Crystal
2. DDR
3. Flash
4. PMIC
5. The E-Cap of the 3.3V Power supply out.

## 3 Product Requirement Document (PRD)

The following table covers the main features offered by MT7981B. Overall,

| Feature | Description |
|---|---|
| CPU | ARM CA53 (1.3GHz, Dual-core) |
| I-Cache, D-Cache | 32kB, 32kB per core |
| L2 Cache | 256KB |
| Security | Support 2* 256-bit Multi-key on OTP efuse<br>Support 64 versions OTP efuse for Anti-roll back |
| DRAM data | 16bit KGD |
| DDR3 | 2133 Mbps |
| WIFI | 2x2 11ax 2.4GHz + 2x2' 11ax 5GHz<br>Integrated PA, LNA and TR-SW 20/40/80/160MHz bandwidth<br>Support up to 1024QAM<br>Support external LNA and PA support (option) |
| Ethernet | HSGMII x 2 |
| HNAT/HQoS | HQoS 128 queues, SFQ 1K queues<br>HNAT (IPv4, IPv6 routing, DS-Lite, 6RD, 6to4) |
| USB | USB3.0 x 1(co-pin w/ SGMII) |
| SPI NAND Flash | ECC (BCH code) acceleration capable of 24-bit error correction<br>(w/. ECC engine) |
| SPI Flash (NOR) | Max 46MHz<br>data bit width x1/x2/x4<br>Support 4-byte address mode compatible with 3-byte address mode |
| eMMC | eMMC v4.5 @50MHz 3.3V |
| I2C | I2C x 1<br>100kHz, Support 7/10-bit addressing |
| SPI | SPI x 1<br>Support DMA and FIFO mode |
| UART | UART-Lite(2-pins) x 1<br>UART(4-pins) x 2 |
| Package | 13 mm x 11.7 mm, BGA |

**Table 3-1 : MT7981B main feature list**

## 4 Hardware Design Kit (HDK)

This application note records the details of MT7981B HW settings. Compared to the MT7981B datasheet, this supplement document is conveniently used during customer board level bring-up.

### 4.1 Schematic

#### 4.1.1 16bit DDR3 DRAM

The DDR3 Controller embedded in MT7981B, EMI_EXTR resistor is 40.2 ohm/1% and the DRAM ZQ resistor is 240 ohm/1%.

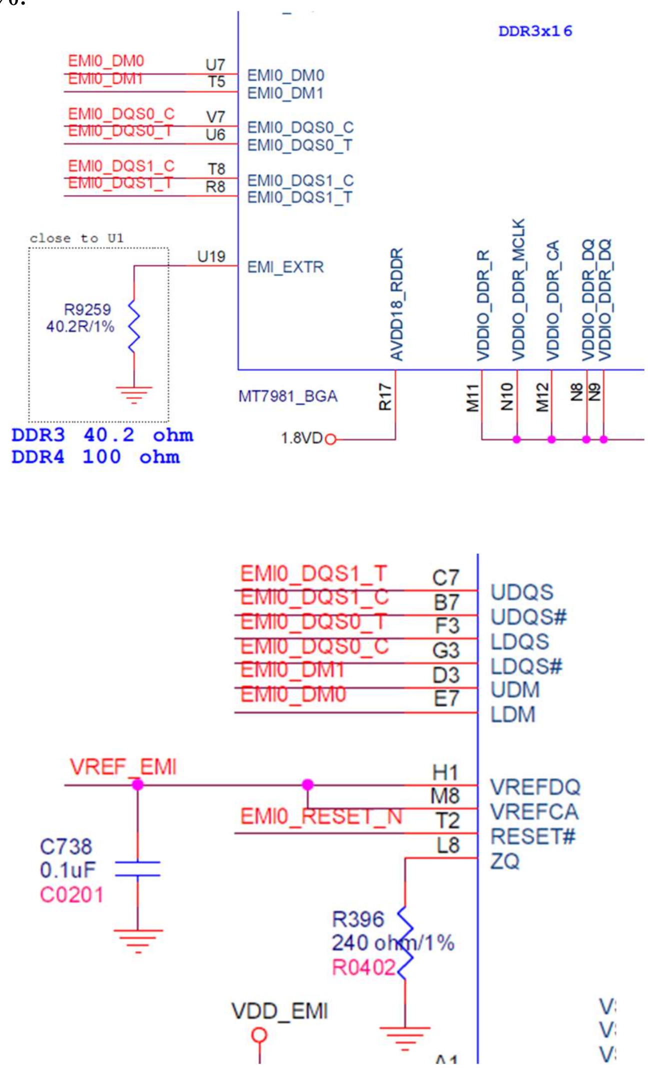



**Fig 4-1 : The DRAM reference registers**

DDR_VREF wire to EMI_TP for DRAM calibration, and schematic reserve VREF 0.1uF and as voltage divider 1K/1% tolerance.

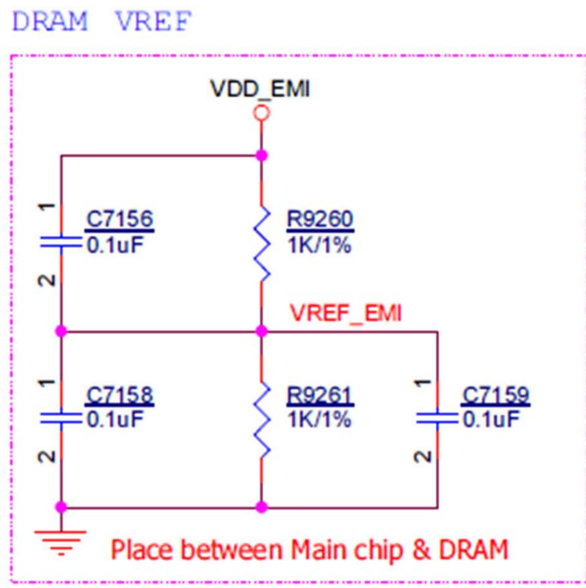



**Fig 4-2 : The capacitors of DRAM VREF**

### 4.1.2 USB2/3 design

USB2_1 is used for USB3 connector

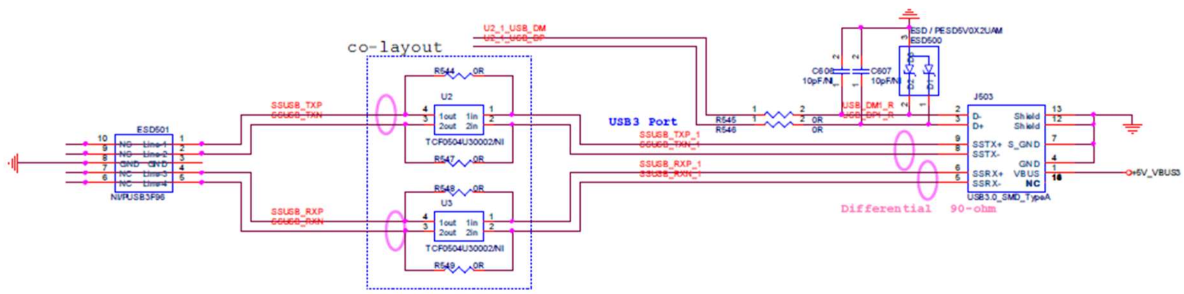



**Fig 4-3 : USB2_1/USB3**

### 4.1.3 Power cap list

Table 4-1 displays the de-coupling cap values of the power trace. The placement guidelines is small capacitors close to MT7981B main chip and the large capacitors are near to the power source.

| Pin name | 0.87V/AVDD18/AVDD12/AVDD09 de-coupling cap value |
|---|---|
| DVDD_CORE | 0.87V/4.1A (0201 1uF*7+ 0201 0.1F*6+10uf) |
| AFE | AVDD18_WBG cap value:1uF+0.1uF<br>AVDD12_WBG cap value:1uF+0.1uF |
| BG_OUT | 1uF |
| REFP | 1uF |
| VQPS | 1.8VD 0.1uF+1uF(no use, tied to GND) |
| USB3 | U3_AVDD09_SSUSB cap :0.1uF+1uF<br>U3_AVDD18_SSUSB cap :0.1uF+1uF |
| USB2 | AVDD18_USB cap :0.1uF+1uF (share u3, work for u3 or u2)<br>AVDD33_USB cap 0.1uF+1uF |
| (H)SGMII | AVDD09_SGMII cap :0.1uF+1uF<br>AVDD18_SGMII cap :0.1uF+1uF |
| DRAM | follow HDK |
| DRAM controller | follow HDK |

**Table 4-1 : Power cap list**

#### 4.1.3.1 U3/HSGMII Power cap

Please follow HDK to add USB3.0/HSGMII cap 1uF+0.1uF for each power pin.

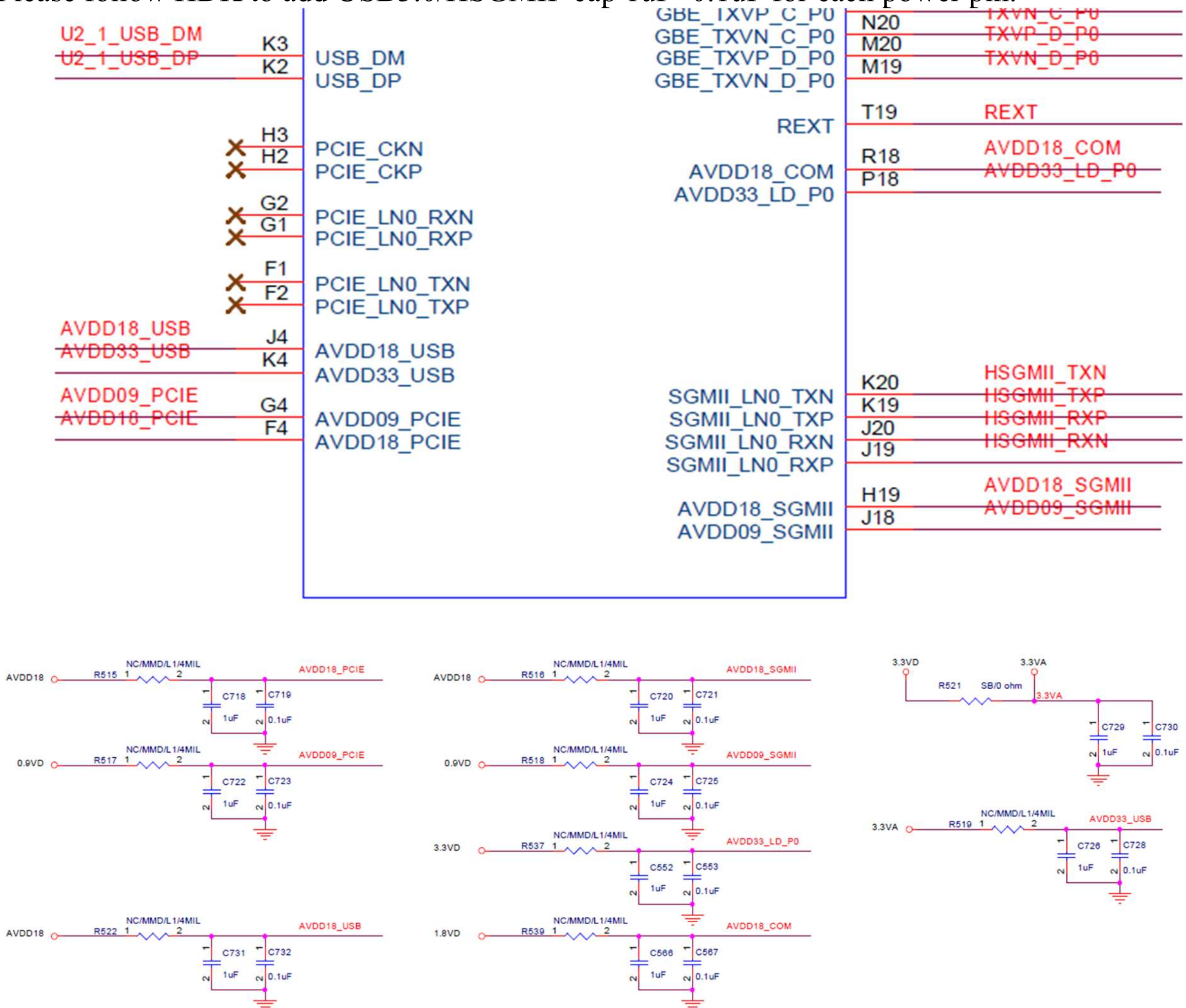



Fig 4-4 : U3+HSGMII Power caps

#### 4.1.3.2 DRAM Power Caps

Please follow HDK to add SOC_DDR Controller Caps follow HDK

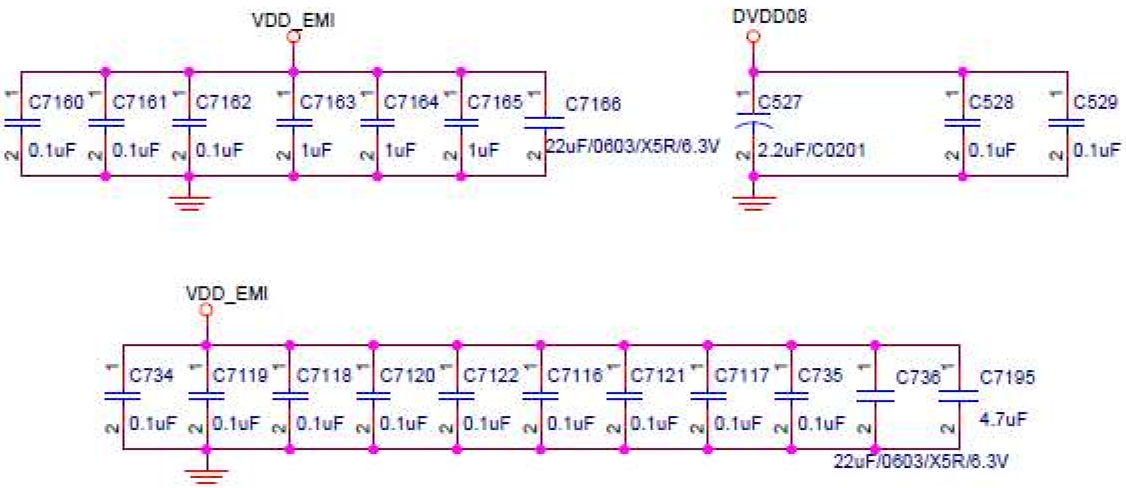



**Fig 4-5 : DRAM controller and DRAM Power Cap**

#### 4.1.3.3 VCCK CORE Power cap

Please follow HDK to add VCCK for power pin.

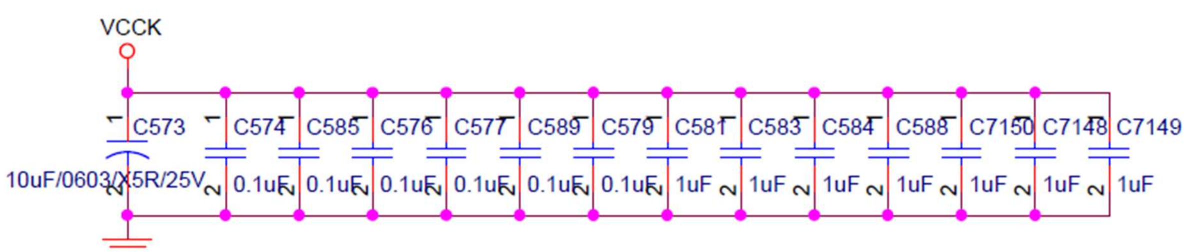



**Fig 4-6 : VCCK Power caps**

### 4.1.4 MT7981B+MT7976C Power Plan

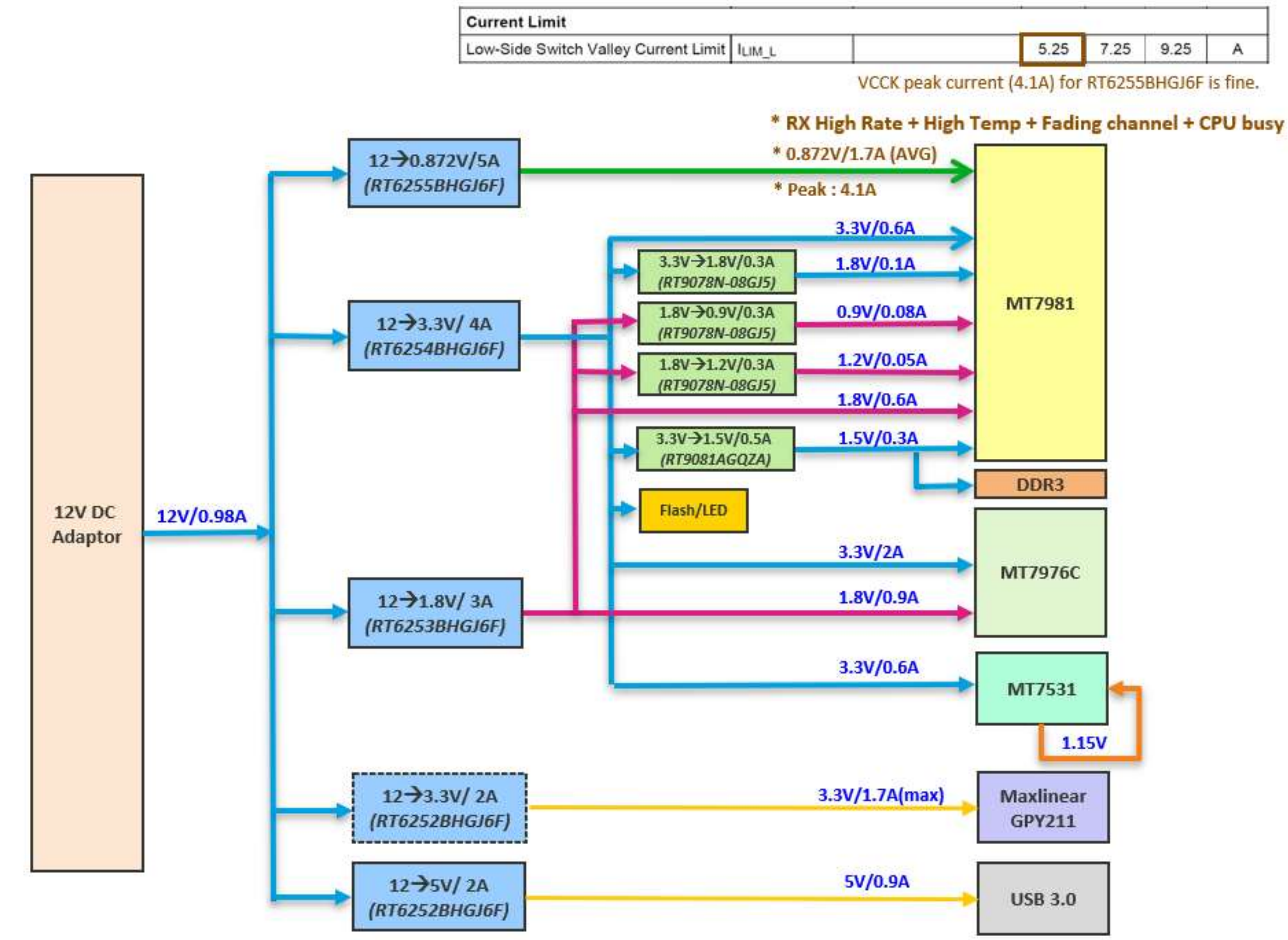



**Fig 4-7 : MT7981B + MT7976C power plan**

The MT7981B+MT7976 total core powers are mentioned in Table 4-2 (refer to the power plan example of Fig 4-4)

| Type | PN | Input | Output | Current(mA) | Enable pin |
|---|---|---|---|---|---|
| BUCK | RT6254B | 12 | 3.3 | 3350 | 12V |
| BUCK | RT6255B | 12 | 0.87 | 4100 | 12V |
| BUCK | RT6252B | 12 | 1.8 | 1650 | 12V |
| LDO | RT9078N-08(adj.) | 1.8 | 0.9 | 80 | 1.8V |
| LDO | RT9078-12GJ5/GQZ | 1.8 | 1.2 | 70 | 1.8V |
| LDO | RT9078-18GJ5/GQZ | 3.3 | 1.8 | 100 | 1.8V |
| LDO-DDR3 | RT9081 (500mA) | 1.8(3.3) | 1.5 | 350 | 1.8V |

**Table 4-2 : MT7981B+MT7976 power table**

### 4.1.5 MT7981B power on sequence

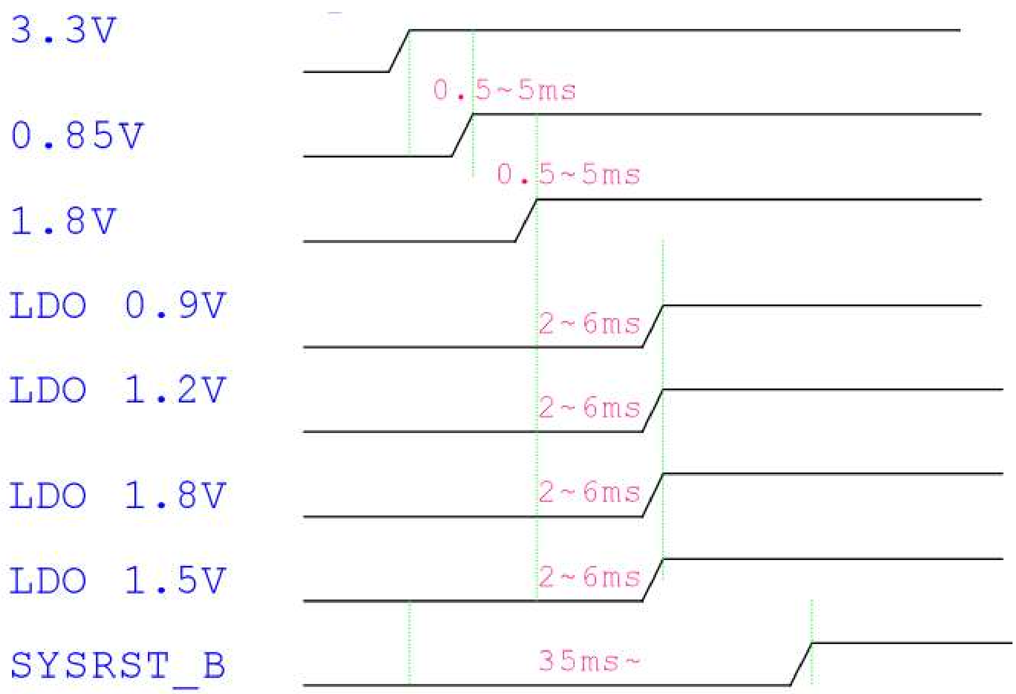



**Fig 4-8 : MT7981B power on sequence**

### 4.1.6 Reset

Fig 4-9 : Reset circuits.

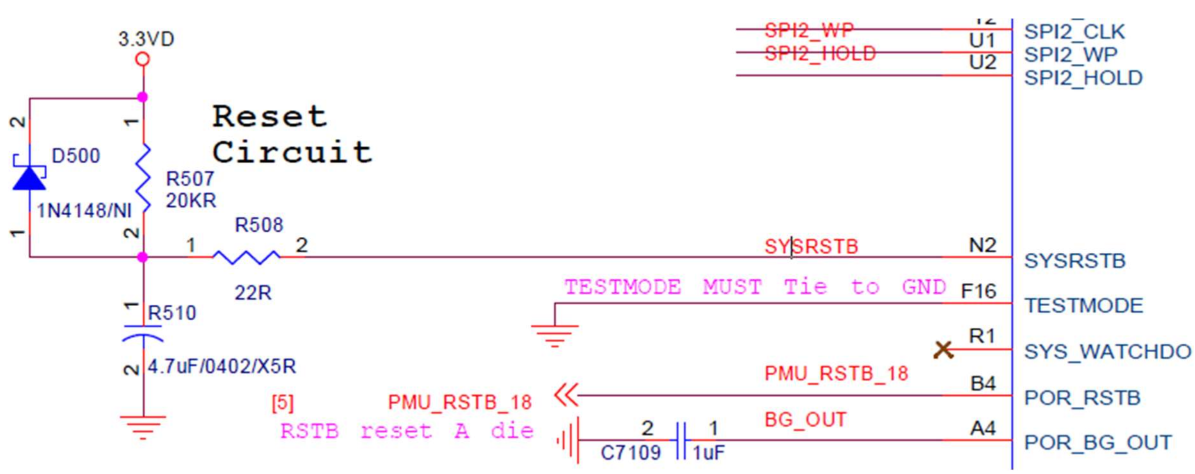



**Fig 4-9 : Reset circuit**

### 4.1.7 GPIO definition

| Pin Name | Aux Func.0 | Aux Func.1 | Aux Func.2 | Aux Func.3 |
|---|---|---|---|---|
| GPIO_WPS | B:GPIO0 | | | |
| GPIO_RESET | B:GPIO1 | | | |
| SYS_WATCHDOG | B:GPIO2 | O:SYS_WATCHDOG | | |
| JTAG_JTDO | B:GPIO4 | O:JTAG_JTDO | O:WM_JTAG_JTDO | I1:UART2_RXD |
| JTAG_JTDI | B:GPIO5 | I1:JTAG_JTDI | I1:WM_JTAG_JTDI | O:UART2_TXD |
| JTAG_JTMS | B:GPIO6 | B1:JTAG_JTMS | I1:WM_JTAG_JTMS | I1:UART2_CTS |
| JTAG_JTCLK | B:GPIO7 | I1:JTAG_JTCLK | I1:WM_JTAG_JTCLK | O:UART2_RTS |
| JTAG_JTRST_N | B:GPIO8 | I0:JTAG_JTRST_N | I0:WM_JTAG_JTRST_N | O:GBE_LED0 |
| WO_JTAG_JTDO | B:GPIO9 | O:WO0_JTAG_JTDO | | |
| WO_JTAG_JTDI | B:GPIO10 | I1:WO0_JTAG_JTDI | | |
| WO_JTAG_JTMS | B:GPIO11 | B1:WO0_JTAG_JTMS | | |
| WO_JTAG_JTCLK | B:GPIO12 | I1:WO0_JTAG_JTCLK | | |
| WO_JTAG_JTRST_N | B:GPIO13 | I0:WO0_JTAG_JTRST_N | O:PWM0 | O:GBE_LED1 |
| USB_VBUS | B:GPIO14 | O:DRV_VBUS | O:PWM1 | |
| PWM0 | B:GPIO15 | O:PWM0 | O:EMMC_RSTB | O:PWM1 |
| SPI0_CLK | B:GPIO16 | O:SPI0_CLK | B1:EMMC_DAT0 | O:SNFI_CLK |
| SPI0_MOSI | B:GPIO17 | B0:SPI0_MOSI | B1:EMMC_DAT1 | B0:SNFI_MOSI |
| SPI0_MISO | B:GPIO18 | B0:SPI0_MISO | B1:EMMC_DAT2 | B0:SNFI_MISO |
| SPI0_CS | B:GPIO19 | O:SPI0_CS | B1:EMMC_DAT3 | O:SNFI_CS |
| SPI0_HOLD | B:GPIO20 | B0:SPI0_HOLD | B1:EMMC_DAT4 | B0:SNFI_HOLD |
| SPI0_WP | B:GPIO21 | B0:SPI0_WP | B1:EMMC_DAT5 | B0:SNFI_WP |
| SPI1_CLK | B:GPIO22 | O:SPI1_CLK | B1:EMMC_DAT6 | I1:UART2_RXD |
| SPI1_MOSI | B:GPIO23 | O:SPI1_MOSI | B1:EMMC_DAT7 | O:UART2_TXD |
| SPI1_MISO | B:GPIO24 | I0:SPI1_MISO | B1:EMMC_CMD | I1:UART2_CTS |
| SPI1_CS | B:GPIO25 | O:SPI1_CS | B1:EMMC_CLK | O:UART2_RTS |
| SPI2_CLK | B:GPIO26 | O:SPI2_CLK | I1:UART1_RXD | |
| SPI2_MOSI | B:GPIO27 | B0:SPI2_MOSI | O:UART1_TXD | |
| SPI2_MISO | B:GPIO28 | B0:SPI2_MISO | I1:UART1_CTS | |
| SPI2_CS | B:GPIO29 | O:SPI2_CS | O:UART1_RTS | |
| SPI2_HOLD | B:GPIO30 | B0:SPI2_HOLD | O:WF2G_LED | |
| SPI2_WP | B:GPIO31 | B0:SPI2_WP | O:WF5G_LED | |
| UART0_RXD | B:GPIO32 | I1:UART0_RXD | | |
| UART0_TXD | B:GPIO33 | O:UART0_TXD | | |
| WF2G_LED | B:GPIO34 | O:WF2G_LED | B1:PCIE_CLK_REQ | |
| WF5G_LED | B:GPIO35 | O:WF5G_LED | I1:PCIE_WAKE_N | |
| SMI_MDC | B:GPIO36 | O:SMI_MDC | B1:I2C_SCL | I1:GBE_EXT_MDC |
| SMI_MDIO | B:GPIO37 | B0:SMI_MDIO | B1:I2C_SDA | B1:GBE_EXT_MDIO |
| GBE_INT | B:GPIO38 | I0:MT7531_INT | | |
| GBE_RESET | B:GPIO39 | | | |

**Table 4-3 : MT7981B GPIO definition**

#### 4.1.8 Strapping option

MT7981B can option to boot from SPIM_NOR/SPIM_NAND/eMMC/SNFI-NAND.
The difference of SPI-NAND and SNFI-NAND is ECC Free.

01 SPIM w/ an external on-die ECC flash (ECC Free)
11 SNFI w/ an external no on-die ECC flash

| PAD Name | CR Address | GPIO Number | |
|---|---|---|---|
| USB_VBUS | | GPIO14 | {PWM0, USB_VBUS}<br>00 : SPIM-NOR<br>01 : SPIM-NAND -->SD<br>10 : EMMC<br>11 : SNAND(SNFI)-->SD |
| PWM0 | | GPIO15 | |
| SPI2_CLK | | GPIO26 | 1 : 40Mhz (A Die Xtal) |

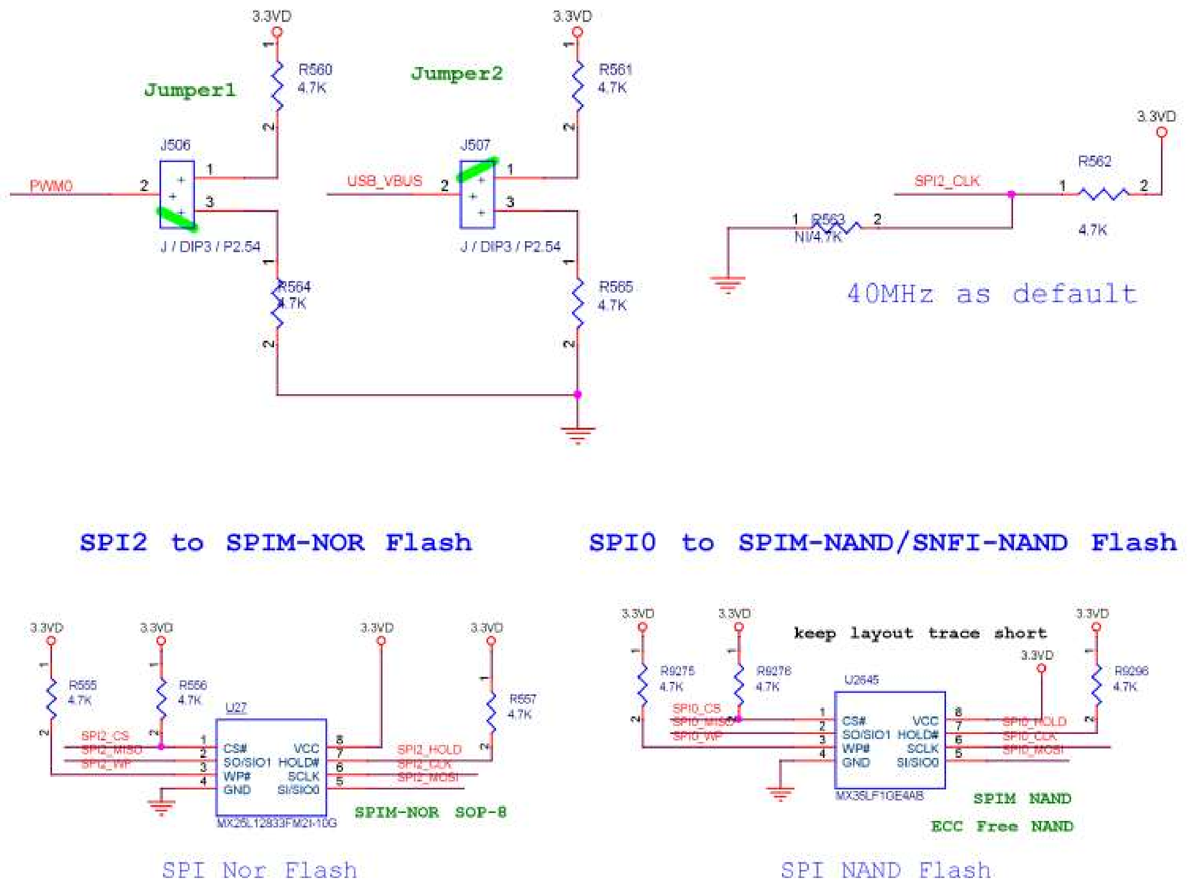



**Fig 4-10 : MT7981B strapping option**

#### 4.1.9 JTAG

GPIO_4~13 share w/ JTAG mode, GPIO4~8 internal pull up, the schematic change these signal pull up to prevent current leakage.

| Pin Name | Aux Func.0 | Aux Func.1 |
|---|---|---|
| JTAG_JTDO | B:GPIO4 | O:JTAG_JTDO |
| JTAG_JTDI | B:GPIO5 | I1:JTAG_JTDI |
| JTAG_JTMS | B:GPIO6 | B1:JTAG_JTMS |
| JTAG_JTCLK | B:GPIO7 | I1:JTAG_JTCLK |
| JTAG_JTRST_N | B:GPIO8 | I0:JTAG_JTRST_N |
| WO_JTAG_JTDO | B:GPIO9 | O:WO0_JTAG_JTDO |
| WO_JTAG_JTDI | B:GPIO10 | I1:WO0_JTAG_JTDI |
| WO_JTAG_JTMS | B:GPIO11 | B1:WO0_JTAG_JTMS |
| WO_JTAG_JTCLK | B:GPIO12 | I1:WO0_JTAG_JTCLK |
| WO_JTAG_JTRST_N | B:GPIO13 | I0:WO0_JTAG_JTRST_N |

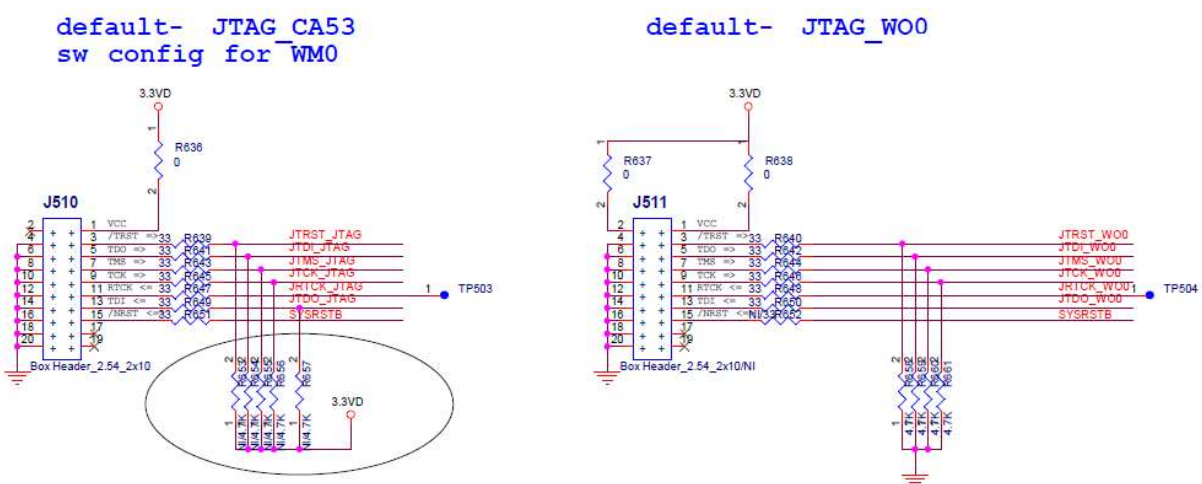



Fig 4-11 : MT7981B JTAG

### 4.1.10 TSAUX

TSAUS block is design for thermal sensor. TSAUX_MD pin should be supplied by 1.8V. MT7976 has an internal thermal sensor too. Keep AUXIN0/1/2 floating or tie to GND in case the pin is not used. SAUX_REFP is sensitive and please keep away from any noise.

< 85 degree C, the thermal tolerance around 5%, > 85 degree C, the tolerance around 7~8%.

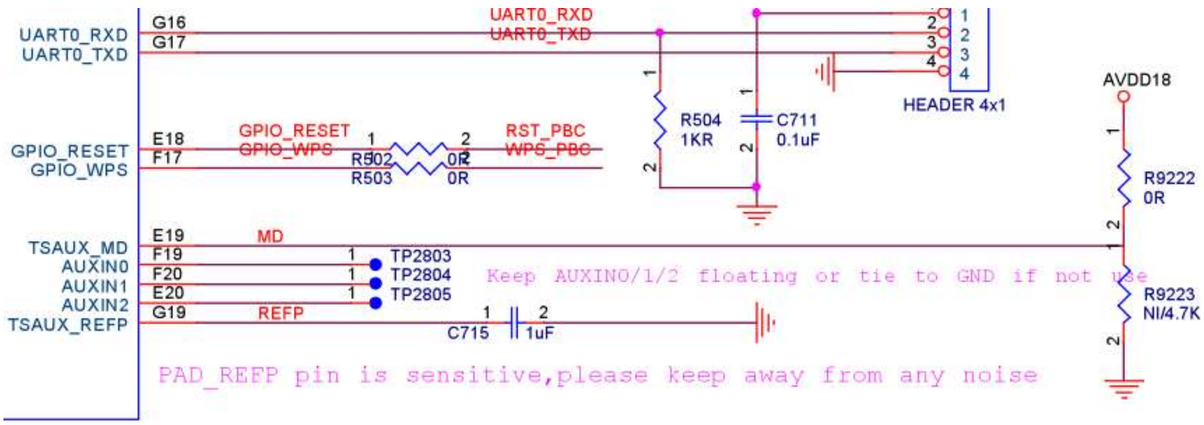



**Fig 4-12 : TXAUS for thermal sensor**

### 4.1.11 PLL

PLLGP_TP and PLLGP_TN are internal debug pins, please keep floating.

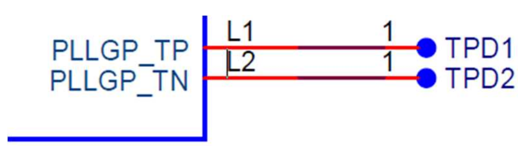



**Fig 4-13 : PLLGP_TP/TN (internal debug pins)**

### 4.1.12 CKSQ

Connect AVDD18_CKSQ to AVDD18 with 1uF+0.1uF cap, and AVDD12_CKSQ connect to AVDD12 with 1uF+0.1uF cap.

### 4.1.13 AFE Control Signal

The control signal of TOP_CLK/HB0/HB0_B are clock signal; One RC circuit for TOP_CLK signal and two RC circuits for HB0 & HB0_B should be reserved to prevent WIFI RX desense.
And 4.7pF are recommended for the caps that are closed to MT7981.

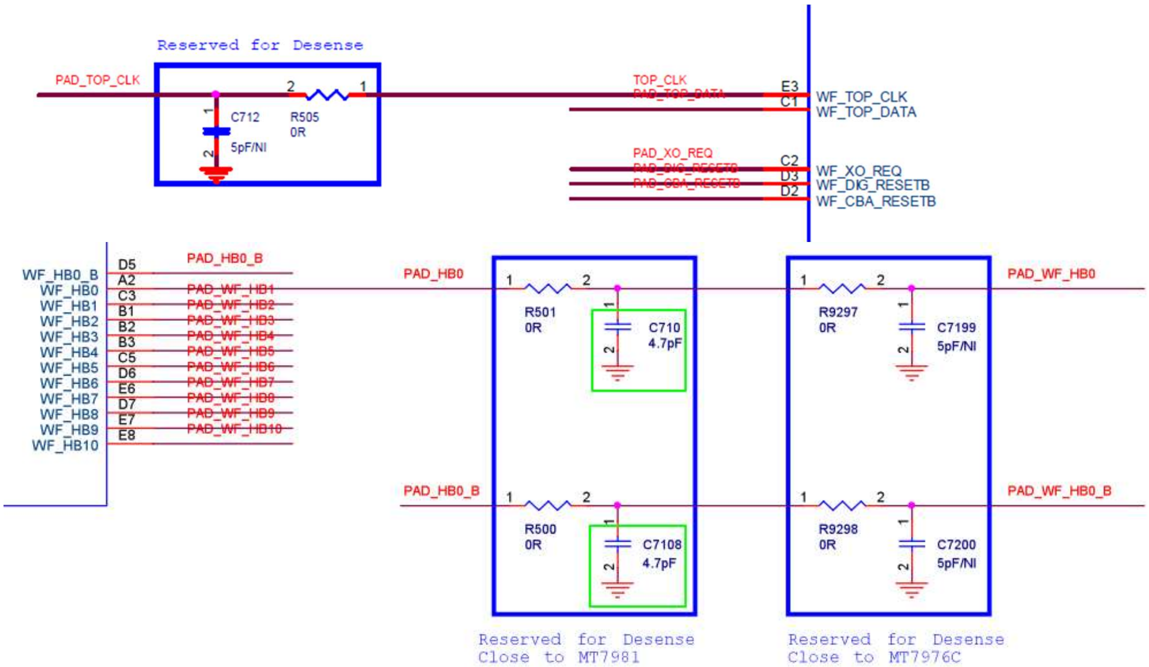



**Fig 4-14 : TOP_CLK/HB0/HB0_B signal design**

### 4.1.14 AFE power Cap

1uF+0.1uF should be placed close to AVDD12_WGB/AVDD18_WGB pins.

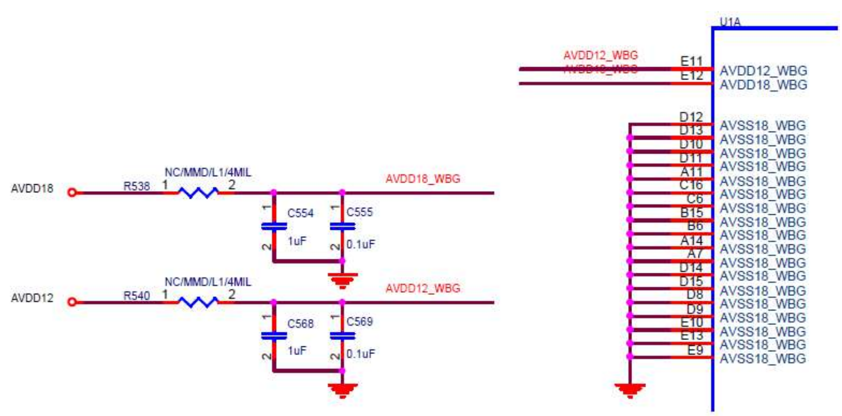



**Fig 4-15 : AFE power Cap**

#### 4.1.15 AFE AIQ design guideline

1. WF2/3/4 IQ Pairs w/solid GND plane and via
2. Trace width 4/4/4mil
3. AIQ Length <35mm
4. Caps close to MT7976
5. 0.6pF on WF4 QP/QN pair only, other IQ pairs with caps but NI.

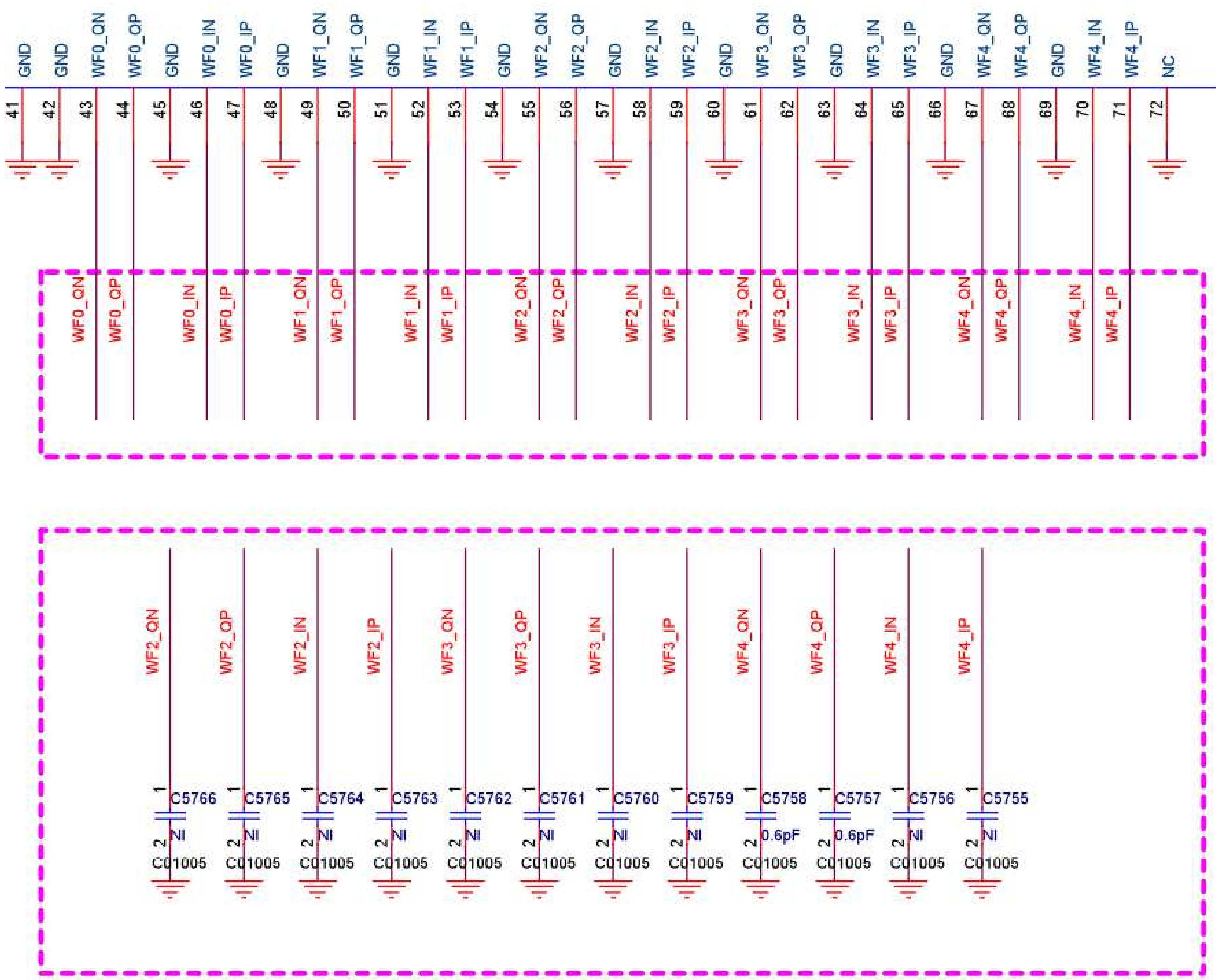



**Fig 4-16 : AIQ design guideline**

#### 4.1.16 WIFI RX desense by SGMII interference design notice

A 0805/0R resistor is recommended to be reserved on 1.8VD power trace.
A 0603/0R resistor is recommended to be reserved on 0.9VD power trace.

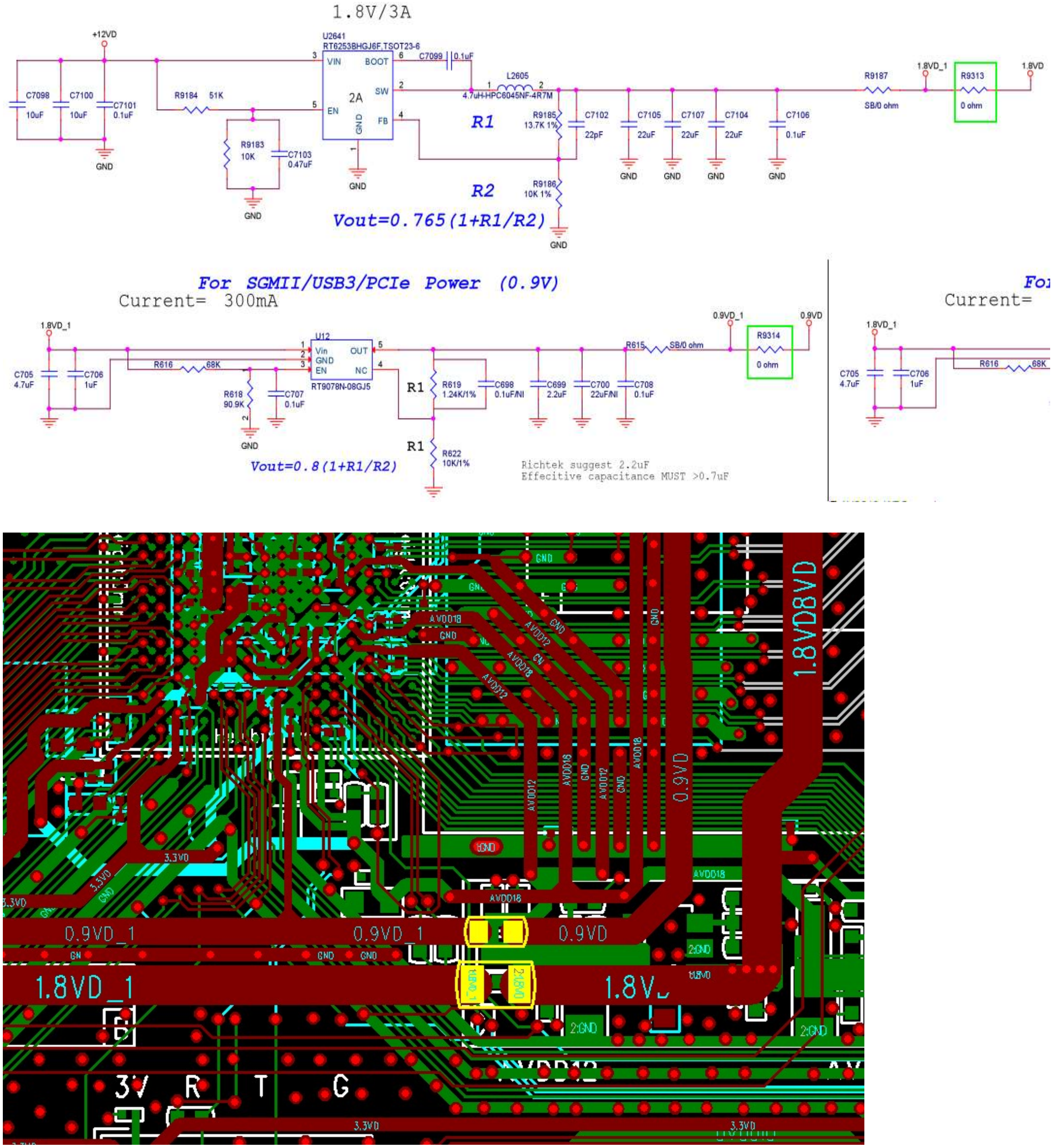



**Fig 4-17 : Solution for WIFI RX desense by SGMII interference**

#### 4.1.17 VQPS

VQPS for internal eFuse voltage supply, default tie to GND.

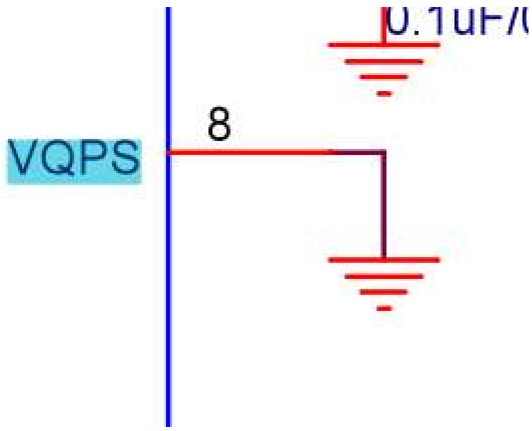



**Fig 4-18 : VQPS pin should be connected to GND**

## 4.2 PCB Layout

### 4.2.1 4L PCB stack-up

| PCB Stack up | | | | | | | Impedance (mil) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Layer | Type | | Thickness (mil) | | | DK | Single end +/-10% | | | | Diff end +/-10% | | | |
| Top Side Solder Mask | | | | 0.80 | mil | | 線寬(mil) | 參考層 | ohm值 | 理論值 | 線寬(mil) | 參考層 | ohm值 | 理論值 |
| L1 | TOP | Differential & Signal | pper+Plati | 1.40 | mil | | 7.5(7.5) | L2 | 50 | 49.71 | 6/4.5(5) | L2 | 85 | 85.70 |
| | | | | | | | | | | | 5/4.5(4.5) | L2 | 90 | 90.59 |
| | | | | | | | | | | | 4.5/5.5(5) | L2 | 100 | 99.57 |
| | | | Prepreg | 4.85 | mil | 3.98 | | | | | | | | |
| L2 | | | Copper | 1.25 | mil | | 6(7) | L1 | 50 | 49.55 | | | | |
| | | | Core | 44.50 | mil | 4 | | | | | | | | |
| L3 | | | Copper | 1.25 | mil | | 6(7) | L4 | 50 | 49.55 | 5/6(8) | | 90 | 89.32 |
| | | | Prepreg | 4.85 | mil | 3.98 | | | | | | | | |
| L4 | BOT | Differential & Signal | pper+Plati | 1.40 | mil | | 7.5(7.5) | L3 | 50 | 49.71 | 6/4.5(5) | L3 | 85 | 85.70 |
| | | | | | | | | | | | 5/4.5(4.5) | L3 | 90 | 90.59 |
| | | | | | | | | | | | 4.5/5.5(5) | L3 | 100 | 99.57 |
| Bottom Side Solder Mask | | | | 0.80 | mil | | | | | | | | | |
| Total | | | | 61.10 | mil | | | | | | | | | |
| | | | | 1.55 | mm | | | | | | | | | |

**Table 4-4 : 4L PCB stack-up**

### 4.2.2 MT7981B RFB

For power on calibration, the antennas or 50 ohm loadings of the WiFi ports should be connected in advance before the system power turned-on.

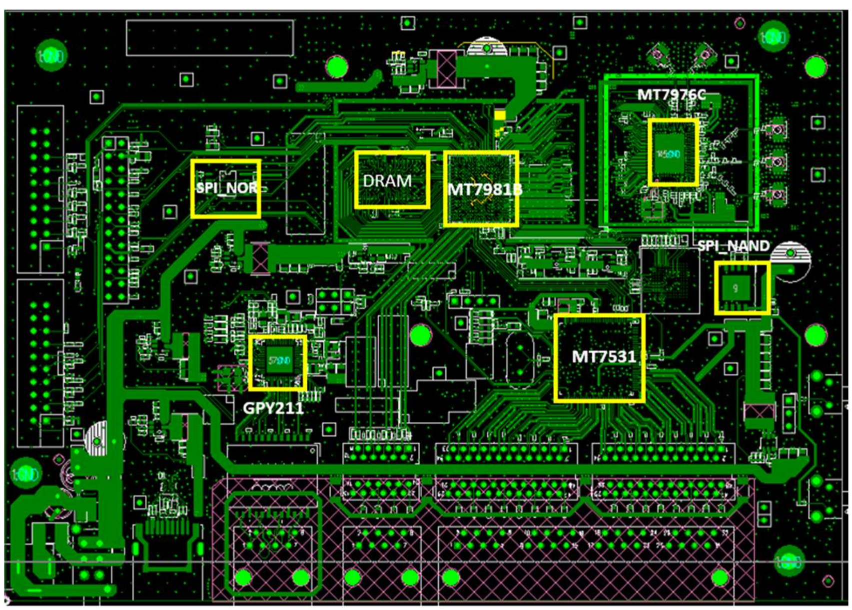
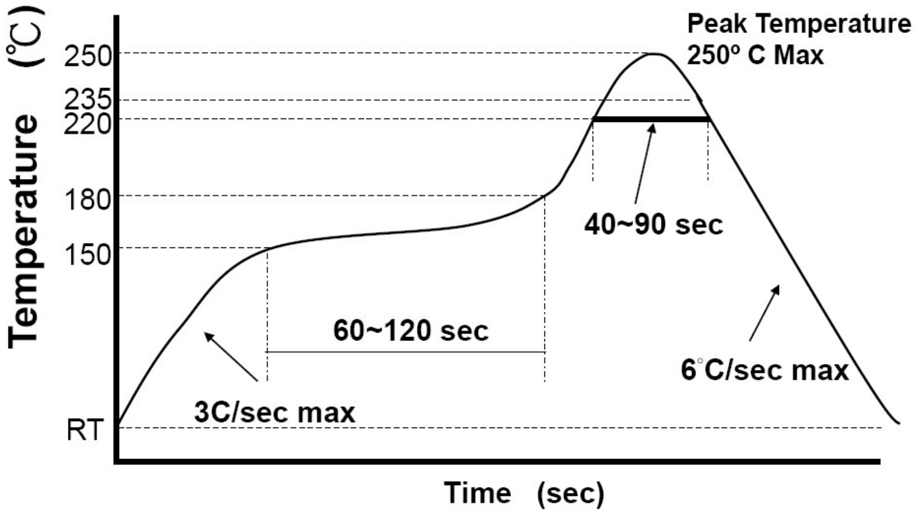



**Fig 4-19 : MT7981B RFB Top view**

### 4.2.3 MT7981B reflow profile



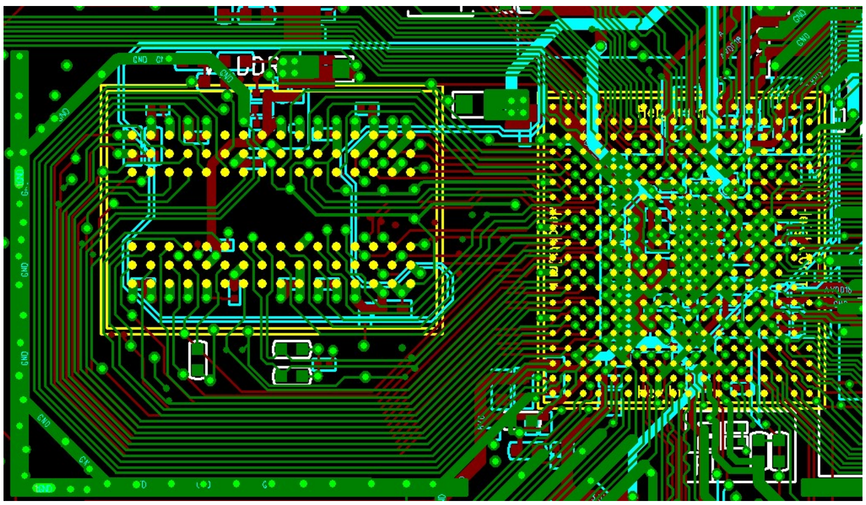

*Notes;*

1. *Reflow profile guideline is designed for SnAgCu lead-free solder paste.*
2. *Reflow temperature is defined at the the lead of package.*
3. *MTK would recommend customer following the solder paste vendor's guideline to design a profile appropriate your line and products.*
4. *Appropriate $N_2$ atmosphere is recommended since it would widen the process window and mitigate the risk for having solder open issues.*

**Fig 4-20 : MT7981B reflow profile**

### 4.2.4 DDR PCB guidelines

- DDR signals group :
  - Clock group : MCLK P/N( ≤ 20mm,Skew ≤ 0.5mm)
  - Data groups : DQS P/N. (length ≤ 17mm , Skew ≤ 0.5mm,)
  - Data groups : DQM, DQ, DQS (length ≤ 17mm , DQvsDQSvsDQM Skew ≤ 7mm)
  - Address, Command and Control group : Address ( includes BA ), Command ( /RAS, /CAS, /WE ), Control ( /CS, CKE, ODT ). (length ≤ 55mm , Skew ≤ 35mm)
  - Power groups : DVDD08, VDDIO, VREF.
- Routing order:
  - 1) Data, VREF, 2) Address/Command, 3) Control, 4) Clocks, and 5) Power
  - Referenced to the solid ground plane.
  - Layer transition should accompany GND via.
- Routing constraint:



All the signal routing and caps location, please MUST follow HDK layout

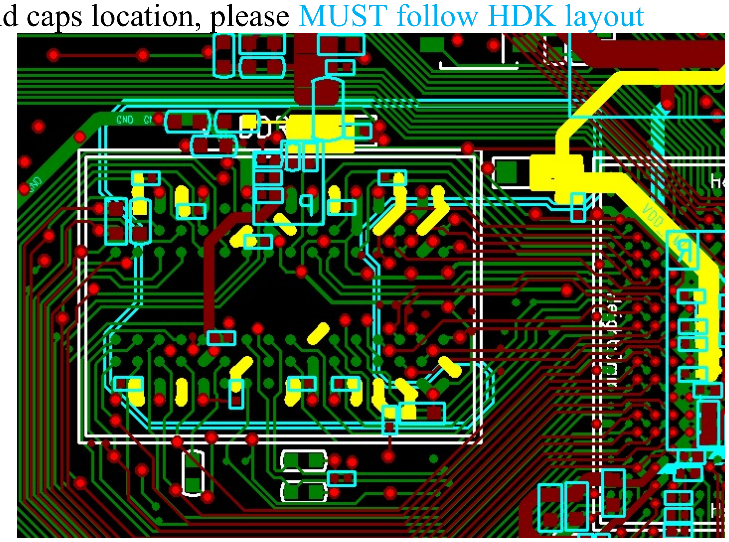
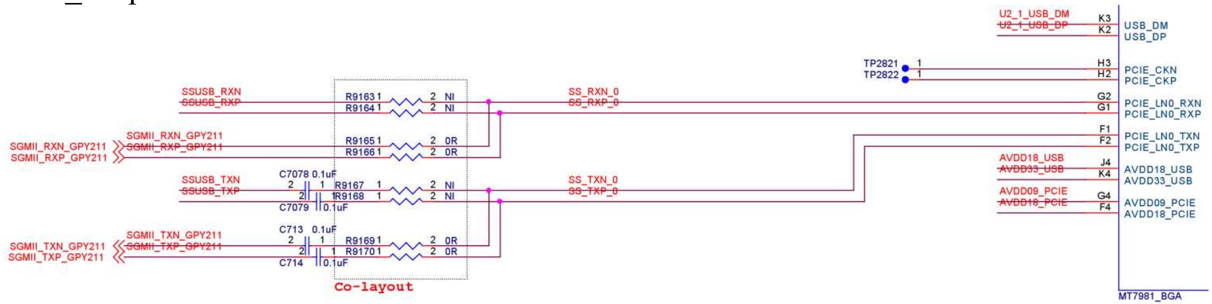


**Fig 4-21 : DDR SOC and DRAM Power Cap placement**

#### 4.2.5 USB2/3

- Keep USB2_DP/DM and USB3 pairs (SSUSB_TX/SSUSB_RX) differential pairs routing with well "GND shielding".
- Impedance is **90-ohm ± 10% (differential)**
- USB2.0 PCB routing **P/N skew <50mils**
- USB3.0 On board **Trace <6000mils** (base on PCBA & eye diagram margin).
- USB3.0 PCB routing **P/N skew < 5mils** for total length from IC to Connector.
- USB_5V power trace >=20mil



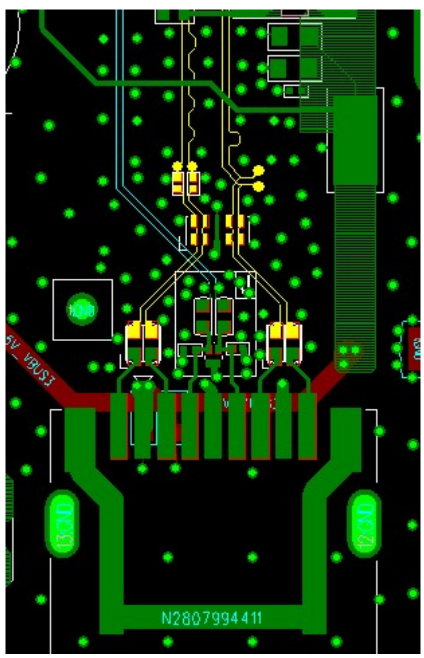
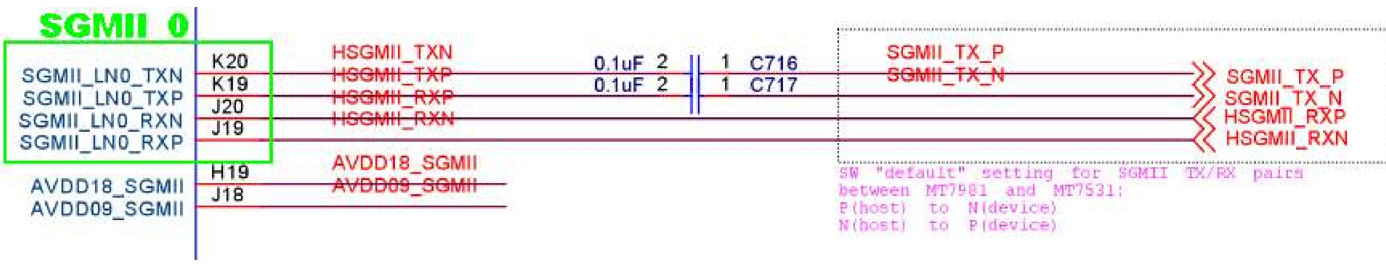


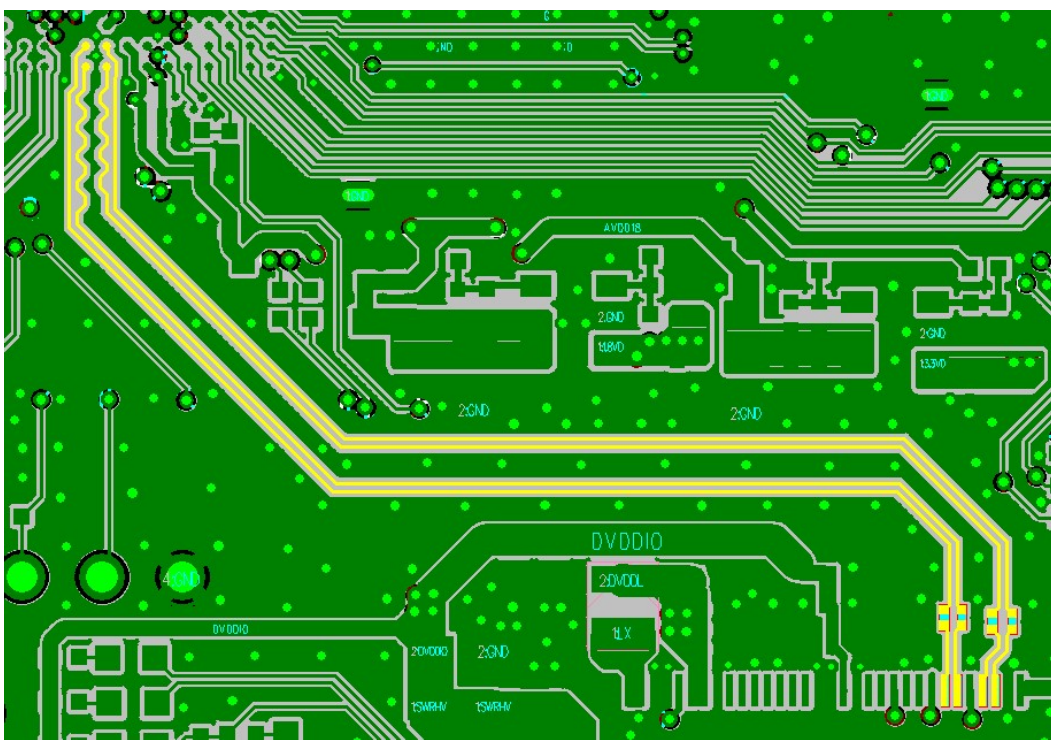
**Fig 4-22 : USB3.0/USB2.0 layout notice**

### 4.2.6 HSGMII layout noitce

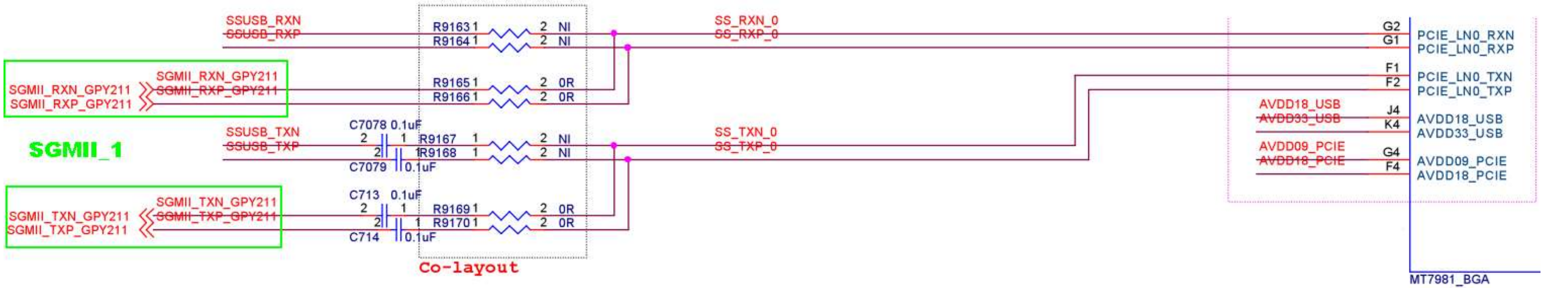
- Separate each HSGMII pairs (SGMII_TX / SGMII_RX) with "well GND shielding"
- SGMII_0 Impedance is **100-ohm ± 10% (differential)**
- SGMII_1 Impedance is **90-ohm ± 10% (differential)**(shared pin with USB3)
- SGMII On board **Trace<6000mils** (base on PCBA & eye diagram margin).
- SGMII PCB routing **P/N skew < 5mil** for total length from IC to Connector.
- SGMII_0 TX/RX pairs P/N need to swap between MT7981 and MT7531
  P(host) to N (device)
  N(host) to P (device)
- SGMII_1 TX/RX pairs P/N doesn't need to swap between MT7981 and MT7531

**[SGMII_0 SCH/PCB design]**



**[SGMII_1 SCH/PCB design]**



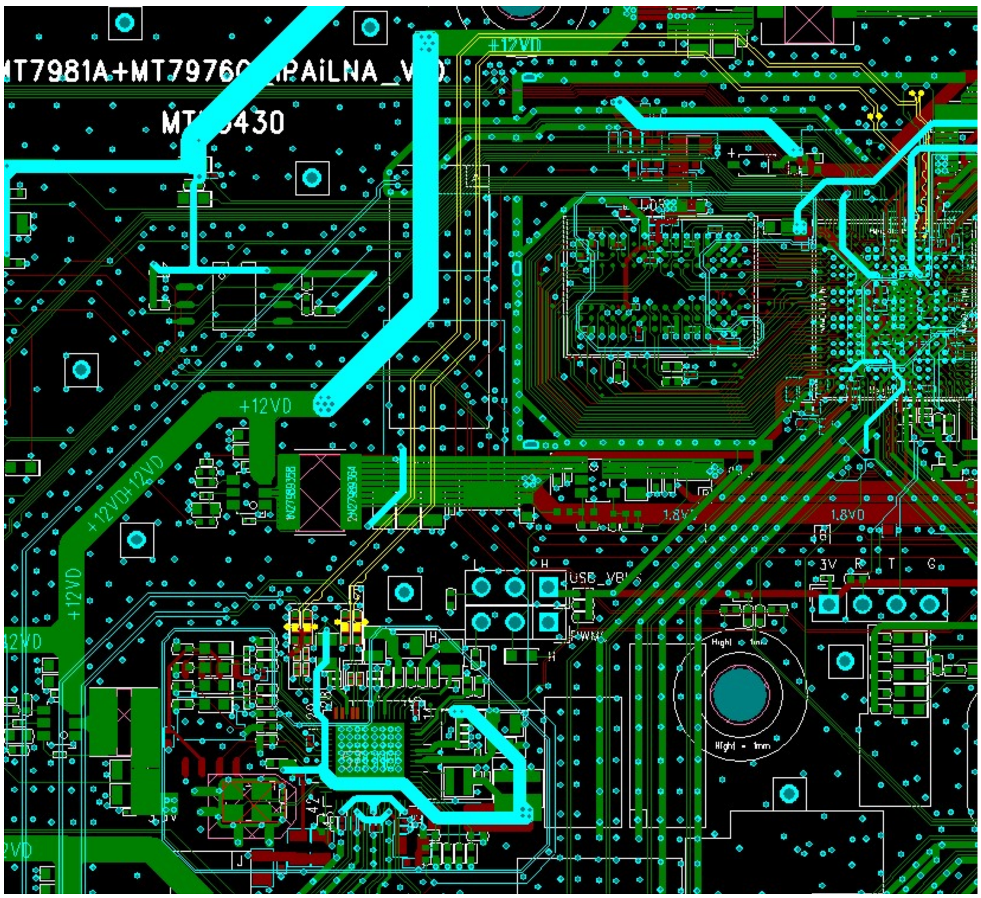




**Fig 4-23 : MT7981 HSGMII layout guideline**

#### 4.2.7 Ethernet 10/100/1Gbps TX

- The Tx+/Tx- and Rx+/Rx- traces should always be as short as possible
- The individual trace impedance of Tx+/Tx- and Rx+/Rx- must be kept the differential characteristic impedance of the pair **must be 100 ohm.**
- Avoid placing noisy digital signal traces near these sensitive pins.
- Internal GPHY **Trace<2500mils (highlight)**

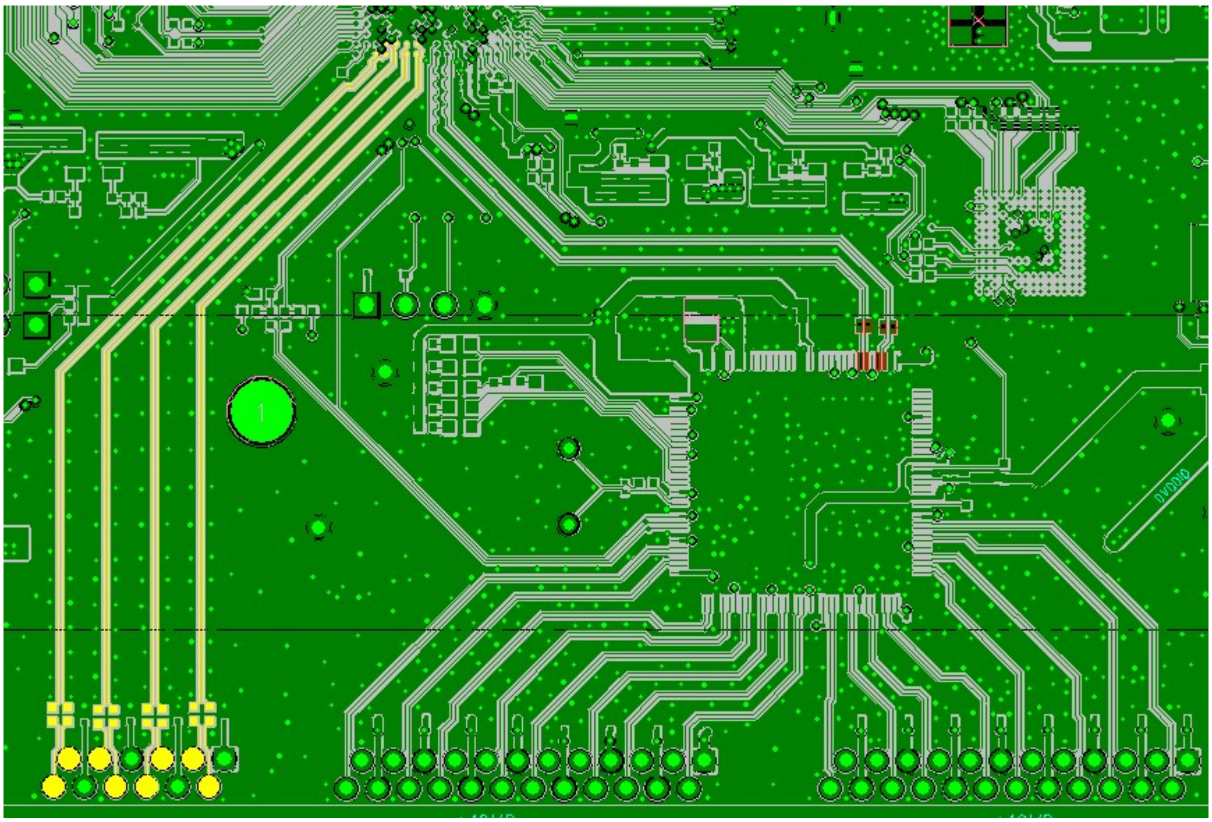


**Fig 4-24 : The shielding line example of Ethernet layout**

### 4.2.8 Buck/LDO design

Most of the power domain of MT7981B are routing by power trace.
VCCK and VDD_EMI (DDR power) are routing by power plane.

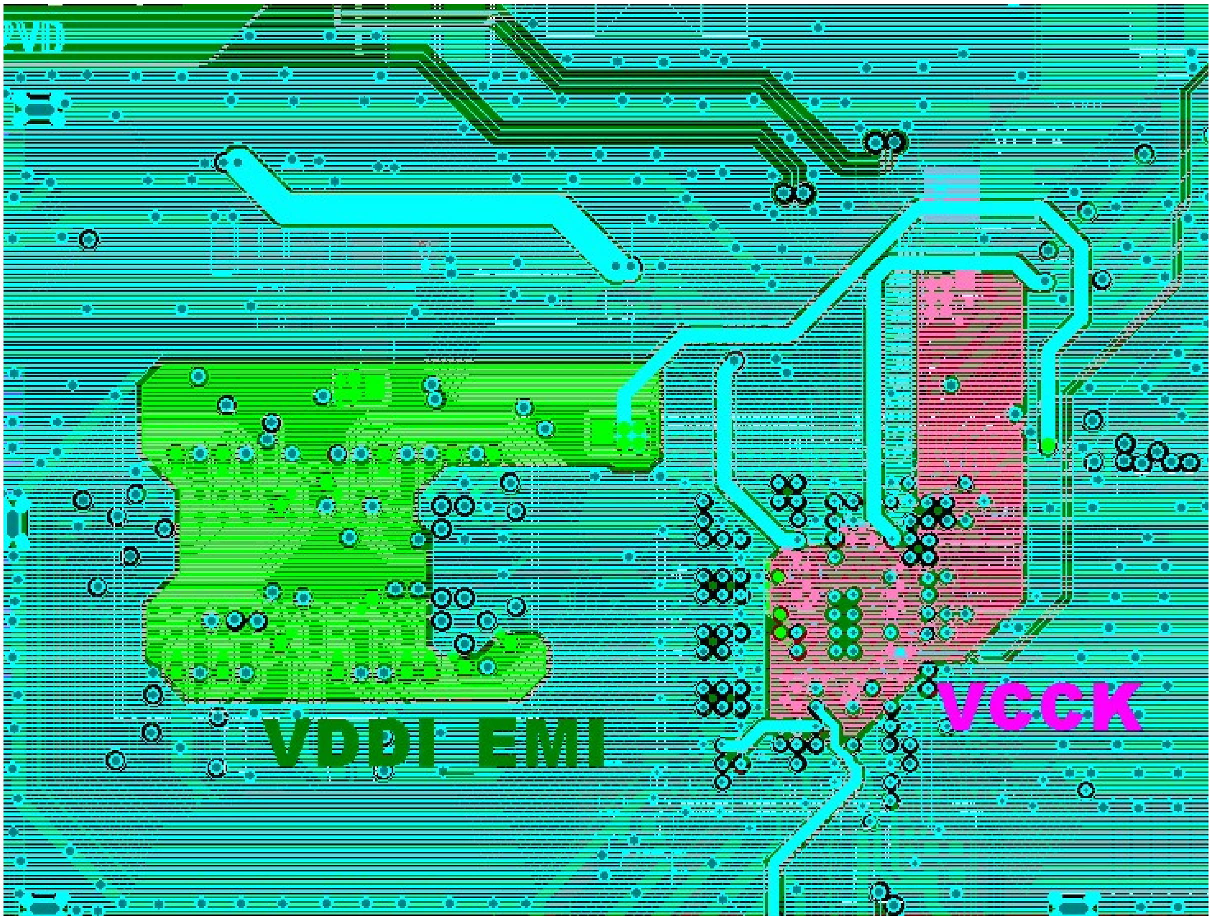
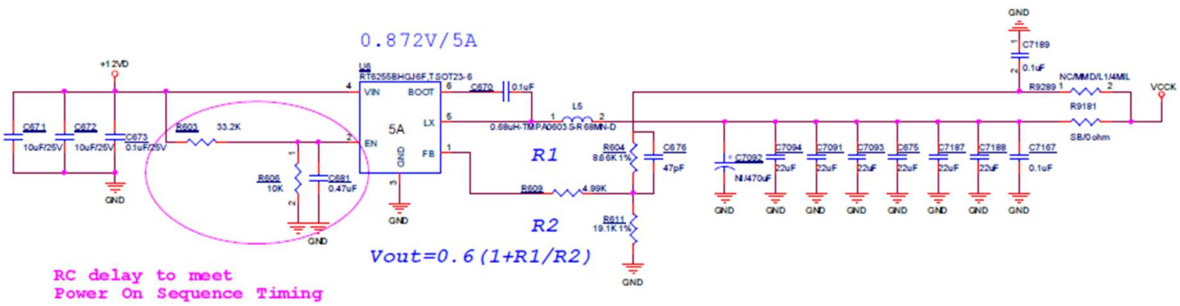



**Fig 4-25 : The power deign of MT7981B.**

#### 4.2.8.1.1 VCCK voltage feedback pin design rule

- Short bar R9289 pads must be placed **very closely to MT7981B DVDD_CORE power ball and the traces must be well grounded**
- 
- The VCCK CORE(0.87V) max power current is 4.1A, the power plant must be well and shorten the distance between regulator and MT7981B to prevent voltage drop.
- The DVDD_CORE(0.87V) feedback  signal Must leave noise signal far away, LX is noise source



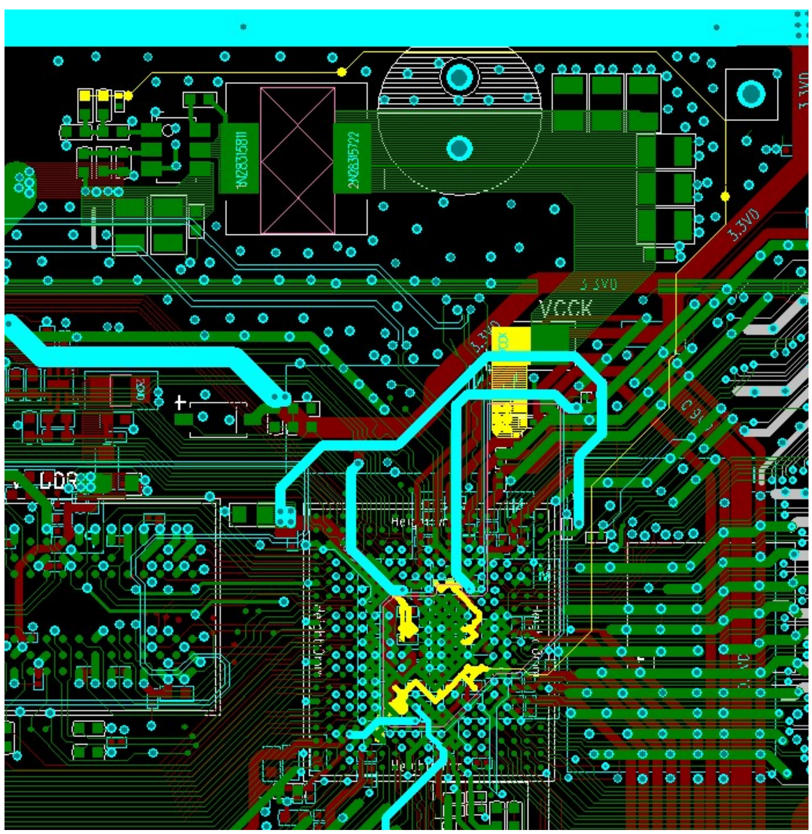
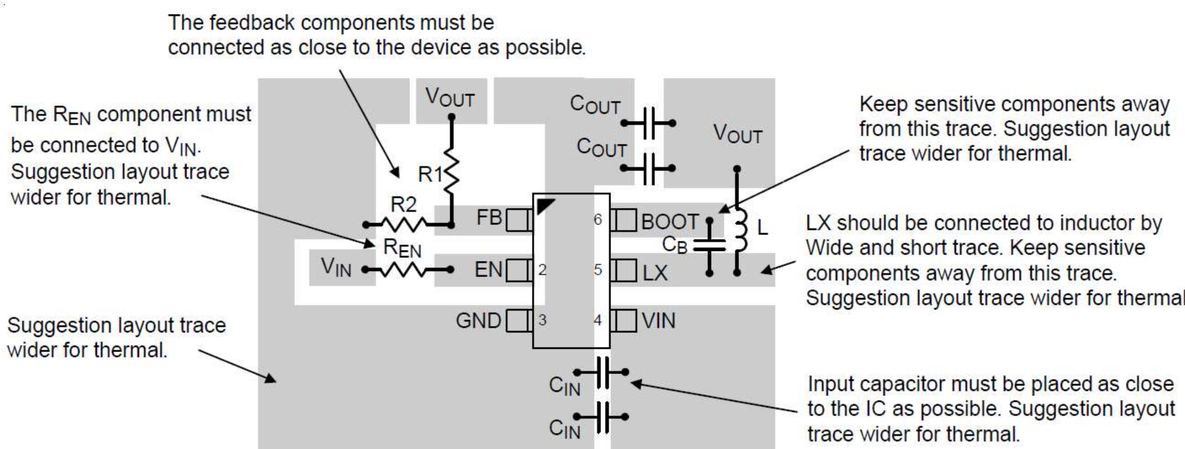



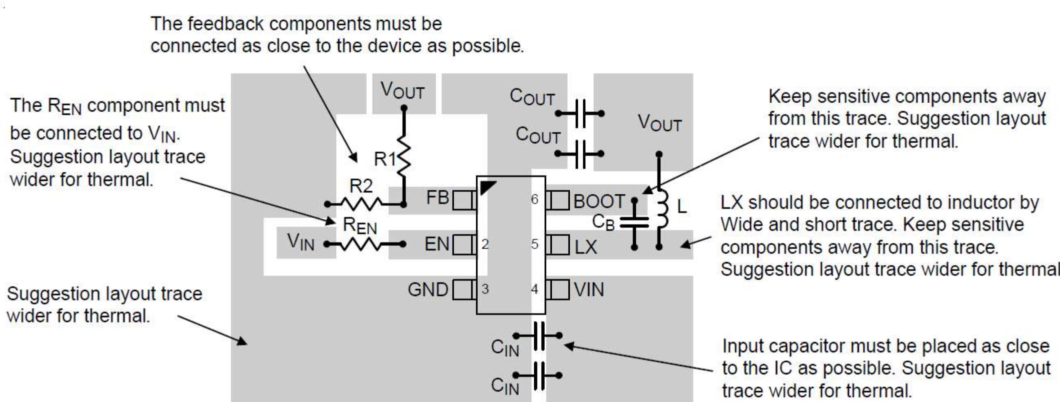

**Fig 4-26 : The VCCK CORE Feedback pin layout guidelines.**

#### 4.2.8.1.2 Buck/LDOs layout guideline summary

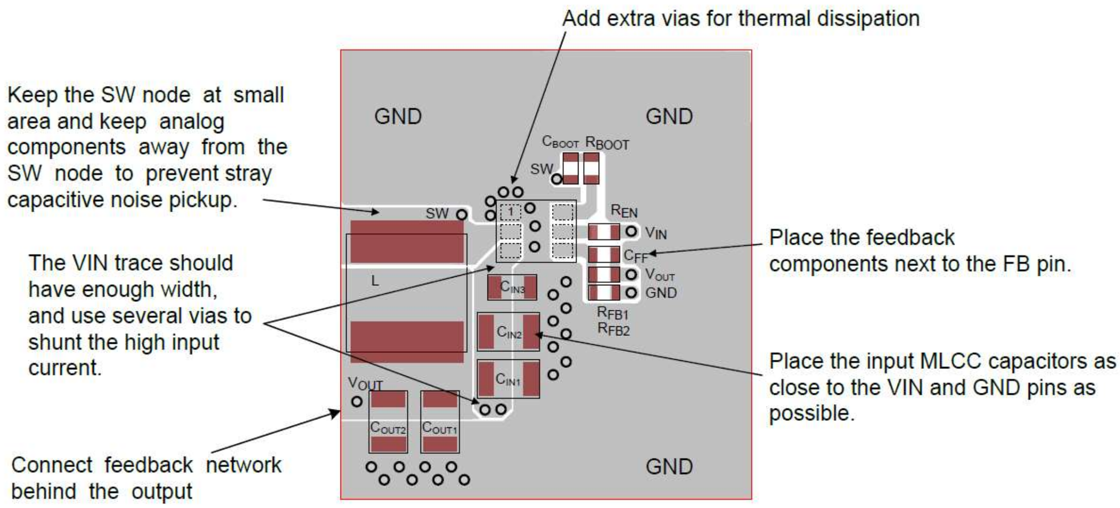
RT6255BHGJ6F (0.872V)



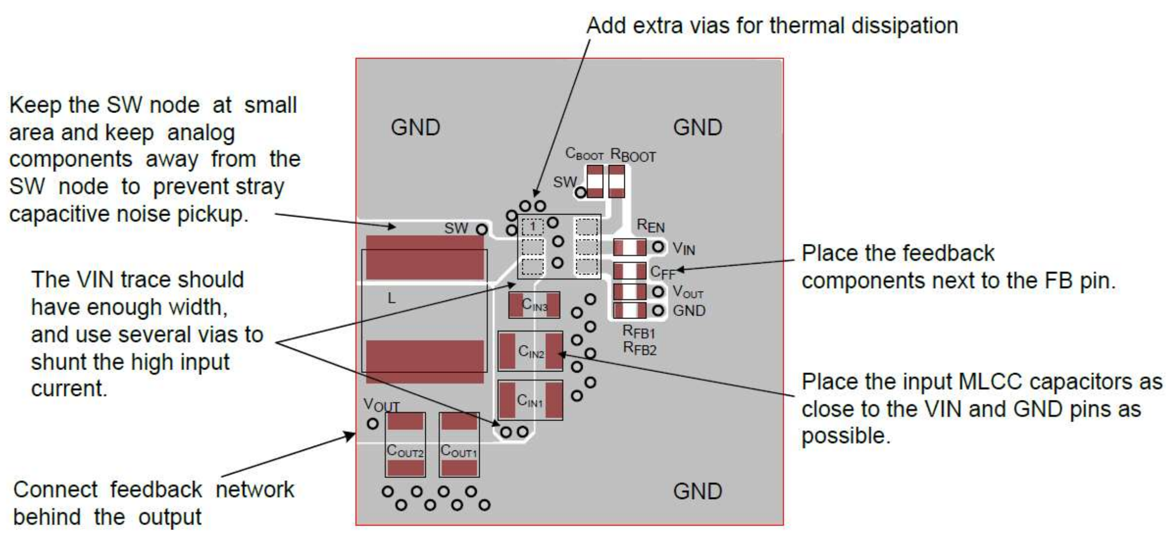

RT6254BHGJ6F(3.3V)



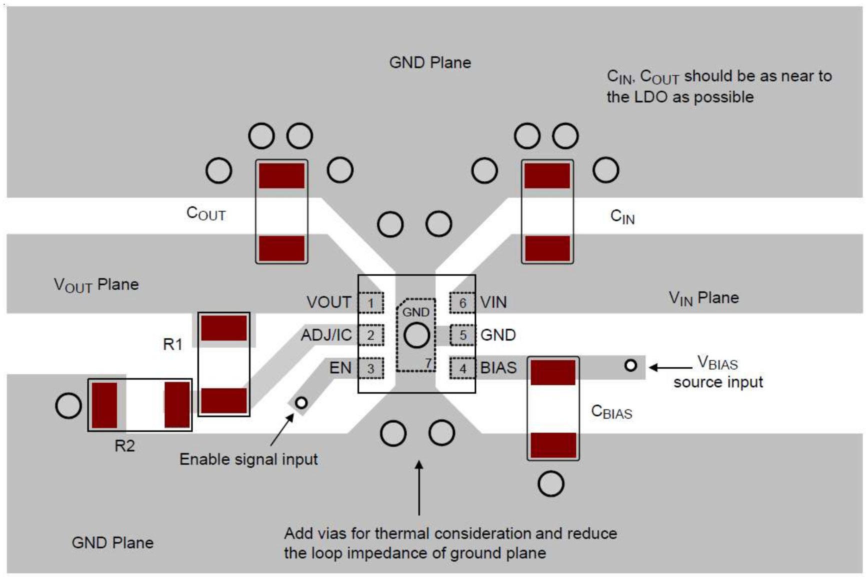
RT6253BHGJ6F(1.8V)




RT6252BHGJ6F(5V)



RT9081AGQZA(1.5V)
RT9078AGQZA(0.9/1.2/1.8V LDO)



#### 4.2.9 WiFi iPAiLNA

For iPAiLNA, from WF0 to WF4, each port's chip out to I-pex trace length should be kept the same and the impedance is designed as 50 ohm to obtain the same RF performance at each I-pex port. For RF and Xtal traces, the GND shielding vias along the RF traces are suggested/required. 錯誤! 找不到參照來源。 lists the RF matching values and its component part numbers. The different value at different RF streams are highlighted in blue color. The Tx/Rx RF performance may need to be checked/tuned again if the component vendor is changed.

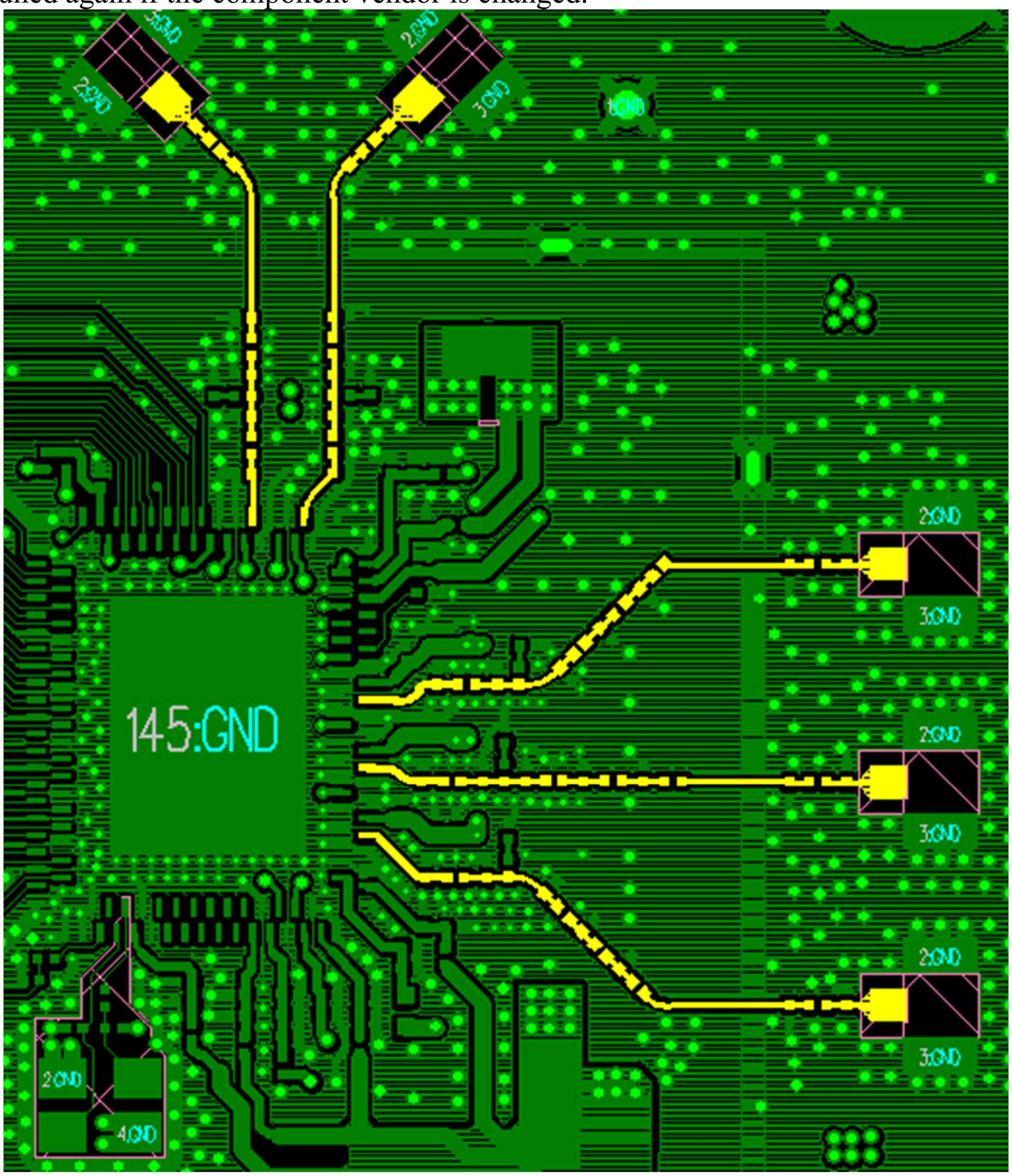
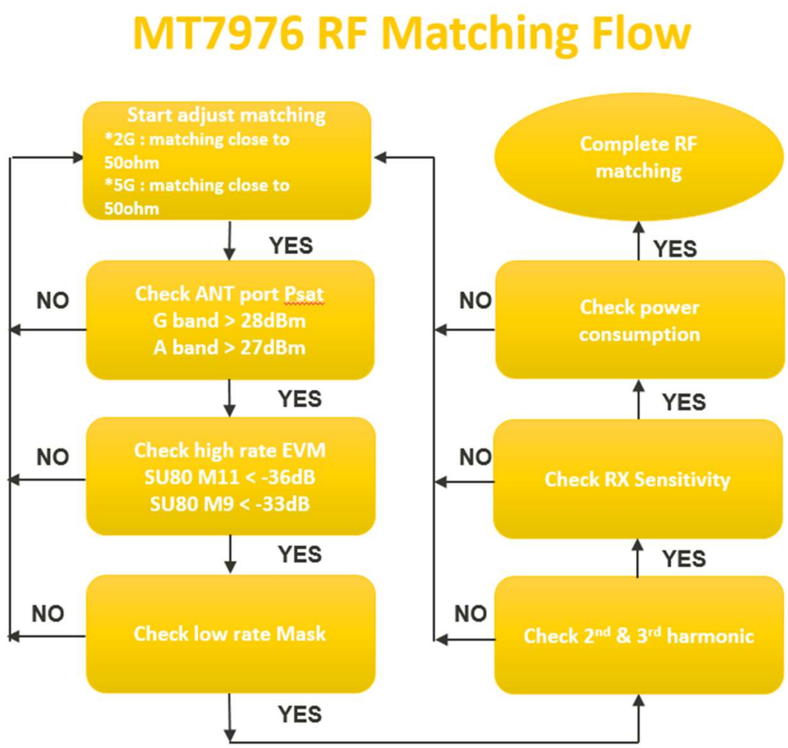



**Fig 4-27 : MT7976 RF trace layout guideline**




**How to Get Psat**

Observing peak power index in WLAN tester UI as below picture. Increasing wanted power until peak power saturates. This point is Psat. MT7976 Psat specification should be around G band 28.5~29dBm, A band 27.5~28dBm at IC chip out.

| Measurement | Value | Unit |
|---|---|---|
| By Analyzed Signal: | | |
| Power | 22.23 | dBm |
| Peak Power | 27.61 | dBm |
| Phase Error | 0.92 | deg |
| Frequency Error | -32.42 | kHz |
| Symbol Clock Error | -12.00 | ppm |
| LO Leakage | -35.38 | dB |
| Amplitude Imbalance | 0.03 | dB |
| Phase Imbalance | -0.09 | deg |
| By Stream: | | |
| EVM | -21.95 | dB |
| EVM (%) | 7.99 | % |
| EVM Data | -21.92 | dB |
| EVM Pilot | -22.27 | dB |

Other Info:

| | |
|---|---|
| 802.11a/g | Packet Type |
| Non-HT | Packet Format |
| 20 | Channel BW (MHz) |
| 1 | Analyzed Signals |
| 1 | Spatial Streams |
| 1 | Space-Time Streams |
| 39 | Symbols 64 Tones |
| Long | Guard Interval |
| 7 | Mod. & Coding Scheme |
| BCC | Coding Type |
| 3/4 | Coding Rate |
| 54.0 | Data Rate (Mbps) |
| 64-QAM | Modulation Type |
| 1028 | PSDU Length (Bytes) |
| Passed | PSDU CRC |
| -- | VHT-SIG-A CRC |
| -- | VHT-SIG-B CRC |
| Passed | L-SIG Parity Check |
| 10 | L-STF Periods Detected |

**Fig 4-28 : iPA/iLNA RF matching**

#### 4.2.10 AIQ trace length control (don't need to impedance control)

2.4G/5G AIQ trace length should be control under 3.5cm. For AIQ and Xtal traces, the GND shielding vias along the AIQ traces are suggested/required, for AIQ GND plant should be keep 4 mil(4-4-4-4-4). A band: the capacitors on AIQ trace for BW160 requirement.

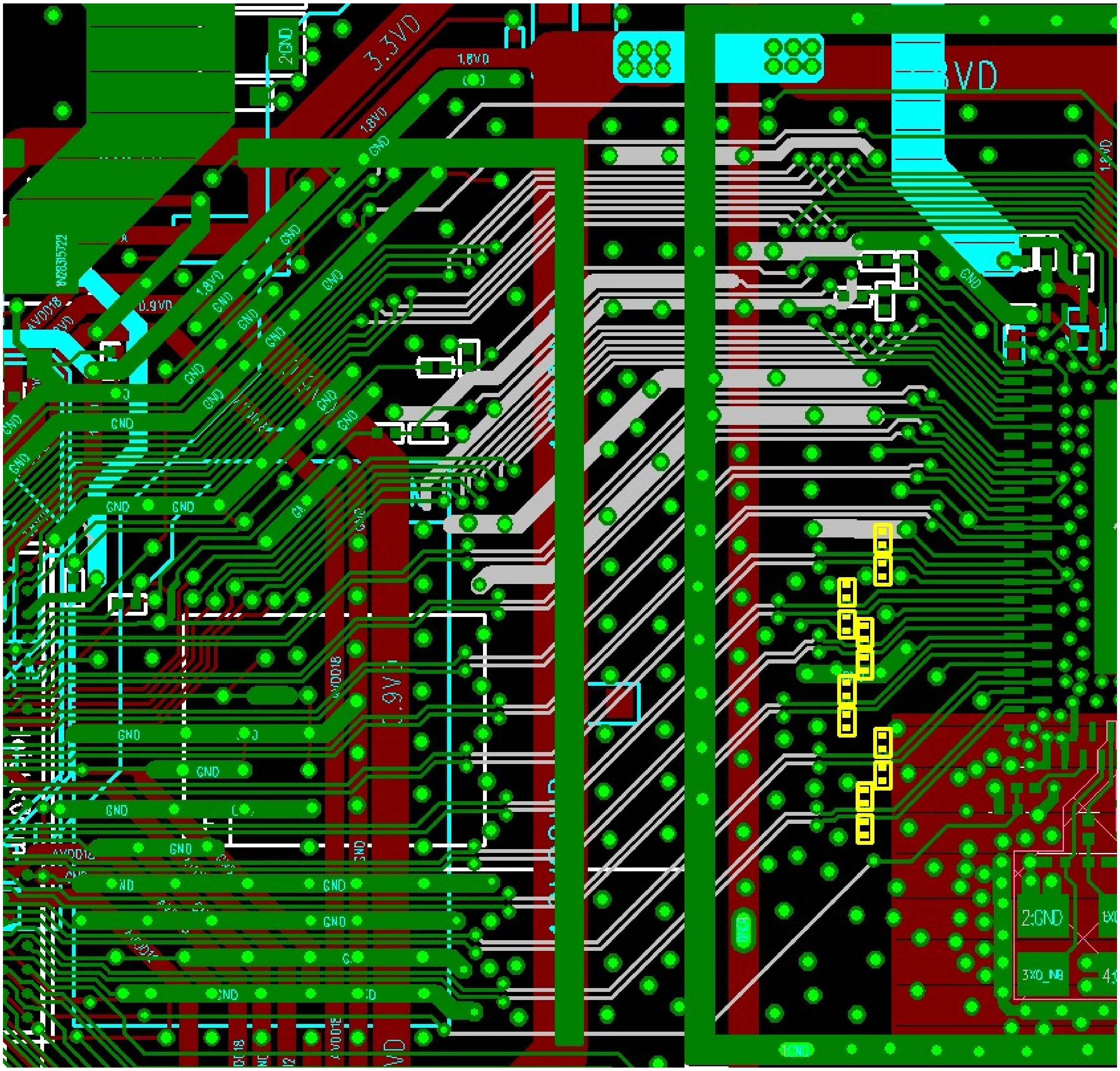
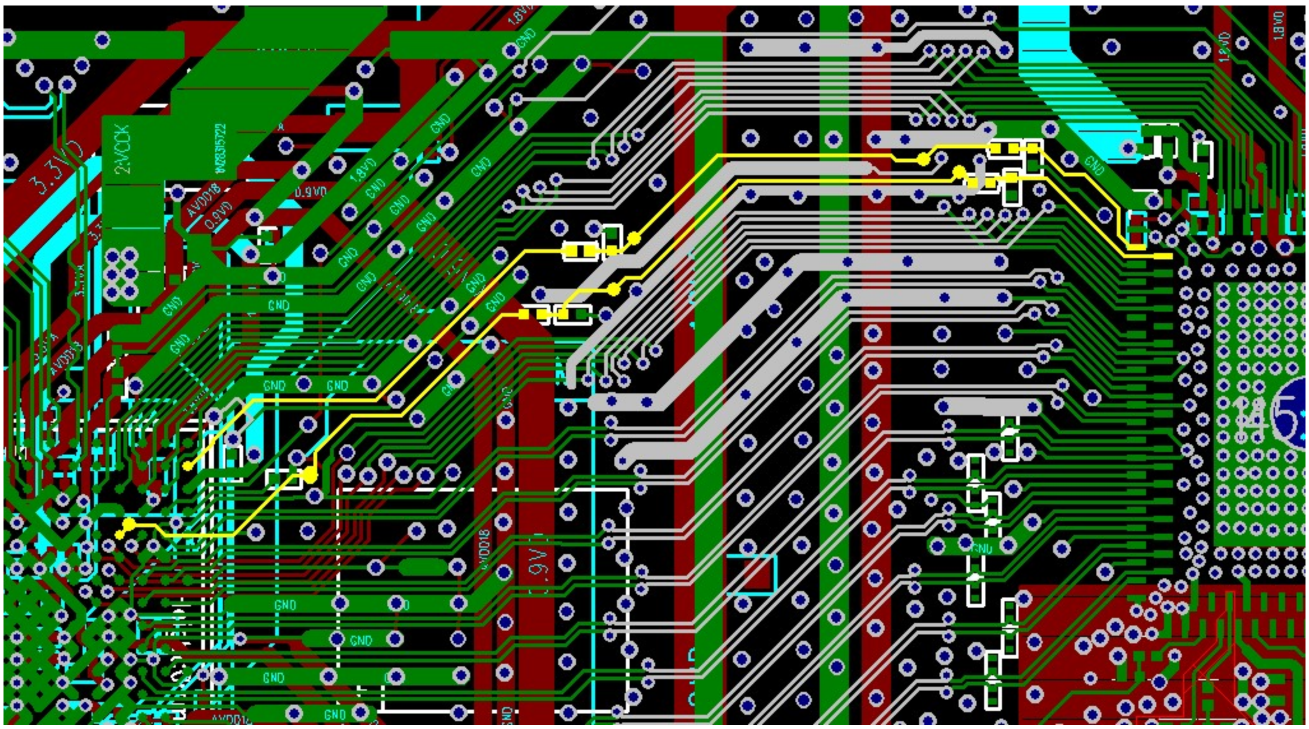



**Fig 4-29 : The G-band/A Band A die AIQ layout**

#### 4.2.11 AFE WRI trace design guide

WF0/1_HB0~10 must control the same length the WF0 or WF1 group delta can't over 15mm (Timing around 100ps)

Two RC circuits for HB0 & HB0_B should be reserved to prevent WIFI RX desense.
And 4.7pF are recommended for the caps that are closed to MT7981.



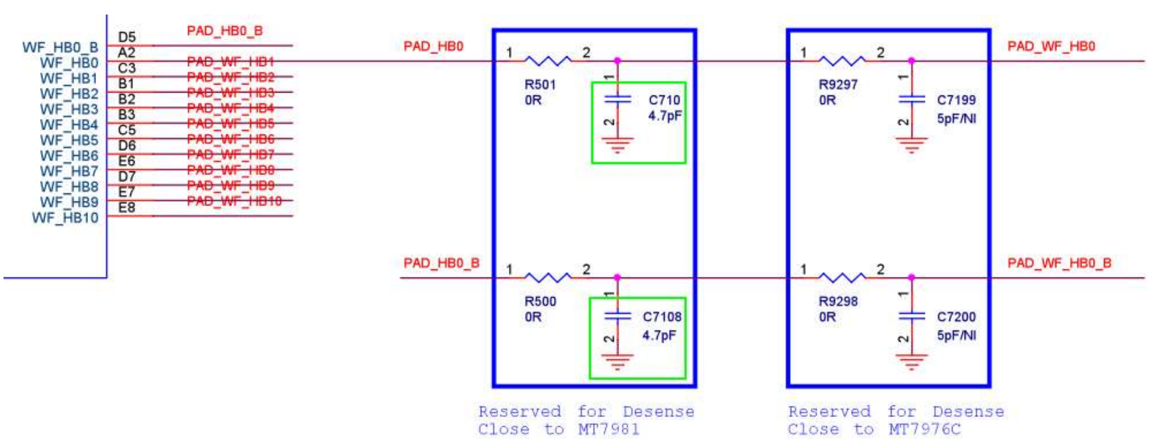



**Fig 4-30 : WF0 HB0/HB0_B is CLK keep other signal away**

#### 4.2.12 PA AVDD33 power De-cap placement.

De-cap location is as close as possible to the MT7976 power pin.
De-cap capacitor location placed from small capacitance to large capacitance.

- IC pin →1pF →10pF →1uF

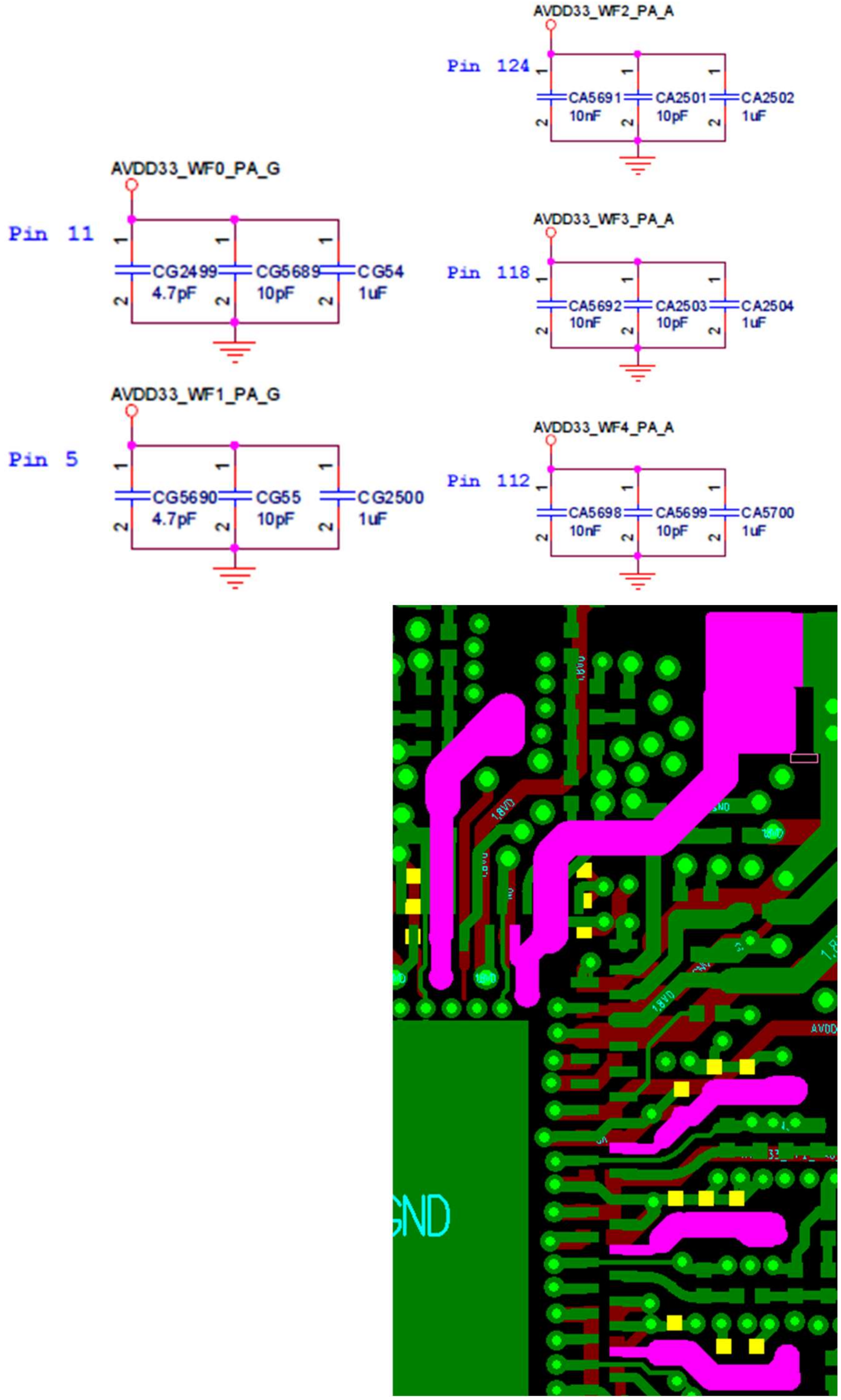



Fig 4-31 : PA AVDD33 power De-cap placemen

#### 4.2.13 GND connection.

1. Make sure that the GND of the IC is connected to the EPAD GND plane.
2. Enhance & improve GND return path.

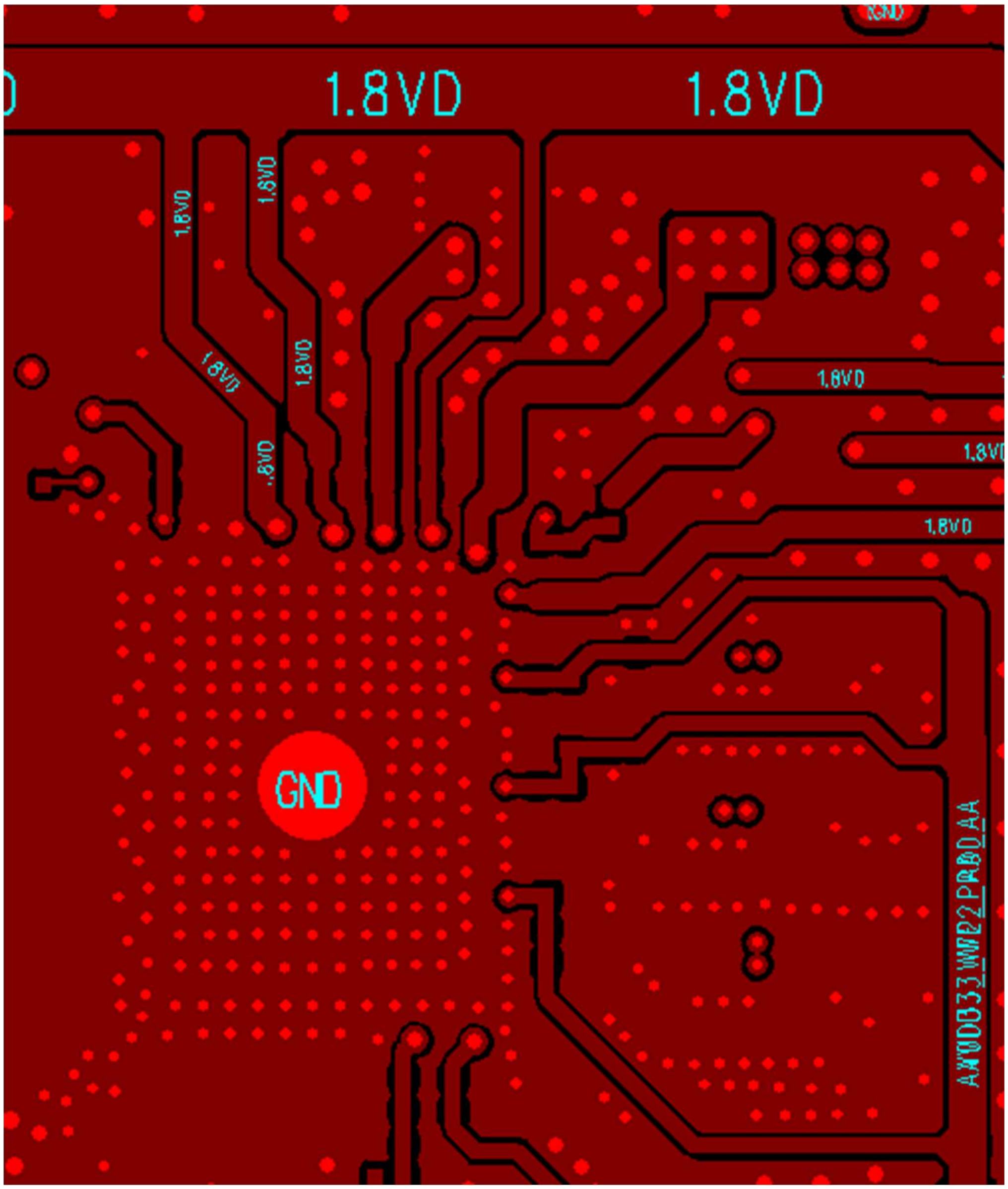



**Fig 4-32 : GND connection**

#### 4.2.14 MT7976 thermal via.

3. In the MT7976 E-pad, using a via hole with 2mm diameter to improve heat dissipation efficiency.
4. Remove solder mask improve thermal.
5. Add more GND via on EPAD to improve heat dissipation.

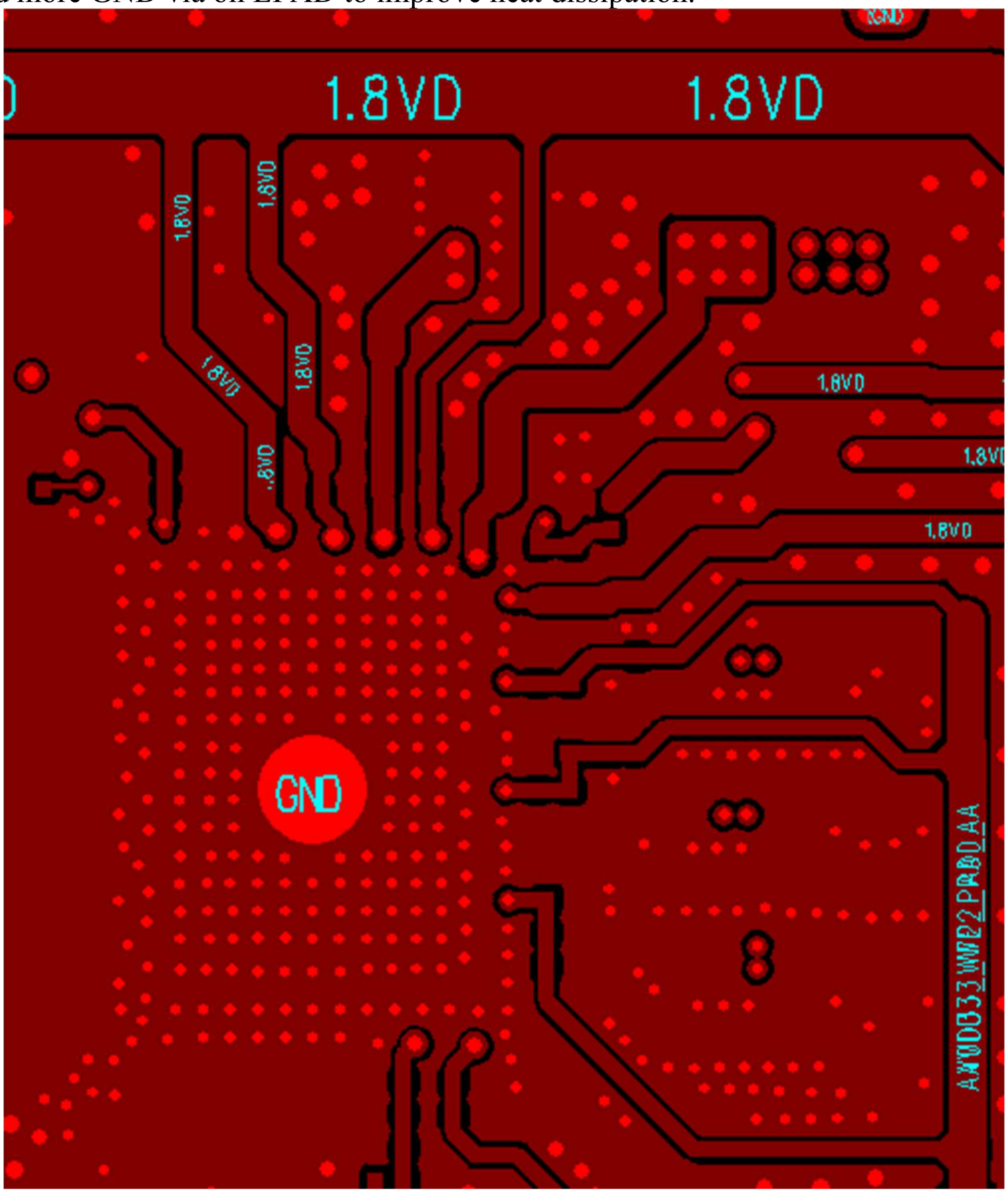



Fig 4-33 : Thermal via

#### 4.2.15 MT7976 Xtal trace

1. Isolated Crystal trace and 3.3V
2. Need to keep-out in layer 2 ➔ Cload consideration
3. Reserve 0R for debugging
4. Well-grounded required

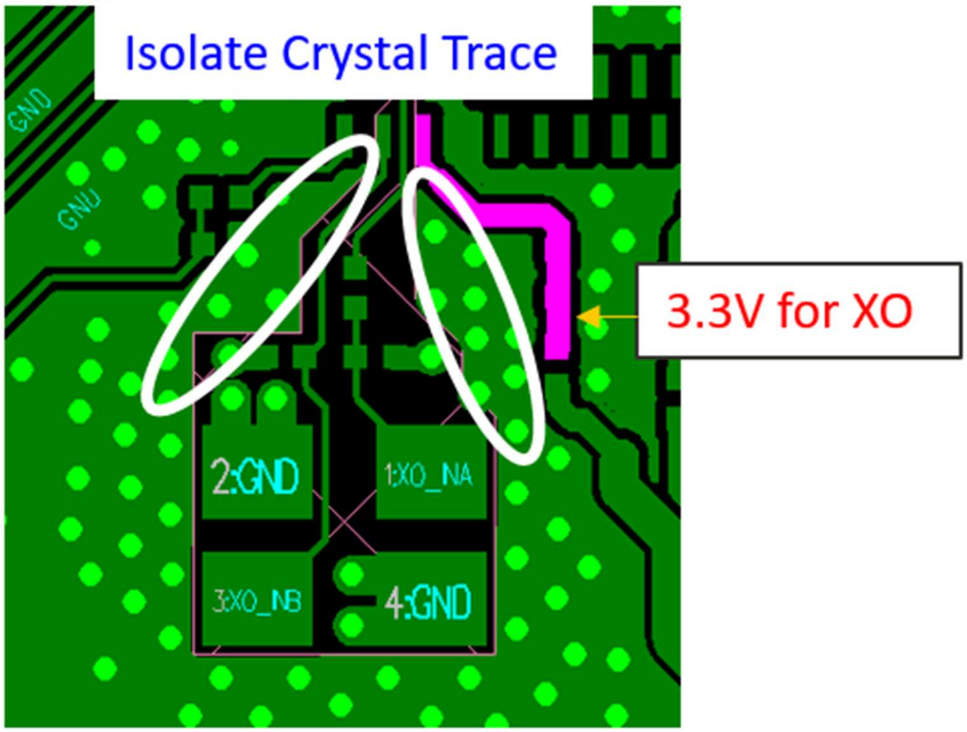



Fig 4-34 : MT7976 Xtal Trace

#### 4.2.16 MT7976 Power Trace Routing Rule

1. Separate 3.3V PA to WF0/1 & WF2/3/4.
2. Using star connection routing to 3.3V PA power trace.
3. PA power trace width > 0.7mm

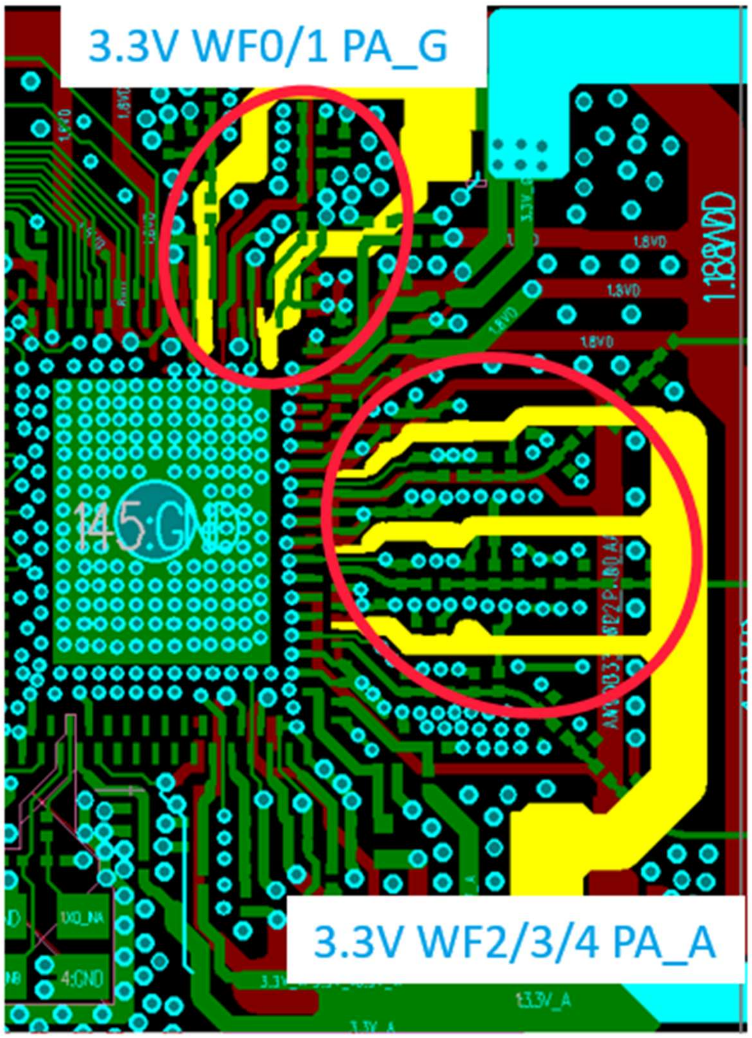



**Fig 4-35 : MT7976 Power Trace Routing Rule**

#### 4.2.17 MT7976 5G PA Power Trace Routing Rule

1. Separate 3.3V PA_A & PAD_A power trace (A band).
2. Using star connection routing to 3.3V PA& PAD power trace.
3. PA power trace width > 0.7mm (yellow line)
4. PAD power trace width > 0.3mm (pink line)

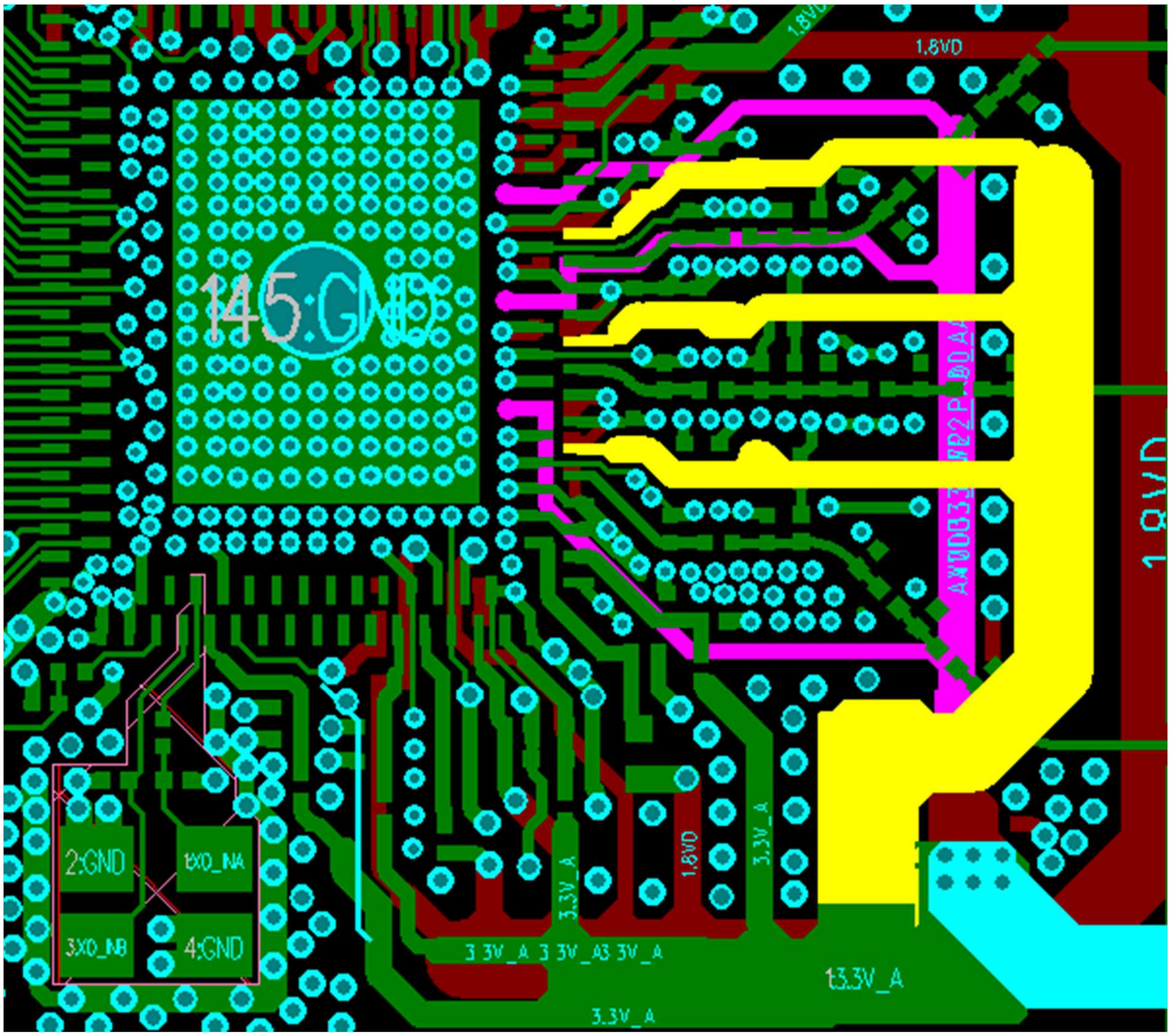



**Fig 4-36 : MT7976 5G PA Power Trace Routing Rule**

#### 4.2.18 MT7976 1.8V Power Trace Routing Rule

1. Using star connection routing to RF 1.8V power trace.
2. RF 1.8 trace width > 0.2mm (input to IC)

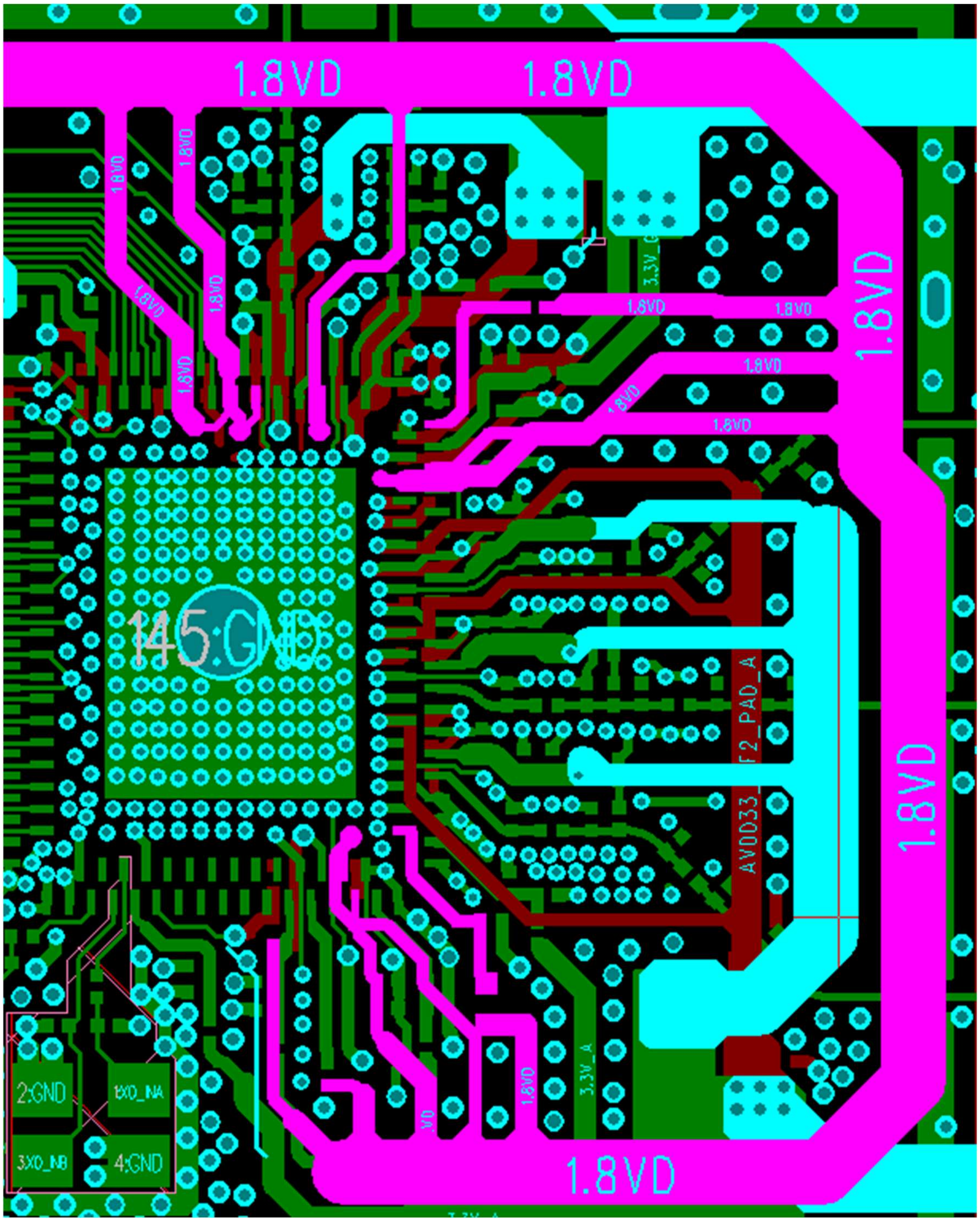



**Fig 4-37 : MT7976 1.8V Power Trace Routing Rule**

#### 4.2.19 MT7976 Band-gap pin isolate

1. Isolated Band-gap pin(pin102/141).
2. Band gap power trace must be separated from 3.3V PA power trace, don't be tied with 3.3V PA
3. Notice band gap pin grounding.

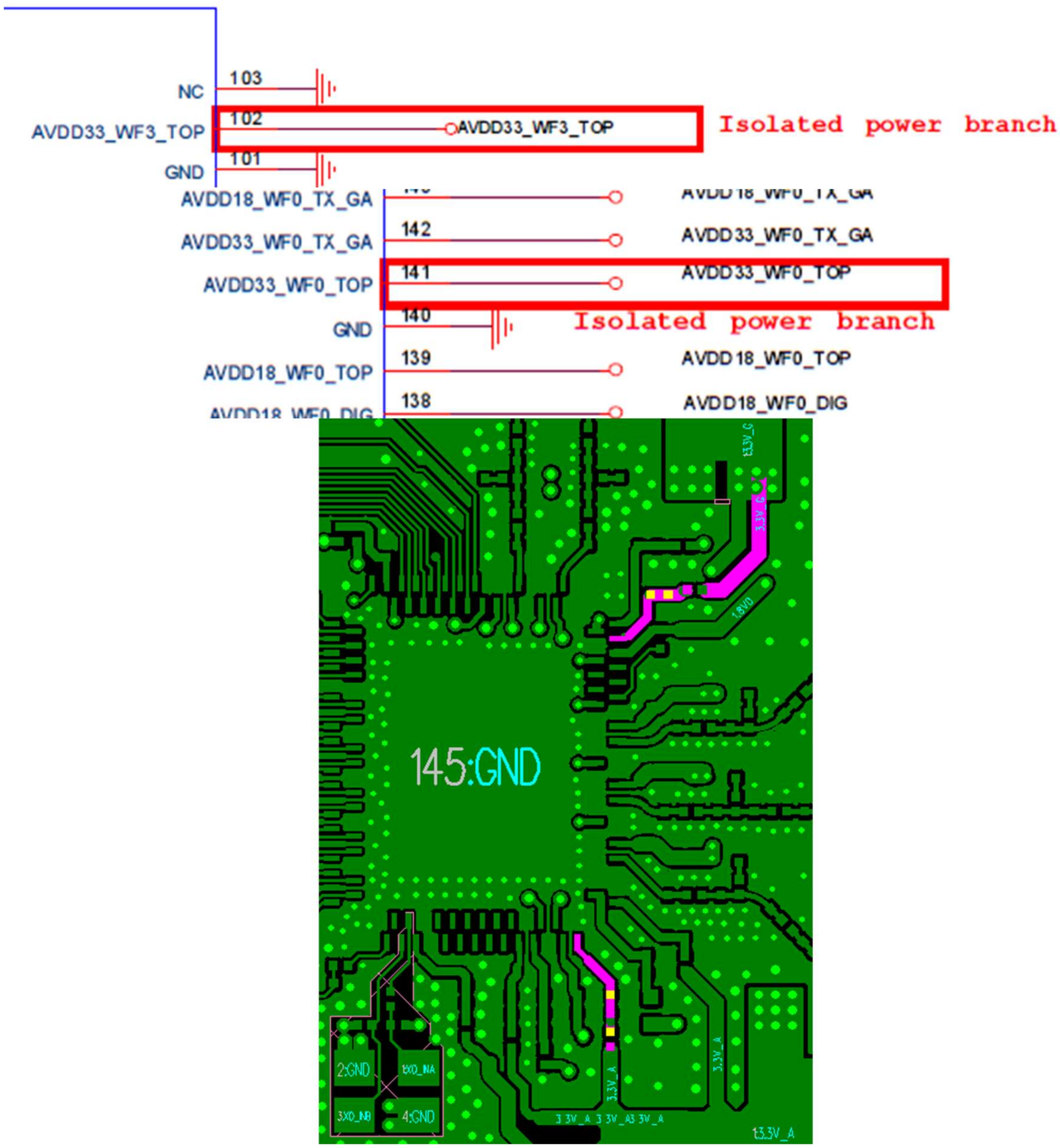



Fig 4-38 : MT7976 Band-gap pin isolate

#### 4.2.20 Shielding frame

- Shielding for harmonic emission, as closed as to prevent RF leakage
- Recommend shielding case height >=3mm

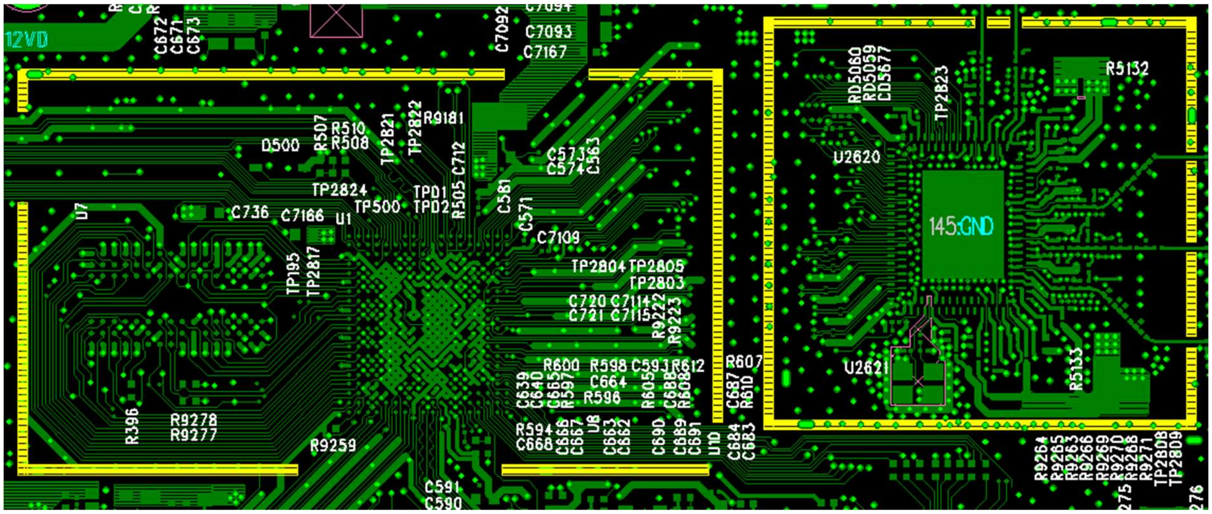



Fig 4-39 : shielding frame

#### 4.2.21 Crystal

Xtal :

- The **25MHz** **DIP/SMD** **Xtal** designed for MT7531
  **Xtal line trace/clearance = 4/4 mil, length 512.78 mil**
- Each layer's signal & ground keep out area is shown below (L1/L2/L3/L4)
- The Xtal trace should be well GND shielding

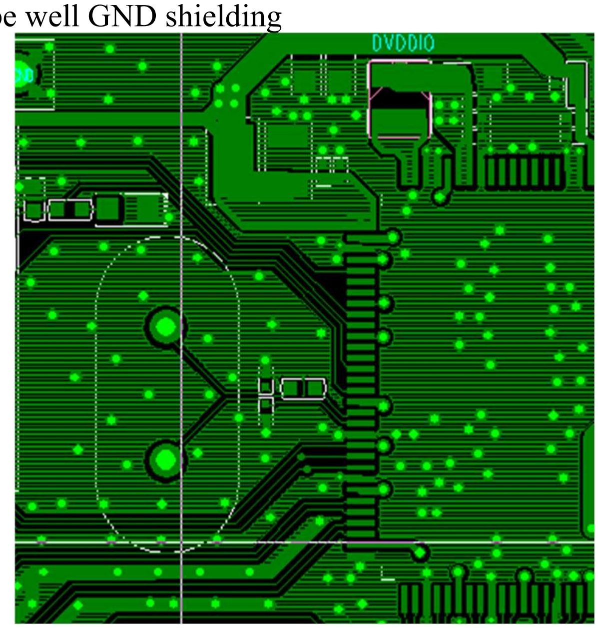



Fig 4-40 : Crystal layout guidelines

#### 4.2.22 Co-CLK design

There are two clock input from MT7976 to MT7981B:

- **Typical 40MHz, 1.2Vpp**
- Each layer's signal & ground keep out area is shown below (L1/L2/L3/L4)
- The OSC trace should be well GND shielding, at least two GND via space to AIQ signal.

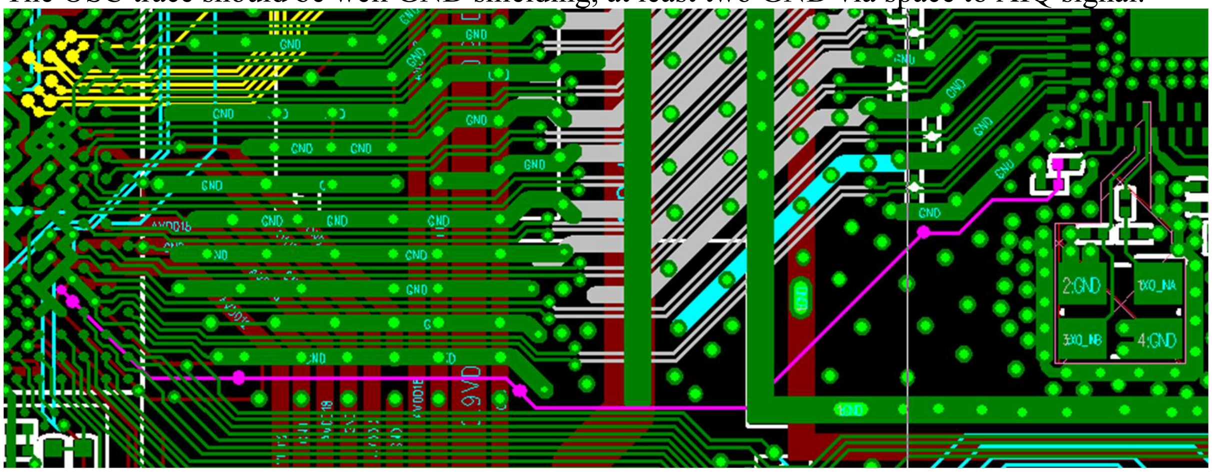


**Fig 4-41 : OSC guidelines**

#### 4.2.23 Flash Interface

There are 4 kinds flash support by MT7981B, SPIM-NOR, SPIM-NAND(ECC free), eMMC, SNFI (SPI NAND host ECC)

##### 4.2.23.1.1 SPI Flash (SPI NAND Flash Interface (SNFI), SPIM NAND, SPI NOR)

For SPI CLK/Data Bus :

- Add a damping resistor on the SPI-CLK , and place it close to SPI-NAND device, and the damping R is recommend to be fined tuned by over/under-shoot waveform.
- The max recommended routing length of CLK/Data is 4000mil
- The difference of CLK/Data bus length ≦400mil
- ≦3 through holes on the CLK/Data bus
- SPI-CLK routing trace could be well protected with solid GND plane (option)

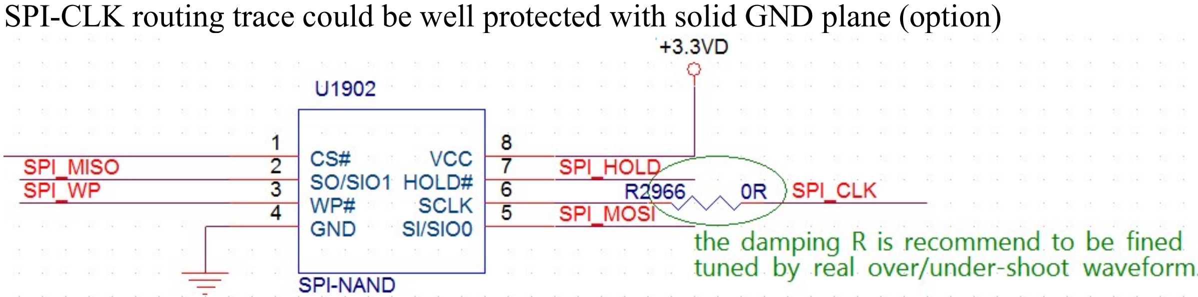



**Fig 4-42 : SPI Flash layout guidelines**

#### 4.2.23.1.2 eMMC 4.5

For eMMC 4.5 only support 3.3V power, and share bus with SPI0/SPI1/PWM0:
Layout guide should follow eMMC design guide

- Mismatch within DAT0~DAT7 ≤300 mil
- CLK to DAT0-7 mismatch ≤ 300 mil
- CLK to CMD mismatch ≤ 300 mil
- CLK to RST_N mismatch ≤ 1000 mil

Decoupling CAPs should be placed close VCC/VCCQ pins.

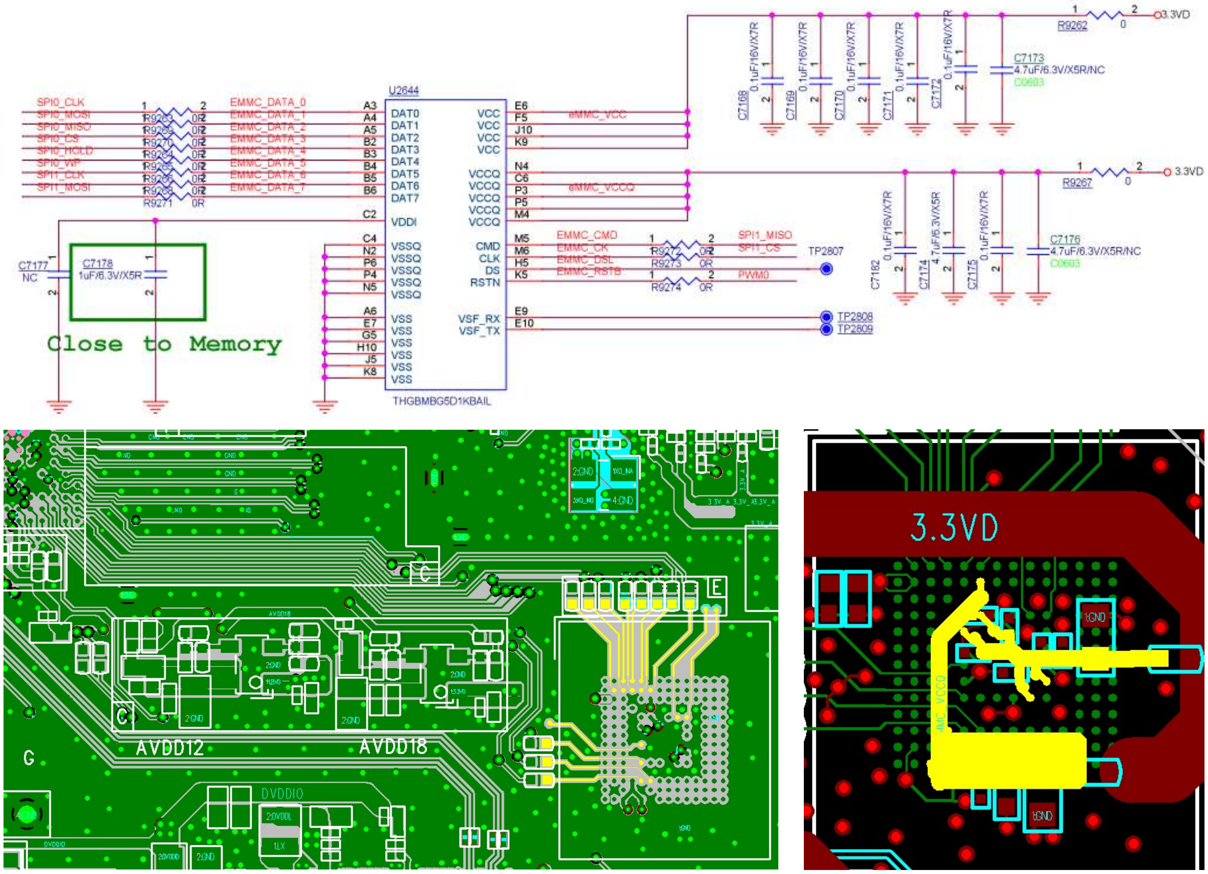



**Fig 4-43 : eMMC NAND SCH/PCB deign**

### 4.3 MT7981B & MT7976 Thermal Characteristics

Thermal characteristics when stationary without an external heat sink in an air-conditioned environment.

| Symbol | Description | Performance | |
|---|---|---|---|
| | | Typ | Unit |
| TJ | Maximum Junction Temperature (Plastic Package) | **125** | °C |
| θJA | Junction to ambient temperature thermal resistance[1] for JEDEC 2L PCB | **23.65** | °C/W |
| θJA | Junction to ambient temperature thermal resistance[1] for JEDEC 4L PCB | **18.05** | °C/W |
| θJB | Junction to bottom temperature thermal resistance | **8.41** | °C/W |
| θJC | Junction to case temperature thermal resistance | **8.05** | °C/W |
| ψJt | Junction to the package thermal resistance for JEDEC 2L PCB | **1.75** | °C/W |
| ψJt | Junction to the package thermal resistance for JEDEC 4L PCB | **1.15** | °C/W |

**Table 4-5 : MT981B Thermal Characteristics**

**MT7976:**
Thermal characteristics without external heat sink in still air condition
Thermal Resistance θJA (°C /W) for JEDEC 2L system PCB……………………………………………………26.59°C/W
Thermal Resistance θJA (°C /W) for JEDEC 4L system PCB……………………………………………………18.51°C/W
Thermal Resistance θJC (°C /W) for JEDEC system PCB…………………………………………………………2.94 °C/W
Thermal Resistance θJB (°C /W) for JEDEC system PCB…………………………………………………………2.68 °C/W
Thermal Characterization parameter ΨJt (°C /W) for JEDEC 2L system PCB………………………………..2.34 °C/W
Thermal Characterization parameter ΨJt (°C /W) for JEDEC 4L system PCB………………………………..1.48 °C/W
NOTE: JEDEC 51-7 system FR4 PCB size: 76.2x114.3mm (3”x4.5”)

**Table 4-6 : MT7976 Thermal Characteristic**

# 5 PHY test commands

## 5.1 Ethernet PHY test commands

### 5.1.1 MT7531 1000-TX mode command

Command format: switch phy cl22 w [port] [CR address] [value]

<Example> port0 test command

Test mode1
```
switch phy cl22 w 0 31 0x0;        //switch to P0 register offset to 0x0
switch phy cl22 w 0 0 0x0140;      //forced link P0 at 1000Mbps
switch phy cl22 w 0 9 0x2600;      //Set transmit test mode 1
```

Test mode2
```
switch phy cl22 w 0 31 0x0;        //switch to P0 register offset to 0x0
switch phy cl22 w 0 0 0x0140;      //forced link P0 at 1000Mbps
switch phy cl22 w 0 9 0x4600;      //Set transmit test mode 2
```

Test mode3
```
switch phy cl22 w 0 31 0x0;        //switch to P0 register offset to 0x0
switch phy cl22 w 0 0 0x0140;      //forced link P0 at 1000Mbps
switch phy cl22 w 0 9 0x6600;      //Set transmit test mode 3
```

Test mode4
```
switch phy cl22 w 0 31 0x0;        //switch to P0 register offset to 0x0
switch phy cl22 w 0 0 0x0140;      //forced link P0 at 1000Mbps
switch phy cl22 w 0 9 0x8600;      //Set transmit test mode 4
```

### 5.1.2 **MT7531** 100-TX mode command

<Example> port0 test command

```
#MDI
switch phy cl22 w 0 31 0x0;
switch phy cl22 w 0 0 0x2100;              //forced link P0 at 100Mbps
switch phy cl45 w 0 0x1e 0x145 0x5010;     //switch to MDI


#MDIX
switch phy cl22 w 0 31 0x0;
switch phy cl22 w 0 0 0x2100;              //forced link P0 at 100Mbps
switch phy cl45 w 0 0x1e 0x145 0x5018;     //switch to MDIX
```

### 5.1.3 **MT7531** 10-T mode command

<Example> port0 test command

```
#MDI/MDIX
switch phy cl45 w 0 0x1e 0x145 0x5010;     //switch to MDI
switch phy cl45 w 0 0x1e 0x145 0x5018;     //switch to MDIX

#Normal (note: must be apply for Random and Harmonic test items)
switch phy cl22 w 0 31 0x0;                //switch to P0 register offset to 0x0
switch phy cl22 w 0 00 0x0100;             //forced link P0 at 10Mbps
switch phy cl45 w 0 0x1e 0x145 0x5010;     //switch to MDI
switch phy cl45 w 0 0x1e 0x33 0x0177;      //disable EEE function

#Random packet
switch phy cl22 w 0 31 0x0001;
switch phy cl22 w 0 29 0xf842;

#Harmonic (note: this command can’t return to do other test items, please reboot if need)
switch phy cl22 w 0 31 0x0;
switch phy cl22 w 0 00 0x0100;
switch phy cl45 w 0 0x1e 0x145 0x5010;
switch phy cl45 w 0 0x1e 0x33 0x0177;
switch phy cl22 w 0 31 0x0001;
switch phy cl22 w 0 29 0xfe40;
```

### 5.1.4 MT7981 1000-TX mode command

<Example> port0 test command
Command format: mii_mgr -s -p **[port]** -r [CR address] -v [value]
Command format: mii_mgr_cl45 -s -p **[port]** -d [CR address1] -r [CR address2] -v [value]

#1000 test mode1

mii_mgr -s -p 0 -r 31 -v 0x0
mii_mgr -s -p 0 -r 00 -v 0x0140
mii_mgr -s -p 0 -r 09 -v 0x2600

#1000 test mode2

mii_mgr -s -p 0 -r 31 -v 0x0
mii_mgr -s -p 0 -r 00 -v 0x0140
mii_mgr -s -p 0 -r 09 -v 0x4600

#1000 test mode3

mii_mgr -s -p 0 -r 31 -v 0x0
mii_mgr -s -p 0 -r 00 -v 0x0140
mii_mgr -s -p 0 -r 09 -v 0x6600

#1000 test mode4

mii_mgr -s -p 0 -r 31 -v 0x0
mii_mgr -s -p 0 -r 00 -v 0x0140
mii_mgr -s -p 0 -r 09 -v 0x8600

### 5.1.5 MT7981 100-TX mode command

#MDI
mii_mgr -s -p 0 -r 31 -v 0x0
mii_mgr -s -p 0 -r 00 -v 0x2100
mii_mgr_cl45 -s -p 0 -d 0x1e -r 0x145 -v 0x5010;

#MDIX
mii_mgr -s -p 0 -r 31 -v 0x0
mii_mgr -s -p 0 -r 00 -v 0x2100
mii_mgr_cl45 -s -p 0 -d 0x1e -r 0x145 -v 0x5018;

### 5.1.6 MT7981 10-TX mode command

# MDI/MDIX  (default use MDI below)
mii_mgr_cl45 -s -p 0 -d 0x1e -r 0x145 -v 0x5010;
mii_mgr_cl45 -s -p 0 -d 0x1e -r 0x145 -v 0x5018;

#Normal link pulse: (note: must be apply for Random and Harmonic test items)
mii_mgr -s -p 0 -r 0x1f -v 0x0;
mii_mgr -s -p 0 -r 0x0 -v 0x0100;
mii_mgr_cl45 -s -p 0 -d 0x1e -r 0x145 -v 0x5010;  //MDI
mii_mgr_cl45 -s -p 0 -d 0x1e -r 0x33 -v 0x0177;

#Random packet:
mii_mgr -s -p 0 -r 0x1f -v 0x0001;
mii_mgr -s -p 0 -r 0x1d -v 0xf842;

#Harmonic (note: this command can't return to do other test items, please reboot if need)
mii_mgr -s -p 0 -r 0x1f -v 0x0;
mii_mgr -s -p 0 -r 0x0 -v 0x0100;
mii_mgr_cl45 -s -p 0 -d 0x1e -r 0x145 -v 0x5010;
mii_mgr_cl45 -s -p 0 -d 0x1e -r 0x33 -v 0x0177;

mii_mgr -s -p 0 -r 0x1f -v 0x0001;
mii_mgr -s -p 0 -r 0x1d -v 0xf840;

## 5.2 USB3 compliance test command

USB3 Compliance Test command

U3 driver default disable CTS mode，it need to set below register to enable CTS mode to test TX compliance. Enable CTS mode setting:

cd /sys/devices/platform/11200000.xhci;
echo 1 >usb3hqa;

## 5.3 USB 2.0 compliance test setting & command

### 5.3.1 USB 2.0 background information

MT7981 can support 1 USB 2.0 High speed ports, and below are register layout information.

```
port        offset    bank
u2 port0    0x0000    MISC
            0x0100    FMREG
            0x0300    U2PHY_COM
u3 port0    0x0700    SPLLC
            0x0800    CHIP
            0x0900    U3PHYD
            0x0a00    U3PHYD_BANK2
            0x0b00    U3PHYA
            0x0c00    U3PHYA_DA
```

### 5.3.2 Software programming

Enable xHCI USB 2.0 toolkits (Please check Software Engineer)

CONFIG_USB_XHCI_MTK_DEBUGFS=y
CONFIG_DEBUG_FS=y

### 5.3.3 Eye-pattern parameter

To submit final your parameters tied in eye-pattern to *.dts file of your project

```
&u2port0 {
mediatek,eye-src = <0x04>;
mediatek,eye-vrt = <0x04>;
mediatek,eye-term = <0x05>;
status = “okay”;
};
```

#### 5.3.4 USB2 compliance Test Command

##### 5.3.4.1 Host High-speed Signal Quality (EL_2, EL_3, EL_6, EL_7)

CLI: echo -n test.packet 2 > /sys/devices/platform/11200000.xhci/hqa

##### 5.3.4.2 Host Controller Packet Parameter (EL_21, EL_22, EL_23, EL_25, EL_55)

CLI: echo -n test.getdesc 2 > /sys/devices/platform/11200000.xhci/hqa

##### 5.3.4.3 Host CHIRP Timing (EL_33, EL_34, EL_35)

CLI: echo -n test.enumbus 2 > /sys/devices/platform/11200000.xhci/hqa

##### 5.3.4.4 Host Suspend/Resume timing (EL_39, EL_41)

CLI (suspend): echo -n test.suspend 2 > /sys/devices/platform/11200000.xhci/hqa

CLI (resume): echo -n test.resume 2 > /sys/devices/platform/11200000.xhci/hqa

##### 5.3.4.5 Host Test J/K, SE0_NAK (EL_8, EL_9)

CLI (J): echo -n test.j 2 > /sys/devices/platform/11200000.xhci/hqa

CLI (K): echo -n test.k 2 > /sys/devices/platform/11200000.xhci/hqa

CLI (SE0): echo -n test.se0 2 > /sys/devices/platform/11200000.xhci/hqa

##### 5.3.4.6 Drop Test

CLI: none

Refer USB Specification as below link:
USB Electrical Compliance Specification v1.07.pdf
https://usb.org/sites/default/files/USB%202%200%20Electrical%20Compliance%20Specification%28v1.07%29.pdf

### 5.4 SGMII TX Test command & SOP

#### 5.4.1 Test Item

A. TX Electrical
B. TX Eye Mask.

Table 5-1 lists the test equipment and Figure 5-1. Shows the realistic setup connections.

### **5.4.2** Test Equipment

| Equipment | Quantity |
|---|---|
| Agilent Scope (BW >8G) | 1 |
| BNC to SMA Connector (for scope) | 2 |
| RF cable with SMA | 2 |
| Agilent Scope Mask Test | 1 |
| Semi rigid cable with SMA < 5cm.<br>(option : if no SMA Connector on board) | 2 |
| | |

**Table 5-1 : SGMII TX Test Equipment**

### **5.4.3** Test Environment Setup

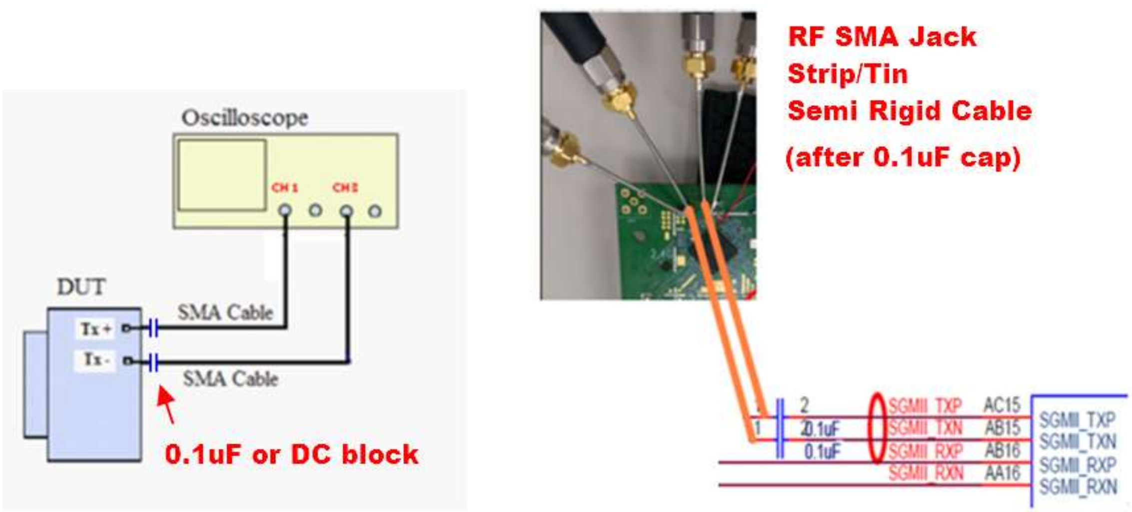



**Fig 5-1 : SGMII TX Electrical Test Environment Setup Diagram**

### **5.4.4** (H)SGMII Enable SSC Command

HSGMII SSC driver default is disable, Customer can use below command to enable SSC mode to compare RF de-sense or EMI.

MT7531 SSC enable :
Port 6 (default is for CPU port)
switch reg w 6110 40000000;
switch reg w 6100 120044f;

Port 5
switch reg w 5110 40000000;
switch reg w 5100 120044f;

MT7981 SSC enable :
HSGMII0
regs w 0x10060110 0x40002000;
regs w 0x10060100 0x12B484F;

HSGMII1
regs w 0x10070110 0x40002000;
regs w 0x10070100 0x12B484F;

#### 5.4.5 (H)SGMII 2.5G/1G force speed command

MT7531A
# port5
# force 2.5G (Gen2)
switch reg w 50e8 10
switch reg w 5128 14817
switch reg w 5020 31120009
switch reg w 5000 140
switch reg w 50e8 0

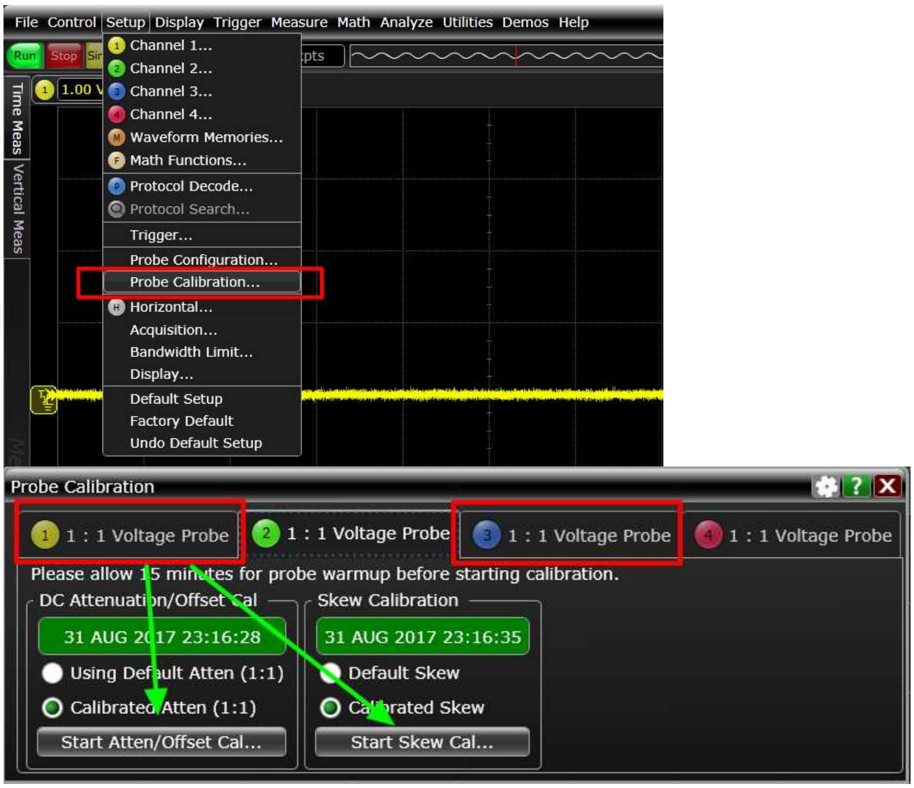
# force 1G (Gen1)
switch reg w 50e8 10
switch reg w 5128 14813
switch reg w 5020 31120009
switch reg w 5000 140
switch reg w 50e8 0

# port6
# force 2.5G (Gen2)
switch reg w 60e8 10
switch reg w 6128 14817
switch reg w 6020 31120009
switch reg w 6000 140
switch reg w 60e8 0

```
# force 1G (Gen1)
switch reg w 60e8 10
switch reg w 6128 14813
switch reg w 6020 31120009
switch reg w 6000 140
switch reg w 60e8 0


MT7981
# SG1 force 2.5G (gen2)
regs w 100700e8 10
regs w 10070128 14817
regs w 10070020 31120019
regs w 10070000 140
regs w 100700e8 0

# SG1 force 1G (gen1)
regs w 100700e8 10
regs w 10070128 14813
regs w 10070020 31120019
regs w 10070000 140
regs w 100700e8 0

# SG0 force 2.5G (gen2)
regs w 100600e8 10
regs w 10060128 14817
regs w 10060020 31120019
regs w 10060000 140
regs w 100600e8 0

# SG0 force 1G (gen1)
regs w 100600e8 10
regs w 10060128 14813
regs w 10060020 31120019
regs w 10060000 140
regs w 100600e8 0
```

### 5.4.6 Test Procedure (TX Timing)

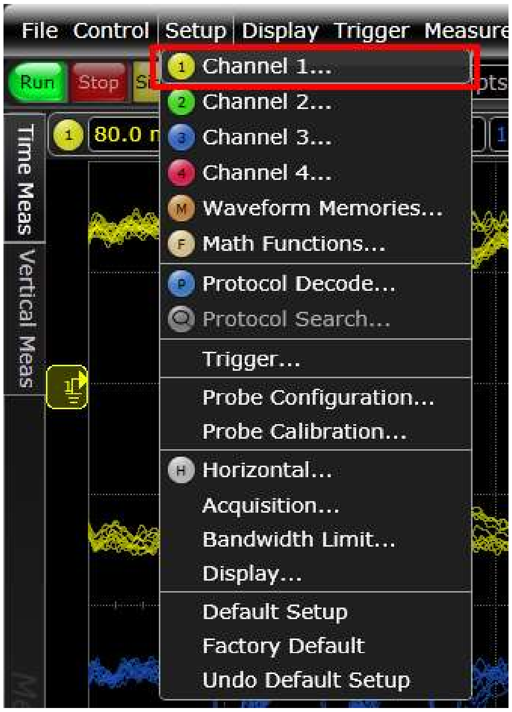
**1. Do scope channel (ex: CH1 and CH3) probe calibration first (* Must ).**

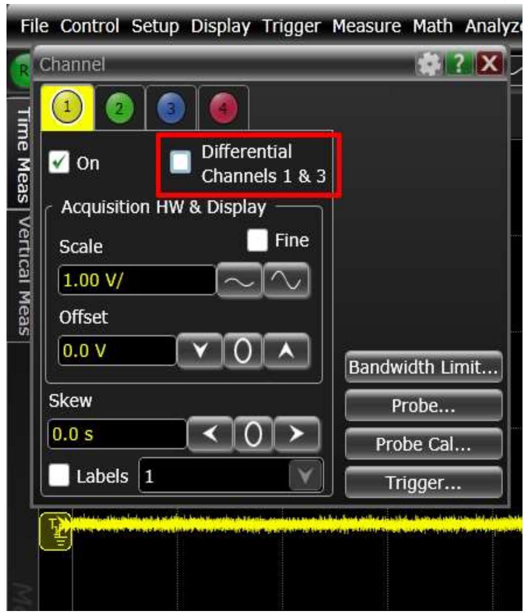



2. Use two RF cables with SMA to connect with DUT “SGMII_TX_P” and “SGMII_TX_N” to Agilent Scope “Channel 1 (TXP) ” and “Channel 3 (TXN) ”. Refer to Figure 1-1.

3. In Scope menu:

**Setup → Channel 1→** **Differential Channel 1&3** → select (☑) → **Channel1-3**




**4. Measure → Add Measurement** → Select measurement items below.

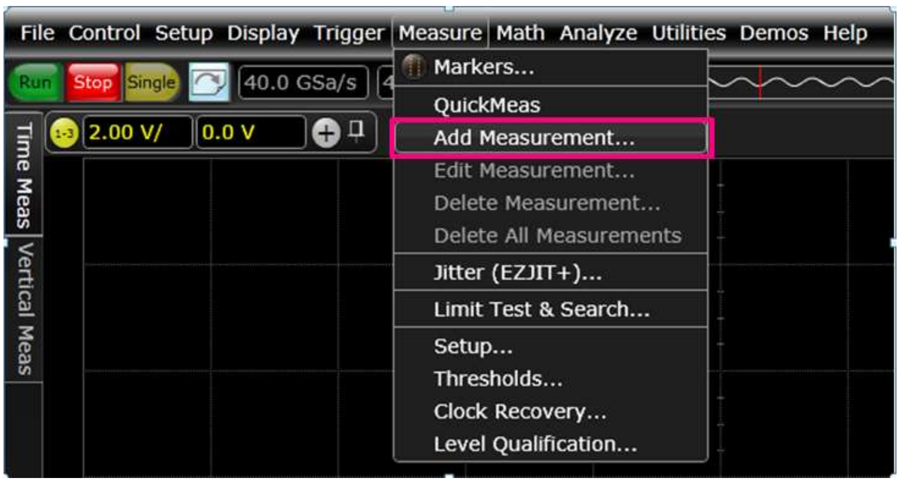
a. Rise time (Typical use 20% ~ 80% , Gen2 by level mode , ex: +/-250mV)

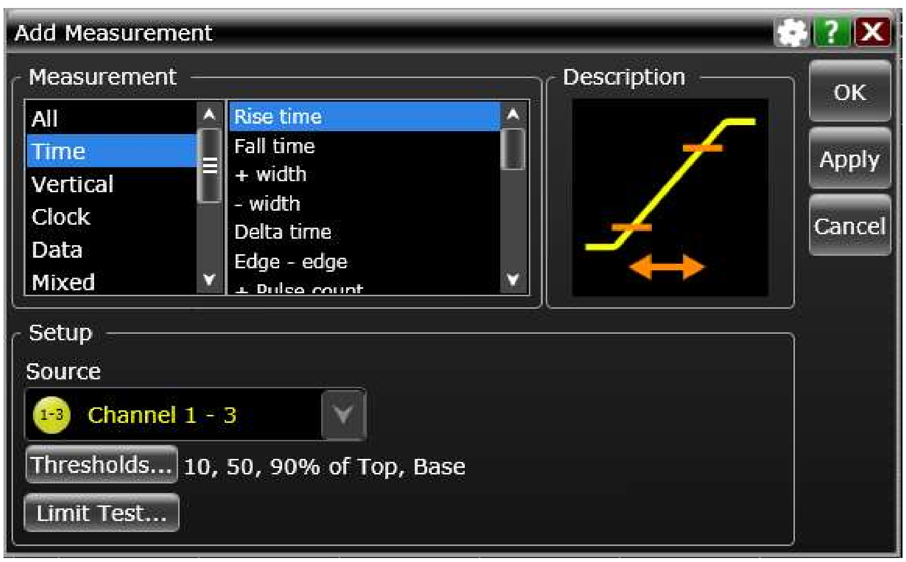
b. Fall time

c. V p-p

d. Unit Interval

e. Data rate

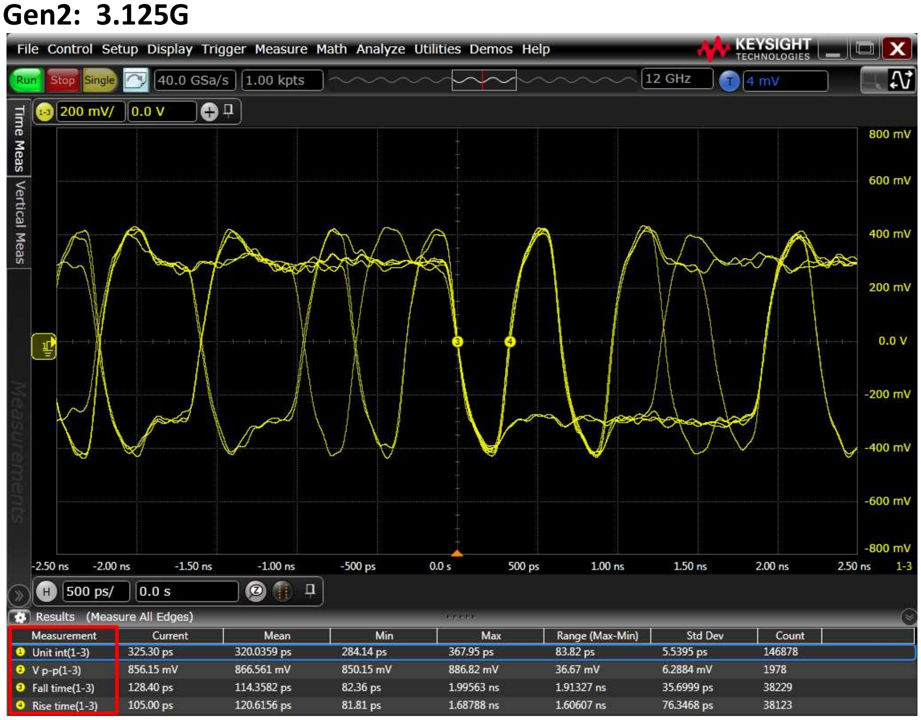


## 5. Electrical Measurement Result example.

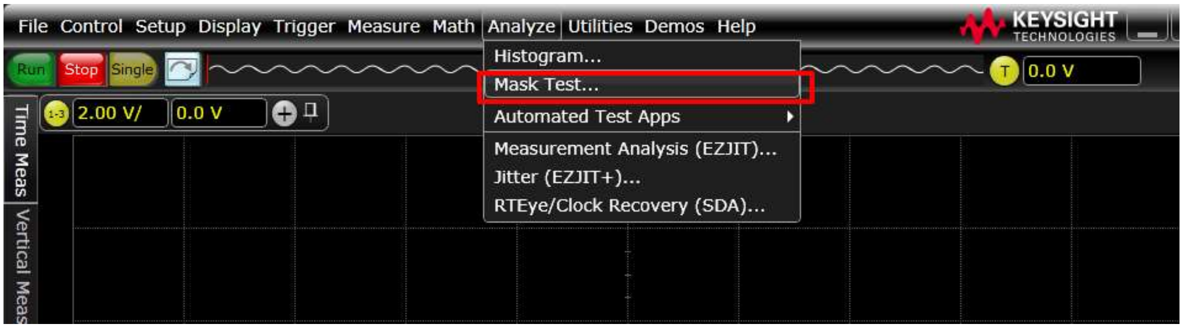
### Gen1: 1.25G


### Gen2: 3.125G



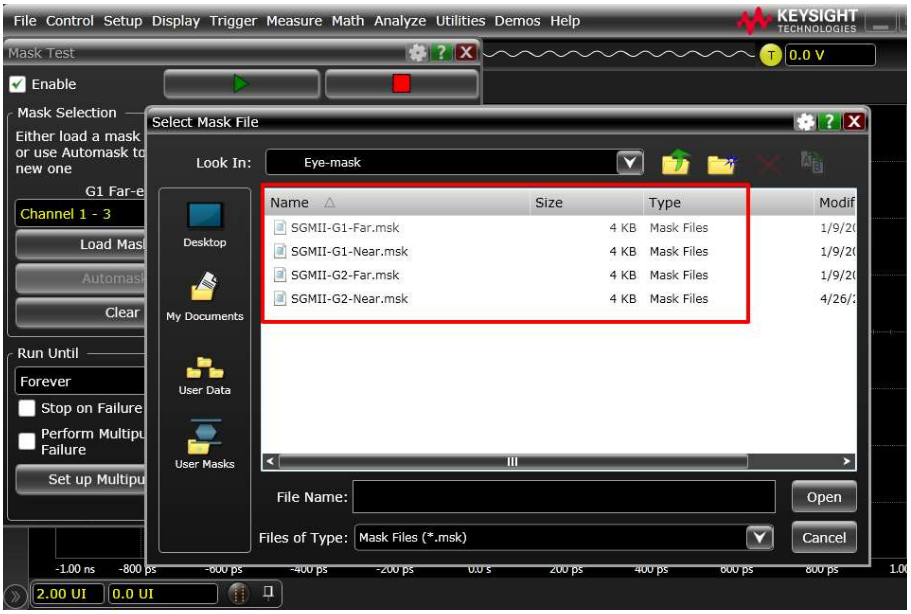
### 5.4.7 Test Procedure (TX Eye Mask)

**#Test command the same as TX Electrical Test (both Gen1/Gen2)**
**Scope Setup → Analyzer → select Mask Test.**



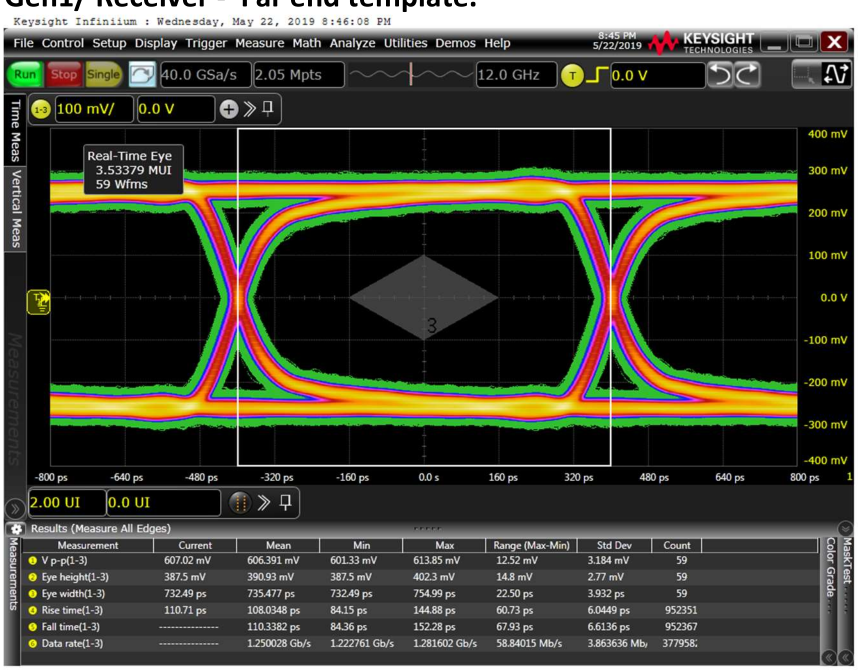

**Enable Mask Test.**

**Load Gen1/Gen2 & Near End/Far End Mask file.**



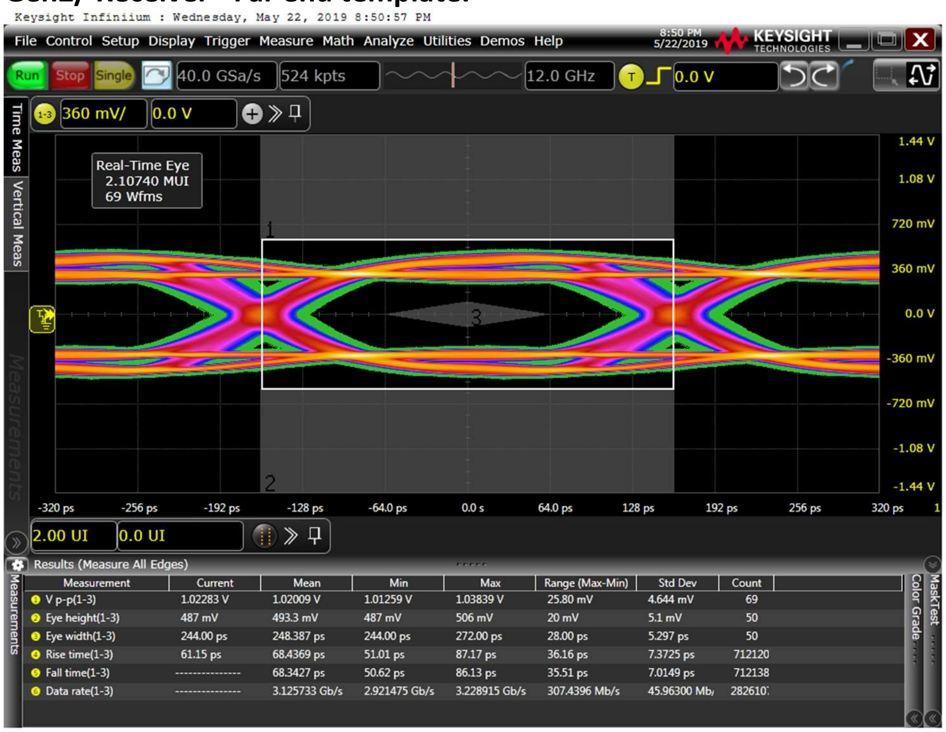

**Example: Gen1 TX Eye Mask.**

**Gen1/ Receiver - Far end template.**



**Example: Gen2 TX Eye Mask.**

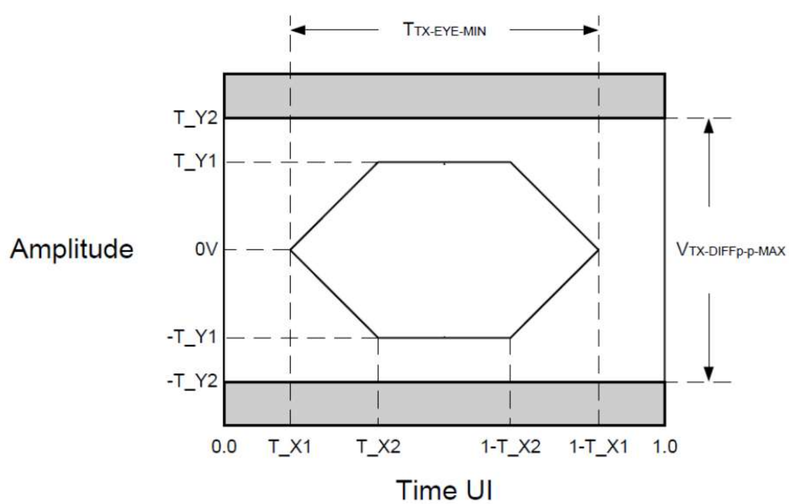
**Gen2/ Receiver - Far end template.**



### 5.4.8 TX Electrical Timing Spec

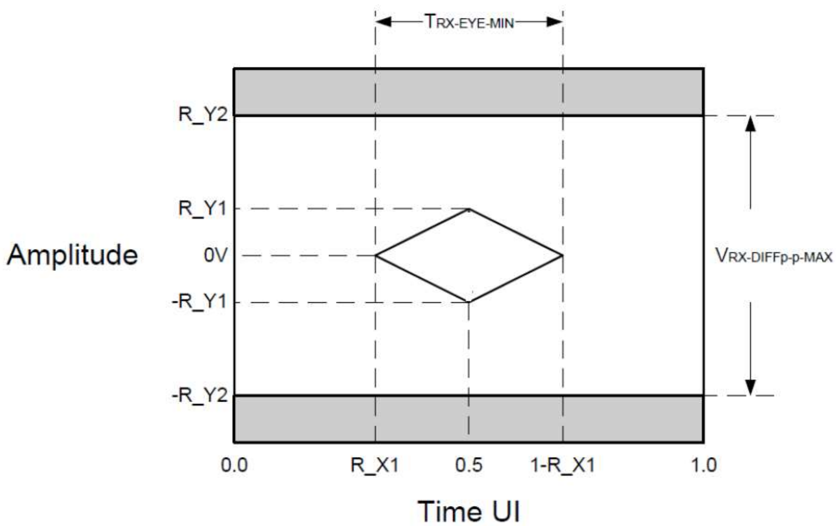
## Gen1 (1.25G) - Differential Transmitter Timing

| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| UI | Unit Interval | 799.92 | 800 | 800.08 | ps | Mean value |
| T_X1 | Eye Mask | - | - | 0.15 | UI | |
| T_X2 | Eye Mask | - | - | 0.4 | UI | |
| T_Y1 | Eye Mask | 140 | - | - | mV | |
| T_Y2 | Eye Mask | - | - | 400 | mV | |
| $V_{TX\text{-}DIFFp\text{-}p}$ | Output Diff Voltage | 300 | 500 | 800 | mV | Vp-p |
| $T_{TX\text{-}EYE}$ | Minimum TX Eye Width | 0.7 | - | - | UI | |
| $T_{TX\text{-}JITTER}$ | Output Jitter | - | - | 0.3 | UI | |
| $T_{TX\text{-}RISE}$ | Output Rise Time | 0.075 | - | - | UI | |
| $T_{TX\text{-}FALL}$ | Output Fall Time | 0.075 | - | - | UI | |
| $R_{TX}$ | Differential Resistance | 80 | 100 | 120 | ohm | |
| $C_{TX}$ | AC Coupling Capacitor | 80 | 100 | 120 | nF | |



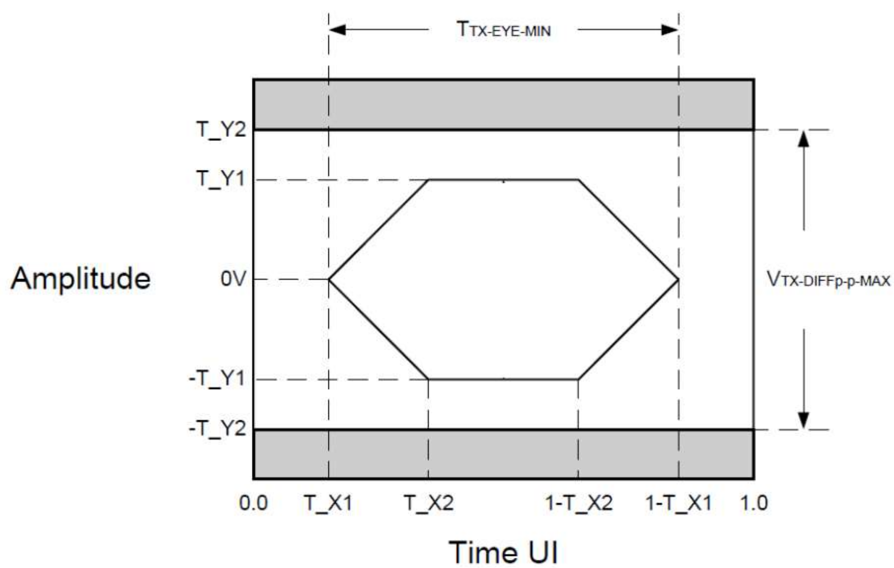
### Gen1 (1.25G) - Differential Receiver Timing

| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| UI | Unit Interval | 799.92 | 800 | 800.08 | ps | Mean value |
| T_X1 | Eye Mask | - | - | 0.3 | UI | |
| T_Y1 | Eye Mask | 100 | - | - | mV | |
| T_Y2 | Eye Mask | - | - | 600 | mV | |
| $V_{RX\text{-}DIFFp\text{-}p}$ | Input Diff Voltage | 200 | - | 1200 | mV | |
| $T_{RX\text{-}EYE}$ | Minimum TX Eye Width | 0.4 | - | - | UI | |
| $T_{RX\text{-}JITTER}$ | Output Jitter | - | - | 0.6 | UI | $1\text{-}T_{RX\text{-}EYE\text{-}MIN}$ |
| $R_{RX}$ | Differential Resistance | 80 | 100 | 120 | ohm | |



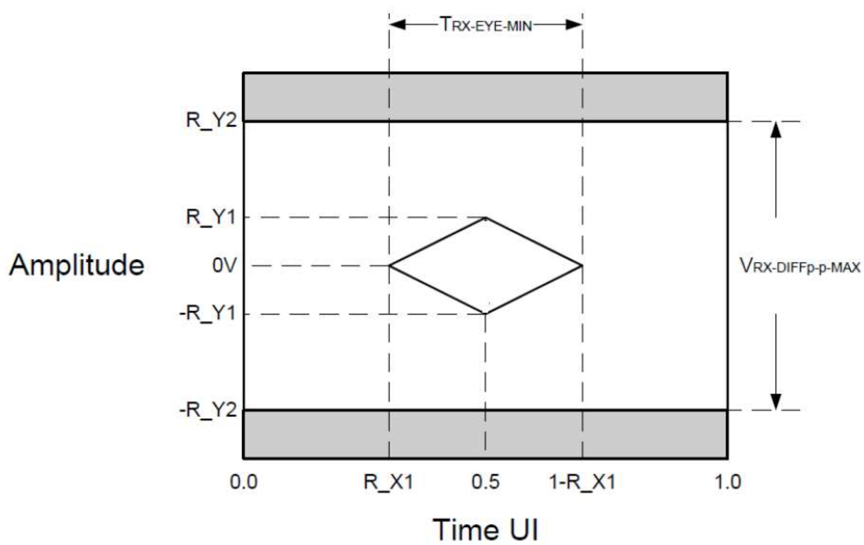
## HSGMII (3.125G) - Differential Transmitter Timing

| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| **UI** | Unit Interval | 319.96 | 320 | 320.04 | ps | Mean value |
| **T_X1** | Eye Mask | - | - | 0.175 | UI | |
| **T_X2** | Eye Mask | - | - | 0.4 | UI | |
| **T_Y1** | Eye Mask | 200 | - | - | mV | |
| **T_Y2** | Eye Mask | - | - | 800 | mV | |
| **$V_{TX-DIFFp-p}$** | Output Diff Voltage | 800 | 900 | 1200 | mV | Vp-p |
| **$T_{TX-EYE}$** | Minimum TX Eye Width | 0.65 | - | - | UI | |
| **$T_{TX-JITTER}$** | Output Jitter | - | - | 0.35 | UI | |
| **$T_{TX-RISE}$** | Output Rise Time | 0.125 | - | - | UI | |
| **$T_{TX-FALL}$** | Output Fall Time | 0.125 | - | - | UI | |
| **$R_{TX}$** | Differential Resistance | 80 | 100 | 120 | ohm | |
| **$C_{TX}$** | AC Coupling Capacitor | 80 | 100 | 120 | nF | |



## HSGMII (3.125G) - Differential Receiver Timing

| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| **UI** | Unit Interval | 319.96 | 320 | 320.04 | ps | Mean value |
| **T_X1** | Eye Mask | - | - | 0.3 | UI | |
| **T_Y1** | Eye Mask | 100 | - | - | mV | |
| **T_Y2** | Eye Mask | - | - | 600 | mV | |
| **$V_{RX-DIFFp-p}$** | Input Diff Voltage | 200 | - | 1200 | mV | Vp-p |
| **$T_{RX-EYE}$** | Minimum TX Eye Width | 0.4 | - | - | UI | |
| **$T_{RX-JITTER}$** | Output Jitter | - | - | 0.6 | UI | |
| **$R_{RX}$** | Differential Resistance | 80 | 100 | 120 | ohm | |



## 6 MT7981 Qualified Vendor List (QVL) Table

### 6.1 Introduction

This document describes the MT7981B qualified Crystals, DDRs and all types of flash memory that MT7981B SDK support. The DDR type is including DDR3(x16), DDR4 (x16). The Flash type is including Serial NOR, SPIM-NAND, SNFI NAND flash memory and eMMC. Customers are strongly recommended to design in with those parts that have been qualified by MTK.

### 6.2 Crystal

MT7981 support 40MHz, CL=10pF DIP and SMD crystal, QVL table as below:
TBD

| Vendor | Part Number | Package |
|---|---|---|
| TAS-SAW | TZ3451D | 3225 |
| SIWARD | XTL571150-M118-161 | |
| YOKETAN | S32A-040000-T10-HSN-1AMKA | |

**Table 6-1 Crystal QVL Table**

The table below lists the requirement for the XTAL.

| Item | Spec. |
|---|---|
| Nominal Frequency | 40MHz |
| Size | 3.2mmx2.5mm |
| Operating Temperature Range | -40°C to +105°C |
| Frequency Tolerance (FL) | +/- 7 ppm @ 25°C +/- 3°C |
| Frequency Stability over Operating Temperature | +/- 15 ppm (referred to the value at 25°C) -40°C to +100°C<br>+/- 20 ppm (referred to the value at 25°C) 100°C to +105°C |
| Equivalent Series Resistance (ESR) | 15 Ω max. |
| Drive Level(DL) | 400uW max |
| Shunt Capacitance (Co) | 3.0 pF max |
| Load Capacitance (CL) | 10 pF |
| Trim Sensitivity Over Load(Ts) | 10~13 ppm/pF |

**Table 6-2： XTAL oscillator requirement**

### 6.3 Serial NOR Flash memory (3.3V only)

| Vendor | Part Number | Density | Package |
|---|---|---|---|
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**Table 6-3 SPI Nor Flash QVL Table**

### 6.4 SFNI Flash (3.3V only)

MT7981 support 4~12bits ECC algorithm, the ECC algorithm selection is depended on spare area size per 512 byte sector,.

| Page size | Spare area size | ECC algorithm |
|---|---|---|
| 2048 bytes | 64 bytes | 4-bits ECC |
| 2048 bytes | 128 bytes | 12-bits ECC |

Before program Image by programmer, users should convert image files by **MTK BCH tool**, please reference to the Readme for bch tool usage.

Reference programmer:
Dediprog http://www.dediprog.com/

| Vendor | Part Number | Density | Page Size | Spare Area |
|---|---|---|---|---|
| | | | | |
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**Table 6-4 SPI-NAND QVL Table**

### 6.5 SPIM-NAND Flash (3.3V only)

MT7981 support Flash ECC, the ECC algorithm depended on flash.

| Page size | Spare area size | ECC algorithm |
|---|---|---|
| 2048 bytes | 64 bytes | 4-bits ECC |
| 2048 bytes | 128 bytes | 12-bits ECC |

Before program Image by programmer, users should convert image files by **MTK BCH tool**, please reference to the Readme for bch tool usage.

Reference programmer:
Dediprog  http://www.dediprog.com/

| Vendor | Part Number | Density | Page Size | Spare Area |
|---|---|---|---|---|
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**Table 6-5 SPIM-NAND QVL Table**

## 6.6 eMMC Flash Memory (3.3V only)

MT7981B only support 3.3V eMMC NAND Flash memory, 8 bit data and compatible with eMMC 4.5 above. The QVL table as below:

| Vendor | Part Number | eMMC version | Package | Density |
|---|---|---|---|---|
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**Table 6-6 eMMC Flash QVL Table**

## 7 Disclaimer

# Proprietary Notice and Liability Disclaimer



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