MT7986A/B/C HW Design Notice

(Keywords: SCH, PCB, power, thermal, flash)

1 Document Revision History

No.	Description	Edited by	Checked by	Date of Approval
1.0	Initial	Steven Kuo	Gary Tsao	2021/08/13
1.1	1. Add SGMII and 2.5G PHY test command. 2. Update boot strapping, SPI description 3. change and Flash QVL (phase 1) 4. Add ePA power tree 5. Add MT7986C, MT7986A data.	Steven Kuo	Gary Tsao	2021/11/22
1.2	1. Update DDR3/DDR4 layout rule 2. update QVL	Steven Kuo	Gary Tsao	2021/12/28
1.3	1. 3-Wire coexist control pin update 2. WRI RC suggest 0R/4.7pF 3. eFEM 27dBm current consumption 4. Memory QVL update 5. MT7976A/DA/C pin 77 must NC 6. Update USB2.0 command 7. Add OSC/Xtal spec	Steven Kuo	Gary Tsao	2022/01/20
1.4	1. Modify typo 2. SPI-Quad IO Mode driver support, layout Notice (5.2.17) 3. Add section to suggest AIQ/SGMII/USB3/PCIe routing at inner layer for well shielding for RF emission and RX de-sense. (5.2.18)	Steven Kuo	Gary Tsao	2022/04/29

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2 Important Notice

For the performance consideration, the critical layout and components show, no-change & critical parts, please follow MTK QVL design.

1. AIQ/OSC/Crystal
2. DDR, layout, power trace and cap position
3. Flash
4. DVDD_CORE, DVDD_PROC_L (MT7986A) cap and position and DVDD_CORE_FB
5. The E-Cap/Inductor of the 3.3V Power supply out. Buck Must Force PWM mode for lower ripple.

3 Product Requirement Document (PRD)

The following table covers the main features offered by MT7986A/B/C datasheet.

Features	MT7986A	MT7986B/C
CPU	ARM CA53 (2.0GHz, Quad-core), NEON	ARM CA53 (1.6GHz, Quad-core), NEON
I-Cache, D-Cache	32kB, 32kB per core	32kB, 32kB per core
L2 Cache	512KB	512KB
Security	Secure boot Crypto Suite Anti Clone	Secure boot Crypto Suite Anti Clone
DRAM	16bit DDR3-2133 2Gb/4Gb 16bit DDR4-3200 8Gb/16Gb (4Gb Planning) 16bit DDR4-2666 4Gb/8Gb/16Gb Planning	16bit DDR3-2133 KGD **256MB(MT7986BS)/512MB(MT7986BL)** SIP **256MB(MT7986CS)/512MB(MT7986CL)** SIP
WIFI	Lead in 4x4+4x4 WIFI6E FEM integration Airtime Fairness Spectrum Analyzer	MT7986B: 4x4+4x4 WIFI6E FEM integration MT7986C: 2x2+3x3 WIFI6E FEM integration Airtime Fairness Spectrum Analyzer
Ethernet	(H)SGMII x 2	(H)SGMII x 2
HW QoS	128 hardware queues SFQ w/ 1k queues. Seamlessly co-work with HW NAT engine.	64 HW queues, FQ w/ 1K queues Seamlessly co-work with HW NAT engine.
WIFI HNAT	Ethernet /WiFi Wired speed IPv4 Routing, NAT, NAPT IPv6 routing, DS-lite, 6RD, 6to4	Ethernet /WiFi Wired speed IPv4 Routing, NAT, NAPT IPv6 routing, DS-lite, 6RD, 6to4
USB	(USB3.0 host+USB2.0 host) x 1 +USB2.0 Hostx1	(USB3.0 host+USB2.0 host) x 1
PCIe	PCIe2.0 2L	No
eMMC	eMMC5.1 (CLK 104MHz), max 16GB(QVL)	eMMC4.5 share w/ SPI0, SPI1, PWM1,
SPIM Flash (NOR/NAND)	1 (max 52MHz) data bit width x1/x2/x4 Support 4-byte address mode compatible with 3-byte address mode	1 (max 52MHz) data bit width x1/x2/x4 Support 4-byte address mode compatible with 3-byte address mode
I2C	1	1
PCM	1	No
UART	1* UART-Lite(2-pins) , 2* 4-pin UART	1* UART-Lite(2-pins), 2*4-pin UART(share pin)
BT/ZigBee coexist	Yes, support 3rd part BT/Zigbee by USB/Uart and 3 wire coexist.	No
Package	VFBGA (16.85 x 16.85 x 0.9 mm)	FCCSP 13.6 x 13.6 mm

Table 3-1 : MT7986 main feature list

4 MT7986 RFB Board

4.1 MT7986 SKU and chip solution

SKU table and chip solution for your reference. Any issue, please contact MTK sales first.
NO 2.4G iFEM+5G eFEM or 2.4G eFEM+5G iFEM mix mode, Must 2.4G/5G iFEM or 2.4G/5G eFEM.

SKU	(2+3) AX4200	(2+3) AX4200	(4+4) AX6000	(4+4) AX6000	(2+3) AX4200	(2+3) AX4200	(4+4) AX6000	(4+4) AX6000	(2+4+2) AX7800	(4+4+4) AX8400
CPU	MT7986C	MT7986C	MT7986B	MT7986B	MT7986A	MT7986A	MT7986A	MT7986A	MT7986A	MT7986A
2.4G	MT7976C	MT7976DA	MT7975N	MT7976G	MT7976C	MT7976DA	MT7975N	MT7976G	-	MT7976G
5/6G			MT7975P	MT7976A			MT7975P	MT7976A	MT7976A (5G)	MT7976A (6G)
FEM	iFEM	eFEM	iFEM	eFEM	iFEM	eFEM	iFEM	eFEM	eFEM	eFEM
DRAM	KGD	KGD	KGD	KGD	External DDR3 DDR4	External DDR3 DDR4	External DDR3 DDR4	External DDR3 DDR4	External DDR3 DDR4	External DDR3 DDR4
PCIe	No	No	No	No	PCIe 2Lx1	PCIe 2Lx1	PCIe 2Lx1	PCIe 2Lx1	PCIe 2Lx1 MT7916 (2G+6G)	PCIe 2Lx1 MT7915 (5G, BW80)

Note, AX4200/AX7800 only use one A die, if use one A die, AFE0_XIN_WBG and AFE1_XIN_WBG must wire together.

Table 4-1 : SKU and chip solution

When power-on calibration, the connectors of antenna need terminated by 50 ohm loading.

Fig 4-1: MT7986A+MT7986C RFB Top view

5 Hardware Design Kit (HDK)

This application note records the details of MT7986 HW settings. Compared to the MT7986 datasheet, this supplement document is conveniently used during customer board level bring-up.

5.1.1 16bit DDR3 DRAM

MT7986B/C DDR3 embedded or MT7986A use DDR3, the EMI_EXTR resistor is 40.2 ohm/1% and the DRAM ZQ resistor is 240 ohm/1%.

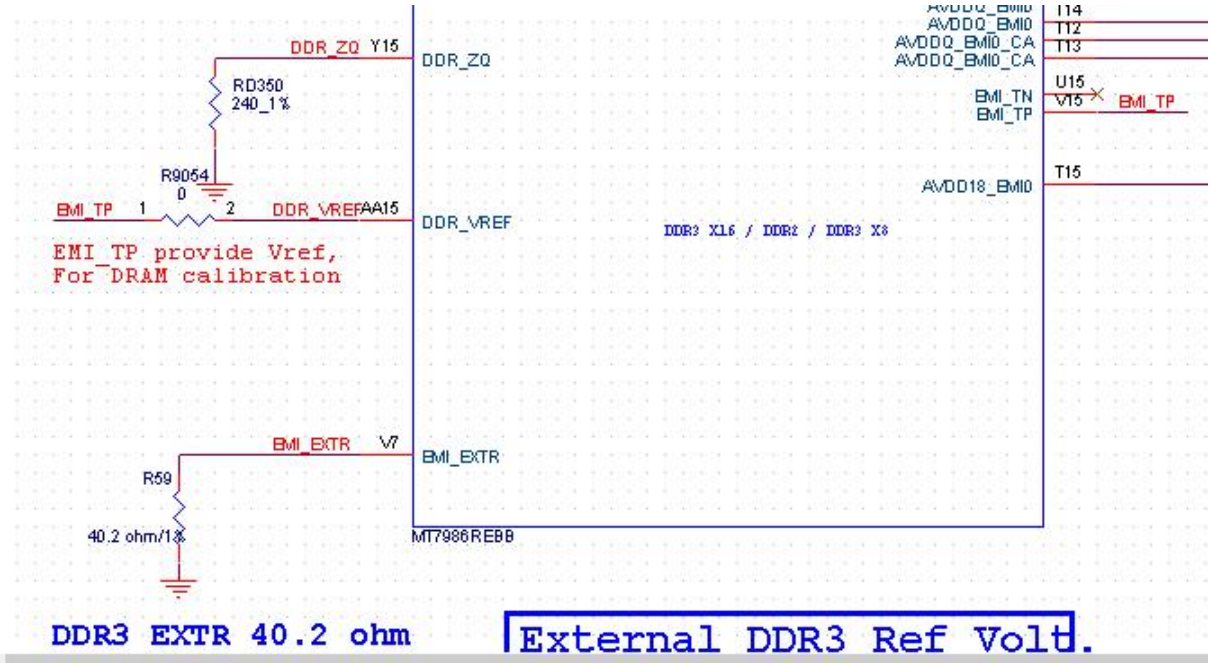


Fig 5-1 : The DRAM reference registers

DDR_VREF connect to EMI_TP for DRAM calibration, and it also needs to reserve 0.1uF/10K1% for Vref and as voltage divider.

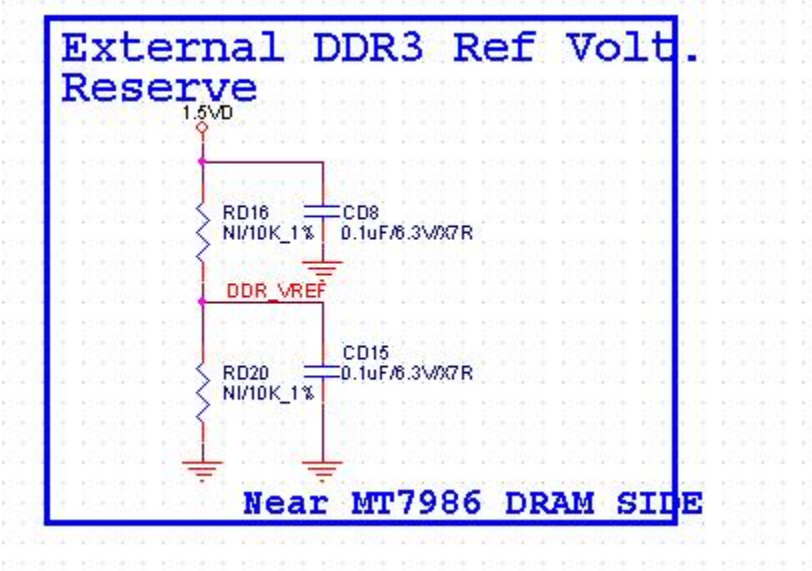


Fig 5-2 : The capacitors of DRAM VREF

MT7986A DDR3 and DDR4 are share pin, if DRAM is DDR3, please use DDR3 pin name. And AVDDQ_EMI0_XX change to 1.5VD, AVDD15_POR change to 1.5VD.

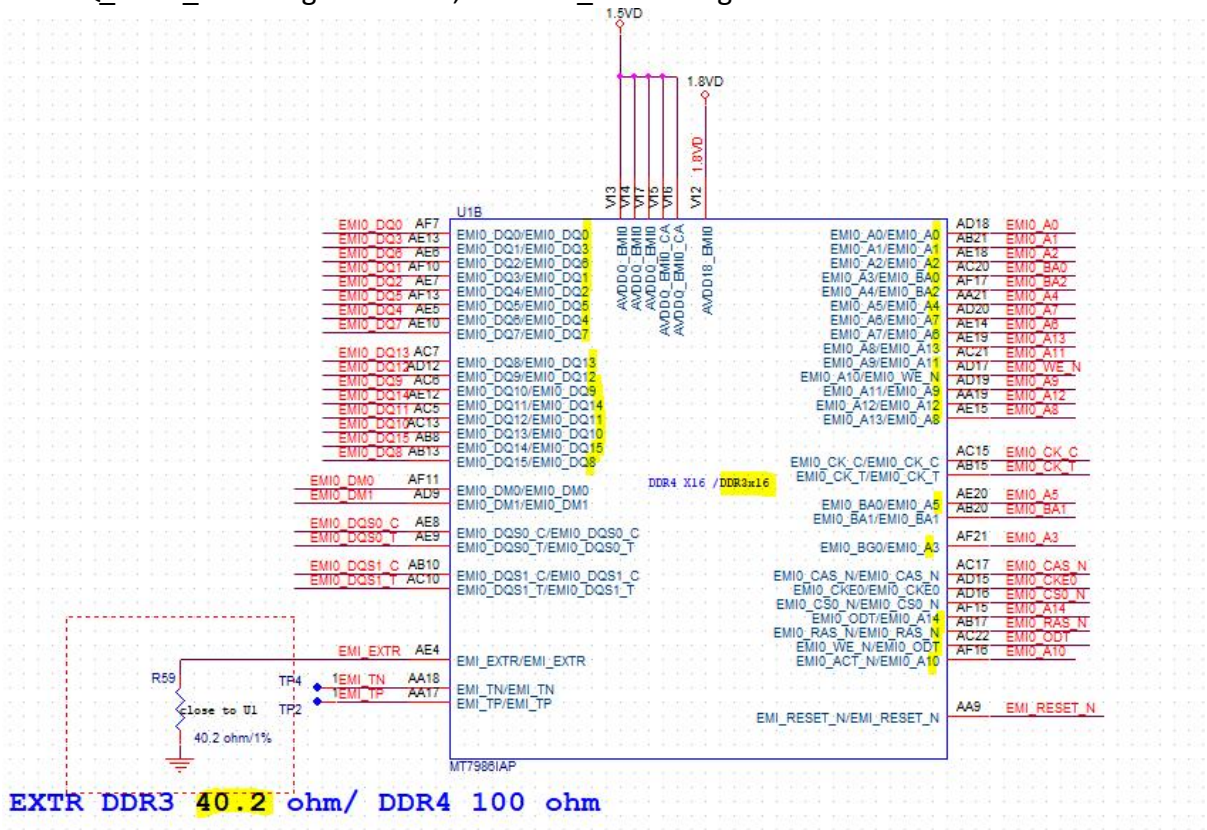


Fig 5-3 : DDR3 pin mux

5.1.2 16bit DDR4 DRAM

MT7986A support DDR4-3200, the EMI_EXTR resistor is 100 ohm/1%. So far DDR4 only support 16bit. Please don't use 8-bitx2 for schematic design.

DDR4 DRAM use 1.2V and 2.5V (VPP), DRAM datasheet/JEDEC standard mention 1.2V should behind 2.5V (VPP). Check some QVL DRAM datasheet, 2.5V (VPP) max current(IPP) around 20~30mA, MTK share AVDD12 (AFE 33mA, USB2 5mA, CKSQ 0.15mA), DRAM AVDDQ_EMI DDR4-3200 238mA. DRAM datasheet max current 363mA, 1.2V total 639mA

Below data is real measurement data 1.2V w/ micron DDR4-3200 8Gb at Normal temperature.

Current measurement point @DC to DC out (include DDR4 I/F+DDR4 chip + AFE + U2 + CLKSQ)
Default, mean current 37mA
Memtest 10M 1 time, 1core 100% busy, mean current 163mA
Memtest 10M 2 time, 2core 100% busy, mean current 223mA
Memtest 10M 3 time, 3core 100%, busy, mean current 250mA
Memtest 10M 4 time, 4core 100%, busy, mean current 272mA, current probe max current 384mA (peak), for high temperature, we suggest use 800mA or 1A LDO for 1.2V design.

NANYA

NTC Proprietary
Level: Property

DDR4-8Gb C-Die
NT5AD1024M8C3/NT5AD512M16C4

Symbol	Description	DDR4-2666		DDR4-3200		Unit
		X8	X16	X8	X16	
I_{DD4W}	Operating Burst Write Current	208	266	253	316	mA
I_{DD4WA}	Operating Burst Write Current (AL=CL-1)	217	275	264	326	mA
I_{DD4WB}	Operating Burst Write Current with Write DBI	209	267	255	317	mA
I_{DD4WC}	Operating Burst Write Current with Write CRC	224	291	275	363	mA

Fig 5-4 : DDR4 RAM 1.2V max current

5.1.3 USB2/3 design

USB2_1 is used for USB3 connector, USB2.0 U2_1 AVDD12_USB need to reserve 0-ohm resistor to prevent USB2.0 power noise to interference AFE, if AFE reserve already, don't need to reserve.

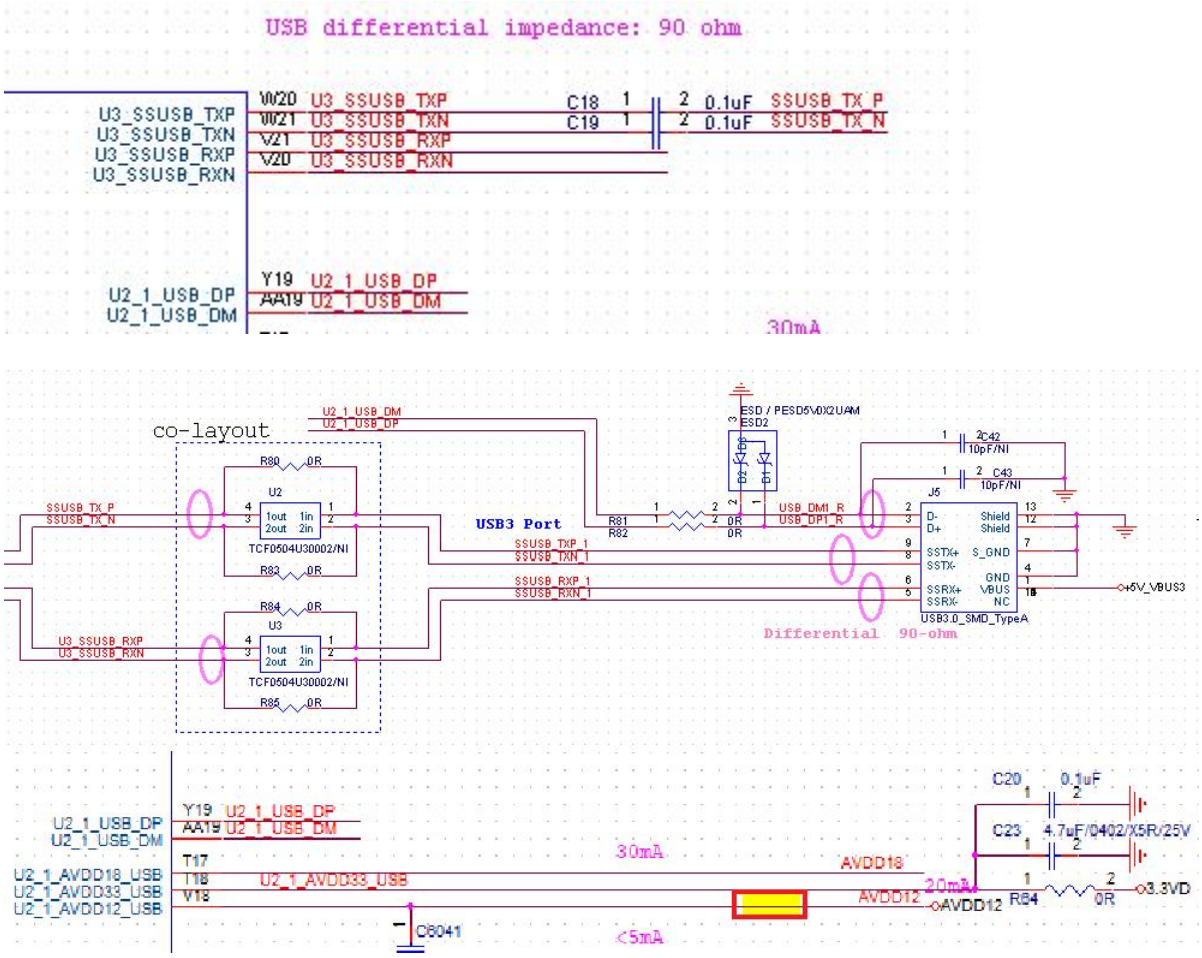


Fig 5-5 : USB2_1/USB3

5.1.4 HSGMII schematic design

For ordinary HW configuration, HSGMII SG0 must wire to MT7531Port 6, HSGMII SG1 wire to MT7531A Port 5. If only one 2.5G PHY, the 2.5G PHY must wire to HSGMII SG1. MT7986 RFB SG0/SG1 default is force link up at 2.5G for MT7531A or 2.5G PHY.

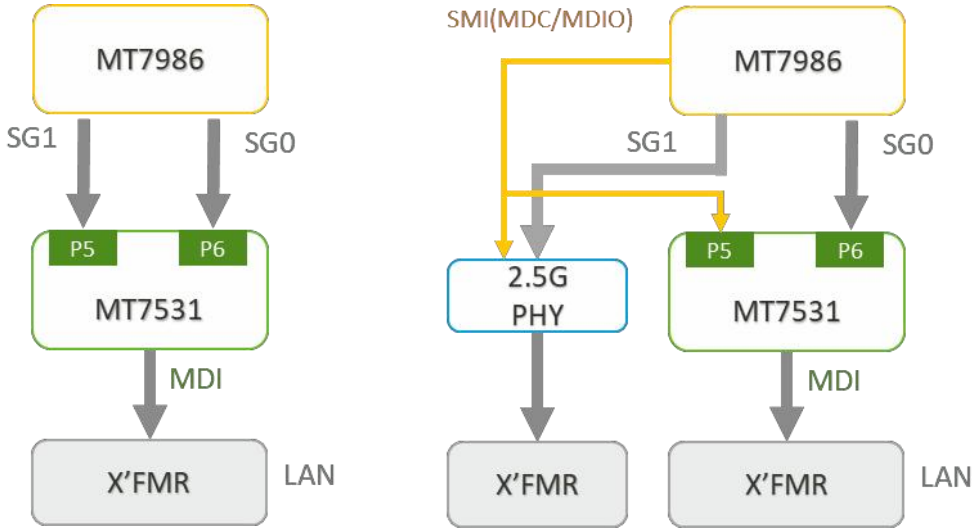


Fig 5-6 : Giga Switch or one 2.5G PHY

If using two 2.5G PHY, HSGMII SG0 must connect to MT7531Port 6, SG1 connect to 2.5G PHY (address 6), MT7531 Port 5 SGMII connect to 2.5G PHY (address 5). Two 2.5G PHY MDC/MDIO control by MT7986, **if customer use non-HDK 2.5G PHY, please reserve PHY interrupt for 2.5G PHY.**

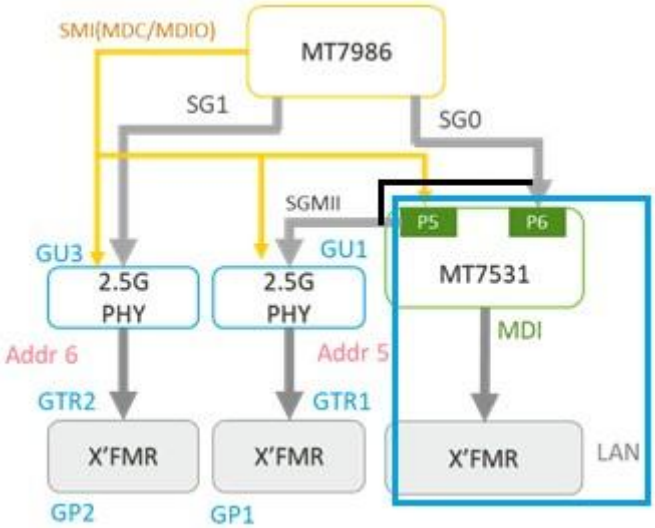


Fig 5-7 : Two 2.5Gbps PHY

If using two 1G ports, Suggest HSGMII SG0/1 must connect to MT7531Port 6/5. Don't suggest to use two single 1G PHY.

5.1.5 PCIe 2.0 2 Lane design

MT7986A support PCIe 2.0 2 lane design

5.1.6 Power cap list

Table 5-1 shows the de-coupling cap values of the power trace. The placement guidelines follow basic rules small capacitors close to MT7986B main chip and the large capacitors are closer to power source.

Pin name	0.85V/AVDD18/AVDD12/AVDD09 de-couping cap value
DVDD_CORE	0.85V/8.24A (0201 1uF*16)
AFE	AFE0_AVDD18_WBG cap value:0.1uF+1uF AFE1_AVDD18_WBG cap value:0.1uF+1uF AFE0_AVDD12_WBG cap value:0.1uF+1uF AFE1_AVDD12_WBG cap value:0.1uF+1uF
BG_OUT	1uF
REFP	1uF
VQPS	1.8VD 0.1uF+1uF
USB30	U3_AVDD09_SSUSB cap :0.1uF+1uF U3_AVDD18_SSUSB cap :0.1uF+1uF
USB2	AVDD18 cap :0.1uF+1uF (share u3, work for u3 or u2) AVDD12 cap 0.1uF AVDD33 cap 0.1uF+4.7uF
(H)SGMII	SG0_AVDD09_SSUSB cap :0.1uF+1uF SG1_AVDD09_SSUSB cap :0.1uF+1uF SG0_AVDD18_SSUSB cap :0.1uF+1uF SG1_AVDD18_SSUSB cap :0.1uF+1uF
DRAM	DDR_VDDQ(1.5VD) cap:0201 0.1uF*5
DRAM controller	AVDDQ_EMI0/ AVDDQ_EMI0_CA (1.5V) Cap: 0201 0.1uF*8 (Top) + 0201 0.1uF *8 (Bottom) AVDD18_EMI0 cap: 0.1uF+1uF

Table 5-1 : Power cap list

5.1.6.1 U3/HSGMII Power cap

Please follow HDK to add USB3.0/HSGMII cap 0.1uF+1uF for each power pin.

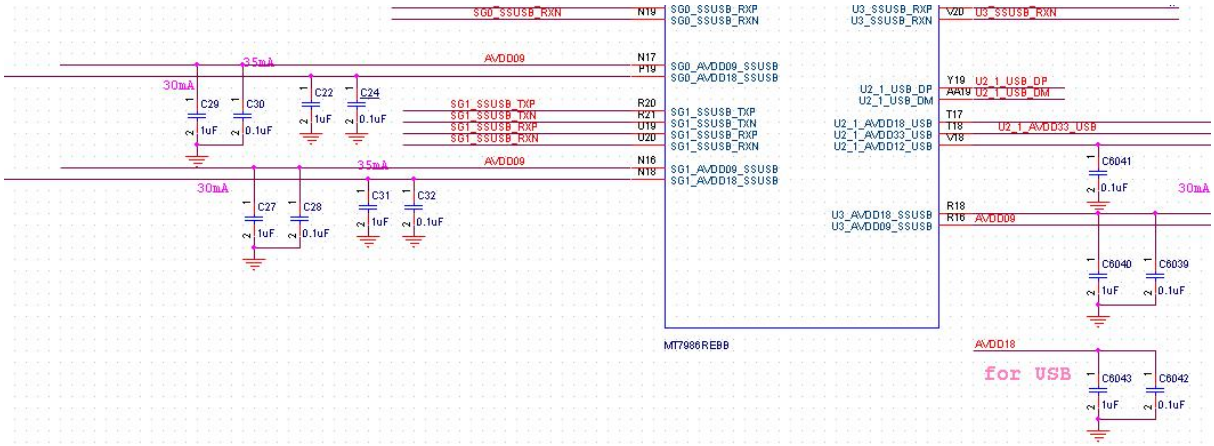


Fig 5-8 : U3+HSGMII Power caps

5.1.6.2 MT7986B/C DRAM Power Caps

Please follow HDK to add SOC_DDR Controller Caps: 0201 *8 (Top) + 0201 *8 (Bottom)
For KGD Dram: 0201 *5

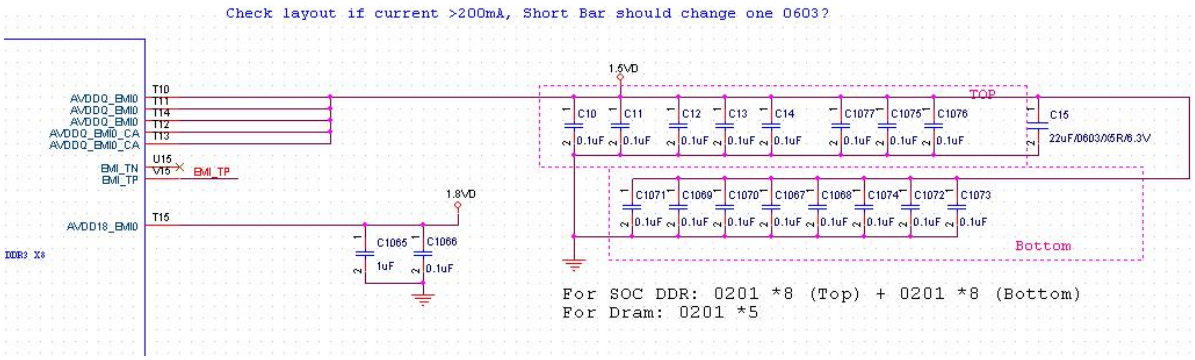


Fig 5-9 : MT7986B/C DRAM controller Power Cap

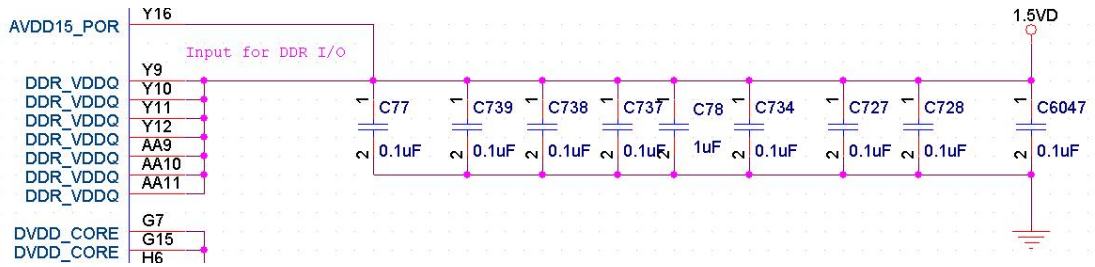


Fig 5-10: MT7986B/C DRAM KGD Power Cap

5.1.6.3 MT7986B/C DVDD_CORE Power cap

Please follow HDK to add DVDD_CORE 1uF*16 for power pin.

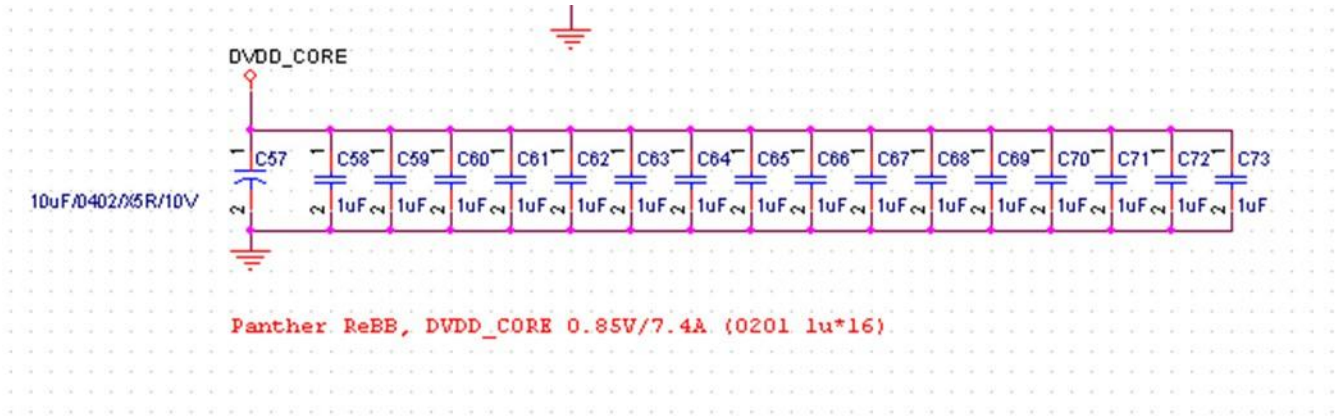


Fig 5-11: MT7986B/C DVDD_CORE Power caps

5.1.6.4 MT7986A DVDD_CORE and DVDD_PROC_L Power cap

Please MUST follow HDK layout use 0201 1uF *10 for DVDD_CORE and use 0201 1uF *8 for DVDD_PROC_L.

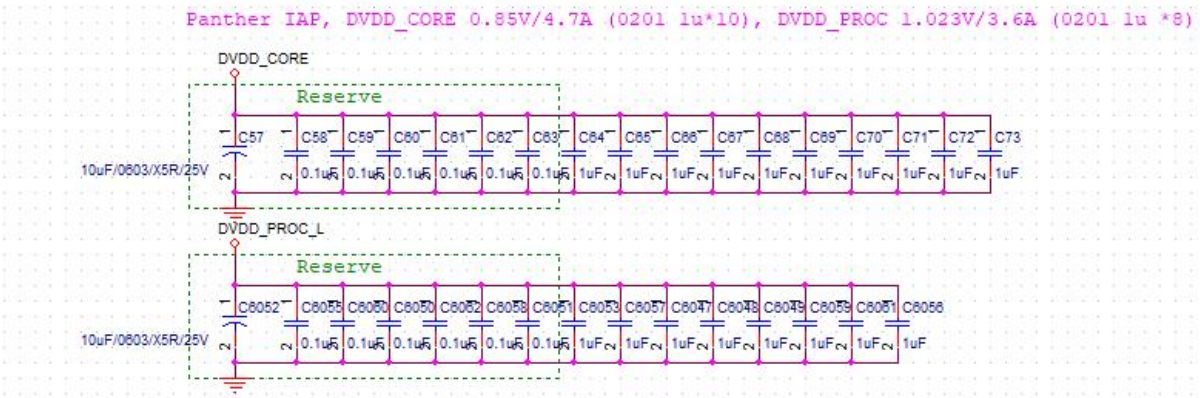


Fig 5-12: MT7986A DVDD_CORE and DVDD_PROC_L Power caps

5.1.7 Power Plan

5.1.7.1 MT7986B+MT7975x2 AX6000 Power Plan (example)

Fig 5-13, the power tree is not for thermal simulation, it only for DC-to-DC regulator selection. The max power consumption calculates for RX and TX at same time, for power

adaptor selection, please refer TX max current. (Note: TX and RX can't work at same time.)

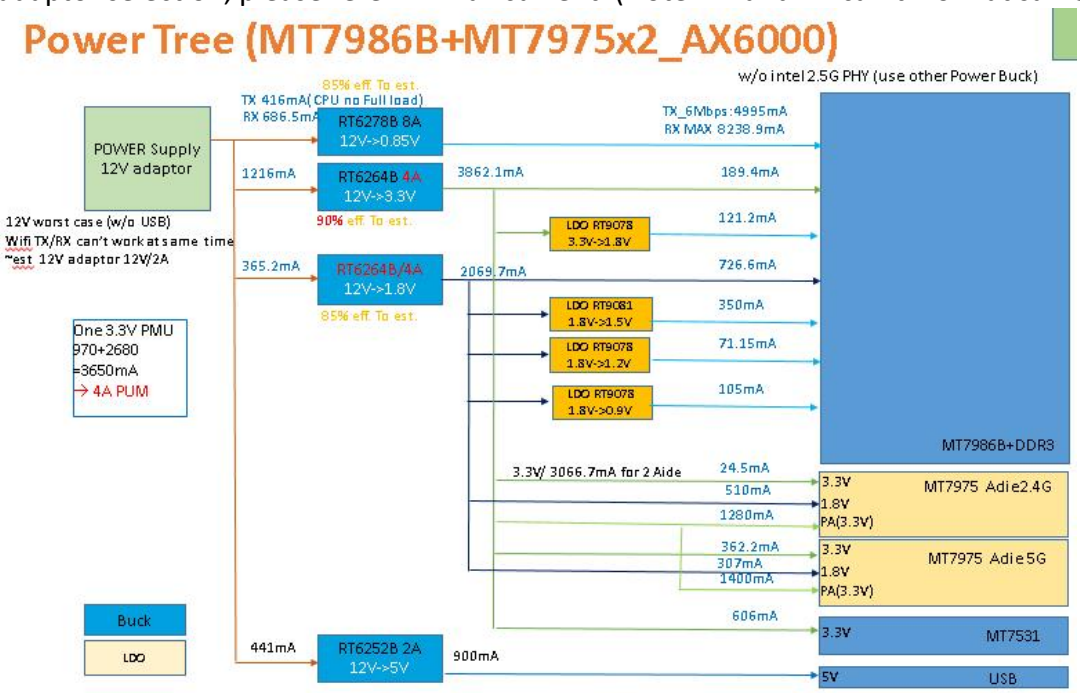


Fig 5-13: MT7986B + MT7975 power plan (example)

5.1.7.2 MT7986B+MT7976x2+ eFEM AX6000 Power Plan (example)

Fig 5-14, the power tree is not for thermal simulation, it only for DC-to-DC regulator selection. The max power consumption calculates for RX and TX at same time, for power adaptor selection, please refer TX max current. (Note: TX and RX can't work at same time.), 5V FEM buck depend on FEM and TX power, If WIFI TX max is 27dBm suggest using 5V/5A.

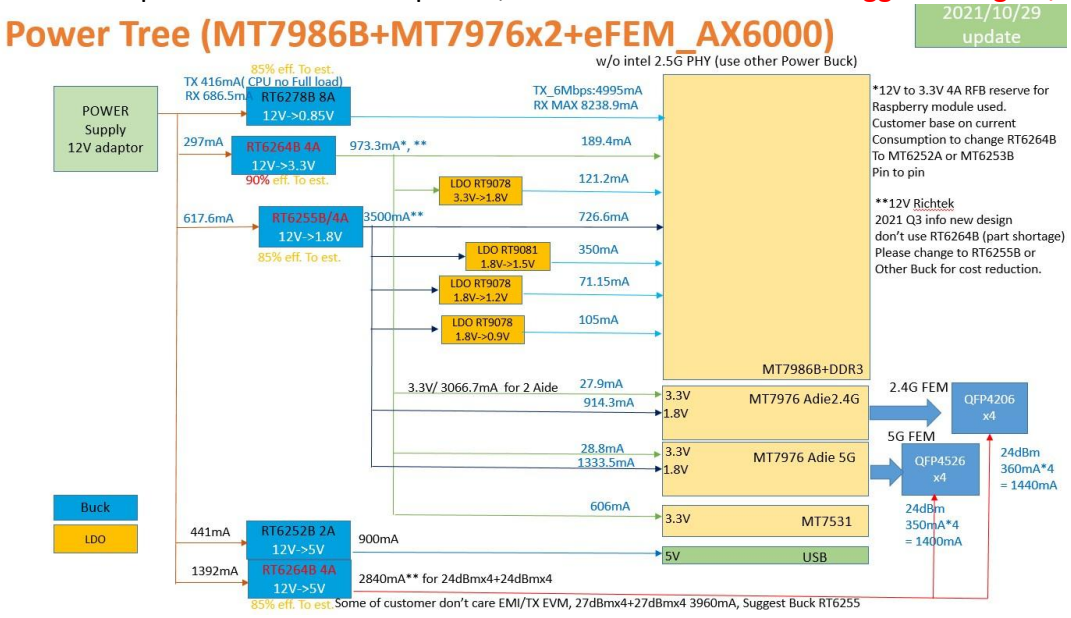


Fig 5-14: MT7986B + MT7976+eFEM power plan (example)

5.1.7.3 MT7986C+MT7976DA+ eFEM AX4200 Power Plan (example)

Fig 5-15, the power tree is not for thermal simulation, it only for DC-to-DC regulator selection. The max power consumption calculates for RX and TX at same time, for power adaptor selection, please refer TX max current. (Note: TX and RX can't work at same time.)
Fig 5-15 FEM power is 23~24dBm, if FEM TX power is >25dBm, please change FEM power to 5V/3A or 4A.

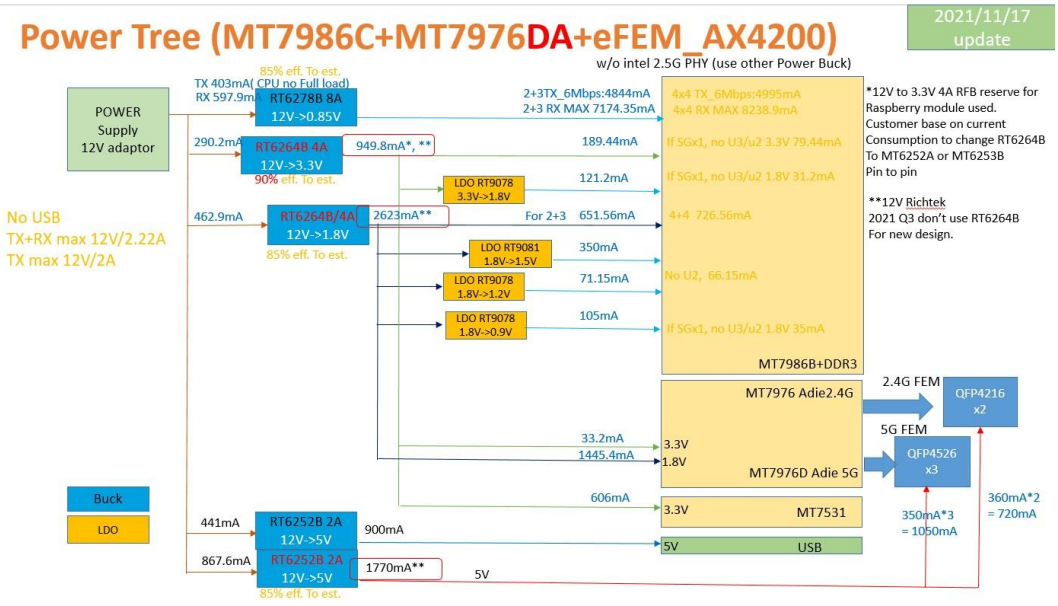


Fig 5-15: MT7986B + MT7976DA+eFEM power plan (example)

5.1.7.4 MT7986C+MT7976C AX4200 Power Plan (example)

Fig 5-16, the power tree is not for thermal simulation, it is only for DC to DC regulator selection. The max power consumption calculate for RX and TX at same time, for power adaptor selection, please refer TX max current. (Note: TX and RX can't work at same time.)

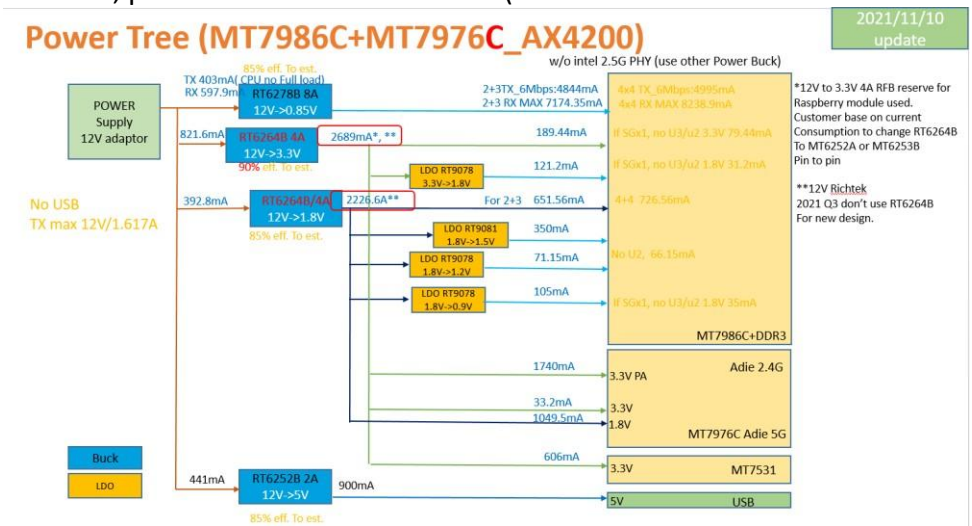


Fig 5-16: MT7986B + MT7976C power plan (example)

5.1.7.5 MT7986A+MT7976x2+ eFEM AX6000 Power Plan (example)

Fig 5-17 DC to DC power for reference only, DC to DC depend on max current. FEM buck suggests 5V/5A, if TX power maybe > 26dBm.

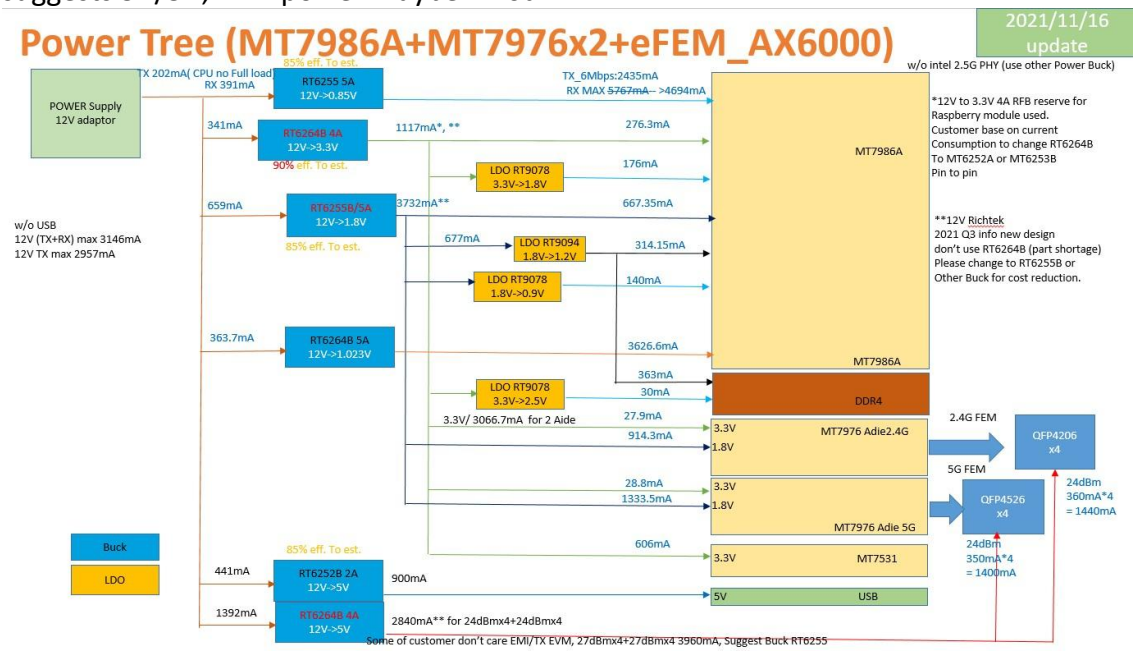


Fig 5-17: MT7986A + MT7976x2+eFEM power plan (example)

5.1.7.6 MT7986A+MT7976C AX4200 Power Plan (example)

Fig 5-18 for DC to DC power regulator design reference only.

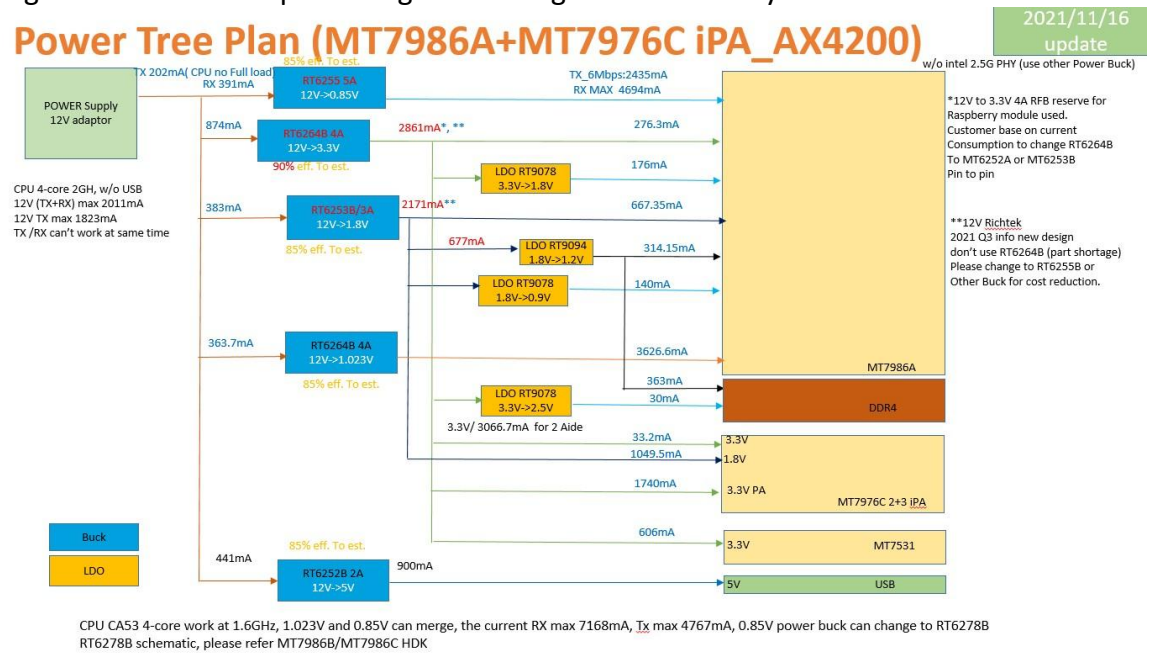


Fig 5-18: MT7986A + MT7976C power plan (example)

5.1.7.7 MT7986A+MT7976C AX4200 Power Plan (example)

Fig 5-19 MT7986A AX4200 ePA DC to DC power regulator for reference only. FEM TX Power 26~27dBm, suggest change FEM busk to 5V/3A or 4A.

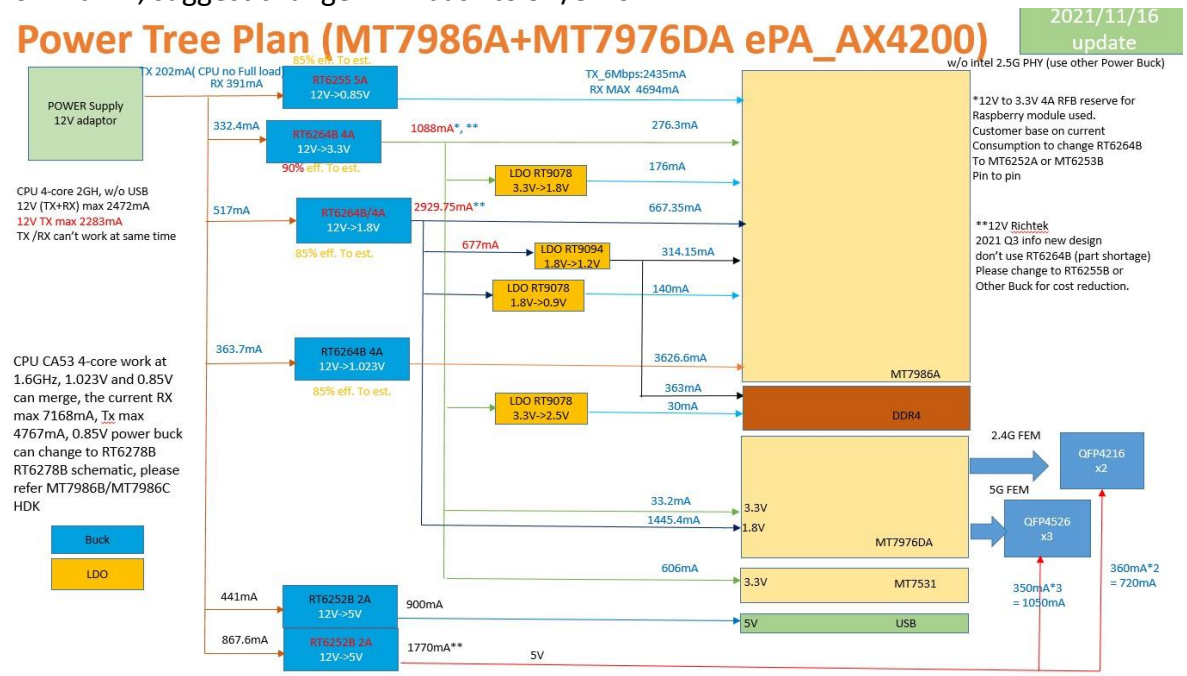
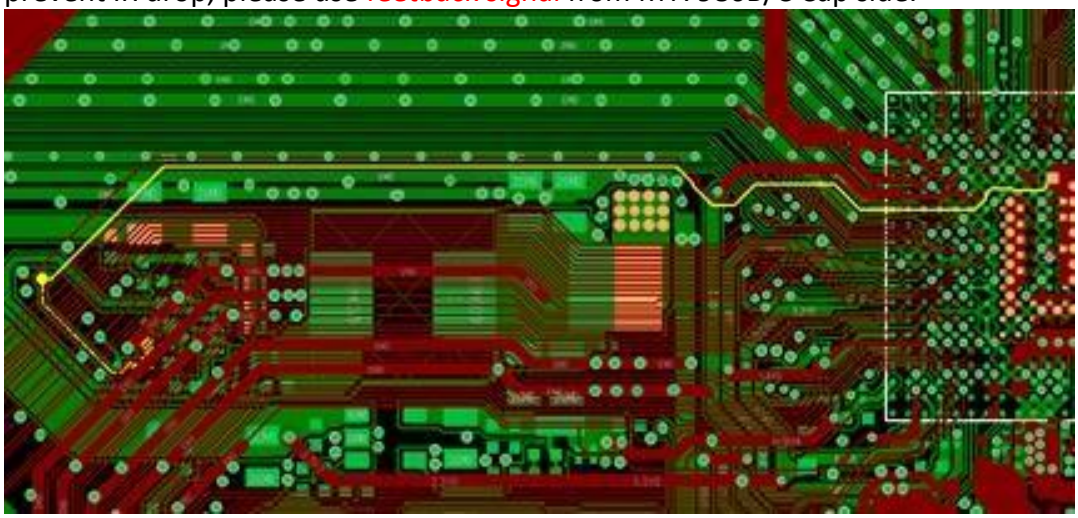


Fig 5-19: MT7986A + MT7976DA power plan (example)

5.1.8 MT7986B/C Core powers

This section simply describes RT6278. For detail layout notice, please refer to RT6278 datasheet.

0.85V worst case is 8.24A for MT7986B, and 7.17A for MT7986C, the IR drop need <6%, to prevent IR drop, please use feetback signal from MT7986B/C Cap side.



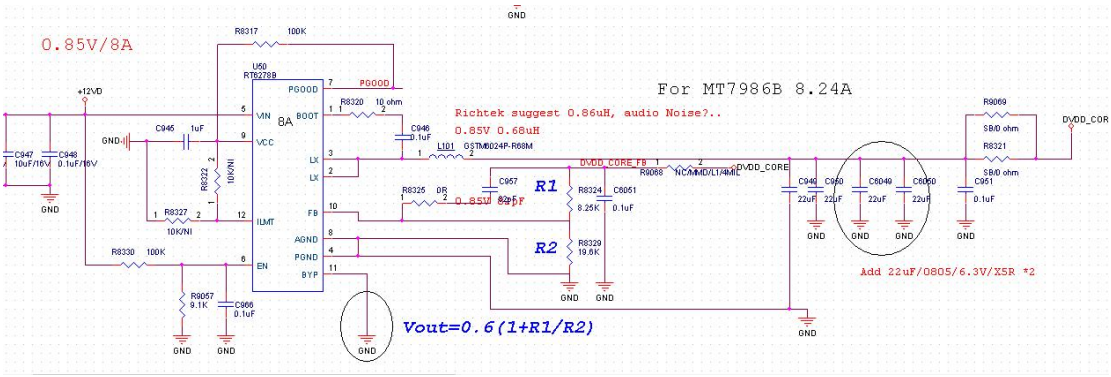


Fig 5-20: RT6278 FB pin

MT7986B+MT7975x2 RC delay for your reference in Table 5-2 (Please check datasheet for Power on sequence design)

Type	PN	Input	Output	Current(mA)	Enable pin	RC delay	Delay time
BUCK	RT6252/2A	12	5	900	12V	X	
BUCK	RT6264/4A	12	3.3	3862	12V	X	
BUCK	RT6278B	12	0.85	8238	12V	R/C=100K/9.1K/0.1uF	1ms
BUCK	RT6264/2A	12	1.8	2069	12V	R/C=100K/20K/0.22uF	2.7ms
LDO	RT9078N-08(adj.)	1.8	0.9	120	1.8V	R/C=68K/91K/100nF	3.13ms
LDO	RT9078-12GJ5/GQZ	1.8	1.2	70	1.8V	R/C=68K/91K/100nF	3.13ms
LDO	RT9078-18GJ5/GQZ	3.3	1.8VA	180	1.8V	R/C=68K/91K/100nF	3.5ms
LDO-DDR3	RT9081 (500mA)	1.8	1.5	350	1.8V	R/C=68K/91K/150nF	8ms

Table 5-2 : MT7986B+MT7975 RC delay

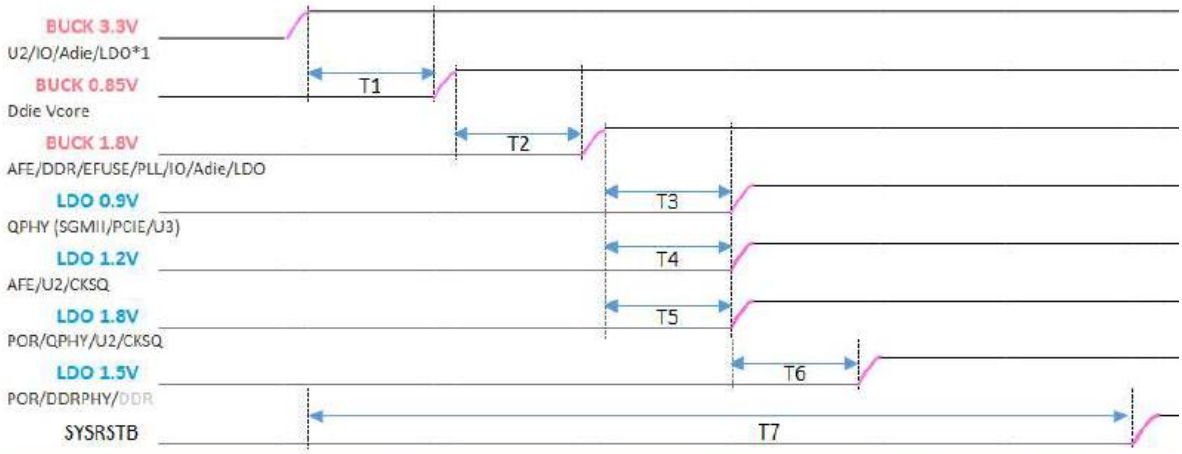
5.1.9 MT7986A DVDD_CORE (0.85V) and DVDD_PROC_L (1.023V) powers

MT7986B/C CPU and WiFi Core use the same voltage 0.85V(Substrate tie together), but MT7986A separate two voltage for WIFI core power(DVDD_CORE) 0.85V/4.69A and ARM CA53 CPU Core power volate(DVDD_PROC_L) 1.023V/3.63A.

5.1.10 Power on sequence

5.1.10.1 MT7986B/C power on sequence

Fig 5-19: it calculate delay time by RC (Table 5-2). The timing is only for reference, the power on sequence MUST follow datasheet to design.
LDO 1.5V must delay at least 3ms than 1.8V (LDO 1.8V), if 1.5V only delay 0~3 ms than LDO 1.8V, MUST wire AVDD18_POR to Buck 1.8V. AVDD18_POR can connect to Buck 1.8V.



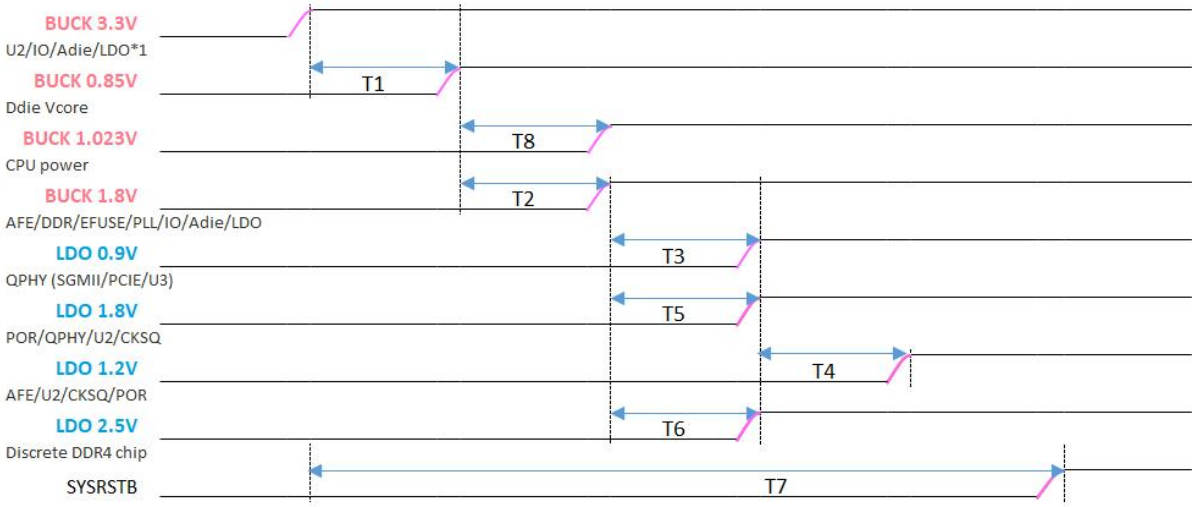
Symbol	Description	Min	Max	Unit
T1	BUCK_3.3V to BUCK_0.85V	0.5	5	ms
T2	BUCK_0.85V to BUCK_1.8V	0.5	5	ms
T3	BUCK_1.8V to LDO_0.9V	2	6	ms
T4	BUCK_1.8V to LDO_1.2V	2	6	ms
T5	BUCK_1.8V to LDO_1.8V	2	6	ms
T6	LDO_1.8V to LDO_1.5V	3	8	ms
T7	BUCK_3.3V to SYSRSTB release	35	-	ms

Fig 5-21: MT7986B/C power on sequence

5.1.10.2 MT7986A w/DDR4 power on sequence

Fig 5-20: RFB calculate delay time by RC. The timing is only for reference, the power on sequence MUST follow datasheet to design.

LDO 1.2V must delay at least 3ms than 1.8V (LDO 1.8V), if 1.2V only delay 0~3 ms than LDO 1.8V, MUST wire AVDD18_POR to Buck 1.8V. AVDD18_POR can connect to Buck 1.8V.



Symbol	Description	Min	Max	Unit
T1	BUCK_3.3V to BUCK_0.85V	0.5	5	ms
T2	BUCK_0.85V to BUCK_1.8V	0.5	5	ms
T8	BUCK_0.85V to BUCK_1.023V	0.5	5	ms
T3	BUCK_1.8V to LDO_0.9V	2	6	ms
T4	LDO_1.8V to LDO_1.2V	3	8	ms
T5	BUCK_1.8V to LDO_1.8V	2	6	ms
T6	BUCK_1.8V to LDO_2.5V	2	6	ms
T7	BUCK_3.3V to SYSRSTB release	35	-	ms

Fig 5-22: MT7986A power on sequence

5.1.10.3 MT7986A w/DDR3 power on sequence

MT7986Aw/ DDR3 power on sequence can check MT7986B when CPU work at 1.6G(DVDD_PROC 0.85V).
If CPU work at 2.0G, DVDD_PROC_L MUST be 1.023V. 1.023V power on sequence timing, please refer 5.1.10.2 T8 timing.

5.1.11 Reset

Fig 5-23: Reset circuit For MT7986 SYSRSTB, Pin V16 (RSTB) is output signal to reset A-die. TESTMODE should be Low for normal mode.
MT7531 and 2.5G PHY reset control by software, use GPIO_0 and GPIO1. It doesn't need to meet power on reset timing.

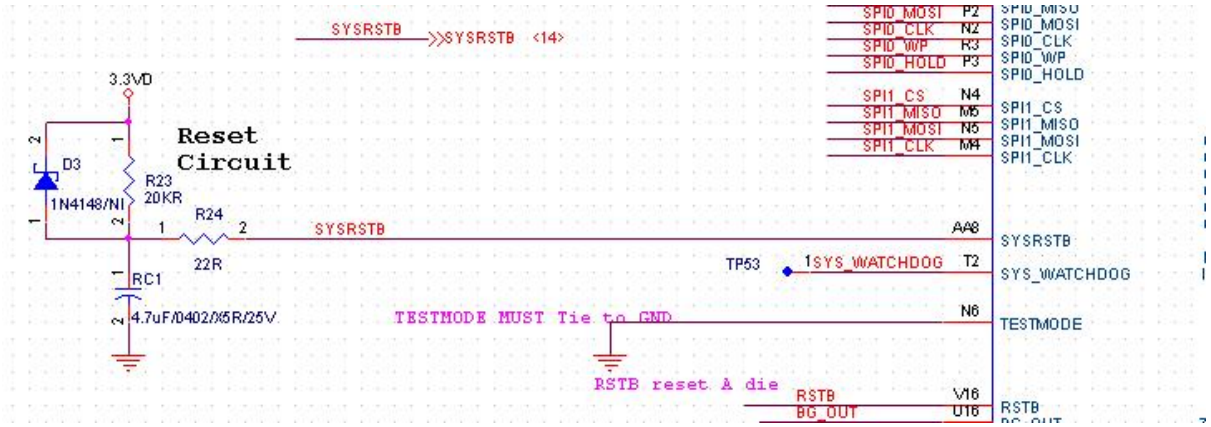


Fig 5-23: Reset circuit

5.1.12 HDK GPIO definition

Ball name	Func.0	Func.1	Bootstrap	RFB GPIO definition	2x13 Raspberry
SYS_WATCHDOG	B:GPIO0	O:SYS_WATCHDOG			2x13 pin 15
WF2G_LED	B:GPIO1	O:WF2G_LED		WF2G LED low active	
WF5G_LED	B:GPIO2	O:WF5G_LED		WF2G LED low active	
I2C_SCL	B:GPIO3	B:I2C_SCL		EVB I2C EEPROM	2x13 pin 5
I2C_SDA	B:GPIO4	B:I2C_SDA		EVB I2C EEPROM	2x13 pin 3
GPIO_0	B:GPIO5	B:PCIE_PHY_I2C_SCL	{GPIO_1,GPIO_0} 00: SPIM-NOR (SPI2) 01: SPIM-NAND (SPI2) 10: eMMC (PWM.SPI0/1) 11: Reserve	GbE_RESET	
GPIO_1	B:GPIO6	B:PCIE_PHY_I2C_SDA	{GPIO_1,GPIO_0}	2.5G PHY Reset	
GPIO_2	B:GPIO7	O:DRV_VBUS			2x13 pin 13
GPIO_3	B:GPIO8	O:DRV_VBUS_1P	0: 2 A-Die/1 Adie SB 1: reserve		2x13 pin 11
GPIO_4	B:GPIO9	B:PCIE_CLK_REQ		RST_PBC	
GPIO_5	B:GPIO10	I:PCIE_WAKE_N		WPS_PBC	
GPIO_6	B:GPIO11	O:JTAG_JTDO		JTAG_JTDO	

GPIO_7	B:GPIO12	I:JTAG_JTDI		JTAG_JTDI	
GPIO_8	B:GPIO13	B:JTAG_JTMS		JTAG_JTMS	
GPIO_9	B:GPIO14	I:JTAG_JTCLK		I:JTAG_JTCLK	
GPIO_10	B:GPIO15	I:JTAG_JTRST_N		I:JTAG_JTRST_N	
GPIO_11	B:GPIO16	O:WO0_JTAG_JTDO		O:WO0_JTAG_JTDO	
GPIO_12	B:GPIO17	I:WO0_JTAG_JTDI		I:WO0_JTAG_JTDI	
GPIO_13	B:GPIO18	B:WO0_JTAG_JTMS		B:WO0_JTAG_JTMS	
GPIO_14	B:GPIO19	I:WO0_JTAG_JTCLK		I:WO0_JTAG_JTCLK	
GPIO_15	B:GPIO20	I:WO0_JTAG_JTRST_N		I:WO0_JTAG_JTRST_N	
PWM0	B:GPIO21	O:PWM0	A die Config 0 : MT7975 1 : MT7976	PWM LED	2x13 pin 26
PWM1	B:GPIO22	O:PWM1		WPS LED low active/ emmc_rstb	2x13 pin 7
SPI0_CLK	B:GPIO23	SNFI_CLK		SPI NAND/ eMMC_DAT0	2x13 pin 10
SPI0_MOSI	B:GPIO24	SNFI_MOSI		SPI NAND/ eMMC_DAT1	2x13 pin 8
SPI0_MISO	B:GPIO25	SNFI_MISO		SPI NAND/ eMMC_DAT2	2x13 pin 18
SPI0_CS	B:GPIO26	SNFI_CS		SPI NAND/ eMMC_DAT3	2x13 pin 16
SPI0_HOLD	B:GPIO27	SNFI_HOLD		SPI NAND/ eMMC_DAT4	2x13 pin 12
SPI0_WP	B:GPIO28	SNFI_WP		SPI NAND/ eMMC_DAT5	2x13 pin 22
SPI1_CLK	B:GPIO29	SPIC_CLK		eMMC_DAT6	2x13 pin 23
SPI1_MOSI	B:GPIO30	SPIC_MOSI		eMMC_DAT7	2x13 pin 19
SPI1_MISO	B:GPIO31	SPIC_MISO		eMMC_CMD	2x13 pin 21
SPI1_CS	B:GPIO32	SPIC_CS		eMMC_CLK	2x13 pin 24
SPI2_CLK	B:GPIO33	SPI0_CLK		SPI NOR and SPI Flash(ECC Free)	
SPI2_MOSI	B:GPIO34	SPI0_MOSI		SPI NOR and SPI Flash(ECC Free)	
SPI2_MISO	B:GPIO35	SPI0_MISO		SPI NOR and SPI Flash(ECC Free)	
SPI2_CS	B:GPIO36	SPI0_CS		SPI NOR and SPI Flash(ECC Free)	
SPI2_HOLD	B:GPIO37	SPI0_HOLD		SPI NOR and SPI Flash(ECC Free)	
SPI2_WP	B:GPIO38	SPI0_WP		SPI NOR and SPI Flash(ECC Free)	

UART0_RXD	B:GPIO39	I:UART0_RXD		UART0_TX	
UART0_TXD	B:GPIO40	O:UART0_TXD	2nd A die 0 : XTAL mode 1 : Buffer mode	UART0_TX	
MT7531_INT	B:GPIO66	I:MT7531_INT		MT7531_INT	
SMI_MDC	B:GPIO67	O:SMI_MDC		SMI_MDC	
SMI_MDIO	B:GPIO68	B:SMI_MDIO		SMI_SDIO	

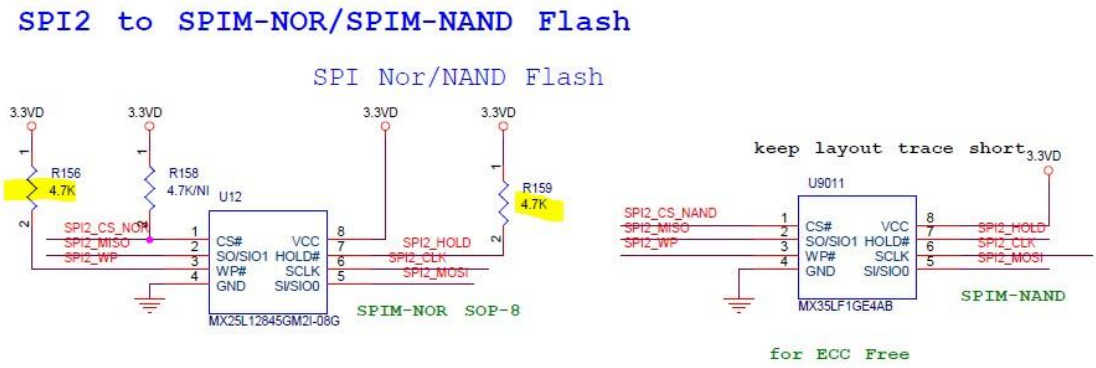
Table 5-3 : MT7986B RFB GPIO definition

5.1.13 I2C

I2C need pull high, SCL up to 400 KHz

5.1.14 SPI

SPI0 for SCK up to 52 MHz, SPI2 for SPIM-NAND or SPIM-NOR, SCK up to 52 MHz, SPI1 support SCK up to 13MHz.
SPI2 default image will work at single or quad mode at different situation.
Please keep HOLD#, WP# pull high.
If you have boot up issue, Schematic and SI is okay, please contact software Engineer to use RFB default image to check first.



5.1.15 SMI (MDC/MDIO)

Support up to 25 MHz, Normally, SDK set MDC CLK at 3.125 MHz(IC default). CPU register 15110000 can read default value 45000504

29:24	PHY_MDC_CFG	**PHY MDC clock configuration** Used to configure the divider N for MDC clock frequency. MDC clock is sourced from 12.5MHz system clock and divided by N. [note] MDC clock is gated or disabled when PHY_MDC_CFG is set to 0.
23:21	RESV0	**Reserved**
20	MDC_TURBO	**MDC clock Turbo mode** When this bit is set, MDC clock is sourced from 25MHz system clock and divided by PHY_MDC_CFG.

5.1.16 PCM

MT7986A just support PCM+SPI or PCM+I2C interface for SLIC (Subscriber Line Interface Circuit ） VOIP FXS port.

5.1.17 SD CARD

Boot mode: 11, Reserve boot from SNFI-NAND and SDCARD for **special** customer can used this design only, below connect verify by MT7986B.

Ball name	Func.0	SD CARD
SPI0_CLK	B:GPIO23	SD_DAT0
SPI0_MOSI	B:GPIO24	SD_DAT1
SPI0_MISO	B:GPIO25	SD_DAT2
SPI0_CS	B:GPIO26	SD_DAT3
SPI1_MISO	B:GPIO31	SD_CMD
SPI1_CS	B:GPIO32	SD_CLK

Table 5-4 : MT7986B/C SD CARD pin mux

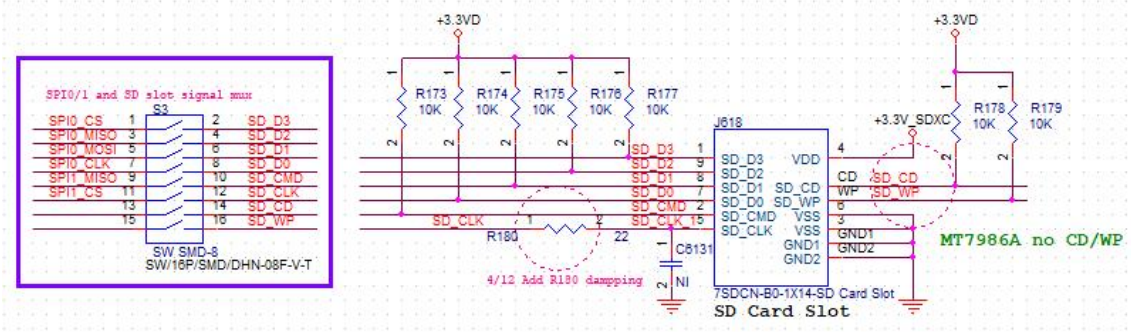


Fig 5-24: SD CARD schematic

5.1.18 ZigBee/BT coexist

Only MT7986A support PTA (3 wire coexist), please use below IO for co-exist, these 3-wire pin can’t be swapped to other GPIO.

MT7986A pin name	GPIO	PTA/Coexist 3-Wire IO	3rd Party signal name
SPI1_CLK	B:GPIO29	I1:UART1_RXD	
SPI1_MOSI	B:GPIO30	O:UART1_TXD	
UART1_RXD	B:GPIO42	I1:UART_PTA_RXD	
UART1_TXD	B:GPIO43	O:UART_PTA_TXD	
UART1_CTS	B:GPIO44	B0:EXT_IF0_0 (zb/bt act)	REQ(Request)
UART1_RTS	B:GPIO45	B0:EXT_IF0_1 (priority)	PRI (Priority)
UART2_RXD	B:GPIO46	B0:EXT_IF0_2 (Wifi Act)	GNT(Grant)
UART2_TXD	B:GPIO47	B0:EXT_IF1_0 (zb/bt act)	REQ(Request)
UART2_CTS	B:GPIO48	B0:EXT_IF1_1 (priority)	PRI (Priority)
UART2_RTS	B:GPIO49	B0:EXT_IF1_2 (Wifi Act)	GNT(Grant)

Table 5-5 : MT7986A ZB/BT coexist pin

5.1.19 Strapping option

MT7986 offer option of boot from SPIM (SPI2)_NOR/ SPIM(SPI2)_NAND/ eMMC. SPIM-NAND ECC control by Flash (Flash ECC or ECC Free). SYS_WATCHDOG is bootstrap for MT7986A only, MT7986B/C don't care.
If MT7986A change DVDD_PROC_L to 0.85V, it will not support external watch dog reset.
GPIO_0 is GSW reset signal, when bootstrap is low, the Giga switch will keep inactive.
GPIO_1 is 2.5G PHY reset signal, when bootstrap is low, the 2.5G PHY will keep inactive
UART_TX0 is bootstrap pin, some of UART console RX signal with other circuit will effect bootstrap, and example UART_RX add LED. Please don't use this kind of USB UART console.
Please note, MT7975 doesn't not support 2nd A die Xtal buffer mode. PWM0 must pull high for 40MHz mode. GPIO_3 setting for AX7800 or AX4200 one A die design, if use one A die, AFE0_XIN_WBG and AFE1_XIN_WBG must wire together.

Pin Name	Strapping Name	Description
{GPIO_1, GPIO_0}	Boot Mode	0 : SPIM-NOR 1 : SPIM-NAND (HDK default) 10 : EMMC 11 : Reserve(SNFI NAND→SD CARD)
GPIO_3	A-Die Mode	0: Two A-Die, or one A die single band(AX7800) 1: One A die Dual band (AX4200)
UART0_TXD	Second A-Die XTAL mode select	0 : XTAL mode (iPA used MT7975 Must) 1 : Buffer mode (Be Care EEPROM bin setting)
PWM0	A-Die Crystal	1 : 40MHz XTAL
SYS_WATCHDOG	CPU 1.023V/0.85V select	For MT798A only MT7986B/C don't care (Don't care)

Table 5-6 : MT7986 strapping option

5.1.20 JTAG

GPIO_6~15 share w/ JTAG mode, GPIO6~10 internal pull up. GPIO11~15 internal pull down.
GPIO_6, GPIO_11 default is output low.
GPIO_6 is internal Pull UP, but default is output low, the behavior will be low when boot up.

Pin	Pin MUX	Pin MUX	Type
GPIO_6	B:GPIO11	OL:JTAG_JTDO	Internal PU
GPIO_7	B:GPIO12	I1:JTAG_JTDI	Internal PU
GPIO_8	B:GPIO13	B1:JTAG_JTMS	Internal PU
GPIO_9	B:GPIO14	I1:JTAG_JTCLK	Internal PU
GPIO_10	B:GPIO15	I0:JTAG_JTRST_N	Internal PU
GPIO_11	B:GPIO16	OL:WO0_JTAG_JTDO	Internal PD
GPIO_12	B:GPIO17	I1:WO0_JTAG_JTDI	Internal PD
GPIO_13	B:GPIO18	B1:WO0_JTAG_JTMS	Internal PD
GPIO_14	B:GPIO19	I1:WO0_JTAG_JTCLK	Internal PD
GPIO_15	B:GPIO20	I0:WO0_JTAG_JTRST_N	Internal PD

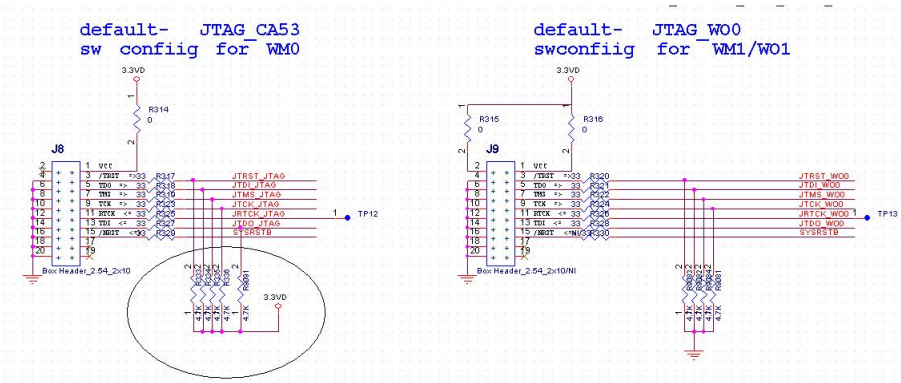


Fig 5-25: MT7986 JTAG

5.1.21 eFuse

MT7986 eFuse voltage pin name is VQPS, it should wire to 1.8V with cap 1uF+0.1uF for secure boot feature to write eFuse, if product don't need secure boot feature, Tie VQPS to GND is okay.

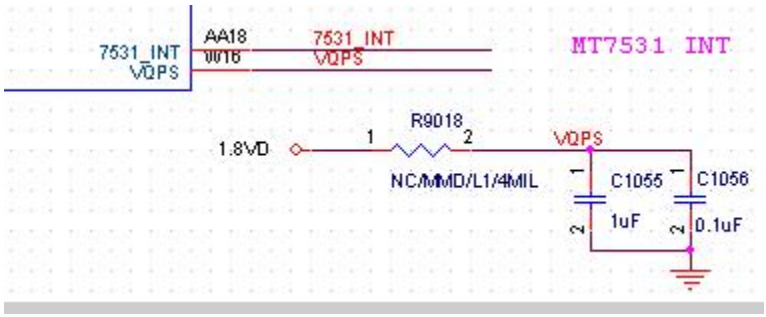


Fig 5-26: MT7986 effuse voltage

5.1.22 TSAUX

MT7986 TSAUS is thermal sensor schematic, the voltage is 1.8V. MT7986/MT7975 have internal thermal sensor too. We didn't use AUXIN1/2/3 to wire thermistor. RFB wire to GND directly. If GND via make power plane not well, keep NC (floating), MD is for TSAUX FT calibration mode, for Normal work, MUST wire to 1.8V.

< 85 degree C, the thermal tolerance around 5%,
> 85 degree C, the tolerance around 7~8%.

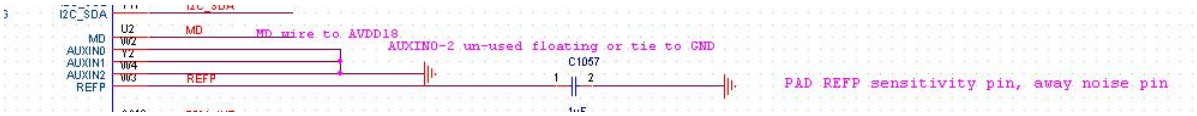


Fig 5-27: TSAUS un-use NC or Tie to GND

5.1.23 OSC

MT7986 reserve 40MHz OSC for D die only Application (No WIFI). Please use 150/100 ohm resistor to divide voltage to 1.6V, MT7986 is co-clock design, MT7975/MT7976 provide Osc source for MT7986. If only one A die or no any A die design, please must wire AFE0_XIN_WBG and AFE1_XIN_WBG (refer Fig 5-30) together, prevent software code to access D die Wi-Fi register to cause system unstable.

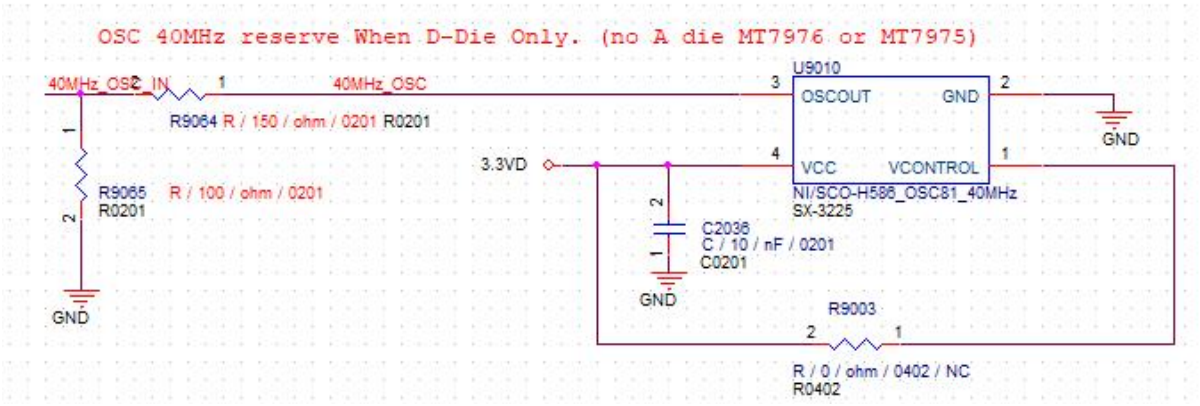


Fig 5-28: OSC 40MHZ

5.1.24 CKQ voltage

MT7986 AVDD18CKQ wire to AVDD18 with 1uF cap, AVDD12_CKQ wire to AVDD12 with 1uF+0.1uF cap.

5.1.25 PLL voltage

PLLGP_TP/PLLGP_TN is differential pair, not in used, Please keep floating.

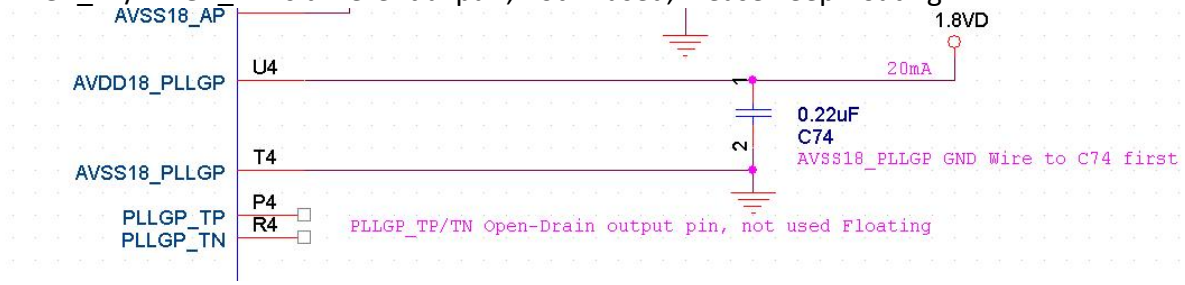


Fig 5-29: PLLGP_TP/TN

5.1.26 AFE

5.1.26.1 Control signal

MT7986C AX4200 control signal is different for2.4G and 5G. They use WF0_HB0_B, and WF0_HB0~10 to MT7976C, WF0_HB0_B is 5G A die control signal clock. WF0_HB0 is 2.4G control signal clock. The CLK must add RC 0R/4.7pF to reduce interference for Wi-Fi 2.4G.

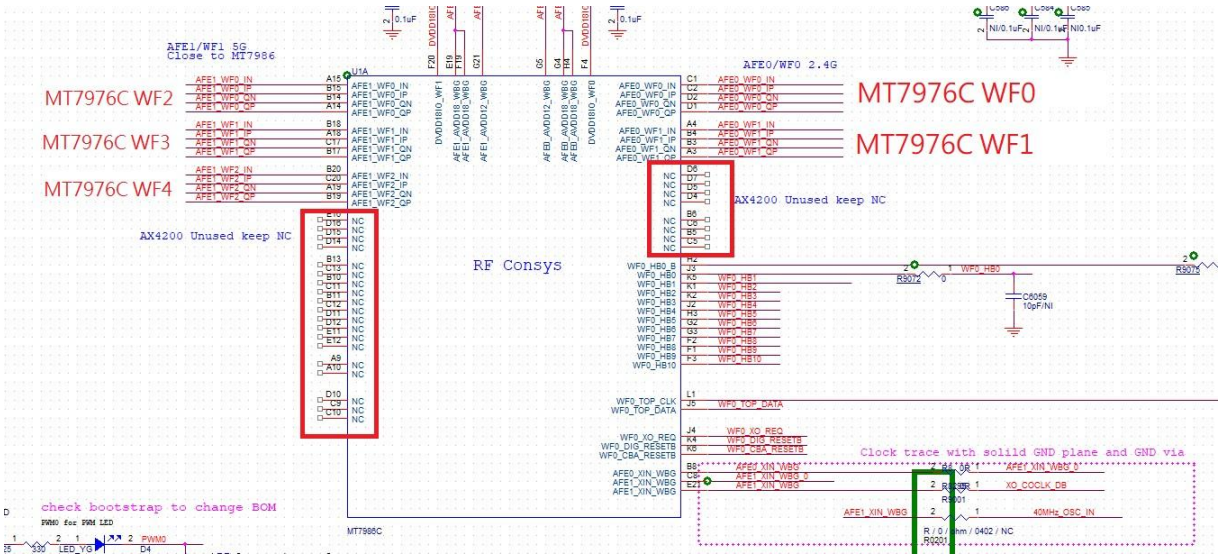


Fig 5-30: MT7986C AX4200 WRI

5.1.26.2 Control signal Clock

The control signal with clock, it should reserve a RC filter close to MT7986 to prevent interference AIQ signal. Suggest RC use 0 ohm, 4.7pF

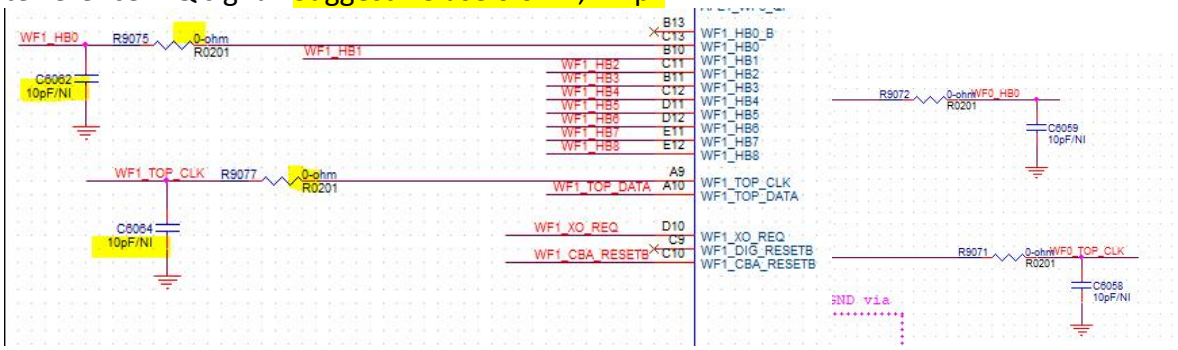


Fig 5-31: WRI/SPI CLK reserve RC

5.1.26.3 AFE power Cap

Per power ball need own two caps 1uF+0.1uF. USB2.0 use the same power source with AFE 1.2V (AVDD12), please reserve 0 ohm resistor to prevent noise.

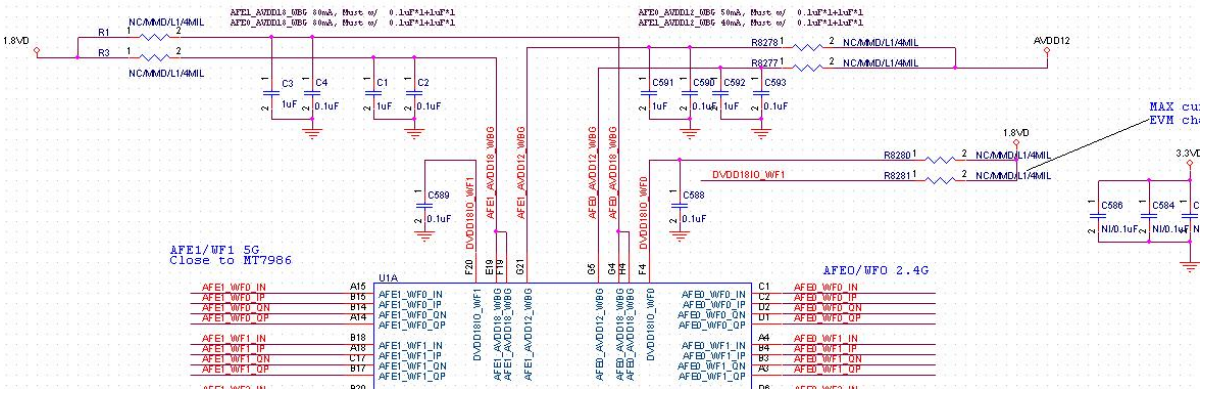


Fig 5-32: AFE power Cap

5.1.26.4 AFE AIQ CLOAD and trace control

AIQ CLOAD signal MUST between 3.6~7pF, don't need impedance control, 5G/6G need to reserve Cap, Close MT7975 or MT7976x. For RF performance, we suggest routing AIQ at layer 3.

.

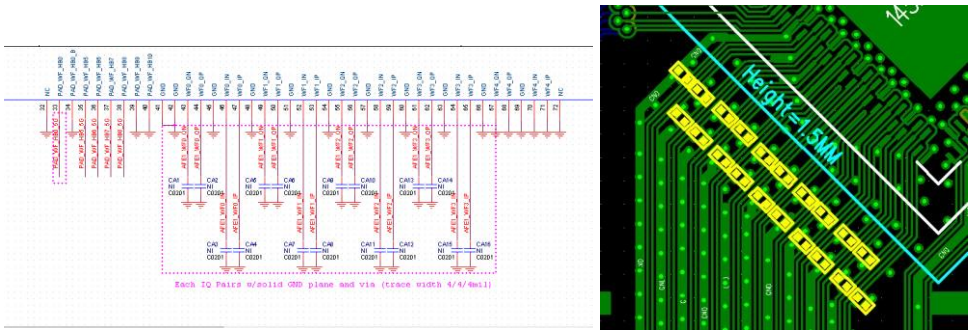


Fig 5-33: AFE power Cap

5.1.26.5 PAD_DIG_RESETB

For AX6000 iPA design use MT7975, MT7986 WF0/1_DIG_RESETB must floating, PAD_DIG_RESETB at MT7975 must pull high to 1.8V and Reserve HB9/HB10 for DIG reset. For AX4200, and AX6000 ePA design, let MT7986x, WFx_DIG_RESETB wire to MT7976x directly.

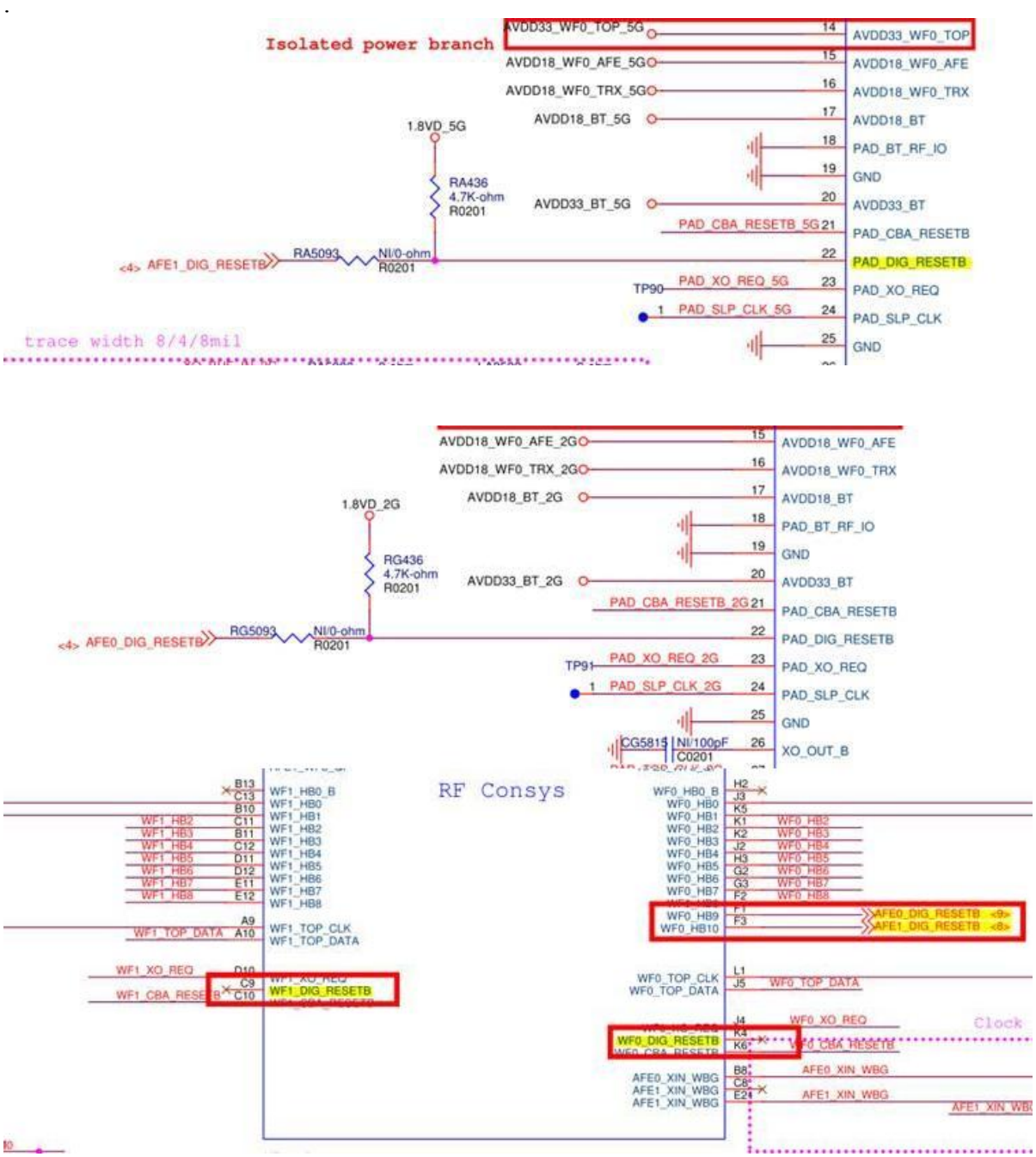


Fig 5-34: MT7975 PAD_DIG_RESETB

5.1.26.6 MT7976x iPA, ePA PA PWR is different

AX4200 iPA design use MT7976C, AX4200 ePA use MT7976DA, AX6000 ePA use MT7976G/A, iPA PA power pin wire to 3.3V, for ePA A die PA power pin wire to 1.8V

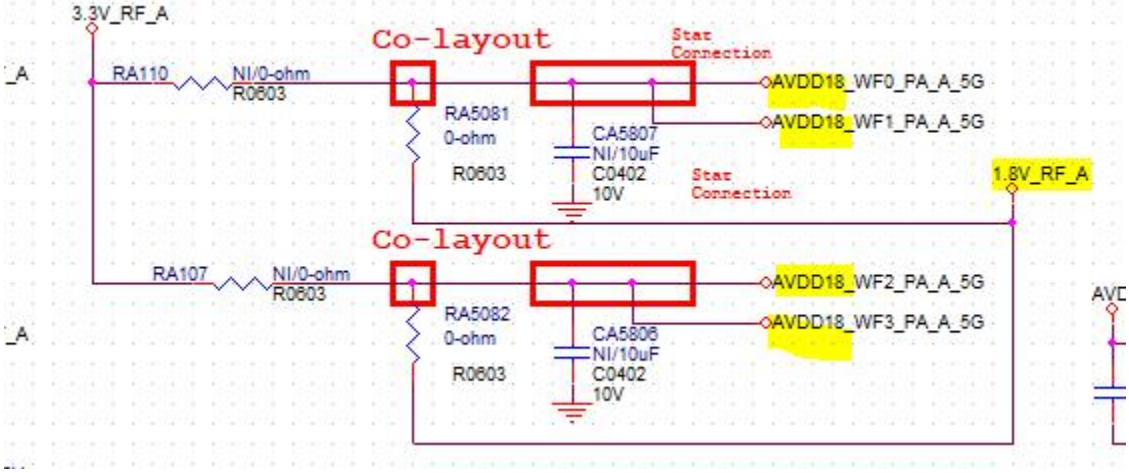


Fig 5-35: MT7976G/A/DA for ePA

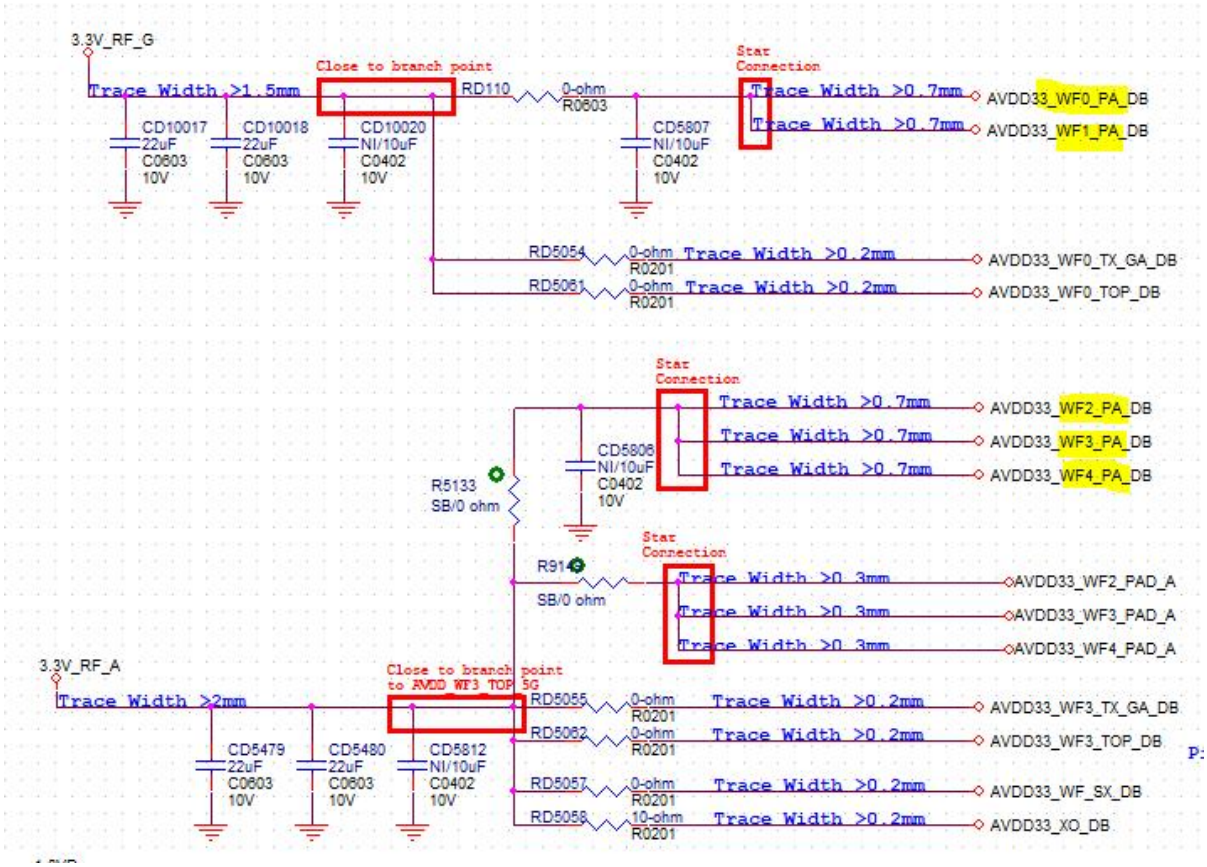
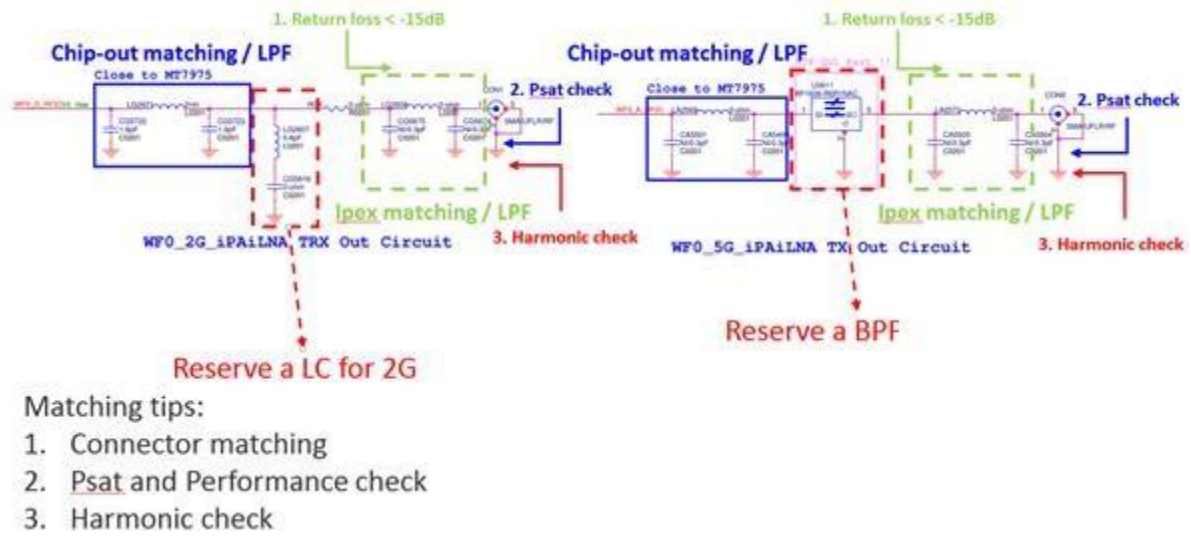


Fig 5-36: MT7976C for iPA

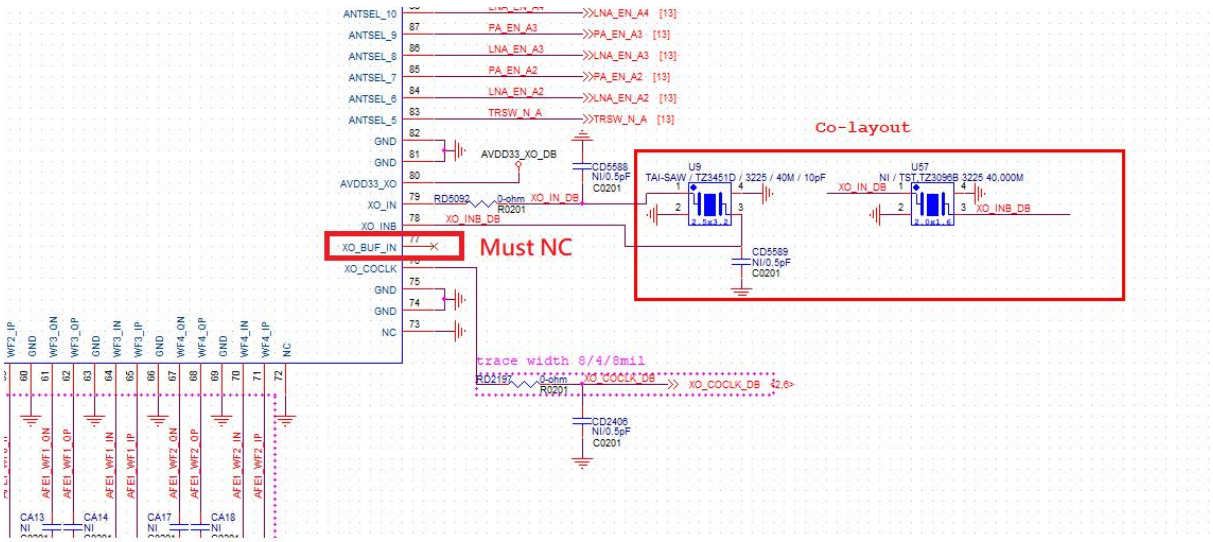
5.1.27 MT7975 WIFI circuit matching



Matching tips:

1. Connector matching
2. Psat and Performance check
3. Harmonic check

5.1.28 MT7976A(5G), MT7976DA(one A die), MT7976C(one A die) pin 77 must NC



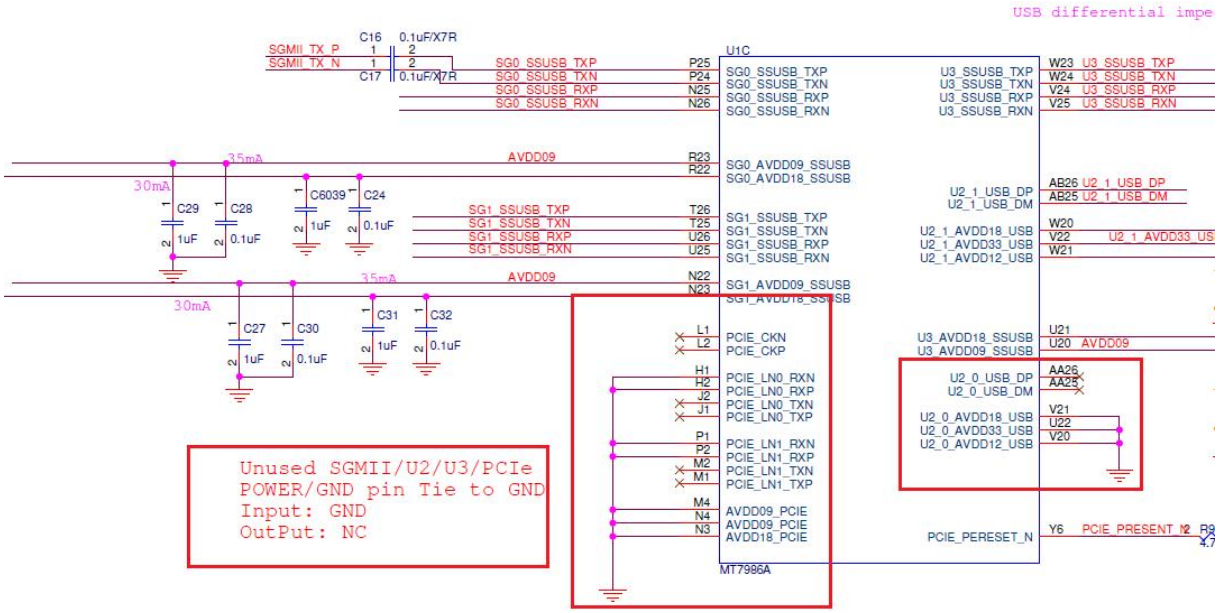
5.1.29 AFE0/1 and Serdes Interface un-used

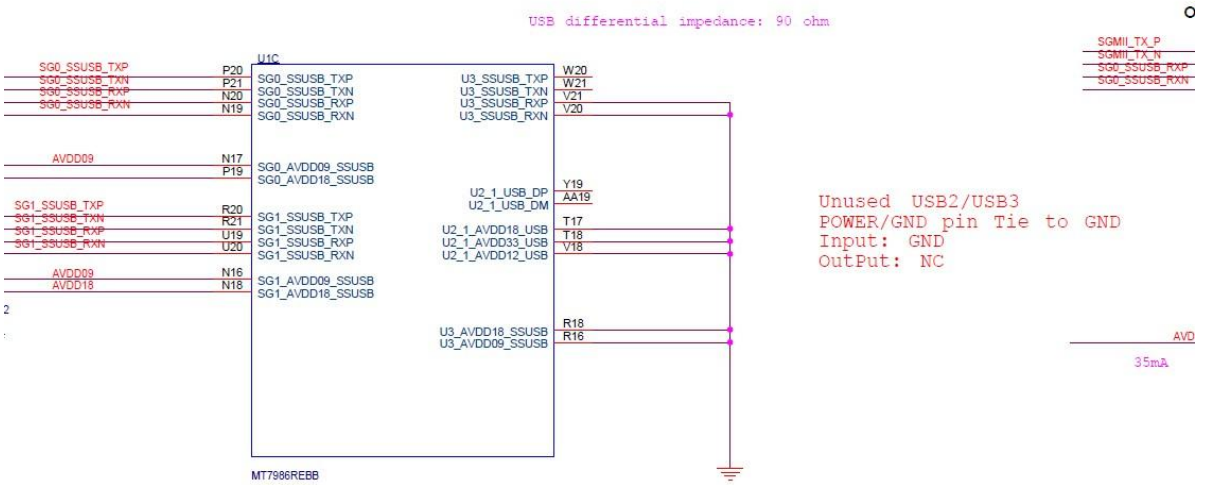
AFE unused

AIQ/WRI: NC
Keep AFE power source pins connected
AFEx_AVDD12_WBG
AFEx_AVDD18_WBG1
AFEx_AVDD18_WBG2
DVDD18IO_WF

Serdes (PCIe/SGMII/USB3.0/USB2.0) Un-used

PWR/GND : GND
RX signal: GND,
TX signal :NC (floating).
Example,





5.2 PCB Layout

5.2.1 4L PCB stack-up

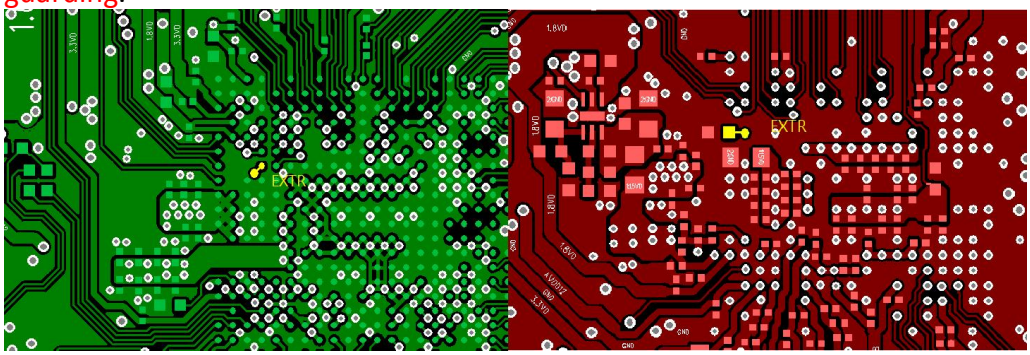
PCB Stack up							Impedance							
Layer	Type		Thickness (mil)			DK	Single end +/-10%				Diff end +/-10%			
Top Side Solder Mask				0.80	mil		線寬(mil)	參考層	ohm值	理論值	線寬(mil)	參考層	ohm值	理論值
L1	TOP	Differential & Signal	pper+Platir	1.40	mil		7(6)	L2	50	49.98	6/4.5(5)	L2	85	85.70
											5/4.5(4.5)	L2	90	90.59
											4.5/5.5(5)	L2	100	99.57
			Prepreg	4.85	mil	3.98								
L2			Copper	1.25	mil		6(7)	L1	50	49.55				
			Core	44.50	mil	4								
L3			Copper	1.25	mil		6(7)	L4	50	49.55				
			Prepreg	4.85	mil	3.98								
L4	BOT	Differential & Signal	pper+Platir	1.40	mil		7(6)	L3	50	49.98	6/4.5(5)	L3	85	85.70
											5/4.5(4.5)	L3	90	90.59
											4.5/5.5(5)	L3	100	99.57
Bottom Side Solder Mask				0.80	mil									
Total				61.10	mil									
				1.55	mm									

Table 5-7 : 4L PCB stack-up

1. Single end 50 ohm : L1/L2,L4/L3 50ohm 7(gap 6mil)
2. Differential pair 90 ohm
   (If Antenna position is not good, suggest routing U3 at L3, prevent 2.4G interference)
   Outer layer: L1/L2, L4/L3 90ohm (5/4.5(gap 4.5mil)
3. Differential100 ohm
   (If Antenna position is not good, suggest routing SGMII at L3, prevent 5G interference)
   Outer layer: L1/L2, L4/L3 100ohm (4.5/5.5(gap 5mil))

5.2.2 DDR layout guidelines

- EXTR for DDR3 40.2 ohm/ DDR4 100 ohm need as short as possible, and good GND guarding.



- MT7986B/C Power Cap Placement

Please MUST follow HDK layout use 0201 0.1uF *8 (TOP) +0201 0.1uF *8 (Bottom) for SOC DDR controller and use 0201 0.1uF *5 at DDR KGD power pin side.

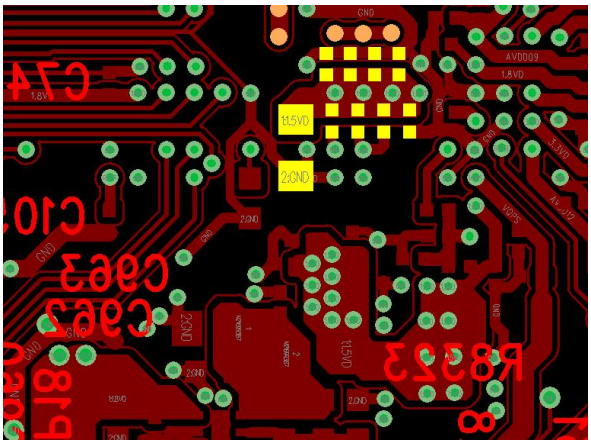


Fig 5-37: DDR SOC Power BOT Cap placement

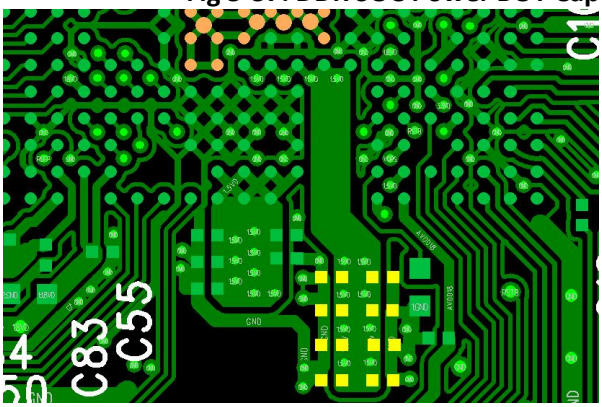


Fig 5-38: DDR SOC power TOP Cap placement

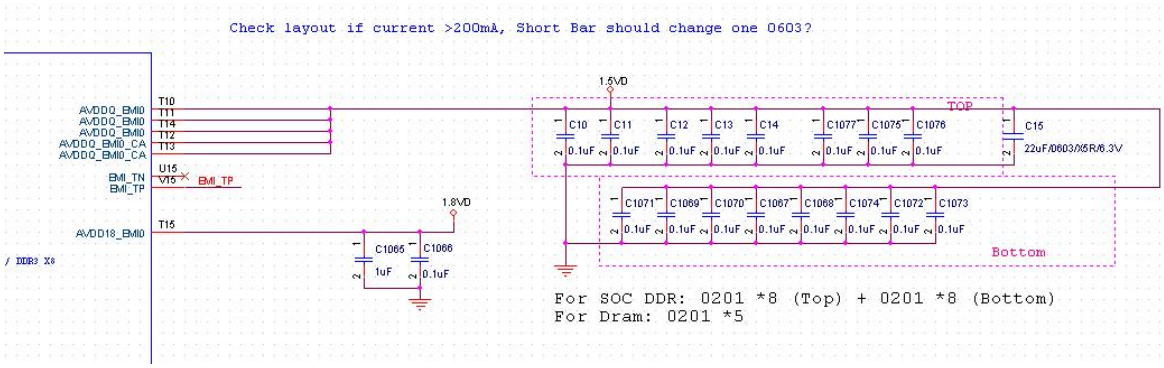


Fig 5-39: MT7986B/C DDR SOC Power schematic

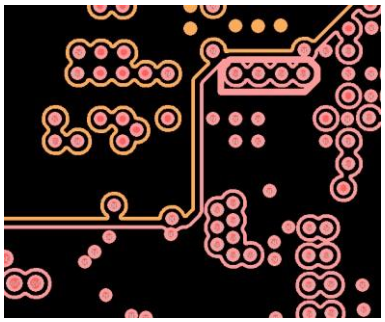


Fig 5-40: MT7986B/C DDR SOC L3 Must add GND guarding

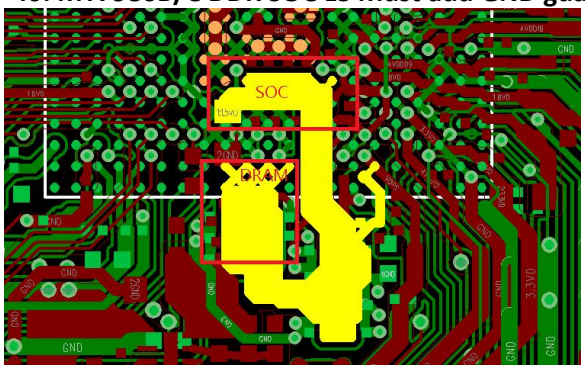


Fig 5-41: MT7986B/C DDR KGD Power

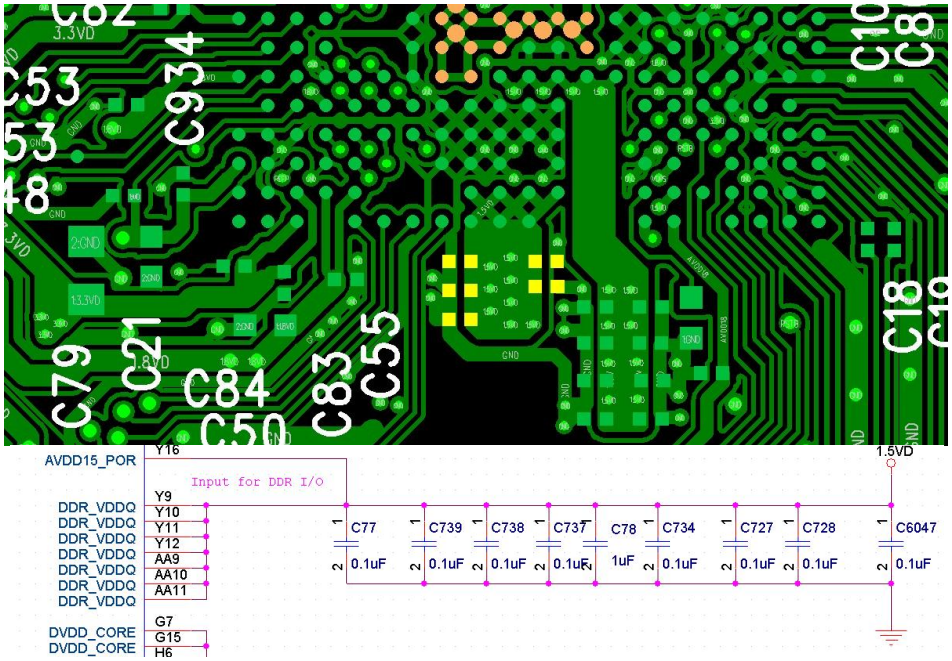


Fig 5-42: MT7986B/C DDR KDG Cap*5 at TOP side

- MT7986A DDR Cap Placement

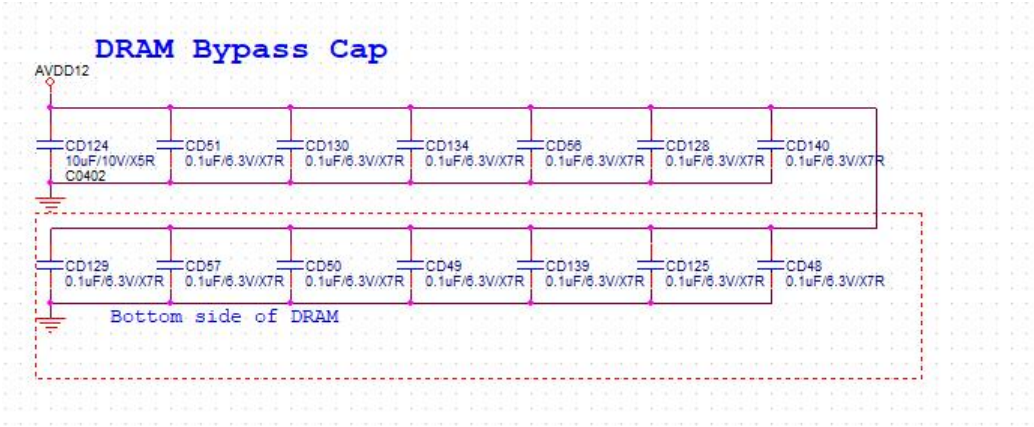
Please MUST follow HDK layout use > below caps number.

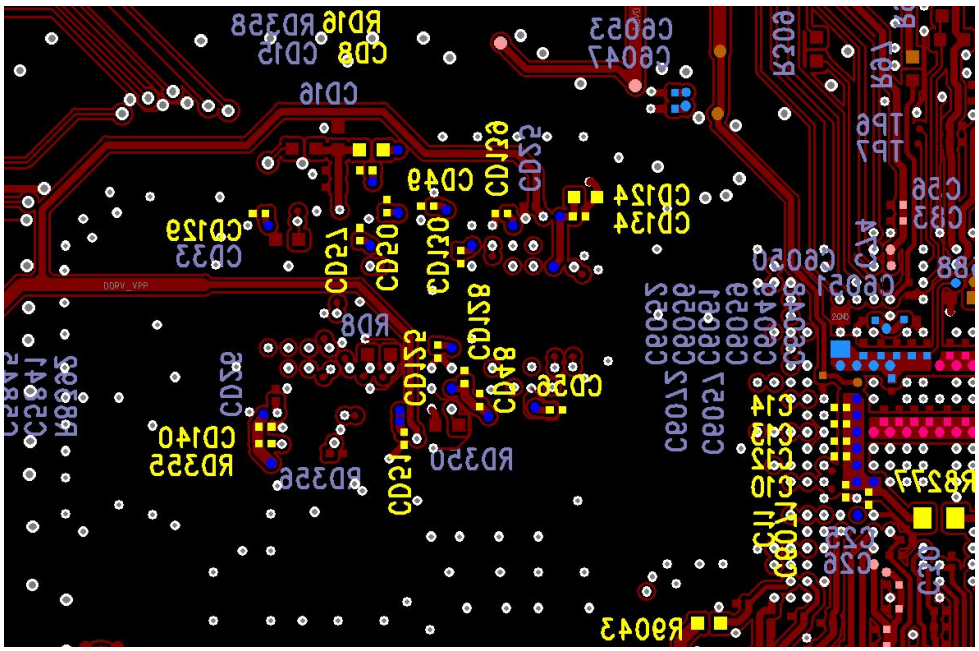
1.2VD

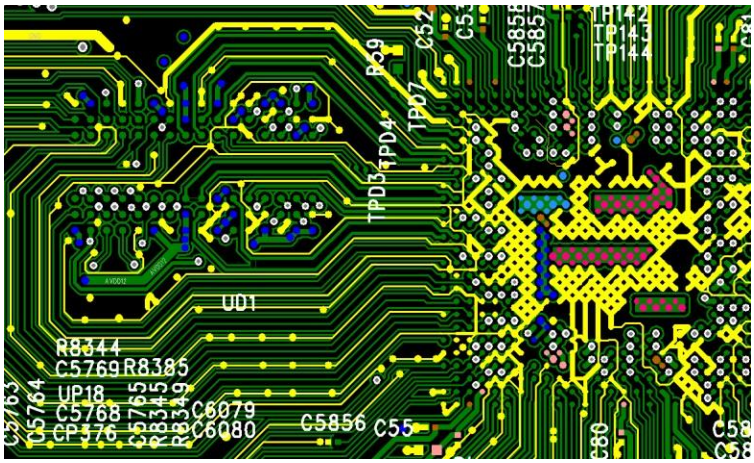
@ SOC side: 0201 *6 [0.1u*3 + 1u*3]

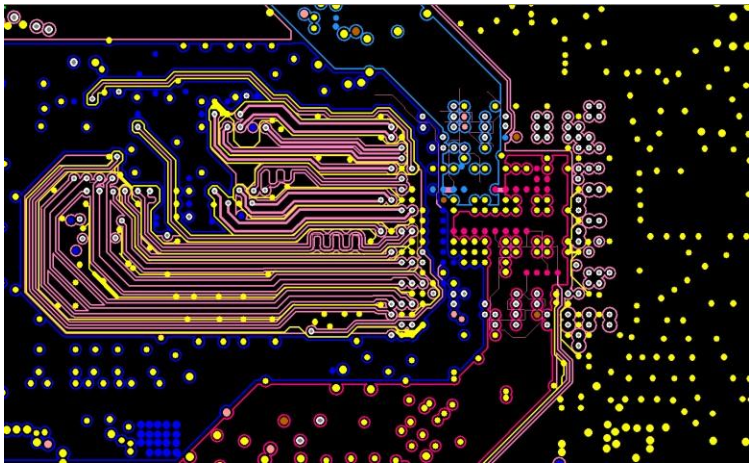
1.8V

@ SOC side: 0201 *1 [0.1u*1]



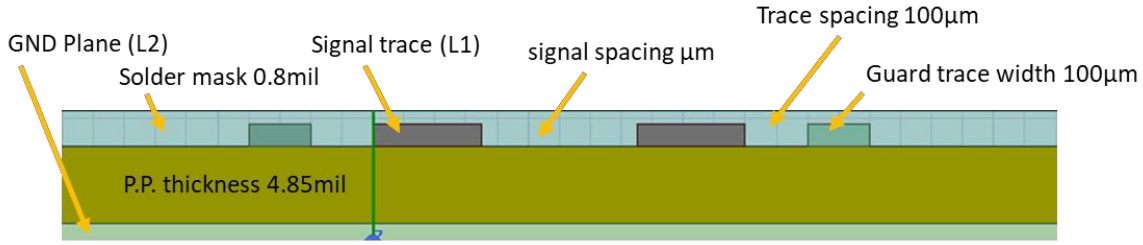




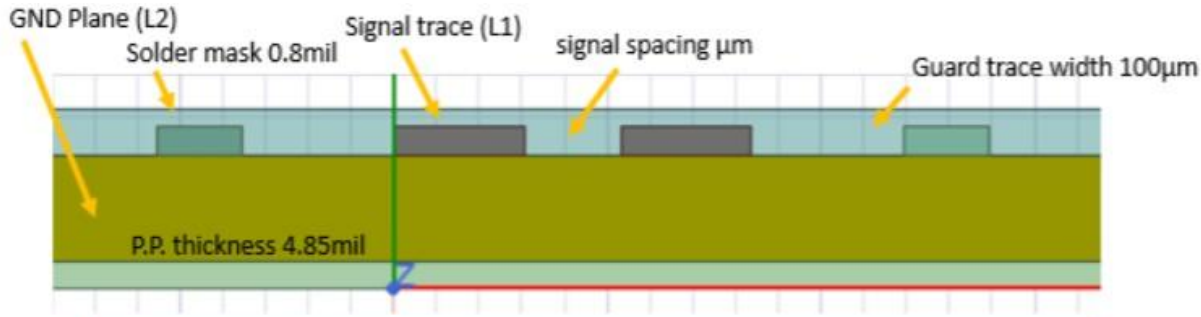


- MT7986A DDR3/4 Layout guide(Suggest copy MTK RFB layout)
  - DDR3/DDR4 Impendence control

    Please refer RFB HDK
    - Differential pair 85~100ohm
    - C/A single end impedance range 55~65 ohm
    - DQ single end impedance range 40~50 ohm



Microstrip (trace on layer 1)			
	Trace Width (μm)	Signal Spacing	Char. Imped. (Ω)
DQ Main Route	175	350	49.1
CA Main Route	100	250	60.4
Strip-line (trace on layer 3)			
DQ Main Route	175	350	44.8
CA Main Route	100	250	55.0



Microstrip (trace on layer 1)			
	Trace Width (μm)	Signal Spacing	Char. Imped. (Ω)
Diff Main Route	100	100	94
Strip-line (trace on layer 3)			
DQ Main Route	100	100	85

Fig 5-43: DQS1/CLK differential pair impedance at layer 3 is 85 ohm

- DDR3 length control
  - Command/Address, Max Length CLK < 2000 mil, Group delta <1000mil
    Or Copy MTK layout (Simulation and test pass), Address A0~13/command <1859mil, except BG0 2174mil, BA0 2051 mil.
  - DQ max length<800 mil, Group delta <300mil
    Or Copy MTK layout will better DQ0~DQ15, DM, DQS max <701mil

Net	|Max() -Min()|< SPEC
EMI0_DM0, EMI0_DQ[0:7]	≦ 300 mil
EMI0_DM1, EMI0_DQ[8:15]	≦ 300 mil

Differential Pair	PN Skew (w/package)
EMI0_DQS0_C, EMI0_DQS0_T	≦ 6 mil

EMI0_DQS1_C, EMI0_DQS1_T	≦ 6 mil
EMI0_CK_C, EMI0_CK_T	≦ 6 mil

- DDR4 length control
  - Command/Address, Max Length CLK < 2000 mil
    Or Copy MTK layout (Simulation and test pass), Address A0~13/command <1991mil, except BG0 2174mil, BA0 2051 mil.
  - DQ max length<800 mil, delta<270mil
    Or Copy MTK layout will better DQ0~DQ15, DM, DQS between 399~801 mil

Net	|Max() -Min()|< SPEC
EMI0_DM0, EMI0_DQ[0:7]	≦ 270 mil
EMI0_DM1, EMI0_DQ[8:15]	≦ 270 mil

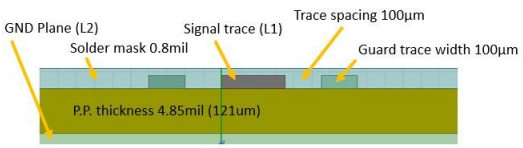
Differential Pair	PN Skew (w/package)
EMI0_DQS0_C, EMI0_DQS0_T	≦ 6 mil
EMI0_DQS1_C, EMI0_DQS1_T	≦ 6 mil
EMI0_CK_C, EMI0_CK_T	≦ 6 mil

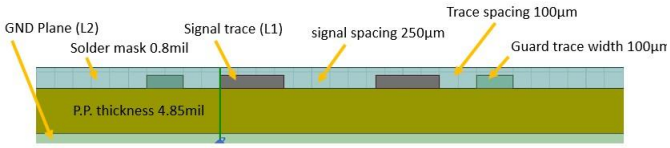
Group	Routing Layer	Reference	Shielding	Width(um)		Edge-to-edge Spacing(um)		Ground Spacing(um)
				Main Route	Breakout	Main Route	Breakout	
DQ	L1, L3	L2	L1 GSSSSSG L3 GSSG	175	100	≥250	≥100	100
CA	L1, L3	L2, L4	L1 GSSSSSG L3 GSSSSSG	100	100	≥250	≥100	100
DQS/CLK*	L3	L2, L4	GSSG	100	100	≥100	≥100	100

➢ Summary of the required trace width and spacing

PCB Stack Up						
Layer	Type		Thickness (mil)			DK
Top side solder mask				0.80	mils	
L1	TOP	Differential & Signal	copper+plating	1.40	mils	
			Prepreg	4.85	mils	3.98
L2			copper	1.25	mils	
			core	44.50	mils	4
L3			copper	1.25	mils	
			Prepreg	4.85	mils	3.98
L4	Bottom	Differential & Signal	copper+plating	1.40	mils	
Bottom side solder mask				0.80	mils	
TOTAL				61.10	mils	
				1.55	mm	

Microstrip
Simulation Topology @ Q2D





Microstrip (trace on layer 1) per-Trace shielding		
	Trace Width (µm)	Char. Imped. (Ω)
Main Route	175	45.3
Break out	100	55.2
Test1	200	43

Microstrip (trace on layer 1) two-Trace shielding			
	Trace Width (µm)	Signal Spacing	Char. Imped. (Ω)
Main Route	175	250	48.7
Break out	100	100	58.7

- Use power/ground for isolation.
- RESET/ALERM don't need to control
- Keep solid L2 reference plane (GND)
- For DQ0~7/DQS0/DM0 /CA at L1, refer to ground beneath
- For DQ8~15/DM1/CA/CLK/DQS1 at L3, refer to ground plane both above and below
- Signal's layout topology should be routed at L1 and L3 as illustrated below
- For DQ routing at L1/L3, two signal traces with adjacent GND shielding are suggested
- For CA routing at L1/L3, three signal traces become a group with nearby GND shielding
- For CA 1T (ODT/CKE/CS), routing at L1/L3, **per signal traces** GND shielding
- For DQS0 routing at L1, per DQS+/- with adjacent GND shielding are suggested, +/- Skew <6mil (with package, Package length, please check below table)
  For DQS1 routing at L3, per DQS+/- with adjacent GND shielding are suggested, +/- Skew <6mil (with package, Package length, please check below table)
- For CLK routing at L3, per CLK+/- with adjacent GND shielding are suggested, +/- Skew <6mil (with package, Package length, please check below table)
- For CA/CLK/DQS at L3, signal traces with GND reference beneath are suggested Ground shielding
- GND Shielding traces at L1 must connect to ground plane at L2 through ground via and/or ground balls at L1 at both SoC side and DRAM side.
- Summary of the required trace width and spacing

Group	Routing Layer	Reference	Shielding	Width(um)		Edge-to-edge Spacing(um)		Ground Spacing(um)
				Main Route	Breakout	Main Route	Breakout	
DQ	L1, L3	L2	L1 GSSSSSG L3 GSSG	175	100	≥250	≥100	100
CA	L1, L3	L2, L4	L1 GSSSSSG L3 GSSSSSG	100	100	≥250	≥100	100
DQS/CLK*	L3	L2, L4	GSSG	100	100	≥100	≥100	100

		<800mil	packcage	P/N SKEW / package <6mil	max delta <300 mil	Trace width	impedance	Layer
DQ0-7	EMI0_DQC	537.3673				7mil		
	EMI0_DQ1	465.2988				7mil		
	EMI0_DQ2	590.7461						
	EMI0_DQ3	528.5453						
	EMI0_DQ4	701.7398						
	EMI0_DQ5	570.3461						
	EMI0_DQ6	632.2244						
	EMI0_DQ7	564.9						
	EMI0_DQS0_C							
	EMI0_DQS							

		<2000mil	packcage	P/N SKEW / package <6mil	max delta <1000mil	Trace Width	impedance
Adderess	EMI0_A0	1439.201			983.2897638	4mil	55-65
	EMI0_A1	1070.836				4mil	
	EMI0_A2	1414.146				4mil	
	EMI0_A3	1859.575				4mil	
	EMI0_A4	1044.358				4mil	
	EMI0_A5	1696.895				4mil	
	EMI0_A6	926.5209				4mil	
	EMI0_A7	1607.882				4mil	
	EMI0_A8	945.8681				4mil	
	EMI0_A9	1449.242				4mil	
	EMI0_A10	1265.945				4mil	
	EMI0_A11	1060.038				4mil	
	EMI0_A12	1037.933				4mil	
	EMI0_A13	1483.702				4mil	
	EMI0_A14	971.1339				4mil	
	EMI0_CK_C	948.2252	121.1670805	0.353137138		4mil	85~100
	EMI0_CK_T	954.1063	114.932841			4mil	
	EMI0_BA0	1164.828				4mil	55-65
	EMI0_BA1	993.1484				4mil	
	EMI0_BA2	1330.42				4mil	
	EMI0_CAS_N	996.2398				4mil	
	EMI0_CKE0	876.285				4mil	
	EMI0_CS0_N	1004.156				4mil	
	EMI0_RAS_N	1086.409				4mil	
	EMI0_WE_N	1372.734				4mil	
	EMI_EXTR	170.0098				4mil	
	EMI_RESET_N	1172.507				4mil	
	EMI0_CKE0	876.285				4mil	

Note: CLK/DQS0/DQS1 DDR3/4 use the same pin, the package length is same

5.2.3 USB2/3

- PCB Fan out TX/RX pairs with PWR/GND isolation in break-out area
- If there is no signal routing below TX/RX BGA → apply anti-pad for better impedance control
- P/N trace length control on PKG+PCB
  - Trace length compensation for ball-pitch on package
  - Routing **P/N (REF CLK included) skew < 5mil** for total length from IC to Connector.
  - USB: Traces must maintain **90 Ω+-10% differential**.
  - Use power/ground for isolation.
  - Use min. width/spacing (ignore Z control in this area) to enlarge the spacing between TX/RX.
  - If there is no signal routing below TX/RX BGA → apply anti-pad for better impedance control

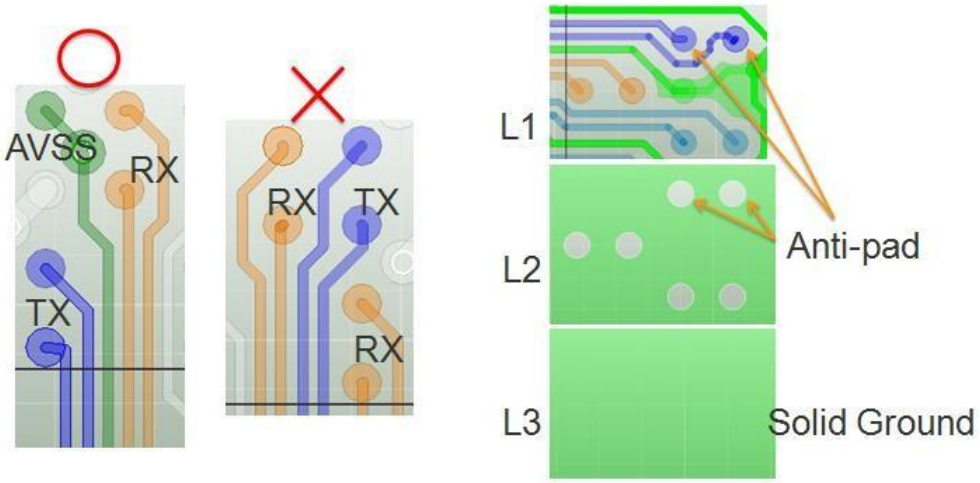


Fig 5-44: USB3 and PCIe ball map and fan-out

The length matching compensation should be made as close as possible to the point where the length variation occurs.

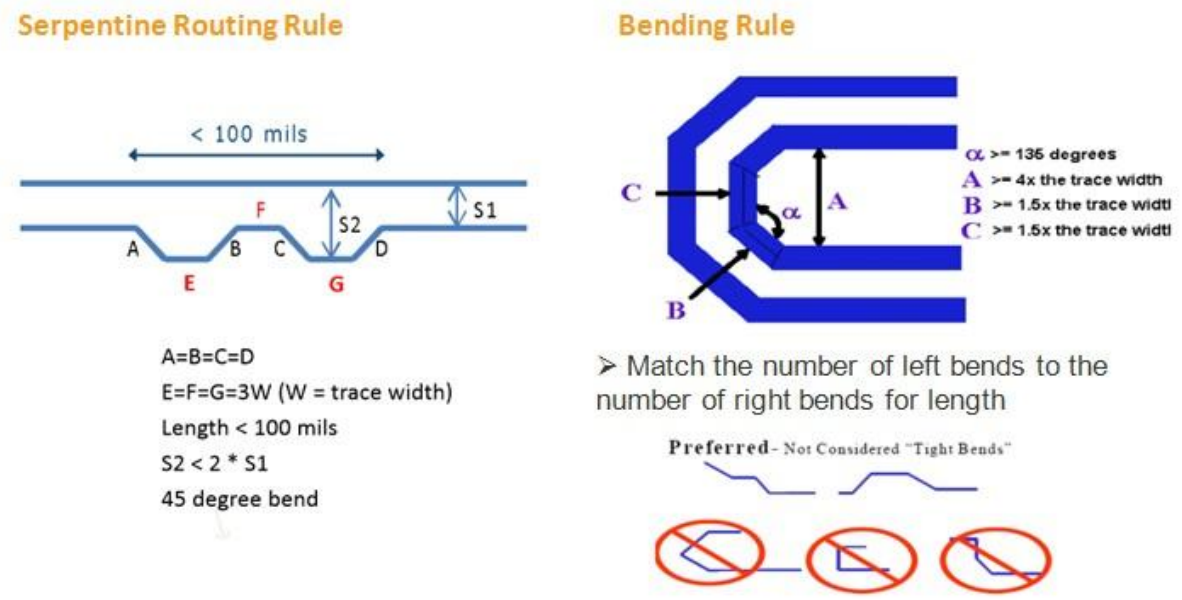


Fig 5-45 : Trace length matching

- Keep USB_DP/DM_P0 and USB_DP/DM_P1 differential pairs routing with well "GND shielding".
- Impedance is 90-ohm (differential)
- USB_5V power trace >=20mil
- Differential pair via count <2

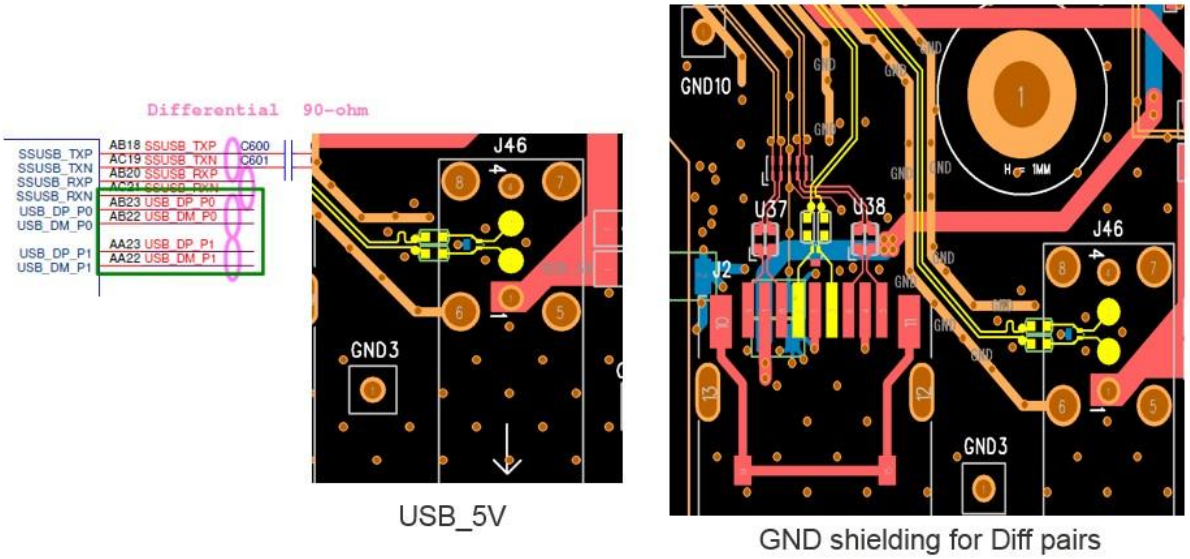


Fig 5-46: USB2.0 layout notice

- Separate each USB3 pairs (SSUSB_TX/SSUSB_RX) with “well GND shielding”
- Impedance is **90-ohm ± 10% (differential)**
- USB3.0 On board **Trace <6000mils** (base on PCBA & eye diagram margin).
- USB3.0 PCB routing **P/N skew < 5mils** for total length from IC to Connector.
- USB2.0 PCB routing **P/N skew <50mils**.

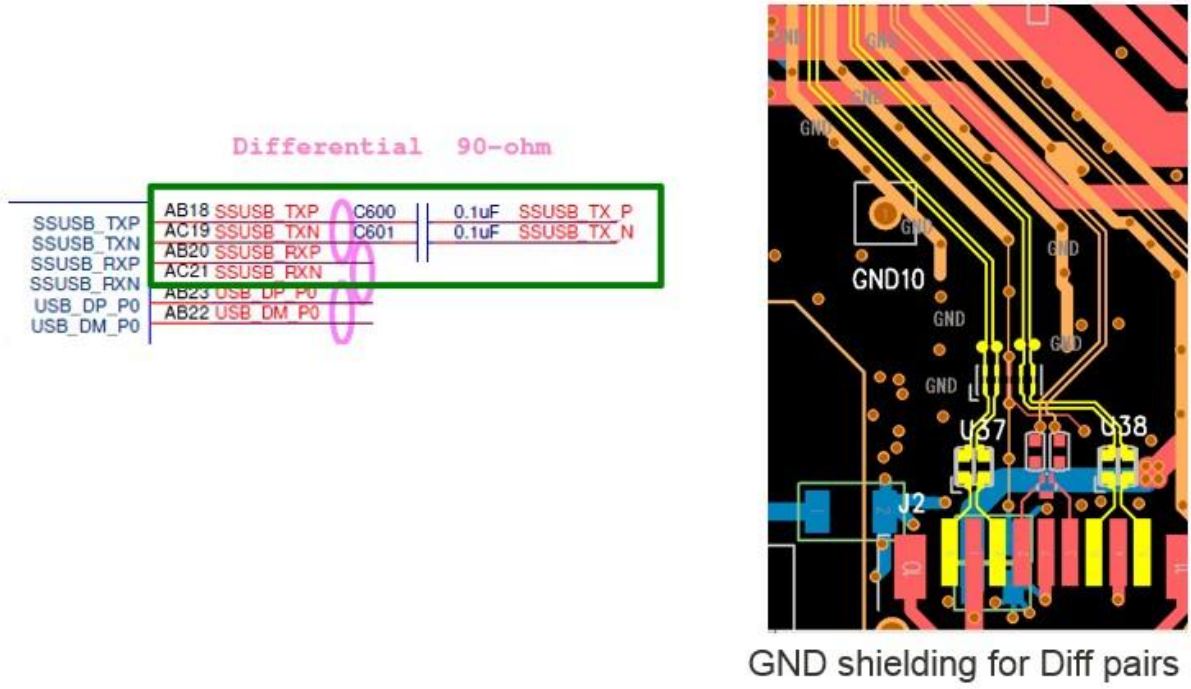


Fig 5-47: USB3.0/USB2.0 layout notice

5.2.4 HSGMII

- Separate each HSGMII pairs (SGMII_TX / SGMII_RX) with “well GND shielding”
- Impedance is **100-ohm ± 10% (differential), run at 3.125Gbps, and 80~100 ohm will be better.**
- SGMII On board **Trace<6000mils** (base on PCBA & eye diagram margin).
- SGMII PCB routing **P/N skew < 5mil** for total length from IC to Connector.
- Differential pair signal, Chip to chip total Via count <2

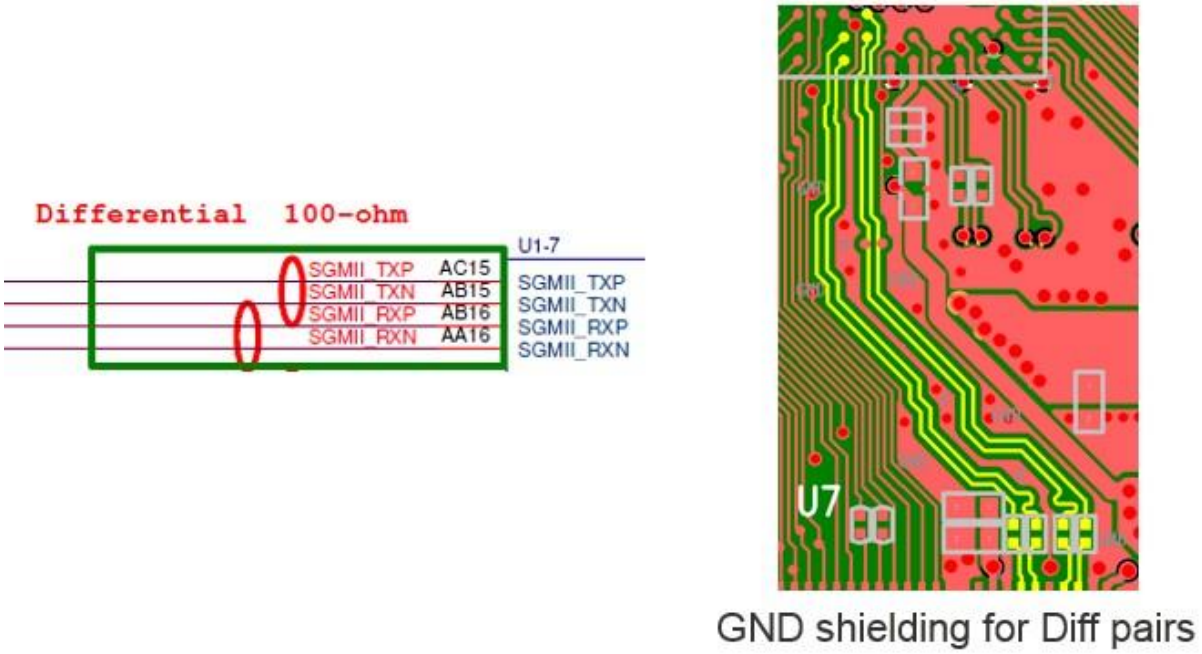


Fig 5-48: SGMII differential line structures

5.2.5 PCIe

- Standard impedance

4.7.8. Differential Data Trace Impedance

The PCB trace pair differential impedance for a 5.0 GT/s capable data pair must be in the range of 68 Ω to 105 Ω. The PCB trace pair differential impedance for an 8.0 GT/s capable data pair must be in the range of 70 Ω to 100 Ω. These limits apply to both the add-in card and the system board.

PCIe0
PCIe0 TX: 85ohm ± 10%
PCIe0 RX: 85ohm ± 10%
PCIe0 CLK: 100 ohm ± 10%
Via count <2
Separate each PCI-e pairs (TX/RX/REFCLK) with “well GND shielding”
PCIE On board Trace<6000mils (base on PCBA & eye diagram margin)
PCIE routing P/N (REF CLK included) skew < 5mil for total length from IC to Connector. Try to keep golden-finger close PAD edge

5.2.6 MT7531A Ethernet 10/100/1Gbps TX

- The Tx+/Tx- and Rx+/Rx- traces should always be as short as possible
- The individual trace impedance of Tx+/Tx- and Rx+/Rx- must be kept the differential characteristic impedance of the pair **must be 100 ohm.**
- Avoid placing noisy digital signal traces near these sensitive pins.

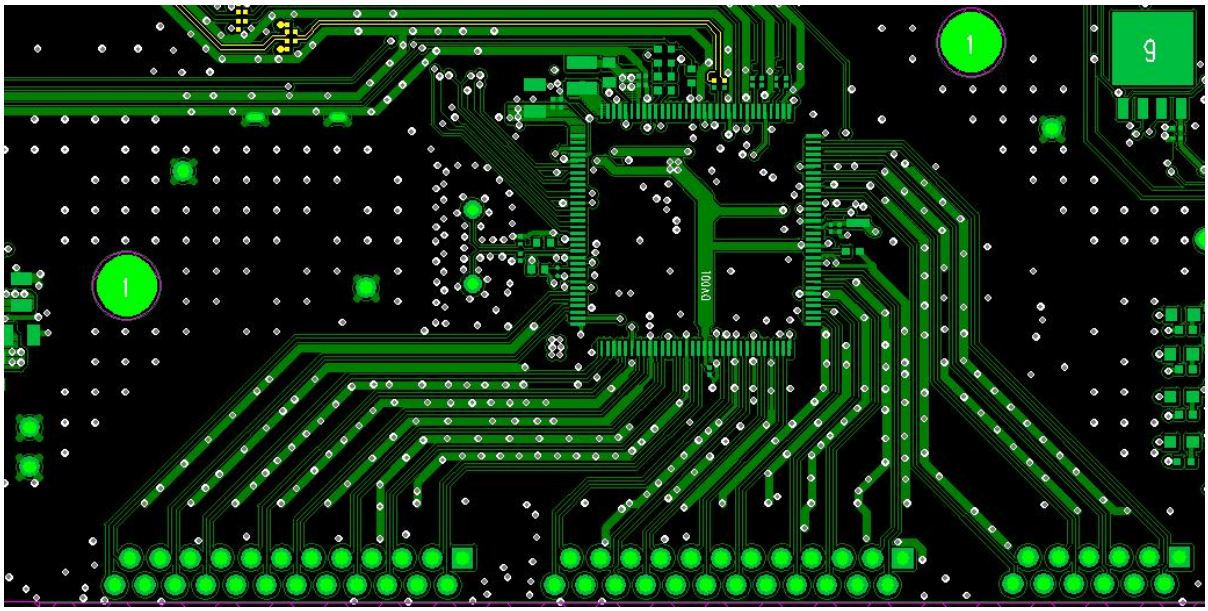


Fig 5-49: The shielding line example of Ethernet layout

5.2.7 PMIC

5.2.7.1.1 DVDD_CORE voltage feedback pin

- Short bar resistor R9058 pads must be placed **very closely to MT7986B DVDD_CORE power ball and the traces must be well grounded**

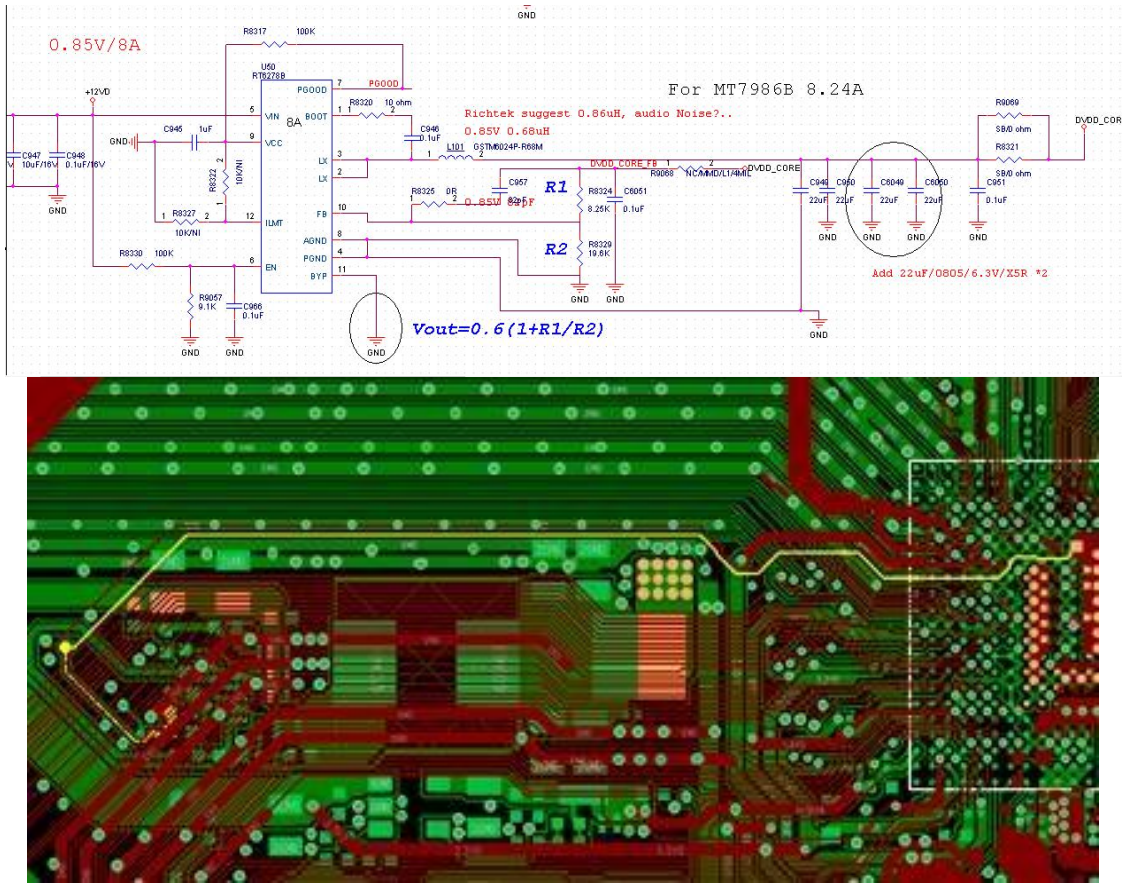


Fig 5-50: The DVDD_CORE Feedback pin layout guidelines.

5.2.7.1.2 DVDD_CORE regulator and MT7986B distance

- The DVDD_CORE (0.85V) max power current is 8.24A (at least use 0201 1uF*16+ 10uF), the power plant must be well and shorten the distance between regulator and MT7986B to prevent voltage drop.

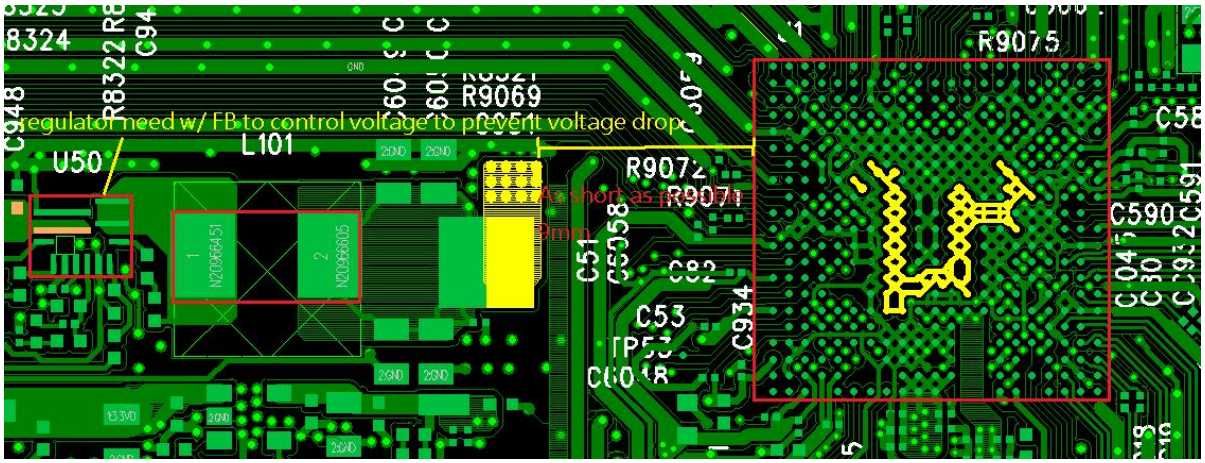


Fig 5-51: The DVDD_CORE and MT7986B distance.

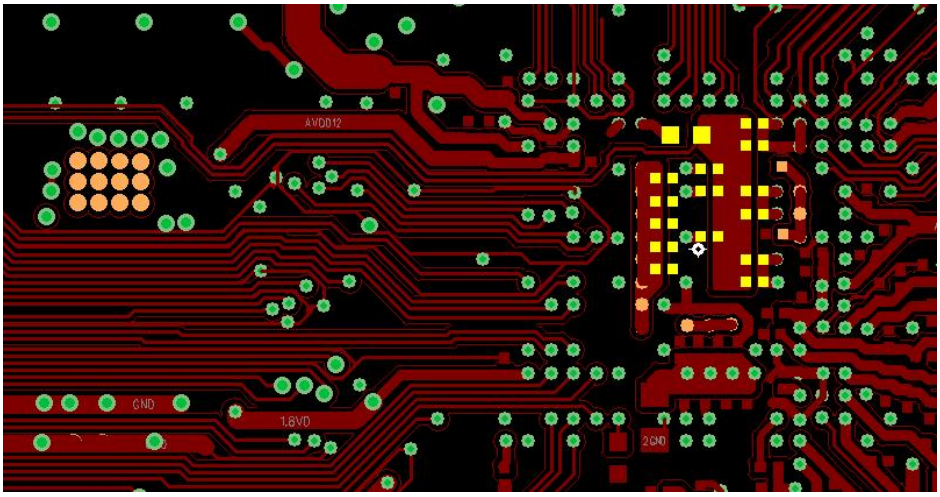
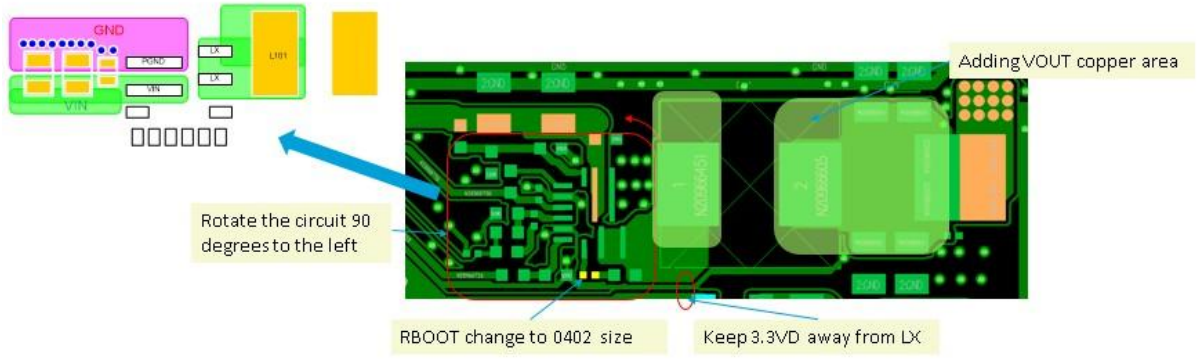


Fig 5-52 : The DVDD_CORE Cap position.

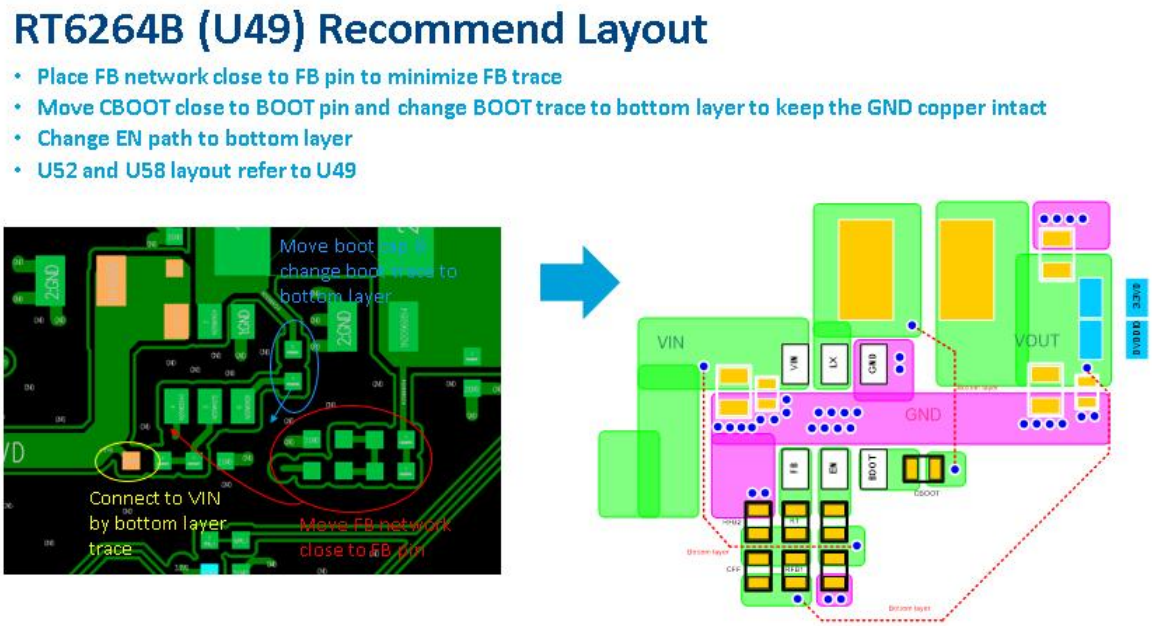
- The DVDD_CORE (0.85V) feedback signal must leave noise signal far away LX is noise source.



5.2.7.1.3 3.3V/1.8V regulator recommend layout

If you follow HDK Buck for design, **Richtek 2021Q3 suggest use RT6255B to replace RT6264B (NOT pin to pin).**

1.8V/3.3V regulator layout suggestion



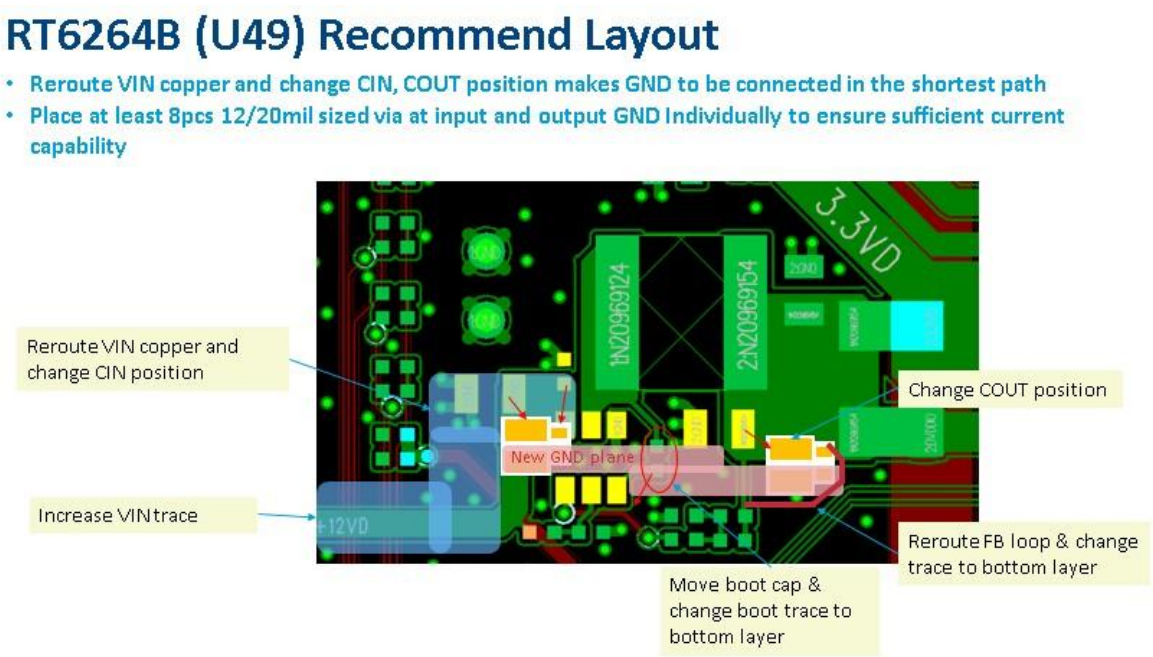


Fig 5-53: The 3.3V power regulator layout suggestion

5.2.7.1.4 5V regulator recommend layout

USB 5V regulator layout suggestion

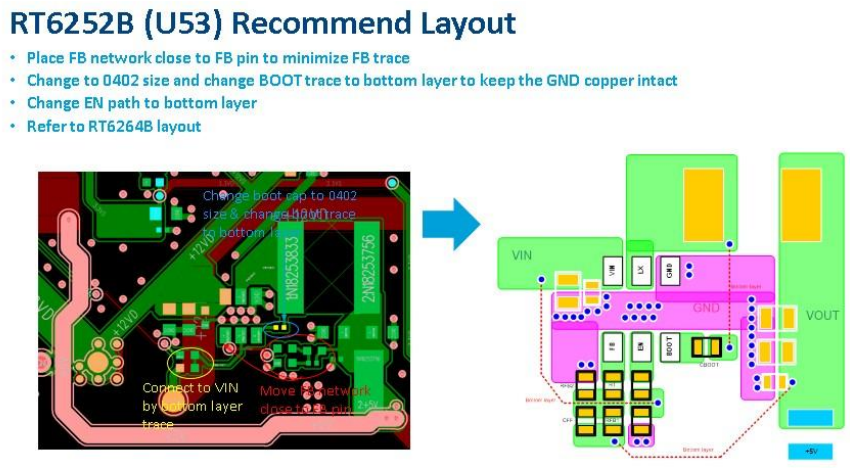


Fig 5-54: The 5V power regulator layout suggestion

5.2.7.1.5 DDR3 1.5V regulator recommend layout

Place COUT (C962) close to VOUT pin, Adding GND via at input and output to increase thermal dissipation

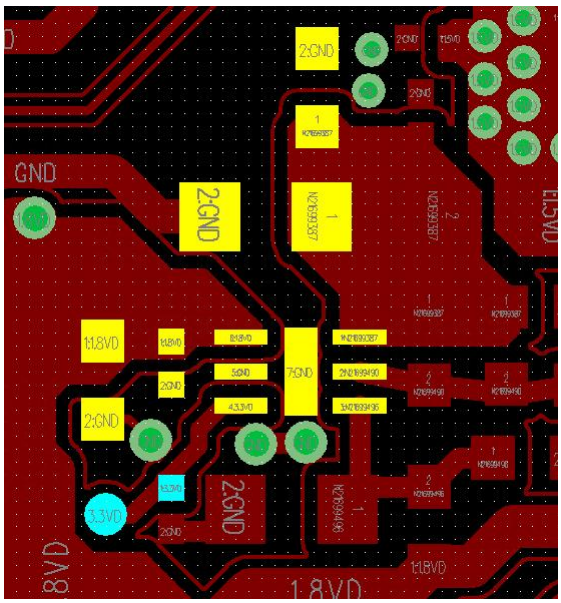


Fig 5-55: The 1.5V power regulator layout suggestion

5.2.7.1.6 AVDD18 LDO regulator recommend layout

Place COUT (C988) close to VOUT pin, Adding GND via at input and output to increase thermal dissipation

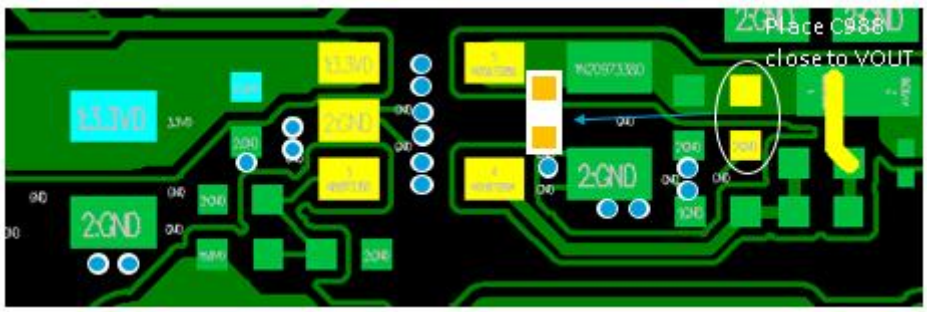


Fig 5-56: The AVDD18 power regulator layout suggestion

5.2.7.1.7 0.9V LDO regulator recommend layout

Change C1002 direction to make CIN ground consistent, place C1004 close to VOUT pin, Adding GND via at input and output to increase thermal dissipation

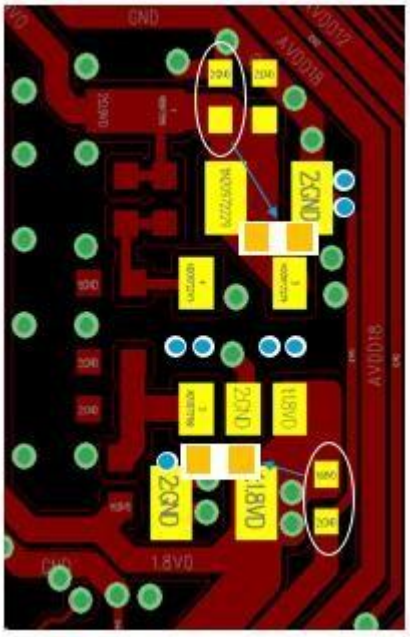


Fig 5-57 : The 0.9V power regulator layout suggestion

5.2.8 VQPS

This is eFuse voltage signal, The power trace need to wider. (Customer board don't need to program eFuse, it can tie to GND.

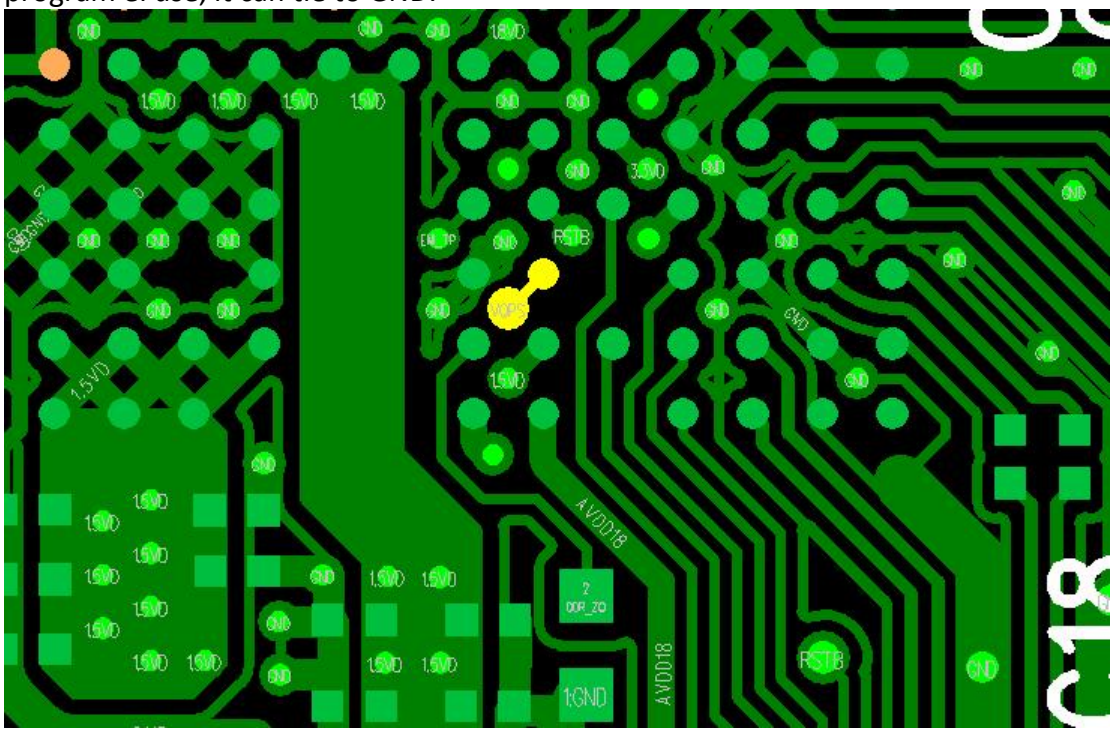
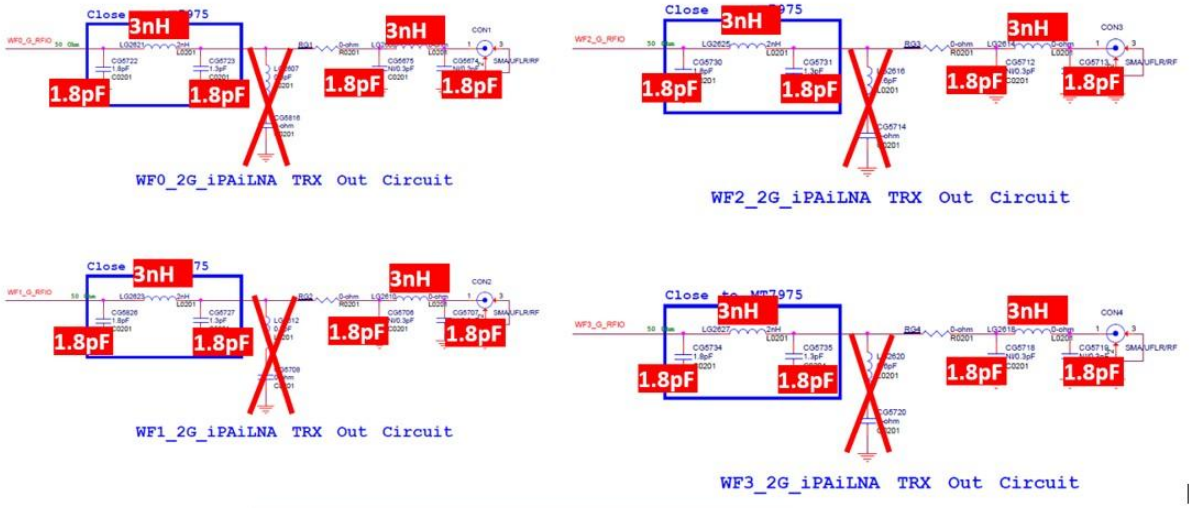


Fig 5-58: VQPS power trace width

5.2.9 MT7975 iPAiLNA design on WiFi

Recommend the trace length from chip-out to ANT port should be similar between WF0 to WF3 with 50 ohm impedance.
RF trace should be isolated by GND vias and keep it away the noisy signal, like XTAL trace. Here, to avoid the interference from XTAL and its trace routing, suggest add GND via around it and its trace routing to increase isolation between it and other traces.
RF matching values and its recommended part numbers are listed in Fig 5-59. RF performance may need to be checked/tuned again if the component vendor or PCB stack are changed.



Part	Package	Tol.	Manufacturer P/N.	Manufacturer
1.8pF	C0201	±0.1pF	GRM0335C1H1R8BA01D	Murata
3nH	L0201	±0.1nH	LQP03TN3N0B02D	Murata

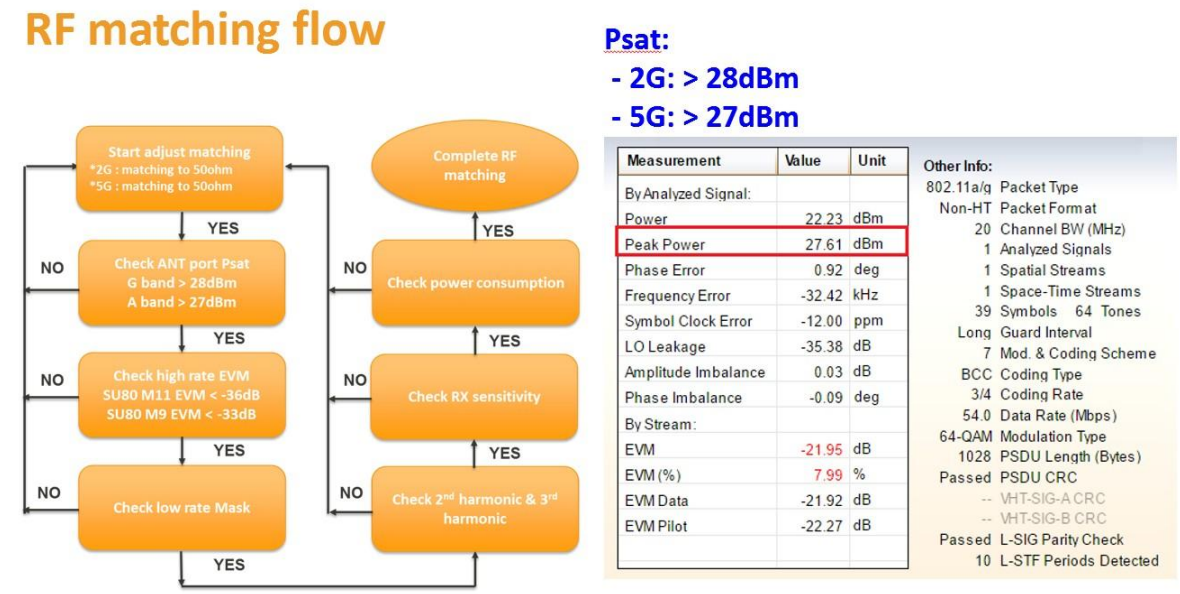


Fig 5-59: iPAiLNA RF recommended matching and the matching flow

5.2.10 MT7976C/DA iPAiLNA design on WiFi

The Wifi matching, please refer MT7916+MT7976 HDK and design document

5.2.11 MT7976x ePAeLNA design on WiFi

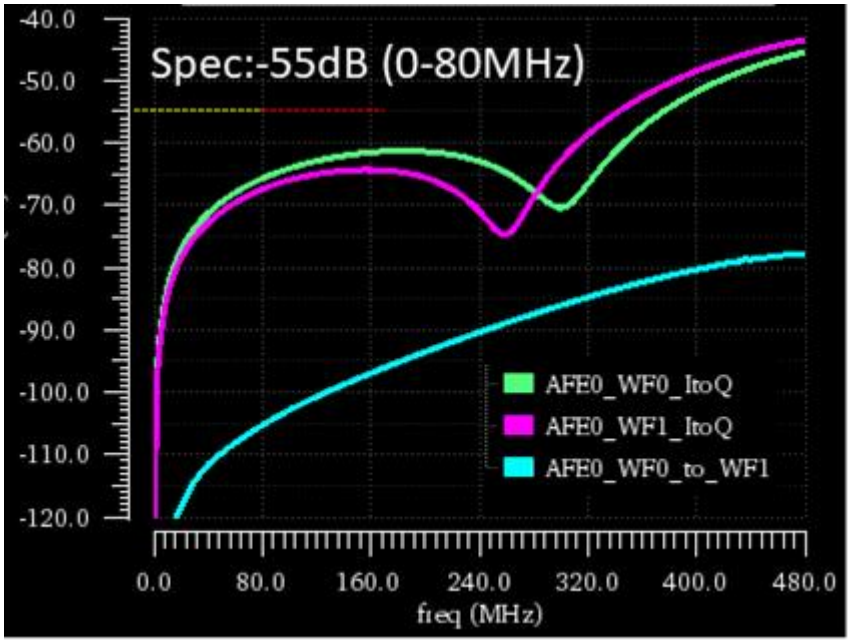
The Wifi matching, please refer MT7986+MT7976 ePAeLNA RF design Guideline document.
[MT7986+MT7976] ePAeLNA RF RF Design Guideline_20211116B.pdf

5.2.12 AIQ trace length control (No need to impedance control)

AIQ trace length should be controlled smaller than 8cm (max Cload 9pF) for 2.4G, and it should be controlled between 3cm (min Cload 3.6pF) and 6cm (max Cload 7pF) for 5G/6G.
It also needs to meet the requirement, trace difference in the same WF smaller than 1.5mm, from D die to A die.
To meet the isolation requirement for maximum BW in Figure 5-60, 40MHz in 2.4G and 160MHz in 5G, suggest follow the recommend in below:

- For 2.4G, there are 4 mil trace width and spacing between the differential pair, and4 mil spacing to GND.
- For 5G, there are 4 mil trace width and spacing between the differential pair, and8 mil spacing to GND.
- Add GND via between pairs.

Fig 5-60: lists the AX6000 AIQ trace length and its net name. The different value at different AIQ streams are highlighted in RED color.



Rules(<1.5mm)	2G AIQ length(mm) <80mm		5G AIQ length(mm)>30mm and <60mm		Rules(<1.5mm)
1.10531	AFE0_WF0_IN	78.03184	AFE1_WF0_IN	52.64774	1.36269
	AFE0_WF0_IP	77.80525	AFE1_WF0_IP	53.64854	
	AFE0_WF0_QN	78.91056	AFE1_WF0_QN	52.95861	
	AFE0_WF0_QP	78.53195	AFE1_WF0_QP	52.28585	
0.08415	AFE0_WF1_IN	76.48171	AFE1_WF1_IN	52.12263	1.36228
	AFE0_WF1_IP	76.44871	AFE1_WF1_IP	51.28576	
	AFE0_WF1_QN	76.40278	AFE1_WF1_QN	52.64804	
	AFE0_WF1_QP	76.39756	AFE1_WF1_QP	52.3459	
0.80533	AFE0_WF2_IN	79.57284	AFE1_WF2_IN	47.2266	1.45234
	AFE0_WF2_IP	79.08076	AFE1_WF2_IP	46.7937	
	AFE0_WF2_QN	78.76751	AFE1_WF2_QN	47.11768	
	AFE0_WF2_QP	78.78957	AFE1_WF2_QP	48.24604	
1.43542	AFE0_WF3_IN	77.07477	AFE1_WF3_IN	52.24313	1.43792
	AFE0_WF3_IP	76.92612	AFE1_WF3_IP	52.23279	
	AFE0_WF3_QN	76.11311	AFE1_WF3_QN	53.67071	
	AFE0_WF3_QP	77.54853	AFE1_WF3_QP	53.46186	

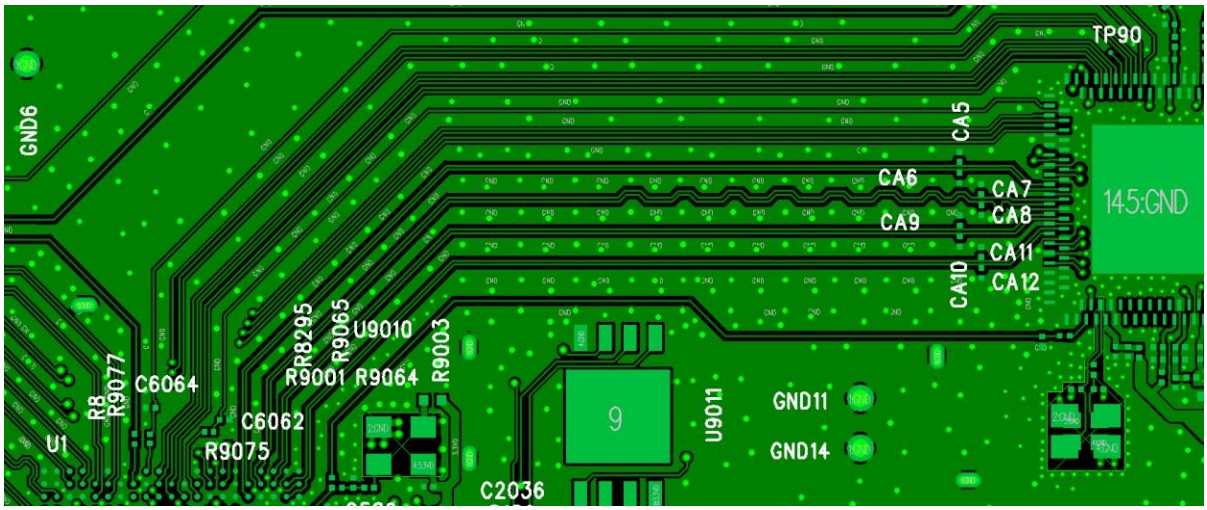


Fig 5-60 : A Band D die to A die Top layer layout

5.2.13 AFE WRI trace length control.

WF0/1_HB0~8 must control the same length the WF0 or WF1 group delta can't over 15mm (Timing around 100ps) highlighted in RED color. and HB0(CLK) need to add RC. Default values suggest to use 0R/4.7pF, for AX4200 HB0/HB0_B RC must add 4.7pF for WRI CLK.

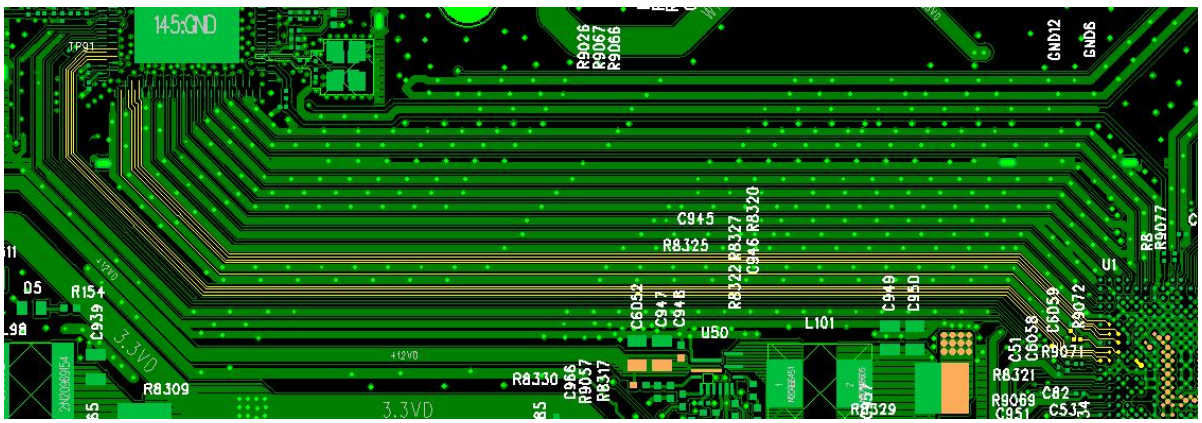


Fig 5-61 : WF0 WRI trace length delta check

MT7975			@ MT7915	@ Panther MT7986		MEMO
Function	Pin #	Pin Name	RFB (MTK2511)	2G (U10)	5G (U8)	
WRI	58	PAD_WF_HB8	PAD_WF_HB8	PAD_WF_HB8_2G	PAD_WF_HB8_5G	
WRI	59	PAD_WF_HB7	PAD_WF_HB7	PAD_WF_HB7_2G	PAD_WF_HB7_5G	
WRI	60	PAD_WF_HB6	PAD_WF_HB6	PAD_WF_HB6_2G	PAD_WF_HB6_5G	
WRI	61	PAD_WF_HB5	PAD_WF_HB5	PAD_WF_HB5_2G	PAD_WF_HB5_5G	
WRI	62	PAD_WF_HB4	PAD_WF_HB4	PAD_WF_HB4_2G	PAD_WF_HB4_5G	
WRI	63	PAD_WF_HB3	PAD_WF_HB3	PAD_WF_HB3_2G	PAD_WF_HB3_5G	
WRI	64	PAD_WF_HB2	PAD_WF_HB2	PAD_WF_HB2_2G	PAD_WF_HB2_5G	
WRI	65	PAD_WF_HB0	PAD_WF_HB0	PAD_WF_HB0_2G	PAD_WF_HB0_5G	WRI CLK, Keep away from XTAL (Isolated with GND)
WRI	66	PAD_WF_HB1	PAD_WF_HB1	PAD_WF_HB1_2G	PAD_WF_HB1_5G	

Note: WRI CLK should be isolated with GND and reserve a RC close to MT7986.

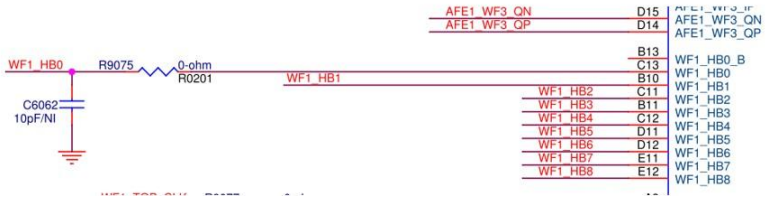


Fig 5-62 : WF0 HB0 is CLK keep other signal away

MT7975			@ MT7915	@ Panther MT7986		MEMO
Function	Pin #	Pin Name	RFB (MTK2511)	2G (U10)	5G (U8)	
SPI	27	PAD_TOP_CLK	PAD_TOP_CLK	PAD_TOP_CLK_2G	PAD_TOP_CLK_5G	SPI CLK (Isolated with GND)
SPI	28	PAD_TOP_DATA	TOP_DATA	PAD_TOP_DATA_2G	PAD_TOP_DATA_5G	

Note: SPI CLK should be isolated with GND and reserve a RC close to MT7986.

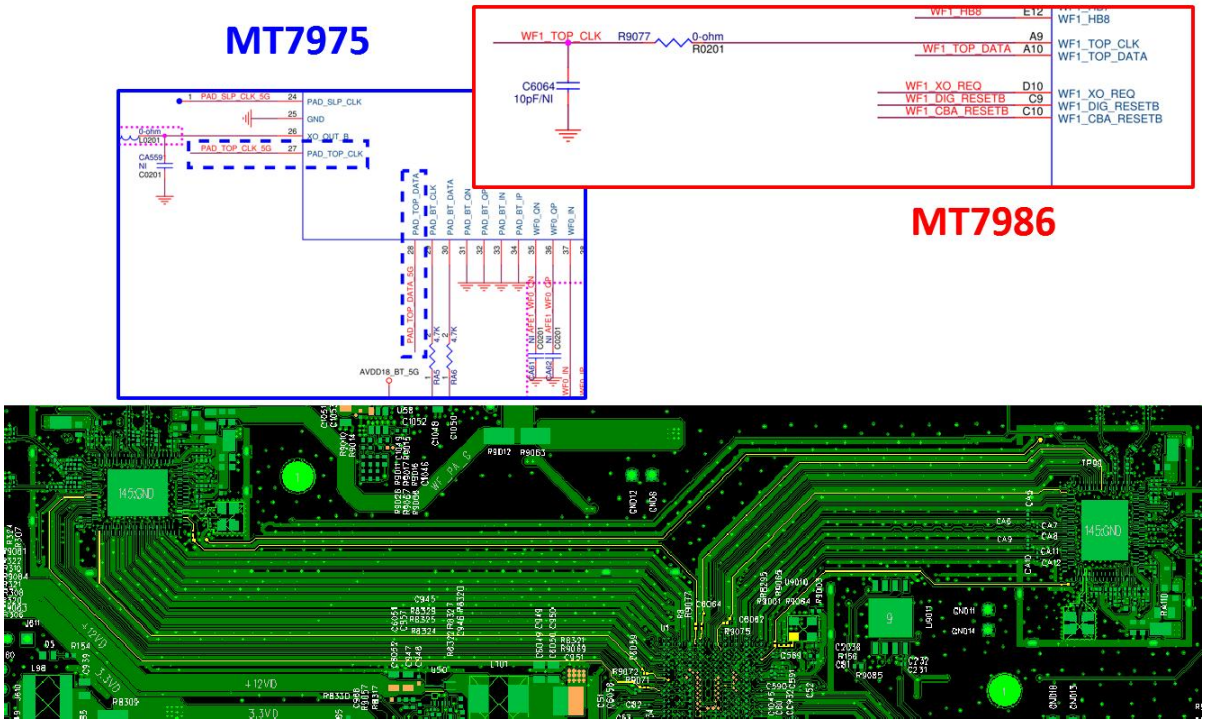


Fig 5-63 : WF0 TP_CLK (SPI CLK) reserve RC and keep other signal away

5.2.14 Heatsink and power consumption for thermal simulation

Please refer AN : MT7986B AX6000 Power Consumption and Thermal Report V1.0 -20210826.pdf for detail.

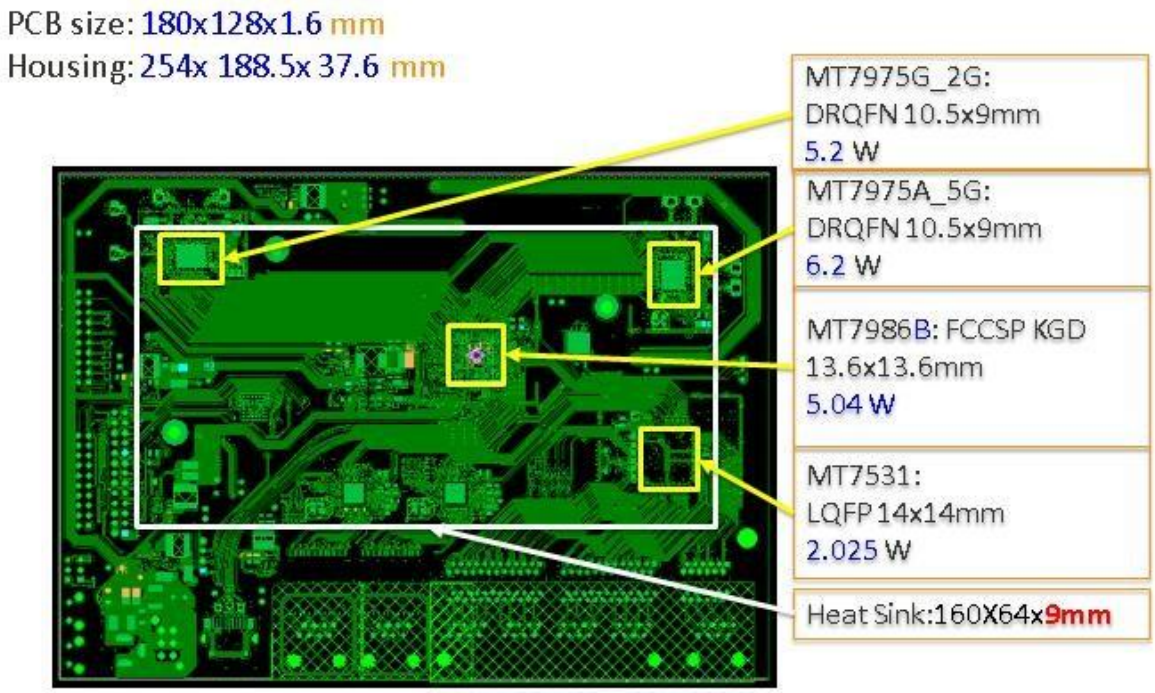


Fig 5-64: Heat sink and power consumption for thermal (iPAiLNA only)

5.2.15 MT7531 Crystal

The Xtal use wrong Part maybe cause IEEE802.3 compliant fail or package loss.
Xtal:

- The **25MHz DIP/SMD Xtal** designed for MT7531
  Xtal line trace/clearance = 4/4 mil, length 512.78 mil
- Each layer's signal & ground keep out area is shown below (L1/L2/L3/L4)
- The Xtal trace should be well GND shielding

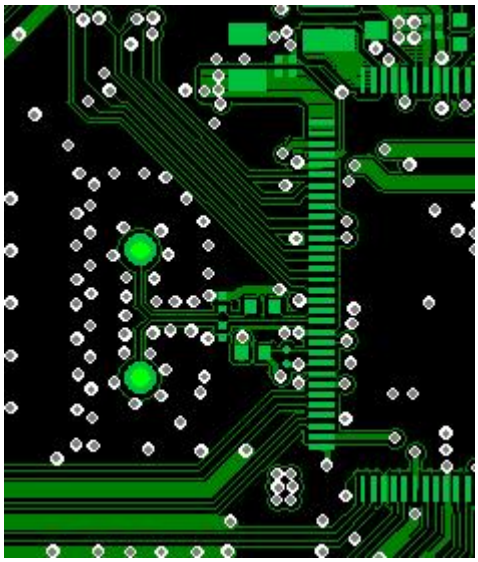


Fig 5-65: Crystal layout guidelines

5.2.16 A die XTAL and D die reference clk input

There are two reference CLK input from MT7975/MT7976 A die to MT7986B D die:

- The **40MHz Osc voltage should be 0.8V to 1.6V**
- Each layer's signal & ground keep out area is shown below (L1/L2/L3/L4)
- The OSC trace should be well GND shielding, at least two GND via space to AIQ signal.

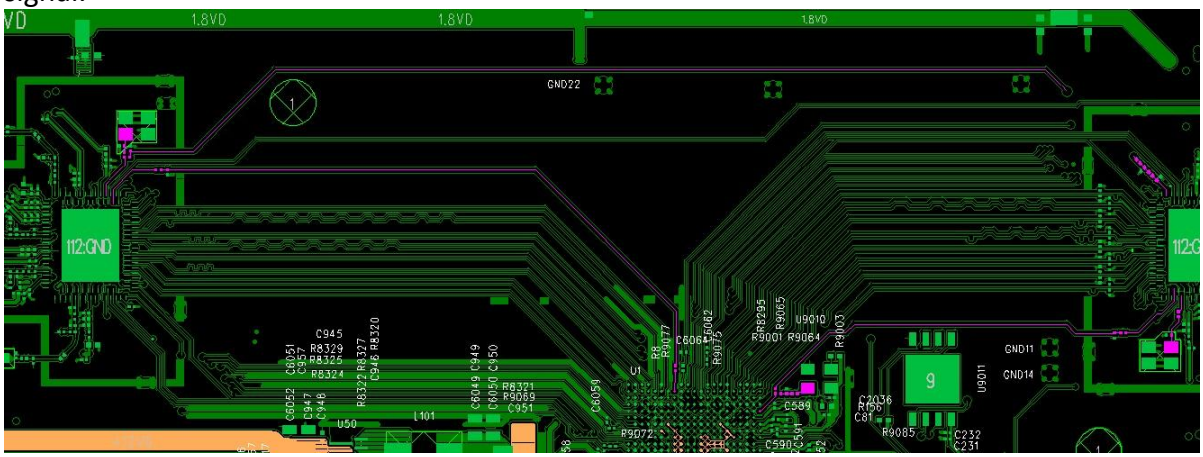


Fig 5-66: A Die CLK to D Die CLK guidelines

5.2.17 Flash Interface

There are 4 kinds flash support by MT7986B, SPIM-NOR, SPIM-NAND (ECC free), eMMC.

5.2.17.1.1 SPI Flash (SPI(M) NAND, SPI NOR)

For SPI CLK/Data Bus:

- Add a damping resistor on the SPI-CLK, and place it close to SPI-NAND device, and the damping R is recommended to be fined tuned by over/under-shoot waveform.
- The max recommended routing length of CLK/Data is 4000mil
- The difference of CLK/Data bus length ≦300mil
- ≦3 through holes on the CLK/Data bus
- SPI-CLK routing trace could be well protected with solid GND plane (option)

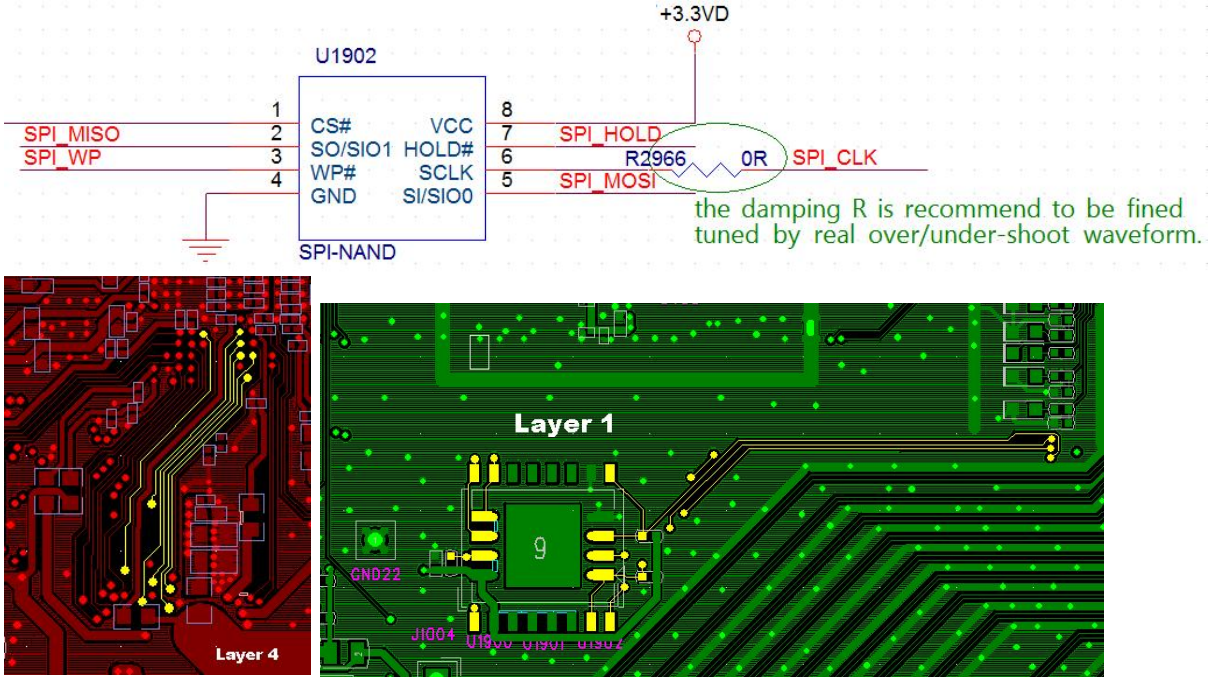


Fig 5-67 : SPI Flash layout guidelines

5.2.17.1.2 eMMC

MT7986B/C eMMC v4.5 only support 3.3V, share bus with SPI0/SPI1/PWM1, CLK **up to 50MHz**
MT7986A eMMC v5.1 work at 1.8V only,CLK up to 104MHz
Layout guide could follow eMMC design guide

- **Reserve Damping for eMMC CLK, if share pin with other IO.**
- 50-ohm impedance
- Mismatch within DAT0~DAT7 ≤ 250 mil
- CLK to DAT0-7 mismatch ≤ 250 mil

- CLK to CMD mismatch ≤ 250 mil
- CLK to RST_N mismatch ≤ 1000 mil

Signal space (H: H is the height of the dielectric between signal and GND (reference layer)

CLK >2H
DS >2H
CMD > 1.5H
RST_N >1.5H

Power/GND, Cap Number, follow eMMC design guide

5.2.18 Reserve shielding for Emission/De-sense

Please reserve shielding for Emission and De-sense consideration
Suggest AIQ/WRI/USB3.0/SGMII/PCIe layout to inner layer to get more sealed shielding cover.

Fig 5-68 : Reserve shielding example

6 PHY test commands

6.1 MT7531 Ethernet PHY test commands

6.1.1 10-T mode command

Example for Port 0
P0 MDI/MDIX
switch phy cl45 w 0 0x1e 0x145 0x5010;
switch phy cl45 w 0 0x1e 0x145 0x5018;

Port0
Normal:
switch phy cl22 w 0 31 0x0;
switch phy cl22 w 0 00 0x0100;
switch phy cl45 w 0 0x1e 0x145 0x5010;
switch phy cl45 w 0 0x1e 0x33 0x0177;

Random
switch phy cl22 w 0 31 0x0001;
switch phy cl22 w 0 29 0xf842;

Harmonic (Reboot)
switch phy cl22 w 0 31 0x0;
switch phy cl22 w 0 00 0x0100;
switch phy cl45 w 0 0x1e 0x145 0x5010;
switch phy cl45 w 0 0x1e 0x33 0x0177;
switch phy cl22 w 0 31 0x0001;
switch phy cl22 w 0 29 0xfe40;

6.1.2 100-Tx mode command

Below command X mean Port
switch phy cl22 w X 31 0x0;
switch phy cl22 w X 0 0x2100;
switch phy cl45 w X 0x1e 0x145 0x5010;

Example Port0

MDI
switch phy cl22 w 0 31 0x0;
switch phy cl22 w 0 0 0x2100;

switch phy cl45 w 0 0x1e 0x145 0x5010;

MDIX
switch phy cl22 w 0 31 0x0;
switch phy cl22 w 0 0 0x2100;
switch phy cl45 w 0 0x1e 0x145 0x5018;

6.1.3 1G mode mode command

Example for Port 0
1000 test mode1
switch phy cl22 w 0 31 0x0;
switch phy cl22 w 0 0 0x0140;
switch phy cl22 w 0 9 0x2600;

1000 test mode2
switch phy cl22 w 0 31 0x0;
switch phy cl22 w 0 0 0x0140;
switch phy cl22 w 0 9 0x4600;

1000 test mode3
switch phy cl22 w 0 31 0x0;
switch phy cl22 w 0 0 0x0140;
switch phy cl22 w 0 9 0x6600;

1000 test mode4
switch phy cl22 w 0 31 0x0;
switch phy cl22 w 0 0 0x0140;
switch phy cl22 w 0 9 0x8600;

6.2 2.5G PHY read/write and test commands

6.2.1 Read command

Example read 2.5G PHY ID (CL22)
mii_mgr -g -p 5 -r 2
mii_mgr -g -p 6 -r 2

6.2.2 Write command

Set: mii_mgr_cl45 -s -p [port number] -d [dev number] -r [register number] -v [value]
Example:

# mii_mgr -g -p 6 -r 0 Get:
phy[6].reg[0] = 3040
# mii_mgr -s -p 6 -r 0 -v B040
Set: phy[6].reg[0] = b040

6.2.3 2.5G Ethernet PHY compliant test command

6.2.3.1 2.5GBASE-T IEEE802.3 compliant test command

Base on IEEE 802.3 CL45 test register to set 10GBASE-T test command as below, if any test issue, please contact Ethernet PHY vendor for support.
Set: mii_mgr_cl45 -s -p [port number] -d [dev number] -r [register number] -v [value]

Table 45–51—10GBASE-T test mode register bit definitions

Bit(s)	Name	Description	R/W[a]
1.132.15:13	Test mode control	15 14 13 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal operation	R/W
1.132.12:10	Transmitter test frequencies	12 11 10 1 1 1 = Reserved 1 1 0 = Dual tone 5 1 0 1 = Dual tone 4 1 0 0 = Dual tone 3 0 1 1 = Reserved 0 1 0 = Dual tone 2 0 0 1 = Dual tone 1 0 0 0 = Reserved	R/W
1.132.9:0	Reserved	Value always 0, writes ignored	RO

[a]R/W = Read/Write

802.3 register back up for MultiGBASE-T1 (802.3 Claude 149 include 2.5G, 5G, 10GBaseT1)

Table 45-155e MultiGBASE-T1 test mode control register bit definitions

Bits(s)	Name	Description	R/W[a]
1.2313.15:13	Test mode control	15 14 13 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Reserved 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W
1.2313.12:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write

2.5G command P5
Test mode 2 : mii_mgr_cl45 -s -p 0x5 -d 1 -r 84 -v 4000
Test mode 4 tone 1 : mii_mgr_cl45 -s -p 0x5 -d 0x1 -r 0x84 -v 0x8400
Test mode 4 tone 2 : mii_mgr_cl45 -s -p 0x5 -d 0x1 -r 0x84 -v 0x8800
Test mode 4 tone 3 : mii_mgr_cl45 -s -p 0x5 -d 0x1 -r 0x84 -v 0x9000
Test mode 4 tone 4 : mii_mgr_cl45 -s -p 0x5 -d 0x1 -r 0x84 -v 0x9400
Test mode 4 tone 5 : mii_mgr_cl45 -s -p 0x5 -d 0x1 -r 0x84 -v 0x9800
Test mode 5 : mii_mgr_cl45 -s -p 0x5 -d 0x1 -r 0x84 -v 0xa000
Test mode 6 : mii_mgr_cl45 -s -p 0x5 -d 0x1 -r 0x84 -v 0xc000
Test mode 7 : mii_mgr_cl45 -s -p 0x5 -d 0x1 -r 0x84 -v 0xe000
Test mode (1 & 3):
Test mode 3 command:
- Master GPY211 Device set at test mode 1:
mii_mgr_cl45 -s -p 0x5 -d 0x7 -r 0x20 -v 0xc0a2
mii_mgr_cl45 -s -p 0x5 -d 0x1 -r 0x84 -v 0x2000
- Slave DUT set at test mode 3:
mii_mgr_cl45 -s -p 0x5 -d 0x7 -r 0x20 -v 0x80a2
mii_mgr_cl45 -s -p 0x5 -d 0x1 -r 0x84 -v 0x6000

2.5G command P6
Test mode 2 : mii_mgr_cl45 -s -p 0x6 -d 1 -r 84 -v 4000
Test mode 4 tone 1 : mii_mgr_cl45 -s -p 0x6 -d 0x1 -r 0x84 -v 0x8400
Test mode 4 tone 2 : mii_mgr_cl45 -s -p 0x6 -d 0x1 -r 0x84 -v 0x8800
Test mode 4 tone 3 : mii_mgr_cl45 -s -p 0x6 -d 0x1 -r 0x84 -v 0x9000
Test mode 4 tone 4 : mii_mgr_cl45 -s -p 0x6 -d 0x1 -r 0x84 -v 0x9400
Test mode 4 tone 5 : mii_mgr_cl45 -s -p 0x6 -d 0x1 -r 0x84 -v 0x9800
Test mode 5 : mii_mgr_cl45 -s -p 0x6 -d 0x1 -r 0x84 -v 0xa000
Test mode 6 : mii_mgr_cl45 -s -p 0x6 -d 0x1 -r 0x84 -v 0xc000
Test mode 7 : mii_mgr_cl45 -s -p 0x6 -d 0x1 -r 0x84 -v 0xe000
Test mode (1 & 3):
Test mode 3 command:
- Master GPY211 Device set at test mode 1:
mii_mgr_cl45 -s -p 0x6 -d 0x7 -r 0x20 -v 0xc0a2
mii_mgr_cl45 -s -p 0x6 -d 0x1 -r 0x84 -v 0x2000
- Slave DUT set at test mode 3:
mii_mgr_cl45 -s -p 0x6 -d 0x7 -r 0x20 -v 0x80a2
mii_mgr_cl45 -s -p 0x6 -d 0x1 -r 0x84 -v 0x6000

6.2.3.2 1000BASE-T IEEE802.3 compliant test command

Below command follow IEEE 802.3 CL22 register 9 to set 1GBASE-T test command.

1000M Test Mode:

Test Mode 1 => Template, Peak Voltage and Droop
Test Mode 2 => Master Clock Jitter
Test Mode 3 => Slave Clock Jitter
Test Mode 4 => Distortion, Return Loss and Common Mode

1000M Command: (PHY address 5)
Test mode 1 - mii_mgr -s -p 0x5 -r 0x9 -v 0x2300
Test mode 2 - mii_mgr -s -p 0x5 -r 0x9 -v 0x4300
Test mode 3 - mii_mgr -s -p 0x5 -r 0x9 -v 0x6300
Test mode 4 - mii_mgr -s -p 0x5 -r 0x9 -v 0x8300

1000M Command: (PHY address 6)
Test mode 1 - mii_mgr -s -p 0x6 -r 0x9 -v 0x2300
Test mode 2 - mii_mgr -s -p 0x6 -r 0x9 -v 0x4300
Test mode 3 - mii_mgr -s -p 0x6 -r 0x9 -v 0x6300
Test mode 4 - mii_mgr -s -p 0x6 -r 0x9 -v 0x8300

6.3 USB3 TX compliance test SOP

6.3.1 U3 TX Compliance Test Item

U3 driver default disable CTS mode，it need to set below register to enable CTS mode to test TX compliance. Enable CTS mode setting: set 0x11200420 to 0x10340
regs w 0x11200420 0x10340

6.4 USB 2.0 TX compliance test SOP

6.4.1 USB 2.0 background information

MT7986 can support 2 USB 2.0 High speed ports, and below are register layout information.

port	offset	bank
u2 port0	0x0000	MISC
	0x0100	FMREG
	0x0300	U2PHY_COM
u3 port0	0x0700	SPLLC
	0x0800	CHIP
	0x0900	U3PHYD
	0x0a00	U3PHYD_BANK2
	0x0b00	U3PHYA
	0x0c00	U3PHYA_DA
u2 port1	0x1000	MISC
	0x1100	FMREG
	0x1300	U2PHY_COM
u3 port1	0x1700	SPLLC
	0x1800	CHIP
	0x1900	U3PHYD
	0x1a00	U3PHYD_BANK2

```
                    0x1b00    U3PHYA
                    0x1c00    U3PHYA_DA
          u2 port2  0x2000    MISC
                    0x2100    FMREG
                    0x2300    U2PHY_COM
```

6.4.2 Software programming

Enable xHCI USB 2.0 toolkits (Please check Software Engineer)

CONFIG_USB_XHCI_MTK_DEBUGFS=y
CONFIG_DEBUG_FS=y

6.4.3 What parameters to xHCI eye-pattern quality

Phy RG_USB20_VRT_VREF_SEL parameters

▪VRT reference voltage selection
Register:

11C21304 USBPHYACR1 U2PHYA Common 1 Register 00A44400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									RG_USB20_INTR_CAL					RG_USB20_OTG_VBUSTH		
Type									RW					RW		
Reset									1	0	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_USB20_VRT_VREF_SEL				RG_USB20_TERM_VREF_SEL			RG_USB20_MPX_SEL							
Type		RW				RW			RW							
Reset		1	0	0		1	0	0	0	0	0	0	0	0	0	0

Bit field:

14:12 RG_USB20_VRT_VREF_SEL

VRT reference voltage selection(share circuit)
000:700mV
001:720mV
010:740mV
011:760mV
100:770mV
101:780mV
110:800mV
111:820mV

Phy RG_USB20_TERM_VREF_SEL parameter

▪HS_TX TERM reference voltage selection
Register:

11C21304 USBPHYACR1 U2PHYA Common 1 Register 00A44400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									RG_USB20_INTR_CAL					RG_USB20_OTG_VBUSTH		
Type									RW					RW		
Reset									1	0	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_USB20_VRT_VREF_SEL				RG_USB20_TERM_VREF_SEL			RG_USB20_MPX_SEL							
Type		RW				RW			RW							
Reset		1	0	0		1	0	0	0	0	0	0	0	0	0	0

Bit field:

10:8 RG_USB20_TERM_VREF_SEL **HS_TX TERM reference voltage selection(share circuit)**

000:320mV
001:340mV
010:360mV
011:380mV
100:400mV
101:420mV
110:440mV
111:460mV

PHY RG_USB20_HSTX_SRCCTRL parameter

▪High speed slew rate control

Register:

11C21314 USBPHYACR5 U2PHYA Common 5 Register 00801000

Bit	31	30	29	28	27	26	25	24	23	22
Name	u2phy_reserve14			RG_USB20_DISC_FIT_EN	RG_USB20_INIT_SQ_EN_DG		RG_USB20_HSTX_TMODE_SEL		RG_USB20_SQD	
Type	RO			RW	RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6
Name	RG_USB20_HSTX_SRCAL_EN	RG_USB20_HSTX_SRCTRL			RG_USB20_HS_100U_U3_EN	RG_USB20_GBIAS_ENB			RG_USB20_DM_ABIST_SOURCE_EN	
Type	RW	RW			RW	RW			RW	
Reset	0	0	0	1	0	0			0	

Bit field:

14:12 RG_USB20_HSTX_SRCTRL **high speed slew rate control**

000: min rise time/fall time
111: max rise time/fall time

6.4.4 Eye-pattern parameter

To submit final your parameters tied in eye-pattern to *.dts file of your project

```
&u2port0 {
mediatek,eye-src = <0x04>;
mediatek,eye-vrt = <0x04>;
mediatek,eye-term = <0x07>;
```

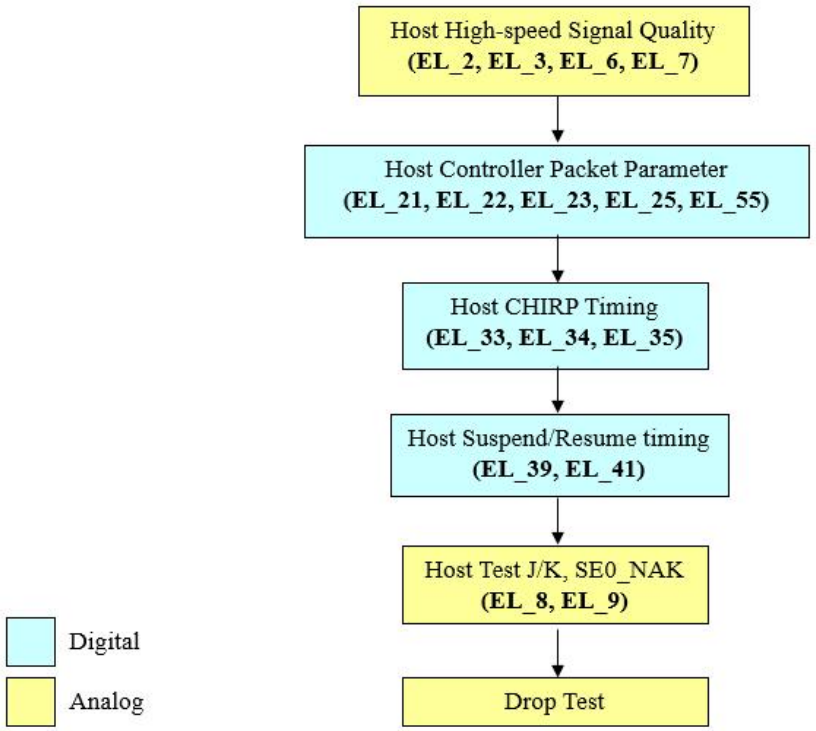
status = “okay”;
};

6.4.5 Software programming USB2.0 test

Enable xHCI USB 2.0 toolkits (Please check Software Engineer)

CONFIG_USB_XHCI_MTK_DEBUGFS=y
CONFIG_DEBUG_FS=y

6.4.6 USBIF compliance Test



6.4.6.1 Host High-speed Signal Quality (EL_2, EL_3, EL_6, EL_7)

CLI: echo -n test.packet 3 >/sys/devices/platform/11200000.xhci/hqa
//U3 connector (U3+U2)
CLI: echo -n test.packet 2 > /sys/devices/platform/11200000.xhci/hqa
//U2 connector (U2 only), MT7986A only

6.4.6.2 Host Controller Packet Parameter (EL_21, EL_22, EL_23, EL_25, EL_55)

CLI: echo -n test.getdesc 3 > /sys/devices/platform/11200000.xhci/hqa
//U3 connector (U3+U2)
CLI: echo -n test.getdesc 2 > /sys/devices/platform/11200000.xhci/hqa
//U2 connector (U2 only), MT7986A only

6.4.6.3 Host CHIRP Timing (EL_33, EL_34, EL_35)

CLI: echo –n test.enumbus 3 > /sys/devices/platform/11200000.xhci/hqa
//U3 connector (U3+U2)
CLI: echo –n test.enumbus 3 > /sys/devices/platform/11200000.xhci/hqa
//U2 connector (U2 only), MT7986A only

6.4.6.4 Host Suspend/Resume timing (EL_39, EL_41)

CLI (suspend): echo -n test.suspend 3 >/sys/devices/platform/11200000.xhci/hqa
//U3 connector (U3+U2)
CLI (suspend): echo -n test.suspend 2 >/sys/devices/platform/11200000.xhci/hqa
//U2 connector (U2 only), MT7986A only

CLI (resume): echo -n test.resume 3 > /sys/devices/platform/11200000.xhci/hqa
//U3 connector (U3+U2)
CLI (suspend): echo -n test.resume 2 >/sys/devices/platform/11200000.xhci/hqa
//U2 connector (U2 only), MT7986A only

6.4.6.5 Host Test J/K, SE0_NAK (EL_8, EL_9)

CLI (J): echo -n test.j 3 > /sys/devices/platform/11200000.xhci/hqa
//U3 connector (U3+U2)
CLI (J): echo -n test.j 2 > /sys/devices/platform/11200000.xhci/hqa
//U2 connector (U2 only), MT7986A only

CLI (K): echo -n test.k 3 > /sys/devices/platform/11200000.xhci/hqa
//U3 connector (U3+U2)
CLI (K): echo -n test.k 2 > /sys/devices/platform/11200000.xhci/hqa
//U2 connector (U2 only), MT7986A only

CLI (SE0): echo -n test.se0 3 > /sys/devices/platform/11200000.xhci/hqa
//U3 connector (U3+U2)
CLI (SE0): echo -n test.se0 2 > /sys/devices/platform/11200000.xhci/hqa
//U2 connector (U2 only), MT7986A only

6.4.6.6 Drop Test

CLI: none

Refer USB Specification as below link:
USB Electrical Compliance Specification v1.07.pdf
https://usb.org/sites/default/files/USB%202%200%20Electrical%20Compliance%20Specification%28v1.07%29.pdf

6.5 (H)SGMII command

6.5.1 (H)SGMII SSC

HSGMII SSC driver default is disable, Customer can use below command to enable SSC mode to compare RF de-sense or EMI.

MT7531 SSC enable command
Port 6(default is for CPU port)
switch reg w 6110 40000000;
switch reg w 6100 120044f;

Port 5
switch reg w 5110 40000000;
switch reg w 5100 120044f;

MT7986 SSC enable command
HSGMII0
regs w 0x10060110 0x40002000;
//2000 -- >bit 30 -- >1 40002000
regs w 0x10060100 0x12B484F;
//010b484f bit 21 -->1, 12B484F

HSGMII1
regs w 0x10070110 0x40002000;
regs w 0x10070100 0x12B484F;

6.5.2 (H)SGMII 2.5G/1G force change command

HSGMII default data rate is 2.5G (baud rate 3.125Gbps),

MT7986
SG1 force 2.5G (gen2)
regs w 100700e8 10
regs w 10070128 14817

```
regs w 10070020 31120019
regs w 10070000 140
regs w 100700e8 0

#
# SG1 force 1G (gen1)
regs w 100700e8 10
regs w 10070128 14813
regs w 10070020 31120019
regs w 10070000 140
regs w 100700e8 0

# SG0 force 2.5G (gen2)
regs w 100600e8 10
regs w 10060128 14817
regs w 10060020 31120019
regs w 10060000 140
regs w 100600e8 0

#
# SG0 force 1G (gen1)
regs w 100600e8 10
regs w 10060128 14813
regs w 10060020 31120019
regs w 10060000 140
regs w 100600e8 0

MT7531A Switch register
# port5
# force SGMII 2.5G
switch reg w 50e8 10
switch reg w 5128 14817
switch reg w 5020 31120009
switch reg w 5000 140
switch reg w 50e8 0
# force SGMII 1G
switch reg w 50e8 10
switch reg w 5128 14813
switch reg w 5020 31120009
switch reg w 5000 140
switch reg w 50e8 0
```

```
# port6
# force 2.5G
switch reg w 60e8 10
switch reg w 6128 14817
switch reg w 6020 31120009
switch reg w 6000 140
switch reg w 60e8 0

# force SGMII 1G
switch reg w 60e8 10
switch reg w 6128 14813
switch reg w 6020 31120009
switch reg w 6000 140
switch reg w 60e8 0
```

6.5.3 (H)SGMII Package Gen for eye pattern

HSGMII default data rate is 2.5G (baud rate 3.125Gbps, use standard XAUI spec. Please refer HQA report for spec, below is package gen command and register.

```
MT7531
# port5
switch reg w 50c4 xxxxxxxx
# port6
switch reg w 60c4 xxxxxxxx
MT7986
SGMII0
regs w 100600C4 xxxxxxxx
SGMII1
regs w 100700C4 xxxxxxxx
```

- PRBS7 or UDP_DATA (User Defined Pattern)

000050C4 PAT_GEN_CTRL_0 Pattern Gen control_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UDP_DATA_15_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								BIST_ERR	BIST_RUN	BIST_OK	PRBS_INJERR	RENEW_MODE	PRBS_MODE		PRBS_CHECK	PRBS_EN
Type								RO	RO	RO	RW	RW	RW		RW	RW
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	UDP_DATA_15_0	User define pattern [15:0]
8	BIST_ERR	BIST Error flag (error bit received)
7	BIST_RUN	BIST Run flag (Pattern generate and check period)
6	BIST_OK	BIST OK flag (no error bit received)
5	PRBS_INJERR	PRBS pattern error bits injection 1'b0 : TX send PRBS pattern normally 1'b1 : TX send specific pattern 20'h5a5a5
4	RENEW_MODE	Mode of Next PRBS golden pattern generation for check 1'b0 : using first RX data to polynomial LFSR 1'b1 : using every RX data to polynomial LFSR
3:2	PRBS_MODE	Type of pattern for generation 2'b00 : PRBS-7 2'b01 : User define pattern 2'b10 : Clock pattern 2'b11 : No used
1	PRBS_CHECK	Start to calculate PRBS error count enable 1'b0 : no active 1'b1 : active
0	PRBS_EN	Pattern Gen enable 1'b0 : disable 1'b1 : enable

MT7531 register, MT7986 offset different

000050C8 PAT_GEN_CTRL_1 Pattern Gen control_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UDP_DATA_47_16															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UDP_DATA_47_16															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	UDP_DATA_47_16	User define pattern [47:16]

000050CC PAT_GEN_CTRL_2 Pattern Gen control_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UDP_DATA_79_48															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UDP_DATA_79_48															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	UDP_DATA_79_48	User define pattern [79:48]

000050D0 PAT_GEN_CTRL_3 Pattern Gen control_3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIST_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.6 MT7986 Thermal sensor ADC command

//Read MT7986 CPU temperature
cat sys/class/thermal/thermal_zone0/temp
example read value is 58222, it means junction temperature around 58.222 ℃.
//check eFuse value
regs d 11D00274 // dump value 0 mean eFuse no value

6.7 CPU core disable command example

//Disable cpu core 1~3
echo 0 > /sys/devices/system/cpu/cpu1/online
echo 0 > /sys/devices/system/cpu/cpu2/online
echo 0 > /sys/devices/system/cpu/cpu3/online

6.8 CPU Full Loading command

//memory test command, command enter 4 times for CPU 100 percent loading.
memtester 10M &
//check CPU loading command
mpstat 2 -P ALL

6.9 WIFI radio off and TX power percentage command

```
//Radio off.
iwpriv ra0 set RadioOn=0
iwpriv rax0 set RadioOn=0

//Tx power percentage, example for 5G 80%.
iwpriv rax0 set PercentageCtrl=1
iwpriv rax0 set PowerDropCtrl=80
```

6.10 GPIO/ WF5F_LED/WF2F_LED on/off command example

```
//Set GPIO PINMUX
regs w 0x1001F300 0
//Set GPIO1/2 //WF2G_LED and WF5G_LED ON
regs w 0x1001F004 0x6
//Clear GPIO1/2 WF2G_LED and WF5G_LED OFF
regs w 0x1001F008 0x6
```

6.11 PWM command at Uboot example

Before test PWM, please ask software engineer to enable following configs in u-boot menuconfig.

```
+CONFIG_CMD_PWM=y
+CONFIG_DM_PWM=y
+CONFIG_PWM_MTK=y

pwm - control pwm channels

Usage:
pwm invert <pwm_dev_num> <channel> <polarity> - invert polarity
pwm config <pwm_dev_num> <channel> <period_ns> <duty_ns> - config PWM
pwm enable <pwm_dev_num> <channel> - enable PWM output
pwm disable <pwm_dev_num> <channel> - eisable PWM output

Example for blink LEDs
MT7986> pwm config 0 0 1000000000 500000000
MT7986> pwm enable 0 0
MT7986> pwm config 0 1 1000000000 500000000
MT7986> pwm enable 0 1

In MT7986, please set <pwm_dev_num> to 0, set <channel> according pwm0 / pwm1
```

7 MT7986 Qualified Vendor List (QVL) Table

7.1 Introduction

This document describes the MT7986 qualified Crystals, DDRs and all types of flash memory that MT7986 SDK support. The DDR type is including DDR3(x16), DDR4 (x16). The Flash type is including Serial NOR, SPIM-NAND, and eMMC. Customers are strongly recommended to design in with those parts that have been qualified by MTK. QVL list in this document will not keep to update, please visit MOL/QVL for the latest QVL list.

Website:
http://online.mediatek.inc/qvl/_layouts/15/mol/qvl/ext/QVLHomeExternal.aspx

7.2 OSC spec and Xtal QVL

MT7986 support 40MHz OSC source from MT7976 and MT7975 (Clock out to MT7986 the clock source guarantee by MTK, it doesn't need to measure Clock quality, MTK fully did stress test already)

External oscillator only for no-A-die (no MT7976 or MT7975)
External OSC spec table as below table.

item	Vlaue		Unit
	Min	Max	
Clock frequency	40	40	MHz
Frequency deviation	+0	+50	ppm
Skew			ps
Duty cycle	45	55	%
Rising Time (Tr)		1000	ps
Falling time (Tf)		1000	ps
Jitter rms		0.15	ps
Jitter pk-pk			ps
input high voltage	0.8	1.9	V
input low voltage	-0.3	0.3	V

Table7 -1 OSC Spec Table

OSC part MTK test as below (only check mini HQA)
TST/ TW0473E, Siward/SCO-H586_OSC81, with 150/100 ohm as voltage divider (please check HDK).

1. Verify POR @-40 and 80 degree C with Corner Chip SS/FF 4pcs, cold start to boot and ethernet ping function (DDR/Flash read, SGMII ping)
2. USB/PCIe eye SI check okay.

MT7976 and MT7975 Xtal spec as below

Item	MT7975	MT7976
Nominal Frequency	40MHz	40MHz
Size	3.2mmx2.5mm	3.2mmx2.5mm
Operating Temperature Range	-40°C to +125°C	-40°C to +105°C
Frequency Tolerance (FL)	+/- 7 ppm @ 25°C +/- 3°C	+/- 7 ppm @ 25°C +/- 3°C
Frequency Stability over Operating Temperature	+/- 20 ppm (referred to the value at 25°C) -40°C to +100°C	+/- 15 ppm (referred to the value at 25°C) -40°C to +100°C
	+/- 10 ppm (referred to the value at 25°C) 100°C to +105°C	+/- 20 ppm (referred to the value at 25°C) 100°C to +105°C
Equivalent Series Resistance (ESR)	30 Ω max.	15 Ω max.
Drive Level(DL)	100uW max	400uW max
Shunt Capacitance (Co)	3.0 pF max	3.0 pF max
Load Capacitance (CL)	11pF	10 pF
Trim Sensitivity Over Load(Ts)	No this information	10~13 ppm/pF

QVL list, please check MOL

MOL Website:
http://online.mediatek.inc/qvl/_layouts/15/mol/qvl/ext/QVLHomeExternal.aspx

7.3 SPI2 Serial NOR Flash memory (3.3V only)

MT7986B SPI NOR Flash QVL will separate phase1, Phase2, Phase3 to release. Below table only list phase 1 QVL. If you want use other Flash source, please contact software Engineer for support. This document will not keep to update, the final update, please visit

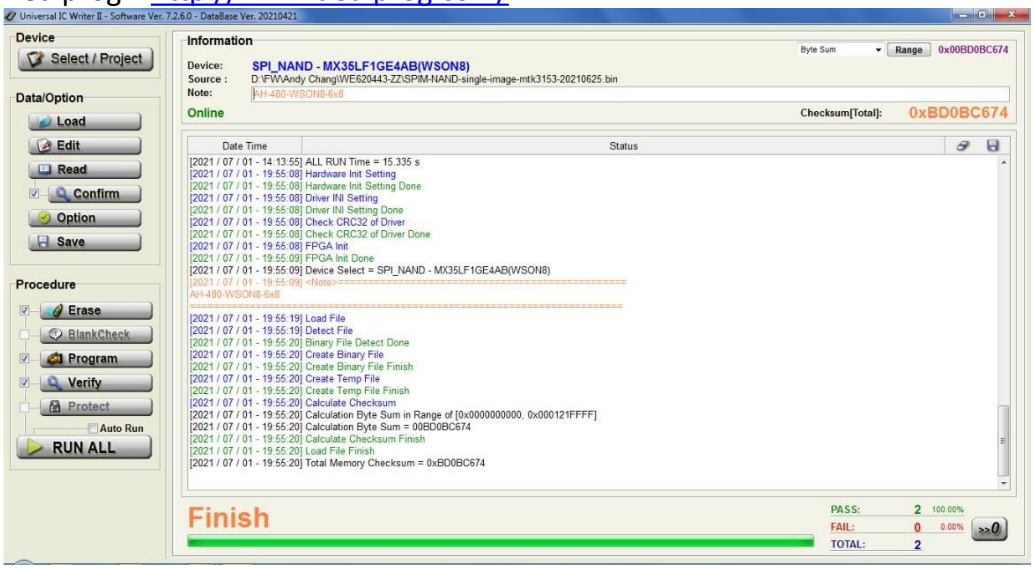
Website:
http://online.mediatek.inc/qvl/_layouts/15/mol/qvl/ext/QVLHomeExternal.aspx

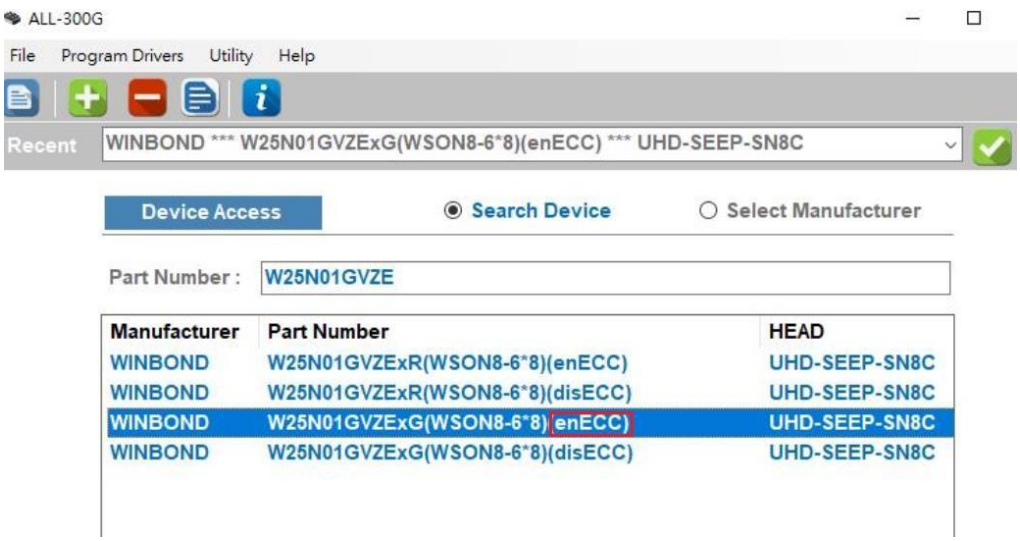
Vendor	Part Number	Density	Package	QVL Plan
MXIC	MX25L12833F (RFB on board)	128Mbit	SOP-8	Phase1
MXIC	MX25L25745G (4B)	256Mbit	SOP-16	Phase1
MXIC	MX25L25645G	256Mbit	SOP-16	PASS
MXIC	MX25L51245G	512Mbit	SOP-16	PASS
Winbond	W25Q128JV (RFB on board)	128Mbit	SOP-8	PASS
Winbond	W25Q256JV	256Mbit	SOP-16/WSON8	Phase1
Winbond	W25M512JV	512Mbit	SOP-16/WSON8	PASS
GigaDevice	GD25Q128E	128Mbit	SOP-8	PASS
ESMT	EN25QH256A	256Mbit	SOP-16	PASS
Cypress/Infineon	S25FL256LAGMFI000	256Mbit		PASS

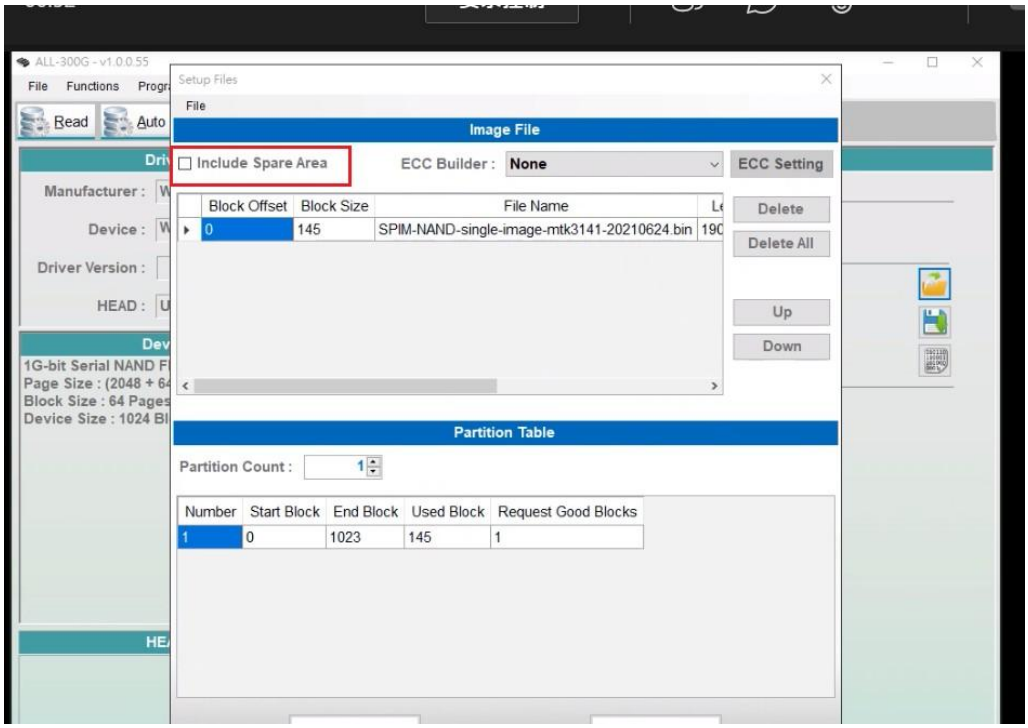
Table 7-2 SPI Nor Flash QVL Table

7.4 SPI2(SPIM)-NAND Flash (3.3V only)

SPI2(SPIM)-NAND boot doesn't support Host ECC, SPI2(SPIM)-NAND support Flash ECC, the ECC algorithm depended on flash. Some of Flash can't be used for this interface, example MX35LF1G24AD-Z4I, It doesn't need convert image files by **MTK BCH tool**.
For programmer, select the part doesn't need to include Spare Area, MUST enable ECC.
Reference programmer:
Dediprog http://www.dediprog.com/







Below table only list SPI-NAND QVL test pass and phase 1 test plan list. If you want use other Flash source, please contact software Engineer for support. This document will not keep updating, the final release, please visit

Website:
http://online.mediatek.inc/qvl/_layouts/15/mol/qvl/ext/QVLHomeExternal.aspx

Vendor	Part Number	Density	Uboot	QVL test	Note
Winbond	W25N01GVZEIG (RFB on board)	1Gbit		PASS	
Winbond	W25N02KVZEIR	2Gbit		PASS	
Gigadevice	GD5F1GQ5UEYIG	1Gbit		PASS	
Gigadevice	GD5F1GQ5UEYIH	1Gbit		PASS	
Gigadevice	GD5F2GQ5UEYIH	2Gbit		PASS	
MXIC	MX35LF1GE4AB-Z4I (RFB on board)	1Gbit		PASS	
MXIC	MX35LF2GE4AD-Z4I	2Gbit		PASS	
MXIC	MX35LF4GE4AD-Z4I	4Gbit	yes	Phase 1	
ESMT	F50L1G41LB-104YG2ME	1Gbit		PASS	
ESMT	F50L2G41KA-104YIG2V	2Gbit		PASS	
ESMT	F50L4G41XB-104RAG2X	4Gbit		PASS	
KIOXIA	TC58CVG1S3HRAIG	2Gbit		PASS	

Table 7-3 SPIM-NAND QVL Table

7.5 eMMC Flash Memory

MT7986A only support 1.8V eMMC NAND Flash memory, and MT7986B/C only support 3.3V eMMC v4.5 NAND Flash memory, QVL part use 8 bit data and compatible with

eMMC 4.5 above. Below table only list QVL pass and phase 1 test plan. If you want use other eMMC Flash source, please contact software Engineer for support. This document will not keep updating, the final release, please visit

Website:
http://online.mediatek.inc/qvl/_layouts/15/mol/qvl/ext/QVLHomeExternal.aspx

The Phase1 QVL table as below

Vendor	Part Number	MT7986A (1.8V)	MT7986B/C (3.3V)	Package	Density	Note
KIOXIA	THGBMNG5D1LBAIL	eMMC v5.1, not test	eMMC v4.5, not test	BGA-153	4GB	Phase 1
KIOXIA	THGBMJG6C1LBAIL	eMMC v5.1, PASS	eMMC v4.5, not test	BGA-153	8GB	
KIOXIA	THGAMRG7T13BAIL	eMMC v5.1, PASS	eMMC v4.5, not test	BGA-153	16GB	
~~MXIC*~~	~~MX52LM04A11XSI~~	~~eMMC v5.1, FAIL~~	~~eMMC v4.5, FAIL~~	~~153BGA~~	~~4GB~~	~~Phase 1~~
~~MXIC*~~	~~MX52LM08A11XVI~~	~~eMMC v5.1, FAIL~~	~~eMMC v4.5, FAIL~~	~~153BGA~~	~~8GB~~	~~Phase 1~~
Samsung	KLM8G1GETF-B041	eMMC v5.1, PASS	eMMC v4.5, not test	BGA-153	8GB	
Samsung	KLMAG1JETD-B041	eMMC v5.1, PASS	eMMC v4.5, not test	BGA-153	16GB	

Table 7-4 eMMC Flash QVL Table

7.6 DDR3 QVL

MT7986A support external DDR3, QVL Qualify status as below table:

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Website:
http://online.mediatek.inc/qvl/_layouts/15/mol/qvl/ext/QVLHomeExternal.aspx

Vendor	Vendor P/N	RAM Type	RAM Size	Qualify Status	MOL Publish Status
Nanya	NT5CB256M16ER-FLI	DDR3-2133	256Mx16bit=4Gb	PASS	Publish
Nanya	NT5CB128M16JR-FLI	DDR3-2133	128Mx16bit=2Gb	PASS	Publish
Winbond	W634GU6QB-09I	DDR3-2133	256Mx16bit=4Gb	PASS	Publish
Winbond	W632GG6NB-09	DDR3-2133	128Mx16bit=2Gb	PASS	Publish
Winbond	W632GG6QB-09I	DDR3-2133	128Mx16bit=2Gb	Corner test okay	SI on going, 2022/4/E
ESMT	M15T4G16256A-EFBIG2S	DDR3-2133	256Mx16bit=4Gb	PASS	Publish
ESMT	M15T2G16128A-EFBIG2R	DDR3-2133	128Mx16bit=2Gb	PASS	Publish
ETRON	EM6GE16EWAKG-09H	DDR3-2133	256Mx16bit=4Gb	PASS	Publish
ETRON	EM6GD16EWBH-09G	DDR3-2133	128Mx16bit=2Gb	PASS	Publish

Table 7-5 DDR3 QVL Table

7.7 DDR4-3200 QVL

MT7986A support external DDR4, Plan QVL table as below:

This document will not keep updating, the final QVL release, please visit Website:
http://online.mediatek.inc/qvl/_layouts/15/mol/qvl/ext/QVLHomeExternal.aspx

Vendor	Vendor P/N	RAM Size	Note	Validation Speed	MOL Publish Status
Samsumg	K4AAG165WA-BCWE**	1GBx16Bit=16Gb		DDR4-3200	Publish
Samsumg	K4A8G165WC-BIWE**	512MBx16bit=8Gb		DDR4-3200	Publish
Samsumg	K4A4G165WF-BCWE**	256MBx16Bit=4Gb		DDR4-3200	Publish
Micron	MT40A1G16KD-062E:E	1GBx16Bit=16Gb		DDR4-3200	Publish
Micron	MT40A512M16TB-062E:R	512MBx16bit=8Gb		DDR4-3200	Publish
Hynix	H5AN8G6NDJR-XNC	512MBx16bit=8Gb		DDR4-3200	Publish
Nanya	NT5AD512M16C4-JR	512MBx16bit=8Gb		DDR4-3200	Publish
Nanya	NT5AD256M16E4-JRI	256MBx16Bit=4Gb		DDR4-3200	Publish 2022/4/13
Nanya	NT5AD256M16E4-JR	256MBx16Bit=4Gb		DDR4-3200	Publish 2022/4/13
ESMT	M16U4G16256A-QLBIG2Z*	256MBx16Bit=4Gb	Not test	DDR4-3200	2022 Plan for test

PS.
1. GD GDQ2BFAA-CJ 4Gb(256MBx6Gb) TX calibration window size<16
2. * MTK plan to test after 2022/Mar.
3. **Due to Samsung few Yield rate issue, please check software Engineer to upgrade BL2 patch 2022/4.

Table 7-6 DDR4-3200 QVL Table

7.8 DDR4-2666 QVL

MT7986A support external DDR4, QVL table as below:

This document will not keep to update, the final QVL release, please visit Website:
http://online.mediatek.inc/qvl/_layouts/15/mol/qvl/ext/QVLHomeExternal.aspx

Vendor	Vendor P/N	RAM Size	Note	Validation Speed	MOL Publish Status
~~Samsung~~	~~K4A4G165WF-BCTD*~~	~~256MBx16Bit=4Gb~~	~~Not test yet~~	~~DDR4-2666~~	
Samsung	K4A8G165WC-BITD*	512MBx16bit=8Gb	Not test yet	DDR4-2666	
Micron	MT40A512M16TB-062E:R *	512MBx16bit=8Gb	Not test yet	DDR4-2666	
ETRON	EM6OE16NWAKA-07H *(0~95'C)	256MBx16Bit=4Gb	Not test yet	DDR4-2666	
ESMT	M16U4G16256A-KJBIG2Z*	256MBx16Bit=4Gb	Not test yet	DDR4-2666	
Nanya	NT5AD256M16E4-JRI*	256MBx16Bit=4Gb	Not test yet	DDR4-2666	
Nanya	NT5AD512M16C4-JRI*	512MBx16bit=8Gb		DDR4-2666	MOL Publish
~~GD~~	~~GDQ2BFAA-CQ*~~	~~256MBx16Bit=4Gb~~	~~Not test yet~~	~~DDR4-2666~~	

* Plan to test after 2022/Mar.

Table 7-7 DDR4-2666 QVL Table

8 Disclaimer

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