

MT7988A

Wi-Fi 7 Generation Router

Platform: Registers Part 1

Open Version

Part 1: Chapter 1 - Chapter 3

Part 2: Chapter 4

Version: 0.1

Release Date: 2023-10-18

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Version History

Version	Date	Description
0.1	2023-10-18	Initial release

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1 MCU and Bus Fabric

1.1 Memory Map

1.1.1 Register Definition

Module name: infracfg_ao Base address: (+0x1000_1000)

Address	Name	Width	Register Function
10001000	<u>INFRASYS_RESERVED</u>	32	Infrasys reserved register
10001004	<u>INFRASYS_BUS_DCM_CTRL</u>	32	Infrasys bus DCM control register
10001008	<u>INFRASYS_MEM_DCM_CTRL</u>	32	Infrasys MEM DCM control register
10001010	<u>MODULE_CLK_SEL_0_SET</u>	32	Infrasys control register - CKMUX 0 set
10001014	<u>MODULE_CLK_SEL_0_CLR</u>	32	Infrasys control register - CKMUX 0 clear
10001018	<u>MODULE_CLK_SEL_0_STA</u>	32	Infrasys control register - CKMUX 0 status
10001020	<u>MODULE_CLK_SEL_1_SET</u>	32	Infrasys control register - CKMUX 1 set
10001024	<u>MODULE_CLK_SEL_1_CLR</u>	32	Infrasys control register - CKMUX 1 clear
10001028	<u>MODULE_CLK_SEL_1_STA</u>	32	Infrasys control register - CKMUX 1 status
10001040	<u>MODULE_SW_CG_0_SET</u>	32	Infrasys DCM control register - Software CG set
10001044	<u>MODULE_SW_CG_0_CLR</u>	32	Infrasys DCM control register - Software CG clear
10001048	<u>MODULE_SW_CG_0_STA</u>	32	Infrasys DCM control register - Software CG status
10001050	<u>MODULE_SW_CG_1_SET</u>	32	Infrasys DCM control register - Software CG set
10001054	<u>MODULE_SW_CG_1_CLR</u>	32	Infrasys DCM control register - Software CG clear
10001058	<u>MODULE_SW_CG_1_STA</u>	32	Infrasys DCM control register - Software CG status
10001060	<u>MODULE_SW_CG_2_SET</u>	32	Infrasys DCM control register - Software CG set
10001064	<u>MODULE_SW_CG_2_CLR</u>	32	Infrasys DCM control register - Software CG clear
10001068	<u>MODULE_SW_CG_2_STA</u>	32	Infrasys DCM control register - Software CG status
10001070	<u>INFRA_GLOBALCON_RST0_SET</u>	32	Infrasys Always-on reset control register
10001074	<u>INFRA_GLOBALCON_RST0_CLR</u>	32	Infrasys Always-on reset control register
10001078	<u>INFRA_GLOBALCON_RST0_STA</u>	32	Infrasys Always-on reset control register
10001080	<u>INFRA_GLOBALCON_RST1_SET</u>	32	Infrasys Always-on reset control register
10001084	<u>INFRA_GLOBALCON_RST1_CLR</u>	32	Infrasys Always-on reset control register
10001088	<u>INFRA_GLOBALCON_RST1_STA</u>	32	Infrasys Always-on reset control register
10001090	<u>INFRA_GLOBALCON_RST2_SET</u>	32	Infrasys Always-on reset control register
10001094	<u>INFRA_GLOBALCON_RST2_CLR</u>	32	Infrasys Always-on reset control register
10001098	<u>INFRA_GLOBALCON_RST2_STA</u>	32	Infrasys Always-on reset control register
10001100	<u>INFRA_AO_SEC_CG_CON0</u>	32	Infra AO CG security enable control 0
10001104	<u>INFRA_AO_SEC_CG_CON1</u>	32	Infra AO CG security enable control 1
10001108	<u>INFRA_AO_SEC_CG_CON2</u>	32	Infra AO CG security enable control 2
10001110	<u>INFRA_AO_SEC_RST_CON0</u>	32	Infra AO RST security enable control 0
10001114	<u>INFRA_AO_SEC_RST_CON1</u>	32	Infra AO RST security enable control 1
10001118	<u>INFRA_AO_SEC_RST_CON2</u>	32	Infra AO RST security enable control 2

10001000 **INFRASYS_RESERVED** Infrasy reserved register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_reserved															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_reserved													pcie_tmbist_clk_sel	tmbist_mbist_en	protect_set_mask_new
Type	RW													RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:3	reg_reserved	Reserved register
2	pcie_tmbist_clk_sel	tmbist clock select for PCIe 0: Normal clock 1: Select tmbist 250-MHz clock to PCIe memory
1	tmbist_mbist_en	tmbist clock select for MSDC 0: Normal clock 1: Select tmbist clock to msdc memory
0	protect_set_mask_new	protect_set_mask for rg_dramc_wer register 0: Disable 1: Enable

10001004 INFRASYS BUS DCM_CTRL Infrasybus DCM control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												rg_me mpsrv_ dis	peri_dc m_rg_f orce_cl koff	peri_dc m_rg_c lkoff_e n	infra_d cm_rg_ force_c lkoff	infra_d cm_rg_ clkoff_ en
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	rg_mempsrv_dis	Disables memory preserved mode clock gating 0: Disable 1: Enable
3	peri_dcm_rg_force_clkoff	Forces peri DCM clock off 0: Disable 1: Enable
2	peri_dcm_rg_clkoff_en	Enables peri DCM clock off 0: Disable 1: Enable
1	infra_dcm_rg_force_clkoff	Forces infra DCM clock off 0: Disable 1: Enable
0	infra_dcm_rg_clkoff_en	Enables infra DCM clock off 0: Disable 1: Enable

10001008 **INFRASYS MEM DCM_CTRL** InfrasyS MEM DCM control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_mem_dcm_ctrl															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_mem_dcm_ctrl															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	reg_mem_dcm_ctrl	mem DCM control register

10001010 MODULE_CLK_SEL_0_SET Infrasys control register - CKMUX 0 set FFFFC7F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pwm8_ck_sel_set		pwm7_ck_sel_set		pwm6_ck_sel_set		pwm5_ck_sel_set		pwm4_ck_sel_set		pwm3_ck_sel_set		pwm2_ck_sel_set		pwm1_ck_sel_set	
Type	WO		WO		WO		WO		WO		WO		WO		WO	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pwm_bck_sel_set					rg_pcie_ref_ck_p3_cg_set	rg_pcie_ref_ck_p2_cg_set	rg_pcie_ref_ck_p1_cg_set	rg_pcie_ref_ck_cg_set	spi2_ck_sel_set	spi1_ck_sel_set	spi0_ck_sel_set	dramc_f26m_sel_set	uart2_ck_sel_set	uart1_ck_sel_set	uart0_ck_sel_set
Type	WO					WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	1	1				1	1	1	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
31:30	pwm8_ck_sel_set	Selects PWM8 clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
29:28	pwm7_ck_sel_set	Selects PWM7 clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
27:26	pwm6_ck_sel_set	Selects PWM6 clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
25:24	pwm5_ck_sel_set	Selects PWM5 clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
23:22	pwm4_ck_sel_set	Selects PWM4 clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
21:20	pwm3_ck_sel_set	Selects PWM3 clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
19:18	pwm2_ck_sel_set	Selects PWM2 clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
17:16	pwm1_ck_sel_set	Selects PWM1 clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
15:14	pwm_bck_sel_set	Selects PWM BCLK clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
10	rg_pcie_ref_ck_p3_cg_set	Sets PCIe P3 REF CK SWCG 0: Disable (with clock) 1: Enable (without clock)
9	rg_pcie_ref_ck_p2_cg_set	Sets PCIe P2 REF CK SWCG 0: Disable (with clock)

Bit(s)	Name	Description
		1: Enable (without clock)
8	rg_pcie_ref_ck_p1_cg_set	Sets PCIe P1 REF CK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
7	rg_pcie_ref_ck_cg_set	Sets PCIe REF CK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
6	spi2_ck_sel_set	Selects SPI2 clock
		0: I2C clock
		1: SPI clock
5	spi1_ck_sel_set	Selects SPI1 clock
		0: I2C clock
		1: SPI clock
4	spi0_ck_sel_set	Selects SPI0 clock
		0: I2C clock
		1: SPI clock
3	dramc_f26m_sel_set	Selects DRAMC 26-MHz clock division
		0: div 1
		1: div 8
2	uart2_ck_sel_set	Selects UART 2 clock
		0: 26-MHz
		1: 52-MHz
1	uart1_ck_sel_set	Selects UART 1 clock
		0: 26-MHz
		1: 52-MHz
0	uart0_ck_sel_set	Selects UART 0 clock
		0: 26-MHz
		1: 52-MHz

10001014 MODULE CLK_SEL_0_CLR Infrasy control register - CKMUX 0 clear FFFFC7F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pwm8_ck_sel_clr		pwm7_ck_sel_clr		pwm6_ck_sel_clr		pwm5_ck_sel_clr		pwm4_ck_sel_clr		pwm3_ck_sel_clr		pwm2_ck_sel_clr		pwm1_ck_sel_clr	
Type	WO		WO		WO		WO		WO		WO		WO		WO	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pwm_bck_sel_clr					rg_pcie_ref_ck_p3_cg_clr	rg_pcie_ref_ck_p2_cg_clr	rg_pcie_ref_ck_p1_cg_clr	rg_pcie_ref_ck_cg_clr	spi2_ck_sel_clr	spi1_ck_sel_clr	spi0_ck_sel_clr	dramc_f26m_sel_clr	uart2_ck_sel_clr	uart1_ck_sel_clr	uart0_ck_sel_clr
Type	WO					WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	1	1				1	1	1	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
31:30	pwm8_ck_sel_clr	Selects PWM8 clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
29:28	pwm7_ck_sel_clr	Selects PWM7 clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
27:26	pwm6_ck_sel_clr	Selects PWM6 clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
25:24	pwm5_ck_sel_clr	Selects PWM5 clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
23:22	pwm4_ck_sel_clr	Selects PWM4 clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
21:20	pwm3_ck_sel_clr	Selects PWM3 clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
19:18	pwm2_ck_sel_clr	Selects PWM2 clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
17:16	pwm1_ck_sel_clr	Selects PWM1 clock 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
15:14	pwm_bck_sel_clr	Selects PWM BCLK 00: 32-kHz, 01: 26-MHz, 10: 78-MHz, 11: PWM
10	rg_pcie_ref_ck_p3_cg_clr	Sets PCIe P3 REF CK SWCG 0: Disable (with clock) 1: Enable (without clock)
9	rg_pcie_ref_ck_p2_cg_clr	Sets PCIe P2 REF CK SWCG 0: Disable (with clock)

Bit(s)	Name	Description
		1: Enable (without clock)
8	rg_pcie_ref_ck_p1_cg_clr	Sets PCIe P1 REF CK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
7	rg_pcie_ref_ck_cg_clr	Sets PCIe REF CK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
6	spi2_ck_sel_clr	Selects SPI2 clock
		0: I2C clock
		1: SPI clock
5	spi1_ck_sel_clr	Selects SPI1 clock
		0: I2C clock
		1: SPI clock
4	spi0_ck_sel_clr	Selects SPI0 clock
		0: I2C clock
		1: SPI clock
3	dramc_f26m_sel_clr	Selects DRAMC 26-MHz clock division
		0: div 1
		1: div 8
2	uart2_ck_sel_clr	Selects UART 2 clock
		0: 26-MHz
		1: 52-MHz
1	uart1_ck_sel_clr	Selects UART 1 clock
		0: 26-MHz
		1: 52-MHz
0	uart0_ck_sel_clr	Selects UART 0 clock
		0: 26-MHz
		1: 52-MHz

10001018 MODULE CLK_SEL 0 STA Infrasy control register - CKMUX 0 status FFFFC7F7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pwm8_ck_sel		pwm7_ck_sel		pwm6_ck_sel		pwm5_ck_sel		pwm4_ck_sel		pwm3_ck_sel		pwm2_ck_sel		pwm1_ck_sel	
Type	RO		RO		RO		RO		RO		RO		RO		RO	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pwm_bck_sel					rg_pcie_ref_ck_p3_cg	rg_pcie_ref_ck_p2_cg	rg_pcie_ref_ck_p1_cg	rg_pcie_ref_ck_cg	spi2_ck_sel	spi1_ck_sel	spi0_ck_sel	dramc_f26m_sel	uart2_ck_sel	uart1_ck_sel	uart0_ck_sel
Type	RO					RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1				1	1	1	1	1	1	1	0	1	1	1

Bit(s)	Name	Description
31:30	pwm8_ck_sel	
29:28	pwm7_ck_sel	
27:26	pwm6_ck_sel	
25:24	pwm5_ck_sel	
23:22	pwm4_ck_sel	
21:20	pwm3_ck_sel	
19:18	pwm2_ck_sel	
17:16	pwm1_ck_sel	
15:14	pwm_bck_sel	
10	rg_pcie_ref_ck_p3_cg	
9	rg_pcie_ref_ck_p2_cg	
8	rg_pcie_ref_ck_p1_cg	
7	rg_pcie_ref_ck_cg	
6	spi2_ck_sel	
5	spi1_ck_sel	
4	spi0_ck_sel	
3	dramc_f26m_sel	
2	uart2_ck_sel	
1	uart1_ck_sel	
0	uart0_ck_sel	

10001020 MODULE_CLK_SEL_1_SET Infrasys control register - CKMUX 1 set 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									pcie_tl_p3_ck_sel_set		pcie_tl_p2_ck_sel_set		pcie_tl_p1_ck_sel_set		pcie_tl_ck_sel_set	
Type									WO		WO		WO		WO	
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:6	pcie_tl_p3_ck_sel_set	Selects PCIe P3 TL clock 00: 32-kHz, 01: 26-MHz, 10: 1'b0, 11: pcie_tl_ck
5:4	pcie_tl_p2_ck_sel_set	Selects PCIe P2 TL clock 00: 32-kHz, 01: 26-MHz, 10: 1'b0, 11: pcie_tl_ck
3:2	pcie_tl_p1_ck_sel_set	Selects PCIe P1 TL clock 00: 32-kHz, 01: 26-MHz, 10: 1'b0, 11: pcie_tl_ck
1:0	pcie_tl_ck_sel_set	Selects PCIe P0 TL clock 00: 32-kHz, 01: 26-MHz, 10: 1'b0, 11: pcie_tl_ck

10001024 MODULE CLK SEL 1 CLR **Infrasys control register - CKMUX 1 clear** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									pcie_tl_p3_ck_sel_clr	pcie_tl_p2_ck_sel_clr	pcie_tl_p1_ck_sel_clr	pcie_tl_ck_sel_clr				
Type									WO	WO	WO	WO				
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:6	pcie_tl_p3_ck_sel_clr	Selects PCIe P3 TL clock 00: 32-kHz, 01: 26-MHz, 10: 1'b0, 11: pcie_tl_ck
5:4	pcie_tl_p2_ck_sel_clr	Selects PCIe P2 TL clock 00: 32-kHz, 01: 26-MHz, 10: 1'b0, 11: pcie_tl_ck
3:2	pcie_tl_p1_ck_sel_clr	Selects PCIe P1 TL clock 00: 32-kHz, 01: 26-MHz, 10: 1'b0, 11: pcie_tl_ck
1:0	pcie_tl_ck_sel_clr	Selects PCIe P0 TL clock 00: 32-kHz, 01: 26-MHz, 10: 1'b0, 11: pcie_tl_ck

10001028 MODULE CLK SEL 1 STA **Infrasys control register - CKMUX 1 status** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									pcie_tl_p3_ck_sel	pcie_tl_p2_ck_sel	pcie_tl_p1_ck_sel	pcie_tl_ck_sel				
Type									RO	RO	RO	RO				
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:6	pcie_tl_p3_ck_sel	Selects PCIe P3 TL clock
5:4	pcie_tl_p2_ck_sel	Selects PCIe P2 TL clock
3:2	pcie_tl_p1_ck_sel	Selects PCIe P1 TL clock
1:0	pcie_tl_ck_sel	Selects PCIe P0 TL clock

10001040 MODULE SW CG 0 SET Infrasy DCM control register - Software CG set 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	trng_ck_cg_set	sej_13m_ck_cg_set	sej_bclk_ck_cg_set	ap_dma_ck_cg_set	dbg_ck_cg_set	dramc_26m_ck_cg_set	audio_engine2_ck_cg_set	audio_engine1_ck_cg_set	audio_audio_ck_cg_set							
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	audio_intbus_ck_cg_set	audio_26m_ck_cg_set	audio_bus_ck_cg_set	cq_dma_bus_ck_cg_set	cq_dma_fpc_ck_cg_set	pwm8_ck_cg_set	pwm7_ck_cg_set	pwm6_ck_cg_set	pwm5_ck_cg_set	pwm4_ck_cg_set	pwm3_ck_cg_set	pwm2_ck_cg_set	pwm1_ck_cg_set	pwm_bclk_cg_set	pwm_hclk_cg_set	apxgpt_cg_set
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	trng_ck_cg_set	Sets TRNG SWCG 0: Disable (with clock) 1: Enable (without clock)
30	sej_13m_ck_cg_set	Sets SEJ 13M SWCG 0: Disable (with clock) 1: Enable (without clock)
29	sej_bclk_ck_cg_set	Sets SEJ SWCG 0: Disable (with clock) 1: Enable (without clock)
28	ap_dma_ck_cg_set	Sets APDMA SWCG 0: Disable (with clock) 1: Enable (without clock)
27	dbg_ck_cg_set	Sets DBG SWCG 0: Disable (with clock) 1: Enable (without clock)
26	dramc_26m_ck_cg_set	Sets DRAMC 26M SWCG 0: Disable (with clock) 1: Enable (without clock)
25	audio_engine2_ck_cg_set	Sets AUDIO ENGINE2 SWCG 0: Disable (with clock) 1: Enable (without clock)
24	audio_engine1_ck_cg_set	Sets AUDIO ENGINE1 SWCG

Bit(s)	Name	Description
		0: Disable (with clock)
		1: Enable (without clock)
23:16	audio_audio_ck_cg_set	Sets AUDIO AUDIO SWCG
		0: Disable (with clock)
		1: Enable (without clock)
15	audio_intbus_ck_cg_set	Sets AUDIO INTBUS SWCG
		0: Disable (with clock)
		1: Enable (without clock)
14	audio_26m_ck_cg_set	Sets AUDIO 26M SWCG
		0: Disable (with clock)
		1: Enable (without clock)
13	audio_bus_ck_cg_set	Sets AUDIO BUS SWCG
		0: Disable (with clock)
		1: Enable (without clock)
12	cq_dma_bus_ck_cg_set	Sets CQDMA BUS SWCG
		0: Disable (with clock)
		1: Enable (without clock)
11	cq_dma_fpc_ck_cg_set	Sets CQDMA FPC SWCG
		0: Disable (with clock)
		1: Enable (without clock)
10	pwm8_ck_cg_set	Sets PWM8 SWCG
		0: Disable (with clock)
		1: Enable (without clock)
9	pwm7_ck_cg_set	Sets PWM7 SWCG
		0: Disable (with clock)
		1: Enable (without clock)
8	pwm6_ck_cg_set	Sets PWM6 SWCG
		0: Disable (with clock)
		1: Enable (without clock)
7	pwm5_ck_cg_set	Sets PWM5 SWCG
		0: Disable (with clock)
		1: Enable (without clock)

Bit(s)	Name	Description
6	pwm4_ck_cg_set	Sets PWM4 SWCG 0: Disable (with clock) 1: Enable (without clock)
5	pwm3_ck_cg_set	Sets PWM3 SWCG 0: Disable (with clock) 1: Enable (without clock)
4	pwm2_ck_cg_set	Sets PWM2 SWCG 0: Disable (with clock) 1: Enable (without clock)
3	pwm1_ck_cg_set	Sets PWM1 SWCG 0: Disable (with clock) 1: Enable (without clock)
2	pwm_bclk_cg_set	Sets PWM BCLK SWCG 0: Disable (with clock) 1: Enable (without clock)
1	pwm_hclk_cg_set	Sets PWM HCLK SWCG 0: Disable (with clock) 1: Enable (without clock)
0	apxgpt_cg_set	Sets APXGPT SWCG 0: Disable (with clock) 1: Enable (without clock)

10001044 MODULE SW CG 0 CLR Infrasy DCM control register - Software CG clear 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	trng_ck_cg_clr	sej_13m_ck_cg_clr	sej_bclk_ck_cg_clr	ap_dma_ck_cg_clr	dbg_ck_cg_clr	dramc_26m_ck_cg_clr	audio_engine2_ck_cg_clr	audio_engine1_ck_cg_clr	audio_audio_ck_cg_clr							
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	audio_intbus_ck_cg_clr	audio_26m_ck_cg_clr	audio_bus_ck_cg_clr	cq_dma_bus_ck_cg_clr	cq_dma_fpc_ck_cg_clr	pwm8_ck_cg_clr	pwm7_ck_cg_clr	pwm6_ck_cg_clr	pwm5_ck_cg_clr	pwm4_ck_cg_clr	pwm3_ck_cg_clr	pwm2_ck_cg_clr	pwm1_ck_cg_clr	pwm_bclk_ck_clr	pwm_hclk_ck_clr	apxgpt_cg_clr
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	trng_ck_cg_clr	Clears TRNG SWCG 0: Enable 1: Disable
30	sej_13m_ck_cg_clr	Clears SEJ 13M SWCG 0: Enable 1: Disable
29	sej_bclk_ck_cg_clr	Clears SEJ SWCG 0: Enable 1: Disable
28	ap_dma_ck_cg_clr	Clears APDMA SWCG 0: Enable 1: Disable
27	dbg_ck_cg_clr	Clears DBG SWCG 0: Enable 1: Disable
26	dramc_26m_ck_cg_clr	Clears DRAMC 26M SWCG 0: Enable 1: Disable
25	audio_engine2_ck_cg_clr	Clears AUDIO ENGINE2 SWCG 0: Enable 1: Disable
24	audio_engine1_ck_cg_clr	Clears AUDIO ENGINE1 SWCG

Bit(s)	Name	Description
		0: Enable
		1: Disable
23:16	audio_audio_ck_cg_clr	Clears AUDIO AUDIO SWCG
		0: Enable
		1: Disable
15	audio_intbus_ck_cg_clr	Clears AUDIO INTBUS SWCG
		0: Enable
		1: Disable
14	audio_26m_ck_cg_clr	Clears AUDIO 26M SWCG
		0: Enable
		1: Disable
13	audio_bus_ck_cg_clr	Clears AUDIO BUS SWCG
		0: Enable
		1: Disable
12	cq_dma_bus_ck_cg_clr	Clears CQDMA BUS SWCG
		0: Enable
		1: Disable
11	cq_dma_fpc_ck_cg_clr	Clears CQDMA FPC SWCG
		0: Enable
		1: Disable
10	pwm8_ck_cg_clr	Clears PWM8 SWCG
		0: Enable
		1: Disable
9	pwm7_ck_cg_clr	Clears PWM7 SWCG
		0: Enable
		1: Disable
8	pwm6_ck_cg_clr	Clears PWM6 SWCG
		0: Enable
		1: Disable
7	pwm5_ck_cg_clr	Clears PWM5 SWCG
		0: Enable
		1: Disable

Bit(s)	Name	Description
6	pwm4_ck_cg_clr	Clears PWM4 SWCG 0: Enable 1: Disable
5	pwm3_ck_cg_clr	Clears PWM3 SWCG 0: Enable 1: Disable
4	pwm2_ck_cg_clr	Clears PWM2 SWCG 0: Enable 1: Disable
3	pwm1_ck_cg_clr	Clears PWM1 SWCG 0: Enable 1: Disable
2	pwm_bclk_cg_clr	Clears PWM BCLK SWCG 0: Enable 1: Disable
1	pwm_hclk_cg_clr	Clears PWM HCLK SWCG 0: Enable 1: Disable
0	apxgpt_cg_clr	Clears APXGPT SWCG 0: Enable 1: Disable

10001048

MODULE SW CG 0 STA

Infrasys DCM control register - Software CG
status

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	trng_ck_cg_sta	sej_13m_ck_cg_sta	sej_bclk_ck_cg_sta	ap_dma_ck_cg_sta	dbg_ck_cg_sta	dramc_26m_ck_cg_sta	audio_engine2_ck_cg_sta	audio_engine1_ck_cg_sta	audio_audio_ck_cg_sta							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	audio_intbus_ck_cg_sta	audio_26m_ck_cg_sta	audio_bus_ck_cg_sta	cq_dma_bus_ck_cg_sta	cq_dma_fpc_ck_cg_sta	pwm8_ck_cg_sta	pwm7_ck_cg_sta	pwm6_ck_cg_sta	pwm5_ck_cg_sta	pwm4_ck_cg_sta	pwm3_ck_cg_sta	pwm2_ck_cg_sta	pwm1_ck_cg_sta	pwm_bclk_ck_sta	pwm_hclk_ck_sta	apxgpt_cg_sta
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	trng_ck_cg_sta	TRNG SWCG STA 0: Enable 1: Disable
30	sej_13m_ck_cg_sta	SEJ 13M SWCG STA 0: Enable 1: Disable
29	sej_bclk_ck_cg_sta	SEJ SWCG STA 0: Enable 1: Disable
28	ap_dma_ck_cg_sta	APDMA SWCG STA 0: Enable 1: Disable
27	dbg_ck_cg_sta	DBG SWCG STA 0: Enable 1: Disable
26	dramc_26m_ck_cg_sta	DRAMC 26M SWCG STA 0: Enable 1: Disable
25	audio_engine2_ck_cg_sta	AUDIO ENGINE2 SWCG STA 0: Enable 1: Disable
24	audio_engine1_ck_cg_sta	AUDIO ENGINE1 SWCG STA

Bit(s)	Name	Description
		0: Enable
		1: Disable
23:16	audio_audio_ck_cg_sta	AUDIO AUDIO SWCG STA
		0: Enable
		1: Disable
15	audio_intbus_ck_cg_sta	AUDIO INTBUS SWCG STA
		0: Enable
		1: Disable
14	audio_26m_ck_cg_sta	AUDIO 26M SWCG STA
		0: Enable
		1: Disable
13	audio_bus_ck_cg_sta	AUDIO BUS SWCG STA
		0: Enable
		1: Disable
12	cq_dma_bus_ck_cg_sta	CQDMA BUS SWCG STA
		0: Enable
		1: Disable
11	cq_dma_fpc_ck_cg_sta	CQDMA FPC SWCG STA
		0: Enable
		1: Disable
10	pwm8_ck_cg_sta	PWM8 SWCG STA
		0: Enable
		1: Disable
9	pwm7_ck_cg_sta	PWM7 SWCG STA
		0: Enable
		1: Disable
8	pwm6_ck_cg_sta	PWM6 SWCG STA
		0: Enable
		1: Disable
7	pwm5_ck_cg_sta	PWM5 SWCG STA
		0: Enable
		1: Disable

Bit(s)	Name	Description
6	pwm4_ck_cg_sta	PWM4 SWCG STA 0: Enable 1: Disable
5	pwm3_ck_cg_sta	PWM3 SWCG STA 0: Enable 1: Disable
4	pwm2_ck_cg_sta	PWM2 SWCG STA 0: Enable 1: Disable
3	pwm1_ck_cg_sta	PWM1 SWCG STA 0: Enable 1: Disable
2	pwm_bclk_cg_sta	PWM BCLK SWCG STA 0: Enable 1: Disable
1	pwm_hclk_cg_sta	PWM HCLK SWCG STA 0: Enable 1: Disable
0	apxgpt_cg_sta	APXGPT SWCG STA 0: Enable 1: Disable

10001050 MODULE SW CG 1 SET Infrasy DCM control register - Software CG set 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	i2c_x16w_pclk_ck_cg_p1_set	i2c_x16w_pclk_ck_cg_set	i2c_x16w_mclk_ck_cg_p1_set	i2c_x16w_mclk_ck_cg_set	fbist2fpc_ck_cg_set	cpum_ck_cg_set	msdc50_66m_ck_cg_set	msdc50_133m_ck_cg_set	fmsdc250_hclk_ck_cg_set	fmsdc400_ck_cg_set			frtc_ck_cg_set		spi2_hclk_ck_cg_set	spi1_hclk_ck_cg_set
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO			WO		WO	WO
Reset	0	0	0	0	0	0	0	0	0	0			0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spi0_hclk_ck_cg_set	spi2_bclk_ck_cg_set	spi1_bclk_ck_cg_set	spi0_bclk_ck_cg_set	nfi_hclk_ck_cg_set	spinfi_ck_cg_set	nfi_ck_cg_set				uart2_ck_cg_set	uart1_ck_cg_set	uart0_ck_cg_set	i2c_ck_cg_p1_set	i2c_ck_cg_set	therm_ck_cg_set
Type	WO	WO	WO	WO	WO	WO	WO				WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0				0	0	0	0	0	0

Bit(s)	Name	Description
31	i2c_x16w_pclk_ck_cg_p1_set	Sets FBIST2FPC SWCG 0: Disable (with clock) 1: Enable (without clock)
30	i2c_x16w_pclk_ck_cg_set	Sets FBIST2FPC SWCG 0: Disable (with clock) 1: Enable (without clock)
29	i2c_x16w_mclk_ck_cg_p1_set	Sets FBIST2FPC SWCG 0: Disable (with clock) 1: Enable (without clock)
28	i2c_x16w_mclk_ck_cg_set	Sets FBIST2FPC SWCG 0: Disable (with clock) 1: Enable (without clock)
27	fbist2fpc_ck_cg_set	Sets FBIST2FPC SWCG 0: Disable (with clock) 1: Enable (without clock)
26	cpum_ck_cg_set	Sets FBIST2FPC SWCG 0: Disable (with clock) 1: Enable (without clock)
25	msdc50_66m_ck_cg_set	Sets FBIST2FPC SWCG 0: Disable (with clock) 1: Enable (without clock)
24	msdc50_133m_ck_cg_set	Sets CPUM SWCG

Bit(s)	Name	Description
		0: Disable (with clock)
		1: Enable (without clock)
23	fmsdc250_hclk_ck_cg_set	Sets AUXADC FRC SWCG
		0: Disable (with clock)
		1: Enable (without clock)
22	fmsdc400_ck_cg_set	Sets AUXADC 26M SWCG
		0: Disable (with clock)
		1: Enable (without clock)
19	frtc_ck_cg_set	Sets FMSDC50 66M SWCG
		0: Disable (with clock)
		1: Enable (without clock)
17	spi2_hclk_ck_cg_set	Sets FMSDC50 HCLK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
16	spi1_hclk_ck_cg_set	Sets FMSDC50 SWCG
		0: Disable (with clock)
		1: Enable (without clock)
15	spi0_hclk_ck_cg_set	Sets FRTC SWCG
		0: Disable (with clock)
		1: Enable (without clock)
14	spi2_bclk_ck_cg_set	Sets SPI1 HCLK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
13	spi1_bclk_ck_cg_set	Sets SPI0 HCLK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
12	spi0_bclk_ck_cg_set	Sets SPI1 BCLK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
11	nfi_hclk_ck_cg_set	Sets SPI0 BCLK SWCG
		0: Disable (with clock)
		1: Enable (without clock)

Bit(s)	Name	Description
10	spinfi_ck_cg_set	Sets NFI HCLK SWCG 0: Disable (with clock) 1: Enable (without clock)
9	nfi_ck_cg_set	Sets SPINFI SWCG 0: Disable (with clock) 1: Enable (without clock)
5	uart2_ck_cg_set	Sets NFI SWCG 0: Disable (with clock) 1: Enable (without clock)
4	uart1_ck_cg_set	Sets UART2 SWCG 0: Disable (with clock) 1: Enable (without clock)
3	uart0_ck_cg_set	Sets UART1 SWCG 0: Disable (with clock) 1: Enable (without clock)
2	i2c_ck_cg_p1_set	Sets UART0 SWCG 0: Disable (with clock) 1: Enable (without clock)
1	i2c_ck_cg_set	Sets I2C SWCG 0: Disable (with clock) 1: Enable (without clock)
0	therm_ck_cg_set	Sets THERM SWCG 0: Disable (with clock) 1: Enable (without clock)

10001054 MODULE SW CG 1 CLR Infrasy DCM control register - Software CG clear 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	i2c_x16w_pclk_ck_cg_p1_clr	i2c_x16w_pclk_ck_cg_clr	i2c_x16w_mclk_ck_cg_p1_clr	i2c_x16w_mclk_ck_cg_clr	fbist2fpc_ck_cg_clr	cpum_ck_cg_clr	msdc50_66m_ck_cg_clr	msdc50_133m_ck_cg_clr	fmsdc250_hclk_ck_cg_clr	fmsdc400_ck_cg_clr			frtc_ck_cg_clr		spi2_hclk_ck_cg_clr	spi1_hclk_ck_cg_clr
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO			WO		WO	WO
Reset	0	0	0	0	0	0	0	0	0	0			0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spi0_hclk_ck_cg_clr	spi2_bclk_ck_cg_clr	spi1_bclk_ck_cg_clr	spi0_bclk_ck_cg_clr	nfi_hclk_ck_cg_clr	spini_ck_cg_clr	nfi_ck_cg_clr				uart2_ck_cg_clr	uart1_ck_cg_clr	uart0_ck_cg_clr	i2c_ck_cg_p1_clr	i2c_ck_cg_clr	therm_ck_cg_clr
Type	WO	WO	WO	WO	WO	WO	WO				WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0				0	0	0	0	0	0

Bit(s)	Name	Description
31	i2c_x16w_pclk_ck_cg_p1_clr	Clears FBIST2FPC SWCG 0: Enable 1: Disable
30	i2c_x16w_pclk_ck_cg_clr	Clears FBIST2FPC SWCG 0: Enable 1: Disable
29	i2c_x16w_mclk_ck_cg_p1_clr	Clears FBIST2FPC SWCG 0: Enable 1: Disable
28	i2c_x16w_mclk_ck_cg_clr	Clears FBIST2FPC SWCG 0: Enable 1: Disable
27	fbist2fpc_ck_cg_clr	Clears FBIST2FPC SWCG 0: Enable 1: Disable
26	cpum_ck_cg_clr	Clears FBIST2FPC SWCG 0: Enable 1: Disable
25	msdc50_66m_ck_cg_clr	Clears CPUM SWCG 0: Enable 1: Disable
24	msdc50_133m_ck_cg_clr	Clears AUXADC FRC SWCG

Bit(s)	Name	Description
		0: Enable
		1: Disable
23	fmsdc250_hclk_ck_cg_clr	Clears AUXADC 26M SWCG
		0: Enable
		1: Disable
22	fmsdc400_ck_cg_clr	Clears FMSDC50 66M SWCG
		0: Enable
		1: Disable
19	frtc_ck_cg_clr	Clears FMSDC50 133M SWCG
		0: Enable
		1: Disable
17	spi2_hclk_ck_cg_clr	Clears FMSDC50 HCLK SWCG
		0: Enable
		1: Disable
16	spi1_hclk_ck_cg_clr	Clears FMSDC50 SWCG
		0: Enable
		1: Disable
15	spi0_hclk_ck_cg_clr	Clears FRTC SWCG
		0: Enable
		1: Disable
14	spi2_bclk_ck_cg_clr	Clears SPI1 HCLK SWCG
		0: Enable
		1: Disable
13	spi1_bclk_ck_cg_clr	Clears SPI0 HCLK SWCG
		0: Enable
		1: Disable
12	spi0_bclk_ck_cg_clr	Clears SPI1 BCLK SWCG
		0: Enable
		1: Disable
11	nfi_hclk_ck_cg_clr	Clears SPI0 BCLK SWCG
		0: Enable
		1: Disable

Bit(s)	Name	Description
10	spinfi_ck_cg_clr	Clears NFI HCLK SWCG 0: Enable 1: Disable
9	nfi_ck_cg_clr	Clears SPINFI SWCG 0: Enable 1: Disable
5	uart2_ck_cg_clr	Clears NFI SWCG 0: Enable 1: Disable
4	uart1_ck_cg_clr	Clears UART2 SWCG 0: Enable 1: Disable
3	uart0_ck_cg_clr	Clears UART1 SWCG 0: Enable 1: Disable
2	i2c_ck_cg_p1_clr	Clears UART0 SWCG 0: Enable 1: Disable
1	i2c_ck_cg_clr	Clears I2C SWCG 0: Enable 1: Disable
0	therm_ck_cg_clr	Clears THERM SWCG 0: Enable 1: Disable

10001058

MODULE SW CG 1 STA

Infrasys DCM control register - Software CG
status

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	i2c_x16w_pclk_ck_cg_p1_sta	i2c_x16w_pclk_ck_cg_sta	i2c_x16w_mclk_ck_cg_p1_sta	i2c_x16w_mclk_ck_cg_sta	fbist2fpc_ck_cg_sta	cpum_ck_cg_sta	msdc50_66m_ck_cg_sta	msdc50_133m_ck_cg_sta	fmsdc250_hclk_ck_cg_sta	fmsdc400_ck_cg_sta			frtc_ck_cg_sta		spi2_hclk_ck_cg_sta	spi1_hclk_ck_cg_sta
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO			RO		RO	RO
Reset	0	0	0	0	0	0	0	0	0	0			0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spi0_hclk_ck_cg_sta	spi2_bclk_ck_cg_sta	spi1_bclk_ck_cg_sta	spi0_bclk_ck_cg_sta	nfi_hclk_ck_cg_sta	spifi_ck_cg_sta	nfi_ck_cg_sta				uart2_ck_cg_sta	uart1_ck_cg_sta	uart0_ck_cg_sta	i2c_ck_cg_p1_sta	i2c_ck_cg_sta	therm_ck_cg_sta
Type	RO	RO	RO	RO	RO	RO	RO				RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0				0	0	0	0	0	0

Bit(s)	Name	Description
31	i2c_x16w_pclk_ck_cg_p1_sta	FBIST2FPC SWCG STA 0: Enable 1: Disable
30	i2c_x16w_pclk_ck_cg_sta	FBIST2FPC SWCG STA 0: Enable 1: Disable
29	i2c_x16w_mclk_ck_cg_p1_sta	FBIST2FPC SWCG STA 0: Enable 1: Disable
28	i2c_x16w_mclk_ck_cg_sta	FBIST2FPC SWCG STA 0: Enable 1: Disable
27	fbist2fpc_ck_cg_sta	FBIST2FPC SWCG STA 0: Enable 1: Disable
26	cpum_ck_cg_sta	FBIST2FPC SWCG STA 0: Enable 1: Disable
25	msdc50_66m_ck_cg_sta	CPUM SWCG STA 0: Enable 1: Disable

Bit(s)	Name	Description
24	msdc50_133m_ck_cg_sta	AUXADC FRC SWCG STA 0: Enable 1: Disable
23	fmsdc250_hclk_ck_cg_sta	AUXADC 26M SWCG STA 0: Enable 1: Disable
22	fmsdc400_ck_cg_sta	FMSDC50 66M SWCG STA 0: Enable 1: Disable
19	frtc_ck_cg_sta	FMSDC50 133M SWCG STA 0: Enable 1: Disable
17	spi2_hclk_ck_cg_sta	FMSDC50 HCLK SWCG STA 0: Enable 1: Disable
16	spi1_hclk_ck_cg_sta	FMSDC50 SWCG STA 0: Enable 1: Disable
15	spi0_hclk_ck_cg_sta	FRTC SWCG STA 0: Enable 1: Disable
14	spi2_bclk_ck_cg_sta	SPI1 HCLK SWCG STA 0: Enable 1: Disable
13	spi1_bclk_ck_cg_sta	SPI0 HCLK SWCG STA 0: Enable 1: Disable
12	spi0_bclk_ck_cg_sta	SPI1 BCLK SWCG STA 0: Enable 1: Disable
11	nfi_hclk_ck_cg_sta	SPI0 BCLK SWCG STA 0: Enable

Bit(s)	Name	Description
		1: Disable
10	spinfi_ck_cg_sta	NFI HCLK SWCG STA
		0: Enable
		1: Disable
9	nfi_ck_cg_sta	SPINFI SWCG STA
		0: Enable
		1: Disable
5	uart2_ck_cg_sta	NFI SWCG STA
		0: Enable
		1: Disable
4	uart1_ck_cg_sta	UART2 SWCG STA
		0: Enable
		1: Disable
3	uart0_ck_cg_sta	UART1 SWCG STA
		0: Enable
		1: Disable
2	i2c_ck_cg_p1_sta	UART0 SWCG STA
		0: Enable
		1: Disable
1	i2c_ck_cg_sta	I2C SWCG STA
		0: Enable
		1: Disable
0	therm_ck_cg_sta	THERM SWCG STA
		0: Enable
		1: Disable

10001060 MODULE SW CG 2 SET Infrasy DCM control register - Software CG set 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pcie_bclk_ck_cg_p3_set	pcie_bclk_ck_cg_p2_set	pcie_bclk_ck_cg_p1_set	pcie_bclk_ck_cg_p0_set	pcie_pipe_ck_cg_p3_set	pcie_pipe_ck_cg_p2_set	pcie_pipe_ck_cg_p1_set	pcie_pipe_ck_cg_p0_set	pcie_tl_ck_cg_p3_set	pcie_tl_ck_cg_p2_set	pcie_tl_ck_cg_p1_set	pcie_tl_ck_cg_p0_set	ssusb_sdin_ck_cg_p1_set	ssusb_scl_ck_cg_p1_set	ssusb_scl_ck_cg_set	ssusb_scl_ck_cg_set
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ssusb_xhci_ck_cg_p1_set	ssusb_xhci_ck_cg_set	ssubs_utmi_ck_cg_p1_set	ssubs_utmi_ck_cg_set	ssubs_pipe_ck_cg_p1_set	ssubs_pipe_ck_cg_set	ssusb_rmcnt_ck_cg_p1_set	ssusb_rmcnt_ck_cg_set	ssusb_rmcnt_ck_cg_p1_set	ssusb_rmcnt_ck_cg_set	ssusb_rmcnt_ck_cg_p1_set	ssusb_rmcnt_ck_cg_set	ssusb_rmcnt_ck_cg_p1_set	ssusb_rmcnt_ck_cg_set	ssusb_rmcnt_ck_cg_p1_set	ssusb_rmcnt_ck_cg_set
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	pcie_bclk_ck_cg_p3_set	Sets PCIe BCLK SWCG 0: Disable (with clock) 1: Enable (without clock)
30	pcie_bclk_ck_cg_p2_set	Sets PCIe BCLK SWCG 0: Disable (with clock) 1: Enable (without clock)
29	pcie_bclk_ck_cg_p1_set	Sets PCIe BCLK SWCG 0: Disable (with clock) 1: Enable (without clock)
28	pcie_bclk_ck_cg_p0_set	Sets PCIe BCLK SWCG 0: Disable (with clock) 1: Enable (without clock)
27	pcie_pipe_ck_cg_p3_set	Sets PCIe BCLK SWCG 0: Disable (with clock) 1: Enable (without clock)
26	pcie_pipe_ck_cg_p2_set	Sets PCIe BCLK SWCG 0: Disable (with clock) 1: Enable (without clock)
25	pcie_pipe_ck_cg_p1_set	Sets PCIe BCLK SWCG 0: Disable (with clock) 1: Enable (without clock)
24	pcie_pipe_ck_cg_p0_set	Sets PCIe BCLK SWCG

Bit(s)	Name	Description
		0: Disable (with clock)
		1: Enable (without clock)
23	pcie_tl_ck_cg_p3_set	Sets PCIe BCLK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
22	pcie_tl_ck_cg_p2_set	Sets PCIe BCLK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
21	pcie_tl_ck_cg_p1_set	Sets PCIe BCLK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
20	pcie_tl_ck_cg_p0_set	Sets PCIe BCLK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
19	ssusb_sdin_ck_cg_p1_set	Sets PCIe BCLK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
18	ssusb_sdin_ck_cg_set	Sets PCIe BCLK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
17	ssusb_scl_ck_cg_p1_set	Sets PCIe BCLK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
16	ssusb_scl_ck_cg_set	Sets PCIe BCLK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
15	ssusb_xhci_ck_cg_p1_set	Sets PCIe BCLK SWCG
		0: Disable (with clock)
		1: Enable (without clock)
14	ssusb_xhci_ck_cg_set	Sets PCIe BCLK SWCG
		0: Disable (with clock)
		1: Enable (without clock)

Bit(s)	Name	Description
13	ssubs_utmi_ck_cg_p1_set	Sets PCIe REF SWCG 0: Disable (with clock) 1: Enable (without clock)
12	ssusb_utmi_ck_cg_set	Sets PCIe PIPE SWCG 0: Disable (with clock) 1: Enable (without clock)
11	ssubs_pipe_ck_cg_p1_set	Sets PCIe TL SWCG 0: Disable (with clock) 1: Enable (without clock)
10	ssubs_pipe_ck_cg_set	Sets SSUSB SDIN SWCG 0: Disable (with clock) 1: Enable (without clock)
9	ssusb_frmcnt_ck_cg_p1_set	Sets SSUSB SCL SWCG 0: Disable (with clock) 1: Enable (without clock)
8	ssusb_frmcnt_ck_cg_set	Sets SSUSB XHCI SWCG 0: Disable (with clock) 1: Enable (without clock)
7	ssusb_ref_ck_cg_p1_set	Sets SSUSB UTMI 1P SWCG 0: Disable (with clock) 1: Enable (without clock)
6	ssusb_ref_ck_cg_set	Sets SSUSB UTMI SWCG 0: Disable (with clock) 1: Enable (without clock)
5	ssubs_sys_ck_cg_p1_set	Sets SSUSB PIPE SWCG 0: Disable (with clock) 1: Enable (without clock)
4	ssubs_sys_ck_cg_set	Sets SSUSB FRMCNT SWCG 0: Disable (with clock) 1: Enable (without clock)
3	ssusb_66m_ck_cg_p1_set	Sets SSUSB REF SWCG 0: Disable (with clock)

Bit(s)	Name	Description
		1: Enable (without clock)
2	ssusb_66m_ck_cg_set	Sets SSUSB SYS SWCG
		0: Disable (with clock)
		1: Enable (without clock)
1	ssusb_133m_ck_cg_p1_set	Sets SSUSB 66M SWCG
		0: Disable (with clock)
		1: Enable (without clock)
0	ssusb_133m_ck_cg_set	Sets SSUSB 133M SWCG
		0: Disable (with clock)
		1: Enable (without clock)

10001064 MODULE SW CG 2 CLR Infrasy DCM control register - Software CG clear 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pcie_bclk_ck_cg_p3_clr	pcie_bclk_ck_cg_p2_clr	pcie_bclk_ck_cg_p1_clr	pcie_bclk_ck_cg_p0_clr	pcie_pipe_ck_cg_p3_clr	pcie_pipe_ck_cg_p2_clr	pcie_pipe_ck_cg_p1_clr	pcie_pipe_ck_cg_p0_clr	pcie_tl_ck_cg_p3_clr	pcie_tl_ck_cg_p2_clr	pcie_tl_ck_cg_p1_clr	pcie_tl_ck_cg_p0_clr	ssusb_sdin_ck_cg_p1_clr	ssusb_sdin_ck_cg_p1_clr	ssusb_scl_ck_cg_p1_clr	ssusb_scl_ck_cg_clr
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ssusb_xhci_ck_cg_p1_clr	ssusb_xhci_ck_cg_clr	ssubs_utmi_ck_cg_p1_clr	ssubs_utmi_ck_cg_clr	ssubs_pipe_ck_cg_p1_clr	ssubs_pipe_ck_cg_clr	ssubs_rmcnt_ck_cg_p1_clr	ssubs_rmcnt_ck_cg_clr	ssusb_ef_ck_cg_p1_clr	ssusb_ef_ck_cg_clr	ssusb_rmcnt_ck_cg_p1_clr	ssusb_rmcnt_ck_cg_clr	ssubs_sclk_cg_p1_clr	ssubs_sclk_cg_clr	ssusb_66m_ck_cg_p1_clr	ssusb_66m_ck_cg_clr
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	pcie_bclk_ck_cg_p3_clr	Clears PCIe BCLK SWCG 0: Enable 1: Disable
30	pcie_bclk_ck_cg_p2_clr	Clears PCIe BCLK SWCG 0: Enable 1: Disable
29	pcie_bclk_ck_cg_p1_clr	Clears PCIe BCLK SWCG 0: Enable 1: Disable
28	pcie_bclk_ck_cg_p0_clr	Clears PCIe BCLK SWCG 0: Enable 1: Disable
27	pcie_pipe_ck_cg_p3_clr	Clears PCIe BCLK SWCG 0: Enable 1: Disable
26	pcie_pipe_ck_cg_p2_clr	Clears PCIe BCLK SWCG 0: Enable 1: Disable
25	pcie_pipe_ck_cg_p1_clr	Clears PCIe BCLK SWCG 0: Enable 1: Disable
24	pcie_pipe_ck_cg_p0_clr	Clears PCIe BCLK SWCG

Bit(s)	Name	Description
		0: Enable
		1: Disable
23	pcie_tl_ck_cg_p3_clr	Clears PCIe BCLK SWCG
		0: Enable
		1: Disable
22	pcie_tl_ck_cg_p2_clr	Clears PCIe BCLK SWCG
		0: Enable
		1: Disable
21	pcie_tl_ck_cg_p1_clr	Clears PCIe BCLK SWCG
		0: Enable
		1: Disable
20	pcie_tl_ck_cg_p0_clr	Clears PCIe BCLK SWCG
		0: Enable
		1: Disable
19	ssusb_sdin_ck_cg_p1_clr	Clears PCIe BCLK SWCG
		0: Enable
		1: Disable
18	ssusb_sdin_ck_cg_clr	Clears PCIe BCLK SWCG
		0: Enable
		1: Disable
17	ssusb_scl_ck_cg_p1_clr	Clears PCIe BCLK SWCG
		0: Enable
		1: Disable
16	ssusb_scl_ck_cg_clr	Clears PCIe BCLK SWCG
		0: Enable
		1: Disable
15	ssusb_xhci_ck_cg_p1_clr	Clears PCIe BCLK SWCG
		0: Enable
		1: Disable
14	ssusb_xhci_ck_cg_clr	Clears PCIe BCLK SWCG
		0: Enable
		1: Disable

Bit(s)	Name	Description
13	ssubs_utmi_ck_cg_p1_clr	Clears PCIe REF SWCG 0: Enable 1: Disable
12	ssusb_utmi_ck_cg_clr	Clears PCIe PIPE SWCG 0: Enable 1: Disable
11	ssubs_pipe_ck_cg_p1_clr	Clears PCIe TL SWCG 0: Enable 1: Disable
10	ssubs_pipe_ck_cg_clr	Clears SSUSB SDIN SWCG 0: Enable 1: Disable
9	ssusb_frmcnt_ck_cg_p1_clr	Clears SSUSB SCL SWCG 0: Enable 1: Disable
8	ssusb_frmcnt_ck_cg_clr	Clears SSUSB XHCI SWCG 0: Enable 1: Disable
7	ssusb_ref_ck_cg_p1_clr	Clears SSUSB UTMI 1P SWCG 0: Enable 1: Disable
6	ssusb_ref_ck_cg_clr	Clears SSUSB UTMI SWCG 0: Enable 1: Disable
5	ssubs_sys_ck_cg_p1_clr	Clears SSUSB PIPE SWCG 0: Enable 1: Disable
4	ssubs_sys_ck_cg_clr	Clears SSUSB FRMCNT SWCG 0: Enable 1: Disable
3	ssusb_66m_ck_cg_p1_clr	Clears SSUSB REF SWCG 0: Enable

Bit(s)	Name	Description
		1: Disable
2	ssusb_66m_ck_cg_clr	Clears SSUSB SYS SWCG 0: Enable 1: Disable
1	ssusb_133m_ck_cg_p1_clr	Clears SSUSB 66M SWCG 0: Enable 1: Disable
0	ssusb_133m_ck_cg_clr	Clears SSUSB 133M SWCG 0: Enable 1: Disable

10001068

MODULE SW CG 2 STA

Infrasys DCM control register - Software CG
status

FEE00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pcie_bclk_ck_cg_p3_sta	pcie_bclk_ck_cg_p2_sta	pcie_bclk_ck_cg_p1_sta	pcie_bclk_ck_cg_p0_sta	pcie_pipe_ck_cg_p3_sta	pcie_pipe_ck_cg_p2_sta	pcie_pipe_ck_cg_p1_sta	pcie_pipe_ck_cg_p0_sta	pcie_tl_ck_cg_p3_sta	pcie_tl_ck_cg_p2_sta	pcie_tl_ck_cg_p1_sta	pcie_tl_ck_cg_p0_sta	ssusb_sdin_ck_cg_p1_sta	ssusb_sdin_ck_cg_p0_sta	ssusb_scl_ck_cg_p1_sta	ssusb_scl_ck_cg_p0_sta
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ssusb_xhci_ck_cg_p1_sta	ssusb_xhci_ck_cg_p0_sta	ssubs_utmi_ck_cg_p1_sta	ssubs_utmi_ck_cg_p0_sta	ssubs_pipe_ck_cg_p1_sta	ssubs_pipe_ck_cg_p0_sta	ssusb_rmcnt_ck_cg_p1_sta	ssusb_rmcnt_ck_cg_p0_sta	ssusb_rmcnt_ef_ck_cg_p1_sta	ssusb_rmcnt_ef_ck_cg_p0_sta	ssubs_rmcnt_ck_cg_p1_sta	ssubs_rmcnt_ck_cg_p0_sta	ssusb_66m_ck_cg_p1_sta	ssusb_66m_ck_cg_p0_sta	ssusb_133m_ck_cg_p1_sta	ssusb_133m_ck_cg_p0_sta
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	pcie_bclk_ck_cg_p3_sta	SSUSB SDIN SWCG STA 0: Enable 1: Disable
30	pcie_bclk_ck_cg_p2_sta	SSUSB SDIN SWCG STA 0: Enable 1: Disable
29	pcie_bclk_ck_cg_p1_sta	SSUSB SDIN SWCG STA 0: Enable 1: Disable
28	pcie_bclk_ck_cg_p0_sta	SSUSB SDIN SWCG STA 0: Enable 1: Disable
27	pcie_pipe_ck_cg_p3_sta	SSUSB SDIN SWCG STA 0: Enable 1: Disable
26	pcie_pipe_ck_cg_p2_sta	SSUSB SDIN SWCG STA 0: Enable 1: Disable
25	pcie_pipe_ck_cg_p1_sta	SSUSB SDIN SWCG STA 0: Enable 1: Disable
24	pcie_pipe_ck_cg_p0_sta	SSUSB SDIN SWCG STA

Bit(s)	Name	Description
		0: Enable
		1: Disable
23	pcie_tl_ck_cg_p3_sta	SSUSB SDIN SWCG STA
		0: Enable
		1: Disable
22	pcie_tl_ck_cg_p2_sta	SSUSB SDIN SWCG STA
		0: Enable
		1: Disable
21	pcie_tl_ck_cg_p1_sta	SSUSB SDIN SWCG STA
		0: Enable
		1: Disable
20	pcie_tl_ck_cg_p0_sta	SSUSB SDIN SWCG STA
		0: Enable
		1: Disable
19	ssusb_sdin_ck_cg_p1_sta	SSUSB SDIN SWCG STA
		0: Enable
		1: Disable
18	ssusb_sdin_ck_cg_sta	SSUSB SDIN SWCG STA
		0: Enable
		1: Disable
17	ssusb_scl_ck_cg_p1_sta	SSUSB SDIN SWCG STA
		0: Enable
		1: Disable
16	ssusb_scl_ck_cg_sta	SSUSB SDIN SWCG STA
		0: Enable
		1: Disable
15	ssusb_xhci_ck_cg_p1_sta	SSUSB SDIN SWCG STA
		0: Enable
		1: Disable
14	ssusb_xhci_ck_cg_sta	PCIe BCLK SWCG STA
		0: Enable
		1: Disable

Bit(s)	Name	Description
13	ssubs_utmi_ck_cg_p1_sta	PCIe REF SWCG STA 0: Enable 1: Disable
12	ssusb_utmi_ck_cg_sta	PCIe PIPE SWCG STA 0: Enable 1: Disable
11	ssubs_pipe_ck_cg_p1_sta	PCIe TL SWCG STA 0: Enable 1: Disable
10	ssubs_pipe_ck_cg_sta	SSUSB SDIN SWCG STA 0: Enable 1: Disable
9	ssusb_frmcnt_ck_cg_p1_sta	SSUSB SCL SWCG STA 0: Enable 1: Disable
8	ssusb_frmcnt_ck_cg_sta	SSUSB XHCI SWCG STA 0: Enable 1: Disable
7	ssusb_ref_ck_cg_p1_sta	SSUSB UTMI 1P SWCG STA 0: Enable 1: Disable
6	ssusb_ref_ck_cg_sta	SSUSB UTMI SWCG STA 0: Enable 1: Disable
5	ssubs_sys_ck_cg_p1_sta	SSUSB PIPE SWCG STA 0: Enable 1: Disable
4	ssubs_sys_ck_cg_sta	SSUSB FRMCNT SWCG STA 0: Enable 1: Disable
3	ssusb_66m_ck_cg_p1_sta	SSUSB REF SWCG STA 0: Enable

Bit(s)	Name	Description
		1: Disable
2	ssusb_66m_ck_cg_sta	SSUSB SYS SWCG STA 0: Enable 1: Disable
1	ssusb_133m_ck_cg_p1_sta	SSUSB 66M SWCG STA 0: Enable 1: Disable
0	ssusb_133m_ck_cg_sta	SSUSB 133M SWCG STA 0: Enable 1: Disable

10001070 **INFRA_GLOBALCON_RST0_SE** Infrasy Always-on reset control register

00000000

I

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															trng_swrst_set	sys_cirq_swrst_set
Type															WO	WO
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	debugtop_swrst_set	cq_dma_swrst_set	audio_swrst_set	infra2conn_gals_mst_swrst_set	conn2infra_gals_slv_swrst_set	conn2emi_m1_gals_slv_swrst_set	conn2emi_m0_gals_slv_swrst_set	eip97_swrst_set	ssusb_swrst_set	pextp_mac_swrst_set	netSYS2infra_gals_slv_swrst_set	netSYS2emi_m1_gals_slv_swrst_set	netSYS2emi_m0_gals_slv_swrst_set	infra2n_etsys_gals_mst_swrst_set	fake_emio1_swrst_set	fake_emio0_swrst_set
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	trng_swrst_set	0: Normal 1: Enable reset
16	sys_cirq_swrst_set	0: Normal 1: Enable reset
15	debugtop_swrst_set	0: Normal 1: Enable reset
14	cq_dma_swrst_set	0: Normal 1: Enable reset
13	audio_swrst_set	0: Normal 1: Enable reset
12	infra2conn_gals_mst_swrst_set	0: Normal 1: Enable reset
11	conn2infra_gals_slv_swrst_set	0: Normal 1: Enable reset
10	conn2emi_m1_gals_slv_swrst_set	0: Normal 1: Enable reset
9	conn2emi_m0_gals_slv_swrst_set	0: Normal 1: Enable reset
8	eip97_swrst_set	0: Normal 1: Enable reset
7	ssusb_swrst_set	0: Normal 1: Enable reset

Bit(s)	Name	Description
6	pextp_mac_swrst_set	0: Normal 1: Enable reset
5	netsys2infra_gals_slv_swrst_set	0: Normal 1: Enable reset
4	netsys2emi_m1_gals_slv_swrst_set	0: Normal 1: Enable reset
3	netsys2emi_m0_gals_slv_swrst_set	0: Normal 1: Enable reset
2	infra2netsys_gals_mst_swrst_set	0: Normal 1: Enable reset
1	fake_emi1_swrst_set	0: Normal 1: Enable reset
0	fake_emi0_swrst_set	0: Normal 1: Enable reset

10001074 **INFRA_GLOBALCON_RST0_CL** Infrasy Always-on reset control register

00000000

R

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															trng_swrst_clr	sys_cirq_swrst_clr
Type															WO	WO
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	debugtop_swrst_clr	cq_dma_swrst_clr	audio_swrst_clr	infra2conn_gals_mst_swrst_clr	conn2infra_gals_slv_swrst_clr	conn2emi_m1_gals_slv_swrst_clr	conn2emi_m0_gals_slv_swrst_clr	eip97_swrst_clr	ssusb_swrst_clr	pextp_mac_swrst_clr	netSYS2infra_gals_slv_swrst_clr	netSYS2emi_m1_gals_slv_swrst_clr	netSYS2emi_m0_gals_slv_swrst_clr	infra2nemi_m1_gals_slv_swrst_clr	fake_e_mi1_swrst_clr	fake_e_mi0_swrst_clr
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	trng_swrst_clr	0: Normal 1: Enable reset
16	sys_cirq_swrst_clr	0: Normal 1: Enable reset
15	debugtop_swrst_clr	0: Normal 1: Enable reset
14	cq_dma_swrst_clr	0: Normal 1: Enable reset
13	audio_swrst_clr	0: Normal 1: Enable reset
12	infra2conn_gals_mst_swrst_clr	0: Normal 1: Enable reset
11	conn2infra_gals_slv_swrst_clr	0: Normal 1: Enable reset
10	conn2emi_m1_gals_slv_swrst_clr	0: Normal 1: Enable reset
9	conn2emi_m0_gals_slv_swrst_clr	0: Normal 1: Enable reset
8	eip97_swrst_clr	0: Normal 1: Enable reset
7	ssusb_swrst_clr	0: Normal 1: Enable reset

Bit(s)	Name	Description
6	pextp_mac_swrst_clr	0: Normal 1: Enable reset
5	netsys2infra_gals_slv_swrst_clr	0: Normal 1: Enable reset
4	netsys2emi_m1_gals_slv_swrst_clr	0: Normal 1: Enable reset
3	netsys2emi_m0_gals_slv_swrst_clr	0: Normal 1: Enable reset
2	infra2netsys_gals_mst_swrst_clr	0: Normal 1: Enable reset
1	fake_emi1_swrst_clr	0: Normal 1: Enable reset
0	fake_emi0_swrst_clr	0: Normal 1: Enable reset

10001078 **INFRA_GLOBALCON_RST0_ST** Infrasy Always-on reset control register

00000000

A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															trng_swrst_sta	sys_cirq_swrst_sta
Type															RO	RO
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	debugtop_swrst_sta	cq_dma_swrst_sta	audio_swrst_sta	infra2conn_gals_mst_swrst_sta	conn2infra_gals_slv_swrst_sta	conn2emi_m1_gals_slv_swrst_sta	conn2emi_m0_gals_slv_swrst_sta	eip97_swrst_sta	ssusb_swrst_sta	pextp_mac_swrst_sta	netSYS2infra_gals_slv_swrst_sta	netSYS2emi_m1_gals_slv_swrst_sta	netSYS2emi_m0_gals_slv_swrst_sta	infra2netSYS_gals_mst_swrst_sta	fake_emio1_swrst_sta	fake_emio0_swrst_sta
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	trng_swrst_sta	0: Normal 1: Enable reset
16	sys_cirq_swrst_sta	0: Normal 1: Enable reset
15	debugtop_swrst_sta	0: Normal 1: Enable reset
14	cq_dma_swrst_sta	0: Normal 1: Enable reset
13	audio_swrst_sta	0: Normal 1: Enable reset
12	infra2conn_gals_mst_swrst_sta	0: Normal 1: Enable reset
11	conn2infra_gals_slv_swrst_sta	0: Normal 1: Enable reset
10	conn2emi_m1_gals_slv_swrst_sta	0: Normal 1: Enable reset
9	conn2emi_m0_gals_slv_swrst_sta	0: Normal 1: Enable reset
8	eip97_swrst_sta	0: Normal 1: Enable reset
7	ssusb_swrst_sta	0: Normal 1: Enable reset

Bit(s)	Name	Description
6	pextp_mac_swrst_sta	0: Normal 1: Enable reset
5	netsys2infra_gals_slv_swrst_sta	0: Normal 1: Enable reset
4	netsys2emi_m1_gals_slv_swrst_sta	0: Normal 1: Enable reset
3	netsys2emi_m0_gals_slv_swrst_sta	0: Normal 1: Enable reset
2	infra2netsys_gals_mst_swrst_sta	0: Normal 1: Enable reset
1	fake_emi1_swrst_sta	0: Normal 1: Enable reset
0	fake_emi0_swrst_sta	0: Normal 1: Enable reset

10001080 **INFRA_GLOBALCON_RST1_SE** Infrasy Always-on reset control register

00000000

I

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		msdc0_swrst_set	i2c_pwr_gate_grst_set	spi2_swrst_set	auxadc_swrst_set	ptp_h_swrst_set	ptp_therm_swrst_set	ptp_swrst_set	uart2_swrst_set	uart1_swrst_set	uart0_swrst_set	spi1_swrst_set	spi0_swrst_set	nfi_swrst_set	i2c_swrst_set	ap_dma_swrst_set
Type		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	msdc0_swrst_set	0: Normal 1: Enable reset
13	i2c_pwr_gate_grst_set	0: Normal 1: Enable reset
12	spi2_swrst_set	0: Normal 1: Enable reset
11	auxadc_swrst_set	0: Normal 1: Enable reset
10	ptp_h_swrst_set	0: Normal 1: Enable reset
9	ptp_therm_swrst_set	0: Normal 1: Enable reset
8	ptp_swrst_set	0: Normal 1: Enable reset
7	uart2_swrst_set	0: Normal 1: Enable reset
6	uart1_swrst_set	0: Normal 1: Enable reset
5	uart0_swrst_set	0: Normal 1: Enable reset
4	spi1_swrst_set	0: Normal 1: Enable reset
3	spi0_swrst_set	0: Normal

Bit(s)	Name	Description
		1: Enable reset
2	nfi_swrst_set	0: Normal
		1: Enable reset
1	i2c_swrst_set	0: Normal
		1: Enable reset
0	ap_dma_swrst_set	0: Normal
		1: Enable reset

10001084 **INFRA_GLOBALCON_RST1_CL** Infrasy Always-on reset control register

00000000

R

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		msdc0_swrst_clr	i2c_pwr_gate_grst_clr	spi2_swrst_clr	auxadc_swrst_clr	ptp_h_swrst_clr	ptp_therm_swrst_clr	ptp_swrst_clr	uart2_swrst_clr	uart1_swrst_clr	uart0_swrst_clr	spi1_swrst_clr	spi0_swrst_clr	nfi_swrst_clr	i2c_swrst_clr	ap_dma_swrst_clr
Type		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	msdc0_swrst_clr	0: Normal 1: Enable reset
13	i2c_pwr_gate_grst_clr	0: Normal 1: Enable reset
12	spi2_swrst_clr	0: Normal 1: Enable reset
11	auxadc_swrst_clr	0: Normal 1: Enable reset
10	ptp_h_swrst_clr	0: Normal 1: Enable reset
9	ptp_therm_swrst_clr	0: Normal 1: Enable reset
8	ptp_swrst_clr	0: Normal 1: Enable reset
7	uart2_swrst_clr	0: Normal 1: Enable reset
6	uart1_swrst_clr	0: Normal 1: Enable reset
5	uart0_swrst_clr	0: Normal 1: Enable reset
4	spi1_swrst_clr	0: Normal 1: Enable reset
3	spi0_swrst_clr	0: Normal

Bit(s)	Name	Description
		1: Enable reset
2	nfi_swrst_clr	0: Normal
		1: Enable reset
1	i2c_swrst_clr	0: Normal
		1: Enable reset
0	ap_dma_swrst_clr	0: Normal
		1: Enable reset

10001088 **INFRA_GLOBALCON_RST1_ST** Infrasy Always-on reset control register

00000000

A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		msdc0_swrst_sta	i2c_pwr_gate_grst_sta	spi2_swrst_sta	auxadc_swrst_sta	ptp_h_swrst_sta	ptp_therm_swrst_sta	ptp_swrst_sta	uart2_swrst_sta	uart1_swrst_sta	uart0_swrst_sta	spi1_swrst_sta	spi0_swrst_sta	nfi_swrst_sta	i2c_swrst_sta	ap_dma_swrst_sta
Type		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	msdc0_swrst_sta	0: Normal 1: Enable reset
13	i2c_pwr_gate_grst_sta	0: Normal 1: Enable reset
12	spi2_swrst_sta	0: Normal 1: Enable reset
11	auxadc_swrst_sta	0: Normal 1: Enable reset
10	ptp_h_swrst_sta	0: Normal 1: Enable reset
9	ptp_therm_swrst_sta	0: Normal 1: Enable reset
8	ptp_swrst_sta	0: Normal 1: Enable reset
7	uart2_swrst_sta	0: Normal 1: Enable reset
6	uart1_swrst_sta	0: Normal 1: Enable reset
5	uart0_swrst_sta	0: Normal 1: Enable reset
4	spi1_swrst_sta	0: Normal 1: Enable reset
3	spi0_swrst_sta	0: Normal

Bit(s)	Name	Description
		1: Enable reset
2	nfi_swrst_sta	0: Normal
		1: Enable reset
1	i2c_swrst_sta	0: Normal
		1: Enable reset
0	ap_dma_swrst_sta	0: Normal
		1: Enable reset

10001090 **INFRA_GLOBALCON_RST2_SE** Infrasy Always-on reset control register

00000000

I

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												pwm_s wrst_s et	debugt op_ao_ swrst_s et	apxgpt _swrst _set	infracfg _ao_m em_reg _swrst _set	ap_cirq _eint_s wrst_s et
Type												WO	WO	WO	WO	WO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	pwm_swrst_set	0: Normal 1: Enable reset
3	debugtop_ao_swrst_set	0: Normal 1: Enable reset
2	apxgpt_swrst_set	0: Normal 1: Enable reset
1	infracfg_ao_mem_reg_swrst_set	0: Normal 1: Enable reset
0	ap_cirq_eint_swrst_set	0: Normal 1: Enable reset

10001094 INFRA_GLOBALCON_RST2_CL Infrasy Always-on reset control register

00000000

R

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												pwm_s wrst_cl r	debugt op_ao_ swrst_c lr	apxgpt _swrst _clr	infracfg _ao_m em_reg _swrst _clr	ap_cirq _eint_s wrst_cl r
Type												WO	WO	WO	WO	WO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	pwm_swrst_clr	0: Normal 1: Enable reset
3	debugtop_ao_swrst_clr	0: Normal 1: Enable reset
2	apxgpt_swrst_clr	0: Normal 1: Enable reset
1	infracfg_ao_mem_reg_swrst_clr	0: Normal 1: Enable reset
0	ap_cirq_eint_swrst_clr	0: Normal 1: Enable reset

10001098 INFRA_GLOBALCON_RST2_ST Infrasy Always-on reset control register

00000000

A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												pwm_s wrst_sta	debugt op_ao_ swrst_s ta	apxgpt _swrst _sta	infracfg _ao_m em_reg _swrst _sta	ap_cirq _eint_s wrst_s ta
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	pwm_swrst_sta	0: Normal 1: Enable reset
3	debugtop_ao_swrst_sta	0: Normal 1: Enable reset
2	apxgpt_swrst_sta	0: Normal 1: Enable reset
1	infracfg_ao_mem_reg_swrst_sta	0: Normal 1: Enable reset
0	ap_cirq_eint_swrst_sta	0: Normal 1: Enable reset

10001100 INFRA AO SEC CG CON0 Infra AO CG security enable control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sw_cgen_sen_0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sw_cgen_sen_0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sw_cgen_sen_0	Security protection for Module CG 0

10001104 INFRA AO SEC CG CON1 Infra AO CG security enable control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sw_cgen_sen_1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sw_cgen_sen_1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sw_cgen_sen_1	Security protection for Module CG 1

10001108 INFRA AO SEC CG CON2 Infra AO CG security enable control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sw_cgen_sen_2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sw_cgen_sen_2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sw_cgen_sen_2	Security protection for Module CG 2

10001110 INFRA AO SEC RST CON0 Infra AO RST security enable control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sw_rst_sen_0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sw_rst_sen_0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sw_rst_sen_0	Security protection for Module RST 0

10001114 INFRA AO SEC RST CON1 Infra AO RST security enable control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sw_rst_sen_1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sw_rst_sen_1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sw_rst_sen_1	Security protection for Module RST 1

10001118 INFRA AO SEC RST CON2 Infra AO RST security enable control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sw_rst_sen_2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sw_rst_sen_2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	sw_rst_sen_2	Security protection for Module RST 2

Module name: infracfg_ao_auto_gen_reg Base address: (+0x1000_3000)

Address	Name	Width	Register Function
10003000	<u>EIP_DCM_IDLE</u>	32	Infrasys EIP DCM control register
10003004	<u>EIP_MBIST_PD_CTRL_0</u>	32	Infrasys EIP MBIST PD control register 0
10003008	<u>EMI_APB_RX.CG_MASK</u>	32	infra misc register
1000300C	<u>EMI_MPU_APB_RX.CG_MASK</u>	32	infra misc register
10003010	<u>EMI_MBIST_PD_CTRL_0</u>	32	EMI MBIST PD control 0
10003014	<u>EMI_MBIST_PD_CTRL_1</u>	32	EMI MBIST PD control 1
10003018	<u>PCIE_INTERRUPT_MUX_SEL</u>	32	PCIe interrupt mux select register
1000301C	<u>rg_pcie_irq_ctrl</u>	32	PICe IRQ control register
10003020	<u>PCIE_M_urgent</u>	32	PCIe master urgent
10003024	<u>PCIE_M1_urgent</u>	32	PCIe master1 urgent
10003028	<u>PCIE_M2_urgent</u>	32	PCIe master2 urgent
1000302C	<u>PCIE_M3_urgent</u>	32	PCIe master3 urgent
10003030	<u>PEXTP_SRAM_PD_CTRL_0</u>	32	PCIe SRAM PD control 0
10003034	<u>PEXTP_SRAM_PD_CTRL_1</u>	32	PCIe SRAM PD control 1
10003038	<u>SSUSB_SRAM_PD_CTRL_0</u>	32	SSUSB SRAM PD control 0
1000303C	<u>SSUSB_SRAM_PD_CTRL_1</u>	32	SSUSB SRAM PD control 1
10003040	<u>SSUSB_I2C_MODE_CTRL</u>	32	SSUSB I2C mode control
10003044	<u>CQDMA_SRAM_PD_CTRL</u>	32	CQDMA SRAM PD control
10003048	<u>SRAMROM_MEM_PD_CTRL</u>	32	SRAMROM ROM/RAM power control
1000304C	<u>SRAMROM_MISC</u>	32	SRAMROM MISC register
10003050	<u>AUDIO_SRAM_PD_CTRL</u>	32	Audio SRAM PD control
10003054	<u>infra_ao_debug_mon_sel_0</u>	32	debug_mon_sel_0
10003058	<u>infra_ao_debug_mon_sel_1</u>	32	debug_mon_sel_1
1000305C	<u>infra_ao_debug_mon_sel_2</u>	32	debug_mon_sel_2
10003060	<u>infra_ao_debug_mon_sel_3</u>	32	debug_mon_sel_3
10003064	<u>infra_ao_debug_mon_sel</u>	32	infra_ao_debug_mon_sel
10003068	<u>rg_delsel_0</u>	32	DESEL 0
1000306C	<u>rg_delsel_1</u>	32	DESEL 1
10003070	<u>rg_delsel_2</u>	32	DESEL 2
10003074	<u>rg_delsel_3</u>	32	DESEL 3
10003078	<u>rg_delsel_4</u>	32	DESEL 4
1000307C	<u>rg_delsel_5</u>	32	DESEL 5
10003080	<u>rg_delsel_6</u>	32	DESEL 6
10003084	<u>rg_delsel_7</u>	32	DESEL 7
10003088	<u>rg_delsel_8</u>	32	DESEL 8
1000308C	<u>rg_delsel_9</u>	32	DESEL 9
10003090	<u>rg_delsel_10</u>	32	DESEL 10
10003094	<u>DBG_HUID_0</u>	32	
10003098	<u>DBG_HUID_1</u>	32	
1000309C	<u>DBG_HUID_2</u>	32	
100030A0	<u>DBG_HUID_3</u>	32	
100030A4	<u>DBG_HUK_0</u>	32	
100030A8	<u>DBG_HUK_1</u>	32	
100030AC	<u>DBG_HUK_2</u>	32	
100030B0	<u>DBG_HUK_3</u>	32	
100030B4	<u>DBG_HUK_4</u>	32	
100030B8	<u>DBG_HUK_5</u>	32	

Address	Name	Width	Register Function
100030BC	<u>DBG HUK 6</u>	32	
100030C0	<u>DBG HUK 7</u>	32	
100030C4	<u>DBG HWBDK</u>	32	
100030C8	<u>EFUSE NETSYS SRM RP 0</u>	32	
100030CC	<u>EFUSE NETSYS SRM RP 1</u>	32	
100030D0	<u>EFUSE NETSYS SRM RP 2</u>	32	
100030D4	<u>EFUSE NETSYS SRM RP 3</u>	32	
100030D8	<u>EFUSE INFRA SRM RP 0</u>	32	
100030DC	<u>EFUSE INFRA SRM RP 1</u>	32	
100030E0	<u>EFUSE INFRA SRM RP 2</u>	32	
100030E4	<u>infra debug mon out</u>	32	
100030E8	<u>tops2emi_gals_slpprot</u>	32	
100030EC	<u>tops2emi_gals_slpprot_1</u>	32	
100030F0	<u>tops2infra_gals_slpprot</u>	32	
100030F4	<u>infra2tops_gals_slpprot</u>	32	
100030F8	<u>infra2tops_npu_slpprot_en</u>	32	
100030FC	<u>tops2infra_npu_slpprot_rdy</u>	32	
10003100	<u>master addr extension</u>	32	Master address extension
10003104	<u>CHN EMI MBIST PD CTRL 0</u>	32	reg_chn_emi_mbist_pd_0_CHA
10003108	<u>CHN EMI MBIST PD CTRL 1</u>	32	reg_chn_emi_mbist_pd_1_CHA
1000310C	<u>hang_free_prot_infra_ao</u>	32	hang_free_prot_infra_ao
10003110	<u>hang_free_prot_infra_pd_0</u>	32	hang_free_prot_infra_pd_0
10003114	<u>hang_free_prot_infra_pd_1</u>	32	hang_free_prot_infra_pd_1
10003118	<u>hang_free_prot_peri_ao</u>	32	hang_free_prot_peri_ao
1000311C	<u>hang_free_prot_peri_pd_0</u>	32	hang_free_prot_peri_pd_0
10003120	<u>hang_free_prot_peri_pd_1</u>	32	hang_free_prot_peri_pd_1

10003000 EIP_DCM_IDLE Infrasys EIP DCM control register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																eip_dcm_idle
Type																RW
Reset																1

Bit(s)	Name	Description
0	eip_dcm_idle	Enables EIP DCM idle 0: Disable 1: Enable

10003004 EIP_MBIST_PD_CTRL_0 Infrasys EIP MBIST PD control register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																eip_mbist_pd0_0
Type																RW
Reset																0

Bit(s)	Name	Description
0	eip_mbist_pd0_0	Infrasys EIP MBIST PD control register bit 0: Disable 1: Enable

10003008 EMI APB RX CG MASK infra misc register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																emi_apb_rx_cg_mask
Type																RW
Reset																0

Bit(s)	Name	Description
0	emi_apb_rx_cg_mask	infra misc register for EMI APB RX cg mask 0: Disable 1: Enable

1000300C EMI MPU APB RX CG MASK infra misc register 00000000
K

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																emi_mpu_apb_rx_cg_mask
Type																RW
Reset																0

Bit(s)	Name	Description
0	emi_mpu_apb_rx_cg_mask	infra misc register for EMI mpu APB RX cg mask 0: Disable 1: Enable

10003010 EMI_MBIST_PD_CTRL_0 EMI MBIST PD control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															emi_m bist_pd 0_1	emi_m bist_pd 0_0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	emi_mbist_pd0_1	infra EMI MBIST 0 PD control register 0: Disable 1: Enable
0	emi_mbist_pd0_0	infra EMI MBIST 0 PD control register 0: Disable 1: Enable

10003014 EMI MBIST_PD_CTRL_1 EMI MBIST PD control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															emi_m bist_pd 1_1	emi_m bist_pd 1_0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	emi_mbist_pd1_1	infra EMI MBIST 1 PD control register 0: Disable 1: Enable
0	emi_mbist_pd1_0	infra EMI MBIST 1 PD control register 0: Disable 1: Enable

10003018 PCIE_INTERRUPT_MUX_SEL PCIe interrupt mux select register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																pcie_in errupt _mux_ sel
Type																RW
Reset																0

Bit(s)	Name	Description
0	pcie_interrupt_mux_sel	PCIe interrupt mux select signal 0: PCIe original interrupt signal 1: WED processed interrupt signal

1000301C **rg_pcie_irq_crtl** **PCIe IRQ control register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														rg_pcie_irq_crtl_p3	rg_pcie_irq_crtl_p1	rg_pcie_irq_crtl_p0
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	rg_pcie_irq_crtl_p3	0: Disable PCIe bride to wed, and send IRQ to GIC 1: Enable PCIe bride to wed
1	rg_pcie_irq_crtl_p1	0: Disable PCIe bride to wed, and send IRQ to GIC 1: Enable PCIe bride to wed
0	rg_pcie_irq_crtl_p0	0: Disable PCIe bride to wed, and send IRQ to GIC 1: Enable PCIe bride to wed

10003020 **PCIE_M_urgent** **PCIe master urgent** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																pcie_m_urgent
Type																RW
Reset																0

Bit(s)	Name	Description
0	pcie_m_urgent	PCIe sends urgent to EMI when a large number of transactions are incoming 0: Do not send urgent to EMI 1: Send urgent to EMI

10003024 **PCIE_M1_urgent** PCIe master1 urgent 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																pcie_m1_urgent
Type																RW
Reset																0

Bit(s)	Name	Description
0	pcie_m1_urgent	PCIe sends urgent to EMI when a large number of transactions are incoming 0: Do not send urgent to EMI 1: Send urgent to EMI

10003028 **PCIE_M2_urgent** PCIe master2 urgent 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																pcie_m2_urgent
Type																RW
Reset																0

Bit(s)	Name	Description
0	pcie_m2_urgent	PCIe sends urgent to EMI when a large number of transactions are incoming 0: Do not send urgent to EMI 1: Send urgent to EMI

1000302C PCIE_M3_urgent PCIe master3 urgent 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																pcie_m3_urgent
Type																RW
Reset																0

Bit(s)	Name	Description
0	pcie_m3_urgent	PCIe sends urgent to EMI when a large number of transactions are incoming 0: Do not send urgent to EMI 1: Send urgent to EMI

10003030 PEXTP_SRAM_PD_CTRL_0 PCIe SRAM PD control 0 00FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									pcie_mem_pwr_off_0							
Type									RW							
Reset									1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcie_mem_pwr_off_0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
23:0	pcie_mem_pwr_off_0	infra PCIe SRAM 0 PD control register 0: Power on 1: Power down

10003034 PEXTP SRAM PD_CTRL_1 PCIe SRAM PD control 1 00FFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									pcie_mem_pwr_off_1							
Type									RW							
Reset									1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pcie_mem_pwr_off_1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
23:0	pcie_mem_pwr_off_1	infra PCIe SRAM 1 PD control register
		0: Power on
		1: Power down

10003038 SSUSB SRAM PD_CTRL_0 SSUSB SRAM PD control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ssusb_sram_pd_0											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	ssusb_sram_pd_0	infra SSUSB SRAM 0 PD control register
		0: Disable
		1: Enable

1000303C **SSUSB_SRAM_PD_CTRL_1** SSUSB SRAM PD control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ssusb_sram_pd_1											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	ssusb_sram_pd_1	infra SSUSB SRAM 1 PD control register
		0: Disable
		1: Enable

10003040 **SSUSB_I2C_MODE_CTRL** SSUSB I2C mode control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ssusb_i2c_mode_p1	ssusb_i2c_mode
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	ssusb_i2c_mode_p1	SSUSB I2C mode_p1 control register
		0: Disable
		1: Enable
0	ssusb_i2c_mode	SSUSB I2C mode control register
		0: Disable
		1: Enable

10003044 CQDMA SRAM_PD_CTRL CQDMA SRAM PD control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																cqdma_sram_pd
Type																RW
Reset																0

Bit(s)	Name	Description
0	cqdma_sram_pd	CQDMA SRAM power down control 0: Power on 1: Power down

10003048 **SRAMROM MEM_PD_CTRL** SRAMROM ROM/RAM power control 00000300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						sramrom_ram_pd	sramrom_ram_slpb	sramrom_ram_isointb	sramrom_rom_pd							
Type						RW	RW	RW	RW							
Reset						0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	sramrom_ram_pd	SRAMROM RAM power down control 0: Power on 1: Power down
9	sramrom_ram_slpb	SRAMROM RAM sleep mode control 0: Enable sleep mode 1: Disable sleep mode
8	sramrom_ram_isointb	SRAMROM RAM isolation control 0: Enable isolation 1: Disable isolation
7:0	sramrom_rom_pd	SRAMROM ROM power down control 0: Power on 1: Power down

1000304C **SRAMROM_MISC** **SRAMROM MISC register** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														l2c_sram_early_response_enable	l2c_sram_pdn	sramrom_cg_disable
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	l2c_sram_early_response_enable	L2C SRAM early response feature control 0: Disable l2c_sram write early response feature 1: Enable l2c_sram write early response feature
1	l2c_sram_pdn	When L2C powers down, set this bit to avoid from accessing L2C 0: When L2C SRAM powers on 1: When L2C SRAM powers down
0	sramrom_cg_disable	SRAMROM auto clock gating control 0: Auto clock gating 1: Disable auto clock gating

10003050 **AUDIO SRAM PD_CTRL** Audio SRAM PD control 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																audio_sram_pd
Type																RW
Reset																1

Bit(s)	Name	Description
0	audio_sram_pd	AUDIO SRAM power down control 0: Power on 1: Power down

10003054 **infra_ao_debug_mon_sel_0** debug_mon_sel_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra_ao_debug_mon_sel_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	infra_ao_debug_mon_sel_0	infra_ao_debug_mon_sel_0 0: Default Else: Lookup table

10003058 infra_ao_debug_mon_sel_1 debug_mon_sel_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra_ao_debug_mon_sel_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	infra_ao_debug_mon_sel_1	infra_ao_debug_mon_sel_1
		0: Default
		Else: Lookup table

1000305C infra_ao_debug_mon_sel_2 debug_mon_sel_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra_ao_debug_mon_sel_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	infra_ao_debug_mon_sel_2	infra_ao_debug_mon_sel_2
		0: Default
		Else: Lookup table

10003060 infra_ao_debug_mon_sel_3 debug_mon_sel_3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra_ao_debug_mon_sel_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	infra_ao_debug_mon_sel_3	infra_ao_debug_mon_sel_3
		0: Default
		Else: Lookup table

10003064 infra_ao_debug_mon_sel infra_ao_debug_mon_sel 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												infra_ao_debug_mon_sel				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	infra_ao_debug_mon_sel	infra_ao_debug_mon_sel
		0: Default
		Else: Lookup table

10003068 rg_delsel_0 DESEL 0 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												rg_use_default_delsel_0	rg_delsel_0			
Type												RW	RW			
Reset												1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_delsel_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20	rg_use_default_delsel_0	MBIST configure SRAM delsel 0: Disable 1: Enable
19:0	rg_delsel_0	MBIST configure SRAM delsel 0: Disable 1: Enable

1000306C rg_dsel_1 DESEL 1 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												rg_use_default_dsel_1	rg_dsel_1			
Type												RW	RW			
Reset												1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_dsel_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20	rg_use_default_dsel_1	MBIST configure SRAM dsel 0: Disable 1: Enable
19:0	rg_dsel_1	MBIST configure SRAM dsel 0: Disable 1: Enable

10003070 rg_delsel_2 DESEL 2 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												rg_use_default_delsel_2	rg_delsel_2			
Type												RW	RW			
Reset												1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_delsel_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20	rg_use_default_delsel_2	MBIST configure SRAM delsel 0: Disable 1: Enable
19:0	rg_delsel_2	MBIST configure SRAM delsel 0: Disable 1: Enable

10003074 rg_delsel_3 DESEL 3 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												rg_use_default_delsel_3	rg_delsel_3			
Type												RW	RW			
Reset												1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_delsel_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20	rg_use_default_delsel_3	MBIST configure SRAM delsel 0: Disable 1: Enable
19:0	rg_delsel_3	MBIST configure SRAM delsel 0: Disable 1: Enable

10003078 rg_dtsel_4 DESEL 4 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												rg_use_default_dtsel_4	rg_dtsel_4			
Type												RW	RW			
Reset												1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_dtsel_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20	rg_use_default_dtsel_4	MBIST configure SRAM dtsel 0: Disable 1: Enable
19:0	rg_dtsel_4	MBIST configure SRAM dtsel 0: Disable 1: Enable

1000307C rg_dsel_5 DESEL 5 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												rg_use_default_dsel_5	rg_dsel_5			
Type												RW	RW			
Reset												1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_dsel_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20	rg_use_default_dsel_5	MBIST configure SRAM dsel 0: Disable 1: Enable
19:0	rg_dsel_5	MBIST configure SRAM dsel 0: Disable 1: Enable

10003080 rg_delsel_6 DESEL 6 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												rg_use_default_delsel_6	rg_delsel_6			
Type												RW	RW			
Reset												1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_delsel_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20	rg_use_default_delsel_6	MBIST configure SRAM delsel 0: Disable 1: Enable
19:0	rg_delsel_6	MBIST configure SRAM delsel 0: Disable 1: Enable

10003084 rg_dtsel_7 DESEL 7 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												rg_use_default_dtsel_7	rg_dtsel_7			
Type												RW	RW			
Reset												1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_dtsel_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20	rg_use_default_dtsel_7	MBIST configure SRAM dtsel 0: Disable 1: Enable
19:0	rg_dtsel_7	MBIST configure SRAM dtsel 0: Disable 1: Enable

10003088 rg_dtsel_8 DESEL 8 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												rg_use_default_dtsel_8	rg_dtsel_8			
Type												RW	RW			
Reset												1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_dtsel_8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20	rg_use_default_dtsel_8	MBIST configure SRAM dtsel 0: Disable 1: Enable
19:0	rg_dtsel_8	MBIST configure SRAM dtsel 0: Disable 1: Enable

1000308C rg_dsel_9 DESEL 9 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												rg_use_default_dsel_9	rg_dsel_9			
Type												RW	RW			
Reset												1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_dsel_9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20	rg_use_default_dsel_9	MBIST configure SRAM dsel 0: Disable 1: Enable
19:0	rg_dsel_9	MBIST configure SRAM dsel 0: Disable 1: Enable

10003090 rg_delsel_10 DESEL 10 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												rg_use_default_delsel_10	rg_delsel_10			
Type												RW	RW			
Reset												1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_delsel_10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20	rg_use_default_delsel_10	MBIST configure SRAM delsel 0: Disable 1: Enable
19:0	rg_delsel_10	MBIST configure SRAM delsel 0: Disable 1: Enable

10003094 DBG_HUID_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dbg_huid_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dbg_huid_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	dbg_huid_0	Test eFuse s2p_rx gets value or not 0: Not blown 1: Blown

10003098 **DBG_HUID_1** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dbg_huid_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dbg_huid_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	dbg_huid_1	Test eFuse s2p_rx gets value or not 0: Not blown 1: Blown

1000309C **DBG_HUID_2** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dbg_huid_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dbg_huid_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	dbg_huid_2	Test eFuse s2p_rx gets value or not 0: Not blown 1: Blown

100030A0 **DBG_HUID_3** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dbg_huid_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dbg_huid_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	dbg_huid_3	Test eFuse s2p_rx gets value or not 0: Not blown 1: Blown

100030A4 **DBG_HUK_0** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dbg_huk_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dbg_huk_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	dbg_huk_0	Test eFuse s2p_rx gets value or not 0: Not blown 1: Blown

100030A8 DBG_HUK_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dbg_huk_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dbg_huk_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	dbg_huk_1	Test eFuse s2p_rx gets value or not 0: Not blown 1: Blown

100030AC DBG_HUK_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dbg_huk_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dbg_huk_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	dbg_huk_2	Test eFuse s2p_rx gets value or not 0: Not blown 1: Blown

100030B0 **DBG_HUK_3** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dbg_huk_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dbg_huk_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	dbg_huk_3	Test eFuse s2p_rx gets value or not 0: Not blown 1: Blown

100030B4 **DBG_HUK_4** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dbg_huk_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dbg_huk_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	dbg_huk_4	Test eFuse s2p_rx gets value or not 0: Not blown 1: Blown

100030B8 **DBG_HUK_5** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dbg_huk_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dbg_huk_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	dbg_huk_5	Test eFuse s2p_rx gets value or not 0: Not blown 1: Blown

100030BC **DBG_HUK_6** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dbg_huk_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dbg_huk_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	dbg_huk_6	Test eFuse s2p_rx gets value or not 0: Not blown 1: Blown

100030C0 **DBG_HUK_7** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dbg_huk_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dbg_huk_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	dbg_huk_7	Test eFuse s2p_rx gets value or not 0: Not blown 1: Blown

100030C4 **DBG_HWBDK** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															dbg_hwbdk_disable	dbg_hwbdk_valid
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	dbg_hwbdk_disable	Test eFuse s2p_rx gets value or not 0: Not blown 1: Blown
0	dbg_hwbdk_valid	Test eFuse s2p_rx gets value or not 0: Not blown 1: Blown

100030C8 EFUSE_NETSYS_SRM_RP_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	efuse_netsys_srm_rp_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	efuse_netsys_srm_rp_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	efuse_netsys_srm_rp_0	Test eFuse s2p_rx gets value or not 0: Blown 1: Not blown

100030CC EFUSE_NETSYS_SRM_RP_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	efuse_netsys_srm_rp_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	efuse_netsys_srm_rp_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	efuse_netsys_srm_rp_1	Test eFuse s2p_rx gets value or not 0: Blown 1: Not blown

100030D0 EFUSE_NETSYS_SRM_RP_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	efuse_netsys_srm_rp_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	efuse_netsys_srm_rp_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	efuse_netsys_srm_rp_2	Test eFuse s2p_rx gets value or not 0: Blown 1: Not blown

100030D4 EFUSE_NETSYS_SRM_RP_3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									efuse_netsys_srm_rp_3							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	efuse_netsys_srm_rp_3	Test eFuse s2p_rx gets value or not 0: Blown 1: Not blown

100030D8 EFUSE INFRA SRM RP_0 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	efuse_infra_srm_rp_0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	efuse_infra_srm_rp_0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	efuse_infra_srm_rp_0	Test eFuse s2p_rx gets value or not 0: Blown 1: Not blown

100030DC EFUSE INFRA SRM RP_1 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	efuse_infra_srm_rp_1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	efuse_infra_srm_rp_1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	efuse_infra_srm_rp_1	Test eFuse s2p_rx gets value or not 0: Blown 1: Not blown

100030E0 EFUSE INFRA SRM RP_2 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	efuse_infra_srm_rp_2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	efuse_infra_srm_rp_2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	efuse_infra_srm_rp_2	Test eFuse s2p_rx gets value or not 0: Blown 1: Not blown

100030E4 infra_debug_mon_out 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	infra_debug_mon_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra_debug_mon_out															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	infra_debug_mon_out	infra_debug_mon_out 0: Disable Others: Lookup table

100030E8 tops2emi_gals_slpprot 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								tops2emi_gals_rx_slpprot_en_comb				tops2emi_gals_rx_slpprot_rdy		tops2emi_gals_rx_slpprot_en		
Type								RO				RO		RW		
Reset								0				0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												tops2emi_gals_tx_slpprot_rdy		tops2emi_gals_tx_slpprot_en		
Type												RO		RW		
Reset												0		0	0	0

Bit(s)	Name	Description
24	tops2emi_gals_rx_slpprot_en_comb	
20	tops2emi_gals_rx_slpprot_rdy	
18:16	tops2emi_gals_rx_slpprot_en	
4	tops2emi_gals_tx_slpprot_rdy	
2:0	tops2emi_gals_tx_slpprot_en	

100030EC tops2emi_gals_slpprot_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								tops2emi_gals_rx_slpprot_en_comb_1				tops2emi_gals_rx_slpprot_rdy_1		tops2emi_gals_rx_slpprot_en_1		
Type								RO				RO		RW		
Reset								0				0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												tops2emi_gals_tx_slpprot_rdy_1		tops2emi_gals_tx_slpprot_en_1		
Type												RO		RW		
Reset												0		0	0	0

Bit(s)	Name	Description
24	tops2emi_gals_rx_slpprot_en_comb_1	
20	tops2emi_gals_rx_slpprot_rdy_1	
18:16	tops2emi_gals_rx_slpprot_en_1	
4	tops2emi_gals_tx_slpprot_rdy_1	
2:0	tops2emi_gals_tx_slpprot_en_1	

100030F0 tops2infra_gals_slpprot 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								tops2in fra_gal s_rx_sl pprot_r dy								tops2in fra_gal s_rx_sl pprot_ en
Type								RO								RW
Reset								0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												tops2in fra_gal s_tx_sl pprot_r dy				tops2in fra_gal s_tx_sl pprot_ en
Type												RO				RW
Reset												0				0

Bit(s)	Name	Description
24	tops2infra_gals_rx_slpprot_rdy	
16	tops2infra_gals_rx_slpprot_en	
4	tops2infra_gals_tx_slpprot_rdy	
0	tops2infra_gals_tx_slpprot_en	

100030F4 infra2tops_gals_slpprot 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								infra2t ops_gal s_rx_sl pprot_r dy								infra2t ops_ga ls_rx_sl pprot_ en
Type								RO								RW
Reset								0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												infra2t ops_gal s_tx_sl pprot_r dy				infra2t ops_ga ls_tx_sl pprot_ en
Type												RO				RW
Reset												0				0

Bit(s)	Name	Description
24	infra2tops_gals_rx_slpprot_rdy	
16	infra2tops_gals_rx_slpprot_en	
4	infra2tops_gals_tx_slpprot_rdy	
0	infra2tops_gals_tx_slpprot_en	

100030F8 infra2tops_npu_slpprot_en 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					infra2tops_npu_slpprot_en2											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra2tops_npu_slpprot_en2										infra2tops_npu_slpprot_en1					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
27:8	infra2tops_npu_slpprot_en2	
5:0	infra2tops_npu_slpprot_en1	

100030FC tops2infra_npu_slpprot_rdy 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					tops2infra_npu_slpprot_rdy2											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tops2infra_npu_slpprot_rdy2										tops2infra_npu_slpprot_rdy1					
Type	RO										RO					
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
27:8	tops2infra_npu_slpprot_rdy2	
5:0	tops2infra_npu_slpprot_rdy1	

10003100 master_addr_extension Master address extension 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	master_addr_extension															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	master_addr_extension															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	master_addr_extension	

10003104 CHN_EMI_MBIST_PD_CTRL_0 reg_chn_emi_mbist_pd_0_CHA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															chn_emi_mbist_pd0_1	chn_emi_mbist_pd0_0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	chn_emi_mbist_pd0_1	infra channel EMI MBIST 0 PD control register 0: Disable 1: Enable
0	chn_emi_mbist_pd0_0	infra channel EMI MBIST 0 PD control register 0: Disable 1: Enable

10003108 CHN_EMI_MBIST_PD_CTRL_1 reg_chn_emi_mbist_pd_1_CHA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															chn_emi_mbist_pd1_1	chn_emi_mbist_pd1_0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	chn_emi_mbist_pd1_1	infra channel EMI MBIST 1 PD control register 0: Disable 1: Enable
0	chn_emi_mbist_pd1_0	infra channel EMI MBIST 1 PD control register 0: Disable 1: Enable

1000310C hang_free_prot_infra_ao hang_free_prot_infra_ao FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hang_free_prot_infra_ao															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hang_free_prot_infra_ao															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	hang_free_prot_infra_ao	

10003110 hang_free_prot_infra_pd_0 hang_free_prot_infra_pd_0 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hang_free_prot_infra_pd_0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hang_free_prot_infra_pd_0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	hang_free_prot_infra_pd_0	

10003114 hang_free_prot_infra_pd_1 hang_free_prot_infra_pd_1 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hang_free_prot_infra_pd_1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hang_free_prot_infra_pd_1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	hang_free_prot_infra_pd_1	

10003118 hang_free_prot_peri_ao hang_free_prot_peri_ao FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hang_free_prot_peri_ao															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hang_free_prot_peri_ao															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	hang_free_prot_peri_ao	

1000311C hang_free_prot_peri_pd_0 hang_free_prot_peri_pd_0 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hang_free_prot_peri_pd_0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hang_free_prot_peri_pd_0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description

31:0	hang_free_prot_peri_pd_0	

10003120 hang_free_prot_peri_pd_1 hang_free_prot_peri_pd_1 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hang_free_prot_peri_pd_1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hang_free_prot_peri_pd_1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description

31:0	hang_free_prot_peri_pd_1	

Module name: infracfg Base address: (+0x1020_9000)

Address	Name	Width	Register Function
10209004	<u>INFRASYS_NETSYS_SLPPROT</u>	32	netsys related GALS sleep protect enable
10209008	<u>INFRASYS_NETSYS_BIST_CON_0</u>	32	netsys related GALS BIST control register 0
1020900C	<u>INFRASYS_NETSYS_BIST_CON_1</u>	32	netsys related GALS BIST control register 1
10209010	<u>INFRASYS_NETSYS_BIST_CON_2</u>	32	netsys related GALS BIST control register 2
10209014	<u>INFRASYS_TOPS_SLPPROT</u>	32	TOPS related GALS sleep protect enable
10209018	<u>INFRASYS_TOPS_BIST_CON_0</u>	32	TOPS related GALS BIST control register 0
1020901C	<u>INFRASYS_TOPS_BIST_CON_1</u>	32	TOPS related GALS BIST control register 1
10209020	<u>INFRASYS_TOPS_BIST_CON_2</u>	32	TOPS related GALS BIST control register 2
10209024	<u>TOPS2EMI0_GALS_DBG</u>	32	TOP2EMI0 GALS debug read
10209028	<u>TOPS2EMI1_GALS_DBG</u>	32	TOP2EMI1 GALS debug read
1020902C	<u>TOPS2AP_GALS_DBG</u>	32	TOP2INFRA GALS debug read
10209030	<u>TOPS_GALS_SLV_CTL</u>	32	TOP GALS control setting register
10209034	<u>INFRA2TOPS_GALS_DBG</u>	32	INFRA2TOPS GALS debug read
10209040	<u>INFRA2NETSYS_GALS_DBG</u>	32	INFRA2NETSYS GALS debug read
10209044	<u>INFRA2NETSYS_GALS_MST_CTL</u>	32	NETSYS GALS control setting register
10209048	<u>INFRA2TOPS_GALS_MST_CTL</u>	32	TOPS GALS control setting register
1020904C	<u>NETSYS2INFRA_GALS_DBG</u>	32	NETSYS2INFRA GALS debug read
10209050	<u>NETSYS2EMI_GALS_DBG</u>	32	NETSYS2EMI GALS debug read
10209054	<u>NETSYS_GALS_SLV_CTL</u>	32	NETSYS slave GALS control setting register

10209004 INFRASYS NETSYS SLPPROT netsys related GALS sleep protect enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			netsys2emi_m1_gals_slpprot_rdy_tx	netsys2emi_m1_gals_slpprot_rdy_rx	netsys2infra_gals_slpprot_rdy_tx	netsys2infra_gals_slpprot_rdy_rx	infra2netsys_gals_slpprot_rdy_tx	infra2netsys_gals_slpprot_rdy_rx			netsys2emi_m1_gals_slpprot_en_tx	netsys2emi_m1_gals_slpprot_en_rx	netsys2infra_gals_slpprot_en_tx	netsys2infra_gals_slpprot_en_rx	infra2netsys_gals_slpprot_en_tx	infra2netsys_gals_slpprot_en_rx
Type			RO	RO	RO	RO	RO	RO			RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
13	netsys2emi_m1_gals_slpprot_rdy_tx	netsys2emi_m1 GALS sleep protect TX ready
12	netsys2emi_m1_gals_slpprot_rdy_rx	netsys2emi_m1 GALS sleep protect RX ready
11	netsys2infra_gals_slpprot_rdy_tx	netsys2infra GALS sleep protect TX ready
10	netsys2infra_gals_slpprot_rdy_rx	netsys2infra GALS sleep protect RX ready
9	infra2netsys_gals_slpprot_rdy_tx	infra2netsys GALS sleep protect TX ready
8	infra2netsys_gals_slpprot_rdy_rx	infra2netsys GALS sleep protect RX ready
5	netsys2emi_m1_gals_slpprot_en_tx	netsys2emi_m1 GALS sleep protect TX enable
4	netsys2emi_m1_gals_slpprot_en_rx	netsys2emi_m1 GALS sleep protect RX enable
3	netsys2infra_gals_slpprot_en_tx	netsys2infra GALS sleep protect TX enable
2	netsys2infra_gals_slpprot_en_rx	netsys2infra GALS sleep protect RX enable
1	infra2netsys_gals_slpprot_en_tx	infra2netsys GALS sleep protect TX enable
0	infra2netsys_gals_slpprot_en_rx	infra2netsys GALS sleep protect RX enable

10209008 INFRASYS NETSYS BIST_CON netsys related GALS BIST control register 0

00000000

0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				infra2n etsys_b ist_fail				infra2n etsys_b ist_don e								infra2n etsys_ bist_en
Type				RO				RO								RW
Reset				0				0								0

Bit(s)	Name	Description
12	infra2netsys_bist_fail	infra2netsys BIST fail
8	infra2netsys_bist_done	infra2netsys BIST done
0	infra2netsys_bist_en	infra2netsys BIST enable

1020900C INFRASYS NETSYS BIST_CON netsys related GALS BIST control register 1

FFFFFFF

1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	infra2netsys_bist_ctrl_1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra2netsys_bist_ctrl_1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	infra2netsys_bist_ctrl_1	infra2netsys BIST control register 1

10209010 INFRASYS NETSYS BIST_CON netsys related GALS BIST control register 2

00003FFF

2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			infra2netsys_bist_ctrl_2													
Type			RW													
Reset			1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
13:0	infra2netsys_bist_ctrl_2	infra2netsys BIST control register 2

10209014 **INFRASYS TOPS_SLPPROT** TOPS related GALS sleep protect enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			tops2emi_gals_slpprot_rdy_tx	tops2emi_gals_slpprot_rdy_rx	tops2infra_gals_slpprot_rdy_tx	tops2infra_gals_slpprot_rdy_rx	infra2tops_gals_slpprot_rdy_tx	infra2tops_gals_slpprot_rdy_rx			tops2emi_gals_slpprot_en_tx	tops2emi_gals_slpprot_en_rx	tops2infra_gals_slpprot_en_tx	tops2infra_gals_slpprot_en_rx	infra2tops_gals_slpprot_en_tx	infra2tops_gals_slpprot_en_rx
Type			RO	RO	RO	RO	RO	RO			RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
13	tops2emi_gals_slpprot_rdy_tx	tops2emii_m1 GALS sleep protect TX ready
12	tops2emi_gals_slpprot_rdy_rx	tops2emi_m1 GALS sleep protect RX ready
11	tops2infra_gals_slpprot_rdy_tx	tops2infra GALS sleep protect TX ready
10	tops2infra_gals_slpprot_rdy_rx	tops2infra GALS sleep protect RX ready
9	infra2tops_gals_slpprot_rdy_tx	infra2tops GALS sleep protect TX ready
8	infra2tops_gals_slpprot_rdy_rx	infra2tops GALS sleep protect RX ready
5	tops2emi_gals_slpprot_en_tx	tops2emii_m1 GALS sleep protect TX enable
4	tops2emi_gals_slpprot_en_rx	tops2emi_m1 GALS sleep protect RX enable
3	tops2infra_gals_slpprot_en_tx	tops2infra GALS sleep protect TX enable
2	tops2infra_gals_slpprot_en_rx	tops2infra GALS sleep protect RX enable
1	infra2tops_gals_slpprot_en_tx	infra2tops GALS sleep protect TX enable
0	infra2tops_gals_slpprot_en_rx	infra2tops GALS sleep protect RX enable

10209018 INFRASYS TOPS_BIST_CON_0 TOPS related GALS BIST control register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				infra2t ops_bis t_fail				infra2t ops_bis t_done								infra2t ops_bi st_en
Type				RO				RO								RW
Reset				0				0								0

Bit(s)	Name	Description
12	infra2tops_bist_fail	infra2tops BIST fail
8	infra2tops_bist_done	infra2tops BIST done
0	infra2tops_bist_en	infra2tops BIST enable

1020901C INFRASYS TOPS_BIST_CON_1 TOPS related GALS BIST control register 1 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	infra2tops_bist_ctrl_1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra2tops_bist_ctrl_1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	infra2tops_bist_ctrl_1	infra2tops BIST control register 1

10209020 INFRASYS TOPS_BIST_CON_2 TOPS related GALS BIST control register 2 0003FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															infra2tops_bist_ctrl_2	
Type															RW	
Reset															1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra2tops_bist_ctrl_2															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
17:0	infra2tops_bist_ctrl_2	infra2tops BIST control register 2

10209024 TOPS2EMI0_GALS_DBG TOP2EMI0 GALS debug read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	tops2emi_gals_axi_dbg_slv															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tops2emi_gals_axi_dbg_slv															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	tops2emi_gals_axi_dbg_slv	TOP2EMI0 GALS debug read data

10209028 TOPS2EMI1_GALS_DBG TOP2EMI1 GALS debug read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	tops2emi1_gals_axi_dbg_slv															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tops2emi1_gals_axi_dbg_slv															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	tops2emi1_gals_axi_dbg_slv	TOP2EMI1 GALS debug read data

1020902C TOPS2AP_GALS_DBG TOP2INFRA_GALS debug read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	tops2infra_gals_axi_dbg_slv															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tops2infra_gals_axi_dbg_slv															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	tops2infra_gals_axi_dbg_slv	TOP2INFRA_GALS debug read

10209030 TOPS_GALS_SLV_CTL TOP GALS control setting register 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	tops2infra_gals_slv_ctrl															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tops2infra_gals_slv_ctrl															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	tops2infra_gals_slv_ctrl	tops2infra GALS slave control [1:0]: mst_sync_sel [3:2]: slv_sync_sel [4]: sample_sel [5]: reg_ar_fctrl_en [6]: reg_aw_fctrl_en [9:7]: wthre [15:10]: depth_val tops2emi GALS slave control [17:16]: mst_sync_sel [19:18]: slv_sync_sel [20]: sample_sel [21]: reg_ar_fctrl_en [22]: reg_aw_fctrl_en [25:23]: wthre [31:26]: depth_val

10209034 **INFRA2TOPS_GALS_DBG** INFRA2TOPS GALS debug read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	infra2tops_gals_mst_gals_axi_dbg_mst															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra2tops_gals_mst_gals_axi_dbg_mst															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	infra2tops_gals_mst_gals_axi_dbg_mst	INFRA2TOPS GALS debug read

10209040 **INFRA2NETSYS_GALS_DBG** INFRA2NETSYS GALS debug read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	infra2netsys_gals_mst_gals_axi_dbg_mst															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra2netsys_gals_mst_gals_axi_dbg_mst															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	infra2netsys_gals_mst_gals_axi_dbg_mst	INFRA2NETSYS GALS debug read

10209044 **INFRA2NETSYS_GALS_MST_C** NETSYS GALS control setting register

00000100

TL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								infra2netsys_gals_mst_ctrl								
Type								RW								
Reset								1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	infra2netsys_gals_mst_ctrl	infra2netsys GALS master control [1:0]: mst_sync_sel [3:2]: slv_sync_sel [5:4]: in_awflush_thre [7:6]: in_arflush_thre [8]: sample_sel

10209048 **INFRA2TOPS_GALS_MST_CTL** TOPS GALS control setting register

00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								infra2tops_gals_mst_ctrl								
Type								RW								
Reset								1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	infra2tops_gals_mst_ctrl	infra2tops GALS master control [1:0]: mst_sync_sel [3:2]: slv_sync_sel [5:4]: in_awflush_thre [7:6]: in_arflush_thre [8]: sample_sel

1020904C NETSYS2INFRA_GALS_DBG NETSYS2INFRA GALS debug read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	netsys2emi_m0_gals_slv_gals_axi_dbg_slv															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	netsys2emi_m0_gals_slv_gals_axi_dbg_slv															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	netsys2emi_m0_gals_slv_gals_axi_dbg_slv	TOP2INFRA GALS debug read slv

10209050 NETSYS2EMI_GALS_DBG NETSYS2EMI GALS debug read 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	netsys2infra_gals_slv_gals_axi_dbg_slv															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	netsys2infra_gals_slv_gals_axi_dbg_slv															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	netsys2infra_gals_slv_gals_axi_dbg_slv	TOP2INFRA GALS debug read

10209054 NETSYS_GALS_SLV_CTL NETSYS slave GALS control setting register 00040100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											ro_netsys2infra_m0_gals_slv_rfifo_near_full	ro_netsys2emi_m0_gals_slv_rfifo_near_full	infra2netsys_gals_mst_ctrl			
Type											RO	RO	RW			
Reset											0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	infra2netsys_gals_mst_ctrl															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	ro_netsys2infra_m0_gals_slv_rfifo_near_full	ro_netsys2infra_m0_gals_slv_rfifo_near_full
20	ro_netsys2emi_m0_gals_slv_rfifo_near_full	ro_netsys2emi_m0_gals_slv_rfifo_near_full
19:0	infra2netsys_gals_mst_ctrl	infra2netsys GALS slv control [1:0]: mst_sync_sel [3:2]: slv_sync_sel [7:4]: rfifo_thre [8]: sample_sel [9]: rfifo_near_full_en

Module name: bcrn_FMEM_PDN_wrapper_u_bcrn_FMEM_PDN_bcrn Base address: (+0x1A01_0000)

Address	Name	Width	Register Function
1A010000	<u>INFRA FMEM M0M1 BUS u</u> <u>Ink INFRA FMEM M0M1 B</u> <u>US SL100 to EMI M0 S DC</u> <u>M PROT ups CTRL 0</u>	32	INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL100_to_EMI_M0_S_DCM_PROT_ups control register 0
1A010004	<u>INFRA FMEM M0M1 BUS u</u> <u>Ink INFRA FMEM M0M1 B</u> <u>US SL100 to EMI M0 S DC</u> <u>M PROT CTRL 0</u>	32	INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL100_to_EMI_M0_S_DCM_PROT control register 0
1A010008	<u>INFRA FMEM M0M1 BUS u</u> <u>Ink INFRA FMEM M0M1 B</u> <u>US SL101 to EMI M1 S DC</u> <u>M PROT ups CTRL 0</u>	32	INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL101_to_EMI_M1_S_DCM_PROT_ups control register 0
1A01000C	<u>INFRA FMEM M0M1 BUS u</u> <u>Ink INFRA FMEM M0M1 B</u> <u>US SL101 to EMI M1 S DC</u> <u>M PROT CTRL 0</u>	32	INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL101_to_EMI_M1_S_DCM_PROT control register 0
1A010010	<u>INFRA FMEM M0M1 BUS u</u> <u>SL100 CTRL 0</u>	32	INFRA_FMEM_M0M1_BUS_u_SL100 control register 0
1A010014	<u>INFRA FMEM M0M1 BUS u</u> <u>SL101 CTRL 0</u>	32	INFRA_FMEM_M0M1_BUS_u_SL101 control register 0
1A010018	<u>INFRA FMEM M2 BUS u Ink</u> <u>INFRA FMEM M2 BUS MI3</u> <u>0 to EMI M2 S DCM PROT</u> <u>ups CTRL 0</u>	32	INFRA_FMEM_M2_BUS_u_Ink_INFRA_FMEM_M2_BUS_MI30_to_EMI_M2_S_DCM_PROT_ups control register 0
1A01001C	<u>INFRA FMEM M2 BUS u Ink</u> <u>INFRA FMEM M2 BUS MI3</u> <u>0 to EMI M2 S DCM PROT</u> <u>CTRL 0</u>	32	INFRA_FMEM_M2_BUS_u_Ink_INFRA_FMEM_M2_BUS_MI30_to_EMI_M2_S_DCM_PROT control register 0
1A010020	<u>INFRA FMEM M2 BUS u MI</u> <u>30 CTRL 0</u>	32	INFRA_FMEM_M2_BUS_u_MI30 control register 0
1A010024	<u>INFRA FMEM M4 BUS u Ink</u> <u>INFRA FMEM M4 BUS MIS</u> <u>I8A to INFRA FAXI BUS MIS</u> <u>I1 ASYNC CTRL 0</u>	32	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC control register 0
1A010028	<u>INFRA FMEM M4 BUS u Ink</u> <u>INFRA FMEM M4 BUS MIS</u> <u>I8B to EMI M4 S DCM PRO</u> <u>T ups CTRL 0</u>	32	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8B_to_EMI_M4_S_DCM_PROT_ups control register 0
1A01002C	<u>INFRA FMEM M4 BUS u Ink</u> <u>INFRA FMEM M4 BUS MIS</u> <u>I8B to EMI M4 S DCM PRO</u> <u>T CTRL 0</u>	32	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8B_to_EMI_M4_S_DCM_PROT control register 0
1A010030	<u>INFRA FMEM M4 BUS u SL</u> <u>18 CTRL 0</u>	32	INFRA_FMEM_M4_BUS_u_SL18 control register 0
1A010034	<u>INFRA FMEM M4 BUS u SL</u> <u>44 CTRL 0</u>	32	INFRA_FMEM_M4_BUS_u_SL44 control register 0
1A010038	<u>INFRA FMEM M4 BUS u MI</u> <u>S18A CTRL 0</u>	32	INFRA_FMEM_M4_BUS_u_MISI8A control register 0
1A01003C	<u>INFRA FMEM M4 BUS u MI</u> <u>S18B CTRL 0</u>	32	INFRA_FMEM_M4_BUS_u_MISI8B control register 0
1A010040	<u>INFRA FMEM M5 BUS u Ink</u> <u>INFRA FMEM M5 BUS MI6</u> <u>0 to EMI M5 S DCM PROT</u> <u>ups CTRL 0</u>	32	INFRA_FMEM_M5_BUS_u_Ink_INFRA_FMEM_M5_BUS_MI60_to_EMI_M5_S_DCM_PROT_ups control register 0

Address	Name	Width	Register Function
1A010044	<u>INFRA FMEM M5 BUS u Ink</u> <u>INFRA FMEM M5 BUS MI6</u> <u>0 to EMI M5 S DCM PROT</u> <u>CTRL 0</u>	32	INFRA_FMEM_M5_BUS_u_Ink_INFRA_FMEM_M5_BUS_MI60_to_EMI_M5_S_DCM_PROT control register 0
1A010048	<u>INFRA FMEM M5 BUS u MI</u> <u>60 CTRL 0</u>	32	INFRA_FMEM_M5_BUS_u_MI60 control register 0
1A01004C	<u>INFRA FMEM M6M7 BUS u</u> <u>Ink INFRA FAXI BUS AXI U</u> <u>P PERI to INFRA FMEM M6</u> <u>M7 BUS SL07 ASYNC CTRL</u> <u>0</u>	32	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FAXI_BUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS_SL07_ASYNC control register 0
1A010050	<u>INFRA FMEM M6M7 BUS u</u> <u>Ink INFRA FMEM M6M7 B</u> <u>US SL07 to EMI M7 S DCM</u> <u>PROT ups CTRL 0</u>	32	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL07_to_EMI_M7_S_DCM_PROT_ups control register 0
1A010054	<u>INFRA FMEM M6M7 BUS u</u> <u>Ink INFRA FMEM M6M7 B</u> <u>US SL07 to EMI M7 S DCM</u> <u>PROT CTRL 0</u>	32	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL07_to_EMI_M7_S_DCM_PROT control register 0
1A010058	<u>INFRA FMEM M6M7 BUS u</u> <u>Ink INFRA FMEM M6M7 B</u> <u>US SL30 to EMI M6 S DCM</u> <u>PROT ups CTRL 0</u>	32	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL30_to_EMI_M6_S_DCM_PROT_ups control register 0
1A01005C	<u>INFRA FMEM M6M7 BUS u</u> <u>Ink INFRA FMEM M6M7 B</u> <u>US SL30 to EMI M6 S DCM</u> <u>PROT CTRL 0</u>	32	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL30_to_EMI_M6_S_DCM_PROT control register 0
1A010060	<u>INFRA FMEM M6M7 BUS u</u> <u>SL30 CTRL 0</u>	32	INFRA_FMEM_M6M7_BUS_u_SL30 control register 0
1A010064	<u>INFRA FMEM M6M7 BUS u</u> <u>SL07 CTRL 0</u>	32	INFRA_FMEM_M6M7_BUS_u_SL07 control register 0

1A010000 INFRA_FMEM_M0M1_BUS_u INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM
 _Ink_INFRA_FMEM_M0M1_B_M0M1_BUS_SL100_to_EMI_M0_S_DCM_PROT
 US_SL100_to_EMI_M0_S_DC _ups control register 0
 M_PROT_ups_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FMEM_M0M1_BUS_1_BUS_u_Ink_INFRA_FMEM_A_FMEM_M0M1_BUS_SL100_to_EMI_M0_S_DCM_PROT_ups_axi_clock_gated_en	INFRA_FMEM_M0M1_BUS_1_BUS_u_Ink_INFRA_FMEM_A_FMEM_M0M1_BUS_SL100_to_EMI_M0_S_DCM_PROT_ups_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL100_to_EMI_M0_S_DCM_PROT_ups_axi_clock_gated_en	
0	INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL100_to_EMI_M0_S_DCM_PROT_ups_axi_clock_gated	

1A010004 INFRA_FMEM_M0M1_BUS_u INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM
Ink_INFRA_FMEM_M0M1_B_M0M1_BUS_SL100_to_EMI_M0_S_DCM_PROT
US_SL100_to_EMI_M0_S_DC control register 0
M_PROT_CTRL_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL100_to_EMI_M0_S_DCM_PROT_axi_clock_gated_en	INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL100_to_EMI_M0_S_DCM_PROT_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL100_to_EMI_M0_S_DCM_PROT_axi_clock_gated_en	
0	INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL100_to_EMI_M0_S_DCM_PROT_axi_clock_gated	

1A010008 INFRA_FMEM_M0M1_BUS_u INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM
Ink_INFRA_FMEM_M0M1_B_M0M1_BUS_SL101_to_EMI_M1_S_DCM_PROT
US_SL101_to_EMI_M1_S_DC _ups control register 0
M_PROT_ups_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL101_to_EMI_M1_S_DCM_PROT_ups_axi_clock_gated_en	INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL101_to_EMI_M1_S_DCM_PROT_ups_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL101_to_EMI_M1_S_DCM_PROT_ups_axi_clock_gated_en	
0	INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL101_to_EMI_M1_S_DCM_PROT_ups_axi_clock_gated	

1A01000C INFRA_FMEM_M0M1_BUS_u_INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM
 _Ink_INFRA_FMEM_M0M1_B_M0M1_BUS_SL101_to_EMI_M1_S_DCM_PROT
 US_SL101_to_EMI_M1_S_DC control register 0
 M_PROT_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL101_to_EMI_M1_S_DCM_PROT_axi_clock_gated_en	INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL101_to_EMI_M1_S_DCM_PROT_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL101_to_EMI_M1_S_DCM_PROT_axi_clock_gated_en	
0	INFRA_FMEM_M0M1_BUS_u_Ink_INFRA_FMEM_M0M1_BUS_SL101_to_EMI_M1_S_DCM_PROT_axi_clock_gated	

1A010010

INFRA_FMEM_M0M1_BUS_u INFRA_FMEM_M0M1_BUS_u_SL100 control
SL100_CTRL_0 register 0

0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												INFRA_FMEM_MOM1_BUS_u_SL100_in_arflush_thre		INFRA_FMEM_MOM1_BUS_u_SL100_axiidle_ou	INFRA_FMEM_MOM1_BUS_u_SL100_in_awflush_thre	
Type												RW		RO	RW	
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	INFRA_FMEM_M0M1_BUS__u_SL100__i n_arflush_thre	
2	INFRA_FMEM_M0M1_BUS__u_SL100__ axi_idle_out	
1:0	INFRA_FMEM_M0M1_BUS__u_SL100__i n_awflush_thre	

1A010014 **INFRA_FMEM_MOM1_BUS_u_INFRA_FMEM_MOM1_BUS_u_SL101 control** 0000001F
SL101_CTRL_0 register 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												INFRA_FMEM_MOM1_BUS_u_SL101_in_arflush_thre	INFRA_FMEM_MOM1_BUS_u_SL101_in_awflush_thre			INFRA_FMEM_MOM1_BUS_u_SL101_axi_idle_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	INFRA_FMEM_MOM1_BUS_u_SL101_in_arflush_thre	
2:1	INFRA_FMEM_MOM1_BUS_u_SL101_in_awflush_thre	
0	INFRA_FMEM_MOM1_BUS_u_SL101_axi_idle_out	

1A010018 INFRA_FMEM_M2_BUS_u_Ink_INFRA_FMEM_M2_BUS_MI30_to_EMI_M2_S_DCM_PROT_ups_CTRL_0 00000000

control register 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FMEM_M2_BUS_u_Ink_INFRA_FMEM_M2_BUS_MI30_to_EMI_M2_S_DCM_PROT_ups_axi_clock_gated_en	INFRA_FMEM_M2_BUS_u_Ink_INFRA_FMEM_M2_BUS_MI30_to_EMI_M2_S_DCM_PROT_ups_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FMEM_M2_BUS_u_Ink_INFRA_FMEM_M2_BUS_MI30_to_EMI_M2_S_DCM_PROT_ups_axi_clock_gated_en	
0	INFRA_FMEM_M2_BUS_u_Ink_INFRA_FMEM_M2_BUS_MI30_to_EMI_M2_S_DCM_PROT_ups_axi_clock_gated	

1A01001C INFRA_FMEM_M2_BUS_u_Ink_INFRA_FMEM_M2_BUS_MI30_to_EMI_M2_S_DCM_PROT control
 00000000
 T_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FMEM_M2_BUS_u_Ink_INFRA_FMEM_M2_BUS_MI30_to_EMI_M2_S_DCM_PROT_axi_clock_gated_en	INFRA_FMEM_M2_BUS_u_Ink_INFRA_FMEM_M2_BUS_MI30_to_EMI_M2_S_DCM_PROT_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FMEM_M2_BUS_u_Ink_INFRA_FMEM_M2_BUS_MI30_to_EMI_M2_S_DCM_PROT_axi_clock_gated_en	
0	INFRA_FMEM_M2_BUS_u_Ink_INFRA_FMEM_M2_BUS_MI30_to_EMI_M2_S_DCM_PROT_axi_clock_gated	

1A010020 **INFRA_FMEM_M2_BUS_u_MI30 control register** 0000001C
30_CTRL_0 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											INFRA_FMEM_M2_BUS_u_MI30_cg_disable	INFRA_FMEM_M2_BUS_u_MI30_INFRA_FMEM_M2_BUS_u_MI30_mi_outstanding_extend_en	INFRA_FMEM_M2_BUS_u_MI30_INFRA_FMEM_M2_BUS_u_MI30_mi_qos_on	INFRA_FMEM_M2_BUS_u_MI30_INFRA_FMEM_M2_BUS_u_MI30_mi_ctrl_updated	INFRA_FMEM_M2_BUS_u_MI30_INFRA_FMEM_M2_BUS_u_MI30_mi_r_busy	INFRA_FMEM_M2_BUS_u_MI30_INFRA_FMEM_M2_BUS_u_MI30_mi_w_busy
Type											RW	RW	RW	RO	RO	RO
Reset											0	1	1	1	0	0

Bit(s)	Name	Description
5	INFRA_FMEM_M2_BUS_u_MI30_cg_disable	
4	INFRA_FMEM_M2_BUS_u_MI30_INFRA_FMEM_M2_BUS_u_MI30_mi_outstanding_extend_en	
3	INFRA_FMEM_M2_BUS_u_MI30_INFRA_FMEM_M2_BUS_u_MI30_mi_qos_on	
2	INFRA_FMEM_M2_BUS_u_MI30_INFRA_FMEM_M2_BUS_u_MI30_mi_ctrl_updated	INFRA_FMEM_M2_BUS_u_MI30_mi master interface control signal updated status
1	INFRA_FMEM_M2_BUS_u_MI30_INFRA_FMEM_M2_BUS_u_MI30_mi_r_busy	INFRA_FMEM_M2_BUS_u_MI30_mi master interface read busy
0	INFRA_FMEM_M2_BUS_u_MI30_INFRA_FMEM_M2_BUS_u_MI30_mi_w_busy	INFRA_FMEM_M2_BUS_u_MI30_mi master interface write busy

1A010024 INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC control register 0 000000FB

SI1_ASYNC_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC__mst_sync_sel		INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC__slv_sync_sel		INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC__in_arflush_thre		INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC__in_awflush_thre		INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC__sample_sel	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC__sync_mode	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC__axi_idle_out	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC__axi_idle_out_reg
Type					RW		RW		RW		RW		RW	RW	RO	RO
Reset					0	0	0	0	1	1	1	1	1	0	1	1

Bit(s)	Name	Description
11:10	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC__mst_sync_sel	
9:8	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC__slv_sync_sel	
7:6	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC__in_arflush_thre	
5:4	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC__in_awflush_thre	
3	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC__sample_sel	
2	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC__sync_mode	Sync mode switch for ASLICE
1	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAXI_BUS_MISI1_ASYNC__axi_idle_out	

Bit(s)	Name	Description
0	INFRA_FMEM_M4_BUS__u_lnk_INFRA_FMEM_M4_BUS_MISI8A_to_INFRA_FAX_I_BUS_MISI1_ASYNC__axi_idle_out_reg	

1A010028 INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8B_to_EMI_M4_S_DCM_PROT_ups 00000000
SI8B_to_EMI_M4_S_DCM_PR control register 0
OT_ups_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8B_to_EMI_M4_S_DCM_PROT_ups_axi_clock_gated_en	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8B_to_EMI_M4_S_DCM_PROT_ups_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8B_to_EMI_M4_S_DCM_PROT_ups_axi_clock_gated_en	
0	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8B_to_EMI_M4_S_DCM_PROT_ups_axi_clock_gated	

1A01002C INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8B_to_EMI_M4_S_DCM_PROT 00000000
SI8B to EMI_M4_S_DCM_PR control register 0
OT_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8B_to_EMI_M4_S_DCM_PROT_axi_clock_gated_en	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8B_to_EMI_M4_S_DCM_PROT_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8B_to_EMI_M4_S_DCM_PROT_axi_clock_gated_en	
0	INFRA_FMEM_M4_BUS_u_Ink_INFRA_FMEM_M4_BUS_MISI8B_to_EMI_M4_S_DCM_PROT_axi_clock_gated	

1A010030 **INFRA_FMEM_M4_BUS_u_SL18 control register** 0000001F
18_CTRL_0 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												INFRA_FMEM_M4_BUS_u_SL18_in_arflush_thre		INFRA_FMEM_M4_BUS_u_SL18_in_awflush_h_thre		INFRA_FMEM_M4_BUS_u_SL18_axi_idle_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	INFRA_FMEM_M4_BUS_u_SL18_in_arflush_thre	
2:1	INFRA_FMEM_M4_BUS_u_SL18_in_awflush_h_thre	
0	INFRA_FMEM_M4_BUS_u_SL18_axi_idle_out	

1A010034 **INFRA_FMEM_M4_BUS_u_SL44 control register** 0000001F
44_CTRL_0 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												INFRA_FMEM_M4_BUS_u_SL44_in_arflush_thre	INFRA_FMEM_M4_BUS_u_SL44_in_awflush_h_thre			INFRA_FMEM_M4_BUS_u_SL44_axi_idle_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	INFRA_FMEM_M4_BUS_u_SL44_in_arflush_thre	
2:1	INFRA_FMEM_M4_BUS_u_SL44_in_awflush_h_thre	
0	INFRA_FMEM_M4_BUS_u_SL44_axi_idle_out	

1A010038 INFRA_FMEM_M4_BUS_u_MIINFRA_FMEM_M4_BUS_u_MISI8A control
SISA_CTRL_0 register 0

0001E001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													INFRA_FMEM_M4_BUS_u_MISI8A_S_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A_S_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A_S_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A_S_u_MISI8A__INFR
Type													RW	RW	RW	RW
Reset													0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INFRA_FMEM_M4_BUS_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A__INFR	INFRA_FMEM_M4_BUS_u_MISI8A__INFR
Type	RW	RW	RW	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
19	INFRA_FMEM_M4_BUS_u_MISI8A_cg_disable	
18	INFRA_FMEM_M4_BUS_u_MISI8A__IN Bypasses idle check when updating SI setting FRA_FMEM_M4_BUS_u_MISI8A_si_ctrl_bypass	
17	INFRA_FMEM_M4_BUS_u_MISI8A__IN si_cabgen slave interface outstanding capability disable control FRA_FMEM_M4_BUS_u_MISI8A_si_outstanding_disable	
16:15	INFRA_FMEM_M4_BUS_u_MISI8A__IN INFRA_FMEM_M4_BUS_u_MISI8A_si slave interface read arbiter FRA_FMEM_M4_BUS_u_MISI8A_si_way interleaving function enable control _interleave_en	
14:13	INFRA_FMEM_M4_BUS_u_MISI8A__IN Control INFRA_FMEM_M4_BUS_u_MISI8A_si address decode output FRA_FMEM_M4_BUS_u_MISI8A_si_way path enable of each way _en	

Bit(s)	Name	Description
12	INFRA_FMEM_M4_BUS__u_MISI8A__IN FRA_FMEM_M4_BUS_u_MISI8A_si_dfsl	INFRA_FMEM_M4_BUS_u_MISI8A_si slave interface default slave write IRQ status
	v_set_wirq	
11	INFRA_FMEM_M4_BUS__u_MISI8A__IN FRA_FMEM_M4_BUS_u_MISI8A_si_dfsl	INFRA_FMEM_M4_BUS_u_MISI8A_si slave interface default slave read IRQ status
	v_set_rirq	
10:8	INFRA_FMEM_M4_BUS__u_MISI8A__IN FRA_FMEM_M4_BUS_u_MISI8A_si_b_c	INFRA_FMEM_M4_BUS_u_MISI8A_si slave interface current write response channel way selection
	hnl_sel	
7	INFRA_FMEM_M4_BUS__u_MISI8A__IN FRA_FMEM_M4_BUS_u_MISI8A_si_set_is	INFRA_FMEM_M4_BUS_u_MISI8A_si slave interface write response ID is missed status
	bid_miss	
6:4	INFRA_FMEM_M4_BUS__u_MISI8A__IN FRA_FMEM_M4_BUS_u_MISI8A_si_r_ch	INFRA_FMEM_M4_BUS_u_MISI8A_si slave interface current read channel way selection
	nl_sel	
3	INFRA_FMEM_M4_BUS__u_MISI8A__IN FRA_FMEM_M4_BUS_u_MISI8A_si_set_status	INFRA_FMEM_M4_BUS_u_MISI8A_si slave interface Read ID is missed status
	rid_miss	
2	INFRA_FMEM_M4_BUS__u_MISI8A__IN FRA_FMEM_M4_BUS_u_MISI8A_si_rd	INFRA_FMEM_M4_BUS_u_MISI8A_si slave interface Read Channel Outstanding Busy
	ot_busy	
1	INFRA_FMEM_M4_BUS__u_MISI8A__IN FRA_FMEM_M4_BUS_u_MISI8A_si_wr	INFRA_FMEM_M4_BUS_u_MISI8A_si slave interface Write Channel Outstanding Busy
	ot_busy	
0	INFRA_FMEM_M4_BUS__u_MISI8A__IN FRA_FMEM_M4_BUS_u_MISI8A_si_ctrl_updated	INFRA_FMEM_M4_BUS_u_MISI8A_si slave interface control signal updated status

1A01003C **INFRA_FMEM_M4_BUS_u_MISI8B control**
SI8B_CTRL_0 register 0

0000001C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											INFRA_FMEM_M4_BUS_u_MISI8B_S_u_MISI8B_M4_BUS_u_MISI8B_A_FME_M_M4_BUS_u_MISI8B_cg_disable	INFRA_FMEM_M4_BUS_u_MISI8B_S_u_MISI8B_M4_BUS_u_MISI8B_A_FME_M_M4_BUS_u_MISI8B_mi_outstanding_extend_en	INFRA_FMEM_M4_BUS_u_MISI8B_S_u_MISI8B_M4_BUS_u_MISI8B_A_FME_M_M4_BUS_u_MISI8B_mi_qos_on	INFRA_FMEM_M4_BUS_u_MISI8B_S_u_MISI8B_M4_BUS_u_MISI8B_A_FME_M_M4_BUS_u_MISI8B_mi_ctrl_updated	INFRA_FMEM_M4_BUS_u_MISI8B_S_u_MISI8B_M4_BUS_u_MISI8B_A_FME_M_M4_BUS_u_MISI8B_mi_r_busy	INFRA_FMEM_M4_BUS_u_MISI8B_S_u_MISI8B_M4_BUS_u_MISI8B_A_FME_M_M4_BUS_u_MISI8B_mi_w_busy
Type											RW	RW	RW	RO	RO	RO
Reset											0	1	1	1	0	0

Bit(s)	Name	Description
5	INFRA_FMEM_M4_BUS_u_MISI8B_cg_disable	
4	INFRA_FMEM_M4_BUS_u_MISI8B_IN FRA_FMEM_M4_BUS_u_MISI8B_mi_outstanding_extend_en	
3	INFRA_FMEM_M4_BUS_u_MISI8B_IN FRA_FMEM_M4_BUS_u_MISI8B_mi_qos_on	
2	INFRA_FMEM_M4_BUS_u_MISI8B_IN INFRA_FMEM_M4_BUS_u_MISI8B_mi master interface control signal updated status	
1	INFRA_FMEM_M4_BUS_u_MISI8B_IN INFRA_FMEM_M4_BUS_u_MISI8B_mi master interface read busy	
0	INFRA_FMEM_M4_BUS_u_MISI8B_IN INFRA_FMEM_M4_BUS_u_MISI8B_mi master interface write busy	

1A010040 INFRA_FMEM_M5_BUS_u_Ink_INFRA_FMEM_M5_BUS_MI60_to_EMI_M5_S_DCM_PROT_ups_CTRL_0 00000000

control register 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FMEM_M5_BUS_u_Ink_INFRA_FMEM_M5_BUS_MI60_to_EMI_M5_S_DCM_PROT_ups_axi_clock_gated_en	INFRA_FMEM_M5_BUS_u_Ink_INFRA_FMEM_M5_BUS_MI60_to_EMI_M5_S_DCM_PROT_ups_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FMEM_M5_BUS_u_Ink_INFRA_FMEM_M5_BUS_MI60_to_EMI_M5_S_DCM_PROT_ups_axi_clock_gated_en	
0	INFRA_FMEM_M5_BUS_u_Ink_INFRA_FMEM_M5_BUS_MI60_to_EMI_M5_S_DCM_PROT_ups_axi_clock_gated	

1A010044 INFRA_FMEM_M5_BUS_u_Ink_INFRA_FMEM_M5_BUS_MI60_to_EMI_M5_S_DCM_PROT control 00000000

T_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FMEM_M5_BUS_u_Ink_INFRA_FMEM_M5_BUS_MI60_to_EMI_M5_S_DCM_PROT_axi_clock_gated_en	INFRA_FMEM_M5_BUS_u_Ink_INFRA_FMEM_M5_BUS_MI60_to_EMI_M5_S_DCM_PROT_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FMEM_M5_BUS_u_Ink_INFRA_FMEM_M5_BUS_MI60_to_EMI_M5_S_DCM_PROT_axi_clock_gated_en	
0	INFRA_FMEM_M5_BUS_u_Ink_INFRA_FMEM_M5_BUS_MI60_to_EMI_M5_S_DCM_PROT_axi_clock_gated	

1A010048 **INFRA_FMEM_M5_BUS_u_MI60 control register** 0000001C
60_CTRL_0 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											INFRA_FMEM_M5_BUS_u_MI60_cg_disable	INFRA_FMEM_M5_BUS_u_MI60_INFRA_FMEM_M5_BUS_u_MI60_mi_outstanding_extend_en	INFRA_FMEM_M5_BUS_u_MI60_INFRA_FMEM_M5_BUS_u_MI60_mi_qos_on	INFRA_FMEM_M5_BUS_u_MI60_INFRA_FMEM_M5_BUS_u_MI60_mi_ctrl_updated	INFRA_FMEM_M5_BUS_u_MI60_INFRA_FMEM_M5_BUS_u_MI60_mi_r_busy	INFRA_FMEM_M5_BUS_u_MI60_INFRA_FMEM_M5_BUS_u_MI60_mi_w_busy
Type											RW	RW	RW	RO	RO	RO
Reset											0	1	1	1	0	0

Bit(s)	Name	Description
5	INFRA_FMEM_M5_BUS_u_MI60_cg_disable	
4	INFRA_FMEM_M5_BUS_u_MI60_INFRA_FMEM_M5_BUS_u_MI60_mi_outstanding_extend_en	
3	INFRA_FMEM_M5_BUS_u_MI60_INFRA_FMEM_M5_BUS_u_MI60_mi_qos_on	
2	INFRA_FMEM_M5_BUS_u_MI60_INFRA_FMEM_M5_BUS_u_MI60_mi_ctrl_updated	INFRA_FMEM_M5_BUS_u_MI60_mi master interface control signal updated status
1	INFRA_FMEM_M5_BUS_u_MI60_INFRA_FMEM_M5_BUS_u_MI60_mi_r_busy	INFRA_FMEM_M5_BUS_u_MI60_mi master interface read busy
0	INFRA_FMEM_M5_BUS_u_MI60_INFRA_FMEM_M5_BUS_u_MI60_mi_w_busy	INFRA_FMEM_M5_BUS_u_MI60_mi master interface write busy

1A01004C INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FAXI_B 000000FB
_Ink_INFRA_FAXI_BUS_AXI_UUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS
P_PERI_to_INFRA_FMEM_M6_SL07_ASYNC control register 0
M7_BUS_SL07_ASYNC_CTRL
0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FAXI_BUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS_SL07_ASYNC__mst_s ync_sel	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FAXI_BUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS_SL07_ASYNC__slv_sy nc_sel	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FAXI_BUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS_SL07_ASYNC__in_arf ush_thre	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FAXI_BUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS_SL07_ASYNC__in_aw flush_thre					INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FAXI_BUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS_SL07_ASYNC__mst_s ync_sel	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FAXI_BUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS_SL07_ASYNC__slv_sy nc_sel	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FAXI_BUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS_SL07_ASYNC__in_arf ush_thre	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FAXI_BUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS_SL07_ASYNC__in_aw flush_thre
Type					RW	RW	RW	RW					RW	RW	RO	RO
Reset					0	0	0	0	1	1	1	1	1	0	1	1

Bit(s)	Name	Description
11:10	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FAXI_BUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS_SL07_ASYNC__mst_s ync_sel	
9:8	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FAXI_BUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS_SL07_ASYNC__slv_sy nc_sel	
7:6	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FAXI_BUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS_SL07_ASYNC__in_arf ush_thre	
5:4	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FAXI_BUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS_SL07_ASYNC__in_aw flush_thre	
3	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FAXI_BUS_AXI_UP_PERI_to_INFRA_F	

Bit(s)	Name	Description
	MEM_M6M7_BUS_SL07_ASYNC__sample_sel	
2	INFRA_FMEM_M6M7_BUS__u_lnk_INFRASync mode switch for ASLICE	
	A_FAXI_BUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS_SL07_ASYNC__sync_mode	
1	INFRA_FMEM_M6M7_BUS__u_lnk_INFRASync mode switch for ASLICE	
	A_FAXI_BUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS_SL07_ASYNC__axi_idle_out	
0	INFRA_FMEM_M6M7_BUS__u_lnk_INFRASync mode switch for ASLICE	
	A_FAXI_BUS_AXI_UP_PERI_to_INFRA_FMEM_M6M7_BUS_SL07_ASYNC__axi_idle_out_reg	

1A010050 INFRA_FMEM_M6M7_BUS_u INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM
Ink_INFRA_FMEM_M6M7_B_M6M7_BUS_SL07_to_EMI_M7_S_DCM_PROT_
US_SL07_to_EMI_M7_S_DCMups control register 0
PROT_ups_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL07_to_EMI_M7_S_DCM_PROT_ups_axi_clock_gated_en	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL07_to_EMI_M7_S_DCM_PROT_ups_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL07_to_EMI_M7_S_DCM_PROT_ups_axi_clock_gated_en	
0	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL07_to_EMI_M7_S_DCM_PROT_ups_axi_clock_gated	

1A010054 INFRA_FMEM_M6M7_BUS_u INFRA_FMEM_M6M7_BUS_u_Ink INFRA_FMEM
Ink INFRA_FMEM_M6M7_B_M6M7_BUS_SL07_to_EMI_M7_S_DCM_PROT
US_SL07_to_EMI_M7_S_DCM control register 0
PROT_CTRL_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_A_FMEM_M6M7_BUS_SL07_to_EMI_M7_S_DCM_PROT_axi_clock_gated_en	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_A_FMEM_M6M7_BUS_SL07_to_EMI_M7_S_DCM_PROT_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL07_to_EMI_M7_S_DCM_PROT_axi_clock_gated_en	
0	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL07_to_EMI_M7_S_DCM_PROT_axi_clock_gated	

1A010058 INFRA_FMEM_M6M7_BUS_u INFRA_FMEM_M6M7_BUS_u_Ink INFRA_FMEM
Ink INFRA_FMEM_M6M7_B_M6M7_BUS_SL30_to_EMI_M6_S_DCM_PROT_
US_SL30_to_EMI_M6_S_DCM ups control register 0
PROT_ups_CTRL_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL30_to_EMI_M6_S_DCM_PROT_ups_axi_clock_gated_en	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL30_to_EMI_M6_S_DCM_PROT_ups_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL30_to_EMI_M6_S_DCM_PROT_ups_axi_clock_gated_en	
0	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL30_to_EMI_M6_S_DCM_PROT_ups_axi_clock_gated	

1A01005C INFRA_FMEM_M6M7_BUS_u INFRA_FMEM_M6M7_BUS_u_Ink INFRA_FMEM
Ink INFRA_FMEM_M6M7_B_M6M7_BUS_SL30_to_EMI_M6_S_DCM_PROT
US_SL30_to_EMI_M6_S_DCM control register 0
PROT_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL30_to_EMI_M6_S_DCM_PROT_axi_clock_gated_en	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL30_to_EMI_M6_S_DCM_PROT_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL30_to_EMI_M6_S_DCM_PROT_axi_clock_gated_en	
0	INFRA_FMEM_M6M7_BUS_u_Ink_INFRA_FMEM_M6M7_BUS_SL30_to_EMI_M6_S_DCM_PROT_axi_clock_gated	

1A010060 **INFRA_FMEM_M6M7_BUS_u** INFRA_FMEM_M6M7_BUS_u_SL30 control
SL30_CTRL_0 **register 0**

0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												INFRA_FMEM_M6M7_BUS_u_SL30_in_arflush_thre	INFRA_FMEM_M6M7_BUS_u_SL30_in_awflush_thre			INFRA_FMEM_M6M7_BUS_u_SL30_axi_idle_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	INFRA_FMEM_M6M7_BUS_u_SL30_in_arflush_thre	
2:1	INFRA_FMEM_M6M7_BUS_u_SL30_in_awflush_thre	
0	INFRA_FMEM_M6M7_BUS_u_SL30_axi_idle_out	

1A010064

INFRA_FMEM_M6M7_BUS_u INFRA_FMEM_M6M7_BUS_u_SL07 control
SL07_CTRL_0 register 0

0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												INFRA_FMEM_M6M7_BUS_u_SL07_in_arflush_thre	INFRA_FMEM_M6M7_BUS_u_SL07_in_awflush_thre			INFRA_FMEM_M6M7_BUS_u_SL07_axi_idle_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	INFRA_FMEM_M6M7_BUS_u_SL07_in_arflush_thre	
2:1	INFRA_FMEM_M6M7_BUS_u_SL07_in_awflush_thre	
0	INFRA_FMEM_M6M7_BUS_u_SL07_axi_idle_out	

Module name: bcrm_INFRA_AO_wrapper_u_bcrm_INFRA_AO_bcrm Base address: (+0x1A02_0000)

Address	Name	Width	Register Function
1A020000	<u>bcrm INFRA AO wrapper u</u> <u>bcrm INFRA AO bcrm exte</u> <u>nded bus protect set CTRL</u> <u>0</u>	32	bcrm_INFRA_AO_wrapper_u_bcrm_INFRA_AO__bcrm _extended_bus_protect_set control register 0
1A020004	<u>bcrm INFRA AO wrapper u</u> <u>bcrm INFRA AO bcrm exte</u> <u>nded bus protect clr CTRL 0</u>	32	bcrm_INFRA_AO_wrapper_u_bcrm_INFRA_AO__bcrm _extended_bus_protect_clr control register 0
1A020008	<u>bcrm INFRA AO wrapper u</u> <u>bcrm INFRA AO bcrm exte</u> <u>nded bus protect rw CTRL</u> <u>0</u>	32	bcrm_INFRA_AO_wrapper_u_bcrm_INFRA_AO__bcrm _extended_bus_protect_rw control register 0
1A02000C	<u>bcrm INFRA AO wrapper u</u> <u>bcrm INFRA AO bcrm exte</u> <u>nded bus protect ro CTRL 0</u>	32	bcrm_INFRA_AO_wrapper_u_bcrm_INFRA_AO__bcrm _extended_bus_protect_ro control register 0
1A020014	<u>VDNR PWR PROT INFRA PA</u> <u>R BUS u spm CTRL 0</u>	32	VDNR_PWR_PROT_INFRA_PAR_BUS_u_spm control register 0
1A020018	<u>VDNR DCM TOP INFRA PAR</u> <u>BUS u INFRA PAR BUS CT</u> <u>RL 0</u>	32	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS control register 0
1A02001C	<u>VDNR DCM TOP INFRA PAR</u> <u>BUS u INFRA PAR BUS CT</u> <u>RL 1</u>	32	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS control register 1
1A020020	<u>VDNR DCM TOP INFRA PAR</u> <u>BUS u INFRA PAR BUS CT</u> <u>RL 2</u>	32	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS control register 2
1A020024	<u>VDNR DCM TOP INFRA PAR</u> <u>BUS u INFRA PAR BUS CT</u> <u>RL 3</u>	32	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS control register 3
1A020028	<u>VDNR DCM TOP INFRA PAR</u> <u>BUS u INFRA PAR BUS CT</u> <u>RL 4</u>	32	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS control register 4
1A02002C	<u>VDNR DCM TOP INFRA PAR</u> <u>BUS u INFRA PAR BUS CT</u> <u>RL 5</u>	32	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS control register 5
1A020030	<u>VDNR DCM TOP INFRA PAR</u> <u>BUS u INFRA PAR BUS CT</u> <u>RL 6</u>	32	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS control register 6
1A020034	<u>VDNR DCM TOP INFRA PAR</u> <u>BUS u INFRA PAR BUS CT</u> <u>RL 7</u>	32	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS control register 7
1A020038	<u>VDNR DCM TOP INFRA PAR</u> <u>BUS u INFRA PAR BUS CT</u> <u>RL 8</u>	32	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS control register 8
1A02003C	<u>VDNR DCM TOP INFRA PAR</u> <u>BUS u INFRA PAR BUS CT</u> <u>RL 9</u>	32	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS control register 9
1A020040	<u>VDNR DCM TOP INFRA PAR</u> <u>BUS u INFRA PAR BUS CT</u> <u>RL 10</u>	32	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS control register 10
1A020044	<u>VDNR DCM TOP INFRA PAR</u> <u>BUS u INFRA PAR BUS CT</u> <u>RL 11</u>	32	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS control register 11

Address	Name	Width	Register Function
1A020048	<u>VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_CTL_12</u>	32	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS control register 12
1A02004C	<u>VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_CTL_13</u>	32	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS control register 13
1A020050	<u>VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_CTL_14</u>	32	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS control register 14

1A020000 bcrn_INFRA_AO_wrapper_u_bcrn_INFRA_AO_wrapper_u_bcrn_INFRA_AO__ 00000000
bcrn_INFRA_AO_bcrn_extbcrn_extended_bus_protect_set control register
ended_bus_protect_set_CTRL0
0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PERI_PAR_FAXI_BUS__u_MI11__prot_en					PERI_P AR_FA XI_BUS __u_In k_PERI _PAR_F AXI_BU S_MI11 _to_PE RI_PAR _FAXI_ BUS_M I14_DC M_PRO T__pro tect_en	PERI_QAXI_AHB BUS__u_MI18__prot_en		PERI_Q AXI_BU S__u_I nk_PER I_QAXI _AHB_ BUS_M I18_to _PERI_ QAXI_ BUS_M ISI3A_ DCM_P ROT__ protect _en
Type								WO					WO	WO		WO
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:4	PERI_PAR_FAXI_BUS__u_MI11__prot_en	
3	PERI_PAR_FAXI_BUS__u_Ink_PERI_PAR_FAXI_BUS_MI11_to_PERI_PAR_FAXI_BUS_MI14_DCM_PROT__protect_en	
2:1	PERI_QAXI_AHB_BUS__u_MI18__prot_en	
0	PERI_QAXI_BUS__u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_DCM_PROT__protect_en	

1A020004 bcrn_INFRA_AO_wrapper_u_bcrn_INFRA_AO_wrapper_u_bcrn_INFRA_AO_ 00000000
bcrn_INFRA_AO_bcrn_extbcrn_extended_bus_protect_clr control register
ended_bus_protect_clr_CTRL 0
0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PERI_PAR_FAXI_BUS__u_MI11__prot_en					PERI_P AR_FA XI_BUS __u_In k_PERI _PAR_F AXI_BU S_MI11 _to_PE RI_PAR _FAXI_ BUS_M I14_DC M_PRO T__pro tect_en	PERI_QAXI_AHB BUS__u_MI18__prot_en		PERI_Q AXI_BU S__u_I nk_PER I_QAXI _AHB_ BUS_M I18_to _PERI_ QAXI_ BUS_M ISI3A_ DCM_P ROT__ protect _en
Type								WO					WO	WO		WO
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:4	PERI_PAR_FAXI_BUS__u_MI11__prot_en	
3	PERI_PAR_FAXI_BUS__u_Ink_PERI_PAR_FAXI_BUS_MI11_to_PERI_PAR_FAXI_BUS_MI14_DCM_PROT__protect_en	
2:1	PERI_QAXI_AHB_BUS__u_MI18__prot_en	
0	PERI_QAXI_BUS__u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_DCM_PROT__protect_en	

1A020008 bcrn_INFRA_AO_wrapper_u_bcrn_INFRA_AO_wrapper_u_bcrn_INFRA_AO__ 00000000
bcrn_INFRA_AO_bcrn_extbcrn_extended_bus_protect_rw control register
ended_bus_protect_rw_CTRL_0
_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PERI_PAR_FAXI_BUS__u_MI11__prot_en					PERI_P AR_FA XI_BUS __u_In k_PERI _PAR_F AXI_BU S_MI11 _to_PE RI_PAR _FAXI_ BUS_M I14_DC M_PRO T__pro tect_en	PERI_QAXI_AHB_BUS__u_MI18__prot_en		PERI_Q AXI_BU S__u_I nk_PER I_QAXI _AHB_ BUS_M I18_to _PERI _QAXI_ BUS_M ISI3A_ DCM_P ROT__ protect _en
Type								RW					RW	RW		RW
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:4	PERI_PAR_FAXI_BUS__u_MI11__prot_en	
3	PERI_PAR_FAXI_BUS__u_Ink_PERI_PAR_FAXI_BUS_MI11_to_PERI_PAR_FAXI_BUS_MI14_DCM_PROT__protect_en	
2:1	PERI_QAXI_AHB_BUS__u_MI18__prot_en	
0	PERI_QAXI_BUS__u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_DCM_PROT__protect_en	

1A02000C bcrn_INFRA_AO_wrapper_u_bcrn_INFRA_AO_wrapper_u_bcrn_INFRA_AO__ 00000000
bcrn_INFRA_AO_bcrn_ext_bcrn_extended_bus_protect_ro control register
ended_bus_protect_ro_CTRL_0
0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PERI_PAR_FAXI_BUS__u_MI11__prot_r eady					PERI_P AR_FA XI_BUS __u_In k_PERI _PAR_F AXI_BU S_MI11 _to_PE RI_PAR _FAXI_ BUS_M I14_DC M_PRO T__pro tect_re ady	PERI_QAXI_AH B_BUS__u_MI1 8__prot_ready		PERI_Q AXI_BU S__u_I nk_PER I_QAXI _AHB_ BUS_M I18_to _PERI_ QAXI_ BUS_M ISI3A_ DCM_P ROT__ protect _ready
Type								RO					RO	RO		RO
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:4	PERI_PAR_FAXI_BUS__u_MI11__prot_r ady	
3	PERI_PAR_FAXI_BUS__u_Ink_PERI_PAR_ FAXI_BUS_MI11_to_PERI_PAR_FAXI_BU S_MI14_DCM_PROT__protect_ready	
2:1	PERI_QAXI_AHB_BUS__u_MI18__prot_r eady	
0	PERI_QAXI_BUS__u_Ink_PERI_QAXI_AH B_BUS_MI18_to_PERI_QAXI_BUS_MISI3 A_DCM_PROT__protect_ready	

1A020014 VDNR_PWR_PROT_INFRA_PAR_BUS_u_spm 00000000
R_BUS_u_spm_CTRL_0 control register 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							VDNR_PWR_P ROT_INFRA_PA R_BUS_u_sp m_rg_pwr_pr ot_en_i	VDNR_PWR_P ROT_INFRA_PA R_BUS_u_sp m_rg_pwr_pr ot_sw_i	VDNR_PWR_P ROT_INFRA_P FRA_P AR_BU S_u_s pm_rg _pwr_p rot_req _ext_o	VDNR_PWR_P ROT_INFRA_PA R_BUS_u_sp m_rg_pwr_pr ot_rdy_o	VDNR_PWR_P ROT_INFRA_PA R_BUS_u_sp m_pwr_prot _en_o	VDNR_PWR_P ROT_INFRA_P FRA_P AR_BU S_u_s pm_rg _pwr_p rot_req _ext_o	VDNR_PWR_P ROT_INFRA_PA R_BUS_u_sp m_pwr_prot _en_o	VDNR_PWR_P ROT_INFRA_PA R_BUS_u_sp m_pwr_prot _en_o	VDNR_PWR_P ROT_INFRA_PA R_BUS_u_sp m_pwr_prot _en_o	VDNR_PWR_P ROT_INFRA_P FRA_P AR_BU S_u_s pm_rg _pwr_p rot_req _ext_o
Type							RW	RW	RW	RW	RO	RO	RO	RO	RO	RO
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:8	VDNR_PWR_PROT_INFRA_PAR_BUS_u _spm_rg_pwr_prot_en_i	
7:6	VDNR_PWR_PROT_INFRA_PAR_BUS_u _spm_rg_pwr_prot_sw_i	
5	VDNR_PWR_PROT_INFRA_PAR_BUS_u _spm_rg_pwr_prot_req_ext_o	
4:3	VDNR_PWR_PROT_INFRA_PAR_BUS_u _spm_rg_pwr_prot_rdy_o	
2:1	VDNR_PWR_PROT_INFRA_PAR_BUS_u _spm_pwr_prot_en_o	
0	VDNR_PWR_PROT_INFRA_PAR_BUS_u _spm_pwr_prot_ack_o	

1A020018 VDNR_DCM_TOP_INFRA_PARVDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PA 00000000
 BUS_u_INFRA_PAR_BUS_CTL_R_BUS control register 0
 RL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg8_cl ock_gr oup_ct rl_pllck _sel_n o_spm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg8_cl ock_gr oup_ct rl_pllck _sel_n o_spm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg7_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg7_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg7_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg6_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg6_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg5_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg5_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg5_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg4_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg4_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg4_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg3_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg3_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg3_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg3_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg2_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg2_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg1_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg1_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg1_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg1_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg1_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg1_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg1_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg1_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg1_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg1_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg1_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg1_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S_rg ckg1_cl ock_gr oup_ct rl_pllck _sel_2 clk_rdy _on_dcm
Type	RW	RW	RW	RW	RW	RW	RW	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	VDNR_DCM_TOP_INFRA_PAR_BUS_u_I NFRA_PAR_BUS_rg_ckg8_clock_group_ ctrl_pllck_sel_no_spm	
30	VDNR_DCM_TOP_INFRA_PAR_BUS_u_I NFRA_PAR_BUS_rg_ckg8_clock_group_ ctrl_sc_axi_dcm_dis_en	
29	VDNR_DCM_TOP_INFRA_PAR_BUS_u_I NFRA_PAR_BUS_rg_ckg7_clock_group_ ctrl_pllck_sel_2_clk_rdy_on_dcm	

Bit(s)	Name	Description
28	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg7_clock_group_ ctrl_pllck_sel_no_spm	
27	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg7_clock_group_ ctrl_sc_axi_dcm_dis_en	
26	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg6_clock_group_ ctrl_pllck_sel_2_clk_rdy_on_dcm	
25	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg6_clock_group_ ctrl_pllck_sel_no_spm	
24	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg6_clock_group_ ctrl_sc_axi_dcm_dis_en	
23	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg5_clock_group_ ctrl_pllck_sel_2_clk_rdy_on_dcm	
22	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg5_clock_group_ ctrl_pllck_sel_no_spm	
21	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg5_clock_group_ ctrl_sc_axi_dcm_dis_en	
20	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg4_clock_group_ ctrl_pllck_sel_2_clk_rdy_on_dcm	
19	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg4_clock_group_ ctrl_pllck_sel_no_spm	
18	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg4_clock_group_ ctrl_sc_axi_dcm_dis_en	
17	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg3_clock_group_ ctrl_pllck_sel_2_clk_rdy_on_dcm	
16	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg3_clock_group_ ctrl_pllck_sel_no_spm	
15	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg3_clock_group_ ctrl_sc_axi_dcm_dis_en	
14	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg2_clock_group_ ctrl_pllck_sel_2_clk_rdy_on_dcm	

Bit(s)	Name	Description
13	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg2_clock_group_ ctrl_pllck_sel_no_spm	
12	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg2_clock_group_ ctrl_sc_axi_dcm_dis_en	
11	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg1_clock_group_ ctrl_pllck_sel_2_clk_rdy_on_dcm	
10	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg1_clock_group_ ctrl_pllck_sel_no_spm	
9	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg1_clock_group_ ctrl_sc_axi_dcm_dis_en	
8	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__clk_rdy_on_dcm_ck10	
7	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__clk_rdy_on_dcm_ck9	
6	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__clk_rdy_on_dcm_ck8	
5	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__clk_rdy_on_dcm_ck7	
4	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__clk_rdy_on_dcm_ck6	
3	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__clk_rdy_on_dcm_ck5	
2	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__clk_rdy_on_dcm_ck4	
1	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__clk_rdy_on_dcm_ck3	
0	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__clk_rdy_on_dcm_ck1	

1A02001C VDNR_DCM_TOP_INFRA_PAR_VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PA 10104404
 BUS_u_INFRA_PAR_BUS_CT R_BUS control register 1
 RL 1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VDNR_DCM_T OP_INF RA_PA R_BUS __u_IN FRA_P AR_BU S_rg_ ck1_db c_ctrl_ dbc_en	VDNR_DCM_TOP_INFRA_PAR_BUS__u_INFRA_PAR_BUS__rg_ck1_dbc_ctrl_dbc_num											
Type				RW	RW											
Reset				1	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDNR_DCM_TOP_INFRA_PAR_BUS__u_INFRA_PAR_BUS__rg_ck1_ctrl_sfsel					VDNR_DCM_TOP_INFRA_PAR_BUS__u_INFRA_PAR_BUS__rg_ck1_ctrl_fselsel					VDNR_DCM_T OP_INF RA_PA R_BUS __u_IN FRA_P AR_BU S_rg_ ck1_ctr l_force _on	VDNR_DCM_T OP_INF RA_PA R_BUS __u_IN FRA_P AR_BU S_rg_ ck1_ctr l_force _clksw	VDNR_DCM_T OP_INF RA_PA R_BUS __u_IN FRA_P AR_BU S_rg_ ck1_ctr l_force _clkloff	VDNR_DCM_T OP_INF RA_PA R_BUS __u_IN FRA_P AR_BU S_rg_ ck1_ctr l_force _clkloff	VDNR_DCM_T OP_INF RA_PA R_BUS __u_IN FRA_P AR_BU S_rg_ ck1_ctr l_force _clkloff	VDNR_DCM_T OP_INF RA_PA R_BUS __u_IN FRA_P AR_BU S_rg_ ck1_ctr l_force _clkloff
Type	RW					RW					RW	RW	RW	RW	RW	RW
Reset	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
28	VDNR_DCM_TOP_INFRA_PAR_BUS__u_INFRA_PAR_BUS__rg_ck1_dbc_ctrl_dbc_en	
27:16	VDNR_DCM_TOP_INFRA_PAR_BUS__u_INFRA_PAR_BUS__rg_ck1_dbc_ctrl_dbc_num	
15:11	VDNR_DCM_TOP_INFRA_PAR_BUS__u_INFRA_PAR_BUS__rg_ck1_ctrl_sfsel	
10:6	VDNR_DCM_TOP_INFRA_PAR_BUS__u_INFRA_PAR_BUS__rg_ck1_ctrl_fselsel	
5	VDNR_DCM_TOP_INFRA_PAR_BUS__u_INFRA_PAR_BUS__rg_ck1_ctrl_force_on	

Bit(s)	Name	Description
4	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck1_ctrl_force_clks low	
3	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck1_ctrl_force_clk off	
2	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck1_ctrl_clkslow_e n	
1	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck1_ctrl_clkoff_en	
0	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ckg8_clock_group_ ctrl_pllck_sel_2_clk_rdy_on_dcm	

1A020020 VDNR_DCM_TOP_INFRA_PAR_VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PA 1012200F
 BUS_u_INFRA_PAR_BUS_CT R_BUS control register 2
 RL 2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck3_ctrl_fsm					VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck3_ctrl_force_on	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck3_ctrl_force_clkslow	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck3_ctrl_force_clkoff	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck3_ctrl_force_clkoff_w_en	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck3_ctrl_force_clkoff_en	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck2_ctrl_fsm		
Type				RW					RW	RW	RW	RW	RW	RW		
Reset				1	0	0	0	0	0	0	0	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck2_ctrl_fsm		VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck2_ctrl_fsm					VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck2_ctrl_force_on	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck2_ctrl_force_clkslow	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck2_ctrl_force_clkoff	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck2_ctrl_force_clkoff_w_en	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck2_ctrl_force_clkoff_en	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck1_early_ctrl			
Type	RW		RW					RW	RW	RW	RW	RW	RW			
Reset	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Name	Description
28:24	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck3_ctrl_fsm	
23	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck3_ctrl_force_on	
22	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck3_ctrl_force_clkslow	
21	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck3_ctrl_force_clkoff	
20	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck3_ctrl_force_clkoff	
19	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck3_ctrl_force_clkoff	

Bit(s)	Name	Description
18:14	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck2_ctrl_sfsel	
13:9	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck2_ctrl_fsel	
8	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck2_ctrl_force_on	
7	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck2_ctrl_force_clks low	
6	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck2_ctrl_force_clk off	
5	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck2_ctrl_clkslow_e n	
4	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck2_ctrl_clkoff_en	
3:0	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck1_early_ctrl	

1A020024

VDNR_DCM_TOP_INFRA_PARVDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PA
 BUS u_INFRA_PAR_BUS_CT R_BUS control register 3
 RL 3

00020208

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck3_dbc_ctrl_dbc_en	VDNR_DCM_TOP_INFRA_PAR_BUS__rg_ck3_dbc_ctrl_dbc_num
Type															RW	RW
Reset															1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDNR_DCM_TOP_INFRA_PAR_BUS__rg_ck3_dbc_ctrl_dbc_num											VDNR_DCM_TOP_INFRA_PAR_BUS__rg_ck3_ctrl_sf sel				
Type	RW											RW				
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
17	VDNR_DCM_TOP_INFRA_PAR_BUS__u_I NFRA_PAR_BUS__rg_ck3_dbc_ctrl_dbc_en	
16:5	VDNR_DCM_TOP_INFRA_PAR_BUS__u_I NFRA_PAR_BUS__rg_ck3_dbc_ctrl_dbc_num	
4:0	VDNR_DCM_TOP_INFRA_PAR_BUS__u_I NFRA_PAR_BUS__rg_ck3_ctrl_sf sel	

1A020028 VDNR_DCM_TOP_INFRA_PAR_VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PA 080BFFFF
 BUS_u_INFRA_PAR_BUS_CTL_R_BUS control register 4
 RL 4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_ctrl_fsm					VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_ctrl_force_on	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_ctrl_force_low	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_ctrl_force_clkoff	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_ctrl_clkslow_en	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_ctrl_clkoff_en	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck3_early_ctrl	
Type					RW					RW	RW	RW	RW	RW	RW	
Reset					1	0	0	0	0	0	0	0	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck3_early_ctrl															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27:23	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_ctrl_fsm	
22	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_ctrl_force_on	
21	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_ctrl_force_clkslow	
20	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_ctrl_force_clkoff	
19	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_ctrl_clkslow_en	
18	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_ctrl_clkoff_en	
17:0	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck3_early_ctrl	

1A02002C

VDNR_DCM_TOP_INFRA_PAR_VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PA
 BUS_u_INFRA_PAR_BUS_CT_R_BUS control register 5
 RL 5

080A0208

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_ctrl_fsm					VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_ctrl_fsm
Type					RW					RW	RW	RW	RW	RW	RW	RW
Reset					1	0	0	0	0	0	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_dbc_ctrl_dbc_num											VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_ctrl_fsm				
Type	RW											RW				
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
27:23	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_ctrl_fsm	
22	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_ctrl_force_on	
21	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_ctrl_force_clkslow	
20	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_ctrl_force_clkoff	
19	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_ctrl_clkslow_en	
18	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_ctrl_clkoff_en	
17	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_dbc_ctrl_dbc_en	
16:5	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_dbc_ctrl_dbc_num	
4:0	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck4_ctrl_fsm	

Bit(s)	Name	Description

1A020030

VDNR_DCM_TOP_INFRA_PAR_VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PA
 BUS_u_INFRA_PAR_BUS_CT_R_BUS control register 6
 RL 6

080A0208

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_fsm					VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_fsm
Type					RW					RW	RW	RW	RW	RW	RW	RW
Reset					1	0	0	0	0	0	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_dbc_ctrl_dbc_num											VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_ctrl_fsm				
Type	RW											RW				
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
27:23	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_fsm	
22	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_force_on	
21	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_force_clkslow	
20	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_force_clkoff	
19	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_clkslow_en	
18	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_clkoff_en	
17	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_dbc_ctrl_dbc_en	
16:5	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_dbc_ctrl_dbc_num	
4:0	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck5_ctrl_fsm	

Bit(s)	Name	Description

1A020034 VDNR_DCM_TOP_INFRA_PAR_VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PA
BUS_u_INFRA_PAR_BUS_CT_R_BUS control register 7

080A0208

RL 7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_fsm					VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_fsm
Type					RW					RW	RW	RW	RW	RW	RW	RW
Reset					1	0	0	0	0	0	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_fsm											VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_fsm				
Type	RW											RW				
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
27:23	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_fsm	
22	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_force_on	
21	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_force_clkslow	
20	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_force_clkoff	
19	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_clkslow_en	
18	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_clkoff_en	
17	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_fsm	
16:5	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_fsm	
4:0	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck6_ctrl_fsm	

Bit(s)	Name	Description

1A020038

VDNR_DCM_TOP_INFRA_PARVDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PA
 BUS_u_INFRA_PAR_BUS_CT R_BUS control register 8
 RL 8

080A0208

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_fsm					VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_fsm
Type					RW					RW	RW	RW	RW	RW	RW	RW
Reset					1	0	0	0	0	0	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_fsm											VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_fsm				
Type	RW											RW				
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
27:23	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_fsm	
22	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_force_on	
21	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_force_clkslow	
20	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_force_clkoff	
19	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_clkslow_en	
18	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_clkoff_en	
17	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_dbc_en	
16:5	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_dbc_num	
4:0	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck7_ctrl_fsm	

Bit(s)	Name	Description

1A02003C

VDNR_DCM_TOP_INFRA_PARVDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PA
BUS_u_INFRA_PAR_BUS_CT R_BUS control register 9

080A0208

RL 9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck9_ctrl_fsm					VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck9_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck9_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck9_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck9_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck9_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck9_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck9_ctrl_fsm
Type					RW					RW	RW	RW	RW	RW	RW	RW
Reset					1	0	0	0	0	0	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_dbc_num											VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_fsm				
Type	RW											RW				
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
27:23	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck9_ctrl_fsm	
22	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck9_ctrl_force_on	
21	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck9_ctrl_force_clkslow	
20	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck9_ctrl_force_clkoff	
19	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck9_ctrl_clkslow_en	
18	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck9_ctrl_clkoff_en	
17	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_dbc_en	
16:5	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_dbc_num	
4:0	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck8_ctrl_fsm	

Bit(s)	Name	Description

1A020040

VDNR_DCM_TOP_INFRA_PARVDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PA
BUS_u_INFRA_PAR_BUS_CT R_BUS control register 10

202E0208

RL 10

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck10_ctrl_fsm					VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck10_ct rl_forc e_clk slow	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck10_ct rl_forc e_clk slow	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck10_ct rl_forc e_clk slow	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck10_ct rl_forc e_clk slow	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck10_ct rl_forc e_clk slow	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck10_ct rl_forc e_clk slow		VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck10_ct rl_forc e_clk slow	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck10_ct rl_forc e_clk slow
Type			RW					RW	RW	RW	RW	RW	RW		RW	RW
Reset			1	0	0	0	0	0	0	0	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck9_dbc_ctrl_dbc_num											VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck9_ctrl_fsm				
Type	RW											RW				
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
29:25	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck10_ctrl_fsm	
24	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck10_ctrl_force_on	
23	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck10_ctrl_force_clkslow	
22	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck10_ctrl_force_clkoff	
21	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck10_ctrl_clkslow_en	
20	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck10_ctrl_clkoff_en	
19:18	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck9_early_ctrl	
17	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck9_dbc_ctrl_dbc_en	
16:5	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck9_dbc_ctrl_dbc_num	

Bit(s)	Name	Description
4:0	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck9_ctrl_sfsel	

1A020044 VDNR_DCM_TOP_INFRA_PAR_VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PA
BUS_u_INFRA_PAR_BUS_CT R_BUS control register 11

08020208

RL 11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck11_ctrl_fsm					VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck11_ct rl_forc e_on	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck11_ct rl_forc e_ksl ow	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck11_ct rl_forc e_ksl off	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck11_ct rl_forc e_ksl off	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck11_ct rl_forc e_ksl off	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck10_d bc_ctrl _dbc_e n	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck10_d bc_ctrl _dbc_n um
Type					RW					RW	RW	RW	RW	RW	RW	RW
Reset					1	0	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck10_dbc_ctrl_dbc_num											VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck10_ctrl_fsm				
Type	RW											RW				
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
27:23	VDNR_DCM_TOP_INFRA_PAR_BUS_u_I NFRA_PAR_BUS__rg_ck11_ctrl_fsm	
22	VDNR_DCM_TOP_INFRA_PAR_BUS_u_I NFRA_PAR_BUS__rg_ck11_ctrl_force_o n	
21	VDNR_DCM_TOP_INFRA_PAR_BUS_u_I NFRA_PAR_BUS__rg_ck11_ctrl_force_cl kslow	
20	VDNR_DCM_TOP_INFRA_PAR_BUS_u_I NFRA_PAR_BUS__rg_ck11_ctrl_force_cl koff	
19	VDNR_DCM_TOP_INFRA_PAR_BUS_u_I NFRA_PAR_BUS__rg_ck11_ctrl_kslow_ en	
18	VDNR_DCM_TOP_INFRA_PAR_BUS_u_I NFRA_PAR_BUS__rg_ck11_ctrl_kloff_e n	
17	VDNR_DCM_TOP_INFRA_PAR_BUS_u_I NFRA_PAR_BUS__rg_ck10_dbc_ctrl_dbc _en	
16:5	VDNR_DCM_TOP_INFRA_PAR_BUS_u_I NFRA_PAR_BUS__rg_ck10_dbc_ctrl_dbc _num	
4:0	VDNR_DCM_TOP_INFRA_PAR_BUS_u_I NFRA_PAR_BUS__rg_ck10_ctrl_fsm	

Bit(s)	Name	Description

1A020048

VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PA
BUS_u_INFRA_PAR_BUS_CT R_BUS control register 12

20044008

RL 12

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VDNR_DCM_TOP_INFRA_PAR_BUS__u_INFRA_PAR_BUS__rg_ck13_ctrl_fsm					VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck13_ct rl_forc e_clk ow	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck13_ct rl_forc e_clk ow	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck13_ct rl_forc e_clk ow	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck13_ct rl_forc e_clk ow	VDNR_DCM_TOP_INFRA_PAR_BUS__u_INFRA_PAR_BUS__rg_ck12_ctrl_fsm				
Type			RW					RW	RW	RW	RW	RW	RW			
Reset			1	0	0	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck12_ctrl_fsm	VDNR_DCM_TOP_INFRA_PAR_BUS__u_INFRA_PAR_BUS__rg_ck12_ctrl_fsm					VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck12_ct rl_forc e_clk ow	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck12_ct rl_forc e_clk ow	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck12_ct rl_forc e_clk ow	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck12_ct rl_forc e_clk ow	VDNR_DCM_TOP_INFRA_PAR_BUS__u_INFRA_PAR_BUS__rg_ck11_ctrl_fsm					
Type	RW	RW					RW	RW	RW	RW	RW	RW				
Reset	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
29:25	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck13_ctrl_fsm	
24	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck13_ctrl_force_on	
23	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck13_ctrl_force_clkslow	
22	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck13_ctrl_force_clkoff	
21	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck13_ctrl_clkslow_en	

Bit(s)	Name	Description
20	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck13_ctrl_clkoff_e n	
19:15	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck12_ctrl_sfsel	
14:10	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck12_ctrl_fsel	
9	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck12_ctrl_force_o n	
8	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck12_ctrl_force_cl kslow	
7	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck12_ctrl_force_cl koff	
6	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck12_ctrl_clkslow_ en	
5	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck12_ctrl_clkoff_e n	
4:0	VDNR_DCM_TOP_INFRA_PAR_BUS__u_l NFRA_PAR_BUS__rg_ck11_ctrl_sfsel	

1A02004C

VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PA
BUS_u_INFRA_PAR_BUS_CT R_BUS control register 13

20044008

RL 13

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VDNR_DCM_TOP_INFRA_PAR_BUS__u__INFRA_PAR_BUS__rg_ck15_ctrl_fsm					VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck15_ct rl_forc e_on	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck15_ct rl_forc e_clksl ow	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck15_ct rl_forc e_clkof f	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck15_ct rl_clkof ow_en	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck15_ct rl_clkof f_en	VDNR_DCM_TOP_INFRA_PAR_BUS__u__INFRA_PAR_BUS__rg_ck14_ctrl_fsm			
Type			RW					RW	RW	RW	RW	RW	RW			
Reset			1	0	0	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck14_c trl_fsm l	VDNR_DCM_TOP_INFRA_PAR_BUS__u__INFRA_PAR_BUS__rg_ck14_ctrl_fsm					VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck14_ct rl_forc e_on	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck14_ct rl_forc e_clksl ow	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck14_ct rl_forc e_clkof f	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck14_ct rl_clkof ow_en	VDNR_DCM_T OP_INF RA_PA R_BUS _u_IN FRA_P AR_BU S__rg_ ck14_ct rl_clkof f_en	VDNR_DCM_TOP_INFRA_PAR_BUS__u__INFRA_PAR_BUS__rg_ck13_ctrl_fsm				
Type	RW	RW					RW	RW	RW	RW	RW	RW				
Reset	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
29:25	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck15_ctrl_fsm	
24	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck15_ctrl_force_on	
23	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck15_ctrl_force_clkslow	
22	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck15_ctrl_force_clkoff	
21	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS__rg_ck15_ctrl_clkslow_en	

Bit(s)	Name	Description
20	VDNR_DCM_TOP_INFRA_PAR_BUS__u_I NFRA_PAR_BUS__rg_ck15_ctrl_clkoff_e n	
19:15	VDNR_DCM_TOP_INFRA_PAR_BUS__u_I NFRA_PAR_BUS__rg_ck14_ctrl_sfsel	
14:10	VDNR_DCM_TOP_INFRA_PAR_BUS__u_I NFRA_PAR_BUS__rg_ck14_ctrl_fselsel	
9	VDNR_DCM_TOP_INFRA_PAR_BUS__u_I NFRA_PAR_BUS__rg_ck14_ctrl_force_o n	
8	VDNR_DCM_TOP_INFRA_PAR_BUS__u_I NFRA_PAR_BUS__rg_ck14_ctrl_force_cl kslow	
7	VDNR_DCM_TOP_INFRA_PAR_BUS__u_I NFRA_PAR_BUS__rg_ck14_ctrl_force_cl koff	
6	VDNR_DCM_TOP_INFRA_PAR_BUS__u_I NFRA_PAR_BUS__rg_ck14_ctrl_clkslow_ en	
5	VDNR_DCM_TOP_INFRA_PAR_BUS__u_I NFRA_PAR_BUS__rg_ck14_ctrl_clkoff_e n	
4:0	VDNR_DCM_TOP_INFRA_PAR_BUS__u_I NFRA_PAR_BUS__rg_ck13_ctrl_sfsel	

1A020050 VDNR_DCM_TOP_INFRA_PAR_VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PA 00044008
 _BUS_u_INFRA_PAR_BUS_CT_R_BUS control register 14

RL 14

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck16_ctrl_sfssel			
Type													RW			
Reset													0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck16_ctrl_sfssel	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck16_ctrl_sfssel					VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck16_ctrl_force_on	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck16_ctrl_force_clkslow	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck16_ctrl_force_clkoff	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck16_ctrl_clkslow_en	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck16_ctrl_clkoff_en	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck15_ctrl_sfssel				
Type	RW	RW					RW	RW	RW	RW	RW	RW				
Reset	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
19:15	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck16_ctrl_sfsel	
14:10	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck16_ctrl_sfsel	
9	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck16_ctrl_force_on	
8	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck16_ctrl_force_clkslow	
7	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck16_ctrl_force_clkoff	
6	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck16_ctrl_clkslow_en	
5	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck16_ctrl_clkoff_en	
4:0	VDNR_DCM_TOP_INFRA_PAR_BUS_u_INFRA_PAR_BUS_rg_ck15_ctrl_sfsel	

Module name: bcrn_INFRA_PDN_wrapper_u_bcrn_INFRA_PDN_bcrn Base address: (+0x1A03_0000)

Address	Name	Width	Register Function
1A030000	<u>INFRA FAXI BUS u Ink CQDMA M to INFRA FAXI BUS MISI1 AXI QOS REPLACE CTRL_0</u>	32	INFRA_FAXI_BUS_u_Ink_CQDMA_M_to_INFRA_FAXI_BUS_MISI1_AXI_QOS_REPLACE control register 0
1A030004	<u>INFRA FAXI BUS u Ink DEBUG M to INFRA FAXI BUS MISI1 DCM PROT ups CTRL_0</u>	32	INFRA_FAXI_BUS_u_Ink_DEBUG_M_to_INFRA_FAXI_BUS_MISI1_DCM_PROT_ups control register 0
1A030008	<u>INFRA FAXI BUS u Ink DEBUG M to INFRA FAXI BUS MISI1 DCM PROT CTRL_0</u>	32	INFRA_FAXI_BUS_u_Ink_DEBUG_M_to_INFRA_FAXI_BUS_MISI1_DCM_PROT control register 0
1A03000C	<u>INFRA FAXI BUS u Ink DEBUG M to INFRA FAXI BUS MISI1 AXI QOS REPLACE CTRL_0</u>	32	INFRA_FAXI_BUS_u_Ink_DEBUG_M_to_INFRA_FAXI_BUS_MISI1_AXI_QOS_REPLACE control register 0
1A030010	<u>INFRA FAXI BUS u Ink PERI_PAR FAXI BUS SL20 to INFRA FAXI BUS MISI1 DCM PROT ups CTRL_0</u>	32	INFRA_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_SL20_to_INFRA_FAXI_BUS_MISI1_DCM_PROT_ups control register 0
1A030014	<u>INFRA FAXI BUS u Ink PERI_PAR FAXI BUS SL20 to INFRA FAXI BUS MISI1 DCM PROT CTRL_0</u>	32	INFRA_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_SL20_to_INFRA_FAXI_BUS_MISI1_DCM_PROT control register 0
1A030018	<u>INFRA FAXI BUS u Ink INFRA FAXI BUS MISI0C to NET_S AXI SECURE CTRL0 CTRL_0</u>	32	INFRA_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISI0C_to_NET_S_AXI_SECURE_CTRL0 control register 0
1A03001C	<u>INFRA FAXI BUS u Ink PERI_PAR FAXI BUS MISI7B to INFRA FAXI BUS MISI0A DCM PROT ups CTRL_0</u>	32	INFRA_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_MISI7B_to_INFRA_FAXI_BUS_MISI0A_DCM_PROT_ups control register 0
1A030020	<u>INFRA FAXI BUS u Ink PERI_PAR FAXI BUS MISI7B to INFRA FAXI BUS MISI0A DCM PROT CTRL_0</u>	32	INFRA_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_MISI7B_to_INFRA_FAXI_BUS_MISI0A_DCM_PROT control register 0
1A030024	<u>INFRA FAXI BUS u Ink PERI_QAXI BUS MISI3 to INFRA FAXI BUS MISI1 S2F CTRL_0</u>	32	INFRA_FAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI3_to_INFRA_FAXI_BUS_MISI1_S2F control register 0
1A030028	<u>INFRA FAXI BUS u MISI1 CTRL_0</u>	32	INFRA_FAXI_BUS_u_MISI1 control register 0
1A03002C	<u>INFRA FAXI BUS u MISI1 1toN added CTRL_0</u>	32	INFRA_FAXI_BUS_u_MISI1_1toN_added control register 0
1A030030	<u>INFRA FAXI BUS u MISI0A CTRL_0</u>	32	INFRA_FAXI_BUS_u_MISI0A control register 0
1A030034	<u>INFRA FAXI BUS u MISI0C CTRL_0</u>	32	INFRA_FAXI_BUS_u_MISI0C control register 0
1A030038	<u>INFRA FAXI BUS u MISI0C CTRL_1</u>	32	INFRA_FAXI_BUS_u_MISI0C control register 1
1A03003C	<u>INFRA FAXI BUS u SL15 CTRL_0</u>	32	INFRA_FAXI_BUS_u_SL15 control register 0
1A030040	<u>INFRA FAXI BUS u SL3 CTRL_0</u>	32	INFRA_FAXI_BUS_u_SL3 control register 0
1A030044	<u>INFRA FAXI BUS u AXI UP PERI CTRL_0</u>	32	INFRA_FAXI_BUS_u_AXI_UP_PERI control register 0

Address	Name	Width	Register Function
1A030048	<u>INFRA FAXI BUS u SL19 CTRL_0</u>	32	INFRA_FAXI_BUS_u_SL19 control register 0
1A03004C	<u>INFRA FAXI BUS u F2S CTRL_0</u>	32	INFRA_FAXI_BUS_u_F2S control register 0
1A030050	<u>INFRA FAXI BUS u APB2AXI_CTRL_0</u>	32	INFRA_FAXI_BUS_u_APB2AXI control register 0
1A030054	<u>INFRA FAXI BUS u AXI_UP_DFD_CTRL_0</u>	32	INFRA_FAXI_BUS_u_AXI_UP_DFD control register 0
1A030058	<u>INFRA FAXI BUS u SL20 CTRL_0</u>	32	INFRA_FAXI_BUS_u_SL20 control register 0
1A03005C	<u>INFRA FAXI BUS u SL04 CTRL_0</u>	32	INFRA_FAXI_BUS_u_SL04 control register 0

1A030000 **INFRA_FAXI_BUS_u_Ink_CQDMA_M_to_INFRA_FAXI_BUS_AXI_BUS_MISI1_AXI_QOS_REPLACE control** 00000000
MISI1_AXI_QOS_REPLACE_CT register 0
RL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INFRA_FAXI_B US_u_Ink_CQ DMA_M_to_IN FRA_FAXI_BUS _MISI1_AXI_Q OS_REPLACE_ reg_arflush	INFRA_FAXI_B US_u_Ink_CQ DMA_M_to_IN FRA_FAXI_BUS _MISI1_AXI_Q OS_REPLACE_ reg_arultra	INFRA_FAXI_B US_u_Ink_CQ DMA_M_to_IN FRA_FAXI_BUS _MISI1_AXI_Q OS_REPLACE_ reg_awflush	INFRA_FAXI_B US_u_Ink_CQ DMA_M_to_IN FRA_FAXI_BUS _MISI1_AXI_Q OS_REPLACE_ reg_awultra				
Type									RW		RW		RW		RW	
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:6	INFRA_FAXI_BUS_u_Ink_CQDMA_M_to_INFRA_FAXI_BUS_MISI1_AXI_QOS_REPLACE__reg_arflush	This is to replace AXI Read Flush QoS for CQDMA_M
5:4	INFRA_FAXI_BUS_u_Ink_CQDMA_M_to_INFRA_FAXI_BUS_MISI1_AXI_QOS_REPLACE__reg_arultra	This is to replace AXI Read Ultra QoS for CQDMA_M
3:2	INFRA_FAXI_BUS_u_Ink_CQDMA_M_to_INFRA_FAXI_BUS_MISI1_AXI_QOS_REPLACE__reg_awflush	This is to replace AXI Write Flush QoS for CQDMA_M
1:0	INFRA_FAXI_BUS_u_Ink_CQDMA_M_to_INFRA_FAXI_BUS_MISI1_AXI_QOS_REPLACE__reg_awultra	This is to replace AXI Write Ultra QoS for CQDMA_M

1A030004 INFRA_FAXI_BUS_u_Ink_DEBUG_M_to_INFRA_F 00000000
UG_M_to_INFRA_FAXI_BUS_AXI_BUS_MISI1_DCM_PROT_ups control register
MISI1_DCM_PROT_ups_CTRL 0
0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FAXI_B US_u Ink_DE BUG_ M_to_I NFRA_ FAXI_B US_MI SI1_DC M_PRO T_ups_ _axi_cl ock_ga ted_en	INFRA_FAXI_B US_u Ink_D EBUG_ M_to_I NFRA_ FAXI_B US_MI SI1_DC M_PR OT_up s_axi_ clock_g ated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FAXI_BUS_u_Ink_DEBUG_M_to _INFRA_FAXI_BUS_MISI1_DCM_PROT_u ps_axi_clock_gated_en	
0	INFRA_FAXI_BUS_u_Ink_DEBUG_M_to _INFRA_FAXI_BUS_MISI1_DCM_PROT_u ps_axi_clock_gated	

1A030008 INFRA_FAXI_BUS_u_Ink_DEBUG_M_to_INFRA_F 00000000
UG_M_to_INFRA_FAXI_BUS_AXI_BUS_MISI1_DCM_PROT control register 0
MISI1_DCM_PROT_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FAXI_B US_u Ink_DE BUG_ M_to_I NFRA_ FAXI_B US_MI SI1_DC M_PRO T_axi_ clock_g ated_e n	INFRA_FAXI_B US_u Ink_DE BUG_ M_to_I NFRA_ FAXI_B US_MI SI1_DC M_PRO T_axi_ OT_ax i_clock _gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FAXI_BUS_u_Ink_DEBUG_M_to _INFRA_FAXI_BUS_MISI1_DCM_PROT_ axi_clock_gated_en	
0	INFRA_FAXI_BUS_u_Ink_DEBUG_M_to _INFRA_FAXI_BUS_MISI1_DCM_PROT_ axi_clock_gated	

1A03000C INFRA_FAXI_BUS_u_Ink_DEBUG_M_to_INFRA_F 00000000
UG_M_to_INFRA_FAXI_BUS_AXI_BUS_MISI1_AXI_QOS_REPLACE control
MISI1_AXI_QOS_REPLACE_CT register 0
RL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INFRA_FAXI_B US_u_Ink_DE BUG_M_to_INF RA_FAXI_BUS_ MISI1_AXI_QO S_REPLACE__re g_arflush	INFRA_FAXI_B US_u_Ink_DE BUG_M_to_INF RA_FAXI_BUS_ MISI1_AXI_QO S_REPLACE__re g_arultra	INFRA_FAXI_B US_u_Ink_DE BUG_M_to_INF RA_FAXI_BUS_ MISI1_AXI_QO S_REPLACE__re g_awflush	INFRA_FAXI_B US_u_Ink_DE BUG_M_to_INF RA_FAXI_BUS_ MISI1_AXI_QO S_REPLACE__re g_awultra				
Type									RW		RW		RW		RW	
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:6	INFRA_FAXI_BUS_u_Ink_DEBUG_M_to_INFRA_FAXI_BUS_MISI1_AXI_QOS_REPLACE__reg_arflush	This is to replace AXI Read Flush QoS for DEBUG_M
5:4	INFRA_FAXI_BUS_u_Ink_DEBUG_M_to_INFRA_FAXI_BUS_MISI1_AXI_QOS_REPLACE__reg_arultra	This is to replace AXI Read Ultra QoS for DEBUG_M
3:2	INFRA_FAXI_BUS_u_Ink_DEBUG_M_to_INFRA_FAXI_BUS_MISI1_AXI_QOS_REPLACE__reg_awflush	This is to replace AXI Write Flush QoS for DEBUG_M
1:0	INFRA_FAXI_BUS_u_Ink_DEBUG_M_to_INFRA_FAXI_BUS_MISI1_AXI_QOS_REPLACE__reg_awultra	This is to replace AXI Write Ultra QoS for DEBUG_M

1A030010 INFRA_FAXI_BUS_u_Ink_PERI_INFRA_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_SL
PAR_FAXI_BUS_SL20_to_INF20_to_INFRA_FAXI_BUS_MISI1_DCM_PROT_ups
RA_FAXI_BUS_MISI1_DCM_P control register 0
ROT_ups_CTRL_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FAXI_B US_u_Ink_P RI_PAR_FAXI BUS_SL20_t NFRA_o_INFR FAXI_BA_FAXI US_MI_SI1_DC M_PROT_ups _axi_clock_g ted_en	INFRA_FAXI_B US_u_Ink_P RI_PAR_FAXI BUS_SL20_t NFRA_o_INFR FAXI_BA_FAXI US_MI_SI1_DC M_PROT_ups _axi_clock_g ted_en
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FAXI_BUS_u_Ink_PERI_PAR_FAXI I_BUS_SL20_to_INFRA_FAXI_BUS_MISI1 _DCM_PROT_ups__axi_clock_gated_en	
0	INFRA_FAXI_BUS_u_Ink_PERI_PAR_FAXI I_BUS_SL20_to_INFRA_FAXI_BUS_MISI1 _DCM_PROT_ups__axi_clock_gated	

1A030014 INFRA_FAXI_BUS_u_Ink_PERI_INFRA_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_SL
PAR_FAXI_BUS_SL20_to_INF20_to_INFRA_FAXI_BUS_MISI1_DCM_PROT
RA_FAXI_BUS_MISI1_DCM_P control register 0
ROT_CTRL_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FAXI_B US_u_Ink_P RI_PAR_FAXI BUS_SL20_t NFRA_o_INFR FAXI_BA_FAXI US_MI_SI1_DC M_PROT_axi clock_gated_e n	INFRA_FAXI_B US_u_Ink_P RI_PAR_FAXI BUS_SL20_t NFRA_o_INFR FAXI_BA_FAXI US_MI_SI1_DC M_PROT_axi clock_gated_e n
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FAXI_BUS_u_Ink_PERI_PAR_FAXI I_BUS_SL20_to_INFRA_FAXI_BUS_MISI1 _DCM_PROT__axi_clock_gated_en	
0	INFRA_FAXI_BUS_u_Ink_PERI_PAR_FAXI I_BUS_SL20_to_INFRA_FAXI_BUS_MISI1 _DCM_PROT__axi_clock_gated	

1A030018 **INFRA FAXI BUS u Ink INFR INFRA_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIO** 00001801
A FAXI_BUS MISIO C to NET C to NET_S_AXI_SECURE_CTRL0 control register
S_AXI_SECURE_CTRL0 CTRL 0

0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INFRA_FAXI_B_US_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_cg_disable	INFRA_FAXI_B_US_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_bypass	INFRA_FAXI_B_US_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_outstanding_disable	INFRA_FAXI_B_US_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_way_interleave_en	INFRA_FAXI_B_US_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_way_en	INFRA_FAXI_B_US_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_set_wirq	INFRA_FAXI_B_US_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_set_rirq	INFRA_FAXI_B_US_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_sel	INFRA_FAXI_B_US_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_sel	INFRA_FAXI_B_US_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_sel	INFRA_FAXI_B_US_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_sel	INFRA_FAXI_B_US_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_sel	INFRA_FAXI_B_US_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_sel	INFRA_FAXI_B_US_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_sel	INFRA_FAXI_B_US_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_sel	INFRA_FAXI_B_US_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_sel
Type	RW	RW	RW	RW	RW	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15	INFRA_FAXI_BUS_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_cg_disable	
14	INFRA_FAXI_BUS_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_bypass	Bypasses idle check when updating SI setting
13	INFRA_FAXI_BUS_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_outstanding_disable	Slave interface outstanding capability disable control
12	INFRA_FAXI_BUS_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_way_interleave_en	Slave interface read arbiter interleaving function enable control
11	INFRA_FAXI_BUS_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_way_en	Control address decode output path enable of each way
10	INFRA_FAXI_BUS_u_Ink_INFRA_FAXI_B_US_MISIO_C_to_NET_S_AXI_SECURE_CTRL0_axi_secure_ctrl_set_wirq	Slave interface default slave write IRQ status

Bit(s)	Name	Description
9	INFRA_FAXI_BUS__u_Ink_INFRA_FAXI_B	Slave interface default slave read IRQ status US_MISIOC_to_NET_S_AXI_SECURE_CTR LO__axi_secure_ctrl_set_rirq
8:7	INFRA_FAXI_BUS__u_Ink_INFRA_FAXI_B	Slave interface current write response channel way selection US_MISIOC_to_NET_S_AXI_SECURE_CTR LO__axi_secure_ctrl_b_chnl_sel
6	INFRA_FAXI_BUS__u_Ink_INFRA_FAXI_B	Slave interface write response ID is missed status US_MISIOC_to_NET_S_AXI_SECURE_CTR LO__axi_secure_ctrl_set_bid_miss
5:4	INFRA_FAXI_BUS__u_Ink_INFRA_FAXI_B	Slave interface current read channel way selection US_MISIOC_to_NET_S_AXI_SECURE_CTR LO__axi_secure_ctrl_r_chnl_sel
3	INFRA_FAXI_BUS__u_Ink_INFRA_FAXI_B	Slave interface Read ID is missed status US_MISIOC_to_NET_S_AXI_SECURE_CTR LO__axi_secure_ctrl_set_rid_miss
2	INFRA_FAXI_BUS__u_Ink_INFRA_FAXI_B	Slave interface Read Channel Outstanding Busy US_MISIOC_to_NET_S_AXI_SECURE_CTR LO__axi_secure_ctrl_rd_ot_busy
1	INFRA_FAXI_BUS__u_Ink_INFRA_FAXI_B	Slave interface Write Channel Outstanding Busy US_MISIOC_to_NET_S_AXI_SECURE_CTR LO__axi_secure_ctrl_wr_ot_busy
0	INFRA_FAXI_BUS__u_Ink_INFRA_FAXI_B	Slave interface control signal updated status US_MISIOC_to_NET_S_AXI_SECURE_CTR LO__axi_secure_ctrl_ctrl_updated

1A03001C INFRA_FAXI_BUS_u_Ink_PERI_INFRA_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_M
 _PAR_FAXI_BUS_MISI7B_to_IISI7B_to_INFRA_FAXI_BUS_MISIOA_DCM_PROT_
 NFRA_FAXI_BUS_MISIOA_DC ups control register 0
 M_PROT ups_CTRL 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FAXI_B US_u_Ink_P RI_PAR_FAXI BUS_M_B ISI7B_t o_INFRA_F A_FAXI_B BUS_MISIO _DCM_PRO ups_a xi_cloc k_gate d_en	INFRA_FAXI_B US_u_Ink_P RI_PAR_FAXI BUS_M_B ISI7B_t o_INFRA_F A_FAXI_B BUS_MISIO _DCM_PRO ups_a xi_cloc s_axi clock_g ated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FAXI_BUS_u_Ink_PERI_PAR_FAXI I_BUS_MISI7B_to_INFRA_FAXI_BUS_MIS IOA_DCM_PROT ups__axi_clock_gated_ en	
0	INFRA_FAXI_BUS_u_Ink_PERI_PAR_FAXI I_BUS_MISI7B_to_INFRA_FAXI_BUS_MIS IOA_DCM_PROT ups__axi_clock_gated	

1A030020 INFRA_FAXI_BUS_u_Ink_PERI_INFRA_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_M 00000000
_PAR_FAXI_BUS_MISI7B_to_IISI7B_to_INFRA_FAXI_BUS_MISIOA_DCM_PROT
INFRA_FAXI_BUS_MISIOA_DC control register 0
M_PROT_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INFRA_FAXI_B US_u_Ink_P RI_PAR_FAXI _BUS_M_B ISI7B_t o_INFRA_F _BUS_MISIO _DCM_PROT _axi_clock gated_en	INFRA_FAXI_B US_u_Ink_P RI_PAR_FAXI _BUS_M_B ISI7B_t o_INFRA_F _BUS_MISIO _DCM_PROT _axi_clock gated_en
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	INFRA_FAXI_BUS_u_Ink_PERI_PAR_FAXI I_BUS_MISI7B_to_INFRA_FAXI_BUS_MIS IOA_DCM_PROT_axi_clock_gated_en	
0	INFRA_FAXI_BUS_u_Ink_PERI_PAR_FAXI I_BUS_MISI7B_to_INFRA_FAXI_BUS_MIS IOA_DCM_PROT_axi_clock_gated	

1A030024 INFRA_FAXI_BUS_u_Ink_PERI_INFRA_FAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI3_ 0000001F
QAXI_BUS_MISI3_to_INFRA_to_INFRA_FAXI_BUS_MISI1_S2F control register
FAXI_BUS_MISI1_S2F_CTRL_0

0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												INFRA_FAXI_B US_u_Ink_PER I_QAXI_BUS_M ISI3_to_INFRA FAXI_BUS_MISI 1_S2F_in_arfl ush_thre		INFRA_FAXI_B US_u_Ink_PER I_QAXI_BUS_M ISI3_to_INFRA FAXI_BUS_MISI 1_S2F_in_awfl ush_thre		INFRA_ FAXI_B US_u _Ink_P ERI_QA XI_BUS _MISI3 _to_IN FRA_F AXI_BU S_MISI 1_S2F_ _axi_id le_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	INFRA_FAXI_BUS_u_Ink_PERI_QAXI_B S_MISI3_to_INFRA_FAXI_BUS_MISI1_S2 F_in_arflush_thre	
2:1	INFRA_FAXI_BUS_u_Ink_PERI_QAXI_B S_MISI3_to_INFRA_FAXI_BUS_MISI1_S2 F_in_awflush_thre	
0	INFRA_FAXI_BUS_u_Ink_PERI_QAXI_B S_MISI3_to_INFRA_FAXI_BUS_MISI1_S2 F_axi_idle_out	

1A030028 **INFRA_FAXI_BUS_u_MISI1_C** INFRA_FAXI_BUS_u_MISI1 control register 0
TRL_0

0000001C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											INFRA_FAXI_BUS_u_MISI1_cg_disable	INFRA_FAXI_BUS_u_MISI1_mi_outstanding_extend_en	INFRA_FAXI_BUS_u_MISI1_mi_qos_on	INFRA_FAXI_BUS_u_MISI1_mi_ctrl_updated	INFRA_FAXI_BUS_u_MISI1_mi_r_busy	INFRA_FAXI_BUS_u_MISI1_mi_w_busy
Type											RW	RW	RW	RO	RO	RO
Reset											0	1	1	1	0	0

Bit(s)	Name	Description
5	INFRA_FAXI_BUS_u_MISI1_cg_disable	
4	INFRA_FAXI_BUS_u_MISI1_INFRA_FAXI_BUS_u_MISI1_mi_outstanding_extend_en	
3	INFRA_FAXI_BUS_u_MISI1_INFRA_FAXI_BUS_u_MISI1_mi_qos_on	
2	INFRA_FAXI_BUS_u_MISI1_INFRA_FAXI_BUS_u_MISI1_mi_ctrl_updated	INFRA_FAXI_BUS_u_MISI1_mi master interface control signal updated status
1	INFRA_FAXI_BUS_u_MISI1_INFRA_FAXI_BUS_u_MISI1_mi_r_busy	INFRA_FAXI_BUS_u_MISI1_mi master interface read busy
0	INFRA_FAXI_BUS_u_MISI1_INFRA_FAXI_BUS_u_MISI1_mi_w_busy	INFRA_FAXI_BUS_u_MISI1_mi master interface write busy

0001E001

register 0

Bit(s)	Name	Description
19	INFRA_FAXI_BUS__u_MISI1_1toN_adde d__cg_disable	
18	INFRA_FAXI_BUS__u_MISI1_1toN_adde d__INFRA_FAXI_BUS_u_MISI1_1toN_ad ded_si_ctrl_bypass	Bypasses idle check when updating SI setting
17	INFRA_FAXI_BUS__u_MISI1_1toN_adde d__INFRA_FAXI_BUS_u_MISI1_1toN_ad ded_si_outstanding_disable	si_cabgen slave interface outstanding capability disable control
16:15	INFRA_FAXI_BUS__u_MISI1_1toN_adde d__INFRA_FAXI_BUS_u_MISI1_1toN_ad ded si way interleave en	INFRA_FAXI_BUS_u_MISI1_1toN_added_si slave interface read arbiter interleaving function enable control

Bit(s)	Name	Description
14:13	INFRA_FAXI_BUS__u_MISI1_1toN_adde d__INFRA_FAXI_BUS__u_MISI1_1toN_ad ded_si_way_en	Control INFRA_FAXI_BUS__u_MISI1_1toN_added_si address decode output path enable of each way
12	INFRA_FAXI_BUS__u_MISI1_1toN_adde d__INFRA_FAXI_BUS__u_MISI1_1toN_ad ded_si_dfslv_set_wirq	INFRA_FAXI_BUS__u_MISI1_1toN_added_si slave interface default slave write IRQ status
11	INFRA_FAXI_BUS__u_MISI1_1toN_adde d__INFRA_FAXI_BUS__u_MISI1_1toN_ad ded_si_dfslv_set_rirq	INFRA_FAXI_BUS__u_MISI1_1toN_added_si slave interface default slave read IRQ status
10:8	INFRA_FAXI_BUS__u_MISI1_1toN_adde d__INFRA_FAXI_BUS__u_MISI1_1toN_ad ded_si_b_chnl_sel	INFRA_FAXI_BUS__u_MISI1_1toN_added_si slave interface current write response channel way selection
7	INFRA_FAXI_BUS__u_MISI1_1toN_adde d__INFRA_FAXI_BUS__u_MISI1_1toN_ad ded_si_set_bid_miss	INFRA_FAXI_BUS__u_MISI1_1toN_added_si slave interface write response ID is missed status
6:4	INFRA_FAXI_BUS__u_MISI1_1toN_adde d__INFRA_FAXI_BUS__u_MISI1_1toN_ad ded_si_r_chnl_sel	INFRA_FAXI_BUS__u_MISI1_1toN_added_si slave interface current read channel way selection
3	INFRA_FAXI_BUS__u_MISI1_1toN_adde d__INFRA_FAXI_BUS__u_MISI1_1toN_ad ded_si_set_rid_miss	INFRA_FAXI_BUS__u_MISI1_1toN_added_si slave interface Read ID is missed status
2	INFRA_FAXI_BUS__u_MISI1_1toN_adde d__INFRA_FAXI_BUS__u_MISI1_1toN_ad ded_si_rd_ot_busy	INFRA_FAXI_BUS__u_MISI1_1toN_added_si slave interface Read Channel Outstanding Busy
1	INFRA_FAXI_BUS__u_MISI1_1toN_adde d__INFRA_FAXI_BUS__u_MISI1_1toN_ad ded_si_wr_ot_busy	INFRA_FAXI_BUS__u_MISI1_1toN_added_si slave interface Write Channel Outstanding Busy
0	INFRA_FAXI_BUS__u_MISI1_1toN_adde d__INFRA_FAXI_BUS__u_MISI1_1toN_ad ded_si_ctrl_updated	INFRA_FAXI_BUS__u_MISI1_1toN_added_si slave interface control signal updated status

1A030030 **INFRA_FAXI_BUS_u_MISIOA_INFRA_FAXI_BUS_u_MISIOA control register 0**
CTRL_0

0000001C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											INFRA_FAXI_BUS_u_MISIOA_cg_disable	INFRA_FAXI_BUS_u_MISIOA_INFRA_FAXI_BUS_u_MISIOA_mi_outstanding_extend_en	INFRA_FAXI_BUS_u_MISIOA_INFRA_FAXI_BUS_u_MISIOA_mi_qos_on	INFRA_FAXI_BUS_u_MISIOA_INFRA_FAXI_BUS_u_MISIOA_mi_ctrl_updated	INFRA_FAXI_BUS_u_MISIOA_INFRA_FAXI_BUS_u_MISIOA_mi_r_busy	INFRA_FAXI_BUS_u_MISIOA_INFRA_FAXI_BUS_u_MISIOA_mi_w_busy
Type											RW	RW	RW	RO	RO	RO
Reset											0	1	1	1	0	0

Bit(s)	Name	Description
5	INFRA_FAXI_BUS_u_MISIOA_cg_disable	
4	INFRA_FAXI_BUS_u_MISIOA_INFRA_FAXI_BUS_u_MISIOA_mi_outstanding_extend_en	
3	INFRA_FAXI_BUS_u_MISIOA_INFRA_FAXI_BUS_u_MISIOA_mi_qos_on	
2	INFRA_FAXI_BUS_u_MISIOA_INFRA_FAXI_BUS_u_MISIOA_mi_ctrl_updated	INFRA_FAXI_BUS_u_MISIOA_mi master interface control signal updated status
1	INFRA_FAXI_BUS_u_MISIOA_INFRA_FAXI_BUS_u_MISIOA_mi_r_busy	INFRA_FAXI_BUS_u_MISIOA_mi master interface read busy
0	INFRA_FAXI_BUS_u_MISIOA_INFRA_FAXI_BUS_u_MISIOA_mi_w_busy	INFRA_FAXI_BUS_u_MISIOA_mi master interface write busy

1A030034 **INFRA_FAXI_BUS_u_MISIOc_INFRA_FAXI_BUS_u_MISIOc control register 0**
CTRL_0

001FE001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INFRA_FAXI_BUS__u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_b_chnl_sel										INFRA_FAXI_BUS_u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_set_bid_miss	INFRA_FAXI_BUS__u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_way_en				
Type	RO										RO	RW				
Reset		0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INFRA_FAXI_BUS__u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_way_en			INFRA_FAXI_BUS__u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_r_chnl_sel								INFRA_FAXI_BUS_u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_set_rid_miss	INFRA_FAXI_BUS_u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_rd_ot_busy	INFRA_FAXI_BUS_u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_wr_ot_busy	INFRA_FAXI_BUS_u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_ctrl_updated	
Type	RW			RO								RO	RO	RO	RO	
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
30:22	INFRA_FAXI_BUS__u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_b_chnl_sel	INFRA_FAXI_BUS_u_MISIOc_si slave interface current write response channel way selection
21	INFRA_FAXI_BUS__u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_set_bid_miss	INFRA_FAXI_BUS_u_MISIOc_si slave interface write response ID is missed status
20:13	INFRA_FAXI_BUS__u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_way_en	Control INFRA_FAXI_BUS_u_MISIOc_si address decode output path enable of each way
12:4	INFRA_FAXI_BUS__u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_r_chnl_sel	INFRA_FAXI_BUS_u_MISIOc_si slave interface current read channel way selection
3	INFRA_FAXI_BUS__u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_set_rid_miss	INFRA_FAXI_BUS_u_MISIOc_si slave interface Read ID is missed status
2	INFRA_FAXI_BUS__u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_rd_ot_busy	INFRA_FAXI_BUS_u_MISIOc_si slave interface Read Channel Outstanding Busy
1	INFRA_FAXI_BUS__u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_wr_ot_busy	INFRA_FAXI_BUS_u_MISIOc_si slave interface Write Channel Outstanding Busy
0	INFRA_FAXI_BUS__u_MISIOc__INFRA_FAXI_BUS_u_MISIOc_si_ctrl_updated	INFRA_FAXI_BUS_u_MISIOc_si slave interface control signal updated status

1A030038 INFRA_FAXI_BUS_u_MISIOc INFRA_FAXI_BUS_u_MISIOc control register 1
CTRL_1

000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				INFRA_FAXI_BUS_u_MISIOc_cg_disable	INFRA_FAXI_BUS_u_MISIOc_INFRA_FAXI_BUS_u_MISIOc_si_ctrl_bypass	INFRA_FAXI_BUS_u_MISIOc_INFRA_FAXI_BUS_u_MISIOc_si_dfslv_set_wirq	INFRA_FAXI_BUS_u_MISIOc_INFRA_FAXI_BUS_u_MISIOc_si_dfslv_set_rirq	INFRA_FAXI_BUS_u_MISIOc_INFRA_FAXI_BUS_u_MISIOc_si_outstanding_disable	INFRA_FAXI_BUS_u_MISIOc_INFRA_FAXI_BUS_u_MISIOc_si_way_interleave_en							
Type				RW	RW	RO	RO	RW	RW							
Reset				0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
12	INFRA_FAXI_BUS_u_MISIOc_cg_disable	
11	INFRA_FAXI_BUS_u_MISIOc_INFRA_FAXI_BUS_u_MISIOc_si_ctrl_bypass	Bypasses idle check when updating SI setting
10	INFRA_FAXI_BUS_u_MISIOc_INFRA_FAXI_BUS_u_MISIOc_si_dfslv_set_wirq	INFRA_FAXI_BUS_u_MISIOc_si slave interface default slave write IRQ status
9	INFRA_FAXI_BUS_u_MISIOc_INFRA_FAXI_BUS_u_MISIOc_si_dfslv_set_rirq	INFRA_FAXI_BUS_u_MISIOc_si slave interface default slave read IRQ status
8	INFRA_FAXI_BUS_u_MISIOc_INFRA_FAXI_BUS_u_MISIOc_si_outstanding_disable	si_cabgen slave interface outstanding capability disable control
7:0	INFRA_FAXI_BUS_u_MISIOc_INFRA_FAXI_BUS_u_MISIOc_si_way_interleave_en	INFRA_FAXI_BUS_u_MISIOc_si slave interface read arbiter interleaving function enable control

1A03003C INFRA_FAXI_BUS_u_SL15_CTL_0 INFRA_FAXI_BUS_u_SL15 control register 0
RL_0

0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												INFRA_FAXI_BUS_u_SL15_in_arflush_thre		INFRA_FAXI_BUS_u_SL15_in_awflush_thre		INFRA_FAXI_BUS_u_SL15_axi_idle_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	INFRA_FAXI_BUS_u_SL15_in_arflush_thre	
2:1	INFRA_FAXI_BUS_u_SL15_in_awflush_thre	
0	INFRA_FAXI_BUS_u_SL15_axi_idle_out	

1A030040 **INFRA_FAXI_BUS_u_SL3_CTR** INFRA_FAXI_BUS_u_SL3 control register 0
L_0

0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												INFRA_FAXI_B US__u_SL3_in _arflush_thre		INFRA_FAXI_B US__u_SL3_in _awflush_thre		INFRA_FAXI_B US__u_SL3__ axi_idl e_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	INFRA_FAXI_BUS__u_SL3__in_arflush_thre	
2:1	INFRA_FAXI_BUS__u_SL3__in_awflush_thre	
0	INFRA_FAXI_BUS__u_SL3__axi_idle_out	

1A030044 INFRA_FAXI_BUS_u_AXI_UP_PERI_CTRL_0 INFRA_FAXI_BUS_u_AXI_UP_PERI control
PERI_CTRL_0 register 0

00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INFRA_FAXI_BUS_u_AXI_UP_PERI__no_dummy_read_en
Type																RW
Reset																1

Bit(s)	Name	Description
0	INFRA_FAXI_BUS__u_AXI_UP_PERI__no_dummy_read_en	Enables no dummy read

1A030048 INFRA_FAXI_BUS_u_SL19_CTL_0 INFRA_FAXI_BUS_u_SL19 control register 0

0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												INFRA_FAXI_BUS_u_SL19_in_arflush_thre		INFRA_FAXI_BUS_u_SL19_in_awflush_thre		INFRA_FAXI_BUS_u_SL19_axi_idle_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	INFRA_FAXI_BUS_u_SL19_in_arflush_thre	
2:1	INFRA_FAXI_BUS_u_SL19_in_awflush_thre	
0	INFRA_FAXI_BUS_u_SL19_axi_idle_out	

1A03004C INFRA_FAXI_BUS_u_F2S_CTL_0 INFRA_FAXI_BUS_u_F2S control register 0

0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												INFRA_FAXI_B US_u_F2S_in _arflush_thre		INFRA_FAXI_B US_u_F2S_in _awflush_thre		INFRA_FAXI_B US_u_F2S_ _axi_idl e_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	INFRA_FAXI_BUS_u_F2S_in_arflush_thre	
2:1	INFRA_FAXI_BUS_u_F2S_in_awflush_thre	
0	INFRA_FAXI_BUS_u_F2S_axi_idle_out	

1A030050 INFRA FAXI BUS u APB2AXI INFRA_FAXI_BUS_u_APB2AXI control register 0 00000000
CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INFRA_FAXI_BUS_u_APB2AXI_other_sig
Type																RW
Reset																0

Bit(s)	Name	Description
0	INFRA_FAXI_BUS_u_APB2AXI_other_sig	

1A030054 INFRA FAXI BUS u AXI UP INFRA_FAXI_BUS_u_AXI_UP_DFD control 00000001
DFD_CTRL_0 register 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INFRA_FAXI_BUS_u_AXI_UP_DFD_no_dummy_read_en
Type																RW
Reset																1

Bit(s)	Name	Description
0	INFRA_FAXI_BUS_u_AXI_UP_DFD_no_dummy_read_en	Enables no dummy read

1A030058 INFRA_FAXI_BUS_u_SL20_CT INFRA_FAXI_BUS_u_SL20 control register 0
RL_0

000000FB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					INFRA_FAXI_B US__u_SL20__ mst_sync_sel		INFRA_FAXI_B US__u_SL20__s lv_sync_sel		INFRA_FAXI_B US__u_SL20__i n_arflush_thre		INFRA_FAXI_B US__u_SL20__i n_arflush_thre		INFRA_FAXI_B US__u_SL20__ sample_sel	INFRA_FAXI_B US__u_SL20__ sync_mode	INFRA_FAXI_B US__u_SL20__ axi_idle_out	INFRA_FAXI_B US__u_SL20__ axi_idle_out_reg
Type					RW		RW		RW		RW		RW	RW	RO	RO
Reset					0	0	0	0	1	1	1	1	1	0	1	1

Bit(s)	Name	Description
11:10	INFRA_FAXI_BUS__u_SL20__mst_sync_sel	
9:8	INFRA_FAXI_BUS__u_SL20__slv_sync_sel	
7:6	INFRA_FAXI_BUS__u_SL20__in_arflush_thre	
5:4	INFRA_FAXI_BUS__u_SL20__in_arflush_thre	
3	INFRA_FAXI_BUS__u_SL20__sample_sel	
2	INFRA_FAXI_BUS__u_SL20__sync_mode	Sync mode switch for ASLICE
1	INFRA_FAXI_BUS__u_SL20__axi_idle_out	
0	INFRA_FAXI_BUS__u_SL20__axi_idle_out_reg	

1A03005C **INFRA_FAXI_BUS_u_SL04_CTL_0** INFRA_FAXI_BUS_u_SL04 control register 0
RL_0

0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												INFRA_FAXI_BUS_u_SL04_in_arflush_thre		INFRA_FAXI_BUS_u_SL04_in_awflush_thre		INFRA_FAXI_BUS_u_SL04_axi_idle_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	INFRA_FAXI_BUS_u_SL04_in_arflush_thre	
2:1	INFRA_FAXI_BUS_u_SL04_in_awflush_thre	
0	INFRA_FAXI_BUS_u_SL04_axi_idle_out	

Module name: bcrn_PERI_AO_wrapper_u_bcrn_PERI_AO_bcrn Base address: (+0x1A04_0000)

Address	Name	Width	Register Function
1A040000	<u>PERI_QAXI_AO_BUS_u_Ink_P</u> <u>ERI_QAXI_AO_BUS_SI13_to_S</u> <u>GMII_SBUS0_S_ASYNC_CTRL</u> <u>0</u>	32	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_SGMII_SBUS0_S_ASYNC control register 0
1A040004	<u>PERI_QAXI_AO_BUS_u_Ink_P</u> <u>ERI_QAXI_AO_BUS_SI13_to_S</u> <u>GMII_SBUS1_S_ASYNC_CTRL</u> <u>0</u>	32	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_SGMII_SBUS1_S_ASYNC control register 0
1A040008	<u>PERI_QAXI_AO_BUS_u_Ink_P</u> <u>ERI_QAXI_AO_BUS_SI13_to</u> <u>USXGMII_SBUS0_S_ASYNC CT</u> <u>RL_0</u>	32	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_USXGMII_SBUS0_S_ASYNC control register 0
1A04000C	<u>PERI_QAXI_AO_BUS_u_Ink_P</u> <u>ERI_QAXI_AO_BUS_SI13_to</u> <u>USXGMII_SBUS1_S_ASYNC CT</u> <u>RL_0</u>	32	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_USXGMII_SBUS1_S_ASYNC control register 0
1A040010	<u>PERI_QAXI_AO_BUS_u_Ink_P</u> <u>ERI_QAXI_AO_BUS_SI13_to E</u> <u>TH2P5G_S_ASYNC_CTRL_0</u>	32	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_ETH2P5G_S_ASYNC control register 0
1A040014	<u>PERI_QAXI_AO_BUS_u_SI11</u> <u>AXI2SBUS_added_CTRL_0</u>	32	PERI_QAXI_AO_BUS_u_SI11_AXI2SBUS_added control register 0
1A040018	<u>PERI_QAXI_AO_BUS_u_SI11</u> <u>CTRL_0</u>	32	PERI_QAXI_AO_BUS_u_SI11 control register 0
1A04001C	<u>PERI_QAXI_AO_BUS_u_SI11</u> <u>CTRL_1</u>	32	PERI_QAXI_AO_BUS_u_SI11 control register 1
1A040020	<u>PERI_QAXI_AO_BUS_u_SI11</u> <u>CTRL_2</u>	32	PERI_QAXI_AO_BUS_u_SI11 control register 2
1A040024	<u>PERI_QAXI_AO_BUS_u_SI11</u> <u>CTRL_3</u>	32	PERI_QAXI_AO_BUS_u_SI11 control register 3
1A040028	<u>PERI_QAXI_AO_BUS_u_SI11</u> <u>CTRL_4</u>	32	PERI_QAXI_AO_BUS_u_SI11 control register 4
1A04002C	<u>PERI_QAXI_AO_BUS_u_SI11</u> <u>CTRL_5</u>	32	PERI_QAXI_AO_BUS_u_SI11 control register 5
1A040030	<u>PERI_QAXI_AO_BUS_u_SI13</u> <u>CTRL_0</u>	32	PERI_QAXI_AO_BUS_u_SI13 control register 0
1A040034	<u>PERI_QAXI_AO_BUS_u_SI18</u> <u>CTRL_0</u>	32	PERI_QAXI_AO_BUS_u_SI18 control register 0
1A040038	<u>PERI_QAXI_AO_BUS_u_SI18</u> <u>CTRL_1</u>	32	PERI_QAXI_AO_BUS_u_SI18 control register 1
1A04003C	<u>PERI_QAXI_AO_BUS_u_SI18</u> <u>CTRL_2</u>	32	PERI_QAXI_AO_BUS_u_SI18 control register 2

1A040000 PERI_QAXI_AO_BUS_u_Ink_P PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS 00000004
 ERI_QAXI_AO_BUS_SI13_to_S_SI13_to_SGMII_SBUS0_S_ASYNC control
 GMII_SBUS0_S_ASYNC_CTRL register 0
 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_SGMII_SBUS0_S_ASYNC_way_en	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_SGMII_SBUS0_S_ASYNC_early_en	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_SGMII_SBUS0_S_ASYNC_ctrl_update
Type														RW	RW	RO
Reset														1	0	0

Bit(s)	Name	Description
2	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_SGMII_SBUS0_S_ASYNC_way_en	
1	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_SGMII_SBUS0_S_ASYNC_early_en	
0	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_SGMII_SBUS0_S_ASYNC_ctrl_update	

1A040004 PERI_QAXI_AO_BUS_u_Ink_P PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS 00000004
 ERI_QAXI_AO_BUS_SI13_to_S_SI13_to_SGMII_SBUS1_S_ASYNC control
 GMII_SBUS1_S_ASYNC_CTRL register 0
 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_SGMII_SBUS1_S_ASYNC_way_en	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_SGMII_SBUS1_S_ASYNC_early_en	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_SGMII_SBUS1_S_ASYNC_ctrl_update
Type														RW	RW	RO
Reset														1	0	0

Bit(s)	Name	Description
2	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_SGMII_SBUS1_S_ASYNC_way_en	
1	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_SGMII_SBUS1_S_ASYNC_early_en	
0	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_SGMII_SBUS1_S_ASYNC_ctrl_update	

1A040008 PERI_QAXI_AO_BUS_u_Ink_P PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS 00000004
 ERI_QAXI_AO_BUS_SI13_to_SI13_to_USXGMII_SBUS0_S_ASYNC control
 USXGMII_SBUS0_S_ASYNC_C register 0
 TRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_USXGMII_SBUS0_S_ASYNC_way_en	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_USXGMII_SBUS0_S_ASYNC_early_en	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_USXGMII_SBUS0_S_ASYNC_ctrl_update
Type														RW	RW	RO
Reset														1	0	0

Bit(s)	Name	Description
2	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_USXGMII_SBUS0_S_ASYNC_way_en	
1	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_USXGMII_SBUS0_S_ASYNC_early_en	
0	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_USXGMII_SBUS0_S_ASYNC_ctrl_update	

1A04000C PERI_QAXI_AO_BUS_u_Ink_P PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS 00000004
 ERI_QAXI_AO_BUS_SI13_to_SI13_to_USXGMII_SBUS1_S_ASYNC control
 USXGMII_SBUS1_S_ASYNC_C register 0
 TRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_USXGMII_SBUS1_S_ASYNC_way_en	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_USXGMII_SBUS1_S_ASYNC_early_en	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_USXGMII_SBUS1_S_ASYNC_ctrl_update
Type														RW	RW	RO
Reset														1	0	0

Bit(s)	Name	Description
2	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_USXGMII_SBUS1_S_ASYNC_way_en	
1	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_USXGMII_SBUS1_S_ASYNC_early_en	
0	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_USXGMII_SBUS1_S_ASYNC_ctrl_update	

1A040010 PERI_QAXI_AO_BUS_u_Ink_P PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS 00000004
 ERI_QAXI_AO_BUS_SI13_to _SI13_to_ETH2P5G_S_ASYNC control register 0
 ETH2P5G_S_ASYNC_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_ETH2P5G_S_ASYNC_way_en	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_ETH2P5G_S_ASYNC_early_en	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_ETH2P5G_S_ASYNC_ctrl_update
Type														RW	RW	RO
Reset														1	0	0

Bit(s)	Name	Description
2	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_ETH2P5G_S_ASYNC_way_en	
1	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_ETH2P5G_S_ASYNC_early_en	
0	PERI_QAXI_AO_BUS_u_Ink_PERI_QAXI_AO_BUS_SI13_to_ETH2P5G_S_ASYNC_ctrl_update	

1A040014 PERI_QAXI_AO_BUS_u_SI11 PERI_QAXI_AO_BUS_u_SI11_AXI2SBUS_added AXI2SBUS_added_CTRL_0 control register 0 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PERI_QAXI_AO_BUS_u_SI11_AXI2SBUS_added_enable_slv_err_resp	PERI_QAXI_AO_BUS_u_SI11_AXI2SBUS_added_wfifo_threshold	
Type														RW	RW	
Reset														1	0	0

Bit(s)	Name	Description
2	PERI_QAXI_AO_BUS_u_SI11_AXI2SBUS_added_enable_slv_err_resp	
1:0	PERI_QAXI_AO_BUS_u_SI11_AXI2SBUS_added_wfifo_threshold	

1A040018 PERI_QAXI_AO_BUS_u_SI11 PERI_QAXI_AO_BUS_u_SI11 control register 0 CTRL_0 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PERI_QAXI_AO_BUS_u_SI11_s2p_idle
Type																RO
Reset																1

Bit(s)	Name	Description
0	PERI_QAXI_AO_BUS_u_SI11_s2p_idle	Idle signal (Synchronous to Input Clock Domain)

1A04001C PERI_QAXI_AO_BUS_u_SI11 PERI_QAXI_AO_BUS_u_SI11 control register 1 FFFFFFFF
CTRL_1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PERI_QAXI_AO_BUS__u_SI11__way_en_ready															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_AO_BUS__u_SI11__way_en_ready															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	PERI_QAXI_AO_BUS__u_SI11__way_en_ready	

1A040020 PERI_QAXI_AO_BUS_u_SI11 PERI_QAXI_AO_BUS_u_SI11 control register 2 00000000
CTRL_2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PERI_QAXI_AO_BUS__u_SI11__force_pready_high															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_AO_BUS__u_SI11__force_pready_high															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PERI_QAXI_AO_BUS__u_SI11__force_pready_high	

1A040024 PERI_QAXI_AO_BUS_u_SI11 PERI_QAXI_AO_BUS_u_SI11 control register 3
CTRL_3

00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PERI_QAXI_AO_BUS_u_SI11_ctrl_update_status
Type																RO
Reset																1

Bit(s)	Name	Description
0	PERI_QAXI_AO_BUS_u_SI11_ctrl_update_status	

1A040028 PERI_QAXI_AO_BUS_u_SI11 PERI_QAXI_AO_BUS_u_SI11 control register 4
CTRL_4

FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PERI_QAXI_AO_BUS_u_SI11_way_en															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_AO_BUS_u_SI11_way_en															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	PERI_QAXI_AO_BUS_u_SI11_way_en	

1A04002C PERI_QAXI_AO_BUS__u_SI11 PERI_QAXI_AO_BUS__u_SI11 control register 5
CTRL_5

00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_QAXI_AO_BUS__u_SI11_enable_slv_err_resp	PERI_QAXI_AO_BUS__u_SI11_ctrl_bypass
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
1	PERI_QAXI_AO_BUS__u_SI11_enable_slv_err_resp	
0	PERI_QAXI_AO_BUS__u_SI11_ctrl_bypass	

1A040030 PERI_QAXI_AO_BUS__u_SI13 PERI_QAXI_AO_BUS__u_SI13 control register 0
CTRL_0

00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PERI_QAXI_AO_BUS__u_SI13__enable_slv_err_resp	PERI_QAXI_AO_BUS__u_SI13__wfifo_threshold	
Type														RW	RW	
Reset														1	0	0

Bit(s)	Name	Description
2	PERI_QAXI_AO_BUS__u_SI13__enable_slv_err_resp	
1:0	PERI_QAXI_AO_BUS__u_SI13__wfifo_threshold	

1A040034 PERI_QAXI_AO_BUS__u_SI18__PERI_QAXI_AO_BUS__u_SI18 control register 0
CTRL_0

001FFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												PERI_QAXI_AO_BUS__u_SI18__ctrl_update_status	PERI_QAXI_AO_BUS__u_SI18__way_en_ready			
Type												RO	RO			
Reset												1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_AO_BUS__u_SI18__way_en_ready															PERI_QAXI_AO_BUS__u_SI18__s2p_idle
Type	RO															RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
20	PERI_QAXI_AO_BUS__u_SI18__ctrl_update_status	
19:1	PERI_QAXI_AO_BUS__u_SI18__way_en_ready	
0	PERI_QAXI_AO_BUS__u_SI18__s2p_idle	Idle signal (Synchronous to Input Clock Domain)

1A040038 PERI_QAXI_AO_BUS_u_SI18 PERI_QAXI_AO_BUS_u_SI18 control register 1

00000000

CTRL_1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														PERI_QAXI_AO_BUS_u_SI18_force_pready_high		
Type														RW		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_AO_BUS_u_SI18_force_pready_high															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18:0	PERI_QAXI_AO_BUS_u_SI18_force_pready_high	

1A04003C PERI_QAXI_AO_BUS_u_SI18 PERI_QAXI_AO_BUS_u_SI18 control register 2

0017FFFF

CTRL_2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												PERI_QAXI_AO_BUS_u_SI18_enable_slv_err_resp	PERI_QAXI_AO_BUS_u_SI18_ctrl_bypass	PERI_QAXI_AO_BUS_u_SI18_way_en		
Type												RW	RW	RW		
Reset												1	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_AO_BUS_u_SI18_way_en															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
20	PERI_QAXI_AO_BUS_u_SI18_enable_slv_err_resp	
19	PERI_QAXI_AO_BUS_u_SI18_ctrl_bypass	
18:0	PERI_QAXI_AO_BUS_u_SI18_way_en	

Module name: bcrm_PERI_AO2_wrapper_u_bcrm_PERI_AO2_bcrm Base address: (+0x1A05_0000)

Address	Name	Width	Register Function
1A050000	<u>PERI_QAXI_AO_BUS_SUB2_u_Ink_PERI_QAXI_AO_BUS_SUB2_SI18B_to_DEBUG_CTRL_FMEM_AO_APB_S_ASYNC_CTRL_0</u>	32	PERI_QAXI_AO_BUS_SUB2_u_Ink_PERI_QAXI_AO_BUS_SUB2_SI18B_to_DEBUG_CTRL_FMEM_AO_APB_S_ASYNC control register 0
1A050004	<u>PERI_QAXI_AO_BUS_SUB2_u_Ink_PERI_QAXI_AO_BUS_SUB2_SI18B_to_DEVICE_APC_FMEM_AO_APB_S_ASYNC_CTRL_0</u>	32	PERI_QAXI_AO_BUS_SUB2_u_Ink_PERI_QAXI_AO_BUS_SUB2_SI18B_to_DEVICE_APC_FMEM_AO_APB_S_ASYNC control register 0
1A050008	<u>PERI_QAXI_AO_BUS_SUB2_u_SI18B_CTRL_0</u>	32	PERI_QAXI_AO_BUS_SUB2_u_SI18B control register 0

1A050000

PERI_QAXI_AO_BUS_SUB2_u_Ink_PERI_QAXI_A
 _Ink_PERI_QAXI_AO_BUS_SUB2_SI18B_to_DEBUG_CTRL_FMEM_A
 B2_SI18B_to_DEBUG_CTRL_FMEM_AO_APB_S_ASYNC control register 0
 MEM_AO_APB_S_ASYNC_CTRL_0

00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_QAXI_AO_BUS_SUB2_u_Ink_PERI_QAXI_AO_BUS_SUB2_SI18B_to_DEBUG_CTRL_FMEM_AO_APB_S_ASYNC_rx_clock_en	PERI_QAXI_AO_BUS_SUB2_SI18B_to_DEBUG_CTRL_FMEM_AO_APB_S_ASYNC_error_flag_en
Type															RW	RW
Reset															1	1

Bit(s)	Name	Description
1	PERI_QAXI_AO_BUS_SUB2_u_Ink_PERI_QAXI_AO_BUS_SUB2_SI18B_to_DEBUG_CTRL_FMEM_AO_APB_S_ASYNC_rx_clock_en	
0	PERI_QAXI_AO_BUS_SUB2_u_Ink_PERI_QAXI_AO_BUS_SUB2_SI18B_to_DEBUG_CTRL_FMEM_AO_APB_S_ASYNC_error_flag_en	Enables error flag. Controls time-out counter

1A050004 PERI_QAXI_AO_BUS_SUB2_u_Ink_PERI_QAXI_A 00000003
 _Ink_PERI_QAXI_AO_BUS_SUB2_SI18B_to_DEVICE_APC_FMEM_AO
 B2_SI18B_to_DEVICE_APC_F_APB_S_ASYNC control register 0
 MEM_AO_APB_S_ASYNC_CTL
 RL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_QAXI_AO_BUS_SUB2_u_Ink_PERI_QAXI_AO_BUS_SUB2_SI18B_to_DEVICE_APC_FMEM_AO_APB_S_ASYNC_CTL_rx_clock_cg_en	PERI_QAXI_AO_BUS_SUB2_u_Ink_PERI_QAXI_AO_BUS_SUB2_SI18B_to_DEVICE_APC_FMEM_AO_APB_S_ASYNC_CTL_rx_clock_cg_en
Type															RW	RW
Reset															1	1

Bit(s)	Name	Description
1	PERI_QAXI_AO_BUS_SUB2_u_Ink_PERI_QAXI_AO_BUS_SUB2_SI18B_to_DEVICE_APC_FMEM_AO_APB_S_ASYNC__rx_clock_cg_en	
0	PERI_QAXI_AO_BUS_SUB2_u_Ink_PERI_QAXI_AO_BUS_SUB2_SI18B_to_DEVICE_APC_FMEM_AO_APB_S_ASYNC__error_flag_en	Enables error flag. Controls time-out counter

1A050008

PERI_QAXI_AO_BUS_SUB2_u PERI_QAXI_AO_BUS_SUB2_u_SI18B control
SI18B_CTRL_0 register 0

017F00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								PERI_QAXI_AO_BUS_SUB2_u_SI18B_enable_slv_err_resp	PERI_QAXI_AO_BUS_SUB2_u_SI18B_ctrl_bypass	PERI_QAXI_AO_BUS_SUB2_u_SI18B_way_en						
Type								RW	RW	RW						
Reset								1	0	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_AO_BUS_SUB2_u_SI18B_ctrl_update_status	PERI_QAXI_AO_BUS_SUB2_u_SI18B_force_pready_high							PERI_QAXI_AO_BUS_SUB2_u_SI18B_way_en_ready							PERI_QAXI_AO_BUS_SUB2_u_SI18B_s2p_idle
Type	RO	RW							RO							RO
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
24	PERI_QAXI_AO_BUS_SUB2_u_SI18B_enable_slv_err_resp	
23	PERI_QAXI_AO_BUS_SUB2_u_SI18B_ctrl_bypass	
22:16	PERI_QAXI_AO_BUS_SUB2_u_SI18B_way_en	
15	PERI_QAXI_AO_BUS_SUB2_u_SI18B_ctrl_update_status	
14:8	PERI_QAXI_AO_BUS_SUB2_u_SI18B_force_pready_high	
7:1	PERI_QAXI_AO_BUS_SUB2_u_SI18B_way_en_ready	
0	PERI_QAXI_AO_BUS_SUB2_u_SI18B_s2p_idle	Idle signal (Synchronous to Input Clock Domain)

Module name: bcrm_PERI_PAR_AO_wrapper_u_bcrm_PERI_PAR_AO_bcrm Base address: (+0x1A06_0000)

Address	Name	Width	Register Function
1A060000	<u>PERI_PAR_QAXI_AO_BUS_u_S</u> <u>I18C_CTRL_0</u>	32	PERI_PAR_QAXI_AO_BUS_u_SI18C control register 0

1A060000 PERI_PAR_QAXI_AO_BUS_u_PERI_PAR_QAXI_AO_BUS_u_SI18C control
SI18C_CTRL_0 register 0

000017F8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PERI_P AR_QAXI_AO_ BUS_u_SI18 C_ena ble_slv_ err_res p	PERI_P AR_QAXI_AO_ BUS_u_SI18 C_ctrl_ bypass s	PERI_P AR_QAXI_AO_ BUS_u_SI18 C_ctrl_ update_ status	PERI_PAR_QAXI_AO_B US_u_SI18C_way_en			PERI_PAR_QAXI_AO_B US_u_SI18C_way_en _ready			PERI_P AR_QAXI_AO_ BUS_u_SI18 C_s2p_ idle	PERI_PAR_QAXI_AO_B US_u_SI18C_force_p ready_high		
Type				RW	RW	RO	RW			RO			RO	RW		
Reset				1	0	1	1	1	1	1	1	1	1	0	0	0

Bit(s)	Name	Description
12	PERI_PAR_QAXI_AO_BUS_u_SI18C_en able_slv_err_resp	
11	PERI_PAR_QAXI_AO_BUS_u_SI18C_ct rl_bypass	
10	PERI_PAR_QAXI_AO_BUS_u_SI18C_ct rl_update_status	
9:7	PERI_PAR_QAXI_AO_BUS_u_SI18C_w ay_en	
6:4	PERI_PAR_QAXI_AO_BUS_u_SI18C_w ay_en_ready	
3	PERI_PAR_QAXI_AO_BUS_u_SI18C_s2 p_idle	Idle signal (Synchronous to Input Clock Domain)
2:0	PERI_PAR_QAXI_AO_BUS_u_SI18C_fo rce_pready_high	

Module name: bcrm_PERI_PAR_PDN_wrapper_u_bcrm_PERI_PAR_PDN_bcrm Base address: (+0x1A07_0000)

Address	Name	Width	Register Function
1A070000	<u>PERI PAR QAXI BUS u Ink P</u> <u>ERI PAR QAXI BUS SI22 to</u> <u>MSDC0 S S2F CTRL 0</u>	32	PERI_PAR_QAXI_BUS_u_Ink_PERI_PAR_QAXI_BUS_SI22_to_MSDC0_S_S2F control register 0
1A070004	<u>PERI PAR QAXI BUS u Ink P</u> <u>ERI PAR QAXI BUS SI15 to</u> <u>AUXADC APB S ASYNC CTRL</u> <u>_0</u>	32	PERI_PAR_QAXI_BUS_u_Ink_PERI_PAR_QAXI_BUS_SI15_to_AUXADC_APB_S_ASYNC control register 0
1A070008	<u>PERI PAR QAXI BUS u SI22</u> <u>CTRL 0</u>	32	PERI_PAR_QAXI_BUS_u_SI22 control register 0
1A07000C	<u>PERI PAR QAXI BUS u SI15</u> <u>CTRL 0</u>	32	PERI_PAR_QAXI_BUS_u_SI15 control register 0
1A070010	<u>PERI PAR QAXI BUS u SI15</u> <u>CTRL 1</u>	32	PERI_PAR_QAXI_BUS_u_SI15 control register 1
1A070014	<u>PERI PAR QAXI BUS u SI15</u> <u>CTRL 2</u>	32	PERI_PAR_QAXI_BUS_u_SI15 control register 2
1A070018	<u>PERI PAR FAXI BUS u Ink I</u> <u>NFRA FAXI BUS MISIOC to</u> <u>PERI PAR FAXI BUS SL45 D</u> <u>CM PROT ups CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL45_DCM_PROT_ups control register 0
1A07001C	<u>PERI PAR FAXI BUS u Ink I</u> <u>NFRA FAXI BUS MISIOC to</u> <u>PERI PAR FAXI BUS SL45 D</u> <u>CM PROT CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL45_DCM_PROT control register 0
1A070020	<u>PERI PAR FAXI BUS u Ink I</u> <u>NFRA FAXI BUS MISIOC to</u> <u>PERI PAR FAXI BUS SL46 D</u> <u>CM PROT ups CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL46_DCM_PROT_ups control register 0
1A070024	<u>PERI PAR FAXI BUS u Ink I</u> <u>NFRA FAXI BUS MISIOC to</u> <u>PERI PAR FAXI BUS SL46 D</u> <u>CM PROT CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL46_DCM_PROT control register 0
1A070028	<u>PERI PAR FAXI BUS u Ink I</u> <u>NFRA FAXI BUS MISIOC to</u> <u>PERI PAR FAXI BUS SL47 D</u> <u>CM PROT ups CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL47_DCM_PROT_ups control register 0
1A07002C	<u>PERI PAR FAXI BUS u Ink I</u> <u>NFRA FAXI BUS MISIOC to</u> <u>PERI PAR FAXI BUS SL47 D</u> <u>CM PROT CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL47_DCM_PROT control register 0
1A070030	<u>PERI PAR FAXI BUS u Ink I</u> <u>NFRA FAXI BUS MISIOC to</u> <u>PERI PAR FAXI BUS SL48 D</u> <u>CM PROT ups CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL48_DCM_PROT_ups control register 0
1A070034	<u>PERI PAR FAXI BUS u Ink I</u> <u>NFRA FAXI BUS MISIOC to</u> <u>PERI PAR FAXI BUS SL48 D</u> <u>CM PROT CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL48_DCM_PROT control register 0
1A070038	<u>PERI PAR FAXI BUS u Ink E</u> <u>MI L2C M to PERI PAR FAX</u> <u>I BUS MI14 ASYNC CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC control register 0
1A07003C	<u>PERI PAR FAXI BUS u Ink S</u> <u>PIO M to PERI PAR FAXI B</u> <u>US MI11 AHB M QOS REPL</u> <u>ACE CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_Ink_SPIO_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE control register 0

Address	Name	Width	Register Function
1A070040	<u>PERI PAR FAXI BUS u Ink SPI1 M to PERI PAR FAXI BUS MI11 AHB M QOS REPLACE CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_Ink_SPI1_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE control register 0
1A070044	<u>PERI PAR FAXI BUS u Ink SPI2 M to PERI PAR FAXI BUS MI11 AHB M QOS REPLACE CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_Ink_SPI2_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE control register 0
1A070048	<u>PERI PAR FAXI BUS u Ink PERI PAR FAXI BUS MI11 to PERI PAR FAXI BUS MI14 DCM PROT CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_MI11_to_PERI_PAR_FAXI_BUS_MI14_DCM_PROT control register 0
1A07004C	<u>PERI PAR FAXI BUS u Ink PERI PAR FAXI BUS MI11 to PERI PAR FAXI BUS MI14 AHB S2AXI CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_MI11_to_PERI_PAR_FAXI_BUS_MI14_AHB_S2AXI control register 0
1A070050	<u>PERI PAR FAXI BUS u Ink NFI M to PERI PAR FAXI BUS MI11 AHB M QOS REPLACE CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_Ink_NFI_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE control register 0
1A070054	<u>PERI PAR FAXI BUS u Ink THERM M to PERI PAR FAXI BUS MI11 AHB M QOS REPLACE CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_Ink_THERM_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE control register 0
1A070058	<u>PERI PAR FAXI BUS u MI14 CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_MI14 control register 0
1A07005C	<u>PERI PAR FAXI BUS u SL20 CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_SL20 control register 0
1A070060	<u>PERI PAR FAXI BUS u SL45 CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_SL45 control register 0
1A070064	<u>PERI PAR FAXI BUS u SL46 CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_SL46 control register 0
1A070068	<u>PERI PAR FAXI BUS u SL47 CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_SL47 control register 0
1A07006C	<u>PERI PAR FAXI BUS u SL48 CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_SL48 control register 0
1A070070	<u>PERI PAR FAXI BUS u MISI4A CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_MISI4A control register 0
1A070074	<u>PERI PAR FAXI BUS u ASL40 CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_ASL40 control register 0
1A070078	<u>PERI PAR FAXI BUS u MISI7B CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_MISI7B control register 0
1A07007C	<u>PERI PAR FAXI BUS u MISI5A CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_MISI5A control register 0
1A070080	<u>PERI PAR FAXI BUS u ASL41 CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_ASL41 control register 0
1A070084	<u>PERI PAR FAXI BUS u MISI6A CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_MISI6A control register 0
1A070088	<u>PERI PAR FAXI BUS u ASL42 CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_ASL42 control register 0
1A07008C	<u>PERI PAR FAXI BUS u MISI7A CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_MISI7A control register 0
1A070090	<u>PERI PAR FAXI BUS u ASL43 CTRL 0</u>	32	PERI_PAR_FAXI_BUS_u_ASL43 control register 0

Address	Name	Width	Register Function
1A070094	<u>PERI_PAR_FAXI_BUS_u_MI11_CTRL_0</u>	32	PERI_PAR_FAXI_BUS_u_MI11 control register 0
1A070098	<u>PERI_PAR_FAXI_BUS_u_MI11_CTRL_1</u>	32	PERI_PAR_FAXI_BUS_u_MI11 control register 1

1A070000 PERI_PAR_QAXI_BUS_u_Ink_PERI_PAR_QAXI_BUS_u_Ink_PERI_PAR_QAXI_B 00000020
 PERI_PAR_QAXI_BUS_SI22_toUS_SI22_to_MSDC0_S_S2F control register 0
 MSDC0_S_S2F_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											PERI_P AR_QA XI_BUS __u_In k_PERI _PAR_ QAXI_B US_SI2 2_to_ MSDC0 _S_S2F __err_f lag_en	PERI_PAR_QAX I_BUS__u_Ink_ PERI_PAR_QAX I_BUS_SI22_to _ahb_flush_th re	PERI_PAR_QAX I_BUS__u_Ink_ PERI_PAR_QAX I_BUS_SI22_to _RG_FIFO_TH RE			PERI_P AR_QA XI_BUS __u_In k_PERI _PAR_ QAXI_ BUS_SI 22_to_ MSDC0 _S_S2F __post write_ dis
Type											RW	RW		RW		RW
Reset											1	0	0	0	0	0

Bit(s)	Name	Description
5	PERI_PAR_QAXI_BUS__u_Ink_PERI_PAR_QAXI_BUS_SI22_to_MSDC0_S_S2F__err_flag_en	
4:3	PERI_PAR_QAXI_BUS__u_Ink_PERI_PAR_QAXI_BUS_SI22_to_MSDC0_S_S2F__ahb_flush_thre	
2:1	PERI_PAR_QAXI_BUS__u_Ink_PERI_PAR_QAXI_BUS_SI22_to_MSDC0_S_S2F__RG_FIFO_THRE	
0	PERI_PAR_QAXI_BUS__u_Ink_PERI_PAR_QAXI_BUS_SI22_to_MSDC0_S_S2F__postwrite_dis	

1A070004 PERI_PAR_QAXI_BUS_u_Ink_PERI_PAR_QAXI_BUS_u_Ink_PERI_PAR_QAXI_B 00000003
 PERI_PAR_QAXI_BUS_SI15_toUS_SI15_to_AUXADC_APB_S_ASYNC control
 AUXADC_APB_S_ASYNC_CT register 0
 RL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_P AR_QAXI BUS_u_In k_PERI _PAR_ QAXI_B US_SI15 to_AUX ADC_APB S_ASYNC C_rx_c lock_c g_en	PERI_P AR_QAXI BUS_u_In k_PERI _PAR_ QAXI_B US_SI15 to_AUX ADC_APB S_ASYNC C_rx_c lock_c g_en
Type															RW	RW
Reset															1	1

Bit(s)	Name	Description
1	PERI_PAR_QAXI_BUS_u_Ink_PERI_PAR_QAXI_BUS_SI15_to_AUXADC_APB_S_ASYNC_rx_clock_cg_en	
0	PERI_PAR_QAXI_BUS_u_Ink_PERI_PAR_QAXI_BUS_SI15_to_AUXADC_APB_S_ASYNC_error_flag_en	Enables error flag. Controls time-out counter

1A070008

PERI_PAR_QAXI_BUS_u_SI22 PERI_PAR_QAXI_BUS_u_SI22 control register 0

0000007F

CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										PERI_P AR_QA XI_BUS __u_SI 22__er ror fla g_en	PERI_PAR_QAXI_BUS__u_SI22__reg_sl ave_way_en					PERI_P AR_QA XI_BUS __u_SI 22__ctr l_upda te_stat us
Type										RW	RW					RO
Reset										1	1	1	1	1	1	1

Bit(s)	Name	Description
6	PERI_PAR_QAXI_BUS__u_SI22__error_flag_en	
5:1	PERI_PAR_QAXI_BUS__u_SI22__reg_slave_way_en	
0	PERI_PAR_QAXI_BUS__u_SI22__ctrl_update_status	

1A07000C PERI_PAR_QAXI_BUS_u_SI15 PERI_PAR_QAXI_BUS_u_SI15 control register 0 0007FFFF
CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														PERI_PAR_QAXI_BUS_u_SI15_way_en_ready		
Type														RO		
Reset														1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_PAR_QAXI_BUS_u_SI15_way_en_ready														PERI_PAR_QAXI_BUS_u_SI15_s2p_idle	
Type	RO														RO	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
18:1	PERI_PAR_QAXI_BUS_u_SI15_way_en_ready	
0	PERI_PAR_QAXI_BUS_u_SI15_s2p_idle	Idle signal (Synchronous to Input Clock Domain)

1A070010 PERI_PAR_QAXI_BUS_u_S115 PERI_PAR_QAXI_BUS_u_S115 control register 1

00040000

CTRL_1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														PERI_P AR_QAXI_BUS __u_S115__ctrl_updat e_status	PERI_PAR_QAXI_BUS__u_S115__force_pread y_high	
Type														RO	RW	
Reset														1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_PAR_QAXI_BUS__u_S115__force_pready_high															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18	PERI_PAR_QAXI_BUS__u_S115__ctrl_up date_status	
17:0	PERI_PAR_QAXI_BUS__u_S115__force_p ready_high	

1A070014 PERI_PAR_QAXI_BUS_u_SI15 PERI_PAR_QAXI_BUS_u_SI15 control register 2
CTRL_2

000BFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													PERI_P AR_QAXI_BUS __u_SI15__enable_slv_err_resp	PERI_P AR_QAXI_BUS __u_SI15__ctrl_bypass	PERI_PAR_QAXI_BUS__u_SI15__way_en	
Type													RW	RW	RW	
Reset													1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_PAR_QAXI_BUS__u_SI15__way_en															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
19	PERI_PAR_QAXI_BUS__u_SI15__enable_slv_err_resp	
18	PERI_PAR_QAXI_BUS__u_SI15__ctrl_bypass	
17:0	PERI_PAR_QAXI_BUS__u_SI15__way_en	

1A070018 PERI_PAR_FAXI_BUS_u_Ink_I PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_M 00000000
 NFRA_FAXI_BUS_MISIOC_to_ISIOC_to_PERI_PAR_FAXI_BUS_SL45_DCM_PROT
 PERI_PAR_FAXI_BUS_SL45_D_ups control register 0
 CM_PROT_ups_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_P AR_FA XI_BUS _u_In k_INFR A_FAXI _BUS_ MISIOC _to_PE RI_PAR _FAXI_ BUS_SL 45_DC M_PRO T_ups_ _axi_cl ock_ga ted_en	PERI_P AR_FA XI_BUS _u_In k_INFR A_FAXI _BUS_ MISIOC _to_PE RI_PAR _FAXI_ BUS_SL 45_DC M_PR OT_up s_axi clock_g ated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL45_DCM_PROT_ups_axi_clock_gated_en	
0	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL45_DCM_PROT_ups_axi_clock_gated	

1A07001C PERI_PAR_FAXI_BUS_u_Ink_I PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_M 00000000
 NFRA_FAXI_BUS_MISIOC_to_ISIOC_to_PERI_PAR_FAXI_BUS_SL45_DCM_PROT
 PERI_PAR_FAXI_BUS_SL45_D control register 0
 CM_PROT_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_P AR_FA XI_BUS _u_In k_INFR A_FAXI _BUS_ MISIOC _to_PE RI_PAR _FAXI_ BUS_SL 45_DC M_PRO T_axi clock_g ated_e n	PERI_P AR_FA XI_BUS _u_In k_INFR A_FAXI _BUS_ MISIOC _to_PE RI_PAR _FAXI_ BUS_SL 45_DC M_PR OT_ax i_clock _gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL45_DCM_PROT_axi_clock_gated_en	
0	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL45_DCM_PROT_axi_clock_gated	

1A070020 PERI_PAR_FAXI_BUS_u_Ink_I PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_M 00000000
 NFRA_FAXI_BUS_MISIOC_to_ISIOC_to_PERI_PAR_FAXI_BUS_SL46_DCM_PROT
 PERI_PAR_FAXI_BUS_SL46_D_ups control register 0
 CM_PROT_ups_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_P AR_FA XI_BUS _u_In k_INFR A_FAXI _BUS_ MISIOC _to_PE RI_PAR _FAXI_ BUS_SL 46_DC M_PRO T_ups_ _axi_cl ock_ga ted_en	PERI_P AR_FA XI_BUS _u_In k_INFR A_FAXI _BUS_ MISIOC _to_PE RI_PAR _FAXI_ BUS_SL 46_DC M_PR OT_up s_axi clock_g ated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL46_DCM_PROT_ups_axi_clock_gated_en	
0	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL46_DCM_PROT_ups_axi_clock_gated	

1A070024 PERI_PAR_FAXI_BUS_u_Ink_I PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_M 00000000
 NFRA_FAXI_BUS_MISIOC_to_ISIOC_to_PERI_PAR_FAXI_BUS_SL46_DCM_PROT
 PERI_PAR_FAXI_BUS_SL46_D control register 0
 CM_PROT_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_P AR_FA XI_BUS _u_In k_INFR A_FAXI _BUS_ MISIOC _to_PE RI_PAR _FAXI_ BUS_SL 46_DC M_PRO T_axi clock_g ated_e n	PERI_P AR_FA XI_BUS _u_In k_INFR A_FAXI _BUS_ MISIOC _to_PE RI_PAR _FAXI_ BUS_SL 46_DC M_PR OT_ax i_clock _gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL46_DCM_PROT_axi_clock_gated_en	
0	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL46_DCM_PROT_axi_clock_gated	

1A070028 PERI_PAR_FAXI_BUS_u_Ink_I PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_M 00000000
 NFRA_FAXI_BUS_MISIOC_to_ISIOC_to_PERI_PAR_FAXI_BUS_SL47_DCM_PROT
 PERI_PAR_FAXI_BUS_SL47_D_ups control register 0
 CM_PROT_ups_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_P AR_FA XI_BUS _u_In k_INFR A_FAXI _BUS_ MISIOC _to_PE RI_PAR _FAXI_ BUS_SL 47_DC M_PRO T_ups_ _axi_cl ock_ga ted_en	PERI_P AR_FA XI_BUS _u_In k_INFR A_FAXI _BUS_ MISIOC _to_PE RI_PAR _FAXI_ BUS_SL 47_DC M_PR OT_up s_axi clock_g ated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL47_DCM_PROT_ups_axi_clock_gated_en	
0	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL47_DCM_PROT_ups_axi_clock_gated	

1A07002C PERI_PAR_FAXI_BUS_u_Ink_I PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_M 00000000
 NFRA_FAXI_BUS_MISIOC_to_ISIOC_to_PERI_PAR_FAXI_BUS_SL47_DCM_PROT
 PERI_PAR_FAXI_BUS_SL47_D control register 0
 CM_PROT_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_P AR_FA XI_BUS _u_In k_INFR A_FAXI _BUS_ MISIOC _to_PE RI_PAR _FAXI_ BUS_SL 47_DC M_PRO T_axi clock_g ated_e n	PERI_P AR_FA XI_BUS _u_In k_INFR A_FAXI _BUS_ MISIOC _to_PE RI_PAR _FAXI_ BUS_SL 47_DC M_PR OT_ax i_clock _gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL47_DCM_PROT_axi_clock_gated_en	
0	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL47_DCM_PROT_axi_clock_gated	

1A070030 PERI_PAR_FAXI_BUS_u_Ink_I PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_M 00000000
 NFRA_FAXI_BUS_MISIOC_to_ISIOC_to_PERI_PAR_FAXI_BUS_SL48_DCM_PROT
 PERI_PAR_FAXI_BUS_SL48_D_ups control register 0
 CM_PROT_ups_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_P AR_FA XI_BUS _u_In k_INFR A_FAXI _BUS_ MISIOC _to_PE RI_PAR _FAXI_ BUS_SL 48_DC M_PRO T_ups_ _axi_cl ock_ga ted_en	PERI_P AR_FA XI_BUS _u_In k_INFR A_FAXI _BUS_ MISIOC _to_PE RI_PAR _FAXI_ BUS_SL 48_DC M_PR OT_up s_axi clock_g ated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL48_DCM_PROT_ups_axi_clock_gated_en	
0	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL48_DCM_PROT_ups_axi_clock_gated	

1A070034 PERI_PAR_FAXI_BUS_u_Ink_I PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_M 00000000
 NFRA_FAXI_BUS_MISIOC_to_ISIOC_to_PERI_PAR_FAXI_BUS_SL48_DCM_PROT
 PERI_PAR_FAXI_BUS_SL48_D control register 0
 CM_PROT_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_P AR_FA XI_BUS _u_In k_INFR A_FAXI _BUS_ MISIOC _to_PE RI_PAR _FAXI_ BUS_SL 48_DC M_PRO T_axi clock_g ated_e n	PERI_P AR_FA XI_BUS _u_In k_INFR A_FAXI _BUS_ MISIOC _to_PE RI_PAR _FAXI_ BUS_SL 48_DC M_PR OT_ax i_clock _gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL48_DCM_PROT_axi_clock_gated_en	
0	PERI_PAR_FAXI_BUS_u_Ink_INFRA_FAXI_BUS_MISIOC_to_PERI_PAR_FAXI_BUS_SL48_DCM_PROT_axi_clock_gated	

1A070038 PERI_PAR_FAXI_BUS_u_Ink_EPERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PER MI_L2C_M_to_PERI_PAR_FAXI_PAR_FAXI_BUS_MI14_ASYNC control register 0 000000FB
 XI_BUS_MI14_ASYNC_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC_mst_sync_sel	PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC_slv_sync_sel	PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC_in_arflush_thre	PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC_in_awflush_thre	PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC_sample_sel	PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC_sync_mode	PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC_axi_idle_out	PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC_axi_idle_out_reg				
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RO	RO
Reset					0	0	0	0	1	1	1	1	1	0	1	1

Bit(s)	Name	Description
11:10	PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC_mst_sync_sel	
9:8	PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC_slv_sync_sel	
7:6	PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC_in_arflush_thre	
5:4	PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC_in_awflush_thre	
3	PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC_sample_sel	
2	PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC_sync_mode	Sync mode switch for ASLICE
1	PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC_axi_idle_out	
0	PERI_PAR_FAXI_BUS_u_Ink_EMI_L2C_M_to_PERI_PAR_FAXI_BUS_MI14_ASYNC_axi_idle_out_reg	

Bit(s)	Name	Description

1A07003C PERI_PAR_FAXI_BUS_u_Ink_SPI0_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE
 US_MI11_AHB_M_QOS_REPL control register 0
 ACE_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PERI_PAR_FAXI_BUS_u_Ink_SPI0_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE_reg_flush	PERI_PAR_FAXI_BUS_u_Ink_SPI0_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE_reg_ultra		
Type													RW		RW	
Reset													0	0	0	0

Bit(s)	Name	Description
3:2	PERI_PAR_FAXI_BUS_u_Ink_SPI0_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE_reg_flush	This is to replace AHBM Flush QoS for SPI0_M
1:0	PERI_PAR_FAXI_BUS_u_Ink_SPI0_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE_reg_ultra	This is to replace AHBM Ultra QoS for SPI0_M

1A070040 PERI_PAR_FAXI_BUS_u_Ink_SPI1_M_to_PERI_PA 00000000
 PI1_M_to_PERI_PAR_FAXI_B_R_FAXI_BUS_MI11_AHB_M_QOS_REPLACE
 US_MI11_AHB_M_QOS_REPL control register 0
 ACE_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PERI_PAR_FAXI BUS_u_Ink_S PI1_M_to_PERI _PAR_FAXI_BU S_MI11_AHB_ M_QOS_REPLA CE_reg_flush	PERI_PAR_FAXI BUS_u_Ink_S PI1_M_to_PERI _PAR_FAXI_BU S_MI11_AHB_ M_QOS_REPLA CE_reg_ultra		
Type														RW	RW	
Reset													0	0	0	0

Bit(s)	Name	Description
3:2	PERI_PAR_FAXI_BUS_u_Ink_SPI1_M_to _PERI_PAR_FAXI_BUS_MI11_AHB_M_Q OS_REPLACE__reg_flush	This is to replace AHBM Flush QoS for SPI1_M
1:0	PERI_PAR_FAXI_BUS_u_Ink_SPI1_M_to _PERI_PAR_FAXI_BUS_MI11_AHB_M_Q OS_REPLACE__reg_ultra	This is to replace AHBM Ultra QoS for SPI1_M

1A070044 PERI_PAR_FAXI_BUS_u_Ink_SPI2_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE
 US_MI11_AHB_M_QOS_REPLACE control register 0
 ACE_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PERI_PAR_FAXI_BUS_u_Ink_SPI2_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE_reg_flush	PERI_PAR_FAXI_BUS_u_Ink_SPI2_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE_reg_ultra		
Type													RW		RW	
Reset													0	0	0	0

Bit(s)	Name	Description
3:2	PERI_PAR_FAXI_BUS_u_Ink_SPI2_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE_reg_flush	This is to replace AHBM Flush QoS for SPI2_M
1:0	PERI_PAR_FAXI_BUS_u_Ink_SPI2_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE_reg_ultra	This is to replace AHBM Ultra QoS for SPI2_M

1A070048 PERI_PAR_FAXI_BUS_u_Ink_PPERI_PAR_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BU 00000001
 ERI_PAR_FAXI_BUS_MI11_to_S_MI11_to_PERI_PAR_FAXI_BUS_MI14_DCM_PR
 PERI_PAR_FAXI_BUS_MI14_OT control register 0
 DCM_PROT_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PERI_P AR_FA XI_BUS _u_In k_PERI _PAR_F AXI_BU S_MI11 _to_PE RI_PAR _FAXI_ BUS_M I14_DC M_PRO T_rg_ monito r_mod e	PERI_P AR_FA XI_BUS _u_In k_PERI _PAR_F AXI_BU S_MI11 _to_PE RI_PAR _FAXI_ BUS_M I14_DC M_PRO T_rg_ monito r_mod e	PERI_P AR_FA XI_BUS _u_In k_PERI _PAR_F AXI_BU S_MI11 _to_PE RI_PAR _FAXI_ BUS_M I14_DC M_PRO T_rg_ monito r_mod e
Type														RW	RW	RW
Reset														0	0	1

Bit(s)	Name	Description
2	PERI_PAR_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_MI11_to_PERI_PAR_FAXI_BUS_MI14_DCM_PROT_rg_monitor_mode	
1	PERI_PAR_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_MI11_to_PERI_PAR_FAXI_BUS_MI14_DCM_PROT_rg_cmd_cnt_clr	
0	PERI_PAR_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_MI11_to_PERI_PAR_FAXI_BUS_MI14_DCM_PROT_error_flag_en	

1A07004C PERI_PAR_FAXI_BUS_u_Ink_PPERI_PAR_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BU 000000F8
 ERI_PAR_FAXI_BUS_MI11_to_S_MI11_to_PERI_PAR_FAXI_BUS_MI14_AHB_S2
 PERI_PAR_FAXI_BUS_MI14_AXI control register 0
 AHB_S2AXI_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							PERI_PAR_FAXI_BUS_u_Ink_P	PERI_PAR_FAXI_BUS_MI11_to_S_MI11	PERI_PAR_FAXI_BUS_MI14_AHB_S2AXI_hflush_thres	PERI_PAR_FAXI_BUS_MI11_to_S_MI11	PERI_PAR_FAXI_BUS_MI11_to_S_MI11	PERI_PAR_FAXI_BUS_MI11_to_S_MI11	PERI_PAR_FAXI_BUS_MI11_to_S_MI11	PERI_PAR_FAXI_BUS_MI11_to_S_MI11	PERI_PAR_FAXI_BUS_MI11_to_S_MI11	PERI_PAR_FAXI_BUS_MI11_to_S_MI11
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	1	1	1	1	1	0	0	0

Bit(s)	Name	Description
9:8	PERI_PAR_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_MI11_to_PERI_PAR_FAXI_BUS_MI14_AHB_S2AXI_hflush_thres	
7	PERI_PAR_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_MI11_to_PERI_PAR_FAXI_BUS_MI14_AHB_S2AXI_hsecur_en	
6	PERI_PAR_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_MI11_to_PERI_PAR_FAXI_BUS_MI14_AHB_S2AXI_hbstrb_en	
5	PERI_PAR_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_MI11_to_PERI_PAR_FAXI_BUS_MI14_AHB_S2AXI_buffer_en	
4	PERI_PAR_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_MI11_to_PERI_PAR_FAXI_BUS_MI14_AHB_S2AXI_merge_en	
3:1	PERI_PAR_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_MI11_to_PERI_PAR_FAXI_BUS_MI14_AHB_S2AXI_fifo_threshold	
0	PERI_PAR_FAXI_BUS_u_Ink_PERI_PAR_FAXI_BUS_MI11_to_PERI_PAR_FAXI_BUS_MI14_AHB_S2AXI_read_ahead_bw	

Bit(s)	Name	Description

1A070050 PERI_PAR_FAXI_BUS_u_Ink_NFI_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE 00000000
US_MI11_AHB_M_QOS_REPLACE control register 0
ACE_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PERI_PAR_FAXI_BUS_u_Ink_NFI_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE_reg_flush	PERI_PAR_FAXI_BUS_u_Ink_NFI_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE_reg_ultra		
Type													RW		RW	
Reset													0	0	0	0

Bit(s)	Name	Description
3:2	PERI_PAR_FAXI_BUS_u_Ink_NFI_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE_reg_flush	This is to replace AHBM Flush QoS for NFI_M
1:0	PERI_PAR_FAXI_BUS_u_Ink_NFI_M_to_PERI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE_reg_ultra	This is to replace AHBM Ultra QoS for NFI_M

1A070054 PERI_PAR_FAXI_BUS_u_Ink_TPERI_PAR_FAXI_BUS_u_Ink_THERM_M_to_PERI
 HERM_M_to_PERI_PAR_FAXI_PAR_FAXI_BUS_MI11_AHB_M_QOS_REPLACE
 BUS_MI11_AHB_M_QOS_REPLACE control register 0
 PLACE_CTRL_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PERI_PAR_FAXI _BUS_u_Ink_T HERM_M_to_P ERI_PAR_FAXI BUS_MI11_AH B_M_QOS_REP LACE_reg_flush	PERI_PAR_FAXI _BUS_u_Ink_ THERM_M_to_ PERI_PAR_FAXI _BUS_MI11_A HB_M_QOS_RE PLACE_reg_ul		
Type													RW	RW		
Reset													0	0	0	0

Bit(s)	Name	Description
3:2	PERI_PAR_FAXI_BUS__u_Ink_THERM_M _to_PERI_PAR_FAXI_BUS_MI11_AHB_M _QOS_REPLACE__reg_flush	This is to replace AHBM Flush QoS for THERM_M
1:0	PERI_PAR_FAXI_BUS__u_Ink_THERM_M _to_PERI_PAR_FAXI_BUS_MI11_AHB_M _QOS_REPLACE__reg_ultra	This is to replace AHBM Ultra QoS for THERM_M

1A070058

PERI_PAR_FAXI_BUS_u_MI14 PERI_PAR_FAXI_BUS_u_MI14 control register 0

0000001C

CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											PERI_P AR_FAXI_BUS_u_MI14_cg_disable	PERI_P AR_FAXI_BUS_u_MI14_PERI_P AR_FAXI_BUS_u_MI14_mi_outstanding_extend_en	PERI_P AR_FAXI_BUS_u_MI14_PERI_P AR_FAXI_BUS_u_MI14_mi_qos_on	PERI_P AR_FAXI_BUS_u_MI14_PERI_P AR_FAXI_BUS_u_MI14_mi_ctrl_updated	PERI_P AR_FAXI_BUS_u_MI14_PERI_P AR_FAXI_BUS_u_MI14_mi_r_busy	PERI_P AR_FAXI_BUS_u_MI14_PERI_P AR_FAXI_BUS_u_MI14_mi_w_busy
Type											RW	RW	RW	RO	RO	RO
Reset											0	1	1	1	0	0

Bit(s)	Name	Description
5	PERI_PAR_FAXI_BUS_u_MI14_cg_disable	
4	PERI_PAR_FAXI_BUS_u_MI14_PERI_P AR_FAXI_BUS_u_MI14_mi_outstanding_extend_en	
3	PERI_PAR_FAXI_BUS_u_MI14_PERI_P AR_FAXI_BUS_u_MI14_mi_qos_on	
2	PERI_PAR_FAXI_BUS_u_MI14_PERI_P PERI_PAR_FAXI_BUS_u_MI14_mi master interface control signal AR_FAXI_BUS_u_MI14_mi_ctrl_updated	updated status
1	PERI_PAR_FAXI_BUS_u_MI14_PERI_P PERI_PAR_FAXI_BUS_u_MI14_mi master interface read busy AR_FAXI_BUS_u_MI14_mi_r_busy	
0	PERI_PAR_FAXI_BUS_u_MI14_PERI_P PERI_PAR_FAXI_BUS_u_MI14_mi master interface write busy AR_FAXI_BUS_u_MI14_mi_w_busy	

1A07005C

PERI_PAR_FAXI_BUS_u_SL20 PERI_PAR_FAXI_BUS_u_SL20 control register 0
CTRL_0

0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PERI_PAR_FAXI_BUS_u_SL20__in_arflush_thre	PERI_PAR_FAXI_BUS_u_SL20__in_awflush_thre			PERI_PAR_FAXI_BUS_u_SL20__axi_idle_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	PERI_PAR_FAXI_BUS__u_SL20__in_arflush_thre	
2:1	PERI_PAR_FAXI_BUS__u_SL20__in_awflush_thre	
0	PERI_PAR_FAXI_BUS__u_SL20__axi_idle_out	

1A070060

PERI_PAR_FAXI_BUS_u_SL45 PERI_PAR_FAXI_BUS_u_SL45 control register 0
CTRL_0

0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PERI_PAR_FAXI_BUS_u_SL45__in_arflush_thre		PERI_PAR_FAXI_BUS_u_SL45__in_awflush_thre		PERI_PAR_FAXI_BUS_u_SL45__axi_idle_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	PERI_PAR_FAXI_BUS__u_SL45__in_arflush_thre	
2:1	PERI_PAR_FAXI_BUS__u_SL45__in_awflush_thre	
0	PERI_PAR_FAXI_BUS__u_SL45__axi_idle_out	

1A070064

PERI_PAR_FAXI_BUS_u_SL46 PERI_PAR_FAXI_BUS_u_SL46 control register 0

0000001F

CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PERI_PAR_FAXI_BUS_u_SL46__in_arflush_thre		PERI_PAR_FAXI_BUS_u_SL46__in_awflush_thre		PERI_PAR_FAXI_BUS_u_SL46__axi_idle_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	PERI_PAR_FAXI_BUS__u_SL46__in_arflush_thre	
2:1	PERI_PAR_FAXI_BUS__u_SL46__in_awflush_thre	
0	PERI_PAR_FAXI_BUS__u_SL46__axi_idle_out	

1A070068

PERI_PAR_FAXI_BUS_u_SL47 PERI_PAR_FAXI_BUS_u_SL47 control register 0

0000001F

CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PERI_PAR_FAXI_BUS_u_SL47__in_arflush_thre		PERI_PAR_FAXI_BUS_u_SL47__in_awflush_thre		PERI_PAR_FAXI_BUS_u_SL47__axi_idle_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	PERI_PAR_FAXI_BUS__u_SL47__in_arflush_thre	
2:1	PERI_PAR_FAXI_BUS__u_SL47__in_awflush_thre	
0	PERI_PAR_FAXI_BUS__u_SL47__axi_idle_out	

1A07006C

PERI_PAR_FAXI_BUS_u_SL48 PERI_PAR_FAXI_BUS_u_SL48 control register 0
CTRL_0

0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PERI_PAR_FAXI_BUS_u_SL48__in_arflush_thre		PERI_PAR_FAXI_BUS_u_SL48__in_awflush_thre		PERI_PAR_FAXI_BUS_u_SL48__axi_idle_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	PERI_PAR_FAXI_BUS__u_SL48__in_arflush_thre	
2:1	PERI_PAR_FAXI_BUS__u_SL48__in_awflush_thre	
0	PERI_PAR_FAXI_BUS__u_SL48__axi_idle_out	

1A070070 PERI_PAR_FAXI_BUS_u_MISI PERI_PAR_FAXI_BUS_u_MISI4A control register 0
4A_CTRL_0

0001E001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													PERI_P AR_FA XI_BUS u_MI SI4A PERI_P AR_FA XI_BUS u_MIS I4A_si ctrl_by pass	PERI_P AR_FA XI_BUS u_MI SI4A PERI_P AR_FA XI_BUS u_MIS I4A_si outstan ding_di sable	PERI_P AR_FA XI_BUS u_MI SI4A PERI_P AR_FA XI_BUS u_MIS I4A_si outstan ding_di sable	PERI_P AR_FA XI_BUS u_MI SI4A PERI_P AR_FA XI_BUS u_MIS I4A_si outstan ding_di sable
Type													RW	RW	RW	RW
Reset													0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_P AR_FA XI_BUS u_MI SI4A PERI_P AR_FA XI_BUS u_MI SI4A PERI_P AR_FA XI_BUS u_MIS I4A_si ctrl_by pass	PERI_PAR_FAXI_BUS_u_MISI4A_PERI_PAR_FAXI_BUS_u_MISI4A_si_way_interleave_en		PERI_P AR_FA XI_BUS u_MI SI4A PERI_P AR_FA XI_BUS u_MIS I4A_si dfsrlv set_wir q	PERI_P AR_FA XI_BUS u_MI SI4A PERI_P AR_FA XI_BUS u_MIS I4A_si dfsrlv set_wir q	PERI_PAR_FAXI_BUS_u_MISI4A_PERI_PAR_FAXI_BUS_u_MISI4A_si_b_chnl_sel			PERI_P AR_FA XI_BUS u_MI SI4A PERI_P AR_FA XI_BUS u_MIS I4A_si dfsrlv set_wir q	PERI_PAR_FAXI_BUS_u_MISI4A_PERI_PAR_FAXI_BUS_u_MISI4A_si_r_chnl_sel			PERI_P AR_FA XI_BUS u_MI SI4A PERI_P AR_FA XI_BUS u_MIS I4A_si dfsrlv set_wir q	PERI_P AR_FA XI_BUS u_MI SI4A PERI_P AR_FA XI_BUS u_MIS I4A_si dfsrlv set_wir q	PERI_P AR_FA XI_BUS u_MI SI4A PERI_P AR_FA XI_BUS u_MIS I4A_si dfsrlv set_wir q	PERI_P AR_FA XI_BUS u_MI SI4A PERI_P AR_FA XI_BUS u_MIS I4A_si dfsrlv set_wir q
Type	RW	RW		RO	RO	RO			RO	RO			RO	RO	RO	RO
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
19	PERI_PAR_FAXI_BUS_u_MISI4A_cg_disable	
18	PERI_PAR_FAXI_BUS_u_MISI4A_PERI_Par_FAXI_BUS_u_MISI4A_si_ctrl_bypass	Bypasses idle check when updating SI setting
17	PERI_PAR_FAXI_BUS_u_MISI4A_PERI_si_cabgen_slave_interface_outstanding_capability_disable_control	
16:15	PERI_PAR_FAXI_BUS_u_MISI4A_PERI_Par_FAXI_BUS_u_MISI4A_si_slave_interface_read_arbiter	
14:13	PERI_PAR_FAXI_BUS_u_MISI4A_PERI_Par_FAXI_BUS_u_MISI4A_si_way_interl	interleaving function enable control
12	PERI_PAR_FAXI_BUS_u_MISI4A_PERI_Par_FAXI_BUS_u_MISI4A_si_slave_interface_default_slave_write	
	PERI_PAR_FAXI_BUS_u_MISI4A_si_dfsrlv_set_IRQ status	
	wirq	

Bit(s)	Name	Description
11	PERI_PAR_FAXI_BUS__u_MISI4A__PERI_PAR_FAXI_BUS_u_MISI4A_si_slave_interface_default_slave_read_IRQ PAR_FAXI_BUS_u_MISI4A_si_dfslv_set_rstatus irq	
10:8	PERI_PAR_FAXI_BUS__u_MISI4A__PERI_PAR_FAXI_BUS_u_MISI4A_si_slave_interface_current_write PAR_FAXI_BUS_u_MISI4A_si_b_chnl_sel	response channel way selection
7	PERI_PAR_FAXI_BUS__u_MISI4A__PERI_PAR_FAXI_BUS_u_MISI4A_si_slave_interface_write_response_ID_is PAR_FAXI_BUS_u_MISI4A_si_set_bid_mimissed_status ss	
6:4	PERI_PAR_FAXI_BUS__u_MISI4A__PERI_PAR_FAXI_BUS_u_MISI4A_si_slave_interface_current_read_channel PAR_FAXI_BUS_u_MISI4A_si_r_chnl_sel	way selection
3	PERI_PAR_FAXI_BUS__u_MISI4A__PERI_PAR_FAXI_BUS_u_MISI4A_si_slave_interface_Read_ID_is_missed PAR_FAXI_BUS_u_MISI4A_si_set_rid_mi_status ss	
2	PERI_PAR_FAXI_BUS__u_MISI4A__PERI_PAR_FAXI_BUS_u_MISI4A_si_slave_interface_Read_Channel PAR_FAXI_BUS_u_MISI4A_si_rd_ot_bus Y	Outstanding Busy
1	PERI_PAR_FAXI_BUS__u_MISI4A__PERI_PAR_FAXI_BUS_u_MISI4A_si_slave_interface_Write_Channel PAR_FAXI_BUS_u_MISI4A_si_wr_ot_bus Y	Outstanding Busy
0	PERI_PAR_FAXI_BUS__u_MISI4A__PERI_PAR_FAXI_BUS_u_MISI4A_si_slave_interface_control_signal PAR_FAXI_BUS_u_MISI4A_si_ctrl_updat ed	updated status

1A070074 PERI_PAR_FAXI_BUS__u_AS L4 PERI_PAR_FAXI_BUS__u_AS L40 control register 0
0_CTRL_0

000000FB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PERI_PAR_FAXI_BUS__u_AS L40__mst_sync_sel	PERI_PAR_FAXI_BUS__u_AS L40__slv_sync_sel	PERI_PAR_FAXI_BUS__u_AS L40__in_arflush_thre	PERI_PAR_FAXI_BUS__u_AS L40__in_awflush_thre	PERI_PAR_FAXI_BUS__u_AS L40__sample_sel	PERI_PAR_FAXI_BUS__u_AS L40__sync_mode	PERI_PAR_FAXI_BUS__u_AS L40__axi_idle_out	PERI_PAR_FAXI_BUS__u_AS L40__axi_idle_out_reg				
Type					RW	RW	RW	RW	RW	RW	RW	RW	RO	RO	RO	RO
Reset					0	0	0	0	1	1	1	1	1	0	1	1

Bit(s)	Name	Description
11:10	PERI_PAR_FAXI_BUS__u_AS L40__mst_sync_sel	
9:8	PERI_PAR_FAXI_BUS__u_AS L40__slv_sync_sel	
7:6	PERI_PAR_FAXI_BUS__u_AS L40__in_arflush_thre	
5:4	PERI_PAR_FAXI_BUS__u_AS L40__in_awflush_thre	
3	PERI_PAR_FAXI_BUS__u_AS L40__sample_sel	
2	PERI_PAR_FAXI_BUS__u_AS L40__sync_mode	Sync mode switch for ASLICE
1	PERI_PAR_FAXI_BUS__u_AS L40__axi_idle_out	
0	PERI_PAR_FAXI_BUS__u_AS L40__axi_idle_out_reg	

1A070078 PERI_PAR_FAXI_BUS_u_MISI7B control register 0 0000001C
7B_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											PERI_PAR_FAXI_BUS_u_MISI7B_cg_disable	PERI_PAR_FAXI_BUS_u_MISI7B_PERI_PAR_FAXI_BUS_u_MISI7B_mi_outstanding_extend_en	PERI_PAR_FAXI_BUS_u_MISI7B_PERI_PAR_FAXI_BUS_u_MISI7B_mi_qos_on	PERI_PAR_FAXI_BUS_u_MISI7B_PERI_PAR_FAXI_BUS_u_MISI7B_mi_master_interface_control_signal_updated_status	PERI_PAR_FAXI_BUS_u_MISI7B_PERI_PAR_FAXI_BUS_u_MISI7B_mi_master_interface_read_busy	PERI_PAR_FAXI_BUS_u_MISI7B_PERI_PAR_FAXI_BUS_u_MISI7B_mi_master_interface_write_busy
Type											RW	RW	RW	RO	RO	RO
Reset											0	1	1	1	0	0

Bit(s)	Name	Description
5	PERI_PAR_FAXI_BUS_u_MISI7B_cg_disable	
4	PERI_PAR_FAXI_BUS_u_MISI7B_PERI_PAR_FAXI_BUS_u_MISI7B_mi_outstanding_extend_en	
3	PERI_PAR_FAXI_BUS_u_MISI7B_PERI_PAR_FAXI_BUS_u_MISI7B_mi_qos_on	
2	PERI_PAR_FAXI_BUS_u_MISI7B_PERI_PAR_FAXI_BUS_u_MISI7B_mi_master_interface_control_signal_updated_status	
1	PERI_PAR_FAXI_BUS_u_MISI7B_PERI_PAR_FAXI_BUS_u_MISI7B_mi_master_interface_read_busy	
0	PERI_PAR_FAXI_BUS_u_MISI7B_PERI_PAR_FAXI_BUS_u_MISI7B_mi_master_interface_write_busy	

1A07007C

PERI_PAR_FAXI_BUS_u_MISI PERI_PAR_FAXI_BUS_u_MISI5A control register 0

0001E001

5A_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													PERI_P AR_FA XI_BUS u_MI SISA_ PERI_P AR_FA XI_BUS u_MIS cg_disa ble	PERI_P AR_FA XI_BUS u_MI SISA_ PERI_P AR_FA XI_BUS u_MIS I5A_si ctrl_by pass	PERI_P AR_FA XI_BUS u_MI SISA_ PERI_P AR_FA XI_BUS u_MIS I5A_si outstan ding_di interlea ve_en	PERI_P AR_FA XI_BUS u_MI SISA_ PERI_P AR_FA XI_BUS u_MIS I5A_si outstan ding_di interlea ve_en
Type													RW	RW	RW	RW
Reset													0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_P AR_FA XI_BUS u_MI SISA_ PERI_P AR_FA XI_BUS u_MI SISA_ I5A_si way_i nterlea ve_en	PERI_PAR_FAXI BUS_u_MISI 5A_PERI_PAR FAXI_BUS_u_ MISI5A_si_wa y_en		PERI_P AR_FA XI_BUS u_MI SISA_ PERI_P AR_FA XI_BUS u_MIS I5A_si dfslv_s et_wir q	PERI_P AR_FA XI_BUS u_MI SISA_ PERI_P AR_FA XI_BUS u_MIS I5A_si dfslv_s et_rirq	PERI_PAR_FAXI_BUS u_MISI5A_PERI_PAR FAXI_BUS_u_MISI5A_si _b_chnl_sel			PERI_P AR_FA XI_BUS u_MI SISA_ PERI_P AR_FA XI_BUS u_MIS I5A_si set_bid _miss	PERI_PAR_FAXI_BUS u_MISI5A_PERI_PAR FAXI_BUS_u_MISI5A_si _r_chnl_sel			PERI_P AR_FA XI_BUS u_MI SISA_ PERI_P AR_FA XI_BUS u_MIS I5A_si set_rid _miss	PERI_P AR_FA XI_BUS u_MI SISA_ PERI_P AR_FA XI_BUS u_MIS I5A_si rd_ot busy	PERI_P AR_FA XI_BUS u_MI SISA_ PERI_P AR_FA XI_BUS u_MIS I5A_si wr_ot busy	PERI_P AR_FA XI_BUS u_MI SISA_ PERI_P AR_FA XI_BUS u_MIS I5A_si _ctrl_u pdated
Type	RW	RW		RO	RO	RO			RO	RO			RO	RO	RO	RO
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
19	PERI_PAR_FAXI_BUS_u_MISI5A_cg_disa sable	
18	PERI_PAR_FAXI_BUS_u_MISI5A_PERI_P AR_FAXI_BUS_u_MISI5A_si_ctrl_bypas s	Bypasses idle check when updating SI setting
17	PERI_PAR_FAXI_BUS_u_MISI5A_PERI_si PAR_FAXI_BUS_u_MISI5A_si_outstandin g_disable	cabgen slave interface outstanding capability disable control
16:15	PERI_PAR_FAXI_BUS_u_MISI5A_PERI PERI_PAR_FAXI_BUS_u_MISI5A_si PAR_FAXI_BUS_u_MISI5A_si_way_interl eave_en	slave interface read arbiter interleaving function enable control
14:13	PERI_PAR_FAXI_BUS_u_MISI5A_PERI Control PERI_PAR_FAXI_BUS_u_MISI5A_si PAR_FAXI_BUS_u_MISI5A_si_way_en	address decode output path enable of each way
12	PERI_PAR_FAXI_BUS_u_MISI5A_PERI PERI_PAR_FAXI_BUS_u_MISI5A_si PAR_FAXI_BUS_u_MISI5A_si_dfslv_set_ IRQ status wirq	slave interface default slave write IRQ status

Bit(s)	Name	Description
11	PERI_PAR_FAXI_BUS__u_MISI5A__PERI_PAR_FAXI_BUS_u_MISI5A_si_dfslv_set_rstatus_irq	PERI_PAR_FAXI_BUS_u_MISI5A_si slave interface default slave read IRQ
10:8	PERI_PAR_FAXI_BUS__u_MISI5A__PERI_PAR_FAXI_BUS_u_MISI5A_si_b_chnl_sel	PERI_PAR_FAXI_BUS_u_MISI5A_si slave interface current write response channel way selection
7	PERI_PAR_FAXI_BUS__u_MISI5A__PERI_PAR_FAXI_BUS_u_MISI5A_si_set_bid_mimissed status ss	PERI_PAR_FAXI_BUS_u_MISI5A_si slave interface write response ID is missed status
6:4	PERI_PAR_FAXI_BUS__u_MISI5A__PERI_PAR_FAXI_BUS_u_MISI5A_si_r_chnl_sel	PERI_PAR_FAXI_BUS_u_MISI5A_si slave interface current read channel way selection
3	PERI_PAR_FAXI_BUS__u_MISI5A__PERI_PAR_FAXI_BUS_u_MISI5A_si_set_rid_mi status ss	PERI_PAR_FAXI_BUS_u_MISI5A_si slave interface Read ID is missed status
2	PERI_PAR_FAXI_BUS__u_MISI5A__PERI_PAR_FAXI_BUS_u_MISI5A_si_rd_ot_bus	PERI_PAR_FAXI_BUS_u_MISI5A_si slave interface Read Channel Outstanding Busy
1	PERI_PAR_FAXI_BUS__u_MISI5A__PERI_PAR_FAXI_BUS_u_MISI5A_si_wr_ot_bus	PERI_PAR_FAXI_BUS_u_MISI5A_si slave interface Write Channel Outstanding Busy
0	PERI_PAR_FAXI_BUS__u_MISI5A__PERI_PAR_FAXI_BUS_u_MISI5A_si_ctrl_updat	PERI_PAR_FAXI_BUS_u_MISI5A_si slave interface control signal updated status

1A070080 PERI_PAR_FAXI_BUS__u_AS_L41 PERI_PAR_FAXI_BUS__u_AS_L41 control register 0 000000FB
1_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PERI_PAR_FAXI_BUS__u_AS_L41__mst_sync_sel	PERI_PAR_FAXI_BUS__u_AS_L41__slv_sync_sel	PERI_PAR_FAXI_BUS__u_AS_L41__in_arflush_thre	PERI_PAR_FAXI_BUS__u_AS_L41__in_awflush_thre	PERI_PAR_FAXI_BUS__u_AS_L41__sample_sel	PERI_PAR_FAXI_BUS__u_AS_L41__sync_mode	PERI_PAR_FAXI_BUS__u_AS_L41__axi_idle_out_reg	PERI_PAR_FAXI_BUS__u_AS_L41__axi_idle_out_reg	PERI_PAR_FAXI_BUS__u_AS_L41__axi_idle_out_reg	PERI_PAR_FAXI_BUS__u_AS_L41__axi_idle_out_reg	PERI_PAR_FAXI_BUS__u_AS_L41__axi_idle_out_reg	PERI_PAR_FAXI_BUS__u_AS_L41__axi_idle_out_reg
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RO	RO
Reset					0	0	0	0	1	1	1	1	1	0	1	1

Bit(s)	Name	Description
11:10	PERI_PAR_FAXI_BUS__u_AS_L41__mst_sync_sel	
9:8	PERI_PAR_FAXI_BUS__u_AS_L41__slv_sync_sel	
7:6	PERI_PAR_FAXI_BUS__u_AS_L41__in_arflush_thre	
5:4	PERI_PAR_FAXI_BUS__u_AS_L41__in_awflush_thre	
3	PERI_PAR_FAXI_BUS__u_AS_L41__sample_sel	
2	PERI_PAR_FAXI_BUS__u_AS_L41__sync_mode	Sync mode switch for ASLICE mode
1	PERI_PAR_FAXI_BUS__u_AS_L41__axi_idle_out_reg	
0	PERI_PAR_FAXI_BUS__u_AS_L41__axi_idle_out_reg	

1A070084

PERI_PAR_FAXI_BUS_u_MISI PERI_PAR_FAXI_BUS_u_MISI6A control register 0

0001E001

6A_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													PERI_P AR_FA XI_BUS u_MI SI6A cg_disa ble	PERI_P AR_FA XI_BUS u_MI SI6A PERI_P AR_FA XI_BUS u_MIS I6A_si ctrl_by pass	PERI_P AR_FA XI_BUS u_MI SI6A PERI_P AR_FA XI_BUS u_MIS I6A_si outstan ding_di interlea ve_en	PERI_P AR_FA XI_BUS u_MI SI6A PERI_P AR_FA XI_BUS u_MIS I6A_si outstan ding_di interlea ve_en
Type													RW	RW	RW	RW
Reset													0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_P AR_FA XI_BUS u_MI SI6A PERI_P AR_FA XI_BUS u_MI SI6A _way_i nterlea ve_en	PERI_PAR_FAXI _BUS_u_MISI 6A_PERI_PAR _FAXI_BUS_u MISI6A_si_wa y_en		PERI_P AR_FA XI_BUS u_MI SI6A PERI_P AR_FA XI_BUS u_MIS I6A_si dfsiv_s et_wir q	PERI_P AR_FA XI_BUS u_MI SI6A PERI_P AR_FA XI_BUS u_MIS I6A_si dfsiv_s et_rirq	PERI_PAR_FAXI_BUS u_MISI6A_PERI_PAR _FAXI_BUS_u_MISI6A_si _b_chnl_sel			PERI_P AR_FA XI_BUS u_MI SI6A PERI_P AR_FA XI_BUS u_MIS I6A_si set_bid _miss	PERI_PAR_FAXI_BUS u_MISI6A_PERI_PAR _FAXI_BUS_u_MISI6A_si _r_chnl_sel			PERI_P AR_FA XI_BUS u_MI SI6A PERI_P AR_FA XI_BUS u_MIS I6A_si set_rid _miss	PERI_P AR_FA XI_BUS u_MI SI6A PERI_P AR_FA XI_BUS u_MIS I6A_si rd_ot busy	PERI_P AR_FA XI_BUS u_MI SI6A PERI_P AR_FA XI_BUS u_MIS I6A_si wr_ot busy	PERI_P AR_FA XI_BUS u_MI SI6A PERI_P AR_FA XI_BUS u_MIS I6A_si ctrl_u pdated
Type	RW	RW		RO	RO	RO			RO	RO			RO	RO	RO	RO
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
19	PERI_PAR_FAXI_BUS_u_MISI6A_cg_disa sable	
18	PERI_PAR_FAXI_BUS_u_MISI6A_PERI_P AR_FAXI_BUS_u_MISI6A_si_ctrl_bypas s	Bypasses idle check when updating SI setting
17	PERI_PAR_FAXI_BUS_u_MISI6A_PERI_P AR_FAXI_BUS_u_MISI6A_si_outstandin g_disable	cabgen slave interface outstanding capability disable control
16:15	PERI_PAR_FAXI_BUS_u_MISI6A_PERI_P AR_FAXI_BUS_u_MISI6A_si_way_interl eave_en	PERI_PAR_FAXI_BUS_u_MISI6A_si slave interface read arbiter interleaving function enable control
14:13	PERI_PAR_FAXI_BUS_u_MISI6A_PERI_P AR_FAXI_BUS_u_MISI6A_si_way_en	Control PERI_PAR_FAXI_BUS_u_MISI6A_si address decode output path enable of each way
12	PERI_PAR_FAXI_BUS_u_MISI6A_PERI_P AR_FAXI_BUS_u_MISI6A_si_dfsiv_set_ wirq	PERI_PAR_FAXI_BUS_u_MISI6A_si slave interface default slave write IRQ status

Bit(s)	Name	Description
11	PERI_PAR_FAXI_BUS__u_MISI6A__PERI_PAR_FAXI_BUS_u_MISI6A_si_slave_interface_default_slave_read_IRQ PAR_FAXI_BUS_u_MISI6A_si_dfslv_set_rstatus irq	
10:8	PERI_PAR_FAXI_BUS__u_MISI6A__PERI_PAR_FAXI_BUS_u_MISI6A_si_slave_interface_current_write PAR_FAXI_BUS_u_MISI6A_si_b_chnl_sel	response channel way selection
7	PERI_PAR_FAXI_BUS__u_MISI6A__PERI_PAR_FAXI_BUS_u_MISI6A_si_slave_interface_write_response_ID_is PAR_FAXI_BUS_u_MISI6A_si_set_bid_mimissed_status ss	
6:4	PERI_PAR_FAXI_BUS__u_MISI6A__PERI_PAR_FAXI_BUS_u_MISI6A_si_slave_interface_current_read_channel PAR_FAXI_BUS_u_MISI6A_si_r_chnl_sel	way selection
3	PERI_PAR_FAXI_BUS__u_MISI6A__PERI_PAR_FAXI_BUS_u_MISI6A_si_slave_interface_Read_ID_is_missed PAR_FAXI_BUS_u_MISI6A_si_set_rid_mi_status ss	
2	PERI_PAR_FAXI_BUS__u_MISI6A__PERI_PAR_FAXI_BUS_u_MISI6A_si_slave_interface_Read_Channel PAR_FAXI_BUS_u_MISI6A_si_rd_ot_bus Y	Outstanding Busy
1	PERI_PAR_FAXI_BUS__u_MISI6A__PERI_PAR_FAXI_BUS_u_MISI6A_si_slave_interface_Write_Channel PAR_FAXI_BUS_u_MISI6A_si_wr_ot_bus Y	Outstanding Busy
0	PERI_PAR_FAXI_BUS__u_MISI6A__PERI_PAR_FAXI_BUS_u_MISI6A_si_slave_interface_control_signal PAR_FAXI_BUS_u_MISI6A_si_ctrl_updat ed	updated status

1A070088 PERI_PAR_FAXI_BUS__u_AS L42 PERI_PAR_FAXI_BUS__u_AS L42 control register 0 000000FB
2_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PERI_PAR_FAXI_BUS__u_AS L42__mst_sync_sel		PERI_PAR_FAXI_BUS__u_AS L42__slv_sync_sel		PERI_PAR_FAXI_BUS__u_AS L42__in_arflush_thre		PERI_PAR_FAXI_BUS__u_AS L42__in_awflush_thre		PERI_PAR_FAXI_BUS__u_AS L42__sample_sel	PERI_PAR_FAXI_BUS__u_AS L42__sync_mode	PERI_PAR_FAXI_BUS__u_AS L42__axi_idle_out	PERI_PAR_FAXI_BUS__u_AS L42__axi_idle_out_reg
Type					RW		RW		RW		RW		RW	RW	RO	RO
Reset					0	0	0	0	1	1	1	1	1	0	1	1

Bit(s)	Name	Description
11:10	PERI_PAR_FAXI_BUS__u_AS L42__mst_sync_sel	
9:8	PERI_PAR_FAXI_BUS__u_AS L42__slv_sync_sel	
7:6	PERI_PAR_FAXI_BUS__u_AS L42__in_arflush_thre	
5:4	PERI_PAR_FAXI_BUS__u_AS L42__in_awflush_thre	
3	PERI_PAR_FAXI_BUS__u_AS L42__sample_sel	
2	PERI_PAR_FAXI_BUS__u_AS L42__sync_mode	Sync mode switch for ASLICE
1	PERI_PAR_FAXI_BUS__u_AS L42__axi_idle_out	
0	PERI_PAR_FAXI_BUS__u_AS L42__axi_idle_out_reg	

1A07008C

PERI_PAR_FAXI_BUS_u_MISI PERI_PAR_FAXI_BUS_u_MISI7A control register 0

0001E001

7A_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													PERI_P AR_FA XI_BUS u_MI SI7A cg_disa ble	PERI_P AR_FA XI_BUS u_MI SI7A PERI_P AR_FA XI_BUS u_MIS I7A_si ctrl_by pass	PERI_P AR_FA XI_BUS u_MI SI7A PERI_P AR_FA XI_BUS u_MIS I7A_si outstan ding_di interlea ve_en	PERI_P AR_FA XI_BUS u_MI SI7A PERI_P AR_FA XI_BUS u_MIS I7A_si outstan ding_di interlea ve_en
Type													RW	RW	RW	RW
Reset													0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_P AR_FA XI_BUS u_MI SI7A PERI_P AR_FA XI_BUS u_MI SI7A ctrl_by pass	PERI_PAR_FAXI_BUS_u_MISI7A_PERI_PAR_FAXI_BUS_u_MISI7A_si_way_interleave_en		PERI_P AR_FA XI_BUS u_MI SI7A PERI_P AR_FA XI_BUS u_MIS I7A_si dfsrlv_s et_wir q	PERI_P AR_FA XI_BUS u_MI SI7A PERI_P AR_FA XI_BUS u_MIS I7A_si dfsrlv_s et_rirq	PERI_PAR_FAXI_BUS_u_MISI7A_PERI_PAR_FAXI_BUS_u_MISI7A_si_b_chnl_sel			PERI_P AR_FA XI_BUS u_MI SI7A PERI_P AR_FA XI_BUS u_MIS I7A_si set_bid _miss	PERI_PAR_FAXI_BUS_u_MISI7A_PERI_PAR_FAXI_BUS_u_MISI7A_si_r_chnl_sel			PERI_P AR_FA XI_BUS u_MI SI7A PERI_P AR_FA XI_BUS u_MIS I7A_si set_rid _miss	PERI_P AR_FA XI_BUS u_MI SI7A PERI_P AR_FA XI_BUS u_MIS I7A_si rd_ot busy	PERI_P AR_FA XI_BUS u_MI SI7A PERI_P AR_FA XI_BUS u_MIS I7A_si wr_ot busy	PERI_P AR_FA XI_BUS u_MI SI7A PERI_P AR_FA XI_BUS u_MIS I7A_si ctrl_u pdated
Type	RW	RW		RO	RO	RO			RO	RO			RO	RO	RO	RO
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
19	PERI_PAR_FAXI_BUS_u_MISI7A_cg_disable	
18	PERI_PAR_FAXI_BUS_u_MISI7A_PERI_Par_FAXI_BUS_u_MISI7A_si_ctrl_bypass	Bypasses idle check when updating SI setting
17	PERI_PAR_FAXI_BUS_u_MISI7A_PERI_si_cabgen_slave_interface_outstanding_capability_disable_control	
16:15	PERI_PAR_FAXI_BUS_u_MISI7A_PERI_Par_FAXI_BUS_u_MISI7A_si_slave_interface_read_arbiter	
14:13	PERI_PAR_FAXI_BUS_u_MISI7A_PERI_Par_FAXI_BUS_u_MISI7A_si_slave_interface_read_arbiter	Control PERI_PAR_FAXI_BUS_u_MISI7A_si address decode output path enable of each way
12	PERI_PAR_FAXI_BUS_u_MISI7A_PERI_Par_FAXI_BUS_u_MISI7A_si_slave_interface_default_slave_write	
	PERI_PAR_FAXI_BUS_u_MISI7A_si_dfsrlv_set_IRQ status	
	wirq	

Bit(s)	Name	Description
11	PERI_PAR_FAXI_BUS__u_MISI7A__PERI_PAR_FAXI_BUS_u_MISI7A_si_dfslv_set_rstatus_irq	PERI_PAR_FAXI_BUS_u_MISI7A_si slave interface default slave read IRQ
10:8	PERI_PAR_FAXI_BUS__u_MISI7A__PERI_PAR_FAXI_BUS_u_MISI7A_si_b_chnl_sel	PERI_PAR_FAXI_BUS_u_MISI7A_si slave interface current write response channel way selection
7	PERI_PAR_FAXI_BUS__u_MISI7A__PERI_PAR_FAXI_BUS_u_MISI7A_si_set_bid_mimissed status ss	PERI_PAR_FAXI_BUS_u_MISI7A_si slave interface write response ID is missed status
6:4	PERI_PAR_FAXI_BUS__u_MISI7A__PERI_PAR_FAXI_BUS_u_MISI7A_si_r_chnl_sel	PERI_PAR_FAXI_BUS_u_MISI7A_si slave interface current read channel way selection
3	PERI_PAR_FAXI_BUS__u_MISI7A__PERI_PAR_FAXI_BUS_u_MISI7A_si_set_rid_mi status ss	PERI_PAR_FAXI_BUS_u_MISI7A_si slave interface Read ID is missed status
2	PERI_PAR_FAXI_BUS__u_MISI7A__PERI_PAR_FAXI_BUS_u_MISI7A_si_rd_ot_bus	PERI_PAR_FAXI_BUS_u_MISI7A_si slave interface Read Channel Outstanding Busy
1	PERI_PAR_FAXI_BUS__u_MISI7A__PERI_PAR_FAXI_BUS_u_MISI7A_si_wr_ot_bus	PERI_PAR_FAXI_BUS_u_MISI7A_si slave interface Write Channel Outstanding Busy
0	PERI_PAR_FAXI_BUS__u_MISI7A__PERI_PAR_FAXI_BUS_u_MISI7A_si_ctrl_updat	PERI_PAR_FAXI_BUS_u_MISI7A_si slave interface control signal updated status

1A070090 PERI_PAR_FAXI_BUS__u_AS_L4 PERI_PAR_FAXI_BUS__u_AS_L43 control register 0
3_CTRL_0

000000FB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PERI_PAR_FAXI_BUS__u_AS_L43__mst_sync_sel	PERI_PAR_FAXI_BUS__u_AS_L43__slv_sync_sel	PERI_PAR_FAXI_BUS__u_AS_L43__in_arflush_thre	PERI_PAR_FAXI_BUS__u_AS_L43__in_awflush_thre	PERI_PAR_FAXI_BUS__u_AS_L43__sample_sel	PERI_PAR_FAXI_BUS__u_AS_L43__sync_mode	PERI_PAR_FAXI_BUS__u_AS_L43__axi_idle_out	PERI_PAR_FAXI_BUS__u_AS_L43__axi_idle_out_reg				
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RO	RO
Reset					0	0	0	0	1	1	1	1	1	0	1	1

Bit(s)	Name	Description
11:10	PERI_PAR_FAXI_BUS__u_AS_L43__mst_sync_sel	
9:8	PERI_PAR_FAXI_BUS__u_AS_L43__slv_sync_sel	
7:6	PERI_PAR_FAXI_BUS__u_AS_L43__in_arflush_thre	
5:4	PERI_PAR_FAXI_BUS__u_AS_L43__in_awflush_thre	
3	PERI_PAR_FAXI_BUS__u_AS_L43__sample_sel	
2	PERI_PAR_FAXI_BUS__u_AS_L43__sync_mode	Sync mode switch for ASLICE mode
1	PERI_PAR_FAXI_BUS__u_AS_L43__axi_idle_out	
0	PERI_PAR_FAXI_BUS__u_AS_L43__axi_idle_out_reg	

1A070094 PERI_PAR_FAXI_BUS_u_MI11 PERI_PAR_FAXI_BUS_u_MI11 control register 0
CTRL_0

00007FC1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PERI_PAR_FAXI_BUS__u_MI11__reg_prot_mode					PERI_PAR_FAXI_BUS__u_MI11__reg_mas_lim_gnt_cnt								PERI_PAR_FAXI_BUS__u_MI11__reg_gntcnt_sel	PERI_PAR_FAXI_BUS__u_MI11__reg_filter_len_sel	
Type	RW					RW								RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_PAR_FAXI_BUS__u_MI11__reg_bw_lim_en	PERI_PAR_FAXI_BUS__u_MI11__reg_slave_way_en	PERI_PAR_FAXI_BUS__u_MI11__reg_master_req_en					PERI_PAR_FAXI_BUS__u_MI11__ahb_bus_layer_idle	PERI_PAR_FAXI_BUS__u_MI11__ctrl_update_status		PERI_PAR_FAXI_BUS__u_MI11__hmaster_s					
Type	RW	RW	RW					RO	RO		RO					
Reset	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1

Bit(s)	Name	Description
31:27	PERI_PAR_FAXI_BUS__u_MI11__reg_prot_mode	
26:19	PERI_PAR_FAXI_BUS__u_MI11__reg_mas_lim_gnt_cnt	
18	PERI_PAR_FAXI_BUS__u_MI11__reg_gntcnt_sel	
17:16	PERI_PAR_FAXI_BUS__u_MI11__reg_filter_len_sel	
15	PERI_PAR_FAXI_BUS__u_MI11__reg_bw_lim_en	
14	PERI_PAR_FAXI_BUS__u_MI11__reg_slave_way_en	
13:9	PERI_PAR_FAXI_BUS__u_MI11__reg_master_req_en	
8	PERI_PAR_FAXI_BUS__u_MI11__ahb_bus_layer_idle	
7:6	PERI_PAR_FAXI_BUS__u_MI11__ctrl_update_status	
5:0	PERI_PAR_FAXI_BUS__u_MI11__hmaster_r_s	

1A070098

PERI_PAR_FAXI_BUS_u_MI11 PERI_PAR_FAXI_BUS_u_MI11 control register 1

00000002

CTRL_1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_P AR_FA XI_BUS __u_MI 11_er ror fla g_en	PERI_P AR_FA XI_BUS XI_BUS __u_MI 11_re g_qos_ en
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
1	PERI_PAR_FAXI_BUS__u_MI11__error_flag_en	
0	PERI_PAR_FAXI_BUS__u_MI11__reg_qos_en	

Module name: bcrn_PERI_PDN_wrapper_u_bcrn_PERI_PDN_bcrn Base address: (+0x1A08_0000)

Address	Name	Width	Register Function
1A080000	<u>PERI_QAXI_BUS_u_Ink_APDMA_EXT_M_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_ups_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_APDMA_EXT_M_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_ups control register 0
1A080004	<u>PERI_QAXI_BUS_u_Ink_APDMA_EXT_M_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_APDMA_EXT_M_to_PERI_QAXI_BUS_MISI3A_DCM_PROT control register 0
1A080008	<u>PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_DCM_PROT control register 0
1A08000C	<u>PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI control register 0
1A080010	<u>PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_DCM_PROT_ups_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_DCM_PROT_ups control register 0
1A080014	<u>PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_DCM_PROT_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_DCM_PROT control register 0
1A080018	<u>PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_AXI_QOS_REPLACE_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_AXI_QOS_REPLACE control register 0
1A08001C	<u>PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0 control register 0
1A080020	<u>PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S control register 0
1A080024	<u>PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0 control register 0
1A080028	<u>PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S control register 0
1A08002C	<u>PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0 control register 0
1A080030	<u>PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S control register 0
1A080034	<u>PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S control register 0
1A080038	<u>PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI11_AXI_PWR_PROT_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI11_AXI_PWR_PROT control register 0

Address	Name	Width	Register Function
	<u>AXI AO BUS SI11 AXI PWR PROT_CTRL_0</u>		
1A08003C	<u>PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI13_AXI_PWR_PROT_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI13_AXI_PWR_PROT control register 0
1A080040	<u>PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_SI12_to_DEBUGSYS_APB_S_SBUS2APB_CTRL_0</u>	32	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_SI12_to_DEBUGSYS_APB_S_SBUS2APB control register 0
1A080044	<u>PERI_QAXI_BUS_u_SL22_CTRL_0</u>	32	PERI_QAXI_BUS_u_SL22 control register 0
1A080048	<u>PERI_QAXI_BUS_u_MISI2A_CTRL_0</u>	32	PERI_QAXI_BUS_u_MISI2A control register 0
1A08004C	<u>PERI_QAXI_BUS_u_MISI3A_CTRL_0</u>	32	PERI_QAXI_BUS_u_MISI3A control register 0
1A080050	<u>PERI_QAXI_BUS_u_MISI3_CTRL_0</u>	32	PERI_QAXI_BUS_u_MISI3 control register 0
1A080054	<u>PERI_QAXI_BUS_u_MISI2B_CTRL_0</u>	32	PERI_QAXI_BUS_u_MISI2B control register 0
1A080058	<u>PERI_QAXI_BUS_u_MISI2B_CTRL_1</u>	32	PERI_QAXI_BUS_u_MISI2B control register 1
1A08005C	<u>PERI_QAXI_BUS_u_SI12_CTRL_0</u>	32	PERI_QAXI_BUS_u_SI12 control register 0
1A080060	<u>PERI_QAXI_BUS_u_SI19_CTRL_0</u>	32	PERI_QAXI_BUS_u_SI19 control register 0
1A080064	<u>PERI_QAXI_BUS_u_SI19_CTRL_1</u>	32	PERI_QAXI_BUS_u_SI19 control register 1
1A080068	<u>PERI_QAXI_AHB_BUS_u_Ink_PWM_M_to_PERI_QAXI_AHB_BUS_MI18_AHB_M_QOS_REPLACE_CTRL_0</u>	32	PERI_QAXI_AHB_BUS_u_Ink_PWM_M_to_PERI_QAXI_AHB_BUS_MI18_AHB_M_QOS_REPLACE control register 0
1A08006C	<u>PERI_QAXI_AHB_BUS_u_Ink_AUDIO_M_to_PERI_QAXI_AHB_BUS_MI18_AHB_M_QOS_REPLACE_CTRL_0</u>	32	PERI_QAXI_AHB_BUS_u_Ink_AUDIO_M_to_PERI_QAXI_AHB_BUS_MI18_AHB_M_QOS_REPLACE control register 0
1A080070	<u>PERI_QAXI_AHB_BUS_u_MI18_CTRL_0</u>	32	PERI_QAXI_AHB_BUS_u_MI18 control register 0

1A080000 PERI_QAXI_BUS_u_Ink_APD PERI_QAXI_BUS_u_Ink_APDMA_EXT_M_to_PERI
 MA_EXT_M_to_PERI_QAXI_B_QAXI_BUS_MISI3A_DCM_PROT_ups control 00000000
 US_MISI3A_DCM_PROT_ups register 0
 CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_QAXI_BUS_u_Ink_APDMA_EXT_M_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_ups_axi_clock_gated_en	PERI_QAXI_BUS_u_Ink_APDMA_EXT_M_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_ups_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	PERI_QAXI_BUS_u_Ink_APDMA_EXT_M_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_ups_axi_clock_gated_en	
0	PERI_QAXI_BUS_u_Ink_APDMA_EXT_M_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_ups_axi_clock_gated	

1A080004 PERI_QAXI_BUS_u_Ink_APD PERI_QAXI_BUS_u_Ink_APDMA_EXT_M_to_PERI
 MA_EXT_M_to_PERI_QAXI_B_QAXI_BUS_MISI3A_DCM_PROT control register
 US_MISI3A_DCM_PROT_CTRL0
 _0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_QAXI_BUS_u_Ink_APDMA_EXT_M_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_axi_clock_gated_en	PERI_QAXI_BUS_u_Ink_APDMA_EXT_M_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	PERI_QAXI_BUS_u_Ink_APDMA_EXT_M_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_axi_clock_gated_en	
0	PERI_QAXI_BUS_u_Ink_APDMA_EXT_M_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_axi_clock_gated	

1A080008 PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_M 00000001
 QAXI_AHB_BUS_MI18_to_PE_I18_to_PERI_QAXI_BUS_MISI3A_DCM_PROT
 RI_QAXI_BUS_MISI3A_DCM control register 0
 PROT_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_rg_monitor_mode	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_rg_cmd_cnt_clr	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_error_flag_en
Type														RW	RW	RW
Reset														0	0	1

Bit(s)	Name	Description
2	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_rg_monitor_mode	
1	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_rg_cmd_cnt_clr	
0	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_DCM_PROT_error_flag_en	

1A08000C PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_M 000000F8
 QAXI_AHB_BUS_MI18_to_PE_I18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI
 RI_QAXI_BUS_MISI3A_AHB_S control register 0
 2AXI_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI_hflush_thres		PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI_hsecur_en	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI_hbst	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI_buffer_en	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI_merge_en	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI_fifo_threshold			PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI_read_ahead_bw
Type							RW		RW	RW	RW	RW	RW			RW
Reset							0	0	1	1	1	1	1	0	0	0

Bit(s)	Name	Description
9:8	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI_hflush_thres	
7	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI_hsecur_en	OPT
6	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI_hbst	
5	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI_buffer_en	
4	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI_merge_en	
3:1	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI_fifo_threshold	
0	PERI_QAXI_BUS_u_Ink_PERI_QAXI_AHB_BUS_MI18_to_PERI_QAXI_BUS_MISI3A_AHB_S2AXI_read_ahead_bw	

Bit(s)	Name	Description

1A080010 PERI_QAXI_BUS_u_Ink_APD PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI 00000000
MA_INT_M_to_PERI_QAXI_B _QAXI_BUS_MISI2A_DCM_PROT_ups control
US_MISI2A_DCM_PROT_ups register 0
CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_DCM_PROT_ups_axi_clock_gated_en	PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_DCM_PROT_ups_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_DCM_PROT_ups_axi_clock_gated_en	
0	PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_DCM_PROT_ups_axi_clock_gated	

1A080014 PERI_QAXI_BUS_u_Ink_APD PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI
 MA_INT_M_to_PERI_QAXI_B_QAXI_BUS_MISI2A_DCM_PROT control register
 US_MISI2A_DCM_PROT_CTRL0
 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_DCM_PROT_axi_clock_gated_en	PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_DCM_PROT_axi_clock_gated
Type															RW	RO
Reset															0	0

Bit(s)	Name	Description
1	PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_DCM_PROT_axi_clock_gated_en	
0	PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_DCM_PROT_axi_clock_gated	

1A080018 PERI_QAXI_BUS_u_Ink_APD PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI
 MA_INT_M_to_PERI_QAXI_B_QAXI_BUS_MISI2A_AXI_QOS_REPLACE control
 US_MISI2A_AXI_QOS_REPLA register 0
 CE_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PERI_QAXI_BU S_u_Ink_APD MA_INT_M_to _PERI_QAXI_B US_MISI2A_AX I_QOS_REPLAC E_reg_arflush	PERI_QAXI_BU S_u_Ink_APD MA_INT_M_to _PERI_QAXI_B US_MISI2A_AX I_QOS_REPLAC E_reg_arultra	PERI_QAXI_BU S_u_Ink_APD MA_INT_M_to _PERI_QAXI_B US_MISI2A_AX I_QOS_REPLAC E_reg_awflush	PERI_QAXI_BU S_u_Ink_APD MA_INT_M_to _PERI_QAXI_B US_MISI2A_AX I_QOS_REPLAC E_reg_awultra				
Type									RW		RW		RW		RW	
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:6	PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_AXI_QOS_REPLACE__reg_arflush	This is to replace AXI Read Flush QoS for APDMA_INT_M
5:4	PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_AXI_QOS_REPLACE__reg_arultra	This is to replace AXI Read Ultra QoS for APDMA_INT_M
3:2	PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_AXI_QOS_REPLACE__reg_awflush	This is to replace AXI Write Flush QoS for APDMA_INT_M
1:0	PERI_QAXI_BUS_u_Ink_APDMA_INT_M_to_PERI_QAXI_BUS_MISI2A_AXI_QOS_REPLACE__reg_awultra	This is to replace AXI Write Ultra QoS for APDMA_INT_M

1A08001C PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B 00001801
 QAXI_BUS_MISI2B_to_AUDIO_to_AUDIO_S_AXI_SECURE_CTRL0 control
 S_AXI_SECURE_CTRL0_CTRL register 0

0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_disable	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_bypass	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_outstanding_disable	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_way_interleave_en	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_way_en	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_wirq	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_rirq	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_bid_miss	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_hnl_sel	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_hnl_sel	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_rid_miss	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_rid_busy	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_wr_ot_busy	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_wr_ot_busy	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_wr_ot_busy	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_wr_ot_busy
Type	RW	RW	RW	RW	RW	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_disable	
14	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_bypass	Bypasses idle check when updating SI setting
13	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_outstanding_disable	Slave interface outstanding capability disable control
12	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_way_interleave_en	Slave interface read arbiter interleaving function enable control
11	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_way_en	Control address decode output path enable of each way
10	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI_SECURE_CTRL0_axi_secure_ctrl_set_wirq	Slave interface default slave write IRQ status

Bit(s)	Name	Description
9	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface default slave read IRQ status _MISI2B_to_AUDIO_S_AXI_SECURE_CTR LO__axi_secure_ctrl_set_rirq	
8:7	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface current write response channel way selection _MISI2B_to_AUDIO_S_AXI_SECURE_CTR LO__axi_secure_ctrl_b_chnl_sel	
6	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface write response ID is missed status _MISI2B_to_AUDIO_S_AXI_SECURE_CTR LO__axi_secure_ctrl_set_bid_miss	
5:4	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface current read channel way selection _MISI2B_to_AUDIO_S_AXI_SECURE_CTR LO__axi_secure_ctrl_r_chnl_sel	
3	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface Read ID is missed status _MISI2B_to_AUDIO_S_AXI_SECURE_CTR LO__axi_secure_ctrl_set_rid_miss	
2	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface Read Channel Outstanding Busy _MISI2B_to_AUDIO_S_AXI_SECURE_CTR LO__axi_secure_ctrl_rd_ot_busy	
1	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface Write Channel Outstanding Busy _MISI2B_to_AUDIO_S_AXI_SECURE_CTR LO__axi_secure_ctrl_wr_ot_busy	
0	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface control signal updated status _MISI2B_to_AUDIO_S_AXI_SECURE_CTR LO__axi_secure_ctrl_ctrl_updated	

1A080020 PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B 00001FD5
 QAXI_BUS_MISI2B_to_AUDIO_to_AUDIO_S_AXI2AHB_S control register 0
 S_AXI2AHB_S_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_bypass_mode	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_flush_thres		PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_arhburst		PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_ahburst		PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_armask_b		PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_arthre		PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_burst_en		PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_buffer_n	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_x2h_idle	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_x2h_idle
Type	RW	RW		RW		RW		RW		RW		RW		RW	RW	RO
Reset	0	0	0	1	1	1	1	1	1	1	0	1	0	1	0	1

Bit(s)	Name	Description
15	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_bypass_mode	
14:13	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_flush_thres	
12:10	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_arhburst	
9:7	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_ahburst	
6	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_armask_b	
5:3	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_arthre	
2	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_burst_en	
1	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_AUDIO_S_AXI2AHB_S_buffer_n	

Bit(s)	Name	Description
0	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS__MIS12B_to_AUDIO_S_AXI2AHB_S__x2h_idle	

1A080024 PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_QAXI_BUS_MISI2B_to_SSUSB_to_SSUSB_S_AXI_SECURE_CTRL0 control 00001801
S_AXI_SECURE_CTRL0_CTRL register 0

0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_cg_disable	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_outstanding_bypass	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_way_interleave_en	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_way_en	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_wirq	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_rirq	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_bid_miss			PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_hnl_sel	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_rid_busy			PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_wr_busy	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_wr_busy	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_wr_busy	
Type	RW	RW	RW	RW	RW	RO	RO	RO			RO	RO			RO	RO	RO
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	

Bit(s)	Name	Description
15	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_cg_disable	
14	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_bypass	Bypasses idle check when updating SI setting
13	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_outstanding_disable	Slave interface outstanding capability disable control
12	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_way_interleave_en	Slave interface read arbiter interleaving function enable control
11	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_way_en	Control address decode output path enable of each way
10	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI_SECURE_CTRL0_axi_secure_ctrl_set_wirq	Slave interface default slave write IRQ status

Bit(s)	Name	Description
9	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface default slave read IRQ status _MISI2B_to_SSUSB_S_AXI_SECURE_CTR LO__axi_secure_ctrl_set_rirq	
8:7	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface current write response channel way selection _MISI2B_to_SSUSB_S_AXI_SECURE_CTR LO__axi_secure_ctrl_b_chnl_sel	
6	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface write response ID is missed status _MISI2B_to_SSUSB_S_AXI_SECURE_CTR LO__axi_secure_ctrl_set_bid_miss	
5:4	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface current read channel way selection _MISI2B_to_SSUSB_S_AXI_SECURE_CTR LO__axi_secure_ctrl_r_chnl_sel	
3	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface Read ID is missed status _MISI2B_to_SSUSB_S_AXI_SECURE_CTR LO__axi_secure_ctrl_set_rid_miss	
2	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface Read Channel Outstanding Busy _MISI2B_to_SSUSB_S_AXI_SECURE_CTR LO__axi_secure_ctrl_rd_ot_busy	
1	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface Write Channel Outstanding Busy _MISI2B_to_SSUSB_S_AXI_SECURE_CTR LO__axi_secure_ctrl_wr_ot_busy	
0	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface control signal updated status _MISI2B_to_SSUSB_S_AXI_SECURE_CTR LO__axi_secure_ctrl_ctrl_updated	

1A080028 PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B 00001FD5
 QAXI_BUS_MISI2B_to_SSUSB_to_SSUSB_S_AXI2AHB_S control register 0
 S_AXI2AHB_S_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_bypass_mode	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_flush_thres		PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_arhburst			PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_ahburst			PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_armask_b			PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_arhre	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_burst_en	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_buffer_en	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_idle
Type	RW	RW		RW			RW			RW			RW	RW	RW	RO
Reset	0	0	0	1	1	1	1	1	1	1	0	1	0	1	0	1

Bit(s)	Name	Description
15	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_bypass_mode	
14:13	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_flush_thres	
12:10	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_arhburst	
9:7	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_ahburst	
6	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_armask_b	
5:3	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_arhre	
2	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_burst_en	
1	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_S_AXI2AHB_S_buffer_en	

Bit(s)	Name	Description
0	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS__MIS12B_to_SSUSB_S_AXI2AHB_S__x2h_idle	

1A08002C

PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B
QAXI_BUS_MISI2B_to_SSUSB_to_SSUSB_P1_S_AXI_SECURE_CTRL0 control
P1_S_AXI_SECURE_CTRL0_C register 0

00001801

TRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_cg_disable	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_by_pass	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_outstanding_disable	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_way_interleave_en	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_way_en	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_set_wirq	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_set_rirq	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_b_chnl_sel	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_r_chnl_sel	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_r_chnl_sel	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_r_chnl_sel	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_r_chnl_sel	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_r_chnl_sel	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_r_chnl_sel	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_r_chnl_sel	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_r_chnl_sel
Type	RW	RW	RW	RW	RW	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_cg_disable	
14	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_by_pass	Bypasses idle check when updating SI setting
13	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_outstanding_disable	Slave interface outstanding capability disable control
12	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_way_interleave_en	Slave interface read arbiter interleaving function enable control
11	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_way_en	Control address decode output path enable of each way
10	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI_SECURE_CTRL0_axi_secure_ctrl_set_wirq	Slave interface default slave write IRQ status

Bit(s)	Name	Description
9	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface default slave read IRQ status _MISI2B_to_SSUSB_P1_S_AXI_SECURE_ CTRL0__axi_secure_ctrl_set_rirq	
8:7	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface current write response channel way selection _MISI2B_to_SSUSB_P1_S_AXI_SECURE_ CTRL0__axi_secure_ctrl_b_chnl_sel	
6	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface write response ID is missed status _MISI2B_to_SSUSB_P1_S_AXI_SECURE_ CTRL0__axi_secure_ctrl_set_bid_miss	
5:4	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface current read channel way selection _MISI2B_to_SSUSB_P1_S_AXI_SECURE_ CTRL0__axi_secure_ctrl_r_chnl_sel	
3	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface Read ID is missed status _MISI2B_to_SSUSB_P1_S_AXI_SECURE_ CTRL0__axi_secure_ctrl_set_rid_miss	
2	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface Read Channel Outstanding Busy _MISI2B_to_SSUSB_P1_S_AXI_SECURE_ CTRL0__axi_secure_ctrl_rd_ot_busy	
1	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface Write Channel Outstanding Busy _MISI2B_to_SSUSB_P1_S_AXI_SECURE_ CTRL0__axi_secure_ctrl_wr_ot_busy	
0	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUSSlave interface control signal updated status _MISI2B_to_SSUSB_P1_S_AXI_SECURE_ CTRL0__axi_secure_ctrl_ctrl_updated	

1A080030 PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_QAXI_BUS_MISI2B_to_SSUSB_to_SSUSB_P1_S_AXI2AHB_S control register 0 00001FD5
P1_S_AXI2AHB_S_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_bypass_mode	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_flush_thres		PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_arhburst			PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_ahburst			PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_armask_b	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_arthre			PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_burst_en	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_buffer_en	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_idle
Type	RW	RW		RW			RW			RW	RW			RW	RW	RO
Reset	0	0	0	1	1	1	1	1	1	1	0	1	0	1	0	1

Bit(s)	Name	Description
15	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_bypass_mode	
14:13	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_flush_thres	
12:10	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_arhburst	
9:7	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_ahburst	
6	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_armask_b	
5:3	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_arthre	
2	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_burst_en	
1	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_SSUSB_P1_S_AXI2AHB_S_buffer_en	

Bit(s)	Name	Description
0	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS__MISI2B_to_SSUSB_P1_S_AXI2AHB_S__x2h_idle	

1A080034 PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_QAXI_BUS_MISI2B_to_PERI_P_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S 00001FD5
 AR_QAXI_BUS_SI22_AXI2AHB control register 0
 S_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S_bypass_mode	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S_flush_thres		PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S_arhburst			PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S_ahburst			PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S_armask_b				PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S_burst_en	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S_buff_en	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S_x2h_idle
Type	RW	RW		RW			RW			RW		RW		RW	RW	RO
Reset	0	0	0	1	1	1	1	1	1	1	0	1	0	1	0	1

Bit(s)	Name	Description
15	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S_bypass_mode	
14:13	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S_flush_thres	
12:10	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S_arhburst	
9:7	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S_ahburst	
6	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S_armask_b	
5:3	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S_arthre	
2	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S_burst_en	

Bit(s)	Name	Description
1	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS__MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S__buffer_en	
0	PERI_QAXI_BUS__u_Ink_PERI_QAXI_BUS__MISI2B_to_PERI_PAR_QAXI_BUS_SI22_AXI2AHB_S__x2h_idle	

1A080038

PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B
 QAXI_BUS_MISI2B_to_PERI_ _to_PERI_QAXI_AO_BUS_SI11_AXI_PWR_PROT
 QAXI_AO_BUS_SI11_AXI_PW control register 0
 R_PROT_CTRL_0

00000005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI11_AXI_PWR_PROT_axi_clock_gated_en	PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI11_AXI_PWR_PROT_error_flag_en	PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI11_AXI_PWR_PROT_axi_clock_gated_en	PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI11_AXI_PWR_PROT_protect_idle
Type													RW	RW	RO	RO
Reset													0	1	0	1

Bit(s)	Name	Description
3	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI11_AXI_PWR_PROT_axi_clock_gated_en	
2	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI11_AXI_PWR_PROT_error_flag_en	
1	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI11_AXI_PWR_PROT_axi_clock_gated	
0	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI11_AXI_PWR_PROT_protect_idle	

1A08003C PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B 00000005
 QAXI_BUS_MISI2B_to_PERI_ _to_PERI_QAXI_AO_BUS_SI13_AXI_PWR_PROT
 QAXI_AO_BUS_SI13_AXI_PW control register 0
 R_PROT_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI13_AXI_PWR_PROT_axi_clock_gated_en	PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI13_AXI_PWR_PROT_error_flag_en	PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI13_AXI_PWR_PROT_axi_clock_gated_en	PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI13_AXI_PWR_PROT_protect_idle
Type													RW	RW	RO	RO
Reset													0	1	0	1

Bit(s)	Name	Description
3	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI13_AXI_PWR_PROT_axi_clock_gated_en	
2	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI13_AXI_PWR_PROT_error_flag_en	
1	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI13_AXI_PWR_PROT_axi_clock_gated_en	
0	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_MISI2B_to_PERI_QAXI_AO_BUS_SI13_AXI_PWR_PROT_protect_idle	

1A080040 PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_SI12_to_QAXI_BUS_SI12_to_DEBUGSYS_DEBUGSYS_APB_S_SBUS2APB control register 0 00000057
S_APB_S_SBUS2APB_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_SI12_to_DEBUGSYS_APB_S_SBUS2APB_enable_slv_err_resp	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_SI12_to_DEBUGSYS_APB_S_SBUS2APB_ctrl_bypass	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_SI12_to_DEBUGSYS_APB_S_SBUS2APB_way_en	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_SI12_to_DEBUGSYS_APB_S_SBUS2APB_force_pready_high	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_SI12_to_DEBUGSYS_APB_S_SBUS2APB_ctrl_update_status	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_SI12_to_DEBUGSYS_APB_S_SBUS2APB_way_en_ready	PERI_QAXI_BUS_SI12_to_DEBUGSYS_APB_S_SBUS2APB_idle
Type										RW	RW	RW	RW	RO	RO	RO
Reset										1	0	1	0	1	1	1

Bit(s)	Name	Description
6	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_SI12_to_DEBUGSYS_APB_S_SBUS2APB_enable_slv_err_resp	
5	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_SI12_to_DEBUGSYS_APB_S_SBUS2APB_ctrl_bypass	
4	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_SI12_to_DEBUGSYS_APB_S_SBUS2APB_way_en	
3	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_SI12_to_DEBUGSYS_APB_S_SBUS2APB_force_pready_high	
2	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_SI12_to_DEBUGSYS_APB_S_SBUS2APB_ctrl_update_status	
1	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUS_SI12_to_DEBUGSYS_APB_S_SBUS2APB_way_en_ready	
0	PERI_QAXI_BUS_u_Ink_PERI_QAXI_BUSIdle Signal (Synchronous to Input Clock Domain) _SI12_to_DEBUGSYS_APB_S_SBUS2APB_s2p_idle	

1A080044

PERI_QAXI_BUS_u_SL22_CTR PERI_QAXI_BUS_u_SL22 control register 0

0000001F

L_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PERI_QAXI_BUS_u_SL22_in_arflush_thre		PERI_QAXI_BUS_u_SL22_in_awflush_thre		PERI_QAXI_BUS_u_SL22_axi_idle_out
Type												RW		RW		RO
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:3	PERI_QAXI_BUS_u_SL22_in_arflush_thre	
2:1	PERI_QAXI_BUS_u_SL22_in_awflush_thre	
0	PERI_QAXI_BUS_u_SL22_axi_idle_out	

1A080048 PERI_QAXI_BUS_u_MISI2A_C PERI_QAXI_BUS_u_MISI2A control register 0
TRL_0

0000001C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											PERI_QAXI_BUS_u_MISI2A_cg_disable	PERI_QAXI_BUS_u_MISI2A_PERI_QAXI_BUS_u_MISI2A_mi_outstanding_ext_end_en	PERI_QAXI_BUS_u_MISI2A_PERI_QAXI_BUS_u_MISI2A_mi_qos_on	PERI_QAXI_BUS_u_MISI2A_PERI_QAXI_BUS_u_MISI2A_mi_ctrl_updated	PERI_QAXI_BUS_u_MISI2A_PERI_QAXI_BUS_u_MISI2A_mi_r_busy	PERI_QAXI_BUS_u_MISI2A_PERI_QAXI_BUS_u_MISI2A_mi_w_busy
Type											RW	RW	RW	RO	RO	RO
Reset											0	1	1	1	0	0

Bit(s)	Name	Description
5	PERI_QAXI_BUS_u_MISI2A_cg_disable	
4	PERI_QAXI_BUS_u_MISI2A_PERI_QAXI_BUS_u_MISI2A_mi_outstanding_ext_end_en	
3	PERI_QAXI_BUS_u_MISI2A_PERI_QAXI_BUS_u_MISI2A_mi_qos_on	
2	PERI_QAXI_BUS_u_MISI2A_PERI_QAXI_BUS_u_MISI2A_mi_ctrl_updated	PERI_QAXI_BUS_u_MISI2A_mi master interface control signal updated status
1	PERI_QAXI_BUS_u_MISI2A_PERI_QAXI_BUS_u_MISI2A_mi_r_busy	PERI_QAXI_BUS_u_MISI2A_mi master interface read busy
0	PERI_QAXI_BUS_u_MISI2A_PERI_QAXI_BUS_u_MISI2A_mi_w_busy	PERI_QAXI_BUS_u_MISI2A_mi master interface write busy

1A08004C PERI_QAXI_BUS_u_MISI3A_C PERI_QAXI_BUS_u_MISI3A control register 0
TRL_0

0000001C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											PERI_QAXI_BUS_u_MISI3A_cg_disable	PERI_QAXI_BUS_u_MISI3A_MI Outstanding_end_en	PERI_QAXI_BUS_u_MISI3A_MI qos_on	PERI_QAXI_BUS_u_MISI3A_MI ctrl_updated	PERI_QAXI_BUS_u_MISI3A_MI r_busy	PERI_QAXI_BUS_u_MISI3A_MI w_busy
Type											RW	RW	RW	RO	RO	RO
Reset											0	1	1	1	0	0

Bit(s)	Name	Description
5	PERI_QAXI_BUS_u_MISI3A_cg_disable	
4	PERI_QAXI_BUS_u_MISI3A_MI Outstanding_end_en	
3	PERI_QAXI_BUS_u_MISI3A_MI qos_on	
2	PERI_QAXI_BUS_u_MISI3A_MI ctrl_updated	PERI_QAXI_BUS_u_MISI3A_mi master interface control signal updated status
1	PERI_QAXI_BUS_u_MISI3A_MI r_busy	PERI_QAXI_BUS_u_MISI3A_mi master interface read busy
0	PERI_QAXI_BUS_u_MISI3A_MI w_busy	PERI_QAXI_BUS_u_MISI3A_mi master interface write busy

1A080050 PERI_QAXI_BUS_u_MISI3_CTL PERI_QAXI_BUS_u_MISI3 control register 0

0001E001

RL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													PERI_QAXI_BUS_u_MISI3_cg_disable	PERI_QAXI_BUS_u_MISI3_si_ctrl_bypass	PERI_QAXI_BUS_u_MISI3_si_outstanding_disable	PERI_QAXI_BUS_u_MISI3_si_way_interleave_en
Type													RW	RW	RW	RW
Reset													0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_BUS_u_MISI3_si_way_interleave_en	PERI_QAXI_BUS_u_MISI3_si_way_interleave_en		PERI_QAXI_BUS_u_MISI3_si_dfslv_set_wirq	PERI_QAXI_BUS_u_MISI3_si_dfslv_set_rirq	PERI_QAXI_BUS_u_MISI3_si_b_chnl_sel			PERI_QAXI_BUS_u_MISI3_si_set_bid_miss	PERI_QAXI_BUS_u_MISI3_si_r_chnl_sel			PERI_QAXI_BUS_u_MISI3_si_set_rid_miss	PERI_QAXI_BUS_u_MISI3_si_rd_ot_busy	PERI_QAXI_BUS_u_MISI3_si_wr_ot_busy	PERI_QAXI_BUS_u_MISI3_si_ctrl_updated
Type	RW	RW		RO	RO	RO			RO	RO			RO	RO	RO	RO
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
19	PERI_QAXI_BUS_u_MISI3_cg_disable	
18	PERI_QAXI_BUS_u_MISI3_PERI_QAXI_BUS_u_MISI3_si_ctrl_bypass	Bypasses idle check when updating SI setting
17	PERI_QAXI_BUS_u_MISI3_PERI_QAXI_BUS_u_MISI3_si_outstanding_disable	PERI_QAXI_si_cabgen slave interface outstanding capability disable control
16:15	PERI_QAXI_BUS_u_MISI3_PERI_QAXI_BUS_u_MISI3_si_way_interleave_en	PERI_QAXI_BUS_u_MISI3_si slave interface read arbiter interleaving function enable control
14:13	PERI_QAXI_BUS_u_MISI3_PERI_QAXI_BUS_u_MISI3_si_dfslv_set_wirq	Control PERI_QAXI_BUS_u_MISI3_si address decode output path enable of each way
12	PERI_QAXI_BUS_u_MISI3_PERI_QAXI_BUS_u_MISI3_si_dfslv_set_rirq	PERI_QAXI_BUS_u_MISI3_si slave interface default slave write IRQ status
11	PERI_QAXI_BUS_u_MISI3_PERI_QAXI_BUS_u_MISI3_si_dfslv_set_rirq	PERI_QAXI_BUS_u_MISI3_si slave interface default slave read IRQ status
10:8	PERI_QAXI_BUS_u_MISI3_PERI_QAXI_BUS_u_MISI3_si_b_chnl_sel	PERI_QAXI_BUS_u_MISI3_si slave interface current write response channel way selection
7	PERI_QAXI_BUS_u_MISI3_PERI_QAXI_BUS_u_MISI3_si_set_bid_miss	PERI_QAXI_BUS_u_MISI3_si slave interface write response ID is missed status

Bit(s)	Name	Description
6:4	PERI_QAXI_BUS__u_MISI3__PERI_QAXI_BUS_u_MISI3_si_r_chnl_sel	PERI_QAXI_BUS_u_MISI3_si slave interface current read channel way selection
3	PERI_QAXI_BUS__u_MISI3__PERI_QAXI_BUS_u_MISI3_si_set_rid_miss	PERI_QAXI_BUS_u_MISI3_si slave interface Read ID is missed status
2	PERI_QAXI_BUS__u_MISI3__PERI_QAXI_BUS_u_MISI3_si_rd_ot_busy	PERI_QAXI_BUS_u_MISI3_si slave interface Read Channel Outstanding Busy
1	PERI_QAXI_BUS__u_MISI3__PERI_QAXI_BUS_u_MISI3_si_wr_ot_busy	PERI_QAXI_BUS_u_MISI3_si slave interface Write Channel Outstanding Busy
0	PERI_QAXI_BUS__u_MISI3__PERI_QAXI_BUS_u_MISI3_si_ctrl_updated	PERI_QAXI_BUS_u_MISI3_si slave interface control signal updated status

1A080054 PERI_QAXI_BUS_u_MISI2B_C PERI_QAXI_BUS_u_MISI2B control register 0
TRL_0

00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								PERI_QAXI_BUS_u_MISI2B_slv_set_wirq	PERI_QAXI_BUS_u_MISI2B_slv_set_rirq	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_si_b_chnl_sel						
Type								RO	RO	RO						
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_BUS_u_MISI2B_si_b_chnl_sel		PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_slv_set_wirq	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_si_r_chnl_sel							PERI_QAXI_BUS_u_MISI2B_slv_set_wirq	PERI_QAXI_BUS_u_MISI2B_slv_set_rirq	PERI_QAXI_BUS_u_MISI2B_slv_set_wirq	PERI_QAXI_BUS_u_MISI2B_slv_set_rirq	PERI_QAXI_BUS_u_MISI2B_slv_set_wirq	PERI_QAXI_BUS_u_MISI2B_slv_set_rirq
Type	RO		RO	RO							RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
24	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_slv_set_wirq	PERI_QAXI_BUS_u_MISI2B_si slave interface default slave write IRQ status
23	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_slv_set_rirq	PERI_QAXI_BUS_u_MISI2B_si slave interface default slave read IRQ status
22:14	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_si_b_chnl_sel	PERI_QAXI_BUS_u_MISI2B_si slave interface current write response channel way selection
13	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_slv_set_wirq	PERI_QAXI_BUS_u_MISI2B_si slave interface write response ID is missed status
12:4	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_si_r_chnl_sel	PERI_QAXI_BUS_u_MISI2B_si slave interface current read channel way selection
3	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_slv_set_rirq	PERI_QAXI_BUS_u_MISI2B_si slave interface Read ID is missed status
2	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_slv_set_wirq	PERI_QAXI_BUS_u_MISI2B_si slave interface Read Channel Outstanding Busy
1	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_slv_set_rirq	PERI_QAXI_BUS_u_MISI2B_si slave interface Write Channel Outstanding Busy
0	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_slv_set_wirq	PERI_QAXI_BUS_u_MISI2B_si slave interface control signal updated status

Bit(s)	Name	Description

1A080058 PERI_QAXI_BUS_u_MISI2B_C PERI_QAXI_BUS_u_MISI2B control register 1 0000FFFF

TRL 1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														PERI_QAXI_BUS_u_MISI2B_C_g_disable	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_si_ctrl_bypass	PERI_QAXI_BUS_u_MISI2B_si_outstanding_disable
Type														RW	RW	RW
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_si_way_interleave_en								PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_si_way_en							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
18	PERI_QAXI_BUS_u_MISI2B_C_g_disable	
17	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_si_ctrl_bypass	Bypasses idle check when updating SI setting
16	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_si_outstanding_disable	si_cabgen slave interface outstanding capability disable control
15:8	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_si_way_interleave_en	PERI_QAXI_BUS_u_MISI2B_si slave interface read arbiter interleaving function enable control
7:0	PERI_QAXI_BUS_u_MISI2B_PERI_QAXI_BUS_u_MISI2B_si_way_en	Control PERI_QAXI_BUS_u_MISI2B_si address decode output path enable of each way

1A08005C

PERI_QAXI_BUS_u_SI12_CTRLPERI_QAXI_BUS_u_SI12 control register 0
0

00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PERI_QAXI_BUS_u_SI12_enable_slv_err_resp	PERI_QAXI_BUS_u_SI12_wfifo_threshold	
Type														RW	RW	
Reset														1	0	0

Bit(s)	Name	Description
2	PERI_QAXI_BUS_u_SI12_enable_slv_err_resp	
1:0	PERI_QAXI_BUS_u_SI12_wfifo_threshold	

1A080060

PERI_QAXI_BUS_u_SI19_CTRLPERI_QAXI_BUS_u_SI19 control register 0
_0

0001FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PERI_QAXI_BUS_u_SI19_force_pready_high															PERI_QAXI_BUS_u_SI19_ctrl_update_status
Type	RW															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_BUS_u_SI19_way_en_ready															PERI_QAXI_BUS_u_SI19_s2p_idle
Type	RO															RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:17	PERI_QAXI_BUS_u_SI19_force_pready_high	
16	PERI_QAXI_BUS_u_SI19_ctrl_update_status	
15:1	PERI_QAXI_BUS_u_SI19_way_en_ready	
0	PERI_QAXI_BUS_u_SI19_s2p_idle	Idle Signal (Synchronous to Input Clock Domain)

1A080064

PERI_QAXI_BUS_u_SI19_CTRL PERI_QAXI_BUS_u_SI19 control register 1

00017FFF

1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PERI_QAXI_BUS_u_SI19_enable_slv_err_resp
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_BUS_u_SI19_ctrl_bypass	PERI_QAXI_BUS_u_SI19_way_en														
Type	RW	RW														
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
16	PERI_QAXI_BUS_u_SI19_enable_slv_err_resp	
15	PERI_QAXI_BUS_u_SI19_ctrl_bypass	
14:0	PERI_QAXI_BUS_u_SI19_way_en	

1A080068 PERI_QAXI_AHB_BUS_u_Ink_PERI_QAXI_AHB_BUS_u_Ink_PWM_M_to_PERI_PWM_M_to_PERI_QAXI_AHB_QAXI_AHB_BUS_MI18_AHB_M_QOS_REPLACE_BUS_MI18_AHB_M_QOS_REPLACE control register 0
PLACE_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PERI_QAXI_AHB_BUS_u_Ink_PWM_M_to_PERI_QAXI_AHB_BUS_MI18_AHB_M_QOS_REPLACE_reg_flush	PERI_QAXI_AHB_BUS_u_Ink_PWM_M_to_PERI_QAXI_AHB_BUS_MI18_AHB_M_QOS_REPLACE_reg_ultra		
Type													RW	RW		
Reset													0	0	0	0

Bit(s)	Name	Description
3:2	PERI_QAXI_AHB_BUS_u_Ink_PWM_M_to_PERI_QAXI_AHB_BUS_MI18_AHB_M_QOS_REPLACE_reg_flush	This is to replace AHBM Flush QoS for PWM_M
1:0	PERI_QAXI_AHB_BUS_u_Ink_PWM_M_to_PERI_QAXI_AHB_BUS_MI18_AHB_M_QOS_REPLACE_reg_ultra	This is to replace AHBM Ultra QoS for PWM_M

1A08006C PERI_QAXI_AHB_BUS_u_Ink_PERI_QAXI_AHB_BUS_u_Ink_AUDIO_M_to_PERI_AUDIO_M_to_PERI_QAXI_AHB_QAXI_AHB_BUS_MI18_AHB_M_QOS_REPLACE_B_BUS_MI18_AHB_M_QOS_Rcontrol register 0 00000000
EPLACE_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PERI_QAXI_AHB_BUS_u_Ink_AUDIO_M_to_PERI_QAXI_AHB_BUS_MI18_AHB_M_QOS_REPLACE_reg_flush	PERI_QAXI_AHB_BUS_u_Ink_AUDIO_M_to_PERI_QAXI_AHB_BUS_MI18_AHB_M_QOS_REPLACE_reg_ultra		
Type													RW	RW		
Reset													0	0	0	0

Bit(s)	Name	Description
3:2	PERI_QAXI_AHB_BUS_u_Ink_AUDIO_M_to_PERI_QAXI_AHB_BUS_MI18_AHB_M_QOS_REPLACE_reg_flush	This is to replace AHBM Flush QoS for AUDIO_M
1:0	PERI_QAXI_AHB_BUS_u_Ink_AUDIO_M_to_PERI_QAXI_AHB_BUS_MI18_AHB_M_QOS_REPLACE_reg_ultra	This is to replace AHBM Ultra QoS for AUDIO_M

1A080070 PERI_QAXI_AHB_BUS_u_MI18 PERI_QAXI_AHB_BUS_u_MI18 control register 0
8_CTRL_0

010001F8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								PERI_QAXI_AHB_BUS_u_MI18_error_flag_en	PERI_QAXI_AHB_BUS_u_MI18_reg_qos_en	PERI_QAXI_AHB_BUS_u_MI18_reg_prot_mode		PERI_QAXI_AHB_BUS_u_MI18_reg_mas_lim_gnt_cnt				
Type								RW	RW	RW		RW				
Reset								1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_AHB_BUS_u_MI18_reg_mas_lim_gnt_cnt			PERI_QAXI_AHB_BUS_u_MI18_reg_gntcnt_sel	PERI_QAXI_AHB_BUS_u_MI18_reg_filter_len_sel		PERI_QAXI_AHB_BUS_u_MI18_reg_bw_lim_en	PERI_QAXI_AHB_BUS_u_MI18_reg_slave_way_en	PERI_QAXI_AHB_BUS_u_MI18_reg_master_req_en		PERI_QAXI_AHB_BUS_u_MI18_ahb_bus_layer_idle	PERI_QAXI_AHB_BUS_u_MI18_ctrl_update_status		PERI_QAXI_AHB_BUS_u_MI18_hmaster_ser_s		
Type	RW			RW	RW		RW	RW	RW		RO	RO		RO		
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0

Bit(s)	Name	Description
24	PERI_QAXI_AHB_BUS_u_MI18_error_flag_en	
23	PERI_QAXI_AHB_BUS_u_MI18_reg_qos_en	
22:21	PERI_QAXI_AHB_BUS_u_MI18_reg_prot_mode	
20:13	PERI_QAXI_AHB_BUS_u_MI18_reg_mas_lim_gnt_cnt	
12	PERI_QAXI_AHB_BUS_u_MI18_reg_gntcnt_sel	
11:10	PERI_QAXI_AHB_BUS_u_MI18_reg_filter_len_sel	
9	PERI_QAXI_AHB_BUS_u_MI18_reg_bw_lim_en	
8	PERI_QAXI_AHB_BUS_u_MI18_reg_slave_way_en	
7:6	PERI_QAXI_AHB_BUS_u_MI18_reg_master_req_en	
5	PERI_QAXI_AHB_BUS_u_MI18_ahb_bus_layer_idle	
4:3	PERI_QAXI_AHB_BUS_u_MI18_ctrl_update_status	
2:0	PERI_QAXI_AHB_BUS_u_MI18_hmaster_ser_s	

Bit(s)	Name	Description

Module name: bcrn_PERI_PDN2_wrapper_u_bcrn_PERI_PDN2_bcrn Base address: (+0x1A09_0000)

Address	Name	Width	Register Function
1A090000	<u>PERI_QAXI_BUS_SUB2_u_Ink</u> <u>PERI_QAXI_BUS_SUB2_SI17_t</u> <u>o_CQ_DMA_APB_S_S2F_CTRL_0</u>	32	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_S I17_to_CQ_DMA_APB_S_S2F control register 0
1A090004	<u>PERI_QAXI_BUS_SUB2_u_Ink</u> <u>PERI_QAXI_BUS_SUB2_SI17_t</u> <u>o_INFRACFG_MEM_APB_S_A</u> <u>SYNC_CTRL_0</u>	32	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_S I17_to_INFRACFG_MEM_APB_S_ASYNC control register 0
1A090008	<u>PERI_QAXI_BUS_SUB2_u_Ink</u> <u>PERI_QAXI_BUS_SUB2_SI17B</u> <u>to_EMI_FAKE_ENGINE_0_APB_S</u> <u>ASYNC_CTRL_0</u>	32	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_S I17B_to_EMI_FAKE_ENGINE_0_APB_S_ASYNC control register 0
1A09000C	<u>PERI_QAXI_BUS_SUB2_u_Ink</u> <u>PERI_QAXI_BUS_SUB2_SI17B</u> <u>to_EMI_FAKE_ENGINE_1_APB_S</u> <u>ASYNC_CTRL_0</u>	32	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_S I17B_to_EMI_FAKE_ENGINE_1_APB_S_ASYNC control register 0
1A090010	<u>PERI_QAXI_BUS_SUB2_u_Ink</u> <u>PERI_QAXI_BUS_SUB2_SI17B</u> <u>to_BCRM_FMEM_PDN_APB_S</u> <u>ASYNC_CTRL_0</u>	32	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_S I17B_to_BCRM_FMEM_PDN_APB_S_ASYNC control register 0
1A090014	<u>PERI_QAXI_BUS_SUB2_u_SI12</u> <u>B_CTRL_0</u>	32	PERI_QAXI_BUS_SUB2_u_SI12B control register 0
1A090018	<u>PERI_QAXI_BUS_SUB2_u_SI17</u> <u>CTRL_0</u>	32	PERI_QAXI_BUS_SUB2_u_SI17 control register 0
1A09001C	<u>PERI_QAXI_BUS_SUB2_u_SI17</u> <u>B_CTRL_0</u>	32	PERI_QAXI_BUS_SUB2_u_SI17B control register 0

1A090000 PERI_QAXI_BUS_SUB2_u_Ink PERI_QAXI_BUS_SUB2_u_Ink PERI_QAXI_BUS_S 00000003
 PERI_QAXI_BUS_SUB2_SI17_UB2_SI17_to_CQ_DMA_APB_S_S2F control
 to_CQ_DMA_APB_S_S2F_CT register 0
 RL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17_to_CQ_DMA_APB_S_S2F_rx_clock_cg_en	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17_to_CQ_DMA_APB_S_S2F_error_flag_en
Type															RW	RW
Reset															1	1

Bit(s)	Name	Description
1	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17_to_CQ_DMA_APB_S_S2F_rx_clock_cg_en	
0	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17_to_CQ_DMA_APB_S_S2F_error_flag_en	Enables error flag. Controls time-out counter

1A090004 PERI_QAXI_BUS_SUB2_u_Ink PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_S 00000003
 PERI_QAXI_BUS_SUB2_SI17 UB2_SI17_to_INFRACFG_MEM_APB_S_ASYNC
 to_INFRACFG_MEM_APB_S control register 0
 ASYNC_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17_to_INFRACFG_MEM_APB_S_ASYNC_rx_clock_cg_en	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17_to_INFRACFG_MEM_APB_S_ASYNC_error_flag_en
Type															RW	RW
Reset															1	1

Bit(s)	Name	Description
1	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17_to_INFRACFG_MEM_APB_S_ASYNC_rx_clock_cg_en	
0	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17_to_INFRACFG_MEM_APB_S_ASYNC_error_flag_en	Enables error flag. Controls time-out counter

1A090008 PERI_QAXI_BUS_SUB2_u_Ink PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_S 00000003
 PERI_QAXI_BUS_SUB2_SI17_UB2_SI17B_to_EMI_FAKE_ENGINE_0_APB_S_AS
 B_to_EMI_FAKE_ENGINE_0_ASYNC control register 0
 PB_S_ASYNC_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17_UB2_SI17B_to_EMI_FAKE_ENGINE_0_APB_S_AS_ASYNC_rx_clock_cg_en	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17_UB2_SI17B_to_EMI_FAKE_ENGINE_0_APB_S_AS_ASYNC_error_flag_en
Type															RW	RW
Reset															1	1

Bit(s)	Name	Description
1	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17_UB2_SI17B_to_EMI_FAKE_ENGINE_0_APB_S_ASYNC_rx_clock_cg_en	
0	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17_UB2_SI17B_to_EMI_FAKE_ENGINE_0_APB_S_ASYNC_error_flag_en	Enables error flag. Controls time-out counter

1A09000C PERI_QAXI_BUS_SUB2_u_Ink PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_S 00000003
 PERI_QAXI_BUS_SUB2_SI17_UB2_SI17B_to_EMI_FAKE_ENGINE_1_APB_S_AS
 B_to_EMI_FAKE_ENGINE_1_ASYNC control register 0
 PB_S_ASYNC_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17_UB2_SI17B_to_EMI_FAKE_ENGINE_1_APB_S_AS_ASYNC_rx_clock_cg_en	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17_UB2_SI17B_to_EMI_FAKE_ENGINE_1_APB_S_AS_ASYNC_error_flag_en
Type															RW	RW
Reset															1	1

Bit(s)	Name	Description
1	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17_UB2_SI17B_to_EMI_FAKE_ENGINE_1_APB_S_ASYNC_rx_clock_cg_en	
0	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17_UB2_SI17B_to_EMI_FAKE_ENGINE_1_APB_S_ASYNC_error_flag_en	Enables error flag. Controls time-out counter

1A090010 PERI_QAXI_BUS_SUB2_u_Ink PERI_QAXI_BUS_SUB2_u_Ink PERI_QAXI_BUS_S 00000003
 PERI_QAXI_BUS_SUB2_SI17 UB2_SI17B_to_BCRM_FMEM_PDN_APB_S_ASYNC
 B to BCRM_FMEM_PDN_APB C control register 0
 B S_ASYNC_CTRL_0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17B_to_BCRM_FMEM_PDN_APB_S_ASYNC_rx_clock_cg_en	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17B_to_BCRM_FMEM_PDN_APB_S_ASYNC_error_flag_en
Type															RW	RW
Reset															1	1

Bit(s)	Name	Description
1	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17B_to_BCRM_FMEM_PDN_APB_S_ASYNC_rx_clock_cg_en	
0	PERI_QAXI_BUS_SUB2_u_Ink_PERI_QAXI_BUS_SUB2_SI17B_to_BCRM_FMEM_PDN_APB_S_ASYNC_error_flag_en	Enables error flag. Controls time-out counter

1A090014 PERI_QAXI_BUS_SUB2_u_SI1 PERI_QAXI_BUS_SUB2_u_SI12B control register 00000004
 2B_CTRL_0 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PERI_QAXI_BUS_SUB2_u_SI12B_enable_slv_err_resp	PERI_QAXI_BUS_SUB2_u_SI12B_wfifo_threshold	
Type														RW	RW	
Reset														1	0	0

Bit(s)	Name	Description
2	PERI_QAXI_BUS_SUB2_u_SI12B_enable_slv_err_resp	
1:0	PERI_QAXI_BUS_SUB2_u_SI12B_wfifo_threshold	

1A090018 PERI_QAXI_BUS_SUB2_u_SI1 PERI_QAXI_BUS_SUB2_u_SI17 control register 0
7_CTRL_0

0BFC03FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					PERI_QAXI_BUS_SUB2_u_SI17_enable_slv_err_resp	PERI_QAXI_BUS_SUB2_u_SI17_ctrl_bypass	PERI_QAXI_BUS_SUB2_u_SI17_way_en								PERI_QAXI_BUS_SUB2_u_SI17_force_pready_high	
Type					RW	RW	RW								RW	
Reset					1	0	1	1	1	1	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_BUS_SUB2_u_SI17_force_pready_high						PERI_QAXI_BUS_SUB2_u_SI17_ctrl_update_status	PERI_QAXI_BUS_SUB2_u_SI17_way_en_ready								PERI_QAXI_BUS_SUB2_u_SI17_s2p_idle
Type	RW						RO	RO								RO
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27	PERI_QAXI_BUS_SUB2_u_SI17_enable_slv_err_resp	
26	PERI_QAXI_BUS_SUB2_u_SI17_ctrl_bypass	
25:18	PERI_QAXI_BUS_SUB2_u_SI17_way_en	
17:10	PERI_QAXI_BUS_SUB2_u_SI17_force_pready_high	
9	PERI_QAXI_BUS_SUB2_u_SI17_ctrl_update_status	
8:1	PERI_QAXI_BUS_SUB2_u_SI17_way_en_ready	
0	PERI_QAXI_BUS_SUB2_u_SI17_s2p_idle	Idle signal (Synchronous to Input Clock Domain)

1A09001C PERI_QAXI_BUS_SUB2_u_SI1 PERI_QAXI_BUS_SUB2_u_SI17B control register 0BFC03FF
7B_CTRL_0 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					PERI_QAXI_BUS_SUB2_u_SI17B_enable_slv_err_resp	PERI_QAXI_BUS_SUB2_u_SI17B_ctrl_bypass	PERI_QAXI_BUS_SUB2_u_SI17B_way_en								PERI_QAXI_BUS_SUB2_u_SI17B_force_pready_high	
Type					RW	RW	RW								RW	
Reset					1	0	1	1	1	1	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PERI_QAXI_BUS_SUB2_u_SI17B_force_pready_high						PERI_QAXI_BUS_SUB2_u_SI17B_ctrl_update_status	PERI_QAXI_BUS_SUB2_u_SI17B_way_en_ready								PERI_QAXI_BUS_SUB2_u_SI17B_s2p_idle
Type	RW						RO	RO								RO
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
27	PERI_QAXI_BUS_SUB2_u_SI17B_enable_slv_err_resp	
26	PERI_QAXI_BUS_SUB2_u_SI17B_ctrl_bypass	
25:18	PERI_QAXI_BUS_SUB2_u_SI17B_way_en	
17:10	PERI_QAXI_BUS_SUB2_u_SI17B_force_pready_high	
9	PERI_QAXI_BUS_SUB2_u_SI17B_ctrl_update_status	
8:1	PERI_QAXI_BUS_SUB2_u_SI17B_way_en_ready	
0	PERI_QAXI_BUS_SUB2_u_SI17B_s2p_idle	Idle signal (Synchronous to Input Clock Domain)

1.2 External Interrupt Controller

1.2.1 Register Definition

Module name: ap_cirq_eint Base address: (+0x1000_B000)

Address	Name	Width	Register Function
1000B000	<u>EINT_STA0</u>	32	External interrupt status register
1000B004	<u>EINT_STA1</u>	32	External interrupt status register
1000B008	<u>EINT_STA2</u>	32	External interrupt status register
1000B040	<u>EINT_ACK0</u>	32	External interrupt acknowledge register
1000B044	<u>EINT_ACK1</u>	32	External interrupt acknowledge register
1000B048	<u>EINT_ACK2</u>	32	External interrupt acknowledge register
1000B080	<u>EINT_MASK0</u>	32	External interrupt mask register
1000B084	<u>EINT_MASK1</u>	32	External interrupt mask register
1000B088	<u>EINT_MASK2</u>	32	External interrupt mask register
1000B0C0	<u>EINT_MASK_SET0</u>	32	External interrupt mask set register
1000B0C4	<u>EINT_MASK_SET1</u>	32	External interrupt mask set register
1000B0C8	<u>EINT_MASK_SET2</u>	32	External interrupt mask set register
1000B100	<u>EINT_MASK_CLR0</u>	32	External interrupt mask clear register
1000B104	<u>EINT_MASK_CLR1</u>	32	External interrupt mask clear register
1000B108	<u>EINT_MASK_CLR2</u>	32	External interrupt mask clear register
1000B140	<u>EINT_SENS0</u>	32	External interrupt sensitivity register
1000B144	<u>EINT_SENS1</u>	32	External interrupt sensitivity register
1000B148	<u>EINT_SENS2</u>	32	External interrupt sensitivity register
1000B180	<u>EINT_SENS_SET0</u>	32	External interrupt sensitivity set register
1000B184	<u>EINT_SENS_SET1</u>	32	External interrupt sensitivity set register
1000B188	<u>EINT_SENS_SET2</u>	32	External interrupt sensitivity set register
1000B1C0	<u>EINT_SENS_CLR0</u>	32	External interrupt sensitivity clear register
1000B1C4	<u>EINT_SENS_CLR1</u>	32	External interrupt sensitivity clear register
1000B1C8	<u>EINT_SENS_CLR2</u>	32	External interrupt sensitivity clear register
1000B200	<u>EINT_SOFT0</u>	32	Software interrupt register
1000B204	<u>EINT_SOFT1</u>	32	Software interrupt register
1000B208	<u>EINT_SOFT2</u>	32	Software interrupt register
1000B240	<u>EINT_SOFT_SET0</u>	32	Software interrupt set register
1000B244	<u>EINT_SOFT_SET1</u>	32	Software interrupt set register
1000B248	<u>EINT_SOFT_SET2</u>	32	Software interrupt set register
1000B280	<u>EINT_SOFT_CLR0</u>	32	Software interrupt clear register
1000B284	<u>EINT_SOFT_CLR1</u>	32	Software interrupt clear register
1000B288	<u>EINT_SOFT_CLR2</u>	32	Software interrupt clear register
1000B300	<u>EINT_POLO</u>	32	External interrupt polarity register
1000B304	<u>EINT_POL1</u>	32	External interrupt polarity register
1000B308	<u>EINT_POL2</u>	32	External interrupt polarity register
1000B340	<u>EINT_POL_SET0</u>	32	External interrupt polarity set register
1000B344	<u>EINT_POL_SET1</u>	32	External interrupt polarity set register
1000B348	<u>EINT_POL_SET2</u>	32	External interrupt polarity set register
1000B380	<u>EINT_POL_CLR0</u>	32	External interrupt polarity clear register
1000B384	<u>EINT_POL_CLR1</u>	32	External interrupt polarity clear register
1000B388	<u>EINT_POL_CLR2</u>	32	External interrupt polarity clear register
1000B400	<u>EINT_DOENO</u>	32	Domain 0 external interrupt enable control register

Address	Name	Width	Register Function
1000B404	<u>EINT_D0EN1</u>	32	Domain 0 external interrupt enable control register
1000B408	<u>EINT_D0EN2</u>	32	Domain 0 external interrupt enable control register
1000B500	<u>EINT_DBNC_3_0</u>	32	External interrupt debounce control register
1000B600	<u>EINT_DBNC_SET_3_0</u>	32	External interrupt debounce control register
1000B700	<u>EINT_DBNC_CLR_3_0</u>	32	External interrupt debounce control register
1000B800	<u>EINT_EVENT_MASK0</u>	32	External interrupt event mask register
1000B840	<u>EINT_EVENT_MASK_SET0</u>	32	External interrupt event mask set register
1000B880	<u>EINT_EVENT_MASK_CLR0</u>	32	External interrupt event mask clear register
1000B900	<u>DEINT_CON0</u>	32	Directly-coupled EINT control register
1000B940	<u>DEINT_SELO</u>	32	Directly-coupled EINT select register
1000B980	<u>DEINT_SEL_SET0</u>	32	Directly-coupled EINT select set register
1000B9C0	<u>DEINT_SEL_CLR0</u>	32	Directly-coupled EINT select clear register
1000B9F0	<u>EINT_EEVT</u>	32	EINT wake-up event status register
1000BA00	<u>EINT_RAW_STA0</u>	32	External interrupt raw status register
1000BA04	<u>EINT_RAW_STA1</u>	32	External interrupt raw status register
1000BA08	<u>EINT_RAW_STA2</u>	32	External interrupt raw status register
1000BC00	<u>EINT_SYNC_EN0</u>	32	External interrupt sync enable register
1000BD00	<u>EINT_SYNC_EN_SET_0</u>	32	External interrupt sync enable set register
1000BE00	<u>EINT_SYNC_EN_CLR_0</u>	32	External interrupt sync enable clear register
1000BF00	<u>FPGA_EMUL_0</u>	32	FPGA emulation register 0
1000BB00	<u>SECURE_EINT_EN0</u>	32	Secure EINT enable
1000BB10	<u>SECURE_DIR_EINT_EN</u>	32	Secure direct EINT enable
1000BB20	<u>DCM_ON</u>	32	DCM enable
1000BB30	<u>SECURE_STATUS</u>	32	Secure status
1000BC20	<u>EINT_SYS_TIMER_LATCH_CTL</u>	32	EINT system timer latch control
1000BC24	<u>EINT_SYS_TIMER_LATCH0_L</u>	32	EINT system timer latch 0 - low
1000BC28	<u>EINT_SYS_TIMER_LATCH0_H</u>	32	EINT system timer latch 0 - high
1000BC2C	<u>EINT_SYS_TIMER_LATCH1_L</u>	32	EINT system timer latch 1 - low
1000BC30	<u>EINT_SYS_TIMER_LATCH1_H</u>	32	EINT system timer latch 1 - high
1000BC34	<u>EINT_SYS_TIMER_LATCH2_L</u>	32	EINT system timer latch 2 - low
1000BC38	<u>EINT_SYS_TIMER_LATCH2_H</u>	32	EINT system timer latch 2 - high
1000BD20	<u>EINT_SYS_TIMER_IRQ_SRC_SEL_0</u>	32	EINT system timer IRQ SRC selection
1000B504	<u>EINT_DBNC_7_4</u>	32	External interrupt debounce control register
1000B604	<u>EINT_DBNC_SET_7_4</u>	32	External interrupt debounce control register
1000B704	<u>EINT_DBNC_CLR_7_4</u>	32	External interrupt debounce control register
1000B508	<u>EINT_DBNC_B_8</u>	32	External interrupt debounce control register
1000B608	<u>EINT_DBNC_SET_B_8</u>	32	External interrupt debounce control register
1000B708	<u>EINT_DBNC_CLR_B_8</u>	32	External interrupt debounce control register
1000B50C	<u>EINT_DBNC_F_C</u>	32	External interrupt debounce control register
1000B60C	<u>EINT_DBNC_SET_F_C</u>	32	External interrupt debounce control register
1000B70C	<u>EINT_DBNC_CLR_F_C</u>	32	External interrupt debounce control register

1000B000 **EINT_STA0** **External interrupt status register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_PEND	Each bit indicates the corresponding external interrupt status. Reading 1 means the interrupt is pending.

1000B004 **EINT_STA1** **External interrupt status register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_PEND	Each bit indicates the corresponding external interrupt status. Reading 1 means the interrupt is pending.

1000B008 EINT_STA2 External interrupt status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_PEND	Each bit indicates the corresponding external interrupt status. Reading 1 means the interrupt is pending.

1000B040 EINT_ACK0 External interrupt acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_ACK	Write 1 to specific bit to acknowledge the corresponding external interrupt.

1000B044 **EINT_ACK1** **External interrupt acknowledge register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_ACK	Write 1 to specific bit to acknowledge the corresponding external interrupt.

1000B048 **EINT_ACK2** **External interrupt acknowledge register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_ACK	Write 1 to specific bit to acknowledge the corresponding external interrupt.

100B080 **EINT_MASK0** **External interrupt mask register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	EINT_MASK	External interrupt mask value

100B084 **EINT_MASK1** **External interrupt mask register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	EINT_MASK	External interrupt mask value

100B088 **EINT_MASK2** **External interrupt mask register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	EINT_MASK	External interrupt mask value

100B0C0 **EINT_MASK_SET0** **External interrupt mask set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_MASK_SET	Write 1 to specific bit to set the mask of corresponding external interrupt.

100B0C4 **EINT_MASK_SET1** **External interrupt mask set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_MASK_SET	Write 1 to specific bit to set the mask of corresponding external interrupt.

100B0C8 **EINT_MASK_SET2** **External interrupt mask set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_MASK_SET	Write 1 to specific bit to set the mask of corresponding external interrupt.

1000B100 **EINT_MASK_CLR0** **External interrupt mask clear register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_MASK_CLR	Write 1 to specific bit to clear the mask of corresponding external interrupt.

1000B104 **EINT_MASK_CLR1** **External interrupt mask clear register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_MASK_CLR	Write 1 to specific bit to clear the mask of corresponding external interrupt.

1000B108 **EINT_MASK_CLR2** **External interrupt mask clear register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_MASK_CLR	Write 1 to specific bit to clear the mask of corresponding external interrupt.

1000B140 **EINT_SENS0** **External interrupt sensitivity register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	EINT_SENS	External interrupt sensitivity value

1000B144 **EINT_SENS1** **External interrupt sensitivity register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	EINT_SENS	External interrupt sensitivity value

1000B148 **EINT_SENS2** **External interrupt sensitivity register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	EINT_SENS	External interrupt sensitivity value

1000B180 EINT_SENS_SET0 External interrupt sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_SENS_SET	Write 1 to specific bit to set the sensitivity of corresponding external interrupt.

1000B184 EINT_SENS_SET1 External interrupt sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_SENS_SET	Write 1 to specific bit to set the sensitivity of corresponding external interrupt.

1000B188 EINT_SENS_SET2 External interrupt sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_SENS_SET	Write 1 to specific bit to set the sensitivity of corresponding external interrupt.

1000B1C0 EINT_SENS_CLR0 External interrupt sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_SENS_CLR	Write 1 to specific bit to clear the sensitivity of corresponding external interrupt.

1000B1C4 **EINT_SENS_CLR1** **External interrupt sensitivity clear register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_SENS_CLR	Write 1 to specific bit to clear the sensitivity of corresponding external interrupt.

1000B1C8 **EINT_SENS_CLR2** **External interrupt sensitivity clear register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_SENS_CLR	Write 1 to specific bit to clear the sensitivity of corresponding external interrupt.

1000B200 **EINT_SOFT0** **Software interrupt register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_SOFT	Software interrupt value

1000B204 **EINT_SOFT1** **Software interrupt register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_SOFT	Software interrupt value

1000B208 **EINT_SOFT2** **Software interrupt register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_SOFT	Software interrupt value

1000B240 **EINT_SOFT_SET0** **Software interrupt set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_SOFT_SET	Write 1 to specific bit to set the corresponding software interrupt.

1000B244 **EINT_SOFT_SET1** **Software interrupt set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_SOFT_SET	Write 1 to specific bit to set the corresponding software interrupt.

1000B248 **EINT_SOFT_SET2** **Software interrupt set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_SOFT_SET	Write 1 to specific bit to set the corresponding software interrupt.

1000B280 **EINT_SOFT_CLR0** **Software interrupt clear register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_SOFT_CLR	Write 1 to specific bit to clear the corresponding software interrupt.

1000B284 **EINT_SOFT_CLR1** **Software interrupt clear register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_SOFT_CLR	Write 1 to specific bit to clear the corresponding software interrupt.

1000B288 **EINT_SOFT_CLR2** **Software interrupt clear register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_SOFT_CLR	Write 1 to specific bit to clear the corresponding software interrupt.

1000B300 **EINT_POL0** **External interrupt polarity register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_POL	External interrupt polarity value

1000B304 **EINT_POL1** **External interrupt polarity register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_POL	External interrupt polarity value

1000B308 **EINT_POL2** **External interrupt polarity register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_POL	External interrupt polarity value

1000B340 **EINT_POL_SET0** **External interrupt polarity set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_POL_SET	Write 1 to specific bit to set the polarity of corresponding external interrupt.

1000B344 **EINT_POL_SET1** **External interrupt polarity set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_POL_SET	Write 1 to specific bit to set the polarity of corresponding external interrupt.

1000B348 **EINT_POL_SET2** **External interrupt polarity set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_POL_SET	Write 1 to specific bit to set the polarity of corresponding external interrupt.

1000B380 **EINT_POL_CLR0** **External interrupt polarity clear register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_POL_CLR	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

1000B384 **EINT_POL_CLR1** **External interrupt polarity clear register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_POL_CLR	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

1000B388 **EINT_POL_CLR2** **External interrupt polarity clear register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_POL_CLR	Write 1 to specific bit to clear the polarity of corresponding external interrupt.

1000B400 **EINT_DOEN0** **Domain 0 external interrupt enable control** **00000000**
register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DOEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DOEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_DOEN	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

1000B404 **EINT_DOEN1** **Domain 0 external interrupt enable control** **00000000**
register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DOEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DOEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_DOEN	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

1000B408

EINT_DOEN2Domain 0 external interrupt enable control
register

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DOEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DOEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_DOEN	Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.

100B500 EINT_DBNC 3 0 External interrupt debounce control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING3						DBNC_RST3	EN3	DBNC_SETTING2						DBNC_RST2	EN2
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING1						DBNC_RST1	EN1	DBNC_SETTING0						DBNC_RST0	EN0
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Name	Description
31:28	DBNC_SETTING3	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
25	DBNC_RST3	Resets debounce counter 0: Negative 1: Positive
24	EN3	Enables debounce function 0: Disable 1: Enable
23:20	DBNC_SETTING2	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms

Bit(s)	Name	Description
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
17	DBNC_RST2	Resets debounce counter
		0: Negative
		1: Positive
16	EN2	Enables debounce function
		0: Disable
		1: Enable
15:12	DBNC_SETTING1	Debounce setting
		0000: 0.125 ms
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
9	DBNC_RST1	Resets debounce counter
		0: Negative
		1: Positive
8	EN1	Enables debounce function
		0: Disable
		1: Enable
7:4	DBNC_SETTING0	Debounce setting
		0000: 0.125 ms

Bit(s)	Name	Description
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
1	DBNC_RST0	Resets debounce counter
		0: Negative
		1: Positive
0	ENO	Enables debounce function
		0: Disable
		1: Enable

1000B600 EINT_DBNC_SET_3_0 External interrupt debounce control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET3						DBNC_RST_SET3	EN_SET3	DBNC_SETTING_SET2						DBNC_RST_SET2	EN_SET2
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET1						DBNC_RST_SET1	EN_SET1	DBNC_SETTING_SET0						DBNC_RST_SET0	EN_SET0
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Name	Description
31:28	DBNC_SETTING_SET3	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
25	DBNC_RST_SET3	Resets debounce counter 0: Negative 1: Positive
24	EN_SET3	Enables debounce function 0: Disable 1: Enable
23:20	DBNC_SETTING_SET2	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms

Bit(s)	Name	Description
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
17	DBNC_RST_SET2	Resets debounce counter
		0: Negative
		1: Positive
16	EN_SET2	Enables debounce function
		0: Disable
		1: Enable
15:12	DBNC_SETTING_SET1	Debounce setting
		0000: 0.125 ms
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
9	DBNC_RST_SET1	Resets debounce counter
		0: Negative
		1: Positive
8	EN_SET1	Enables debounce function
		0: Disable
		1: Enable
7:4	DBNC_SETTING_SET0	Debounce setting

Bit(s)	Name	Description
		0000: 0.125 ms
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
1	DBNC_RST_SET0	Resets debounce counter
		0: Negative
		1: Positive
0	EN_SET0	Enables debounce function
		0: Disable
		1: Enable

1000B700 EINT_DBNC_CLR_3_0 External interrupt debounce control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR3						DBNC_RST3	EN_CLR3	DBNC_SETTING_CLR_CLR2						DBNC_RST2	EN_CLR2
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR1						DBNC_RST1	EN_CLR1	DBNC_SETTING_CLR_CLR0						DBNC_RST0	EN_CLR0
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Name	Description
31:28	DBNC_SETTING_CLR_CLR3	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
25	DBNC_RST3	Resets debounce counter 0: Negative 1: Positive
24	EN_CLR3	Enables debounce function 0: Disable 1: Enable
23:20	DBNC_SETTING_CLR_CLR2	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms

Bit(s)	Name	Description
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
17	DBNC_RST2	Resets debounce counter
		0: Negative
		1: Positive
16	EN_CLR2	Enables debounce function
		0: Disable
		1: Enable
15:12	DBNC_SETTING_CLR_CLR1	Debounce setting
		0000: 0.125 ms
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
9	DBNC_RST1	Resets debounce counter
		0: Negative
		1: Positive
8	EN_CLR1	Enables debounce function
		0: Disable
		1: Enable
7:4	DBNC_SETTING_CLR_CLR0	Debounce setting
		0000: 0.125 ms

Bit(s)	Name	Description
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
1	DBNC_RST0	Resets debounce counter
		0: Negative
		1: Positive
0	EN_CLR0	Enables debounce function
		0: Disable
		1: Enable

1000B800	EINT_EVENT_MASK0					External interrupt event mask register											FFFFFFF				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16					
Name	EINT_EVENT_MASK																				
Type	RO																				
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
Name	EINT_EVENT_MASK																				
Type	RO																				
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					

Bit(s)	Name	Description
31:0	EINT_EVENT_MASK	External interrupt event mask value

1000B840 **EINT_EVENT_MASK_SET0** External interrupt event mask set register **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_EVENT_MASK_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_EVENT_MASK_SET															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_EVENT_MASK_SET	Write 1 to specific bit to set the event mask of the corresponding external interrupt.

1000B880 **EINT_EVENT_MASK_CLR0** External interrupt event mask clear register **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_EVENT_MASK_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_EVENT_MASK_CLR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_EVENT_MASK_CLR	Write 1 to any bit to clear the event mask of corresponding external interrupt.

1000B900 DEINT_CON0 Directly-coupled EINT control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DEINT_CON			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DEINT_CON	Controls directly-coupled EINT
		0: Disable
		1: Enable

1000B940 DEINT_SELO Directly-coupled EINT select register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEINT_SEL3								DEINT_SEL2							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEINT_SEL1								DEINT_SELO							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DEINT_SEL3	Selects directly-coupled EINT3
		#: EINT number
23:16	DEINT_SEL2	Selects directly-coupled EINT2
		#: EINT number
15:8	DEINT_SEL1	Selects directly-coupled EINT1
		#: EINT number
7:0	DEINT_SELO	Selects directly-coupled EINT0
		#: EINT number

1000B980 DEINT_SEL_SET0 Directly-coupled EINT select set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEINT_SEL3								DEINT_SEL2							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEINT_SEL1								DEINT_SELO							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DEINT_SEL3	Sets directly-coupled EINT3 selection #: EINT number
23:16	DEINT_SEL2	Sets directly-coupled EINT2 selection #: EINT number
15:8	DEINT_SEL1	Sets directly-coupled EINT1 selection #: EINT number
7:0	DEINT_SELO	Sets directly-coupled EINT0 selection #: EINT number

1000B9C0 DEINT_SEL_CLR0 Directly-coupled EINT select clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEINT_SEL3								DEINT_SEL2							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEINT_SEL1								DEINT_SEL0							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DEINT_SEL3	Clears directly-coupled EINT3 selection #: EINT number
23:16	DEINT_SEL2	Clears directly-coupled EINT2 selection #: EINT number
15:8	DEINT_SEL1	Clears directly-coupled EINT1 selection #: EINT number
7:0	DEINT_SEL0	Clears directly-coupled EINT0 selection #: EINT number

1000B9F0 **EINT_EEVT** **EINT wake-up event status register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EINT_EEVT
Type																RO
Reset																1

Bit(s)	Name	Description
0	EINT_EEVT	EINT wake-up event status

1000BA00 **EINT_RAW_STA0** **External interrupt raw status register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_RAW_PEND	Each bit indicates the corresponding external interrupt status. Reading 1 means the interrupt is pending, no matter whether it is masked or not.

1000BA04 EINT_RAW_STA1 External interrupt raw status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_RAW_PEND	Each bit indicates the corresponding external interrupt status. Reading 1 means the interrupt is pending, no matter whether it is masked or not.

1000BA08 EINT_RAW_STA2 External interrupt raw status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EINT_RAW_PEND	Each bit indicates the corresponding external interrupt status. Reading 1 means the interrupt is pending, no matter whether it is masked or not.

1000BC00 **EINT_SYNC_EN0** **External interrupt sync enable register** **03FFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYNC_EN0															
Type	RO															
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_EN0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	SYNC_EN0	External interrupt sync enable If the register is 0, it means the interrupt cannot be received. Bit Y, control $y*4 + 3$: $y*4$ EINT 0: Disable sync 1: Enable sync

1000BD00 **EINT_SYNC_EN_SET_0** **External interrupt sync enable set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYNC_EN_SET_0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_EN_SET_0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYNC_EN_SET_0	Set EN0 to 1. 0: Disable 1: Enable

1000BE00 EINT_SYNC_EN_CLR_0 External interrupt sync enable clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYNC_EN_CLR_0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYNC_EN_CLR_0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYNC_EN_CLR_0	Set EN0 to 1. 0: Disable 1: Enable

1000BF00 FPGA_EMUL_0 FPGA emulation register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FPGA_EMUL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FPGA_EMUL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FPGA_EMUL	Emulates IO pads

1000BB00 SECURE_EINT_EN0 Secure EINT enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	secure_en															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	secure_en	Controls whether EINT 15 to 0 are in secure path or not

1000BB10 SECURE_DIR_EINT_EN Secure direct EINT enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													direct_secure_en			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	direct_secure_en	Controls whether direct IRQ 3 to 0 are in secure path or not

1000BB20 **DCM_ON** DCM enable 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																dcm_on
Type																RW
Reset																1

Bit(s)	Name	Description
0	dcm_on	Enables DCM

1000BB30 **SECURE_STATUS** Secure status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	secure_status															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	secure_status	Same meaning as status Will be 1 only when secure EINT is enabled and an interrupt occurs.

1000BC20 EINT_SYS_TIMER_LATCH_CTR EINT system timer latch control

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									SYS_TIMER_LATCH_CTRL2							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYS_TIMER_LATCH_CTRL1								SYS_TIMER_LATCH_CTRL0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:16	SYS_TIMER_LATCH_CTRL2	Selects EINT to be latched as latch 2
15:8	SYS_TIMER_LATCH_CTRL1	Selects EINT to be latched as latch 1
7:0	SYS_TIMER_LATCH_CTRL0	Selects EINT to be latched as latch 0

1000BC24 EINT_SYS_TIMER_LATCH0_L EINT system timer latch 0 - low

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYS_TIMER_LATCH0_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYS_TIMER_LATCH0_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYS_TIMER_LATCH0_L	Latch 0 LSB

1000BC28 EINT_SYS_TIMER_LATCH0_H EINT system timer latch 0 - high 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYS_TIMER_LATCH0_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYS_TIMER_LATCH0_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYS_TIMER_LATCH0_H	Latch 0 MSB

1000BC2C EINT_SYS_TIMER_LATCH1_L EINT system timer latch 1 - low 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYS_TIMER_LATCH1_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYS_TIMER_LATCH1_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYS_TIMER_LATCH1_L	Latch 1 LSB

1000BC30 EINT_SYS_TIMER_LATCH1_H EINT system timer latch 1 - high 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYS_TIMER_LATCH1_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYS_TIMER_LATCH1_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYS_TIMER_LATCH1_H	Latch 1 MSB

1000BC34 **EINT_SYS_TIMER_LATCH2_L** EINT system timer latch 2 - low 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYS_TIMER_LATCH2_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYS_TIMER_LATCH2_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYS_TIMER_LATCH2_L	Latch 2 LSB

1000BC38 **EINT_SYS_TIMER_LATCH2_H** EINT system timer latch 2 - high 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYS_TIMER_LATCH2_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYS_TIMER_LATCH2_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYS_TIMER_LATCH2_H	Latch 2 MSB

1000BD20 EINT_SYS_TIMER_IRQ_SRC_S EINT system timer IRQ SRC selection
EL_0

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYS_TIMER_IRQ_SRC_SEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYS_TIMER_IRQ_SRC_SEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SYS_TIMER_IRQ_SRC_SEL	Configures EINT to be level or edge while latching system timer 0: Level 1: Edge

1000B504 EINT_DBNC 7 4 External interrupt debounce control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING3						DBNC_RST3	EN3	DBNC_SETTING2						DBNC_RST2	EN2
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING1						DBNC_RST1	EN1	DBNC_SETTING0						DBNC_RST0	EN0
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Name	Description
31:28	DBNC_SETTING3	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
25	DBNC_RST3	Resets debounce counter 0: Negative 1: Positive
24	EN3	Enables debounce function 0: Disable 1: Enable
23:20	DBNC_SETTING2	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms

Bit(s)	Name	Description
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
17	DBNC_RST2	Resets debounce counter
		0: Negative
		1: Positive
16	EN2	Enables debounce function
		0: Disable
		1: Enable
15:12	DBNC_SETTING1	Debounce setting
		0000: 0.125 ms
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
9	DBNC_RST1	Resets debounce counter
		0: Negative
		1: Positive
8	EN1	Enables debounce function
		0: Disable
		1: Enable
7:4	DBNC_SETTING0	Debounce setting
		0000: 0.125 ms

Bit(s)	Name	Description
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
1	DBNC_RST0	Resets debounce counter
		0: Negative
		1: Positive
0	ENO	Enables debounce function
		0: Disable
		1: Enable

1000B604 EINT_DBNC_SET 7 4 External interrupt debounce control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET3						DBNC_RST_SET3	EN_SET3	DBNC_SETTING_SET2						DBNC_RST_SET2	EN_SET2
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET1						DBNC_RST_SET1	EN_SET1	DBNC_SETTING_SET0						DBNC_RST_SET0	EN_SET0
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Name	Description
31:28	DBNC_SETTING_SET3	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
25	DBNC_RST_SET3	Resets debounce counter 0: Negative 1: Positive
24	EN_SET3	Enables debounce function 0: Disable 1: Enable
23:20	DBNC_SETTING_SET2	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms

Bit(s)	Name	Description
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
17	DBNC_RST_SET2	Resets debounce counter
		0: Negative
		1: Positive
16	EN_SET2	Enables debounce function
		0: Disable
		1: Enable
15:12	DBNC_SETTING_SET1	Debounce setting
		0000: 0.125 ms
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
9	DBNC_RST_SET1	Resets debounce counter
		0: Negative
		1: Positive
8	EN_SET1	Enables debounce function
		0: Disable
		1: Enable
7:4	DBNC_SETTING_SET0	Debounce setting

Bit(s)	Name	Description
		0000: 0.125 ms
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
1	DBNC_RST_SET0	Resets debounce counter
		0: Negative
		1: Positive
0	EN_SET0	Enables debounce function
		0: Disable
		1: Enable

1000B704 EINT_DBNC_CLR_7_4 External interrupt debounce control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR3						DBNC_RST3	EN_CLR3	DBNC_SETTING_CLR_CLR2						DBNC_RST2	EN_CLR2
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR1						DBNC_RST1	EN_CLR1	DBNC_SETTING_CLR_CLR0						DBNC_RST0	EN_CLR0
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Name	Description
31:28	DBNC_SETTING_CLR_CLR3	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
25	DBNC_RST3	Resets debounce counter 0: Negative 1: Positive
24	EN_CLR3	Enables debounce function 0: Disable 1: Enable
23:20	DBNC_SETTING_CLR_CLR2	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms

Bit(s)	Name	Description
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
17	DBNC_RST2	Resets debounce counter
		0: Negative
		1: Positive
16	EN_CLR2	Enables debounce function
		0: Disable
		1: Enable
15:12	DBNC_SETTING_CLR_CLR1	Debounce setting
		0000: 0.125 ms
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
9	DBNC_RST1	Resets debounce counter
		0: Negative
		1: Positive
8	EN_CLR1	Enables debounce function
		0: Disable
		1: Enable
7:4	DBNC_SETTING_CLR_CLR0	Debounce setting
		0000: 0.125 ms

Bit(s)	Name	Description
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
1	DBNC_RST0	Resets debounce counter
		0: Negative
		1: Positive
0	EN_CLR0	Enables debounce function
		0: Disable
		1: Enable

100B508 EINT_DBNC B 8 External interrupt debounce control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING3						DBNC_RST3	EN3	DBNC_SETTING2						DBNC_RST2	EN2
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING1						DBNC_RST1	EN1	DBNC_SETTING0						DBNC_RST0	EN0
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Name	Description
31:28	DBNC_SETTING3	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
25	DBNC_RST3	Resets debounce counter 0: Negative 1: Positive
24	EN3	Enables debounce function 0: Disable 1: Enable
23:20	DBNC_SETTING2	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms

Bit(s)	Name	Description
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
17	DBNC_RST2	Resets debounce counter
		0: Negative
		1: Positive
16	EN2	Enables debounce function
		0: Disable
		1: Enable
15:12	DBNC_SETTING1	Debounce setting
		0000: 0.125 ms
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
9	DBNC_RST1	Resets debounce counter
		0: Negative
		1: Positive
8	EN1	Enables debounce function
		0: Disable
		1: Enable
7:4	DBNC_SETTING0	Debounce setting
		0000: 0.125 ms

Bit(s)	Name	Description
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
1	DBNC_RST0	Resets debounce counter
		0: Negative
		1: Positive
0	ENO	Enables debounce function
		0: Disable
		1: Enable

1000B608 EINT_DBNC_SET_B_8 External interrupt debounce control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET3						DBNC_RST_SET3	EN_SET3	DBNC_SETTING_SET2						DBNC_RST_SET2	EN_SET2
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET1						DBNC_RST_SET1	EN_SET1	DBNC_SETTING_SET0						DBNC_RST_SET0	EN_SET0
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Name	Description
31:28	DBNC_SETTING_SET3	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
25	DBNC_RST_SET3	Resets debounce counter 0: Negative 1: Positive
24	EN_SET3	Enables debounce function 0: Disable 1: Enable
23:20	DBNC_SETTING_SET2	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms

Bit(s)	Name	Description
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
17	DBNC_RST_SET2	Resets debounce counter
		0: Negative
		1: Positive
16	EN_SET2	Enables debounce function
		0: Disable
		1: Enable
15:12	DBNC_SETTING_SET1	Debounce setting
		0000: 0.125 ms
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
9	DBNC_RST_SET1	Resets debounce counter
		0: Negative
		1: Positive
8	EN_SET1	Enables debounce function
		0: Disable
		1: Enable
7:4	DBNC_SETTING_SET0	Debounce setting

Bit(s)	Name	Description
		0000: 0.125 ms
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
1	DBNC_RST_SET0	Resets debounce counter
		0: Negative
		1: Positive
0	EN_SET0	Enables debounce function
		0: Disable
		1: Enable

1000B708 EINT_DBNC_CLR_B_8 External interrupt debounce control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR3						DBNC_RST3	EN_CLR3	DBNC_SETTING_CLR_CLR2						DBNC_RST2	EN_CLR2
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR1						DBNC_RST1	EN_CLR1	DBNC_SETTING_CLR_CLR0						DBNC_RST0	EN_CLR0
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Name	Description
31:28	DBNC_SETTING_CLR_CLR3	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
25	DBNC_RST3	Resets debounce counter 0: Negative 1: Positive
24	EN_CLR3	Enables debounce function 0: Disable 1: Enable
23:20	DBNC_SETTING_CLR_CLR2	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms

Bit(s)	Name	Description
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
17	DBNC_RST2	Resets debounce counter
		0: Negative
		1: Positive
16	EN_CLR2	Enables debounce function
		0: Disable
		1: Enable
15:12	DBNC_SETTING_CLR_CLR1	Debounce setting
		0000: 0.125 ms
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
9	DBNC_RST1	Resets debounce counter
		0: Negative
		1: Positive
8	EN_CLR1	Enables debounce function
		0: Disable
		1: Enable
7:4	DBNC_SETTING_CLR_CLR0	Debounce setting
		0000: 0.125 ms

Bit(s)	Name	Description
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
1	DBNC_RST0	Resets debounce counter
		0: Negative
		1: Positive
0	EN_CLR0	Enables debounce function
		0: Disable
		1: Enable

1000B50C EINT_DBNC_F_C External interrupt debounce control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING3						DBNC_RST3	EN3	DBNC_SETTING2						DBNC_RST2	EN2
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING1						DBNC_RST1	EN1	DBNC_SETTING0						DBNC_RST0	EN0
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Name	Description
31:28	DBNC_SETTING3	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
25	DBNC_RST3	Resets debounce counter 0: Negative 1: Positive
24	EN3	Enables debounce function 0: Disable 1: Enable
23:20	DBNC_SETTING2	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms

Bit(s)	Name	Description
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
17	DBNC_RST2	Resets debounce counter
		0: Negative
		1: Positive
16	EN2	Enables debounce function
		0: Disable
		1: Enable
15:12	DBNC_SETTING1	Debounce setting
		0000: 0.125 ms
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
9	DBNC_RST1	Resets debounce counter
		0: Negative
		1: Positive
8	EN1	Enables debounce function
		0: Disable
		1: Enable
7:4	DBNC_SETTING0	Debounce setting
		0000: 0.125 ms

Bit(s)	Name	Description
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
1	DBNC_RST0	Resets debounce counter
		0: Negative
		1: Positive
0	ENO	Enables debounce function
		0: Disable
		1: Enable

1000B60C EINT_DBNC_SET_F_C External interrupt debounce control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET3						DBNC_RST_SET3	EN_SET3	DBNC_SETTING_SET2						DBNC_RST_SET2	EN_SET2
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET1						DBNC_RST_SET1	EN_SET1	DBNC_SETTING_SET0						DBNC_RST_SET0	EN_SET0
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Name	Description
31:28	DBNC_SETTING_SET3	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
25	DBNC_RST_SET3	Resets debounce counter 0: Negative 1: Positive
24	EN_SET3	Enables debounce function 0: Disable 1: Enable
23:20	DBNC_SETTING_SET2	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms

Bit(s)	Name	Description
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
17	DBNC_RST_SET2	Resets debounce counter
		0: Negative
		1: Positive
16	EN_SET2	Enables debounce function
		0: Disable
		1: Enable
15:12	DBNC_SETTING_SET1	Debounce setting
		0000: 0.125 ms
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
9	DBNC_RST_SET1	Resets debounce counter
		0: Negative
		1: Positive
8	EN_SET1	Enables debounce function
		0: Disable
		1: Enable
7:4	DBNC_SETTING_SET0	Debounce setting

Bit(s)	Name	Description
		0000: 0.125 ms
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
1	DBNC_RST_SET0	Resets debounce counter
		0: Negative
		1: Positive
0	EN_SET0	Enables debounce function
		0: Disable
		1: Enable

1000B70C **EINT_DBNC_CLR_F_C** **External interrupt debounce control register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR3						DBNC_RST3	EN_CLR3	DBNC_SETTING_CLR_CLR2						DBNC_RST2	EN_CLR2
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR1						DBNC_RST1	EN_CLR1	DBNC_SETTING_CLR_CLR0						DBNC_RST0	EN_CLR0
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Name	Description
31:28	DBNC_SETTING_CLR_CLR3	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
25	DBNC_RST3	Resets debounce counter 0: Negative 1: Positive
24	EN_CLR3	Enables debounce function 0: Disable 1: Enable
23:20	DBNC_SETTING_CLR_CLR2	Debounce setting 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms

Bit(s)	Name	Description
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
17	DBNC_RST2	Resets debounce counter
		0: Negative
		1: Positive
16	EN_CLR2	Enables debounce function
		0: Disable
		1: Enable
15:12	DBNC_SETTING_CLR_CLR1	Debounce setting
		0000: 0.125 ms
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
9	DBNC_RST1	Resets debounce counter
		0: Negative
		1: Positive
8	EN_CLR1	Enables debounce function
		0: Disable
		1: Enable
7:4	DBNC_SETTING_CLR_CLR0	Debounce setting
		0000: 0.125 ms

Bit(s)	Name	Description
		0001: 0.25 ms
		0010: 0.5 ms
		0011: 1 ms
		0100: 16 ms
		0101: 32 ms
		0110: 64 ms
		0111: 128 ms
		1000: 256 ms
		1001: 512 ms
		Others: 0.5 ms
1	DBNC_RST0	Resets debounce counter
		0: Negative
		1: Positive
0	EN_CLR0	Enables debounce function
		0: Disable
		1: Enable

1.3 System Interrupt Controller

1.3.1 Register Definition

Module name: sys_cirq Base address: (+0x1020_4000)

Address	Name	Width	Register Function
10204000	<u>CIRQ_STA0</u>	32	System CIRQ status register
10204004	<u>CIRQ_STA1</u>	32	System CIRQ status register
10204008	<u>CIRQ_STA2</u>	32	System CIRQ status register
1020400C	<u>CIRQ_STA3</u>	32	System CIRQ status register
10204010	<u>CIRQ_STA4</u>	32	System CIRQ status register
10204014	<u>CIRQ_STA5</u>	32	System CIRQ status register
10204018	<u>CIRQ_STA6</u>	32	System CIRQ status register
1020401C	<u>CIRQ_STA7</u>	32	System CIRQ status register
10204080	<u>CIRQ_ACK0</u>	32	System CIRQ acknowledge register
10204084	<u>CIRQ_ACK1</u>	32	System CIRQ acknowledge register
10204088	<u>CIRQ_ACK2</u>	32	System CIRQ acknowledge register
1020408C	<u>CIRQ_ACK3</u>	32	System CIRQ acknowledge register
10204090	<u>CIRQ_ACK4</u>	32	System CIRQ acknowledge register
10204094	<u>CIRQ_ACK5</u>	32	System CIRQ acknowledge register
10204098	<u>CIRQ_ACK6</u>	32	System CIRQ acknowledge register
1020409C	<u>CIRQ_ACK7</u>	32	System CIRQ acknowledge register
10204100	<u>CIRQ_MASK0</u>	32	System CIRQ mask register
10204104	<u>CIRQ_MASK1</u>	32	System CIRQ mask register
10204108	<u>CIRQ_MASK2</u>	32	System CIRQ mask register
1020410C	<u>CIRQ_MASK3</u>	32	System CIRQ mask register
10204110	<u>CIRQ_MASK4</u>	32	System CIRQ mask register
10204114	<u>CIRQ_MASK5</u>	32	System CIRQ mask register
10204118	<u>CIRQ_MASK6</u>	32	System CIRQ mask register
1020411C	<u>CIRQ_MASK7</u>	32	System CIRQ mask register
10204180	<u>CIRQ_MASK_SET0</u>	32	System CIRQ mask set register
10204184	<u>CIRQ_MASK_SET1</u>	32	System CIRQ mask set register
10204188	<u>CIRQ_MASK_SET2</u>	32	System CIRQ mask set register
1020418C	<u>CIRQ_MASK_SET3</u>	32	System CIRQ mask set register
10204190	<u>CIRQ_MASK_SET4</u>	32	System CIRQ mask set register
10204194	<u>CIRQ_MASK_SET5</u>	32	System CIRQ mask set register
10204198	<u>CIRQ_MASK_SET6</u>	32	System CIRQ mask set register
1020419C	<u>CIRQ_MASK_SET7</u>	32	System CIRQ mask set register
10204200	<u>CIRQ_MASK_CLR0</u>	32	System CIRQ mask set register
10204204	<u>CIRQ_MASK_CLR1</u>	32	System CIRQ mask set register
10204208	<u>CIRQ_MASK_CLR2</u>	32	System CIRQ mask set register
1020420C	<u>CIRQ_MASK_CLR3</u>	32	System CIRQ mask set register
10204210	<u>CIRQ_MASK_CLR4</u>	32	System CIRQ mask set register
10204214	<u>CIRQ_MASK_CLR5</u>	32	System CIRQ mask set register
10204218	<u>CIRQ_MASK_CLR6</u>	32	System CIRQ mask set register
1020421C	<u>CIRQ_MASK_CLR7</u>	32	System CIRQ mask set register
10204280	<u>CIRQ_SENS0</u>	32	System CIRQ sensitivity register
10204284	<u>CIRQ_SENS1</u>	32	System CIRQ sensitivity register
10204288	<u>CIRQ_SENS2</u>	32	System CIRQ sensitivity register
1020428C	<u>CIRQ_SENS3</u>	32	System CIRQ sensitivity register

Address	Name	Width	Register Function
10204290	<u>CIRQ_SENS4</u>	32	System CIRQ sensitivity register
10204294	<u>CIRQ_SENS5</u>	32	System CIRQ sensitivity register
10204298	<u>CIRQ_SENS6</u>	32	System CIRQ sensitivity register
1020429C	<u>CIRQ_SENS7</u>	32	System CIRQ sensitivity register
10204300	<u>CIRQ_SENS_SET0</u>	32	System CIRQ sensitivity set register
10204304	<u>CIRQ_SENS_SET1</u>	32	System CIRQ sensitivity set register
10204308	<u>CIRQ_SENS_SET2</u>	32	System CIRQ sensitivity set register
1020430C	<u>CIRQ_SENS_SET3</u>	32	System CIRQ sensitivity set register
10204310	<u>CIRQ_SENS_SET4</u>	32	System CIRQ sensitivity set register
10204314	<u>CIRQ_SENS_SET5</u>	32	System CIRQ sensitivity set register
10204318	<u>CIRQ_SENS_SET6</u>	32	System CIRQ sensitivity set register
1020431C	<u>CIRQ_SENS_SET7</u>	32	System CIRQ sensitivity set register
10204380	<u>CIRQ_SENS_CLR0</u>	32	System CIRQ sensitivity clear register
10204384	<u>CIRQ_SENS_CLR1</u>	32	System CIRQ sensitivity clear register
10204388	<u>CIRQ_SENS_CLR2</u>	32	System CIRQ sensitivity clear register
1020438C	<u>CIRQ_SENS_CLR3</u>	32	System CIRQ sensitivity clear register
10204390	<u>CIRQ_SENS_CLR4</u>	32	System CIRQ sensitivity clear register
10204394	<u>CIRQ_SENS_CLR5</u>	32	System CIRQ sensitivity clear register
10204398	<u>CIRQ_SENS_CLR6</u>	32	System CIRQ sensitivity clear register
1020439C	<u>CIRQ_SENS_CLR7</u>	32	System CIRQ sensitivity clear register
10204400	<u>CIRQ_POL0</u>	32	External interrupt polarity register
10204404	<u>CIRQ_POL1</u>	32	External interrupt polarity register
10204408	<u>CIRQ_POL2</u>	32	External interrupt polarity register
1020440C	<u>CIRQ_POL3</u>	32	External interrupt polarity register
10204410	<u>CIRQ_POL4</u>	32	External interrupt polarity register
10204414	<u>CIRQ_POL5</u>	32	External interrupt polarity register
10204418	<u>CIRQ_POL6</u>	32	External interrupt polarity register
1020441C	<u>CIRQ_POL7</u>	32	External interrupt polarity register
10204480	<u>CIRQ_POL_SET0</u>	32	External interrupt polarity set register
10204484	<u>CIRQ_POL_SET1</u>	32	External interrupt polarity set register
10204488	<u>CIRQ_POL_SET2</u>	32	External interrupt polarity set register
1020448C	<u>CIRQ_POL_SET3</u>	32	External interrupt polarity set register
10204490	<u>CIRQ_POL_SET4</u>	32	External interrupt polarity set register
10204494	<u>CIRQ_POL_SET5</u>	32	External interrupt polarity set register
10204498	<u>CIRQ_POL_SET6</u>	32	External interrupt polarity set register
1020449C	<u>CIRQ_POL_SET7</u>	32	External interrupt polarity set register
10204500	<u>CIRQ_POL_CLR0</u>	32	External interrupt polarity clear register
10204504	<u>CIRQ_POL_CLR1</u>	32	External interrupt polarity clear register
10204508	<u>CIRQ_POL_CLR2</u>	32	External interrupt polarity clear register
1020450C	<u>CIRQ_POL_CLR3</u>	32	External interrupt polarity clear register
10204510	<u>CIRQ_POL_CLR4</u>	32	External interrupt polarity clear register
10204514	<u>CIRQ_POL_CLR5</u>	32	External interrupt polarity clear register
10204518	<u>CIRQ_POL_CLR6</u>	32	External interrupt polarity clear register
1020451C	<u>CIRQ_POL_CLR7</u>	32	External interrupt polarity clear register
10204600	<u>CIRQ_CON</u>	32	System CIRQ control register
10204604	<u>CIRQ_VERSION</u>	32	IP version of SYS_CIRQ
10204608	<u>CIRQ_EDGE_OFLW</u>	32	
1020460C	<u>CIRQ_DEFCONF</u>	32	Defer function control register
10204680	<u>CIRQ_GROP00</u>	32	Timer group setting of interrupt

Address	Name	Width	Register Function
10204684	<u>CIRQ_GROP01</u>	32	Timer group setting of interrupt
10204688	<u>CIRQ_GROP02</u>	32	Timer group setting of interrupt
1020468C	<u>CIRQ_GROP03</u>	32	Timer group setting of interrupt
10204690	<u>CIRQ_GROP04</u>	32	Timer group setting of interrupt
10204694	<u>CIRQ_GROP05</u>	32	Timer group setting of interrupt
10204698	<u>CIRQ_GROP06</u>	32	Timer group setting of interrupt
1020469C	<u>CIRQ_GROP07</u>	32	Timer group setting of interrupt
102046A0	<u>CIRQ_GROP08</u>	32	Timer group setting of interrupt
102046A4	<u>CIRQ_GROP09</u>	32	Timer group setting of interrupt
102046A8	<u>CIRQ_GROP10</u>	32	Timer group setting of interrupt
102046AC	<u>CIRQ_GROP11</u>	32	Timer group setting of interrupt
102046B0	<u>CIRQ_GROP12</u>	32	Timer group setting of interrupt
102046B4	<u>CIRQ_GROP13</u>	32	Timer group setting of interrupt
102046B8	<u>CIRQ_GROP14</u>	32	Timer group setting of interrupt
102046BC	<u>CIRQ_GROP15</u>	32	Timer group setting of interrupt
102046C0	<u>CIRQ_GROP16</u>	32	Timer group setting of interrupt
102046C4	<u>CIRQ_GROP17</u>	32	Timer group setting of interrupt
102046C8	<u>CIRQ_GROP18</u>	32	Timer group setting of interrupt
102046CC	<u>CIRQ_GROP19</u>	32	Timer group setting of interrupt
102046D0	<u>CIRQ_GROP20</u>	32	Timer group setting of interrupt
102046D4	<u>CIRQ_GROP21</u>	32	Timer group setting of interrupt
102046D8	<u>CIRQ_GROP22</u>	32	Timer group setting of interrupt
102046DC	<u>CIRQ_GROP23</u>	32	Timer group setting of interrupt
102046E0	<u>CIRQ_GROP24</u>	32	Timer group setting of interrupt
102046E4	<u>CIRQ_GROP25</u>	32	Timer group setting of interrupt
102046E8	<u>CIRQ_GROP26</u>	32	Timer group setting of interrupt
102046EC	<u>CIRQ_GROP27</u>	32	Timer group setting of interrupt
102046F0	<u>CIRQ_GROP28</u>	32	Timer group setting of interrupt
102046F4	<u>CIRQ_GROP29</u>	32	Timer group setting of interrupt
102046F8	<u>CIRQ_GROP30</u>	32	Timer group setting of interrupt
102046FC	<u>CIRQ_GROP31</u>	32	Timer group setting of interrupt
10204700	<u>CIRQ_GROP32</u>	32	Timer group setting of interrupt
10204704	<u>CIRQ_GROP33</u>	32	Timer group setting of interrupt
10204708	<u>CIRQ_GROP34</u>	32	Timer group setting of interrupt
10204880	<u>LATCH OF CIRQ_STATUS_NEXT0</u>	32	Latch of CORQ_STATUS_NEXT
10204884	<u>LATCH OF CIRQ_STATUS_NEXT1</u>	32	Latch of CORQ_STATUS_NEXT
10204888	<u>LATCH OF CIRQ_STATUS_NEXT2</u>	32	Latch of CORQ_STATUS_NEXT
1020488C	<u>LATCH OF CIRQ_STATUS_NEXT3</u>	32	Latch of CORQ_STATUS_NEXT
10204890	<u>LATCH OF CIRQ_STATUS_NEXT4</u>	32	Latch of CORQ_STATUS_NEXT
10204894	<u>LATCH OF CIRQ_STATUS_NEXT5</u>	32	Latch of CORQ_STATUS_NEXT
10204898	<u>LATCH OF CIRQ_STATUS_NEXT6</u>	32	Latch of CORQ_STATUS_NEXT
1020489C	<u>LATCH OF CIRQ_STATUS_NEXT7</u>	32	Latch of CORQ_STATUS_NEXT

10204000 CIRQ_STA0 System CIRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_STA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_STA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_STA0	Reading 1 indicates the corresponding system CIRQ is pending.

10204004 CIRQ_STA1 System CIRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_STA1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_STA1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_STA1	Reading 1 indicates the corresponding system CIRQ is pending.

10204008 CIRQ_STA2 System CIRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_STA2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_STA2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_STA2	Reading 1 indicates the corresponding system CIRQ is pending.

1020400C CIRQ_STA3 System CIRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_STA3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_STA3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_STA3	Reading 1 indicates the corresponding system CIRQ is pending.

10204010 CIRQ_STA4 System CIRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_STA4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_STA4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_STA4	Reading 1 indicates the corresponding system CIRQ is pending.

10204014 **CIRQ_STA5** **System CIRQ status register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_STA5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_STA5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_STA5	Reading 1 indicates the corresponding system CIRQ is pending.

10204018 **CIRQ_STA6** **System CIRQ status register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_STA6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_STA6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_STA6	Reading 1 indicates the corresponding system CIRQ is pending.

1020401C CIRQ_STA7 System CIRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_STA7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CIRQ_STA7	Reading 1 indicates the corresponding system CIRQ is pending.

10204080 CIRQ_ACK0 System CIRQ acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_ACK0	Write 1 to specific bit to acknowledge the corresponding system CIRQ.

10204084 **CIRQ_ACK1** **System CIRQ acknowledge register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_ACK1	Write 1 to specific bit to acknowledge the corresponding system CIRQ.

10204088 **CIRQ_ACK2** **System CIRQ acknowledge register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_ACK2	Write 1 to specific bit to acknowledge the corresponding system CIRQ.

1020408C CIRQ_ACK3 System CIRQ acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_ACK3	Write 1 to specific bit to acknowledge the corresponding system CIRQ.

10204090 CIRQ_ACK4 System CIRQ acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_ACK4	Write 1 to specific bit to acknowledge the corresponding system CIRQ.

10204094 CIRQ_ACK5 System CIRQ acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_ACK5	Write 1 to specific bit to acknowledge the corresponding system CIRQ.

10204098 CIRQ_ACK6 System CIRQ acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_ACK6	Write 1 to specific bit to acknowledge the corresponding system CIRQ.

1020409C CIRQ_ACK7 System CIRQ acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK7															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CIRQ_ACK7	Write 1 to specific bit to acknowledge the corresponding system CIRQ.

10204100 CIRQ_MASK0 System CIRQ mask register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK0	System CIRQ mask value

10204104 CIRQ_MASK1 System CIRQ mask register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK1	System CIRQ mask value

10204108 CIRQ_MASK2 System CIRQ mask register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK2	System CIRQ mask value

1020410C CIRQ_MASK3 System CIRQ mask register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK3	System CIRQ mask value

10204110 CIRQ_MASK4 System CIRQ mask register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK4	System CIRQ mask value

10204114 **CIRQ_MASK5** **System CIRQ mask register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK5	System CIRQ mask value

10204118 **CIRQ_MASK6** **System CIRQ mask register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK6	System CIRQ mask value

1020411C CIRQ_MASK7 System CIRQ mask register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CIRQ_MASK7	System CIRQ mask value

10204180 CIRQ_MASK_SET0 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK_SET0	Write 1 to specific bit to set the mask of the corresponding system CIRQ.

10204184 **CIRQ_MASK_SET1** **System CIRQ mask set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK_SET1	Write 1 to specific bit to set the mask of the corresponding system CIRQ.

10204188 **CIRQ_MASK_SET2** **System CIRQ mask set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK_SET2	Write 1 to specific bit to set the mask of the corresponding system CIRQ.

1020418C CIRQ_MASK_SET3 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK_SET3	Write 1 to specific bit to set the mask of the corresponding system CIRQ.

10204190 CIRQ_MASK_SET4 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK_SET4	Write 1 to specific bit to set the mask of the corresponding system CIRQ.

10204194 CIRQ_MASK_SET5 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK_SET5	Write 1 to specific bit to set the mask of the corresponding system CIRQ.

10204198 CIRQ_MASK_SET6 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK_SET6	Write 1 to specific bit to set the mask of the corresponding system CIRQ.

1020419C CIRQ_MASK_SET7 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET7															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CIRQ_MASK_SET7	Write 1 to specific bit to set the mask of the corresponding system CIRQ.

10204200 CIRQ_MASK_CLR0 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK_CLR0	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

10204204 CIRQ_MASK_CLR1 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK_CLR1	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

10204208 CIRQ_MASK_CLR2 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK_CLR2	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

1020420C CIRQ_MASK_CLR3 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK_CLR3	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

10204210 CIRQ_MASK_CLR4 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK_CLR4	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

10204214 **CIRQ_MASK_CLR5** **System CIRQ mask set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK_CLR5	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

10204218 **CIRQ_MASK_CLR6** **System CIRQ mask set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_MASK_CLR6	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

1020421C CIRQ_MASK_CLR7 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR7															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CIRQ_MASK_CLR7	Write 1 to specific bit to clear the mask of the corresponding system CIRQ.

10204280 CIRQ_SENS0 System CIRQ sensitivity register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS0	System CIRQ sensitivity value

10204284 CIRQ_SENS1 System CIRQ sensitivity register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS1	System CIRQ sensitivity value

10204288 CIRQ_SENS2 System CIRQ sensitivity register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS2	System CIRQ sensitivity value

1020428C CIRQ_SENS3 System CIRQ sensitivity register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS3	System CIRQ sensitivity value

10204290 CIRQ_SENS4 System CIRQ sensitivity register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS4	System CIRQ sensitivity value

10204294 **CIRQ_SENS5** **System CIRQ sensitivity register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS5	System CIRQ sensitivity value

10204298 **CIRQ_SENS6** **System CIRQ sensitivity register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS6	System CIRQ sensitivity value

1020429C CIRQ_SENS7 System CIRQ sensitivity register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CIRQ_SENS7	System CIRQ sensitivity value

10204300 CIRQ_SENS_SET0 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS_SET0	Write 1 to specific bit to set the sensitivity of the corresponding system CIRQ.

10204304 CIRQ_SENS_SET1 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS_SET1	Write 1 to specific bit to set the sensitivity of the corresponding system CIRQ.

10204308 CIRQ_SENS_SET2 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS_SET2	Write 1 to specific bit to set the sensitivity of the corresponding system CIRQ.

1020430C CIRQ_SENS_SET3 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS_SET3	Write 1 to specific bit to set the sensitivity of the corresponding system CIRQ.

10204310 CIRQ_SENS_SET4 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS_SET4	Write 1 to specific bit to set the sensitivity of the corresponding system CIRQ.

10204314 CIRQ_SENS_SET5 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS_SET5	Write 1 to specific bit to set the sensitivity of the corresponding system CIRQ.

10204318 CIRQ_SENS_SET6 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS_SET6	Write 1 to specific bit to set the sensitivity of the corresponding system CIRQ.

1020431C CIRQ_SENS_SET7 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET7															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CIRQ_SENS_SET7	Write 1 to specific bit to set the sensitivity of the corresponding system CIRQ.

10204380 CIRQ_SENS_CLR0 System CIRQ sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS_CLR0	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

10204384 CIRQ_SENS_CLR1 System CIRQ sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS_CLR1	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

10204388 CIRQ_SENS_CLR2 System CIRQ sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS_CLR2	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

1020438C CIRQ_SENS_CLR3 System CIRQ sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS_CLR3	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

10204390 CIRQ_SENS_CLR4 System CIRQ sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS_CLR4	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

10204394 CIRQ_SENS_CLR5 System CIRQ sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS_CLR5	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

10204398 CIRQ_SENS_CLR6 System CIRQ sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_SENS_CLR6	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

1020439C CIRQ_SENS_CLR7 System CIRQ sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR7															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CIRQ_SENS_CLR7	Write 1 to specific bit to clear the sensitivity of the corresponding system CIRQ.

10204400 CIRQ_POLO External interrupt polarity register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POLO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POLO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POLO	System CIRQ polarity value

10204404 **CIRQ_POL1** **External interrupt polarity register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL1	System CIRQ polarity value

10204408 **CIRQ_POL2** **External interrupt polarity register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL2	System CIRQ polarity value

1020440C **CIRQ_POL3** **External interrupt polarity register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL3	System CIRQ polarity value

10204410 **CIRQ_POL4** **External interrupt polarity register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL4	System CIRQ polarity value

10204414 **CIRQ_POL5** **External interrupt polarity register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL5	System CIRQ polarity value

10204418 **CIRQ_POL6** **External interrupt polarity register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL6	System CIRQ polarity value

1020441C CIRQ_POL7 External interrupt polarity register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CIRQ_POL7	System CIRQ polarity value

10204480 CIRQ_POL_SET0 External interrupt polarity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL_SET0	Write 1 to specific bit to set the polarity of the corresponding system CIRQ.

10204484 **CIRQ_POL_SET1** **External interrupt polarity set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL_SET1	Write 1 to specific bit to set the polarity of the corresponding system CIRQ.

10204488 **CIRQ_POL_SET2** **External interrupt polarity set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL_SET2	Write 1 to specific bit to set the polarity of the corresponding system CIRQ.

1020448C CIRQ_POL_SET3 External interrupt polarity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL_SET3	Write 1 to specific bit to set the polarity of the corresponding system CIRQ.

10204490 CIRQ_POL_SET4 External interrupt polarity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL_SET4	Write 1 to specific bit to set the polarity of the corresponding system CIRQ.

10204494 **CIRQ_POL_SET5** **External interrupt polarity set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL_SET5	Write 1 to specific bit to set the polarity of the corresponding system CIRQ.

10204498 **CIRQ_POL_SET6** **External interrupt polarity set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL_SET6	Write 1 to specific bit to set the polarity of the corresponding system CIRQ.

1020449C CIRQ_POL_SET7 External interrupt polarity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET7															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CIRQ_POL_SET7	Write 1 to specific bit to set the polarity of the corresponding system CIRQ.

10204500 CIRQ_POL_CLR0 External interrupt polarity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL_CLR0	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

10204504 CIRQ_POL_CLR1 External interrupt polarity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL_CLR1	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

10204508 CIRQ_POL_CLR2 External interrupt polarity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL_CLR2	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

1020450C CIRQ_POL_CLR3 External interrupt polarity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL_CLR3	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

10204510 CIRQ_POL_CLR4 External interrupt polarity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL_CLR4	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

10204514 CIRQ_POL_CLR5 External interrupt polarity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR5															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL_CLR5	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

10204518 CIRQ_POL_CLR6 External interrupt polarity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR6															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_POL_CLR6	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

1020451C CIRQ_POL_CLR7 External interrupt polarity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR7															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CIRQ_POL_CLR7	Write 1 to specific bit to clear the polarity of the corresponding system CIRQ.

10204600 CIRQ_CON System CIRQ control register 80100170

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_EVENT_B											SW_RESET_B				CIRQ_WIDTH_CNT
Type	RO											WO				RO
Reset	1											1				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_WIDTH_CNT							CIRQ_WIDTH_EXTEND					CIRQ_FLUSH_BUSY	CIRQ_FLUSH	CIRQ_EDGE_ONLY	CIRQ_EN
Type	RO							RW					RO	WO	RW	RW
Reset	0	0	0	0				1	0	1	1	1	0	0	0	0

Bit(s)	Name	Description
31	CIRQ_EVENT_B	Indicates sys_cirq_irq_b is triggered
20	SW_RESET_B	Software resets CIRQ_POL, CIRQ_SENS and CIRQ_MASK
16:12	CIRQ_WIDTH_CNT	Nth extra cycle of CIRQ after flush
8:4	CIRQ_WIDTH_EXTEND	Required number of extra cycles of CIRQ after flush
3	CIRQ_FLUSH_BUSY	Indicates flush is being serviced
2	CIRQ_FLUSH	Flushes pending interrupts
1	CIRQ_EDGE_ONLY	Sets edge-only mode
		Only edge-triggered interrupts are recorded.
0	CIRQ_EN	Enable bit of system CIRQ controller

10204604 **CIRQ_VERSION** IP version of SYS_CIRQ 00000200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_VERSION															
Type	RO															
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CIRQ_VERSION	Hardware version of SYS_CIRQ

10204608 **CIRQ_EDGE_OFLW** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_EDGE_OFLW															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_EDGE_OFLW															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIRQ_EDGE_OFLW	

1020460C CIRQ_DEFCNF Defer function control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DIS_CIRQ_IRQ	DIS_CIRQ_EVENT_B	CIRQ_BUS_SEL
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	DIS_CIRQ_IRQ	0: Enable 1: Disable
1	DIS_CIRQ_EVENT_B	0: Enable 1: Disable
0	CIRQ_BUS_SEL	0: Org bus 1: Defer bus

10204680 CIRQ_GROP00 Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT7				CIRQ_GRP_INT6				CIRQ_GRP_INT5				CIRQ_GRP_INT4		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT3				CIRQ_GRP_INT2				CIRQ_GRP_INT1				CIRQ_GRP_INT0		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT7	Group 0
26:24	CIRQ_GRP_INT6	Group 0
22:20	CIRQ_GRP_INT5	Group 0
18:16	CIRQ_GRP_INT4	Group 0
14:12	CIRQ_GRP_INT3	Group 0
10:8	CIRQ_GRP_INT2	Group 0
6:4	CIRQ_GRP_INT1	Group 0
2:0	CIRQ_GRP_INT0	Group 0

10204684 CIRQ_GROP01 Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT15				CIRQ_GRP_INT14				CIRQ_GRP_INT13				CIRQ_GRP_INT12		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT11				CIRQ_GRP_INT10				CIRQ_GRP_INT9				CIRQ_GRP_INT8		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT15	Group 1
26:24	CIRQ_GRP_INT14	Group 1
22:20	CIRQ_GRP_INT13	Group 1
18:16	CIRQ_GRP_INT12	Group 1
14:12	CIRQ_GRP_INT11	Group 1
10:8	CIRQ_GRP_INT10	Group 1
6:4	CIRQ_GRP_INT9	Group 1
2:0	CIRQ_GRP_INT8	Group 1

10204688 **CIRQ_GROP02** **Timer group setting of interrupt** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT23				CIRQ_GRP_INT22				CIRQ_GRP_INT21				CIRQ_GRP_INT20		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT19				CIRQ_GRP_INT18				CIRQ_GRP_INT17				CIRQ_GRP_INT16		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT23	Group 2
26:24	CIRQ_GRP_INT22	Group 2
22:20	CIRQ_GRP_INT21	Group 2
18:16	CIRQ_GRP_INT20	Group 2
14:12	CIRQ_GRP_INT19	Group 2
10:8	CIRQ_GRP_INT18	Group 2
6:4	CIRQ_GRP_INT17	Group 2
2:0	CIRQ_GRP_INT16	Group 2

1020468C CIRQ_GROP03 Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT31				CIRQ_GRP_INT30				CIRQ_GRP_INT29				CIRQ_GRP_INT28		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT27				CIRQ_GRP_INT26				CIRQ_GRP_INT25				CIRQ_GRP_INT24		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT31	Group 3
26:24	CIRQ_GRP_INT30	Group 3
22:20	CIRQ_GRP_INT29	Group 3
18:16	CIRQ_GRP_INT28	Group 3
14:12	CIRQ_GRP_INT27	Group 3
10:8	CIRQ_GRP_INT26	Group 3
6:4	CIRQ_GRP_INT25	Group 3
2:0	CIRQ_GRP_INT24	Group 3

10204690 **CIRQ_GROP04** **Timer group setting of interrupt** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT39				CIRQ_GRP_INT38				CIRQ_GRP_INT37				CIRQ_GRP_INT36		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT35				CIRQ_GRP_INT34				CIRQ_GRP_INT33				CIRQ_GRP_INT32		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT39	Group 4
26:24	CIRQ_GRP_INT38	Group 4
22:20	CIRQ_GRP_INT37	Group 4
18:16	CIRQ_GRP_INT36	Group 4
14:12	CIRQ_GRP_INT35	Group 4
10:8	CIRQ_GRP_INT34	Group 4
6:4	CIRQ_GRP_INT33	Group 4
2:0	CIRQ_GRP_INT32	Group 4

10204694 **CIRQ_GROP05** **Timer group setting of interrupt** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT47				CIRQ_GRP_INT46				CIRQ_GRP_INT45				CIRQ_GRP_INT44		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT43				CIRQ_GRP_INT42				CIRQ_GRP_INT41				CIRQ_GRP_INT40		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT47	Group 5
26:24	CIRQ_GRP_INT46	Group 5
22:20	CIRQ_GRP_INT45	Group 5
18:16	CIRQ_GRP_INT44	Group 5
14:12	CIRQ_GRP_INT43	Group 5
10:8	CIRQ_GRP_INT42	Group 5
6:4	CIRQ_GRP_INT41	Group 5
2:0	CIRQ_GRP_INT40	Group 5

10204698 **CIRQ_GROP06** **Timer group setting of interrupt** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT55				CIRQ_GRP_INT54				CIRQ_GRP_INT53				CIRQ_GRP_INT52		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT51				CIRQ_GRP_INT50				CIRQ_GRP_INT49				CIRQ_GRP_INT48		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT55	Group 6
26:24	CIRQ_GRP_INT54	Group 6
22:20	CIRQ_GRP_INT53	Group 6
18:16	CIRQ_GRP_INT52	Group 6
14:12	CIRQ_GRP_INT51	Group 6
10:8	CIRQ_GRP_INT50	Group 6
6:4	CIRQ_GRP_INT49	Group 6
2:0	CIRQ_GRP_INT48	Group 6

1020469C **CIRQ_GROP07** **Timer group setting of interrupt** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT63				CIRQ_GRP_INT62				CIRQ_GRP_INT61				CIRQ_GRP_INT60		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT59				CIRQ_GRP_INT58				CIRQ_GRP_INT57				CIRQ_GRP_INT56		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT63	Group 7
26:24	CIRQ_GRP_INT62	Group 7
22:20	CIRQ_GRP_INT61	Group 7
18:16	CIRQ_GRP_INT60	Group 7
14:12	CIRQ_GRP_INT59	Group 7
10:8	CIRQ_GRP_INT58	Group 7
6:4	CIRQ_GRP_INT57	Group 7
2:0	CIRQ_GRP_INT56	Group 7

102046A0 **CIRQ_GROP08** **Timer group setting of interrupt** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT71				CIRQ_GRP_INT70				CIRQ_GRP_INT99				CIRQ_GRP_INT88		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT67				CIRQ_GRP_INT66				CIRQ_GRP_INT65				CIRQ_GRP_INT64		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT71	Group 8
26:24	CIRQ_GRP_INT70	Group 8
22:20	CIRQ_GRP_INT99	Group 8
18:16	CIRQ_GRP_INT88	Group 8
14:12	CIRQ_GRP_INT67	Group 8
10:8	CIRQ_GRP_INT66	Group 8
6:4	CIRQ_GRP_INT65	Group 8
2:0	CIRQ_GRP_INT64	Group 8

102046A4 **CIRQ_GROP09** **Timer group setting of interrupt** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT79				CIRQ_GRP_INT78				CIRQ_GRP_INT77				CIRQ_GRP_INT76		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT75				CIRQ_GRP_INT74				CIRQ_GRP_INT73				CIRQ_GRP_INT72		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT79	Group 9
26:24	CIRQ_GRP_INT78	Group 9
22:20	CIRQ_GRP_INT77	Group 9
18:16	CIRQ_GRP_INT76	Group 9
14:12	CIRQ_GRP_INT75	Group 9
10:8	CIRQ_GRP_INT74	Group 9
6:4	CIRQ_GRP_INT73	Group 9
2:0	CIRQ_GRP_INT72	Group 9

102046A8 **CIRQ_GROP10** **Timer group setting of interrupt** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT87				CIRQ_GRP_INT86				CIRQ_GRP_INT85				CIRQ_GRP_INT84		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT83				CIRQ_GRP_INT82				CIRQ_GRP_INT81				CIRQ_GRP_INT80		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT87	Group 10
26:24	CIRQ_GRP_INT86	Group 10
22:20	CIRQ_GRP_INT85	Group 10
18:16	CIRQ_GRP_INT84	Group 10
14:12	CIRQ_GRP_INT83	Group 10
10:8	CIRQ_GRP_INT82	Group 10
6:4	CIRQ_GRP_INT81	Group 10
2:0	CIRQ_GRP_INT80	Group 10

102046AC CIRQ_GROP11 Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT95				CIRQ_GRP_INT94				CIRQ_GRP_INT93				CIRQ_GRP_INT92		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT91				CIRQ_GRP_INT90				CIRQ_GRP_INT89				CIRQ_GRP_INT88		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT95	Group 11
26:24	CIRQ_GRP_INT94	Group 11
22:20	CIRQ_GRP_INT93	Group 11
18:16	CIRQ_GRP_INT92	Group 11
14:12	CIRQ_GRP_INT91	Group 11
10:8	CIRQ_GRP_INT90	Group 11
6:4	CIRQ_GRP_INT89	Group 11
2:0	CIRQ_GRP_INT88	Group 11

102046B0 **CIRQ_GROP12** Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT103				CIRQ_GRP_INT102				CIRQ_GRP_INT101				CIRQ_GRP_INT100		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT99				CIRQ_GRP_INT98				CIRQ_GRP_INT97				CIRQ_GRP_INT96		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT103	Group 12
26:24	CIRQ_GRP_INT102	Group 12
22:20	CIRQ_GRP_INT101	Group 12
18:16	CIRQ_GRP_INT100	Group 12
14:12	CIRQ_GRP_INT99	Group 12
10:8	CIRQ_GRP_INT98	Group 12
6:4	CIRQ_GRP_INT97	Group 12
2:0	CIRQ_GRP_INT96	Group 12

102046B4 **CIRQ_GROP13** Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT111				CIRQ_GRP_INT110				CIRQ_GRP_INT109				CIRQ_GRP_INT108		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT107				CIRQ_GRP_INT106				CIRQ_GRP_INT105				CIRQ_GRP_INT104		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT111	Group 13
26:24	CIRQ_GRP_INT110	Group 13
22:20	CIRQ_GRP_INT109	Group 13
18:16	CIRQ_GRP_INT108	Group 13
14:12	CIRQ_GRP_INT107	Group 13
10:8	CIRQ_GRP_INT106	Group 13
6:4	CIRQ_GRP_INT105	Group 13
2:0	CIRQ_GRP_INT104	Group 13

102046B8 **CIRQ_GROP14** **Timer group setting of interrupt** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT119				CIRQ_GRP_INT118				CIRQ_GRP_INT117				CIRQ_GRP_INT116		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT115				CIRQ_GRP_INT114				CIRQ_GRP_INT113				CIRQ_GRP_INT112		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT119	Group 14
26:24	CIRQ_GRP_INT118	Group 14
22:20	CIRQ_GRP_INT117	Group 14
18:16	CIRQ_GRP_INT116	Group 14
14:12	CIRQ_GRP_INT115	Group 14
10:8	CIRQ_GRP_INT114	Group 14
6:4	CIRQ_GRP_INT113	Group 14
2:0	CIRQ_GRP_INT112	Group 14

102046BC CIRQ_GRP15 Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT127				CIRQ_GRP_INT126				CIRQ_GRP_INT125				CIRQ_GRP_INT124		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT123				CIRQ_GRP_INT122				CIRQ_GRP_INT121				CIRQ_GRP_INT120		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT127	Group 15
26:24	CIRQ_GRP_INT126	Group 15
22:20	CIRQ_GRP_INT125	Group 15
18:16	CIRQ_GRP_INT124	Group 15
14:12	CIRQ_GRP_INT123	Group 15
10:8	CIRQ_GRP_INT122	Group 15
6:4	CIRQ_GRP_INT121	Group 15
2:0	CIRQ_GRP_INT120	Group 15

102046C0 **CIRQ_GROP16** **Timer group setting of interrupt** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT135				CIRQ_GRP_INT134				CIRQ_GRP_INT133				CIRQ_GRP_INT132		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT131				CIRQ_GRP_INT130				CIRQ_GRP_INT129				CIRQ_GRP_INT128		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT135	Group 16
26:24	CIRQ_GRP_INT134	Group 16
22:20	CIRQ_GRP_INT133	Group 16
18:16	CIRQ_GRP_INT132	Group 16
14:12	CIRQ_GRP_INT131	Group 16
10:8	CIRQ_GRP_INT130	Group 16
6:4	CIRQ_GRP_INT129	Group 16
2:0	CIRQ_GRP_INT128	Group 16

102046C4 **CIRQ_GROP17** **Timer group setting of interrupt** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT143				CIRQ_GRP_INT142				CIRQ_GRP_INT141				CIRQ_GRP_INT140		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT139				CIRQ_GRP_INT138				CIRQ_GRP_INT137				CIRQ_GRP_INT136		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT143	Group 17
26:24	CIRQ_GRP_INT142	Group 17
22:20	CIRQ_GRP_INT141	Group 17
18:16	CIRQ_GRP_INT140	Group 17
14:12	CIRQ_GRP_INT139	Group 17
10:8	CIRQ_GRP_INT138	Group 17
6:4	CIRQ_GRP_INT137	Group 17
2:0	CIRQ_GRP_INT136	Group 17

102046C8 **CIRQ_GROP18** Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT151				CIRQ_GRP_INT150				CIRQ_GRP_INT149				CIRQ_GRP_INT148		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT147				CIRQ_GRP_INT146				CIRQ_GRP_INT145				CIRQ_GRP_INT144		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT151	Group 18
26:24	CIRQ_GRP_INT150	Group 18
22:20	CIRQ_GRP_INT149	Group 18
18:16	CIRQ_GRP_INT148	Group 18
14:12	CIRQ_GRP_INT147	Group 18
10:8	CIRQ_GRP_INT146	Group 18
6:4	CIRQ_GRP_INT145	Group 18
2:0	CIRQ_GRP_INT144	Group 18

102046CC CIRQ_GRP19 Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT159				CIRQ_GRP_INT158				CIRQ_GRP_INT157				CIRQ_GRP_INT156		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT155				CIRQ_GRP_INT154				CIRQ_GRP_INT153				CIRQ_GRP_INT152		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT159	Group 19
26:24	CIRQ_GRP_INT158	Group 19
22:20	CIRQ_GRP_INT157	Group 19
18:16	CIRQ_GRP_INT156	Group 19
14:12	CIRQ_GRP_INT155	Group 19
10:8	CIRQ_GRP_INT154	Group 19
6:4	CIRQ_GRP_INT153	Group 19
2:0	CIRQ_GRP_INT152	Group 19

102046D0 CIRQ_GROP20 Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT167				CIRQ_GRP_INT166				CIRQ_GRP_INT165				CIRQ_GRP_INT164		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT163				CIRQ_GRP_INT162				CIRQ_GRP_INT161				CIRQ_GRP_INT160		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT167	Group 20
26:24	CIRQ_GRP_INT166	Group 20
22:20	CIRQ_GRP_INT165	Group 20
18:16	CIRQ_GRP_INT164	Group 20
14:12	CIRQ_GRP_INT163	Group 20
10:8	CIRQ_GRP_INT162	Group 20
6:4	CIRQ_GRP_INT161	Group 20
2:0	CIRQ_GRP_INT160	Group 20

102046D4 CIRQ_GRP21 Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT175				CIRQ_GRP_INT174				CIRQ_GRP_INT173				CIRQ_GRP_INT172		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT171				CIRQ_GRP_INT170				CIRQ_GRP_INT169				CIRQ_GRP_INT168		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT175	Group 21
26:24	CIRQ_GRP_INT174	Group 21
22:20	CIRQ_GRP_INT173	Group 21
18:16	CIRQ_GRP_INT172	Group 21
14:12	CIRQ_GRP_INT171	Group 21
10:8	CIRQ_GRP_INT170	Group 21
6:4	CIRQ_GRP_INT169	Group 21
2:0	CIRQ_GRP_INT168	Group 21

102046D8 CIRQ_GRP22 Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT183				CIRQ_GRP_INT182				CIRQ_GRP_INT181				CIRQ_GRP_INT180		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT179				CIRQ_GRP_INT178				CIRQ_GRP_INT177				CIRQ_GRP_INT176		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT183	Group 22
26:24	CIRQ_GRP_INT182	Group 22
22:20	CIRQ_GRP_INT181	Group 22
18:16	CIRQ_GRP_INT180	Group 22
14:12	CIRQ_GRP_INT179	Group 22
10:8	CIRQ_GRP_INT178	Group 22
6:4	CIRQ_GRP_INT177	Group 22
2:0	CIRQ_GRP_INT176	Group 22

102046DC **CIRQ_GROP23** **Timer group setting of interrupt** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT191				CIRQ_GRP_INT190				CIRQ_GRP_INT189				CIRQ_GRP_INT188		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT187				CIRQ_GRP_INT186				CIRQ_GRP_INT185				CIRQ_GRP_INT184		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT191	Group 23
26:24	CIRQ_GRP_INT190	Group 23
22:20	CIRQ_GRP_INT189	Group 23
18:16	CIRQ_GRP_INT188	Group 23
14:12	CIRQ_GRP_INT187	Group 23
10:8	CIRQ_GRP_INT186	Group 23
6:4	CIRQ_GRP_INT185	Group 23
2:0	CIRQ_GRP_INT184	Group 23

102046E0 **CIRQ_GROP24** **Timer group setting of interrupt** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT199				CIRQ_GRP_INT198				CIRQ_GRP_INT197				CIRQ_GRP_INT196		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT195				CIRQ_GRP_INT194				CIRQ_GRP_INT193				CIRQ_GRP_INT192		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT199	Group 24
26:24	CIRQ_GRP_INT198	Group 24
22:20	CIRQ_GRP_INT197	Group 24
18:16	CIRQ_GRP_INT196	Group 24
14:12	CIRQ_GRP_INT195	Group 24
10:8	CIRQ_GRP_INT194	Group 24
6:4	CIRQ_GRP_INT193	Group 24
2:0	CIRQ_GRP_INT192	Group 24

102046E4 **CIRQ_GROP25** Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT207				CIRQ_GRP_INT206				CIRQ_GRP_INT205				CIRQ_GRP_INT204		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT203				CIRQ_GRP_INT202				CIRQ_GRP_INT201				CIRQ_GRP_INT200		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT207	Group 25
26:24	CIRQ_GRP_INT206	Group 25
22:20	CIRQ_GRP_INT205	Group 25
18:16	CIRQ_GRP_INT204	Group 25
14:12	CIRQ_GRP_INT203	Group 25
10:8	CIRQ_GRP_INT202	Group 25
6:4	CIRQ_GRP_INT201	Group 25
2:0	CIRQ_GRP_INT200	Group 25

102046E8 **CIRQ_GROP26** **Timer group setting of interrupt** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT215				CIRQ_GRP_INT214				CIRQ_GRP_INT213				CIRQ_GRP_INT212		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT211				CIRQ_GRP_INT210				CIRQ_GRP_INT209				CIRQ_GRP_INT208		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT215	Group 26
26:24	CIRQ_GRP_INT214	Group 26
22:20	CIRQ_GRP_INT213	Group 26
18:16	CIRQ_GRP_INT212	Group 26
14:12	CIRQ_GRP_INT211	Group 26
10:8	CIRQ_GRP_INT210	Group 26
6:4	CIRQ_GRP_INT209	Group 26
2:0	CIRQ_GRP_INT208	Group 26

102046EC **CIRQ_GROP27** **Timer group setting of interrupt** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT223				CIRQ_GRP_INT222				CIRQ_GRP_INT221				CIRQ_GRP_INT220		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT219				CIRQ_GRP_INT218				CIRQ_GRP_INT217				CIRQ_GRP_INT216		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT223	Group 27
26:24	CIRQ_GRP_INT222	Group 27
22:20	CIRQ_GRP_INT221	Group 27
18:16	CIRQ_GRP_INT220	Group 27
14:12	CIRQ_GRP_INT219	Group 27
10:8	CIRQ_GRP_INT218	Group 27
6:4	CIRQ_GRP_INT217	Group 27
2:0	CIRQ_GRP_INT216	Group 27

102046F0 **CIRQ_GROP28** Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT231				CIRQ_GRP_INT230				CIRQ_GRP_INT229				CIRQ_GRP_INT228		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT227				CIRQ_GRP_INT226				CIRQ_GRP_INT225				CIRQ_GRP_INT224		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT231	Group 28
26:24	CIRQ_GRP_INT230	Group 28
22:20	CIRQ_GRP_INT229	Group 28
18:16	CIRQ_GRP_INT228	Group 28
14:12	CIRQ_GRP_INT227	Group 28
10:8	CIRQ_GRP_INT226	Group 28
6:4	CIRQ_GRP_INT225	Group 28
2:0	CIRQ_GRP_INT224	Group 28

102046F4 **CIRQ_GROP29** **Timer group setting of interrupt** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT239				CIRQ_GRP_INT238				CIRQ_GRP_INT237				CIRQ_GRP_INT236		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT235				CIRQ_GRP_INT234				CIRQ_GRP_INT233				CIRQ_GRP_INT232		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT239	Group 29
26:24	CIRQ_GRP_INT238	Group 29
22:20	CIRQ_GRP_INT237	Group 29
18:16	CIRQ_GRP_INT236	Group 29
14:12	CIRQ_GRP_INT235	Group 29
10:8	CIRQ_GRP_INT234	Group 29
6:4	CIRQ_GRP_INT233	Group 29
2:0	CIRQ_GRP_INT232	Group 29

102046F8 CIRQ_GROP30 Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT247				CIRQ_GRP_INT246				CIRQ_GRP_INT245				CIRQ_GRP_INT244		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT243				CIRQ_GRP_INT242				CIRQ_GRP_INT241				CIRQ_GRP_INT240		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT247	Group 30
26:24	CIRQ_GRP_INT246	Group 30
22:20	CIRQ_GRP_INT245	Group 30
18:16	CIRQ_GRP_INT244	Group 30
14:12	CIRQ_GRP_INT243	Group 30
10:8	CIRQ_GRP_INT242	Group 30
6:4	CIRQ_GRP_INT241	Group 30
2:0	CIRQ_GRP_INT240	Group 30

102046FC CIRQ_GRP31 Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT255				CIRQ_GRP_INT254				CIRQ_GRP_INT253				CIRQ_GRP_INT252		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT251				CIRQ_GRP_INT250				CIRQ_GRP_INT249				CIRQ_GRP_INT248		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT255	Group 31
26:24	CIRQ_GRP_INT254	Group 31
22:20	CIRQ_GRP_INT253	Group 31
18:16	CIRQ_GRP_INT252	Group 31
14:12	CIRQ_GRP_INT251	Group 31
10:8	CIRQ_GRP_INT250	Group 31
6:4	CIRQ_GRP_INT249	Group 31
2:0	CIRQ_GRP_INT248	Group 31

10204700 CIRQ_GROP32 Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT263				CIRQ_GRP_INT262				CIRQ_GRP_INT261				CIRQ_GRP_INT260		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT259				CIRQ_GRP_INT258				CIRQ_GRP_INT257				CIRQ_GRP_INT256		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT263	Group 32
26:24	CIRQ_GRP_INT262	Group 32
22:20	CIRQ_GRP_INT261	Group 32
18:16	CIRQ_GRP_INT260	Group 32
14:12	CIRQ_GRP_INT259	Group 32
10:8	CIRQ_GRP_INT258	Group 32
6:4	CIRQ_GRP_INT257	Group 32
2:0	CIRQ_GRP_INT256	Group 32

10204704 **CIRQ_GROP33** Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_GRP_INT271				CIRQ_GRP_INT270				CIRQ_GRP_INT269				CIRQ_GRP_INT268		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT267				CIRQ_GRP_INT266				CIRQ_GRP_INT265				CIRQ_GRP_INT264		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	CIRQ_GRP_INT271	Group 33
26:24	CIRQ_GRP_INT270	Group 33
22:20	CIRQ_GRP_INT269	Group 33
18:16	CIRQ_GRP_INT268	Group 33
14:12	CIRQ_GRP_INT267	Group 33
10:8	CIRQ_GRP_INT266	Group 33
6:4	CIRQ_GRP_INT265	Group 33
2:0	CIRQ_GRP_INT264	Group 33

10204708 CIRQ_GROP34 Timer group setting of interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CIRQ_GRP_INT275				CIRQ_GRP_INT274				CIRQ_GRP_INT273				CIRQ_GRP_INT272		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
14:12	CIRQ_GRP_INT275	Group 34
10:8	CIRQ_GRP_INT274	Group 34
6:4	CIRQ_GRP_INT273	Group 34
2:0	CIRQ_GRP_INT272	Group 34

10204880 LATCH_OF_CIRQ_STATUS_NEXT Latch of CORQ_STATUS_NEXT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LATCH_OF_CIRQ_STATUS_NEXT0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LATCH_OF_CIRQ_STATUS_NEXT0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LATCH_OF_CIRQ_STATUS_NEXT0	Latch of cirq_status_next for Interrupts 0 to 31

10204884 LATCH_OF_CIRQ_STATUS_NE Latch of CORQ_STATUS_NEXT

00000000

XT1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LATCH_OF_CIRQ_STATUS_NEXT1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LATCH_OF_CIRQ_STATUS_NEXT1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LATCH_OF_CIRQ_STATUS_NEXT1	Latch of cirq_status_next for Interrupts 32 to 63

10204888 LATCH_OF_CIRQ_STATUS_NE Latch of CORQ_STATUS_NEXT

00000000

XT2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LATCH_OF_CIRQ_STATUS_NEXT2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LATCH_OF_CIRQ_STATUS_NEXT2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LATCH_OF_CIRQ_STATUS_NEXT2	Latch of cirq_status_next for Interrupts 64 to 95

1020488C **LATCH_OF_CIRQ_STATUS_NE Latch of CORQ_STATUS_NEXT**
XT3
00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LATCH_OF_CIRQ_STATUS_NEXT3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LATCH_OF_CIRQ_STATUS_NEXT3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LATCH_OF_CIRQ_STATUS_NEXT3	Latch of cirq_status_next for Interrupts 96 to 127

10204890 **LATCH_OF_CIRQ_STATUS_NE Latch of CORQ_STATUS_NEXT**
XT4
00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LATCH_OF_CIRQ_STATUS_NEXT4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LATCH_OF_CIRQ_STATUS_NEXT4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LATCH_OF_CIRQ_STATUS_NEXT4	Latch of cirq_status_next for Interrupts 128 to 159

10204894 LATCH_OF_CIRQ_STATUS_NE Latch of CORQ_STATUS_NEXT

00000000

XT5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LATCH_OF_CIRQ_STATUS_NEXT5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LATCH_OF_CIRQ_STATUS_NEXT5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LATCH_OF_CIRQ_STATUS_NEXT5	Latch of cirq_status_next for Interrupts 160 to 191

10204898 LATCH_OF_CIRQ_STATUS_NE Latch of CORQ_STATUS_NEXT

00000000

XT6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LATCH_OF_CIRQ_STATUS_NEXT6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LATCH_OF_CIRQ_STATUS_NEXT6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LATCH_OF_CIRQ_STATUS_NEXT6	Latch of cirq_status_next for Interrupts 192 to 223

1020489C LATCH_OF_CIRQ_STATUS_NEXT Latch of CIRQ_STATUS_NEXT
XTZ

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LATCH_OF_CIRQ_STATUS_NEXT7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	LATCH_OF_CIRQ_STATUS_NEXT7	Latch of cirq_status_next for Interrupts 224 to 255

1.4 AP_DMA (Application Processor Direct Memory Access)

1.4.1 Register Definition

Module name: AP_DMA Base address: (+0x10217000)

Address	Name	Width	Register Function
10217020	<u>AP_DMA_GLOBAL_INT_FLAG</u>	32	AP DMA global interrupt flag register
10217004	<u>AP_DMA_GLOBAL_RST</u>	32	AP DMA reset register
10217024	<u>AP_DMA_GLOBAL_RUNNING_STATUS</u>	32	AP DMA global running status register
1021700C	<u>AP_DMA_GLOBAL_SLOW_DOWN</u>	32	AP DMA AXI slow down register
10217010	<u>AP_DMA_GLOBAL_SEC_EN</u>	32	AP DMA security enable register
10217080	<u>AP_DMA_I2C0_CHN_INT_FLAG</u>	32	Peripheral DMA interrupt flag register
10217084	<u>AP_DMA_I2C0_CHN_INT_EN</u>	32	Peripheral DMA interrupt enable register
10217088	<u>AP_DMA_I2C0_CHN_EN</u>	32	Peripheral DMA enable register
1021708C	<u>AP_DMA_I2C0_CHN_RST</u>	32	Peripheral DMA reset register
10217090	<u>AP_DMA_I2C0_CHN_STOP</u>	32	Peripheral DMA enable register
10217094	<u>AP_DMA_I2C0_CHN_FLUSH</u>	32	Peripheral DMA flush register
10217098	<u>AP_DMA_I2C0_CHN_CON</u>	32	Peripheral DMA control register
1021709C	<u>AP_DMA_I2C0_CHN_TX_MEM_ADDR</u>	32	Peripheral DMA memory address register
102170A0	<u>AP_DMA_I2C0_CHN_RX_MEM_ADDR</u>	32	Peripheral DMA memory address register
102170A4	<u>AP_DMA_I2C0_CHN_TX_LEN</u>	32	Peripheral DMA transfer length register
102170A8	<u>AP_DMA_I2C0_CHN_RX_LEN</u>	32	Peripheral DMA transfer length register
102170B8	<u>AP_DMA_I2C0_CHN_INT_BUF_SIZE</u>	32	Peripheral DMA internal buffer size register
102170D4	<u>AP_DMA_I2C0_CHN_TX_MEM_ADDR2</u>	32	Peripheral DMA memory address register
102170D8	<u>AP_DMA_I2C0_CHN_RX_MEM_ADDR2</u>	32	Peripheral DMA memory address register
10217100	<u>AP_DMA_I2C1_CHN_INT_FLAG</u>	32	Peripheral DMA interrupt flag register
10217104	<u>AP_DMA_I2C1_CHN_INT_EN</u>	32	Peripheral DMA interrupt enable register
10217108	<u>AP_DMA_I2C1_CHN_EN</u>	32	Peripheral DMA enable register
1021710C	<u>AP_DMA_I2C1_CHN_RST</u>	32	Peripheral DMA reset register
10217110	<u>AP_DMA_I2C1_CHN_STOP</u>	32	Peripheral DMA enable register
10217114	<u>AP_DMA_I2C1_CHN_FLUSH</u>	32	Peripheral DMA flush register
10217118	<u>AP_DMA_I2C1_CHN_CON</u>	32	Peripheral DMA control register
1021711C	<u>AP_DMA_I2C1_CHN_TX_MEM_ADDR</u>	32	Peripheral DMA memory address register
10217120	<u>AP_DMA_I2C1_CHN_RX_MEM_ADDR</u>	32	Peripheral DMA memory address register
10217124	<u>AP_DMA_I2C1_CHN_TX_LEN</u>	32	Peripheral DMA transfer length register
10217128	<u>AP_DMA_I2C1_CHN_RX_LEN</u>	32	Peripheral DMA transfer length register
10217138	<u>AP_DMA_I2C1_CHN_INT_BUF_SIZE</u>	32	Peripheral DMA internal buffer size register
10217154	<u>AP_DMA_I2C1_CHN_TX_MEM_ADDR2</u>	32	Peripheral DMA memory address register

Address	Name	Width	Register Function
10217158	<u>AP_DMA_I2C1_CHN_RX_MEM_ADDR2</u>	32	Peripheral DMA memory address register
10217180	<u>AP_DMA_I2C2_CHN_INT_FLAG</u>	32	Peripheral DMA interrupt flag register
10217184	<u>AP_DMA_I2C2_CHN_INT_EN</u>	32	Peripheral DMA interrupt enable register
10217188	<u>AP_DMA_I2C2_CHN_EN</u>	32	Peripheral DMA enable register
1021718C	<u>AP_DMA_I2C2_CHN_RST</u>	32	Peripheral DMA reset register
10217190	<u>AP_DMA_I2C2_CHN_STOP</u>	32	Peripheral DMA enable register
10217194	<u>AP_DMA_I2C2_CHN_FLUSH</u>	32	Peripheral DMA flush register
10217198	<u>AP_DMA_I2C2_CHN_CON</u>	32	Peripheral DMA control register
1021719C	<u>AP_DMA_I2C2_CHN_TX_MEM_ADDR</u>	32	Peripheral DMA memory address register
102171A0	<u>AP_DMA_I2C2_CHN_RX_MEM_ADDR</u>	32	Peripheral DMA memory address register
102171A4	<u>AP_DMA_I2C2_CHN_TX_LEN</u>	32	Peripheral DMA transfer length register
102171A8	<u>AP_DMA_I2C2_CHN_RX_LEN</u>	32	Peripheral DMA transfer length register
102171B8	<u>AP_DMA_I2C2_CHN_INT_BUF_SIZE</u>	32	Peripheral DMA internal buffer size register
102171D4	<u>AP_DMA_I2C2_CHN_TX_MEM_ADDR2</u>	32	Peripheral DMA memory address register
102171D8	<u>AP_DMA_I2C2_CHN_RX_MEM_ADDR2</u>	32	Peripheral DMA memory address register
10217200	<u>AP_DMA_UART_0_TX_INT_FLAG</u>	32	UART TX virtual FIFO interrupt flag register
10217204	<u>AP_DMA_UART_0_TX_INT_EN</u>	32	UART TX virtual FIFO interrupt enable register
10217208	<u>AP_DMA_UART_0_TX_EN</u>	32	UART TX virtual FIFO enable register
1021720C	<u>AP_DMA_UART_0_TX_RST</u>	32	UART TX virtual FIFO reset register
10217210	<u>AP_DMA_UART_0_TX_STOP</u>	32	UART TX virtual FIFO enable register
10217214	<u>AP_DMA_UART_0_TX_FLUSH</u>	32	UART TX virtual FIFO flush register
1021721C	<u>AP_DMA_UART_0_TX_VFF_ADDR</u>	32	UART TX virtual FIFO base address register
10217224	<u>AP_DMA_UART_0_TX_VFF_LEN</u>	32	UART TX virtual FIFO length register
10217228	<u>AP_DMA_UART_0_TX_VFF_THRE</u>	32	UART TX virtual FIFO threshold register
1021722C	<u>AP_DMA_UART_0_TX_VFF_WRITE_PT</u>	32	UART TX virtual FIFO write pointer register
10217230	<u>AP_DMA_UART_0_TX_VFF_READ_PT</u>	32	UART TX virtual FIFO read pointer register
10217238	<u>AP_DMA_UART_0_TX_INT_BUF_SIZE</u>	32	UART TX internal buffer size register
1021723C	<u>AP_DMA_UART_0_TX_VFF_VALID_SIZE</u>	32	UART TX virtual FIFO valid size register
10217240	<u>AP_DMA_UART_0_TX_VFF_LEFT_SIZE</u>	32	UART TX virtual FIFO left size register
10217254	<u>AP_DMA_UART_0_TX_VFF_ADDR2</u>	32	UART TX virtual FIFO base address register
10217258	<u>AP_DMA_UART_0_TX_VFF_WRITE_PT_VALID</u>	32	UART TX virtual FIFO write pointer register by HW control
1021725C	<u>AP_DMA_UART_0_TX_VFF_WRITE_PT_VALID2</u>	32	UART TX virtual FIFO write pointer register by HW control

Address	Name	Width	Register Function
10217260	<u>AP DMA UART 0 TX FLUSH ACT</u>	32	UART TX virtual FIFO flush status register
10217264	<u>AP DMA UART 0 TX HW FLUSH</u>	32	UART TX virtual FIFO HW flush register
10217268	<u>AP DMA UART 0 TX VFF WPT REAL</u>	32	UART TX virtual FIFO write pointer register Value
10217280	<u>AP DMA UART 0 RX INT FLAG</u>	32	UART RX virtual FIFO interrupt flag register
10217284	<u>AP DMA UART 0 RX INT EN</u>	32	UART RX virtual FIFO interrupt enable register
10217288	<u>AP DMA UART 0 RX EN</u>	32	UART RX virtual FIFO enable register
1021728C	<u>AP DMA UART 0 RX RST</u>	32	UART RX virtual FIFO reset register
10217290	<u>AP DMA UART 0 RX STOP</u>	32	UART RX virtual FIFO enable register
10217294	<u>AP DMA UART 0 RX FLUSH</u>	32	UART RX virtual FIFO flush register
1021729C	<u>AP DMA UART 0 RX VFF ADDR</u>	32	UART RX virtual FIFO base address register
102172A4	<u>AP DMA UART 0 RX VFF LEN</u>	32	UART RX virtual FIFO length register
102172A8	<u>AP DMA UART 0 RX VFF THRE</u>	32	UART RX virtual FIFO threshold register
102172AC	<u>AP DMA UART 0 RX VFF WPT</u>	32	UART RX virtual FIFO write pointer register
102172B0	<u>AP DMA UART 0 RX VFF RPT</u>	32	UART RX virtual FIFO read pointer register
102172B4	<u>AP DMA UART 0 RX FLOW CTRL THRE</u>	32	UART RX virtual FIFO flow control threshold
102172B8	<u>AP DMA UART 0 RX INT BUF SIZE</u>	32	UART RX internal buffer size register
102172BC	<u>AP DMA UART 0 RX VFF VALID SIZE</u>	32	UART RX virtual FIFO valid size register
102172C0	<u>AP DMA UART 0 RX VFF LEFT SIZE</u>	32	UART RX virtual FIFO left size register
102172D4	<u>AP DMA UART 0 RX VFF ADDR2</u>	32	UART RX virtual FIFO base address register
10217300	<u>AP DMA UART 1 TX INT FLAG</u>	32	UART TX virtual FIFO interrupt flag register
10217304	<u>AP DMA UART 1 TX INT EN</u>	32	UART TX virtual FIFO interrupt enable register
10217308	<u>AP DMA UART 1 TX EN</u>	32	UART TX virtual FIFO enable register
1021730C	<u>AP DMA UART 1 TX RST</u>	32	UART TX virtual FIFO reset register
10217310	<u>AP DMA UART 1 TX STOP</u>	32	UART TX virtual FIFO enable register
10217314	<u>AP DMA UART 1 TX FLUSH</u>	32	UART TX virtual FIFO flush register
1021731C	<u>AP DMA UART 1 TX VFF ADDR</u>	32	UART TX virtual FIFO base address register
10217324	<u>AP DMA UART 1 TX VFF LEN</u>	32	UART TX virtual FIFO length register
10217328	<u>AP DMA UART 1 TX VFF THRE</u>	32	UART TX virtual FIFO threshold register
1021732C	<u>AP DMA UART 1 TX VFF WPT</u>	32	UART TX virtual FIFO write pointer register
10217330	<u>AP DMA UART 1 TX VFF RPT</u>	32	UART TX virtual FIFO read pointer register

Address	Name	Width	Register Function
10217338	<u>AP_DMA_UART_1_TX_INT_BUF_SIZE</u>	32	UART TX internal buffer size register
1021733C	<u>AP_DMA_UART_1_TX_VFF_VALID_SIZE</u>	32	UART TX virtual FIFO valid size register
10217340	<u>AP_DMA_UART_1_TX_VFF_LEFT_SIZE</u>	32	UART TX virtual FIFO left size register
10217354	<u>AP_DMA_UART_1_TX_VFF_ADDR2</u>	32	UART TX virtual FIFO base address register
10217358	<u>AP_DMA_UART_1_TX_VFF_WRITE_POINTER_VALID</u>	32	UART TX virtual FIFO write pointer register by HW control
1021735C	<u>AP_DMA_UART_1_TX_VFF_WRITE_POINTER_VALID2</u>	32	UART TX virtual FIFO write pointer register by HW control
10217360	<u>AP_DMA_UART_1_TX_FLUSH_ACT</u>	32	UART TX virtual FIFO flush status register
10217364	<u>AP_DMA_UART_1_TX_HW_FLUSH</u>	32	UART TX virtual FIFO HW flush register
10217368	<u>AP_DMA_UART_1_TX_VFF_WRITE_POINTER_REAL</u>	32	UART TX virtual FIFO write pointer register Value
10217380	<u>AP_DMA_UART_1_RX_INT_FLAG</u>	32	UART RX virtual FIFO interrupt flag register
10217384	<u>AP_DMA_UART_1_RX_INT_ENABLE</u>	32	UART RX virtual FIFO interrupt enable register
10217388	<u>AP_DMA_UART_1_RX_ENABLE</u>	32	UART RX virtual FIFO enable register
1021738C	<u>AP_DMA_UART_1_RX_RST</u>	32	UART RX virtual FIFO reset register
10217390	<u>AP_DMA_UART_1_RX_STOP</u>	32	UART RX virtual FIFO enable register
10217394	<u>AP_DMA_UART_1_RX_FLUSH</u>	32	UART RX virtual FIFO flush register
1021739C	<u>AP_DMA_UART_1_RX_VFF_ADDR</u>	32	UART RX virtual FIFO base address register
102173A4	<u>AP_DMA_UART_1_RX_VFF_LENGTH</u>	32	UART RX virtual FIFO length register
102173A8	<u>AP_DMA_UART_1_RX_VFF_THRESHOLD</u>	32	UART RX virtual FIFO threshold register
102173AC	<u>AP_DMA_UART_1_RX_VFF_WRITE_POINTER</u>	32	UART RX virtual FIFO write pointer register
102173B0	<u>AP_DMA_UART_1_RX_VFF_READ_POINTER</u>	32	UART RX virtual FIFO read pointer register
102173B4	<u>AP_DMA_UART_1_RX_FLOW_CTRL_THRE</u>	32	UART RX virtual FIFO flow control threshold
102173B8	<u>AP_DMA_UART_1_RX_INT_BUF_SIZE</u>	32	UART RX internal buffer size register
102173BC	<u>AP_DMA_UART_1_RX_VFF_VALID_SIZE</u>	32	UART RX virtual FIFO valid size register
102173C0	<u>AP_DMA_UART_1_RX_VFF_LEFT_SIZE</u>	32	UART RX virtual FIFO left size register
102173D4	<u>AP_DMA_UART_1_RX_VFF_ADDR2</u>	32	UART RX virtual FIFO base address register
10217400	<u>AP_DMA_UART_2_TX_INT_FLAG</u>	32	UART TX virtual FIFO interrupt flag register
10217404	<u>AP_DMA_UART_2_TX_INT_ENABLE</u>	32	UART TX virtual FIFO interrupt enable register
10217408	<u>AP_DMA_UART_2_TX_ENABLE</u>	32	UART TX virtual FIFO enable register
1021740C	<u>AP_DMA_UART_2_TX_RST</u>	32	UART TX virtual FIFO reset register
10217410	<u>AP_DMA_UART_2_TX_STOP</u>	32	UART TX virtual FIFO enable register

Address	Name	Width	Register Function
10217414	<u>AP_DMA_UART_2_TX_FLUSH</u>	32	UART TX virtual FIFO flush register
1021741C	<u>AP_DMA_UART_2_TX_VFF_A</u> <u>DDR</u>	32	UART TX virtual FIFO base address register
10217424	<u>AP_DMA_UART_2_TX_VFF_LE</u> <u>N</u>	32	UART TX virtual FIFO length register
10217428	<u>AP_DMA_UART_2_TX_VFF_T</u> <u>HRE</u>	32	UART TX virtual FIFO threshold register
1021742C	<u>AP_DMA_UART_2_TX_VFF_W</u> <u>PT</u>	32	UART TX virtual FIFO write pointer register
10217430	<u>AP_DMA_UART_2_TX_VFF_R</u> <u>PT</u>	32	UART TX virtual FIFO read pointer register
10217438	<u>AP_DMA_UART_2_TX_INT_B</u> <u>UF_SIZE</u>	32	UART TX internal buffer size register
1021743C	<u>AP_DMA_UART_2_TX_VFF_V</u> <u>ALID_SIZE</u>	32	UART TX virtual FIFO valid size register
10217440	<u>AP_DMA_UART_2_TX_VFF_LE</u> <u>FT_SIZE</u>	32	UART TX virtual FIFO left size register
10217454	<u>AP_DMA_UART_2_TX_VFF_A</u> <u>DDR2</u>	32	UART TX virtual FIFO base address register
10217458	<u>AP_DMA_UART_2_TX_VFF_W</u> <u>PT_VALID</u>	32	UART TX virtual FIFO write pointer register by HW control
1021745C	<u>AP_DMA_UART_2_TX_VFF_W</u> <u>PT_VALID2</u>	32	UART TX virtual FIFO write pointer register by HW control
10217460	<u>AP_DMA_UART_2_TX_FLUSH</u> <u>ACT</u>	32	UART TX virtual FIFO flush status register
10217464	<u>AP_DMA_UART_2_TX_HW_FL</u> <u>USH</u>	32	UART TX virtual FIFO HW flush register
10217468	<u>AP_DMA_UART_2_TX_VFF_W</u> <u>PT_REAL</u>	32	UART TX virtual FIFO write pointer register Value
10217480	<u>AP_DMA_UART_2_RX_INT_FL</u> <u>AG</u>	32	UART RX virtual FIFO interrupt flag register
10217484	<u>AP_DMA_UART_2_RX_INT_E</u> <u>N</u>	32	UART RX virtual FIFO interrupt enable register
10217488	<u>AP_DMA_UART_2_RX_EN</u>	32	UART RX virtual FIFO enable register
1021748C	<u>AP_DMA_UART_2_RX_RST</u>	32	UART RX virtual FIFO reset register
10217490	<u>AP_DMA_UART_2_RX_STOP</u>	32	UART RX virtual FIFO enable register
10217494	<u>AP_DMA_UART_2_RX_FLUSH</u>	32	UART RX virtual FIFO flush register
1021749C	<u>AP_DMA_UART_2_RX_VFF_A</u> <u>DDR</u>	32	UART RX virtual FIFO base address register
102174A4	<u>AP_DMA_UART_2_RX_VFF_LE</u> <u>N</u>	32	UART RX virtual FIFO length register
102174A8	<u>AP_DMA_UART_2_RX_VFF_T</u> <u>HRE</u>	32	UART RX virtual FIFO threshold register
102174AC	<u>AP_DMA_UART_2_RX_VFF_W</u> <u>PT</u>	32	UART RX virtual FIFO write pointer register
102174B0	<u>AP_DMA_UART_2_RX_VFF_R</u> <u>PT</u>	32	UART RX virtual FIFO read pointer register
102174B4	<u>AP_DMA_UART_2_RX_FLOW</u> <u>CTRL_THRE</u>	32	UART RX virtual FIFO flow control threshold
102174B8	<u>AP_DMA_UART_2_RX_INT_B</u> <u>UF_SIZE</u>	32	UART RX internal buffer size register
102174BC	<u>AP_DMA_UART_2_RX_VFF_V</u> <u>ALID_SIZE</u>	32	UART RX virtual FIFO valid size register

Address	Name	Width	Register Function
102174C0	<u>AP_DMA_UART_2_RX_VFF_LEFT_SIZE</u>	32	UART RX virtual FIFO left size register
102174D4	<u>AP_DMA_UART_2_RX_VFF_ADDRESS2</u>	32	UART RX virtual FIFO base address register

10217020 AP_DMA_GLOBAL_INT_FLAG AP DMA global interrupt flag register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								UART2_RX	UART2_TX	UART1_RX	UART1_TX	UART0_RX	UART0_TX	I2C2	I2C1	I2C0
Type								RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	UART2_RX	UART2 RX interrupt 0: No interrupt event 1: Interrupt event occurred
7	UART2_TX	UART2 TX interrupt 0: No interrupt event 1: Interrupt event occurred
6	UART1_RX	UART1 RX interrupt 0: No interrupt event 1: Interrupt event occurred
5	UART1_TX	UART1 TX interrupt 0: No interrupt event 1: Interrupt event occurred
4	UART0_RX	UART0 RX interrupt 0: No interrupt event 1: Interrupt event occurred
3	UART0_TX	UART0 TX interrupt 0: No interrupt event 1: Interrupt event occurred
2	I2C2	I2C2 interrupt 0: No interrupt event 1: Interrupt event occurred
1	I2C1	I2C1 interrupt 0: No interrupt event 1: Interrupt event occurred

Bit(s)	Name	Description
0	I2C0	I2C0 interrupt 0: No interrupt event 1: Interrupt event occurred

10217004	AP_DMA_GLOBAL_RST					AP DMA reset register										00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	General DMA hard reset (reset regardless of the current transaction) SW sets hard_rst to 1 and then back to 0 to finish the reset mechanism 0: Disable 1: Enable
0	WARM_RST	General DMA warm reset (after the current transaction) SW sets warm_rst to 1 and waits until all running statuses to become 0. SW then sets warm_rst back to 0 to finish the reset mechanism 0: Disable 1: Enable

10217024 **AP_DMA_GLOBAL_RUNNING** AP DMA global running status register
STATUS

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								UART2_RX	UART2_TX	UART1_RX	UART1_TX	UART0_RX	UART0_TX	I2C2	I2C1	I2C0
Type								RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	UART2_RX	0: Idle 1: Running
7	UART2_TX	0: Idle 1: Running
6	UART1_RX	0: Idle 1: Running
5	UART1_TX	0: Idle 1: Running
4	UART0_RX	0: Idle 1: Running
3	UART0_TX	0: Idle 1: Running
2	I2C2	0: Idle 1: Running
1	I2C1	0: Idle 1: Running
0	I2C0	0: Idle 1: Running

1021700C **AP_DMA_GLOBAL_SLOW_DOWN** AP DMA AXI slow down register
WN

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	W_SLOW_CNT															W_SLOW_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0						0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R_SLOW_CNT															R_SLOW_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0						0

Bit(s)	Name	Description
31:22	W_SLOW_CNT	AXI write to external AXI slow-down counter (0 to 1023) The number means cycle 0: Wait for 0 cycle and then issue request 1: Wait for 1 cycle and then issue request
16	W_SLOW_EN	Enables AXI write to external AXI slow-down 0: Do not slow down 1: Slow down
15:6	R_SLOW_CNT	AXI read from external AXI slow-down counter (0 to 1023) The number means cycle 0: Wait for 0 cycle and then issue request 1: Wait for 1 cycle and then issue request
0	R_SLOW_EN	Enables Arm-side AXI read from external AXI slow-down 0: Do not slow down 1: Slow down

10217010 AP_DMA_GLOBAL_SEC_EN AP DMA security enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LOCK	DLOCK														
Type	RW	RW														
Reset	0	0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	LOCK	Locks the secure bit 0: Unlock channel secure bit write 1: Lock channel secure bit
30	DLOCK	Locks the domain registers 0: Unlock channel domain register write 1: Lock channel domain register write

10217080 AP_DMA_I2C0_CHN_INT_FLA Peripheral DMA interrupt flag register

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RX_FLAG	TX_FLAG
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RX_FLAG	Raised when RX DMA is finished. Write 0 to clear.
0	TX_FLAG	This flag is raised when TX DMA is finished. Write 0 to clear. - After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. - If STOP = 1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. - If FLUSH = 1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. - If WARM_RST = 1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. - If HARD_RST = 1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

10217084 AP_DMA_I2C0_CHN_INT_EN Peripheral DMA interrupt enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN_RX_FLAG	INTEN_TX_FLAG
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN_RX_FLAG	Enables interrupt for RX_FLAG 0: Disable 1: Enable
0	INTEN_TX_FLAG	Enables interrupt for TX_FLAG 0: Disable 1: Enable

10217088 AP_DMA_I2C0_CHN_EN Peripheral DMA enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	Enables peripheral DMA Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1021708C AP_DMA_I2C0_CHN_RST Peripheral DMA reset register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	Peripheral DMA hard reset (reset regardless of the current transaction) SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	Peripheral DMA warm reset (after the current transaction) SW sets WARM_RST to 1 and waits for EN to become 0. HW automatically sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217090 AP_DMA_I2C0_CHN_STOP Peripheral DMA enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	Pauses peripheral DMA Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	Stops peripheral DMA Set to 1 to stop DMA and wait for EN to become 0. HW then automatically sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

10217094 AP_DMA_I2C0_CHN_FLUSH Peripheral DMA flush register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	Flushes peripheral DMA Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

10217098 AP_DMA_I2C0_CHN_CON Peripheral DMA control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							dir_change	addr_ctrl			align	skip_config	req_blk	async_mode	FIX_EN	DIR
Type							RW	RW			RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	dir_change	If I2C needs direction change, please set 1.
8:6	addr_ctrl	Make this reg as default.
5	align	Make this reg as default. 0: Half word align 1: Word align
4	skip_config	Please config 1 as I2C setting. 0: Config 1: No config
3	req_blk	Make this reg as default. 0: Request block 1: Non-request block
2	async_mode	Please config 1 as I2C setting. 0: Old hand-shake 1: New hand-shake
1	FIX_EN	Peripheral DMA fixed pattern When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as TX. 0: Do not use fixed pattern 1: Use fixed pattern
0	DIR	Half duplex peripheral DMA direction 0: TX 1: RX

1021709C AP_DMA_I2C0_CHN_TX_ME Peripheral DMA memory address register

00000000

M_ADDR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	Peripheral DMA memory address It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. DO NOT set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when users use SYSRAM as a destination, e.g. 0xff9 ~ 0xff are not allowed to be TX_MEM_ADDR when users use SYSRAM as a source memory.

102170A0 AP_DMA_I2C0_CHN_RX_ME Peripheral DMA memory address register

00000000

M_ADDR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	Peripheral DMA memory address It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when users use SYSRAM as a destination, e.g. 0xff9 ~ 0xff are not allowed to be RX_MEM_ADDR when users use SYSRAM as a destination memory.

102170A4 AP_DMA_I2C0_CHN_TX_LEN Peripheral DMA transfer length register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	Peripheral DMA transfer length It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

102170A8 AP_DMA_I2C0_CHN_RX_LEN Peripheral DMA transfer length register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	Peripheral DMA transfer length It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

102170B8 AP_DMA_I2C0_CHN_INT_BUF Peripheral DMA internal buffer size register 00000000
SIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	Byte size in internal buffer

102170D4 AP_DMA_I2C0_CHN_TX_ME Peripheral DMA memory address register 00000000
M_ADDR2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TX_MEM_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

102170D8 AP_DMA_I2C0_CHN_RX_ME Peripheral DMA memory address register 00000000
M_ADDR2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RX_MEM_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

10217100 AP_DMA_I2C1_CHN_INT_FLG Peripheral DMA interrupt flag register 00000000
G

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RX_FLAG	TX_FLAG
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RX_FLAG	Raised when RX DMA is finished. Write 0 to clear.
0	TX_FLAG	This flag is raised when TX DMA is finished. Write 0 to clear. - After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. - If STOP = 1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. - If FLUSH = 1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. - If WARM_RST = 1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. - If HARD_RST = 1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

10217104 AP_DMA_I2C1_CHN_INT_EN Peripheral DMA interrupt enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN_RX_FLAG	INTEN_TX_FLAG
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN_RX_FLAG	Enables interrupt for RX_FLAG 0: Disable 1: Enable
0	INTEN_TX_FLAG	Enables interrupt for TX_FLAG 0: Disable 1: Enable

10217108 AP_DMA_I2C1_CHN_EN Peripheral DMA enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	Enables peripheral DMA Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1021710C AP_DMA_I2C1_CHN_RST Peripheral DMA reset register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	Peripheral DMA hard reset (reset regardless of the current transaction) SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	Peripheral DMA warm reset (after the current transaction) SW sets WARM_RST to 1 and waits for EN to become 0. HW automatically sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217110 AP_DMA_I2C1_CHN_STOP Peripheral DMA enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	Pauses peripheral DMA Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	Stops peripheral DMA Set to 1 to stop DMA and wait for EN to become 0. HW then automatically sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

10217114 AP_DMA_I2C1_CHN_FLUSH Peripheral DMA flush register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	Flushes peripheral DMA Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

10217118 AP_DMA_I2C1_CHN_CON Peripheral DMA control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							dir_change	addr_ctrl			align	skip_config	req_blk	async_mode	FIX_EN	DIR
Type							RW	RW			RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	dir_change	If I2C needs direction change, please set 1.
8:6	addr_ctrl	Make this reg as default.
5	align	Make this reg as default. 0: Half word align 1: Word align
4	skip_config	Please config 1 as I2C setting. 0: Config 1: No config
3	req_blk	Make this reg as default. 0: Request block 1: Non-request block
2	async_mode	Please config 1 as I2C setting. 0: Old hand-shake 1: New hand-shake
1	FIX_EN	Peripheral DMA fixed pattern When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as TX. 0: Do not use fixed pattern 1: Use fixed pattern
0	DIR	Half duplex peripheral DMA direction 0: TX 1: RX

1021711C AP_DMA_I2C1_CHN_TX_ME Peripheral DMA memory address register 00000000
M_ADDR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	Peripheral DMA memory address It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. DO NOT set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when users use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when users use SYSRAM as a source memory.

10217120 AP_DMA_I2C1_CHN_RX_ME Peripheral DMA memory address register 00000000
M_ADDR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	Peripheral DMA memory address It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when users use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when users use SYSRAM as a destination memory.

10217124 AP_DMA_I2C1_CHN_TX_LEN Peripheral DMA transfer length register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	Peripheral DMA transfer length It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

10217128 AP_DMA_I2C1_CHN_RX_LEN Peripheral DMA transfer length register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	Peripheral DMA transfer length It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

10217138 **AP_DMA_I2C1_CHN_INT_BUF** Peripheral DMA internal buffer size register 00000000
SIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	Byte size in internal buffer

10217154 **AP_DMA_I2C1_CHN_TX_ME** Peripheral DMA memory address register 00000000
M_ADDR2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TX_MEM_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

10217158 **AP_DMA_I2C1_CHN_RX_ME** Peripheral DMA memory address register **00000000**
M_ADDR2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RX_MEM_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

10217180 **AP_DMA_I2C2_CHN_INT_FLG** Peripheral DMA interrupt flag register **00000000**
G

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RX_FLAG	TX_FLAG
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RX_FLAG	Raised when RX DMA is finished. Write 0 to clear.
0	TX_FLAG	This flag is raised when TX DMA is finished. Write 0 to clear. - After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. - If STOP = 1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. - If FLUSH = 1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. - If WARM_RST = 1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. - If HARD_RST = 1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

10217184 AP_DMA_I2C2_CHN_INT_EN Peripheral DMA interrupt enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN_RX_FLAG	INTEN_TX_FLAG
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN_RX_FLAG	Enables interrupt for RX_FLAG 0: Disable 1: Enable
0	INTEN_TX_FLAG	Enables interrupt for TX_FLAG 0: Disable 1: Enable

10217188 AP_DMA_I2C2_CHN_EN Peripheral DMA enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	Enables peripheral DMA Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1021718C AP_DMA_I2C2_CHN_RST Peripheral DMA reset register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	Peripheral DMA hard reset (reset regardless of the current transaction) SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	Peripheral DMA warm reset (after the current transaction) SW sets WARM_RST to 1 and waits for EN to become 0. HW automatically sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217190 AP_DMA_I2C2_CHN_STOP Peripheral DMA enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	Pauses peripheral DMA Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	Stops peripheral DMA Set to 1 to stop DMA and wait for EN to become 0. HW then automatically sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

10217194 AP_DMA_I2C2_CHN_FLUSH Peripheral DMA flush register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	Flushes peripheral DMA Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

10217198 AP_DMA_I2C2_CHN_CON Peripheral DMA control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							dir_change	addr_ctrl			align	skip_config	req_blk	async_mode	FIX_EN	DIR
Type							RW	RW			RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	dir_change	If I2C needs direction change, please set 1.
8:6	addr_ctrl	Make this reg as default.
5	align	Make this reg as default. 0: Half word align 1: Word align
4	skip_config	Please config 1 as I2C setting. 0: Config 1: No config
3	req_blk	Make this reg as default. 0: Request block 1: Non-request block
2	async_mode	Please config 1 as I2C setting. 0: Old hand-shake 1: New hand-shake
1	FIX_EN	Peripheral DMA fixed pattern When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as TX. 0: Do not use fixed pattern 1: Use fixed pattern
0	DIR	Half duplex peripheral DMA direction 0: TX 1: RX

1021719C AP_DMA_I2C2_CHN_TX_ME Peripheral DMA memory address register
M_ADDR

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	Peripheral DMA memory address It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. DO NOT set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when users use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when users use SYSRAM as a source memory.

102171A0 AP_DMA_I2C2_CHN_RX_ME Peripheral DMA memory address register
M_ADDR

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	Peripheral DMA memory address It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when users use SYSRAM as a destination, e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when users use SYSRAM as a destination memory.

102171A4 AP_DMA_I2C2_CHN_TX_LEN Peripheral DMA transfer length register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	Peripheral DMA transfer length It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

102171A8 AP_DMA_I2C2_CHN_RX_LEN Peripheral DMA transfer length register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	Peripheral DMA transfer length It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how many data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

102171B8 AP_DMA_I2C2_CHN_INT_BUF Peripheral DMA internal buffer size register 00000000
SIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	Byte size in internal buffer

102171D4 AP_DMA_I2C2_CHN_TX_ME Peripheral DMA memory address register 00000000
M_ADDR2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TX_MEM_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

102171D8 **AP_DMA_I2C2_CHN_RX_ME** Peripheral DMA memory address register **00000000**
M_ADDR2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RX_MEM_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RX_MEM_ADDR2	Peripheral DMA TX memory address bit [32]

10217200 **AP_DMA_UART_0_TX_INT_FL**UART TX virtual FIFO interrupt flag register **00000000**
AG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	Write 0 to clear. Interrupt will be issued to HW when FLAG = 1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN = 1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

10217204 AP_DMA_UART_0_TX_INT_EN UART TX virtual FIFO interrupt enable register 00000000
N

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	Controls interrupt enabling This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Do not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto set inten back to 0 when tx_vff_left_size >= tx_vff_thrs

10217208 AP_DMA_UART_0_TX_EN UART TX virtual FIFO enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	Enables UART TX virtual FIFO Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (a AHB slave port), VFF_W will ignore this command, and the data will not be written to virtual FIFO. 0: Disable 1: Enable

1021720C AP_DMA_UART_0_TX_RST UART TX virtual FIFO reset register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	Peripheral DMA hard reset (regardless of the current transaction) SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	Peripheral DMA warm reset (after the current transaction) SW sets WARM_RST to 1 and waits for EN to become 0. HW automatically sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217210 AP_DMA_UART_0_TX_STOP UART TX virtual FIFO enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	Stops UART TX virtual FIFO Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

10217214 **AP_DMA_UART_0_TX_FLUSH** UART TX virtual FIFO flush register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	Flushes UART TX virtual FIFO Set FLUSH to 1 to allow DMA to flush its internal buffer residual data to EMI. However, even after flush, there may still be residual data because MCU keeps putting data or due to in-coherent problems (Even if MCU issues data to VFF first and then sends flush, DMA can still receive data after flush). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1021721C **AP_DMA_UART_0_TX_VFF_A** UART TX virtual FIFO base address register 00000000
DDR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	UART memory address Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

10217224 **AP_DMA_UART_0_TX_VFF_L** **UART TX virtual FIFO length register**
EN
00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	VFF length Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

10217228 **AP_DMA_UART_0_TX_VFF_T** **UART TX virtual FIFO threshold register**
HRE
00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	VFF threshold in byte alignment In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1021722C **AP_DMA_UART_0_TX_VFF_WPT** UART TX virtual FIFO write pointer register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	TX VFF write pointer wrap bit maintained by software It is initialized to 0. When wrap-around to the ring head occurs, invert this bit.
15:0	TX_VFF_WPT	TX VFF write pointer maintained by software In byte alignment.

10217230 **AP_DMA_UART_0_TX_VFF_RPT** UART TX virtual FIFO read pointer register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	TX VFF read pointer wrap bit maintained by hardware It is initialized to 0. When wrap-around to the ring head occurs, invert this bit.
15:0	TX_VFF_RPT	TX VFF read pointer maintained by hardware In byte alignment.

10217238 **AP_DMA_UART_0_TX_INT_B** UART TX internal buffer size register
UF_SIZE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	Virtual FIFO DMA TX internal buffer size 0: 0 byte 1: 1 byte

1021723C **AP_DMA_UART_0_TX_VFF_V** UART TX virtual FIFO valid size register
ALID_SIZE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	TX virtual FIFO valid size 0: 0 byte 1: 1 byte

10217240 **AP_DMA_UART_0_TX_VFF_L** UART TX virtual FIFO left size register
EFT_SIZE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	TX virtual FIFO left size 0: 0 byte 1: 1 byte

10217254 **AP_DMA_UART_0_TX_VFF_A** UART TX virtual FIFO base address register **00000000**
DDR2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TX_VFF_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TX_VFF_ADDR2	UART memory address bit[32]

10217258 **AP_DMA_UART_0_TX_VFF_WPT_VALID** UART TX virtual FIFO write pointer register by HW control **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	TX VFF write pointer wrap bit If FLUSH= 0, sync with TX_VFF_WPT_WRAP. If flush occurs, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	TX VFF write pointer If FLUSH= 0, sync with TX_VFF_WPT. If flush occurs, it will not update the value until the flush is finished.

1021725C AP_DMA_UART_0_TX_VFF_WPT_VALID2 UART TX virtual FIFO write pointer register by HW control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_WPT_VALID2	TX VFF write pointer If FLUSH= 0, sync with TX_VFF_WPT. If flush occurs, it will not update the value until the flush is finished.

10217260 AP_DMA_UART_0_TX_FLUSH_ACT UART TX virtual FIFO flush status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	There is a flush command when the UART TX channel is flushing.
0	FLUSH_ACT	UART TX channel flush status

10217264 **AP_DMA_UART_0_TX_HW_F** UART TX virtual FIFO HW flush register
LUSH

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	Flush control bit Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update write pointer with SW setting 1: Update write pointer when flush =0

10217268 **AP_DMA_UART_0_TX_VFF_WPT_REAL** UART TX virtual FIFO write pointer register Value
WPT_REAL

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_REAL
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_REAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	TX VFF write pointer wrap bit If HW_FLUSH = 1, sync with TX_VFF_WPT_WRAP_VALID. If HW_FLUSH = 0, sync with TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	TX VFF write pointer If HW_FLUSH = 1, sync with TX_VFF_WPT_VALID. If HW_FLUSH = 0, sync with TX_VFF_WPT.

10217280

AP_DMA_UART_0_RX_INT_FLUART RX virtual FIFO interrupt flag register
AG

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	Write 1 to clear. This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.
0	FLAG0	Write 1 to clear. This flag is raised when rx_vff_valid_size >= rx_vff_thre. (VFF is almost full and MCU needs to consume those data.)

10217284 AP_DMA_UART_0_RX_INT_E UART RX virtual FIFO interrupt enable register 00000000
N

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	Controls interrupt enabling Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	Controls interrupt enabling Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

10217288 AP_DMA_UART_0_RX_EN UART RX virtual FIFO enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	Enables UART1 RX virtual FIFO Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1021728C AP_DMA_UART_0_RX_RST UART RX virtual FIFO reset register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	Peripheral DMA hard reset (regardless of the current transaction) SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	Peripheral DMA warm reset (after the current transaction) SW sets WARM_RST to 1 and waits for EN to become 0. HW automatically sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217290 AP_DMA_UART_0_RX_STOP UART RX virtual FIFO enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	Stops UART RX virtual FIFO Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

10217294 **AP_DMA_UART_0_RX_FLUSH** UART RX virtual FIFO flush register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	Flushes UART RX virtual FIFO Set FLUSH to 1 to allow DMA to flush its internal buffer residual data to EMI. However, even after flush, there may still be residual data because MCU keeps putting data or due to in-coherent problems (Even if MCU issues data to VFF first and then sends flush, DMA can still receive data after flush). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1021729C **AP_DMA_UART_0_RX_VFF_A** UART RX virtual FIFO base address register 00000000**DDR**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	UART memory address Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

102172A4 **AP_DMA_UART_0_RX_VFF_L** UART RX virtual FIFO length register
EN

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	VFF length Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

102172A8 **AP_DMA_UART_0_RX_VFF_T** UART RX virtual FIFO threshold register
HRE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	VFF threshold in byte alignment In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

102172AC AP_DMA_UART_0_RX_VFF_WPT UART RX virtual FIFO write pointer register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	RX VFF write pointer wrap bit maintained by hardware It is initialized to 0. When wrap-around to the ring head occurs, invert this bit.
15:0	RX_VFF_WPT	RX VFF write pointer maintained by hardware In byte alignment.

102172B0 AP_DMA_UART_0_RX_VFF_RPT UART RX virtual FIFO read pointer register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	RX VFF read pointer wrap bit maintained by software It is initialized to 0. When wrap-around to the ring head occurs, invert this bit.
15:0	RX_VFF_RPT	RX VFF read pointer maintained by software In byte alignment.

102172B4 **AP_DMA_UART_0_RX_FLOW_CTRL_THRE** UART RX virtual FIFO flow control threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	VFF flow control threshold in byte alignment In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

102172B8 **AP_DMA_UART_0_RX_INT_BUF_SIZE** UART RX internal buffer size register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	Virtual FIFO DMA RX internal buffer size 0: 0 byte 1: 1 byte

102172BC **AP_DMA_UART_0_RX_VFF_V** UART RX virtual FIFO valid size register
ALID_SIZE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	RX virtual FIFO valid size 0: 0 byte 1: 1 byte

102172C0 **AP_DMA_UART_0_RX_VFF_L** UART RX virtual FIFO left size register
EFT_SIZE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	RX virtual FIFO left size 0: 0 byte 1: 1 byte

102172D4 **AP_DMA_UART_0_RX_VFF_A** UART RX virtual FIFO base address register **00000000**
DDR2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RX_VFF_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RX_VFF_ADDR2	UART memory address bit[32]

10217300 **AP_DMA_UART_1_TX_INT_FL** UART TX virtual FIFO interrupt flag register **00000000**
AG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	Write 0 to clear. Interrupt will be issued to HW when FLAG = 1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN = 1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

10217304 AP_DMA_UART_1_TX_INT_EN UART TX virtual FIFO interrupt enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	Controls interrupt enabling This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Do not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto set inten back to 0 when tx_vff_left_size >= tx_vff_thrs

10217308 AP_DMA_UART_1_TX_EN UART TX virtual FIFO enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	Enables UART TX virtual FIFO Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1021730C AP_DMA_UART_1_TX_RST UART TX virtual FIFO reset register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	Peripheral DMA hard reset (regardless of the current transaction) SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	Peripheral DMA warm reset (after the current transaction) SW sets WARM_RST to 1 and waits for EN to become 0. HW automatically sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217310 AP_DMA_UART_1_TX_STOP UART TX virtual FIFO enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	Stops UART TX virtual FIFO Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

10217314 **AP_DMA_UART_1_TX_FLUSH** UART TX virtual FIFO flush register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	Flushes UART TX virtual FIFO Set FLUSH to 1 to allow DMA to flush its internal buffer residual data to EMI. However, even after flush, there may still be residual data because MCU keeps putting data or due to in-coherent problems (Even if MCU issues data to VFF first and then sends flush, DMA can still receive data after flush). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1021731C **AP_DMA_UART_1_TX_VFF_A** UART TX virtual FIFO base address register 00000000
DDR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	UART memory address Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

10217324 **AP_DMA_UART_1_TX_VFF_L** **UART TX virtual FIFO length register**
EN

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	VFF length Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

10217328 **AP_DMA_UART_1_TX_VFF_T** **UART TX virtual FIFO threshold register**
HRE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	VFF threshold in byte alignment In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1021732C **AP_DMA_UART_1_TX_VFF_WPT** UART TX virtual FIFO write pointer register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	TX VFF write pointer wrap bit maintained by software It is initialized to 0. When wrap-around to the ring head occurs, invert this bit.
15:0	TX_VFF_WPT	TX VFF write pointer maintained by software In byte alignment.

10217330 **AP_DMA_UART_1_TX_VFF_RPT** UART TX virtual FIFO read pointer register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	TX VFF read pointer wrap bit maintained by hardware It is initialized to 0. When wrap-around to the ring head occurs, invert this bit.
15:0	TX_VFF_RPT	TX VFF read pointer maintained by hardware In byte alignment.

10217338 **AP_DMA_UART_1_TX_INT_B** UART TX internal buffer size register
UF_SIZE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	Virtual FIFO DMA TX internal buffer size 0: 0 byte 1: 1 byte

1021733C **AP_DMA_UART_1_TX_VFF_V** UART TX virtual FIFO valid size register
ALID_SIZE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	TX virtual FIFO valid size 0: 0 byte 1: 1 byte

10217340 **AP_DMA_UART_1_TX_VFF_L** **UART TX virtual FIFO left size register**
EFT_SIZE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	TX virtual FIFO left size 0: 0 byte 1: 1 byte

10217354 **AP_DMA_UART_1_TX_VFF_A** **UART TX virtual FIFO base address register**
DDR2

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TX_VFF_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TX_VFF_ADDR2	UART memory address bit[32]

10217358 AP_DMA_UART_1_TX_VFF_WPT_VALID UART TX virtual FIFO write pointer register by HW control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	TX VFF write pointer wrap bit If FLUSH= 0, sync with TX_VFF_WPT_WRAP. If flush occurs, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	TX VFF write pointer If FLUSH= 0, sync with TX_VFF_WPT. If flush occurs, it will not update the value until the flush is finished.

1021735C AP_DMA_UART_1_TX_VFF_WPT_VALID2 UART TX virtual FIFO write pointer register by HW control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_WPT_VALID2	TX VFF write pointer If FLUSH= 0, sync with TX_VFF_WPT. If flush occurs, it will not update the value until the flush is finished.

10217360 **AP_DMA_UART_1_TX_FLUSH_UART_TX_virtual_FIFO_flush_status_register**
ACT

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	There is a flush command when the UART TX channel is flushing.
0	FLUSH_ACT	UART TX channel flush status

10217364 **AP_DMA_UART_1_TX_HW_FLUSH_UART_TX_virtual_FIFO_HW_flush_register**
LUSH

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	Flush control bit Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update write pointer with SW setting 1: Update write pointer when flush =0

10217368 AP_DMA_UART_1_TX_VFF_WPT_REAL UART TX virtual FIFO write pointer register Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_REAL
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_REAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	TX VFF write pointer wrap bit If HW_FLUSH = 1, sync with TX_VFF_WPT_WRAP_VALID. If HW_FLUSH = 0, sync with TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	TX VFF write pointer If HW_FLUSH = 1, sync with TX_VFF_WPT_VALID. If HW_FLUSH = 0, sync with TX_VFF_WPT.

10217380 AP_DMA_UART_1_RX_INT_FLAG UART RX virtual FIFO interrupt flag register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	Write 1 to clear. This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.
0	FLAG0	Write 1 to clear. This flag is raised when rx_vff_valid_size >= rx_vff_thre. (VFF is almost full and MCU needs to consume those data.)

10217384 AP_DMA_UART_1_RX_INT_E UART RX virtual FIFO interrupt enable register 00000000
N

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	Controls interrupt enabling Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	Controls interrupt enabling Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

10217388 AP_DMA_UART_1_RX_EN UART RX virtual FIFO enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	Enables UART1 RX virtual FIFO Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1021738C AP_DMA_UART_1_RX_RST UART RX virtual FIFO reset register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	Peripheral DMA hard reset (regardless of the current transaction) SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	Peripheral DMA warm reset (after the current transaction) SW sets WARM_RST to 1 and waits for EN to become 0. HW automatically sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217390 AP_DMA_UART_1_RX_STOP UART RX virtual FIFO enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	Stops UART RX virtual FIFO Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

10217394 AP_DMA_UART_1_RX_FLUSH UART RX virtual FIFO flush register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	Flushes UART RX virtual FIFO Set FLUSH to 1 to allow DMA to flush its internal buffer residual data to EMI. However, even after flush, there may still be residual data because MCU keeps putting data or due to in-coherent problems (Even if MCU issues data to VFF first and then sends flush, DMA can still receive data after flush). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1021739C **AP_DMA_UART_1_RX_VFF_A** UART RX virtual FIFO base address register
DDR

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	UART memory address Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

102173A4 **AP_DMA_UART_1_RX_VFF_L** UART RX virtual FIFO length register
EN

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	VFF length Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

102173A8 **AP_DMA_UART_1_RX_VFF_T** **UART RX virtual FIFO threshold register**
HRE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	VFF threshold in byte alignment In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

102173AC **AP_DMA_UART_1_RX_VFF** **UART RX virtual FIFO write pointer register**
WPT

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	RX VFF write pointer wrap bit maintained by hardware It is initialized to 0. When wrap-around to the ring head occurs, invert this bit.
15:0	RX_VFF_WPT	RX VFF write pointer maintained by hardware In byte alignment.

102173B0 AP_DMA_UART_1_RX_VFF_R UART RX virtual FIFO read pointer register

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	RX VFF read pointer wrap bit maintained by software It is initialized to 0. When wrap-around to the ring head occurs, invert this bit.
15:0	RX_VFF_RPT	RX VFF read pointer maintained by software In byte alignment.

102173B4 AP_DMA_UART_1_RX_FLOW_CTRL_THRE UART RX virtual FIFO flow control threshold

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	VFF flow control threshold in byte alignment In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

102173B8 AP_DMA_UART_1_RX_INT_B UART RX internal buffer size register

00000000

UF_SIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	Virtual FIFO DMA RX internal buffer size
		0: 0 byte
		1: 1 byte

102173BC AP_DMA_UART_1_RX_VFF_V UART RX virtual FIFO valid size register

00000000

ALID_SIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	RX virtual FIFO valid size
		0: 0 byte
		1: 1 byte

102173C0 **AP_DMA_UART_1_RX_VFF_L** UART RX virtual FIFO left size register
EFT_SIZE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	RX virtual FIFO left size 0: 0 byte 1: 1 byte

102173D4 **AP_DMA_UART_1_RX_VFF_A** UART RX virtual FIFO base address register
DDR2

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RX_VFF_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RX_VFF_ADDR2	UART memory address bit[32]

10217400 AP_DMA_UART_2_TX_INT_FLUART TX virtual FIFO interrupt flag register
AG

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	Write 0 to clear. Interrupt will be issued to HW when FLAG = 1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN = 1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

10217404 AP_DMA_UART_2_TX_INT_EN UART TX virtual FIFO interrupt enable register 00000000
N

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	Controls interrupt enabling This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Do not set flag to 1, even tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto set inten back to 0 when tx_vff_left_size >= tx_vff_thrs

10217408 AP_DMA_UART_2_TX_EN UART TX virtual FIFO enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	Enables UART TX virtual FIFO Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1021740C AP_DMA_UART_2_TX_RST UART TX virtual FIFO reset register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	Peripheral DMA hard reset (regardless of the current transaction) SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	Peripheral DMA warm reset (after the current transaction) SW sets WARM_RST to 1 and waits for EN to become 0. HW automatically sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217410 AP_DMA_UART_2_TX_STOP UART TX virtual FIFO enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	Stops UART TX virtual FIFO Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

10217414 AP_DMA_UART_2_TX_FLUSH UART TX virtual FIFO flush register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	Flushes UART TX virtual FIFO Set FLUSH to 1 to allow DMA to flush its internal buffer residual data to EMI. However, even after flush, there may still be residual data because MCU keeps putting data or due to in-coherent problems (Even if MCU issues data to VFF first and then sends flush, DMA can still receive data after flush). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1021741C AP_DMA_UART_2_TX_VFF_A UART TX virtual FIFO base address register 00000000
DDR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	UART memory address Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

10217424 **AP_DMA_UART_2_TX_VFF_L** **UART TX virtual FIFO length register**
EN

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	VFF length Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

10217428 **AP_DMA_UART_2_TX_VFF_T** **UART TX virtual FIFO threshold register**
HRE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	VFF threshold in byte alignment In TX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1021742C AP_DMA_UART_2_TX_VFF_WPT UART TX virtual FIFO write pointer register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	TX VFF write pointer wrap bit maintained by software It is initialized to 0. When wrap-around to the ring head occurs, invert this bit.
15:0	TX_VFF_WPT	TX VFF write pointer maintained by software In byte alignment.

10217430 AP_DMA_UART_2_TX_VFF_RPT UART TX virtual FIFO read pointer register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	TX VFF read pointer wrap bit maintained by hardware It is initialized to 0. When wrap-around to the ring head occurs, invert this bit.
15:0	TX_VFF_RPT	TX VFF read pointer maintained by hardware In byte alignment.

10217438 **AP_DMA_UART_2_TX_INT_B** UART TX internal buffer size register
UF_SIZE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	Virtual FIFO DMA TX internal buffer size 0: 0 byte 1: 1 byte

1021743C **AP_DMA_UART_2_TX_VFF_V** UART TX virtual FIFO valid size register
ALID_SIZE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	TX virtual FIFO valid size 0: 0 byte 1: 1 byte

10217440 **AP_DMA_UART_2_TX_VFF_L** UART TX virtual FIFO left size register
EFT_SIZE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	TX virtual FIFO left size 0: 0 byte 1: 1 byte

10217454 **AP_DMA_UART_2_TX_VFF_A** UART TX virtual FIFO base address register **00000000**
DDR2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TX_VFF_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TX_VFF_ADDR2	UART memory address bit[32]

10217458 **AP_DMA_UART_2_TX_VFF_WPT_VALID** UART TX virtual FIFO write pointer register by HW control **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	TX VFF write pointer wrap bit If FLUSH= 0, sync with TX_VFF_WPT_WRAP. If flush occurs, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	TX VFF write pointer If FLUSH= 0, sync with TX_VFF_WPT. If flush occurs, it will not update the value until the flush is finished.

1021745C AP_DMA_UART_2_TX_VFF_WPT_VALID2 UART TX virtual FIFO write pointer register by HW control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_WPT_VALID2	TX VFF write pointer If FLUSH= 0, sync with TX_VFF_WPT. If flush occurs, it will not update the value until the flush is finished.

10217460 AP_DMA_UART_2_TX_FLUSH_ACT UART TX virtual FIFO flush status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	There is a flush command when the UART TX channel is flushing.
0	FLUSH_ACT	UART TX channel flush status

10217464 **AP_DMA_UART_2_TX_HW_F** UART TX virtual FIFO HW flush register
LUSH

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	Flush control bit Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update write pointer with SW setting 1: Update write pointer when flush =0

10217468 **AP_DMA_UART_2_TX_VFF_WPT_REAL** UART TX virtual FIFO write pointer register Value
WPT_REAL

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_REAL
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_REAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	TX VFF write pointer wrap bit If HW_FLUSH = 1, sync with TX_VFF_WPT_WRAP_VALID. If HW_FLUSH = 0, sync with TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	TX VFF write pointer If HW_FLUSH = 1, sync with TX_VFF_WPT_VALID. If HW_FLUSH = 0, sync with TX_VFF_WPT.

10217480

AP_DMA_UART_2_RX_INT_FLUART RX virtual FIFO interrupt flag register
AG

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	Write 1 to clear. This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.
0	FLAG0	Write 1 to clear. This flag is raised when rx_vff_valid_size >= rx_vff_thre. (VFF is almost full and MCU needs to consume those data.)

10217484 **AP_DMA_UART_2_RX_INT_E** UART RX virtual FIFO interrupt enable register 00000000
N

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	Controls interrupt enabling Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	Controls interrupt enabling Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

10217488 AP_DMA_UART_2_RX_EN UART RX virtual FIFO enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	Enables UART1 RX virtual FIFO Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1021748C AP_DMA_UART_2_RX_RST UART RX virtual FIFO reset register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	Peripheral DMA hard reset (regardless of the current transaction) SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	Peripheral DMA warm reset (after the current transaction) SW sets WARM_RST to 1 and waits for EN to become 0. HW automatically sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217490 AP_DMA_UART_2_RX_STOP UART RX virtual FIFO enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	Stops UART RX virtual FIFO Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

10217494 AP_DMA_UART_2_RX_FLUSH UART RX virtual FIFO flush register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	Flushes UART RX virtual FIFO Set FLUSH to 1 to allow DMA to flush its internal buffer residual data to EMI. However, even after flush, there may still be residual data because MCU keeps putting data or due to in-coherent problems (Even if MCU issues data to VFF first and then sends flush, DMA can still receive data after flush). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1021749C AP_DMA_UART_2_RX_VFF_A UART RX virtual FIFO base address register 00000000
DDR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	UART memory address Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

102174A4 **AP_DMA_UART_2_RX_VFF_L** UART RX virtual FIFO length register
EN

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	VFF length Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

102174A8 **AP_DMA_UART_2_RX_VFF_T** UART RX virtual FIFO threshold register
HRE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	VFF threshold in byte alignment In RX mode, DMA issues interrupt when data in VFF are smaller than the threshold. In TX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

102174AC AP_DMA_UART_2_RX_VFF_WPT UART RX virtual FIFO write pointer register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	RX VFF write pointer wrap bit maintained by hardware It is initialized to 0. When wrap-around to the ring head occurs, invert this bit.
15:0	RX_VFF_WPT	RX VFF write pointer maintained by hardware In byte alignment.

102174B0 AP_DMA_UART_2_RX_VFF_RPT UART RX virtual FIFO read pointer register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	RX VFF read pointer wrap bit maintained by software It is initialized to 0. When wrap-around to the ring head occurs, invert this bit.
15:0	RX_VFF_RPT	RX VFF read pointer maintained by software In byte alignment.

102174B4 **AP_DMA_UART_2_RX_FLOW_CTRL_THRE** UART RX virtual FIFO flow control threshold **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	VFF flow control threshold in byte alignment In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

102174B8 **AP_DMA_UART_2_RX_INT_BUF_SIZE** UART RX internal buffer size register **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	Virtual FIFO DMA RX internal buffer size 0: 0 byte 1: 1 byte

102174BC **AP_DMA_UART_2_RX_VFF_V** UART RX virtual FIFO valid size register
ALID_SIZE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	RX virtual FIFO valid size 0: 0 byte 1: 1 byte

102174C0 **AP_DMA_UART_2_RX_VFF_L** UART RX virtual FIFO left size register
EFT_SIZE

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	RX virtual FIFO left size 0: 0 byte 1: 1 byte

102174D4

AP_DMA_UART_2_RX_VFF_A UART RX virtual FIFO base address register

00000000

DDR2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RX_VFF_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RX_VFF_ADDR2	UART memory address bit[32]

2 Clock and Power Control

2.1 Top Clock Generator

2.1.1 Register Definition

Module name: TOPCKGEN Base address: (+0x1001B000)

Address	Name	Width	Register Function
1001B000	<u>CLK_CFG_0</u>	32	Function clock selection register 0
1001B004	<u>CLK_CFG_0_SET</u>	32	SET control of clock configuration 0
1001B008	<u>CLK_CFG_0_CLR</u>	32	CLR control of clock configuration 0
1001B010	<u>CLK_CFG_1</u>	32	Function clock selection register 1
1001B014	<u>CLK_CFG_1_SET</u>	32	SET control of clock configuration 1
1001B018	<u>CLK_CFG_1_CLR</u>	32	CLR control of clock configuration 1
1001B020	<u>CLK_CFG_2</u>	32	Function clock selection register 2
1001B024	<u>CLK_CFG_2_SET</u>	32	SET control of clock configuration 2
1001B028	<u>CLK_CFG_2_CLR</u>	32	CLR control of clock configuration 2
1001B030	<u>CLK_CFG_3</u>	32	Function clock selection register 3
1001B034	<u>CLK_CFG_3_SET</u>	32	SET control of clock configuration 3
1001B038	<u>CLK_CFG_3_CLR</u>	32	CLR control of clock configuration 3
1001B040	<u>CLK_CFG_4</u>	32	Function clock selection register 4
1001B044	<u>CLK_CFG_4_SET</u>	32	SET control of clock configuration 4
1001B048	<u>CLK_CFG_4_CLR</u>	32	CLR control of clock configuration 4
1001B050	<u>CLK_CFG_5</u>	32	Function clock selection register 5
1001B054	<u>CLK_CFG_5_SET</u>	32	SET control of clock configuration 5
1001B058	<u>CLK_CFG_5_CLR</u>	32	CLR control of clock configuration 5
1001B060	<u>CLK_CFG_6</u>	32	Function clock selection register 6
1001B064	<u>CLK_CFG_6_SET</u>	32	SET control of clock configuration 6
1001B068	<u>CLK_CFG_6_CLR</u>	32	CLR control of clock configuration 6
1001B070	<u>CLK_CFG_7</u>	32	Function clock selection register 7
1001B074	<u>CLK_CFG_7_SET</u>	32	SET control of clock configuration 7
1001B078	<u>CLK_CFG_7_CLR</u>	32	CLR control of clock configuration 7
1001B080	<u>CLK_CFG_8</u>	32	Function clock selection register 8
1001B084	<u>CLK_CFG_8_SET</u>	32	SET control of clock configuration 8
1001B088	<u>CLK_CFG_8_CLR</u>	32	CLR control of clock configuration 8
1001B090	<u>CLK_CFG_9</u>	32	Function clock selection register 9
1001B094	<u>CLK_CFG_9_SET</u>	32	SET control of clock configuration 9
1001B098	<u>CLK_CFG_9_CLR</u>	32	CLR control of clock configuration 9
1001B0A0	<u>CLK_CFG_10</u>	32	Function clock selection register 10
1001B0A4	<u>CLK_CFG_10_SET</u>	32	SET control of clock configuration 10
1001B0A8	<u>CLK_CFG_10_CLR</u>	32	CLR control of clock configuration 10
1001B0B0	<u>CLK_CFG_11</u>	32	Function clock selection register 11
1001B0B4	<u>CLK_CFG_11_SET</u>	32	SET control of clock configuration 11
1001B0B8	<u>CLK_CFG_11_CLR</u>	32	CLR control of clock configuration 11
1001B0C0	<u>CLK_CFG_12</u>	32	Function clock selection register 12
1001B0C4	<u>CLK_CFG_12_SET</u>	32	SET control of clock configuration 12
1001B0C8	<u>CLK_CFG_12_CLR</u>	32	CLR control of clock configuration 12
1001B0D0	<u>CLK_CFG_13</u>	32	Function clock selection register 13

Address	Name	Width	Register Function
1001B0D4	<u>CLK_CFG_13_SET</u>	32	SET control of clock configuration 13
1001B0D8	<u>CLK_CFG_13_CLR</u>	32	CLR control of clock configuration 13
1001B0E0	<u>CLK_CFG_14</u>	32	Function clock selection register 14
1001B0E4	<u>CLK_CFG_14_SET</u>	32	SET control of clock configuration 14
1001B0E8	<u>CLK_CFG_14_CLR</u>	32	CLR control of clock configuration 14
1001B0F0	<u>CLK_CFG_15</u>	32	Function clock selection register 15
1001B0F4	<u>CLK_CFG_15_SET</u>	32	SET control of clock configuration 15
1001B0F8	<u>CLK_CFG_15_CLR</u>	32	CLR control of clock configuration 15
1001B100	<u>CLK_CFG_16</u>	32	Function clock selection register 16
1001B104	<u>CLK_CFG_16_SET</u>	32	SET control of clock configuration 16
1001B108	<u>CLK_CFG_16_CLR</u>	32	CLR control of clock configuration 16
1001B110	<u>CLK_CFG_17</u>	32	Function clock selection register 17
1001B114	<u>CLK_CFG_17_SET</u>	32	SET control of clock configuration 17
1001B118	<u>CLK_CFG_17_CLR</u>	32	CLR control of clock configuration 17
1001B120	<u>CLK_CFG_18</u>	32	Function clock selection register 18
1001B124	<u>CLK_CFG_18_SET</u>	32	SET control of clock configuration 18
1001B128	<u>CLK_CFG_18_CLR</u>	32	CLR control of clock configuration 18
1001B140	<u>CLK_CFG_20</u>	32	Function clock selection register 20
1001B144	<u>CLK_CFG_20_SET</u>	32	SET control of clock configuration 20
1001B148	<u>CLK_CFG_20_CLR</u>	32	CLR control of clock configuration 20
1001B1C0	<u>CLK_CFG_UPDATE0</u>	32	Clock configuration update register 0
1001B1C4	<u>CLK_CFG_UPDATE1</u>	32	Clock configuration update register 1
1001B1C8	<u>CLK_CFG_UPDATE2</u>	32	Clock configuration update register 2
1001B330	<u>CKSTA_REG0</u>	32	Function clock selection status register 0
1001B334	<u>CKSTA_REG1</u>	32	Function clock selection status register 1
1001B200	<u>CLK_MISC_CFG_0</u>	32	Miscellaneous control
1001B210	<u>CLK_MISC_CFG_1</u>	32	Miscellaneous control
1001B320	<u>CLK26CALI_0</u>	32	Frequency meter control register 0
1001B324	<u>CLK26CALI_1</u>	32	Frequency meter control register 1
1001B360	<u>DCM_CFG</u>	32	DCM configuration
1001B400	<u>CLKMON_CLK_SEL_REG</u>	32	Clock monitor selection register
1001B404	<u>CLKMON_K1_REG</u>	32	Clock monitor divider register
1001B420	<u>CLK_AUDDIV_0</u>	32	Audio clock selection register

1001B000 CLK_CFG_0 Function clock selection register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_netsys_gsw			clk_netsys_gsw_inv			clk_netsys_gsw_sel		pdn_netsys_2x			clk_netsys_2x_inv			clk_netsys_2x_sel	
Type	RW			RW			RW		RW			RW			RW	
Reset	0			0			0	0	0			0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_netsys_500m			clk_netsys_500m_inv			clk_netsys_500m_sel		pdn_netsys			clk_netsys_inv			clk_netsys_sel	
Type	RW			RW			RW		RW			RW			RW	
Reset	0			0			0	0	0			0			0	0

Bit(s)	Name	Description
31	pdn_netsys_gsw	Turns off netsys_gsw_ck 1: Enable clock off
28	clk_netsys_gsw_inv	netsys_gsw_ck clock phase invert 1: Enable phase invert
25:24	clk_netsys_gsw_sel	netsys_gsw_ck clock mux select 0: cb_cksq_40m 1: cb_net1pll_d4 2: cb_net1pll_d5
23	pdn_netsys_2x	Turns off netsys_2x_ck 1: Enable clock off
20	clk_netsys_2x_inv	netsys_2x_ck clock phase invert 1: Enable phase invert
17:16	clk_netsys_2x_sel	netsys_2x_ck clock mux select 0: cb_cksq_40m 1: cb_net2pll_800m 2: cb_mmppll_720m
15	pdn_netsys_500m	Turns off netsys_500m_ck 1: Enable clock off
12	clk_netsys_500m_inv	netsys_500m_ck clock phase invert 1: Enable phase invert
9:8	clk_netsys_500m_sel	netsys_500m_ck clock mux select 0: cb_cksq_40m 1: cb_net1pll_d5

Bit(s)	Name	Description
		2: net1pll_d5_d2
7	pdn_netsys	Turns off netsys_ck 1: Enable clock off
4	clk_netsys_inv	netsys_ck clock phase invert 1: Enable phase invert
1:0	clk_netsys_sel	netsys_ck clock mux select 0: cb_cksq_40m 1: cb_net2pll_d2 2: cb_mmppll_d2

1001B004 CLK_CFG_0_SET SET control of clock configuration 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_0_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_0_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_0_set	Sets the corresponding bit of CLG_CFG_SEL_0 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B008 CLK_CFG_0_CLR CLR control of clock configuration 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_0_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_0_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_0_clr	Clears the corresponding bit of CLG_CFG_SEL_0 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B010 CLK_CFG_1 Function clock selection register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_eip197			clk_eip197_inv		clk_eip197_sel			pdn_netsys_pao_2x			clk_netsys_pao_2x_inv		clk_netsys_pao_2x_sel		
Type	RW			RW		RW			RW			RW		RW		
Reset	0			0		0	0	0	0			0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_netsys_wed_mcu			clk_netsys_wed_mcu_inv		clk_netsys_wed_mcu_sel			pdn_eth_gmii			clk_eth_gmii_inv				clk_eth_gmii_sel
Type	RW			RW		RW			RW			RW				RW
Reset	0			0		0	0	0	0			0				0

Bit(s)	Name	Description
31	pdn_eip197	Turns off eip197_ck 1: Enable clock off
28	clk_eip197_inv	eip197_ck clock phase invert 1: Enable phase invert
26:24	clk_eip197_sel	eip197_ck clock mux select 0: cb_cksq_40m 1: cb_netsyspll_850m 2: cb_net2pll_800m 3: cb_mmppll_720m 4: cb_net1pll_d4 5: cb_net1pll_d5
23	pdn_netsys_pao_2x	Turns off netsys_pao_2x_ck 1: Enable clock off
20	clk_netsys_pao_2x_inv	netsys_pao_2x_ck clock phase invert 1: Enable phase invert
18:16	clk_netsys_pao_2x_sel	netsys_pao_2x_ck clock mux select 0: cb_cksq_40m 1: cb_net2pll_800m 2: cb_mmppll_720m 3: cb_net1pll_d4 4: cb_net1pll_d5 5: cb_mpll_416m

Bit(s)	Name	Description
15	pdn_netsys_wed_mcu	Turns off netsys_wed_mcu_ck 1: Enable clock off
12	clk_netsys_wed_mcu_inv	netsys_wed_mcu_ck clock phase invert 1: Enable phase invert
10:8	clk_netsys_wed_mcu_sel	netsys_wed_mcu_ck clock mux select 0: cb_cksq_40m 1: cb_net2pll_800m 2: cb_mmppll_720m 3: cb_net1pll_d4 4: cb_net1pll_d5 5: cb_mpll_416m
7	pdn_eth_gmii	Turns off eth_gmii_ck 1: Enable clock off
4	clk_eth_gmii_inv	eth_gmii_ck clock phase invert 1: Enable phase invert
0	clk_eth_gmii_sel	eth_gmii_ck clock mux select 0: cb_cksq_40m 1: net1pll_d5_d4

1001B014 CLK_CFG_1_SET SET control of clock configuration 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_1_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_1_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_1_set	Sets the corresponding bit of CLG_CFG_SEL_1 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B018 CLK_CFG_1_CLR CLR control of clock configuration 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_1_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_1_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_1_clr	Clears the corresponding bit of CLG_CFG_SEL_1 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B020 CLK_CFG_2 Function clock selection register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_emmc_400m			clk_emmc_400m_inv		clk_emmc_400m_sel			pdn_emmc_250m			clk_emmc_250m_inv			clk_emmc_250m_sel	
Type	RW			RW		RW			RW			RW			RW	
Reset	0			0		0	0	0	0			0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_uart_bclk			clk_uart_bclk_inv			clk_uart_bclk_sel		pdn_axi_infra			clk_axi_infra_inv				clk_axi_infra_sel
Type	RW			RW			RW		RW			RW				RW
Reset	0			0			0	0	0			0				0

Bit(s)	Name	Description
31	pdn_emmc_400m	Turns off emmc_400m_ck 1: Enable clock off
28	clk_emmc_400m_inv	emmc_400m_ck clock phase invert 1: Enable phase invert
26:24	clk_emmc_400m_sel	emmc_400m_ck clock mux select 0: cb_cksq_40m 1: cb_msdcpll_400m 2: cb_mmppll_d2 3: cb_mpll_d2 4: cb_mmppll_d4 5: net1pll_d8_d2
23	pdn_emmc_250m	Turns off emmc_250m_ck 1: Enable clock off
20	clk_emmc_250m_inv	emmc_250m_ck clock phase invert 1: Enable phase invert
17:16	clk_emmc_250m_sel	emmc_250m_ck clock mux select 0: cb_cksq_40m 1: net1pll_d5_d2 2: cb_mmppll_d4
15	pdn_uart_bclk	Turns off uart_bclk_ck 1: Enable clock off
12	clk_uart_bclk_inv	uart_bclk_ck clock phase invert 1: Enable phase invert

Bit(s)	Name	Description
9:8	clk_uart_bclk_sel	uart_bclk_ck clock mux select 0: cb_cksq_40m 1: cb_mpll_d8 2: mpll_d8_d2
7	pdn_axi_infra	Turns off axi_infra_ck 1: Enable clock off
4	clk_axi_infra_inv	axi_infra_ck clock phase invert 1: Enable phase invert
0	clk_axi_infra_sel	axi_infra_ck clock mux select 0: cb_cksq_40m 1: net1pll_d8_d2

1001B024 CLK_CFG_2_SET SET control of clock configuration 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_2_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_2_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_2_set	Sets the corresponding bit of CLG_CFG_SEL_2 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B028 CLK_CFG_2_CLR CLR control of clock configuration 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_2_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_2_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_2_clr	Clears the corresponding bit of CLG_CFG_SEL_2 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B030 CLK_CFG_3 Function clock selection register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_spinfi_bclk			clk_spinfi_bclk_inv		clk_spinfi_bclk_sel			pdn_nfi1x			clk_nfi1x_inv		clk_nfi1x_sel		
Type	RW			RW		RW			RW			RW		RW		
Reset	0			0		0	0	0	0			0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_spinm_mst			clk_spinm_mst_inv		clk_spinm_mst_sel			pdn_spi			clk_spi_inv		clk_spi_sel		
Type	RW			RW		RW			RW			RW		RW		
Reset	0			0		0	0	0	0			0		0	0	0

Bit(s)	Name	Description
31	pdn_spinfi_bclk	Turns off spinfi_bclk_ck 1: Enable clock off
28	clk_spinfi_bclk_inv	spinfi_bclk_ck clock phase invert 1: Enable phase invert
26:24	clk_spinfi_bclk_sel	spinfi_bclk_ck clock mux select 0: cksq_40m_d2 1: cb_cksq_40m 2: net1pll_d5_d4 3: cb_mpll_d4 4: cb_mmppll_d8 5: net1pll_d8_d4 6: mmppll_d6_d2 7: cb_mpll_d8
23	pdn_nfi1x	Turns off nfi1x_ck 1: Enable clock off
20	clk_nfi1x_inv	nfi1x_ck clock phase invert 1: Enable phase invert
18:16	clk_nfi1x_sel	nfi1x_ck clock mux select 0: cb_cksq_40m 1: cb_mmppll_d4 2: net1pll_d8_d2 3: cb_net2pll_d6 4: cb_mpll_d4

Bit(s)	Name	Description
		5: cb_mmppll_d8
		6: net1pll_d8_d4
		7: cb_mpll_d8
15	pdn_spim_mst	Turns off spim_mst_ck 1: Enable clock off
12	clk_spim_mst_inv	spim_mst_ck clock phase invert 1: Enable phase invert
10:8	clk_spim_mst_sel	spim_mst_ck clock mux select 0: cb_cksq_40m 1: cb_mpll_d2 2: cb_mmppll_d4 3: net1pll_d8_d2 4: cb_net2pll_d6 5: net1pll_d5_d4 6: cb_mpll_d4 7: net1pll_d8_d4
7	pdn_spi	Turns off spi_ck 1: Enable clock off
4	clk_spi_inv	spi_ck clock phase invert 1: Enable phase invert
2:0	clk_spi_sel	spi_ck clock mux select 0: cb_cksq_40m 1: cb_mpll_d2 2: cb_mmppll_d4 3: net1pll_d8_d2 4: cb_net2pll_d6 5: net1pll_d5_d4 6: cb_mpll_d4 7: net1pll_d8_d4

1001B034

CLK_CFG_3_SET

SET control of clock configuration 3

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_3_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_3_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_3_set	Sets the corresponding bit of CLG_CFG_SEL_3 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B038 CLK_CFG_3_CLR CLR control of clock configuration 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_3_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_3_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_3_clr	Clears the corresponding bit of CLG_CFG_SEL_3 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B040 CLK_CFG_4 Function clock selection register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_p extp_tl _clk			clk_pex tp_tl_cl k_inv		clk_pextp_tl_clk_sel			pdn_pc ie_mbi st_250 m			clk_pci e_mbis t_250m _inv				clk_pci e_mbis t_250 m_sel
Type	RW			RW		RW			RW			RW				RW
Reset	0			0		0	0	0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_i2 c_bclk			clk_i2c _bclk_i nv			clk_i2c_bclk_sel		pdn_p wm_bc lk			clk_pw m_bclk _inv		clk_pwm_bclk_sel		
Type	RW			RW			RW		RW			RW		RW		
Reset	0			0			0	0	0			0		0	0	0

Bit(s)	Name	Description
31	pdn_pextp_tl_clk	Turns off pextp_tl_clk_ck 1: Enable clock off
28	clk_pextp_tl_clk_inv	pextp_tl_clk_ck clock phase invert 1: Enable phase invert
26:24	clk_pextp_tl_clk_sel	pextp_tl_clk_ck clock mux select 0: cb_cksq_40m 1: cb_net2pll_d6 2: cb_mmppll_d8 3: mppll_d8_d2 4: cb_rtc_32k
23	pdn_pcie_mbist_250m	Turns off pcie_mbist_250m_ck 1: Enable clock off
20	clk_pcie_mbist_250m_inv	pcie_mbist_250m_ck clock phase invert 1: Enable phase invert
16	clk_pcie_mbist_250m_sel	pcie_mbist_250m_ck clock mux select 0: cb_cksq_40m 1: net1pll_d5_d2
15	pdn_i2c_bclk	Turns off i2c_bclk_ck 1: Enable clock off
12	clk_i2c_bclk_inv	i2c_bclk_ck clock phase invert 1: Enable phase invert
9:8	clk_i2c_bclk_sel	i2c_bclk_ck clock mux select

Bit(s)	Name	Description
		0: cb_cksq_40m
		1: net1pll_d5_d4
		2: cb_mpll_d4
		3: net1pll_d8_d4
7	pdn_pwm_bclk	Turns off pwm_bclk_ck 1: Enable clock off
4	clk_pwm_bclk_inv	pwm_bclk_ck clock phase invert 1: Enable phase invert
2:0	clk_pwm_bclk_sel	pwm_bclk_ck clock mux select 0: cb_cksq_40m 1: net1pll_d8_d2 2: net1pll_d5_d4 3: cb_mpll_d4 4: mpll_d8_d2 5: cb_rtc_32k

1001B044 CLK_CFG_4 SET SET control of clock configuration 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_4_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_4_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_4_set	Sets the corresponding bit of CLG_CFG_SEL_4 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B048 **CLK_CFG_4_CLR** CLR control of clock configuration 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_4_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_4_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_4_clr	Clears the corresponding bit of CLG_CFG_SEL_4 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B050 CLK_CFG_5 Function clock selection register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_ssusb_top_sys			clk_ssusb_top_sys_invert				clk_ssusb_top_sys_sel	pdn_pextp_tl_clk_p3			clk_pextp_tl_clk_p3_invert		clk_pextp_tl_clk_p3_sel		
Type	RW			RW				RW	RW			RW		RW		
Reset	0			0				0	0			0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_pextp_tl_clk_p2			clk_pextp_tl_clk_p2_invert		clk_pextp_tl_clk_p2_sel			pdn_pextp_tl_clk_p1			clk_pextp_tl_clk_p1_invert		clk_pextp_tl_clk_p1_sel		
Type	RW			RW		RW			RW			RW		RW		
Reset	0			0		0	0	0	0			0		0	0	0

Bit(s)	Name	Description
31	pdn_ssusb_top_sys	Turns off ssusb_top_sys_ck 1: Enable clock off
28	clk_ssusb_top_sys_invert	ssusb_top_sys_ck clock phase invert 1: Enable phase invert
24	clk_ssusb_top_sys_sel	ssusb_top_sys_ck clock mux select 0: cb_cksq_40m 1: net1pll_d5_d4
23	pdn_pextp_tl_clk_p3	Turns off pextp_tl_clk_p3_ck 1: Enable clock off
20	clk_pextp_tl_clk_p3_invert	pextp_tl_clk_p3_ck clock phase invert 1: Enable phase invert
18:16	clk_pextp_tl_clk_p3_sel	pextp_tl_clk_p3_ck clock mux select 0: cb_cksq_40m 1: cb_net2pll_d6 2: cb_mmppll_d8 3: mppll_d8_d2 4: cb_rtc_32k
15	pdn_pextp_tl_clk_p2	Turns off pextp_tl_clk_p2_ck 1: Enable clock off
12	clk_pextp_tl_clk_p2_invert	pextp_tl_clk_p2_ck clock phase invert 1: Enable phase invert
10:8	clk_pextp_tl_clk_p2_sel	pextp_tl_clk_p2_ck clock mux select

Bit(s)	Name	Description
		0: cb_cksq_40m
		1: cb_net2pll_d6
		2: cb_mmppll_d8
		3: mpll_d8_d2
		4: cb_rtc_32k
7	pdn_pextp_tl_clk_p1	Turns off pextp_tl_clk_p1_ck
		1: Enable clock off
4	clk_pextp_tl_clk_p1_inv	pextp_tl_clk_p1_ck clock phase invert
		1: Enable phase invert
2:0	clk_pextp_tl_clk_p1_sel	pextp_tl_clk_p1_ck clock mux select
		0: cb_cksq_40m
		1: cb_net2pll_d6
		2: cb_mmppll_d8
		3: mpll_d8_d2
		4: cb_rtc_32k

1001B054 CLK_CFG_5_SET SET control of clock configuration 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_5_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_5_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_5_set	Sets the corresponding bit of CLG_CFG_SEL_5 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B058 CLK_CFG_5_CLR CLR control of clock configuration 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_5_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_5_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_5_clr	Clears the corresponding bit of CLG_CFG_SEL_5 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B060 CLK_CFG_6 Function clock selection register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_ssusb_top_frmcnt			clk_ssusb_top_frmcnt_inv				clk_ssusb_top_frmcnt_sel	pdn_ssusb_top_xhci_p1			clk_ssusb_top_xhci_p1_inv				clk_ssusb_top_xhci_p1_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_ssusb_top_xhci			clk_ssusb_top_xhci_inv				clk_ssusb_top_xhci_sel	pdn_ssusb_top_sys_p1			clk_ssusb_top_sys_p1_inv				clk_ssusb_top_sys_p1_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0

Bit(s)	Name	Description
31	pdn_ssusb_top_frmcnt	Turns off ssusb_top_frmcnt_ck 1: Enable clock off
28	clk_ssusb_top_frmcnt_inv	ssusb_top_frmcnt_ck clock phase invert 1: Enable phase invert
24	clk_ssusb_top_frmcnt_sel	ssusb_top_frmcnt_ck clock mux select 0: cb_cksq_40m 1: cb_mmp1l_d3_d5
23	pdn_ssusb_top_xhci_p1	Turns off ssusb_top_xhci_p1_ck 1: Enable clock off
20	clk_ssusb_top_xhci_p1_inv	ssusb_top_xhci_p1_ck clock phase invert 1: Enable phase invert
16	clk_ssusb_top_xhci_p1_sel	ssusb_top_xhci_p1_ck clock mux select 0: cb_cksq_40m 1: net1pll_d5_d4
15	pdn_ssusb_top_xhci	Turns off ssusb_top_xhci_ck 1: Enable clock off
12	clk_ssusb_top_xhci_inv	ssusb_top_xhci_ck clock phase invert 1: Enable phase invert
8	clk_ssusb_top_xhci_sel	ssusb_top_xhci_ck clock mux select 0: cb_cksq_40m 1: net1pll_d5_d4
7	pdn_ssusb_top_sys_p1	Turns off ssusb_top_sys_p1_ck

Bit(s)	Name	Description
		1: Enable clock off
4	clk_ssusb_top_sys_p1_inv	ssusb_top_sys_p1_ck clock phase invert 1: Enable phase invert
0	clk_ssusb_top_sys_p1_sel	ssusb_top_sys_p1_ck clock mux select 0: cb_cksq_40m 1: net1pll_d5_d4

1001B064 CLK_CFG_6 SET SET control of clock configuration 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_6_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_6_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_6_set	Sets the corresponding bit of CLG_CFG_SEL_6 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B068 **CLK_CFG_6_CLR** CLR control of clock configuration 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_6_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_6_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_6_clr	Clears the corresponding bit of CLG_CFG_SEL_6 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B070 CLK_CFG_7 Function clock selection register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_aud_intbus			clk_aud_intbus_inv			clk_aud_intbus_sel		pdn_a1sys			clk_a1sys_inv				clk_a1sys_sel
Type	RW			RW			RW		RW			RW				RW
Reset	0			0			0	0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_aud			clk_aud_inv				clk_aud_sel	pdn_ssusb_top_frmcnt_p1			clk_ssusb_top_frmcnt_p1_inv				clk_ssusb_top_frmcnt_p1_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0

Bit(s)	Name	Description
31	pdn_aud_intbus	Turns off aud_intbus_ck 1: Enable clock off
28	clk_aud_intbus_inv	aud_intbus_ck clock phase invert 1: Enable phase invert
25:24	clk_aud_intbus_sel	aud_intbus_ck clock mux select 0: cb_cksq_40m 1: cb_apll2_196m 2: mpll_d8_d2
23	pdn_a1sys	Turns off a1sys_ck 1: Enable clock off
20	clk_a1sys_inv	a1sys_ck clock phase invert 1: Enable phase invert
16	clk_a1sys_sel	a1sys_ck clock mux select 0: cb_cksq_40m 1: cb_apll2_d4
15	pdn_aud	Turns off aud_ck 1: Enable clock off
12	clk_aud_inv	aud_ck clock phase invert 1: Enable phase invert
8	clk_aud_sel	aud_ck clock mux select 0: cb_cksq_40m 1: cb_apll2_196m

Bit(s)	Name	Description
7	pdn_ssusb_top_frmcnt_p1	Turns off ssusb_top_frmcnt_p1_ck 1: Enable clock off
4	clk_ssusb_top_frmcnt_p1_inv	ssusb_top_frmcnt_p1_ck clock phase invert 1: Enable phase invert
0	clk_ssusb_top_frmcnt_p1_sel	ssusb_top_frmcnt_p1_ck clock mux select 0: cb_cksq_40m 1: cb_mmp1l_d3_d5

1001B074 CLK_CFG_7 SET SET control of clock configuration 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_7_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_7_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_7_set	Sets the corresponding bit of CLG_CFG_SEL_7 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B078 **CLK_CFG_7_CLR** CLR control of clock configuration 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_7_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_7_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_7_clr	Clears the corresponding bit of CLG_CFG_SEL_7 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B080	CLK_CFG_8			Function clock selection register 8												00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_usxgmii_sbusr0			clk_usxgmii_sbusr0_inv				clk_usxgmii_sbusr0_sel	pdn_ssusb_dphy_ref			clk_ssusb_dphy_ref_inv				clk_ssusb_dphy_ref_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_sspxtp_ref			clk_sspxtp_ref_inv				clk_sspxtp_ref_sel	pdn_apll_tuner			clk_apll_tuner_inv				clk_apll_tuner_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0

Bit(s)	Name	Description
31	pdn_usxgmii_sbusr0	Turns off usxgmii_sbusr0_ck 1: Enable clock off
28	clk_usxgmii_sbusr0_inv	usxgmii_sbusr0_ck clock phase invert 1: Enable phase invert
24	clk_usxgmii_sbusr0_sel	usxgmii_sbusr0_ck clock mux select 0: cb_cksq_40m 1: net1pll_d8_d4
23	pdn_ssusb_dphy_ref	Turns off ssusb_dphy_ref_ck 1: Enable clock off
20	clk_ssusb_dphy_ref_inv	ssusb_dphy_ref_ck clock phase invert 1: Enable phase invert
16	clk_ssusb_dphy_ref_sel	ssusb_dphy_ref_ck clock mux select 0: cksq_40m_d2 1: mpll_d8_d2
15	pdn_sspxtp_ref	Turns off sspxtp_ref_ck 1: Enable clock off
12	clk_sspxtp_ref_inv	sspxtp_ref_ck clock phase invert 1: Enable phase invert
8	clk_sspxtp_ref_sel	sspxtp_ref_ck clock mux select 0: cksq_40m_d2 1: mpll_d8_d2
7	pdn_apll_tuner	Turns off apll_tuner_ck 1: Enable clock off

Bit(s)	Name	Description
4	clk_apll_tuner_inv	apll_tuner_ck clock phase invert 1: Enable phase invert
0	clk_apll_tuner_sel	apll_tuner_ck clock mux select 0: cb_cksq_40m 1: cb_apll2_d4

1001B084 CLK_CFG_8 SET SET control of clock configuration 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_8_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_8_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_8_set	Sets the corresponding bit of CLG_CFG_SEL_8 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B088 **CLK_CFG_8_CLR** CLR control of clock configuration 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_8_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_8_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_8_clr	Clears the corresponding bit of CLG_CFG_SEL_8 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B090 CLK_CFG_9 Function clock selection register 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_sg mii_1			clk_sg mii_1_i nv				clk_sg mii_1_ sel	pdn_sg mii_sb us_0			clk_sg mii_sb us_0_i nv				clk_sg mii_sb us_0_s el
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_sg mii_0			clk_sg mii_0_i nv				clk_sg mii_0_ sel	pdn_us gmii_s bus_1			clk_usx gmii_s bus_1_ inv				clk_usx gmii_s bus_1_ sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0

Bit(s)	Name	Description
31	pdn_sgmmi_1	Turns off sgmmi_1_ck 1: Enable clock off
28	clk_sgmmi_1_inv	sgmmi_1_ck clock phase invert 1: Enable phase invert
24	clk_sgmmi_1_sel	sgmmi_1_ck clock mux select 0: cb_cksq_40m 1: cb_sgmmipll_325m
23	pdn_sgmmi_sbus_0	Turns off sgmmi_sbus_0_ck 1: Enable clock off
20	clk_sgmmi_sbus_0_inv	sgmmi_sbus_0_ck clock phase invert 1: Enable phase invert
16	clk_sgmmi_sbus_0_sel	sgmmi_sbus_0_ck clock mux select 0: cb_cksq_40m 1: net1pll_d8_d4
15	pdn_sgmmi_0	Turns off sgmmi_0_ck 1: Enable clock off
12	clk_sgmmi_0_inv	sgmmi_0_ck clock phase invert 1: Enable phase invert
8	clk_sgmmi_0_sel	sgmmi_0_ck clock mux select 0: cb_cksq_40m 1: cb_sgmmipll_325m
7	pdn_usxgmii_sbus_1	Turns off usxgmii_sbus_1_ck

Bit(s)	Name	Description
		1: Enable clock off
4	clk_usxgmii_sbus_1_inv	usxgmii_sbus_1_ck clock phase invert 1: Enable phase invert
0	clk_usxgmii_sbus_1_sel	usxgmii_sbus_1_ck clock mux select 0: cb_cksq_40m 1: net1pll_d8_d4

1001B094 CLK_CFG_9_SET SET control of clock configuration 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_9_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_9_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_9_set	Sets the corresponding bit of CLG_CFG_SEL_9 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B098 CLK_CFG_9_CLR CLR control of clock configuration 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_9_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_9_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_9_clr	Clears the corresponding bit of CLG_CFG_SEL_9 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B0A0 CLK_CFG_10 Function clock selection register 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_sysaxi			clk_sysaxi_inv				clk_sysaxi_sel	pdn_xfi_phy_1_ref_xtal			clk_xfi_phy_1_ref_xtal_inv				clk_xfi_phy_1_ref_xtal_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_xfi_phy_0_ref_xtal			clk_xfi_phy_0_ref_xtal_inv				clk_xfi_phy_0_ref_xtal_sel	pdn_sg_mii_sb_us_1			clk_sg_mii_sb_us_1_inv				clk_sg_mii_sb_us_1_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0

Bit(s)	Name	Description
31	pdn_sysaxi	Turns off sysaxi_ck 1: Enable clock off
28	clk_sysaxi_inv	sysaxi_ck clock phase invert 1: Enable phase invert
24	clk_sysaxi_sel	sysaxi_ck clock mux select 0: cb_cksq_40m 1: net1pll_d8_d2
23	pdn_xfi_phy_1_ref_xtal	Turns off xfi_phy_1_ref_xtal_ck 1: Enable clock off
20	clk_xfi_phy_1_ref_xtal_inv	xfi_phy_1_ref_xtal_ck clock phase invert 1: Enable phase invert
16	clk_xfi_phy_1_ref_xtal_sel	xfi_phy_1_ref_xtal_ck clock mux select 0: cksq_40m_d2 1: mpll_d8_d2
15	pdn_xfi_phy_0_ref_xtal	Turns off xfi_phy_0_ref_xtal_ck 1: Enable clock off
12	clk_xfi_phy_0_ref_xtal_inv	xfi_phy_0_ref_xtal_ck clock phase invert 1: Enable phase invert
8	clk_xfi_phy_0_ref_xtal_sel	xfi_phy_0_ref_xtal_ck clock mux select 0: cksq_40m_d2 1: mpll_d8_d2
7	pdn_sg_mii_sb_us_1	Turns off sg_mii_sb_us_1_ck

Bit(s)	Name	Description
		1: Enable clock off
4	clk_sgmi_i_sb_1_inv	sgmii_sb_1_ck clock phase invert 1: Enable phase invert
0	clk_sgmi_i_sb_1_sel	sgmii_sb_1_ck clock mux select 0: cb_cksq_40m 1: net1pll_d8_d4

1001B0A4 **CLK_CFG_10_SET** SET control of clock configuration 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_10_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_10_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_10_set	Sets the corresponding bit of CLG_CFG_SEL_10 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B0A8 **CLK_CFG_10_CLR** CLR control of clock configuration 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_10_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_10_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_10_clr	Clears the corresponding bit of CLG_CFG_SEL_10 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B0B0		CLK_CFG_11			Function clock selection register 11										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_eth_syspll_l			clk_eth_syspll_inv				clk_eth_syspll_sel	pdn_eth_syspll_200m			clk_eth_syspll_200m_inv				clk_eth_syspll_200m_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_eth_refclk_50m			clk_eth_refclk_50m_inv				clk_eth_refclk_50m_sel	pdn_sysapb			clk_sysapb_inv				clk_sysapb_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0

Bit(s)	Name	Description
31	pdn_eth_syspll	Turns off eth_syspll_ck 1: Enable clock off
28	clk_eth_syspll_inv	eth_syspll_ck clock phase invert 1: Enable phase invert
24	clk_eth_syspll_sel	eth_syspll_ck clock mux select 0: cb_cksq_40m 1: net1pll_d5_d2
23	pdn_eth_syspll_200m	Turns off eth_syspll_200m_ck 1: Enable clock off
20	clk_eth_syspll_200m_inv	eth_syspll_200m_ck clock phase invert 1: Enable phase invert
16	clk_eth_syspll_200m_sel	eth_syspll_200m_ck clock mux select 0: cb_cksq_40m 1: cb_net2pll_d4
15	pdn_eth_refclk_50m	Turns off eth_refclk_50m_ck 1: Enable clock off
12	clk_eth_refclk_50m_inv	eth_refclk_50m_ck clock phase invert 1: Enable phase invert
8	clk_eth_refclk_50m_sel	eth_refclk_50m_ck clock mux select 0: cb_cksq_40m 1: net2pll_d4_d4
7	pdn_sysapb	Turns off sysapb_ck

Bit(s)	Name	Description
		1: Enable clock off
4	clk_sysapb_inv	sysapb_ck clock phase invert
		1: Enable phase invert
0	clk_sysapb_sel	sysapb_ck clock mux select
		0: cb_cksq_40m
		1: mpll_d3_d2

1001B0B4 **CLK_CFG_11_SET** SET control of clock configuration 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_11_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_11_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_11_set	Sets the corresponding bit of CLG_CFG_SEL_11
		0: Unchanged
		1: Set 1'b1 to the corresponding bit

1001B0B8 **CLK_CFG_11_CLR** CLR control of clock configuration 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_11_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_11_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_11_clr	Clears the corresponding bit of CLG_CFG_SEL_11 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B0C0 CLK_CFG_12 Function clock selection register 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_dramc_ref			clk_dramc_ref_inv				clk_dramc_ref_sel	pdn_npu_tops			clk_npu_tops_inv				clk_npu_tops_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_bus_tops			clk_bus_tops_inv			clk_bus_tops_sel		pdn_eth_xgmii			clk_eth_xgmii_inv			clk_eth_xgmii_sel	
Type	RW			RW			RW		RW			RW			RW	
Reset	0			0			0	0	0			0			0	0

Bit(s)	Name	Description
31	pdn_dramc_ref	Turns off dramc_ref_ck 1: Enable clock off
28	clk_dramc_ref_inv	dramc_ref_ck clock phase invert 1: Enable phase invert
24	clk_dramc_ref_sel	dramc_ref_ck clock mux select 0: cksq_40m_d2 1: mpll_d8_d2
23	pdn_npu_tops	Turns off npu_tops_ck 1: Enable clock off
20	clk_npu_tops_inv	npu_tops_ck clock phase invert 1: Enable phase invert
16	clk_npu_tops_sel	npu_tops_ck clock mux select 0: cb_cksq_40m 1: cb_net2pll_800m
15	pdn_bus_tops	Turns off bus_tops_ck 1: Enable clock off
12	clk_bus_tops_inv	bus_tops_ck clock phase invert 1: Enable phase invert
9:8	clk_bus_tops_sel	bus_tops_ck clock mux select 0: cb_cksq_40m 1: cb_net1pll_d5 2: cb_net2pll_d2
7	pdn_eth_xgmii	Turns off eth_xgmii_ck

Bit(s)	Name	Description
		1: Enable clock off
4	clk_eth_xgmii_inv	eth_xgmii_ck clock phase invert
		1: Enable phase invert
1:0	clk_eth_xgmii_sel	eth_xgmii_ck clock mux select
		0: cksq_40m_d2
		1: net1pll_d8_d8
		2: net1pll_d8_d16

1001B0C4 **CLK_CFG_12_SET** SET control of clock configuration 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_12_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_12_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_12_set	Sets the corresponding bit of CLG_CFG_SEL_12
		0: Unchanged
		1: Set 1'b1 to the corresponding bit

1001B0C8 **CLK_CFG_12_CLR** CLR control of clock configuration 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_12_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_12_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_12_clr	Clears the corresponding bit of CLG_CFG_SEL_12 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B0D0 CLK_CFG_13 Function clock selection register 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_pextp_p1_ref			clk_pextp_p1_ref_inv				clk_pextp_p1_ref_sel	pdn_pextp_p0_ref			clk_pextp_p0_ref_inv				clk_pextp_p0_ref_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_csw_infra_f26m			clk_csw_infra_f26m_inv				clk_csw_infra_f26m_sel	pdn_pwr_dramc_md32			clk_pwr_dramc_md32_inv				clk_pwr_dramc_md32_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0			0	0

Bit(s)	Name	Description
31	pdn_pextp_p1_ref	Turns off pextp_p1_ref_ck 1: Enable clock off
28	clk_pextp_p1_ref_inv	pextp_p1_ref_ck clock phase invert 1: Enable phase invert
24	clk_pextp_p1_ref_sel	pextp_p1_ref_ck clock mux select 0: cksq_40m_d2 1: mpll_d8_d2
23	pdn_pextp_p0_ref	Turns off pextp_p0_ref_ck 1: Enable clock off
20	clk_pextp_p0_ref_inv	pextp_p0_ref_ck clock phase invert 1: Enable phase invert
16	clk_pextp_p0_ref_sel	pextp_p0_ref_ck clock mux select 0: cksq_40m_d2 1: mpll_d8_d2
15	pdn_csw_infra_f26m	Turns off csw_infra_f26m_ck 1: Enable clock off
12	clk_csw_infra_f26m_inv	csw_infra_f26m_ck clock phase invert 1: Enable phase invert
8	clk_csw_infra_f26m_sel	csw_infra_f26m_ck clock mux select 0: cksq_40m_d2 1: mpll_d8_d2
7	pdn_pwr_dramc_md32	Turns off pwr_dramc_md32_ck

Bit(s)	Name	Description
		1: Enable clock off
4	clk_pwr_dramc_md32_inv	pwr_dramc_md32_ck clock phase invert 1: Enable phase invert
1:0	clk_pwr_dramc_md32_sel	pwr_dramc_md32_ck clock mux select 0: cb_cksq_40m 1: cb_mpll_d2 2: cb_wedmcupll_208m

1001B0D4 CLK_CFG_13_SET SET control of clock configuration 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_13_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_13_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_13_set	Sets the corresponding bit of CLG_CFG_SEL_13 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B0D8 CLK_CFG_13_CLR CLR control of clock configuration 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_13_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_13_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_13_clr	Clears the corresponding bit of CLG_CFG_SEL_13 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B0E0 CLK_CFG_14 Function clock selection register 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_da_xtp_glb_p1			clk_da_xtp_glb_p1_inv				clk_da_xtp_glb_p1_sel	pdn_da_xtp_glb_p0			clk_da_xtp_glb_p0_inv				clk_da_xtp_glb_p0_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_pextp_p3_ref			clk_pextp_p3_ref_inv				clk_pextp_p3_ref_sel	pdn_pextp_p2_ref			clk_pextp_p2_ref_inv				clk_pextp_p2_ref_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0

Bit(s)	Name	Description
31	pdn_da_xtp_glb_p1	Turns off da_xtp_glb_p1_ck 1: Enable clock off
28	clk_da_xtp_glb_p1_inv	da_xtp_glb_p1_ck clock phase invert 1: Enable phase invert
24	clk_da_xtp_glb_p1_sel	da_xtp_glb_p1_ck clock mux select 0: cb_cksq_40m 1: cb_net2pll_d8
23	pdn_da_xtp_glb_p0	Turns off da_xtp_glb_p0_ck 1: Enable clock off
20	clk_da_xtp_glb_p0_inv	da_xtp_glb_p0_ck clock phase invert 1: Enable phase invert
16	clk_da_xtp_glb_p0_sel	da_xtp_glb_p0_ck clock mux select 0: cb_cksq_40m 1: cb_net2pll_d8
15	pdn_pextp_p3_ref	Turns off pextp_p3_ref_ck 1: Enable clock off
12	clk_pextp_p3_ref_inv	pextp_p3_ref_ck clock phase invert 1: Enable phase invert
8	clk_pextp_p3_ref_sel	pextp_p3_ref_ck clock mux select 0: cksq_40m_d2 1: mpll_d8_d2
7	pdn_pextp_p2_ref	Turns off pextp_p2_ref_ck

Bit(s)	Name	Description
		1: Enable clock off
4	clk_pextp_p2_ref_inv	pextp_p2_ref_ck clock phase invert 1: Enable phase invert
0	clk_pextp_p2_ref_sel	pextp_p2_ref_ck clock mux select 0: cksq_40m_d2 1: mpll_d8_d2

1001B0E4 **CLK_CFG_14_SET** SET control of clock configuration 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_14_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_14_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_14_set	Sets the corresponding bit of CLG_CFG_SEL_14 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B0E8 **CLK_CFG_14_CLR** CLR control of clock configuration 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_14_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_14_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_14_clr	Clears the corresponding bit of CLG_CFG_SEL_14 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B0F0		CLK_CFG_15				Function clock selection register 15										00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_da			clk_da_inv				clk_da_sel	pdn_ckm_ref			clk_ckm_ref_inv				clk_ckm_ref_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_da_xtp_glb_p3			clk_da_xtp_glb_p3_inv				clk_da_xtp_glb_p3_sel	pdn_da_xtp_glb_p2			clk_da_xtp_glb_p2_inv				clk_da_xtp_glb_p2_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0

Bit(s)	Name	Description
31	pdn_da	Turns off da_ck 1: Enable clock off
28	clk_da_inv	da_ck clock phase invert 1: Enable phase invert
24	clk_da_sel	da_ck clock mux select 0: cksq_40m_d2 1: mpll_d8_d2
23	pdn_ckm_ref	Turns off ckm_ref_ck 1: Enable clock off
20	clk_ckm_ref_inv	ckm_ref_ck clock phase invert 1: Enable phase invert
16	clk_ckm_ref_sel	ckm_ref_ck clock mux select 0: cksq_40m_d2 1: mpll_d8_d2
15	pdn_da_xtp_glb_p3	Turns off da_xtp_glb_p3_ck 1: Enable clock off
12	clk_da_xtp_glb_p3_inv	da_xtp_glb_p3_ck clock phase invert 1: Enable phase invert
8	clk_da_xtp_glb_p3_sel	da_xtp_glb_p3_ck clock mux select 0: cb_cksq_40m 1: cb_net2pll_d8
7	pdn_da_xtp_glb_p2	Turns off da_xtp_glb_p2_ck 1: Enable clock off

Bit(s)	Name	Description
4	clk_da_xtp_glb_p2_inv	da_xtp_glb_p2_ck clock phase invert 1: Enable phase invert
0	clk_da_xtp_glb_p2_sel	da_xtp_glb_p2_ck clock mux select 0: cb_cksq_40m 1: cb_net2pll_d8

1001B0F4 CLK_CFG_15_SET SET control of clock configuration 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_15_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_15_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_15_set	Sets the corresponding bit of CLG_CFG_SEL_15 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B0F8 **CLK_CFG_15_CLR** CLR control of clock configuration 15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_15_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_15_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_15_clr	Clears the corresponding bit of CLG_CFG_SEL_15 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B100 CLK_CFG_16 Function clock selection register 16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_netsys_sync_250m			clk_netsys_sync_250m_inv				clk_netsys_sync_250m_sel	pdn_mcusys_backup_625m			clk_mcusys_backup_625m_inv				clk_mcusys_backup_625m_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_tops_p2_26m			clk_tops_p2_26m_inv				clk_tops_p2_26m_sel	pdn_pextp_ref			clk_pextp_ref_inv				clk_pextp_ref_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0

Bit(s)	Name	Description
31	pdn_netsys_sync_250m	Turns off netsys_sync_250m_ck 1: Enable clock off
28	clk_netsys_sync_250m_inv	netsys_sync_250m_ck clock phase invert 1: Enable phase invert
24	clk_netsys_sync_250m_sel	netsys_sync_250m_ck clock mux select 0: cb_cksq_40m 1: net1pll_d5_d2
23	pdn_mcusys_backup_625m	Turns off mcusys_backup_625m_ck 1: Enable clock off
20	clk_mcusys_backup_625m_inv	mcusys_backup_625m_ck clock phase invert 1: Enable phase invert
16	clk_mcusys_backup_625m_sel	mcusys_backup_625m_ck clock mux select 0: cb_cksq_40m 1: cb_net1pll_d4
15	pdn_tops_p2_26m	Turns off tops_p2_26m_ck 1: Enable clock off
12	clk_tops_p2_26m_inv	tops_p2_26m_ck clock phase invert 1: Enable phase invert
8	clk_tops_p2_26m_sel	tops_p2_26m_ck clock mux select 0: cksq_40m_d2 1: mpll_d8_d2
7	pdn_pextp_ref	Turns off pextp_ref_ck

Bit(s)	Name	Description
		1: Enable clock off
4	clk_pextp_ref_inv	pextp_ref_ck clock phase invert
		1: Enable phase invert
0	clk_pextp_ref_sel	pextp_ref_ck clock mux select
		0: cksq_40m_d2
		1: mpll_d8_d2

1001B104 CLK_CFG_16_SET SET control of clock configuration 16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_16_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_16_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_16_set	Sets the corresponding bit of CLG_CFG_SEL_16
		0: Unchanged
		1: Set 1'b1 to the corresponding bit

1001B108 **CLK_CFG_16_CLR** CLR control of clock configuration 16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_16_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_16_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_16_clr	Clears the corresponding bit of CLG_CFG_SEL_16 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B110 CLK_CFG_17 Function clock selection register 17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_netsys_warp			clk_netsys_warp_inv			clk_netsys_warp_sel		pdn_netsys_ppfb_250m			clk_netsys_ppfb_250m_inv				clk_netsys_ppfb_250m_sel
Type	RW			RW			RW		RW			RW				RW
Reset	0			0			0	0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_netsys_tops_400m			clk_netsys_tops_400m_inv				clk_netsys_tops_400m_sel	pdn_macsec			clk_macsec_inv			clk_macsec_sel	
Type	RW			RW				RW	RW			RW			RW	
Reset	0			0				0	0			0			0	0

Bit(s)	Name	Description
31	pdn_netsys_warp	Turns off netsys_warp_ck 1: Enable clock off
28	clk_netsys_warp_inv	netsys_warp_ck clock phase invert 1: Enable phase invert
25:24	clk_netsys_warp_sel	netsys_warp_ck clock mux select 0: cb_cksq_40m 1: cb_net2pll_d2 2: cb_mmppll_d2
23	pdn_netsys_ppfb_250m	Turns off netsys_ppfb_250m_ck 1: Enable clock off
20	clk_netsys_ppfb_250m_inv	netsys_ppfb_250m_ck clock phase invert 1: Enable phase invert
16	clk_netsys_ppfb_250m_sel	netsys_ppfb_250m_ck clock mux select 0: cb_cksq_40m 1: net1pll_d5_d2
15	pdn_netsys_tops_400m	Turns off netsys_tops_400m_ck 1: Enable clock off
12	clk_netsys_tops_400m_inv	netsys_tops_400m_ck clock phase invert 1: Enable phase invert
8	clk_netsys_tops_400m_sel	netsys_tops_400m_ck clock mux select 0: cb_cksq_40m 1: cb_net2pll_d2

Bit(s)	Name	Description
7	pdn_macsec	Turns off macsec_ck 1: Enable clock off
4	clk_macsec_inv	macsec_ck clock phase invert 1: Enable phase invert
1:0	clk_macsec_sel	macsec_ck clock mux select 0: cb_cksq_40m 1: cb_sgmipll_325m 2: cb_net1pll_d8

1001B114 CLK_CFG_17_SET SET control of clock configuration 17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_17_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_17_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_17_set	Sets the corresponding bit of CLG_CFG_SEL_17 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B118 CLK_CFG_17_CLR CLR control of clock configuration 17 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_17_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_17_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_17_clr	Clears the corresponding bit of CLG_CFG_SEL_17 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B120 CLK_CFG_18 Function clock selection register 18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_clk_npu			clk_clk_npu_inv			clk_clk_npu_sel		pdn_eth_mii			clk_eth_mii_inv				clk_eth_mii_sel
Type	RW			RW			RW		RW			RW				RW
Reset	0			0			0	0	0			0				0

Bit(s)	Name	Description
15	pdn_clk_npu	Turns off clk_npu_ck 1: Enable clock off
12	clk_clk_npu_inv	clk_npu_ck clock phase invert 1: Enable phase invert
9:8	clk_clk_npu_sel	clk_npu_ck clock mux select 0: cb_cksq_40m 1: cb_net2pll_800m 2: cb_mmppll_720m
7	pdn_eth_mii	Turns off eth_mii_ck 1: Enable clock off
4	clk_eth_mii_inv	eth_mii_ck clock phase invert 1: Enable phase invert
0	clk_eth_mii_sel	eth_mii_ck clock mux select 0: cksq_40m_d2 1: net2pll_d4_d8

1001B124 CLK_CFG_18_SET SET control of clock configuration 18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_18_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_18_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_18_set	Sets the corresponding bit of CLG_CFG_SEL_18 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B128 CLK_CFG_18_CLR CLR control of clock configuration 18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_18_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_18_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_18_clr	Clears the corresponding bit of CLG_CFG_SEL_18 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B140 CLK_CFG_20 Function clock selection register 20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																en_spm2cksys_mem_ck_mux_update
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
16	en_spm2cksys_mem_ck_mux_update	en_spm2cksys_mem_ck_mux_update 1: Enable

1001B144 CLK_CFG_20_SET SET control of clock configuration 20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_20_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_20_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_20_set	Sets the corresponding bit of CLG_CFG_SEL_11 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B148 **CLK_CFG_20_CLR** CLR control of clock configuration 20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_20_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_20_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_20_clr	Clears the corresponding bit of CLG_CFG_SEL_11 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B1C0	CLK_CFG_UPDATE0				Clock configuration update register 0										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		a1sys_clk_update	aud_clk_update	ssusb_top_frmcnt_p1_clk_update	ssusb_top_frmcnt_ck_update	ssusb_top_xhci_p1_clk_update	ssusb_top_xhci_ck_update	ssusb_top_sys_p1_clk_update	ssusb_top_sys_ck_update	pextp_tl_clk_p3_ck_update	pextp_tl_clk_p2_ck_update	pextp_tl_clk_p1_ck_update	pextp_tl_clk_ck_update	pcie_m_bist_250m_ck_update	i2c_bcl_k_ck_update	pwm_b_clk_ck_update
Type		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spinfi_bclck_update	nfi1x_ck_update	spim_mst_ck_update	spi_ck_update	emmc_400m_ck_update	emmc_250m_ck_update	uart_bclck_update	axi_infra_ck_update	eip197_ck_update	netsys_pao_2xwed_mcu_ck_update	netsys_gsw_ck_update	eth_gm_ii_ck_update	netsys_gsw_ck_update	netsys_2x_ck_update	netsys_500m_ck_update	netsys_ck_update
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	a1sys_clk_update	Write 1 to update the change for clk_sel and clk_inv 1: update a1sys_clkmux
29	aud_clk_update	Write 1 to update the change for clk_sel and clk_inv 1: update aud_clkmux
28	ssusb_top_frmcnt_p1_clk_update	Write 1 to update the change for clk_sel and clk_inv 1: update ssusb_top_frmcnt_p1_clkmux
27	ssusb_top_frmcnt_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update ssusb_top_frmcnt_ckmux
26	ssusb_top_xhci_p1_clk_update	Write 1 to update the change for clk_sel and clk_inv 1: update ssusb_top_xhci_p1_clkmux
25	ssusb_top_xhci_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update ssusb_top_xhci_ckmux
24	ssusb_top_sys_p1_clk_update	Write 1 to update the change for clk_sel and clk_inv 1: update ssusb_top_sys_p1_clkmux
23	ssusb_top_sys_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update ssusb_top_sys_ckmux
22	pextp_tl_clk_p3_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update pextp_tl_clk_p3_clkmux
21	pextp_tl_clk_p2_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update pextp_tl_clk_p2_clkmux
20	pextp_tl_clk_p1_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update pextp_tl_clk_p1_clkmux

Bit(s)	Name	Description
19	pextp_tl_clk_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update pextp_tl_clk_clkmux
18	pcie_mbist_250m_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update pcie_mbist_250m_clkmux
17	i2c_bclk_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update i2c_bclk_clkmux
16	pwm_bclk_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update pwm_bclk_clkmux
15	spinfi_bclk_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update spinfi_bclk_clkmux
14	nfi1x_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update nfi1x_clkmux
13	spim_mst_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update spim_mst_clkmux
12	spi_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update spi_clkmux
11	emmc_400m_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update emmc_400m_clkmux
10	emmc_250m_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update emmc_250m_clkmux
9	uart_bclk_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update uart_bclk_clkmux
8	axi_infra_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update axi_infra_clkmux
7	eip197_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update eip197_clkmux
6	netsys_pao_2x_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update netsys_pao_2x_clkmux
5	netsys_wed_mcu_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update netsys_wed_mcu_clkmux
4	eth_gmii_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update eth_gmii_clkmux

Bit(s)	Name	Description
3	netsys_gsw_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update netsys_gsw_clkmux
2	netsys_2x_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update netsys_2x_clkmux
1	netsys_500m_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update netsys_500m_clkmux
0	netsys_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update netsys_clkmux

1001B1C4 CLK_CFG_UPDATE1 Clock configuration update register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		da_xtp_glb_p3_ck_update	da_xtp_glb_p2_ck_update	da_xtp_glb_p1_ck_update	da_xtp_glb_p0_ck_update	pextp_p3_ref_ck_update	pextp_p2_ref_ck_update	pextp_p1_ref_ck_update	pextp_p0_ref_ck_update	cs_w_infra_f26m_ck_update	pwr_dramc_md32_ck_update	dramc_ref_ck_update	npu_to_ps_ck_update	bus_to_ps_ck_update	eth_xgmii_ck_update	eth_syspll_ck_update
Type		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eth_syspll_20m_ck_update	eth_refclk_50m_ck_update	sysapb_ck_update	sysaxi_ck_update	xfi_phy1_ref_xtal_ck_update	xfi_phy0_ref_xtal_ck_update	sgmii_sbus1_ck_update	sgmii1_ck_update	sgmii0_ck_update	sgmii0_ck_update	usxgmii_sbus1_ck_update	usxgmii_sbus0_ck_update	ssusb_dphy_ref_ck_update	sspxtp_ref_ck_update	apl_tuner_ck_update	aud_in_tbus_ck_update
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	da_xtp_glb_p3_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update da_xtp_glb_p3_clkmux
29	da_xtp_glb_p2_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update da_xtp_glb_p2_clkmux
28	da_xtp_glb_p1_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update da_xtp_glb_p1_clkmux
27	da_xtp_glb_p0_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update da_xtp_glb_p0_clkmux
26	pextp_p3_ref_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update pextp_p3_ref_clkmux
25	pextp_p2_ref_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update pextp_p2_ref_clkmux
24	pextp_p1_ref_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update pextp_p1_ref_clkmux
23	pextp_p0_ref_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update pextp_p0_ref_clkmux
22	cs_w_infra_f26m_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update cs_w_infra_f26m_clkmux
21	pwr_dramc_md32_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update pwr_dramc_md32_clkmux
20	dramc_ref_ck_update	Write 1 to update the change for clk_sel and clk_inv

Bit(s)	Name	Description
		1: update dramc_ref_clkmux
19	npu_tops_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update npu_tops_clkmux
18	bus_tops_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update bus_tops_clkmux
17	eth_xgmii_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update eth_xgmii_clkmux
16	eth_syspll_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update eth_syspll_clkmux
15	eth_syspll_200m_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update eth_syspll_200m_clkmux
14	eth_refclk_50m_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update eth_refclk_50m_clkmux
13	sysapb_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update sysapb_clkmux
12	sysaxi_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update sysaxi_clkmux
11	xfi_phy_1_ref_xtal_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update xfi_phy_1_ref_xtal_clkmux
10	xfi_phy_0_ref_xtal_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update xfi_phy_0_ref_xtal_clkmux
9	sgmii_sbus_1_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update sgmii_sbus_1_clkmux
8	sgmii_1_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update sgmii_1_clkmux
7	sgmii_sbus_0_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update sgmii_sbus_0_clkmux
6	sgmii_0_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update sgmii_0_clkmux
5	usxgmii_sbus_1_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update usxgmii_sbus_1_clkmux
4	usxgmii_sbus_0_ck_update	Write 1 to update the change for clk_sel and clk_inv

Bit(s)	Name	Description
		1: update usxgmii_sbus_0_clkmux
3	ssusb_dphy_ref_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update ssusb_dphy_ref_clkmux
2	sspctp_ref_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update sspctp_ref_clkmux
1	apll_tuner_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update apll_tuner_clkmux
0	aud_intbus_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update aud_intbus_clkmux

1001B1C8 CLK_CFG_UPDATE2 Clock configuration update register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					clk_npu_ck_update	eth_mii_ck_update	netsys_warp_ck_update	netsys_ppefb_250m_ck_update	netsys_tops_400m_ck_update	macsec_ck_update	netsys_sync_250m_ck_update	mcusys_backup_625m_ck_update	tops_p2_26m_ck_update	pextp_ref_ck_update	da_ck_update	ckm_ref_ck_update
Type					WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	clk_npu_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update clk_npu_clkmux
10	eth_mii_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update eth_mii_clkmux
9	netsys_warp_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update netsys_warp_clkmux
8	netsys_ppefb_250m_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update netsys_ppefb_250m_clkmux
7	netsys_tops_400m_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update netsys_tops_400m_clkmux
6	macsec_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update macsec_clkmux
5	netsys_sync_250m_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update netsys_sync_250m_clkmux
4	mcusys_backup_625m_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update mcusys_backup_625m_clkmux
3	tops_p2_26m_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update tops_p2_26m_clkmux
2	pextp_ref_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update pextp_ref_clkmux
1	da_ck_update	Write 1 to update the change for clk_sel and clk_inv 1: update da_clkmux
0	ckm_ref_ck_update	Write 1 to update the change for clk_sel and clk_inv

Bit(s)	Name	Description
		1: update ckm_ref_clkmux

1001B330	CKSTA_REG0				Function clock selection status register 0										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		a1sys_ck_change	aud_ck_change	ssusb_top_frmcnt_p1_ck_change	ssusb_top_frmcnt_ck_change	ssusb_top_xhci_p1_ck_change	ssusb_top_xhci_ck_change	ssusb_top_sys_p1_ck_change	ssusb_top_sys_ck_change	pextp_tl_clk_p3_ck_change	pextp_tl_clk_p2_ck_change	pextp_tl_clk_p1_ck_change	pextp_tl_clk_ck_change	pcie_m_bist_250m_ck_change	i2c_bcl_k_ck_change	pwm_bclk_ck_change
Type		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spinfi_bclk_ck_change	nfi1x_ck_change	spim_mst_ck_change	spi_ck_change	emmc_400m_ck_change	emmc_250m_ck_change	uart_bclk_ck_change	axi_infra_ck_change	eip197_ck_change	netssys_pao_2xwed_mcu_ck_change	netssys_wed_mcu_ck_change	eth_gm_ii_ck_change	netssys_gsw_ck_change	netssys_2x_ck_change	netssys_500m_ck_change	netssys_ck_change
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	a1sys_ck_change	Clock switch status 1: Clock switch is in progress
29	aud_ck_change	Clock switch status 1: Clock switch is in progress
28	ssusb_top_frmcnt_p1_ck_change	Clock switch status 1: Clock switch is in progress
27	ssusb_top_frmcnt_ck_change	Clock switch status 1: Clock switch is in progress
26	ssusb_top_xhci_p1_ck_change	Clock switch status 1: Clock switch is in progress
25	ssusb_top_xhci_ck_change	Clock switch status 1: Clock switch is in progress
24	ssusb_top_sys_p1_ck_change	Clock switch status 1: Clock switch is in progress
23	ssusb_top_sys_ck_change	Clock switch status 1: Clock switch is in progress
22	pextp_tl_clk_p3_ck_change	Clock switch status 1: Clock switch is in progress
21	pextp_tl_clk_p2_ck_change	Clock switch status 1: Clock switch is in progress
20	pextp_tl_clk_p1_ck_change	Clock switch status 1: Clock switch is in progress

Bit(s)	Name	Description
19	pexptp_tl_clk_ck_change	Clock switch status 1: Clock switch is in progress
18	pcie_mbist_250m_ck_change	Clock switch status 1: Clock switch is in progress
17	i2c_bclk_ck_change	Clock switch status 1: Clock switch is in progress
16	pwm_bclk_ck_change	Clock switch status 1: Clock switch is in progress
15	spinfi_bclk_ck_change	Clock switch status 1: Clock switch is in progress
14	nfi1x_ck_change	Clock switch status 1: Clock switch is in progress
13	spim_mst_ck_change	Clock switch status 1: Clock switch is in progress
12	spi_ck_change	Clock switch status 1: Clock switch is in progress
11	emmc_400m_ck_change	Clock switch status 1: Clock switch is in progress
10	emmc_250m_ck_change	Clock switch status 1: Clock switch is in progress
9	uart_bclk_ck_change	Clock switch status 1: Clock switch is in progress
8	axi_infra_ck_change	Clock switch status 1: Clock switch is in progress
7	eip197_ck_change	Clock switch status 1: Clock switch is in progress
6	netsys_pao_2x_ck_change	Clock switch status 1: Clock switch is in progress
5	netsys_wed_mcu_ck_change	Clock switch status 1: Clock switch is in progress
4	eth_gmii_ck_change	Clock switch status 1: Clock switch is in progress

Bit(s)	Name	Description
3	netsys_gsw_ck_change	Clock switch status 1: Clock switch is in progress
2	netsys_2x_ck_change	Clock switch status 1: Clock switch is in progress
1	netsys_500m_ck_change	Clock switch status 1: Clock switch is in progress
0	netsys_ck_change	Clock switch status 1: Clock switch is in progress

1001B334 CKSTA_REG1 Function clock selection status register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		da_xtp_glb_p3_ck_change	da_xtp_glb_p2_ck_change	da_xtp_glb_p1_ck_change	da_xtp_glb_p0_ck_change	pextp_p3_ref_ck_change	pextp_p2_ref_ck_change	pextp_p1_ref_ck_change	pextp_p0_ref_ck_change	csw_infra_f26m_ck_change	pwr_dramc_md32_ck_change	dramc_ref_ck_change	npu_to_ps_ck_change	bus_to_ps_ck_change	eth_xgmii_ck_change	eth_sypll_ck_change
Type		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eth_sypll_20m_ck_change	eth_refclk_50m_ck_change	sysapb_ck_change	sysaxi_ck_change	xfi_phy1_ref_xtal_ck_change	xfi_phy0_ref_xtal_ck_change	sgmii_sbus_1_ck_change	sgmii_1_ck_change	sgmii_sbus_0_ck_change	sgmii_0_ck_change	usxgmii_sbus_1_ck_change	usxgmii_sbus_0_ck_change	ssusb_dphy_ref_ck_change	sspxtp_ref_ck_change	apl_tuner_ck_change	aud_in_tbus_ck_change
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	da_xtp_glb_p3_ck_change	Clock switch status 1: Clock switch is in progress
29	da_xtp_glb_p2_ck_change	Clock switch status 1: Clock switch is in progress
28	da_xtp_glb_p1_ck_change	Clock switch status 1: Clock switch is in progress
27	da_xtp_glb_p0_ck_change	Clock switch status 1: Clock switch is in progress
26	pextp_p3_ref_ck_change	Clock switch status 1: Clock switch is in progress
25	pextp_p2_ref_ck_change	Clock switch status 1: Clock switch is in progress
24	pextp_p1_ref_ck_change	Clock switch status 1: Clock switch is in progress
23	pextp_p0_ref_ck_change	Clock switch status 1: Clock switch is in progress
22	csw_infra_f26m_ck_change	Clock switch status 1: Clock switch is in progress
21	pwr_dramc_md32_ck_change	Clock switch status 1: Clock switch is in progress
20	dramc_ref_ck_change	Clock switch status

Bit(s)	Name	Description
		1: Clock switch is in progress
19	npu_tops_ck_change	Clock switch status
		1: Clock switch is in progress
18	bus_tops_ck_change	Clock switch status
		1: Clock switch is in progress
17	eth_xgmii_ck_change	Clock switch status
		1: Clock switch is in progress
16	eth_syspll_ck_change	Clock switch status
		1: Clock switch is in progress
15	eth_syspll_200m_ck_change	Clock switch status
		1: Clock switch is in progress
14	eth_refclk_50m_ck_change	Clock switch status
		1: Clock switch is in progress
13	sysapb_ck_change	Clock switch status
		1: Clock switch is in progress
12	sysaxi_ck_change	Clock switch status
		1: Clock switch is in progress
11	xfi_phy_1_ref_xtal_ck_change	Clock switch status
		1: Clock switch is in progress
10	xfi_phy_0_ref_xtal_ck_change	Clock switch status
		1: Clock switch is in progress
9	sgmii_sbus_1_ck_change	Clock switch status
		1: Clock switch is in progress
8	sgmii_1_ck_change	Clock switch status
		1: Clock switch is in progress
7	sgmii_sbus_0_ck_change	Clock switch status
		1: Clock switch is in progress
6	sgmii_0_ck_change	Clock switch status
		1: Clock switch is in progress
5	usxgmii_sbus_1_ck_change	Clock switch status
		1: Clock switch is in progress
4	usxgmii_sbus_0_ck_change	Clock switch status

Bit(s)	Name	Description
		1: Clock switch is in progress
3	ssusb_dphy_ref_ck_change	Clock switch status 1: Clock switch is in progress
2	sspctp_ref_ck_change	Clock switch status 1: Clock switch is in progress
1	apll_tuner_ck_change	Clock switch status 1: Clock switch is in progress
0	aud_intbus_ck_change	Clock switch status 1: Clock switch is in progress

1001B200 CLK_MISC_CFG_0									Miscellaneous control							FF00FF00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ckgen_k1															
Type	RW															
Reset	1	1	1	1	1	1	1	1								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31:24	ckgen_k1	Frequency meter divider configuration 0: Measure clock does not need to be divided Other: Measure clock divided by the number

1001B210	CLK_MISC_CFG_1				Miscellaneous control								00FFF000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ckm_ref_ck_change	da_ck_change	pextp_ref_ck_change	tops_p2_26m_ck_change	mcusys_backup_625m_ck_change	netsys_sync_250m_ck_change	macsec_ck_change	netsys_tops_400m_ck_change	netsys_ppefb_250m_ck_change	netsys_warp_ck_change	eth_mii_ck_change	clk_npu_ck_change
Type					RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	ckm_ref_ck_change	Clock switch status 1: Clock switch is in progress
10	da_ck_change	Clock switch status 1: Clock switch is in progress
9	pextp_ref_ck_change	Clock switch status 1: Clock switch is in progress
8	tops_p2_26m_ck_change	Clock switch status 1: Clock switch is in progress
7	mcusys_backup_625m_ck_change	Clock switch status 1: Clock switch is in progress
6	netsys_sync_250m_ck_change	Clock switch status 1: Clock switch is in progress
5	macsec_ck_change	Clock switch status 1: Clock switch is in progress
4	netsys_tops_400m_ck_change	Clock switch status 1: Clock switch is in progress
3	netsys_ppefb_250m_ck_change	Clock switch status 1: Clock switch is in progress
2	netsys_warp_ck_change	Clock switch status 1: Clock switch is in progress
1	eth_mii_ck_change	Clock switch status 1: Clock switch is in progress
0	clk_npu_ck_change	Clock switch status

Bit(s)	Name	Description
		1: Clock switch is in progress

1001B320 CLK26CALI 0 Frequency meter control register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								fmeter_en				ckgen_clk_exc				ckgen_tri_cal
Type								RW				RW				RW
Reset								0				0				0

Bit(s)	Name	Description
8	fmeter_en	Enables crystal clock to fqmr 0: Disable fmeter 1: Enable fmeter
4	ckgen_clk_exc	Selects measure clock 1: Crystal clock 0: Measure PLL clock 0: f_fckgen_ck 1: CLK26M
0	ckgen_tri_cal	Triggers frequency meter on f_fckgen_ck Auto-cleared when calibration is done. 0: Disable 1: Enable

1001B324 CLK26CALI_1 Frequency meter control register 1 3FF00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			ckgen_load_cnt										cal_target_offset			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cal_target_value															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:20	ckgen_load_cnt	clock_sync period ('h27 =>1usï¼'h18f=>10us)
19:16	cal_target_offset	Target value offset of frequency meter result
15:0	cal_target_value	Target value of frequency meter result

1001B360 DCM_CFG DCM configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED_BITS															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVED_BITS															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RESERVED_BITS	No use

1001B400 CLKMON_CLK_SEL_REG Clock monitor selection register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ckmon4_clk_sel								ckmon3_clk_sel			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ckmon2_clk_sel								ckmon1_clk_sel			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
27:24	ckmon4_clk_sel	No use
19:16	ckmon3_clk_sel	No use
11:8	ckmon2_clk_sel	No use
3:0	ckmon1_clk_sel	No use

1001B404 CLKMON_K1_REG Clock monitor divider register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ckmon4_k4								ckmon3_k3							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ckmon2_k2								ckmon1_k1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	ckmon4_k4	No use
23:16	ckmon3_k3	No use
15:8	ckmon2_k2	No use
7:0	ckmon1_k1	No use

1001B420 CLK_AUDDIV_0 Audio clock selection register 00000701

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	apll12_ck_div_pcm											apll12_div_pcm_inv				apll12_div_pcm_pdn
Type	RW											RW				RW
Reset	0	0	0	0	0	1	1	1				0				1

Bit(s)	Name	Description
15:8	apll12_ck_div_pcm	Divider setting of f_faud_pcm_m_ck, n = [7:0] $f\_faud\_pcm\_m\_ck = \text{clock source} * [1/(n + 1)]$
4	apll12_div_pcm_inv	Inverts f_faud_pcm_m_ck clock phase 1: Enable phase inversion
0	apll12_div_pcm_pdn	Powers down apll12_div_pcm divider 1: Enable power down

2.2 TOP Reset Generator Unit (TOPRGU)

2.2.1 Register Definition

Module name: TOPRGU Base address: (+0x1001C000)

Address	Name	Width	Register Function
1001C000	<u>WDT_MODE</u>	32	Watchdog mode register
1001C004	<u>WDT_LENGTH</u>	32	Watchdog counter setting register
1001C008	<u>WDT_RESTART</u>	32	Watchdog counter restart register
1001C00C	<u>WDT_STA</u>	32	Watchdog status register
1001C010	<u>WDT_INTERVAL</u>	32	Watchdog reset pulse width register
1001C014	<u>WDT_SWRST</u>	32	Software watchdog reset register
1001C018	<u>WDT_SWSYSRST</u>	32	System software reset register
1001C01C	<u>WDT_SWSYSRST_ADD</u>	32	System software reset register
1001C030	<u>WDT_REQ_MODE</u>	32	Reset request mode register
1001C034	<u>WDT_REQ_IRQ_EN</u>	32	Reset request IRQ enable register
1001C050	<u>WDT_INTERCORE_SYNC</u>	32	Intercore sync register
1001C054	<u>WDT_INTERCORE_SYNC_SET</u>	32	Set control of intercore sync register
1001C058	<u>WDT_INTERCORE_SYNC_CLR</u>	32	Clear control of intercore sync register
1001C060	<u>STRAP_PAR</u>	32	Parallel HW trap
1001C080	<u>WDT_DEBUG_CTL3</u>	32	Debug system control register
1001C0A4	<u>WDT_PWR_LATCH</u>	32	Software bootup ready
1001C500	<u>DEBUG_0_REG</u>	32	Shadow register of WDT_MODE
1001C504	<u>DEBUG_1_REG</u>	32	Shadow register of WDT_STA
1001C50C	<u>DEBUG_3_REG</u>	32	Shadow register of WDT_REQ_MODE
1001C510	<u>DEBUG_4_REG</u>	32	Shadow register of WDT_REQ_IRQ_EN
1001C514	<u>DEBUG_5_REG</u>	32	Shadow register of WDT_DEBUG_CTL3
1001C518	<u>DEBUG_6_REG</u>	32	Watchdog counter
1001C580	<u>WDT_EAP_TIMER</u>	32	TOPRGU WDT_DEBUG(LATCH)_CTL_2 timeout value

1001C000	WDT_MODE								Watchdog mode register								0000004D	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	unlock_key																	
Type	WO																	
Reset	0	0	0	0	0	0	0	0										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name								wdt_cnt_reset_sel		dual_mode	irq_lvl_en		wdt_irq	exten	extpol	wdt_en		
Type								RW		RW	RW		RW	RW	RW	RW		
Reset								0		1	0		1	1	0	1		

Bit(s)	Name	Description
31:24	unlock_key	Write 0x22 to unlock the write protection of this register Do not change WDT_mode if WDT reboot occurs. Or else, WDT_STA is cleared.
8	wdt_cnt_reset_sel	Selects reset source of watchdog timer 0: Reset only by external reset 1: Reset by TOPRGU
6	dual_mode	Enables dual_mode Turns on watchdog timer and enables the corresponding irq_en and wdt_en if dual_mode is used 0: Disable 1: Enable
5	irq_lvl_en	Selects IRQ type 0: Edge (32K) 1: Level
3	wdt_irq	Enables watchdog timer IRQ 0: Trigger reset 1: Trigger IRQ
2	exten	Enables watchdog output reset signal 0: Disable 1: Enable
1	extpol	Watchdog output reset signal polarity 0: Active low 1: Active high
0	wdt_en	Enables watchdog timer 0: Disable

Bit(s)	Name	Description
		1: Enable

1001C004 WDT_LENGTH Watchdog counter setting register 0000FFE0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdt_length											unlock_key				
Type	RW											WO				
Reset	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
15:5	wdt_length	Watchdog timeout counter setting The counter is restarted with {wdt_length [10:0], 1_1111_1111b}, and therefore the watchdog timer timeout period is a multiple of 512*T32k=15.6ms
4:0	unlock_key	Write 0x8 to unlock the write protection of this register

1001C008 WDT_RESTART Watchdog counter restart register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdt_restart															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	wdt_restart	Write 0x1971 to reset the watchdog timeout counter

1001C00C WDT_STA Watchdog status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hw_wdt_rst	sw_wdt_rst	irq_assert	security_rst							pgu_rst	pgd_rst			debug_rst	thermal_ctl_rst
Type	RO	RO	RO	RO							RO	RO			RO	RO
Reset	0	0	0	0							0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															spm_rst	spm_thermal_rst
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
31	hw_wdt_rst	Indicates hardware watchdog generated reset is asserted
30	sw_wdt_rst	Indicates software watchdog generated reset is asserted
29	irq_assert	Indicates IRQ is asserted instead of reset
28	security_rst	Indicates security reset is asserted
21	pgu_rst	Indicates power good detect reset is asserted
20	pgd_rst	Indicates power good unit reset is asserted
17	debug_rst	Indicates debug generated reset is asserted
16	thermal_ctl_rst	Indicates thermal reset generated by thermal controller is asserted
1	spm_rst	Indicates scpsys timeout generated reset is asserted
0	spm_thermal_rst	Indicates thermal reset generated by scpsys reset is asserted

1001C010 WDT_INTERVAL Watchdog reset pulse width register 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					wdt_reset_interval											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
11:0	wdt_reset_interval	Resets pulse width generated by watchdog 2T 32K duration is required for TD modem. Unit: 1T=1x32kHz

1001C014 WDT_SWRST Software watchdog reset register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unlock_key															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	unlock_key	Write 0x1209 to generate a software watchdog reset

1001C018 WDT_SWSYSRST System software reset register 00F00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key								RESV1_bit							xfi_pll_grstb
Type	WO								RW							RW
Reset	0	0	0	0	0	0	0	0	1	1	1	1				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	xfi_pexpt_1_grstb	xfi_pexpt_0_grstb	xfi_1_grstb	xfi_0_grstb	u2phy_p1_grstb	u32phy_grstb	gephy_grstb	ethdma_grstb	u30phy_grstb		u2phy_grstb	RESV0_bit	infra_grstb	sgmii1_grstb	sgmii0_grstb	apmixedsys_grstb
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0

Bit(s)	Name	Description
31:24	unlock_key	Write 0x88 to unlock the write protection of this register
23:20	RESV1_bit	Write 1 to reset CONNSYS
16	xfi_pll_grstb	Write 1 to reset gephy
15	xfi_pexpt_1_grstb	Write 1 to reset gephy
14	xfi_pexpt_0_grstb	Write 1 to reset gephy
13	xfi_1_grstb	Write 1 to reset gephy
12	xfi_0_grstb	Write 1 to reset gephy
11	u2phy_p1_grstb	Write 1 to reset gephy
10	u32phy_grstb	Write 1 to reset gephy
9	gephy_grstb	Write 1 to reset gephy
8	ethdma_grstb	Write 1 to reset ethdma
7	u30phy_grstb	Write 1 to reset ssusb
5	u2phy_grstb	Write 1 to reset u2phy
4	RESV0_bit	Reserved
3	infra_grstb	Write 1 to reset infra
2	sgmii1_grstb	Write 1 to reset sgmii1
1	sgmii0_grstb	Write 1 to reset sgmii0
0	apmixedsys_grstb	Write 1 to reset apmixedsys

1001C01C WDT_SWSYSRST_ADD System software reset register 00F00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key								RESV_bits							
Type	WO								RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										tops_grst_b	eth_2p5f_grst_b	ckm_grst_b	pcie_p3_grst_b	pcie_p2_grst_b	pcie_p1_grst_b	pcie_p0_grst_b
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	unlock_key	Write 0x88 to unlock the write protection of this register
23:20	RESV_bits	Reserved
6	tops_grst_b	Write 1 to reset pcie
5	eth_2p5f_grst_b	Write 1 to reset u2phy
4	ckm_grst_b	Reserved
3	pcie_p3_grst_b	Write 1 to reset infra
2	pcie_p2_grst_b	Write 1 to reset sgmi1
1	pcie_p1_grst_b	Write 1 to reset sgmi0
0	pcie_p0_grst_b	Write 1 to reset apmixedsys

1001C030 WDT_REQ_MODE Reset request mode register 00330003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key										pgu_en	pgd_en			debug_en	
Type	WO										RW	RW			RW	
Reset	0	0	0	0	0	0	0	0			1	1			1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															spm_en	
Type															RW	
Reset															1	

Bit(s)	Name	Description
31:24	unlock_key	Write 0x33 to unlock the write protection of this register
21	pgu_en	Power good unit enable
20	pgd_en	Power good detect enable
17	debug_en	Enables debugsys reset
		0: Disable
		1: Enable
1	spm_en	Enables scpsys reset
		0: Disable
		1: Enable

1001C034 WDT_REQ_IRQ_EN Reset request IRQ enable register 00030003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key										pgu_irq	pgd_irq			debug_irq	
Type	WO										RW	RW			RW	
Reset	0	0	0	0	0	0	0	0			0	0			1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															scpsys_irq	
Type															RW	
Reset															1	

Bit(s)	Name	Description
31:24	unlock_key	Write 0x44 to unlock the write protection of this register
21	pgu_irq	Power good unit IRQ
20	pgd_irq	Power good detect IRQ
17	debug_irq	Triggers IRQ instead of reset when debugsys reset is enabled 0: Trigger reset 1: Trigger IRQ
1	scpsys_irq	Triggers IRQ instead of reset when scpsys reset is enabled 0: Trigger reset 1: Trigger IRQ

1001C050 WDT_INTERCORE_SYNC Intercore sync register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_intercore_sync															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_intercore_sync															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rg_intercore_sync	Register for using intercore sync

1001C054 WDT_INTERCORE_SYNC_SET Set control of intercore sync register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_intercore_sync_set															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_intercore_sync_set															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rg_intercore_sync_set	Sets 1'b1 to the corresponding bit of rg_intercore_sync

1001C058 WDT_INTERCORE_SYNC_CLR Clear control of intercore sync register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_intercore_sync_clr															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_intercore_sync_clr															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rg_intercore_sync_clr	Sets 1'b0 to the corresponding bit of rg_intercore_sync

1001C060 STRAP_PAR Parallel HW trap 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV															testmode
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:1	RESV	Reserved
0	testmode	PAD_TESTMODE value 0: Default 1: PAD_TESTMODE is set

1001C080 WDT_DEBUG_CTL3 Debug system control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key										debugsys_wdt_ack_32k					debugsys_success
Type	WO										RO					RW
Reset	0	0	0	0	0	0	0	0			0					0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	debugsys_req	debugsys_thermal_req														
Type	RW	RW														
Reset	0	0														

Bit(s)	Name	Description
31:24	unlock_key	Write 0x51 to unlock the write protection of this register
21	debugsys_wdt_ack_32k	ACK from DDR reserve mode module
16	debugsys_success	Write address 0x0 && Write data 0x23000100 to clear this bit
15	debugsys_req	Request to DDR reserve mode module in normal
14	debugsys_thermal_req	Request to DDR reserve mode module

1001C0A4 WDT_PWR_LATCH Software bootup ready 66000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key															
Type	WO															
Reset	0	1	1	0	0	1	1	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																sw_bootup_ready
Type																RW
Reset																0

Bit(s)	Name	Description
31:24	unlock_key	Writes 0x66 to unlock the write protection of this register
0	sw_bootup_ready	Informs PMIC about if system is ready during bootup at ROM stage 0: System is not ready at ROM stage. 1: System is ready at ROM stage.

1001C500 **DEBUG_0_REG** Shadow register of WDT_MODE 0000004D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								shado w_wdt _cnt_re set_sel		shado w_dual _mode	shado w_irq_l vl_en	shado w_wdt _restar t_dum my_en	shado w_wdt _irq	shado w_exte n	shado w_extp ol	shado w_wdt _en
Type								RO		RO	RO	RO	RO	RO	RO	RO
Reset								0		1	0	0	1	1	0	1

Bit(s)	Name	Description
8	shadow_wdt_cnt_reset_sel	Shadow wdt_cnt_reset_sel
6	shadow_dual_mode	Shadow dual_mode
5	shadow_irq_lvl_en	Shadow irq_lvl_en
4	shadow_wdt_restart_dummy_en	Shadow wdt_restart_dummy_en
3	shadow_wdt_irq	Shadow wdt_irq
2	shadow_exten	Shadow exten
1	shadow_extpol	Shadow extpol
0	shadow_wdt_en	Shadow wdt_en

1001C504 **DEBUG_1_REG** Shadow register of WDT_STA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	shadow_hw_wdt_rst	shadow_sw_wdt_rst	shadow_irq_assert	shadow_security_rst									shadow_debug_rst	shadow_thermal_ctl_rst		
Type	RO	RO	RO	RO									RO	RO		
Reset	0	0	0	0									0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															shadow_spm_wdt_rst	shadow_thermal_rst
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
31	shadow_hw_wdt_rst	Shadow hw_wdt_rst
30	shadow_sw_wdt_rst	Shadow sw_wdt_rst
29	shadow_irq_assert	Shadow irq_assert
28	shadow_security_rst	Shadow security_rst
19	shadow_debug_rst	Shadow debug_rst
18	shadow_thermal_ctl_rst	Shadow thermal_ctl_rst
1	shadow_spm_wdt_rst	Shadow spm_wdt_rst
0	shadow_thermal_rst	Shadow thermal_rst

1001C50C	DEBUG_3_REG				Shadow register of WDT_REQ_MODE										000F0003	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															shadow_debug_en	shadow_thermal_ctl_en
Type															RO	RO
Reset															1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															shadow_scpsys_en	shadow_thermal_en
Type															RO	RO
Reset															1	1

Bit(s)	Name	Description
17	shadow_debug_en	Shadow debug_en
16	shadow_thermal_ctl_en	Shadow thermal_ctl_en
1	shadow_scpsys_en	Shadow scpsys_en
0	shadow_thermal_en	Shadow thermal_en

1001C510 DEBUG_4_REG Shadow register of WDT_REG_IRQ_EN 00030003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															shadow_debug_irq	shadow_thermal_ctl_irq
Type															RO	RO
Reset															1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															shadow_scpsys_irq	shadow_thermal_irq
Type															RO	RO
Reset															1	1

Bit(s)	Name	Description
17	shadow_debug_irq	Shadow debug_irq
16	shadow_thermal_ctl_irq	Shadow thermal_ctl_irq
1	shadow_scpsys_irq	Shadow scpsys_irq
0	shadow_thermal_irq	Shadow thermal_irq

1001C514 DEBUG_5_REG Shadow register of WDT_DEBUG_CTL3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											shadow_debugsys_wdt_ack_32k					shadow_debugsys_success
Type											RO					RO
Reset											0					0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	shadow_debugsys_req	shadow_debugsys_thermal_req														
Type	RO	RO														
Reset	0	0														

Bit(s)	Name	Description
21	shadow_debugsys_wdt_ack_32k	Shadow debugsys_wdt_ack_32k
16	shadow_debugsys_success	Shadow debugsys_success
15	shadow_debugsys_req	Shadow debugsys_req
14	shadow_debugsys_thermal_req	Shadow debugsys_thermal_req

1001C518 DEBUG_6_REG Watchdog counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																sw_boot_rdy_status
Type																RO
Reset																0

Bit(s)	Name	Description
0	sw_boot_rdy_status	Software boot ready status

1001C580

WDT_EAP_TIMER

TOPRGU WDT_DEBUG(LATCH)_CTL_2 timeout
value

0000010F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																rg_eap_timer
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_eap_timer															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1

Bit(s)	Name	Description
16:0	rg_eap_timer	EAP timer

2.3 AP Mixedsys

2.3.1 Register Definition

Module name: APMIXEDSYS Base address: (+0x1001E000)

Address	Name	Width	Register Function
1001E000	<u>PLLON_CON0</u>	32	PLLON control 0
1001E004	<u>PLLON_CON1</u>	32	PLLON control 1
1001E008	<u>PLLON_CON2</u>	32	PLLON control 2
1001E100	<u>AP_PLLGP_8X_CON0</u>	32	AP_PLLGP_8X control 0
1001E104	<u>NETSYSPLL_CON0</u>	32	NETSYSPLL control 0
1001E108	<u>NETSYSPLL_CON1</u>	32	NETSYSPLL control 1
1001E110	<u>NETSYSPLL_CON3</u>	32	NETSYSPLL control 3
1001E114	<u>MPLL_CON0</u>	32	MPLL control 0
1001E118	<u>MPLL_CON1</u>	32	MPLL control 1
1001E120	<u>MPLL_CON3</u>	32	MPLL control 3
1001E124	<u>MMPLL_CON0</u>	32	MMPLL control 0
1001E128	<u>MMPLL_CON1</u>	32	MMPLL control 1
1001E130	<u>MMPLL_CON3</u>	32	MMPLL control 3
1001E134	<u>APLL2_CON0</u>	32	APLL2 control 0
1001E138	<u>APLL2_CON1</u>	32	APLL2 control 1
1001E140	<u>APLL2_CON3</u>	32	APLL2 control 3
1001E144	<u>NET1PLL_CON0</u>	32	NET1PLL control 0
1001E148	<u>NET1PLL_CON1</u>	32	NET1PLL control 1
1001E150	<u>NET1PLL_CON3</u>	32	NET1PLL control 3
1001E154	<u>NET2PLL_CON0</u>	32	NET2PLL control 0
1001E158	<u>NET2PLL_CON1</u>	32	NET2PLL control 1
1001E160	<u>NET2PLL_CON3</u>	32	NET2PLL control 3
1001E164	<u>WEDMCUPLL_CON0</u>	32	WEDMCUPLL control 0
1001E168	<u>WEDMCUPLL_CON1</u>	32	WEDMCUPLL control 1
1001E170	<u>WEDMCUPLL_CON3</u>	32	WEDMCUPLL control 3
1001E174	<u>SGMIIPLL_CON0</u>	32	SGMIIPLL control 0
1001E178	<u>SGMIIPLL_CON1</u>	32	SGMIIPLL control 1
1001E180	<u>SGMIIPLL_CON3</u>	32	SGMIIPLL control 3
1001E200	<u>AP_PLLGP_2X_1_CON0</u>	32	AP_PLLGP_2X_1 control 0
1001E204	<u>ARMPLL_B_CON0</u>	32	ARMPLL_B control 0
1001E208	<u>ARMPLL_B_CON1</u>	32	ARMPLL_B control 1
1001E210	<u>ARMPLL_B_CON3</u>	32	ARMPLL_B control 3
1001E214	<u>CCIPLL2_B_CON0</u>	32	CCIPLL2_B control 0
1001E218	<u>CCIPLL2_B_CON1</u>	32	CCIPLL2_B control 1
1001E220	<u>CCIPLL2_B_CON3</u>	32	CCIPLL2_B control 3
1001E300	<u>AP_PLLGP_2X_2_CON0</u>	32	AP_PLLGP_2X_2 control 0
1001E304	<u>ARMPLL_RSV_CON0</u>	32	ARMPLL_RSV control 0
1001E308	<u>ARMPLL_RSV_CON1</u>	32	ARMPLL_RSV control 1
1001E310	<u>ARMPLL_RSV_CON3</u>	32	ARMPLL_RSV control 3
1001E314	<u>MSDCPLL_CON0</u>	32	MSDCPLL control 0
1001E318	<u>MSDCPLL_CON1</u>	32	MSDCPLL control 1
1001E320	<u>MSDCPLL_CON3</u>	32	MSDCPLL control 3
1001E400	<u>AP_CLKSQ_CON0</u>	32	AP_CLKSQ control 0

Address	Name	Width	Register Function
1001E600	<u>AP_XTAL_40M_CON0</u>	32	AP_XTAL_40M control 0
1001E604	<u>AP_XTAL_40M_CON1</u>	32	AP_XTAL_40M control 1
1001E700	<u>APLL2_CON4</u>	32	APLL2 control register 4
1001E704	<u>APLL2_CON5</u>	32	APLL2 control register 5
1001E72C	<u>MMPLL_D3_CON0</u>	32	MMPLL D3 control register 0
1001E730	<u>DRAMC_CON</u>	32	DRAMC PLL setting
1001E734	<u>POR_CON1</u>	32	POR control register 1
1001E74C	<u>MCU_CLK_CTRL0</u>	32	MCUSYS clock control 0
1001E750	<u>MCU_CLK_CTRL1</u>	32	MCUSYS clock control 1
1001E754	<u>MCU_MON_CLK_SEL</u>	32	MCUSYS monitor clock select

1001E000	PLLON_CON0						PLLON control 0						03FFFFFF			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ARMPL L_B_RS TB_SEL	ARMPL L_RSV RSTB_S EL	CCIPLL 2_B_RS TB_SEL	MPLL RSTB_S EL	MMPLL RSTB_ SEL	NET1PL L_RSTB _SEL	NET2PL L_RSTB _SEL	SGMIIP LL_RST B_SEL	WEDM CUPLL RSTB_S EL	NETSYS PLL_RS TB_SEL
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDCP LL_RST B_SEL	APLL2 RSTB_S EL	CLKSQ RSTB_S EL	ARMPL L_B_EN _SEL	ARMPL L_RSV EN_SEL	CCIPLL 2_B_E N_SEL	MPLL EN_SEL	MMPLL EN_SE L	NET1PL L_EN_S EL	NET2PL L_EN_S EL	SGMIIP LL_EN SEL	WEDM CUPLL EN_SEL	NETSYS PLL_EN _SEL	MSDCP LL_EN SEL	APLL2 EN_SEL	CLKSQ EN_SE L
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
25	ARMPLL_B_RSTB_SEL	Selects ARMPLL_B RSTB control 0: Sleep control 1: Register control
24	ARMPLL_RSV_RSTB_SEL	Selects ARMPLL_RSV RSTB control 0: Sleep control 1: Register control
23	CCIPLL2_B_RSTB_SEL	Selects CCIPLL2_B RSTB control 0: Sleep control 1: Register control
22	MPLL_RSTB_SEL	Selects MPLL RSTB control 0: Sleep control 1: Register control
21	MMPLL_RSTB_SEL	Selects MMPLL RSTB control 0: Sleep control 1: Register control
20	NET1PLL_RSTB_SEL	Selects NET1PLL RSTB control 0: Sleep control 1: Register control
19	NET2PLL_RSTB_SEL	Selects NET2PLL RSTB control 0: Sleep control 1: Register control
18	SGMIIPLL_RSTB_SEL	Selects SGMIIPLL RSTB control 0: Sleep control

Bit(s)	Name	Description
		1: Register control
17	WEDMCUPLL_RSTB_SEL	Selects WEDMCUPLL RSTB control 0: Sleep control 1: Register control
16	NETSYSPLL_RSTB_SEL	Selects NETSYSPLL RSTB control 0: Sleep control 1: Register control
15	MSDCPLL_RSTB_SEL	Selects MSDCPLL RSTB control 0: Sleep control 1: Register control
14	APLL2_RSTB_SEL	Selects APLL2 RSTB control 0: Sleep control 1: Register control
13	CLKSQ_RSTB_SEL	Selects CLKSQ RSTB control 0: Sleep control 1: Register control
12	ARMPLL_B_EN_SEL	Selects ARMPLL_B enable control 0: Sleep control 1: Register control
11	ARMPLL_RSV_EN_SEL	Selects ARMPLL_RSV enable control 0: Sleep control 1: Register control
10	CCIPLL2_B_EN_SEL	Selects CCIPLL2_B enable control 0: Sleep control 1: Register control
9	MPLL_EN_SEL	Selects MPLL enable control 0: Sleep control 1: Register control
8	MMPLL_EN_SEL	Selects MMPLL enable control 0: Sleep control 1: Register control
7	NET1PLL_EN_SEL	Selects NET1PLL enable control

Bit(s)	Name	Description
		0: Sleep control
		1: Register control
6	NET2PLL_EN_SEL	Selects NET2PLL enable control
		0: Sleep control
		1: Register control
5	SGMIIPLL_EN_SEL	Selects SGMIIPLL enable control
		0: Sleep control
		1: Register control
4	WEDMCUPLL_EN_SEL	Selects WEDMCUPLL enable control
		0: Sleep control
		1: Register control
3	NETSYSPLL_EN_SEL	Selects NETSYSPLL enable control
		0: Sleep control
		1: Register control
2	MSDCPLL_EN_SEL	Selects MSDCPLL enable control
		0: Sleep control
		1: Register control
1	APLL2_EN_SEL	Selects APLL2 enable control
		0: Sleep control
		1: Register control
0	CLKSQ_EN_SEL	Selects CLKSQ enable control
		0: Sleep control
		1: Register control

1001E004	PLLON_CON1						PLLON control 1						03FFFFFF			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ARMPL L_B_IS O_SEL	ARMPL L_RSV_ ISO_SE L	CCIPLL 2_B_IS O_SEL	MPLL_I SO_SEL	MMPLL L_ISO_S EL	NET1PL L_ISO_ SEL	NET2PL L_ISO_ SEL	SGMIIP LL_ISO _SEL	WEDM CUPLL_ ISO_SE L	NETSYS PLL_IS O_SEL
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDCP LL_ISO _SEL	APLL2_ ISO_SE L	CLKSQ_ ISO_SE L	ARMPL L_B_P WR_SE L	ARMPL L_RSV_ PWR_S EL	CCIPLL 2_B_P WR_SE L	MPLL_ PWR_S EL	MMPLL PWR_ SEL	NET1PL L_PWR _SEL	NET2PL L_PWR _SEL	SGMIIP LL_PW R_SEL	WEDM CUPLL_ PWR_S EL	NETSYS PLL_P WR_SE L	MSDCP LL_PW R_SEL	APLL2_ PWR_S EL	CLKSQ_ PWR_ SEL
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
25	ARMPLL_B_ISO_SEL	Selects ARMPLL_B ISO_EN control 0: Sleep control 1: Register control
24	ARMPLL_RSV_ISO_SEL	Selects ARMPLL_RSV ISO_EN control 0: Sleep control 1: Register control
23	CCIPLL2_B_ISO_SEL	Selects CCIPLL2_B ISO_EN control 0: Sleep control 1: Register control
22	MPLL_ISO_SEL	Selects MPLL ISO_EN control 0: Sleep control 1: Register control
21	MMPLL_ISO_SEL	Selects MMPLL ISO_EN control 0: Sleep control 1: Register control
20	NET1PLL_ISO_SEL	Selects NET1PLL ISO_EN control 0: Sleep control 1: Register control
19	NET2PLL_ISO_SEL	Selects NET2PLL ISO_EN control 0: Sleep control 1: Register control
18	SGMIIPLL_ISO_SEL	Selects SGMIIPLL ISO_EN control

Bit(s)	Name	Description
		0: Sleep control
		1: Register control
17	WEDMCUPLL_ISO_SEL	Selects WEDMCUPLL ISO_EN control
		0: Sleep control
		1: Register control
16	NETSYSPLL_ISO_SEL	Selects NETSYSPLL ISO_EN control
		0: Sleep control
		1: Register control
15	MSDCPLL_ISO_SEL	Selects MSDCPLL ISO_EN control
		0: Sleep control
		1: Register control
14	APLL2_ISO_SEL	Selects APLL2 ISO_EN control
		0: Sleep control
		1: Register control
13	CLKSQ_ISO_SEL	Selects CLKSQ ISO_EN control
		0: Sleep control
		1: Register control
12	ARMPLL_B_PWR_SEL	Selects ARMPLL_B PWR_ON control
		0: Sleep control
		1: Register control
11	ARMPLL_RSV_PWR_SEL	Selects ARMPLL_RSV PWR_ON control
		0: Sleep control
		1: Register control
10	CCIPLL2_B_PWR_SEL	Selects CCIPLL2_B PWR_ON control
		0: Sleep control
		1: Register control
9	MPLL_PWR_SEL	Selects MPLL PWR_ON control
		0: Sleep control
		1: Register control
8	MMPLL_PWR_SEL	Selects MMPLL PWR_ON control
		0: Sleep control
		1: Register control

Bit(s)	Name	Description
7	NET1PLL_PWR_SEL	Selects NET1PLL PWR_ON control 0: Sleep control 1: Register control
6	NET2PLL_PWR_SEL	Selects NET2PLL PWR_ON control 0: Sleep control 1: Register control
5	SGMIIPLL_PWR_SEL	Selects SGMIIPLL PWR_ON control 0: Sleep control 1: Register control
4	WEDMCUPLL_PWR_SEL	Selects WEDMCUPLL PWR_ON control 0: Sleep control 1: Register control
3	NETSYSPLL_PWR_SEL	Selects NETSYSPLL PWR_ON control 0: Sleep control 1: Register control
2	MSDCPLL_PWR_SEL	Selects MSDCPLL PWR_ON control 0: Sleep control 1: Register control
1	APLL2_PWR_SEL	Selects APLL2 PWR_ON control 0: Sleep control 1: Register control
0	CLKSQ_PWR_SEL	Selects CLKSQ PWR_ON control 0: Sleep control 1: Register control

1001E008	PLLON_CON2						PLLON control 2						03FFE000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ARMPL L_B_O UT_OF F_SEL	ARMPL L_RSV_ OUT_O FF_SEL	CCIPLL 2_B_O UT_OF F_SEL	MPLL OUT_O FF_SEL	MMPLL OUT_ OFF_SE L	NET1PL L_OUT _OFF_S EL	NET2PL L_OUT _OFF_S EL	SGMIIP LL_OUT _OFF_S EL	WEDM CUPLL_ OUT_O FF_SEL	NETSYS PLL_O UT_OF F_SEL
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDCP LL_OU T_OFF_ SEL	APLL2_ OUT_O FF_SEL	CLKSQ OUT_O FF_SEL	ARMPL L_B_O UT_OF F	ARMPL L_RSV_ OUT_O FF	CCIPLL 2_B_O UT_OF F	MPLL OUT_O FF	MMPLL OUT_ OFF	NET1PL L_OUT _OFF	NET2PL L_OUT _OFF	SGMIIP LL_OUT _OFF	WEDM CUPLL_ OUT_O FF	NETSYS PLL_O UT_OF F	MSDCP LL_OUT _OFF	APLL2_ OUT_O FF	CLKSQ OUT_ _OFF
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25	ARMPLL_B_OUT_OFF_SEL	Selects ARMPLL_B CG control 0: Sleep control 1: Register control
24	ARMPLL_RSV_OUT_OFF_SEL	Selects ARMPLL_RSV CG control 0: Sleep control 1: Register control
23	CCIPLL2_B_OUT_OFF_SEL	Selects CCIPLL2_B CG control 0: Sleep control 1: Register control
22	MPLL_OUT_OFF_SEL	Selects MPLL CG control 0: Sleep control 1: Register control
21	MMPLL_OUT_OFF_SEL	Selects MMPLL CG control 0: Sleep control 1: Register control
20	NET1PLL_OUT_OFF_SEL	Selects NET1PLL CG control 0: Sleep control 1: Register control
19	NET2PLL_OUT_OFF_SEL	Selects NET2PLL CG control 0: Sleep control 1: Register control
18	SGMIIPLL_OUT_OFF_SEL	Selects SGMIIPLL CG control

Bit(s)	Name	Description
		0: Sleep control
		1: Register control
17	WEDMCUPLL_OUT_OFF_SEL	Selects WEDMCUPLL CG control
		0: Sleep control
		1: Register control
16	NETSYSPLL_OUT_OFF_SEL	Selects NETSYSPLL CG control
		0: Sleep control
		1: Register control
15	MSDCPLL_OUT_OFF_SEL	Selects MSDCPLL CG control
		0: Sleep control
		1: Register control
14	APLL2_OUT_OFF_SEL	Selects APLL2 CG control
		0: Sleep control
		1: Register control
13	CLKSQ_OUT_OFF_SEL	Selects CLKSQ CG control
		0: Sleep control
		1: Register control
12	ARMPLL_B_OUT_OFF	Controls ARMPLL_B CG register
11	ARMPLL_RSV_OUT_OFF	Controls ARMPLL_RSV CG register
10	CCIPLL2_B_OUT_OFF	Controls CCIPLL2_B CG register
9	MPLL_OUT_OFF	Controls MPLL CG register
8	MMPLL_OUT_OFF	Controls MMPLL CG register
7	NET1PLL_OUT_OFF	Controls NET1PLL CG register
6	NET2PLL_OUT_OFF	Controls NET2PLL CG register
5	SGMIIPLL_OUT_OFF	Controls SGMIIPLL CG register
4	WEDMCUPLL_OUT_OFF	Controls WEDMCUPLL CG register
3	NETSYSPLL_OUT_OFF	Controls NETSYSPLL CG register
2	MSDCPLL_OUT_OFF	Controls MSDCPLL CG register
1	APLL2_OUT_OFF	Controls APLL2 CG register
0	CLKSQ_OUT_OFF	Controls CLKSQ CG register

1001E100 **AP_PLLGP_8X_CON0** **AP_PLLGP_8X control 0** 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								RG_PLLGP_8X_RESERVE								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_PLLGP_8X_RESERVE							RG_PLLGP_8X_REFCK_DIV2_SEL	RG_PLLGP_8X_TST_SEL		RG_PLLGP_8X_TST_EN	RG_PLLGP_8X_TSTOP_EN	RG_PLLGP_8X_TSTOD_VOD_EN	RG_PLLGP_8X_TSTOD_EN	RG_PLLGP_8X_TSTOD_A2DCK_EN	RG_PLLGP_8X_TSTCK_EN
Type	RW							RW	RW		RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:9	RG_PLLGP_8X_RESERVE	Reserved
8	RG_PLLGP_8X_REFCK_DIV2_SEL	Reference clock divide option 1'b0: Divided by 2 1'b1: Not divided
7:6	RG_PLLGP_8X_TST_SEL	Test Mux Selection
5	RG_PLLGP_8X_TST_EN	Testing mode enable
4	RG_PLLGP_8X_TSTOP_EN	Overdrive open drain LDO
3	RG_PLLGP_8X_TSTOD_VOD_EN	Overdrive open drain LDO
2	RG_PLLGP_8X_TSTOD_EN	Enable open drain
1	RG_PLLGP_8X_TSTOD_A2DCK_EN	LPF pole control register 1'b0: 40-MHz 1'b1: 20-MHz
0	RG_PLLGP_8X_TSTCK_EN	PLL output clock testing mode enable

1001E104 NETSYSPLL CON0 NETSYSPLL control 0 00670114

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										RG_NETSYSPLL_BP	RG_NETSYSPLL_BR	RG_NETSYSPLL_LVROD_EN	RG_NETSYSPLL_RST_DLY		RG_NETSYSPLL_GLITCH_FREE_EN	RG_NETSYSPLL_BLP
Type										RW	RW	RW	RW		RW	RW
Reset										1	1	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_NETSYSPLL_SDM_FRA_EN		RG_NETSYSPLL_POSDIV				RG_NETSYSPLL_SDM_PCW_CHG		RG_NETSYSPLL_EN
Type								RW		RW				RW		RW
Reset								1		0	0	1		1		0

Bit(s)	Name	Description
22	RG_NETSYSPLL_BP	LPF pole control register 1'b0: 40-MHz 1'b1: 20-MHz
21	RG_NETSYSPLL_BR	LPF pole control register 1'b0: 40-MHz 1'b1: 20-MHz
20	RG_NETSYSPLL_LVROD_EN	Overdrive LDO
19:18	RG_NETSYSPLL_RST_DLY	ARMPLL_LL reset sequence delay control
17	RG_NETSYSPLL_GLITCH_FREE_EN	NETSYSPLL glitch free enable 1'b0: Disable 1'b1: Enable
16	RG_NETSYSPLL_BLP	LPF pole control register 1'b0: 40-MHz 1'b1: 20-MHz
8	RG_NETSYSPLL_SDM_FRA_EN	ARMPLL_LL fraction mode enable 1'b0: Integer mode 1'b1: Fraction mode
6:4	RG_NETSYSPLL_POSDIV	Post divide ratio 3'b000: /1 3'b001: /2 3'b010: /4

Bit(s)	Name	Description
		3'b011: /8
		3'b100: /16
		Others: Clock Gating
2	RG_NETSYSPLL_SDM_PCW_CHG	Feedback divide ratio update signal
0	RG_NETSYSPLL_EN	NETSYSPLL enable
		1'b0: Disable
		1'b1: Enable

1001E108 NETSYSPLL_CON1 NETSYSPLL control 1 55000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_NETSYSPLL_SDM_PCW															
Type	RW															
Reset	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_NETSYSPLL_SDM_PCW															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RG_NETSYSPLL_SDM_PCW	Feedback divide ratio
		8-bit integer + 24-bit fractional
		divider ratio = PCW[31:0]/16777216

1001E110 NETSYSPLL_CON3 NETSYSPLL control 3 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_NETSYSPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_NETSYSPLL_SDM_ISO_EN	RG_NETSYSPLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	RG_NETSYSPLL_SDM_PWR_ACK	netsyspll power ack
1	RG_NETSYSPLL_SDM_ISO_EN	netsyspll iso enable
0	RG_NETSYSPLL_SDM_PWR_ON	netsyspll power on

1001E114	MPLL CON0								MPLL control 0				E2650124			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_MPLL_DIG_DIV2_EN	RG_MPLL_DIG_DIV3_EN	RG_MPLL_DIG_DIV4_EN	RG_MPLL_DIG_DIV5_EN	RG_MPLL_DIG_DIV6_EN	RG_MPLL_DIG_DIV7_EN	RG_MPLL_DIG_DIV8_EN	RG_MPLL_DIG_DIV9_EN	RG_MPLL_DIV_RSTB	RG_MPLL_BP	RG_MPLL_BR	RG_MPLL_LVR_OD_EN	RG_MPLL_RST_DLY		RG_MPLL_GLITCH_FREE_EN	RG_MPLL_BLP
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	1	1	1	0	0	0	1	0	0	1	1	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_MPLL_SDM_FRA_EN		RG_MPLL_POSDIV				RG_MPLL_SDMP_CFG		RG_MPLL_EN
Type								RW		RW				RW		RW
Reset								1		0	1	0		1		0

Bit(s)	Name	Description
31	RG_MPLL_DIG_DIV2_EN	Enables mppll div2
30	RG_MPLL_DIG_DIV3_EN	Enables mppll div3
29	RG_MPLL_DIG_DIV4_EN	Enables mppll div4
28	RG_MPLL_DIG_DIV5_EN	Enables mppll div5
27	RG_MPLL_DIG_DIV6_EN	Enables mppll div6
26	RG_MPLL_DIG_DIV7_EN	Enables mppll div7
25	RG_MPLL_DIG_DIV8_EN	Enables mppll div8
24	RG_MPLL_DIG_DIV9_EN	Enables mppll div9
23	RG_MPLL_DIV_RSTB	PLL divider reset bar
22	RG_MPLL_BP	Not used
21	RG_MPLL_BR	Not used
20	RG_MPLL_LVR_OD_EN	Not used
19:18	RG_MPLL_RST_DLY	Not used
17	RG_MPLL_GLITCH_FREE_EN	Glitch-free divider enable 1'b0: Disable 1'b1: Enable
16	RG_MPLL_BLP	Fast locking enable 1'b0: Disable 1'b1: Enable
8	RG_MPLL_SDM_FRA_EN	SDMPLL Fractional Mode En 1'b0: Integer Mode 1'b1: Fractional Mode

Bit(s)	Name	Description
6:4	RG_MPLL_POSDIV	Post divide ratio 3'b000: /1 3'b001: /2 3'b010: /4 3'b011: /8 3'b100: /16 Others: Clock Gating
2	RG_MPLL_SDM_PCW_CHG	Feedback divide ratio update signal
0	RG_MPLL_EN	PLL Enable 1'b0: Power down 1'b1: Enable

1001E118 **MPLL_CON1** **MPLL control 1** **53333333**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_MPLL_SDM_PCW															
Type	RW															
Reset	0	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_MPLL_SDM_PCW															
Type	RW															
Reset	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

Bit(s)	Name	Description
31:0	RG_MPLL_SDM_PCW	Feedback divide ratio 8-bit integer + 24-bit fractional divider ratio = PCW[31:0]/16777216

1001E120 **MPLL_CON3** **MPLL control 3** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_MPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_MPLL_SDM_ISO_EN	RG_MPLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	RG_MPLL_SDM_PWR_ACK	mpll power ack
1	RG_MPLL_SDM_ISO_EN	mpll iso enable
0	RG_MPLL_SDM_PWR_ON	mpll power on

1001E124	MMPLL_CON0				MMPLL control 0								FA650124			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_MMPLL_DIG_DIV2_EN	RG_MMPLL_DIG_DIV3_EN	RG_MMPLL_DIG_DIV4_EN	RG_MMPLL_DIG_DIV5_EN	RG_MMPLL_DIG_DIV6_EN	RG_MMPLL_DIG_DIV7_EN	RG_MMPLL_DIG_DIV8_EN	RG_MMPLL_DIG_DIV9_EN	RG_MMPLL_DIV_RSTB	RG_MMPLL_BP	RG_MMPLL_BR	RG_MMPLL_LVROD_EN	RG_MMPLL_RST_DLY		RG_MMPLL_GLITCH_FREE_EN	RG_MMPLL_BLP
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	1	1	1	1	1	0	1	0	0	1	1	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_MMPLL_SDM_FRA_EN		RG_MMPLL_POSDIV				RG_MMPLL_SDM_PCW_CHG		RG_MMPLL_EN
Type								RW		RW				RW		RW
Reset								1		0	1	0		1		0

Bit(s)	Name	Description
31	RG_MMPLL_DIG_DIV2_EN	Enables mmpll div2
30	RG_MMPLL_DIG_DIV3_EN	Enables mmpll div3
29	RG_MMPLL_DIG_DIV4_EN	Enables mmpll div4
28	RG_MMPLL_DIG_DIV5_EN	Enables mmpll div5
27	RG_MMPLL_DIG_DIV6_EN	Enables mmpll div6
26	RG_MMPLL_DIG_DIV7_EN	Enables mmpll div7
25	RG_MMPLL_DIG_DIV8_EN	Enables mmpll div8
24	RG_MMPLL_DIG_DIV9_EN	Enables mmpll div9
23	RG_MMPLL_DIV_RSTB	PLL divider reset bar
22	RG_MMPLL_BP	Not used
21	RG_MMPLL_BR	Not used
20	RG_MMPLL_LVROD_EN	Not used
19:18	RG_MMPLL_RST_DLY	Not used
17	RG_MMPLL_GLITCH_FREE_EN	Glitch-free divider enable 1'b0: Disable 1'b1: Enable
16	RG_MMPLL_BLP	Fast locking enable 1'b0: Disable 1'b1: Enable
8	RG_MMPLL_SDM_FRA_EN	SDMPLL Fractional Mode En 1'b0: Integer Mode

Bit(s)	Name	Description
		1'b1: Fractional Mode
6:4	RG_MMPLL_POSDIV	Post divide ratio 3'b000: /1 3'b001: /2 3'b010: /4 3'b011: /8 3'b100: /16 Others: Clock Gating
2	RG_MMPLL_SDM_PCW_CHG	Feedback divide ratio update signal
0	RG_MMPLL_EN	PLL Enable 1'b0: Power down 1'b1: Enable

1001E128	<u>MMPLL_CON1</u>				MMPLL control 1								90000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_MMPLL_SDM_PCW															
Type	RW															
Reset	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_MMPLL_SDM_PCW															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RG_MMPLL_SDM_PCW	Feedback divide ratio 8-bit integer + 24-bit fractional divider ratio = PCW[31:0]/16777216

1001E130 MMPLL_CON3 MMPLL control 3 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_MMPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_MMPLL_SDM_ISO_EN	RG_MMPLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	RG_MMPLL_SDM_PWR_ACK	mmpll power ack
1	RG_MMPLL_SDM_ISO_EN	mmpll iso enable
0	RG_MMPLL_SDM_PWR_ON	mmpll power on

1001E134	APLL2_CON0				APLL2 control 0								00650134			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										RG_AP LL2_BP	RG_AP LL2_BR	RG_AP LL2_LV ROD_EN	RG_APLL2_RST _DLY		RG_AP LL2_GLI TCH_FRE EE_EN	RG_AP LL2_BLP
Type										RW	RW	RW	RW		RW	RW
Reset										1	1	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_AP LL2_SDM_FRA _EN		RG_APLL2_POSDIV				RG_AP LL2_SDM_PC W_CHG		RG_AP LL2_EN
Type								RW		RW				RW		RW
Reset								1		0	1	1		1		0

Bit(s)	Name	Description
22	RG_APLL2_BP	Not used
21	RG_APLL2_BR	Not used
20	RG_APLL2_LVROD_EN	Not used
19:18	RG_APLL2_RST_DLY	Not used
17	RG_APLL2_GLITCH_FREE_EN	Glitch-free divider enable 1'b0: Disable 1'b1: Enable
16	RG_APLL2_BLP	Fast locking enable 1'b0: Disable 1'b1: Enable
8	RG_APLL2_SDM_FRA_EN	SDMPLL Fractional Mode En 1'b0: Integer Mode 1'b1: Fractional Mode
6:4	RG_APLL2_POSDIV	Post divide ratio 3'b000: /1 3'b001: /2 3'b010: /4 3'b011: /8 3'b100: /16 Others: Clock Gating
2	RG_APLL2_SDM_PCW_CHG	Feedback divide ratio update signal

Bit(s)	Name	Description
0	RG_APLL2_EN	PLL Enable 1'b0: Power down 1'b1: Enable

1001E138 APLL2_CON1 APLL2 control 1 4EA4A8C1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_APLL2_SDM_PCW															
Type	RW															
Reset	0	1	0	0	1	1	1	0	1	0	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_APLL2_SDM_PCW															
Type	RW															
Reset	1	0	1	0	1	0	0	0	1	1	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	RG_APLL2_SDM_PCW	Feedback divide ratio 8-bit integer + 24-bit fractional divider ratio = PCW[31:0]/16777216

1001E140 **APLL2_CON3** **APLL2 control 3** 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_AP LL2_SD M_PW R_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_AP LL2_SD M_ISO _EN	RG_AP LL2_SD M_PW R_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	RG_APLL2_SDM_PWR_ACK	apll2 power ack
1	RG_APLL2_SDM_ISO_EN	apll2 iso enable
0	RG_APLL2_SDM_PWR_ON	apll2 power on

1001E144 NET1PLL_CON0 NET1PLL control 0 32650104

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_NET1PLL_DIG_DIV2_EN	RG_NET1PLL_DIG_DIV3_EN	RG_NET1PLL_DIG_DIV4_EN	RG_NET1PLL_DIG_DIV5_EN	RG_NET1PLL_DIG_DIV6_EN	RG_NET1PLL_DIG_DIV7_EN	RG_NET1PLL_DIG_DIV8_EN	RG_NET1PLL_DIG_DIV9_EN	RG_NET1PLL_DIV_RSTB	RG_NET1PLL_BP	RG_NET1PLL_BR	RG_NET1PLL_LVROD_EN	RG_NET1PLL_RST_DLY		RG_NET1PLL_GLITCH_FREE_EN	RG_NET1PLL_BLP
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	1	1	0	0	1	0	0	1	1	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_NET1PLL_SDM_FRA_EN		RG_NET1PLL_POSDIV				RG_NET1PLL_SDM_PCW_CHG		RG_NET1PLL_EN
Type								RW		RW				RW		RW
Reset								1		0	0	0		1		0

Bit(s)	Name	Description
31	RG_NET1PLL_DIG_DIV2_EN	Enables net1pll div2
30	RG_NET1PLL_DIG_DIV3_EN	Enables net1pll div3
29	RG_NET1PLL_DIG_DIV4_EN	Enables net1pll div4
28	RG_NET1PLL_DIG_DIV5_EN	Enables net1pll div5
27	RG_NET1PLL_DIG_DIV6_EN	Enables net1pll div6
26	RG_NET1PLL_DIG_DIV7_EN	Enables net1pll div7
25	RG_NET1PLL_DIG_DIV8_EN	Enables net1pll div8
24	RG_NET1PLL_DIG_DIV9_EN	Enables net1pll div9
23	RG_NET1PLL_DIV_RSTB	PLL divider reset bar
22	RG_NET1PLL_BP	Not used
21	RG_NET1PLL_BR	Not used
20	RG_NET1PLL_LVROD_EN	Not used
19:18	RG_NET1PLL_RST_DLY	Not used
17	RG_NET1PLL_GLITCH_FREE_EN	Glitch-free divider enable 1'b0: Disable 1'b1: Enable
16	RG_NET1PLL_BLP	Fast locking enable 1'b0: Disable 1'b1: Enable
8	RG_NET1PLL_SDM_FRA_EN	SDMPLL Fractional Mode En 1'b0: Integer Mode

Bit(s)	Name	Description
		1'b1: Fractional Mode
6:4	RG_NET1PLL_POSDIV	Post divide ratio 3'b000: /1 3'b001: /2 3'b010: /4 3'b011: /8 3'b100: /16 Others: Clock Gating
2	RG_NET1PLL_SDM_PCW_CHG	Feedback divide ratio update signal
0	RG_NET1PLL_EN	PLL Enable 1'b0: Power down 1'b1: Enable

1001E148	<u>NET1PLL_CON1</u>				NET1PLL control 1												7D000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	RG_NET1PLL_SDM_PCW																	
Type	RW																	
Reset	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	RG_NET1PLL_SDM_PCW																	
Type	RW																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:0	RG_NET1PLL_SDM_PCW	Feedback divide ratio 8-bit integer + 24-bit fractional divider ratio = PCW[31:0]/16777216

1001E150 **NET1PLL_CON3** **NET1PLL control 3** 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_NET1PLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_NET1PLL_SDM_ISO_EN	RG_NET1PLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	RG_NET1PLL_SDM_PWR_ACK	net1pll power ack
1	RG_NET1PLL_SDM_ISO_EN	net1pll iso enable
0	RG_NET1PLL_SDM_PWR_ON	net1pll power on

1001E154 NET2PLL_CON0 NET2PLL control 0 AA650114

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_NET2PLL_DIG_DIV2_EN	RG_NET2PLL_DIG_DIV3_EN	RG_NET2PLL_DIG_DIV4_EN	RG_NET2PLL_DIG_DIV5_EN	RG_NET2PLL_DIG_DIV6_EN	RG_NET2PLL_DIG_DIV7_EN	RG_NET2PLL_DIG_DIV8_EN	RG_NET2PLL_DIG_DIV9_EN	RG_NET2PLL_DIV_RSTB	RG_NET2PLL_BP	RG_NET2PLL_BR	RG_NET2PLL_LVROD_EN	RG_NET2PLL_RST_DLY		RG_NET2PLL_GLITCH_FREE_EN	RG_NET2PLL_BLP
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	1	0	1	0	1	0	1	0	0	1	1	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_NET2PLL_SDM_FRA_EN		RG_NET2PLL_POSDIV				RG_NET2PLL_SDM_PCW_CHG		RG_NET2PLL_EN
Type								RW		RW				RW		RW
Reset								1		0	0	1		1		0

Bit(s)	Name	Description
31	RG_NET2PLL_DIG_DIV2_EN	Enables net2pll div2
30	RG_NET2PLL_DIG_DIV3_EN	Enables net2pll div3
29	RG_NET2PLL_DIG_DIV4_EN	Enables net2pll div4
28	RG_NET2PLL_DIG_DIV5_EN	Enables net2pll div5
27	RG_NET2PLL_DIG_DIV6_EN	Enables net2pll div6
26	RG_NET2PLL_DIG_DIV7_EN	Enables net2pll div7
25	RG_NET2PLL_DIG_DIV8_EN	Enables net2pll div8
24	RG_NET2PLL_DIG_DIV9_EN	Enables net2pll div9
23	RG_NET2PLL_DIV_RSTB	PLL divider reset bar
22	RG_NET2PLL_BP	Not used
21	RG_NET2PLL_BR	Not used
20	RG_NET2PLL_LVROD_EN	Not used
19:18	RG_NET2PLL_RST_DLY	Not used
17	RG_NET2PLL_GLITCH_FREE_EN	Glitch-free divider enable 1'b0: Disable 1'b1: Enable
16	RG_NET2PLL_BLP	Fast locking enable 1'b0: Disable 1'b1: Enable
8	RG_NET2PLL_SDM_FRA_EN	SDMPLL Fractional Mode En 1'b0: Integer Mode

Bit(s)	Name	Description
		1'b1: Fractional Mode
6:4	RG_NET2PLL_POSDIV	Post divide ratio 3'b000: /1 3'b001: /2 3'b010: /4 3'b011: /8 3'b100: /16 Others: Clock Gating
2	RG_NET2PLL_SDM_PCW_CHG	Feedback divide ratio update signal
0	RG_NET2PLL_EN	PLL Enable 1'b0: Power down 1'b1: Enable

1001E158	<u>NET2PLL_CON1</u>				NET2PLL control 1								50000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_NET2PLL_SDM_PCW															
Type	RW															
Reset	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_NET2PLL_SDM_PCW															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RG_NET2PLL_SDM_PCW	Feedback divide ratio 8-bit integer + 24-bit fractional divider ratio = PCW[31:0]/16777216

1001E160 **NET2PLL_CON3** **NET2PLL control 3** 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_NET2PLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_NET2PLL_SDM_ISO_EN	RG_NET2PLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	RG_NET2PLL_SDM_PWR_ACK	net2pll power ack
1	RG_NET2PLL_SDM_ISO_EN	net2pll iso enable
0	RG_NET2PLL_SDM_PWR_ON	net2pll power on

1001E164 WEDMCUPLL_CON0 WEDMCUPLL control 0 00650134

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										RG_WEDMCUPLL_BP	RG_WEDMCUPLL_BR	RG_WEDMCUPLL_LVROD_EN	RG_WEDMCUPLL_RST_DLY		RG_WEDMCUPLL_GLITCH_FREE_EN	RG_WEDMCUPLL_BLP
Type										RW	RW	RW	RW		RW	RW
Reset										1	1	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_WEDMCUPLL_SDM_FRA_EN		RG_WEDMCUPLL_POSDIV				RG_WEDMCUPLL_SDM_PCW_CHG		RG_WEDMCUPLL_EN
Type								RW		RW				RW		RW
Reset								1		0	1	1		1		0

Bit(s)	Name	Description
22	RG_WEDMCUPLL_BP	Not used
21	RG_WEDMCUPLL_BR	Not used
20	RG_WEDMCUPLL_LVROD_EN	Not used
19:18	RG_WEDMCUPLL_RST_DLY	Not used
17	RG_WEDMCUPLL_GLITCH_FREE_EN	Glitch-free divider enable 1'b0: Disable 1'b1: Enable
16	RG_WEDMCUPLL_BLP	Fast locking enable 1'b0: Disable 1'b1: Enable
8	RG_WEDMCUPLL_SDM_FRA_EN	SDMPLL Fractional Mode En 1'b0: Integer Mode 1'b1: Fractional Mode
6:4	RG_WEDMCUPLL_POSDIV	Post divide ratio 3'b000: /1 3'b001: /2 3'b010: /4 3'b011: /8 3'b100: /16 Others: Clock Gating

Bit(s)	Name	Description
2	RG_WEDMCUPLL_SDM_PCW_CHG	Feedback divide ratio update signal
0	RG_WEDMCUPLL_EN	PLL Enable
		1'b0: Power down
		1'b1: Enable

1001E168 **WEDMCUPLL_CON1** **WEDMCUPLL control 1** **53333333**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_WEDMCUPLL_SDM_PCW															
Type	RW															
Reset	0	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_WEDMCUPLL_SDM_PCW															
Type	RW															
Reset	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

Bit(s)	Name	Description
31:0	RG_WEDMCUPLL_SDM_PCW	Feedback divide ratio
		8-bit integer + 24-bit fractional
		divider ratio = PCW[31:0]/16777216

1001E170 WEDMCUPLL_CON3 WEDMCUPLL control 3 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_WEDMCUPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_WEDMCUPLL_SDM_ISO_EN	RG_WEDMCUPLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	RG_WEDMCUPLL_SDM_PWR_ACK	wedmcupll power ack
1	RG_WEDMCUPLL_SDM_ISO_EN	wedmcupll iso enable
0	RG_WEDMCUPLL_SDM_PWR_ON	wedmcupll power on

1001E174 SGMIIPLL_CON0 SGMIIPLL control 0 00650134

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										RG_SG MIIPLL _BP	RG_SG MIIPLL _BR	RG_SG MIIPLL _LVRO D_EN	RG_SGMIIPLL_ RST_DLY		RG_SG MIIPLL _GLITC H_FREE _EN	RG_SG MIIPLL _BLP
Type										RW	RW	RW	RW		RW	RW
Reset										1	1	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_SG MIIPLL _SDM_ FRA_E N		RG_SGMIIPLL_POSDIV				RG_SG MIIPLL _SDM_ PCW_C HG		RG_SG MIIPLL _EN
Type								RW		RW				RW		RW
Reset								1		0	1	1		1		0

Bit(s)	Name	Description
22	RG_SGMIIPLL_BP	Not used
21	RG_SGMIIPLL_BR	Not used
20	RG_SGMIIPLL_LVROD_EN	Not used
19:18	RG_SGMIIPLL_RST_DLY	Not used
17	RG_SGMIIPLL_GLITCH_FREE_EN	Glitch-free divider enable 1'b0: Disable 1'b1: Enable
16	RG_SGMIIPLL_BLP	Fast locking enable 1'b0: Disable 1'b1: Enable
8	RG_SGMIIPLL_SDM_FRA_EN	SDMPLL Fractional Mode En 1'b0: Integer Mode 1'b1: Fractional Mode
6:4	RG_SGMIIPLL_POSDIV	Post divide ratio 3'b000: /1 3'b001: /2 3'b010: /4 3'b011: /8 3'b100: /16 Others: Clock Gating
2	RG_SGMIIPLL_SDM_PCW_CHG	Feedback divide ratio update signal

Bit(s)	Name	Description
0	RG_SGMIIPLL_EN	PLL Enable 1'b0: Power down 1'b1: Enable

1001E178 SGMIIPLL_CON1 SGMIIPLL control 1 82000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_SGMIIPLL_SDM_PCW															
Type	RW															
Reset	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SGMIIPLL_SDM_PCW															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RG_SGMIIPLL_SDM_PCW	Feedback divide ratio 8-bit integer + 24-bit fractional divider ratio = PCW[31:0]/16777216

1001E180 **SGMIIPLL_CON3** SGMIIPLL control 3 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_SGMIIPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_SGMIIPLL_SDM_ISO_EN	RG_SGMIIPLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	RG_SGMIIPLL_SDM_PWR_ACK	sgmiipll power ack
1	RG_SGMIIPLL_SDM_ISO_EN	sgmiipll iso enable
0	RG_SGMIIPLL_SDM_PWR_ON	sgmiipll power on

1001E200 AP_PLLGP_2X_1_CON0 AP_PLLGP_2X_1 control 0 00000005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_PLLGP_2X_MCU_TST_SEL		RG_PLLGP_2X_MCU_TST_EN	RG_PLLGP_2X_MCU_TSTOP_EN	RG_PLLGP_2X_MCU_TSTOD_VOD_EN	RG_PLLGP_2X_MCU_TSTOD_EN	RG_PLLGP_2X_MCU_TSTOD_A2DC_K_EN	RG_PLLGP_2X_MCU_TSTCK_EN	RG_PLLGP_2X_MCU_RESERVE							
Type	RW		RW	RW	RW	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit(s)	Name	Description
15:14	RG_PLLGP_2X_MCU_TST_SEL	Test mux selection
13	RG_PLLGP_2X_MCU_TST_EN	Testing mode enable
12	RG_PLLGP_2X_MCU_TSTOP_EN	Overdrive open drain LDO
11	RG_PLLGP_2X_MCU_TSTOD_VOD_EN	Overdrive open drain LDO
10	RG_PLLGP_2X_MCU_TSTOD_EN	Enable open drain
9	RG_PLLGP_2X_MCU_TSTOD_A2DCK_EN	LPF pole control register 1'b0: 40-MHz 1'b1: 20-MHz
8	RG_PLLGP_2X_MCU_TSTCK_EN	PLL output clock testing mode enable
7:0	RG_PLLGP_2X_MCU_RESERVE	bit7~4: Reserved register bit3~2: ARMPLL_B reference clock divide option bit1~0: CCIPLL2_B reference clock divide option 2'b01: Divided by 2 2'b11: Divided by 4

1001E204 ARMPLL_B_CON0 ARMPLL_B control 0 00650114

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_ARMPLL_B_DIG_DIV2_EN	RG_ARMPLL_B_DIG_DIV3_EN	RG_ARMPLL_B_DIG_DIV4_EN	RG_ARMPLL_B_DIG_DIV5_EN	RG_ARMPLL_B_DIG_DIV6_EN	RG_ARMPLL_B_DIG_DIV7_EN	RG_ARMPLL_B_DIG_DIV8_EN	RG_ARMPLL_B_DIG_DIV9_EN	RG_ARMPLL_B_DIV_RSTB	RG_ARMPLL_B_BP	RG_ARMPLL_B_BR	RG_ARMPLL_B_LVRD_OD_EN	RG_ARMPLL_B_RST_DLY		RG_ARMPLL_B_GLITCH_FREE_EN	RG_ARMPLL_B_BLP
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_ARMPLL_B_SDM_FRA_EN		RG_ARMPLL_B_POSDIV				RG_ARMPLL_B_SDM_PCW_CHG		RG_ARMPLL_B_EN
Type								RW		RW				RW		RW
Reset								1		0	0	1		1		0

Bit(s)	Name	Description
31	RG_ARMPLL_B_DIG_DIV2_EN	Enables armppll_b div2
30	RG_ARMPLL_B_DIG_DIV3_EN	Enables armppll_b div3
29	RG_ARMPLL_B_DIG_DIV4_EN	Enables armppll_b div4
28	RG_ARMPLL_B_DIG_DIV5_EN	Enables armppll_b div5
27	RG_ARMPLL_B_DIG_DIV6_EN	Enables armppll_b div6
26	RG_ARMPLL_B_DIG_DIV7_EN	Enables armppll_b div7
25	RG_ARMPLL_B_DIG_DIV8_EN	Enables armppll_b div8
24	RG_ARMPLL_B_DIG_DIV9_EN	Enables armppll_b div9
23	RG_ARMPLL_B_DIV_RSTB	PLL divider reset bar
22	RG_ARMPLL_B_BP	LPF pole control register 1'b0: 40-MHz 1'b1: 20-MHz
21	RG_ARMPLL_B_BR	LPF pole control register 1'b0: 40-MHz 1'b1: 20-MHz
20	RG_ARMPLL_B_LVRD_OD_EN	Overdrive LDO
19:18	RG_ARMPLL_B_RST_DLY	ARMPLL reset sequence delay control
17	RG_ARMPLL_B_GLITCH_FREE_EN	ARMPLL glitch free enable 1'b0: Disable 1'b1: Enable
16	RG_ARMPLL_B_BLP	LPF pole control register

Bit(s)	Name	Description
		1'b0: 40-MHz
		1'b1: 20-MHz
8	RG_ARMPLL_B_SDM_FRA_EN	ARMPLL_B fraction mode enable 1'b0: Integer mode 1'b1: Fraction mode
6:4	RG_ARMPLL_B_POSDIV	Post divide ratio 3'b000: /1 3'b001: /2 3'b010: /4 3'b011: /8 3'b100: /16 Others: Clock Gating
2	RG_ARMPLL_B_SDM_PCW_CHG	Feedback divide ratio update signal
0	RG_ARMPLL_B_EN	ARMPLL_B enable 1'b0: Disable 1'b1: Enable

1001E208 ARMPLL_B_CON1 ARMPLL_B control 1 A0000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_ARMPLL_B_SDM_PCW															
Type	RW															
Reset	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ARMPLL_B_SDM_PCW															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RG_ARMPLL_B_SDM_PCW	Feedback divide ratio 8-bit integer + 24-bit fractional divider ratio = PCW[31:0]/16777216

1001E210 **ARMPLL_B_CON3** **ARMPLL_B control 3** 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_ARMPLL_B_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_ARMPLL_B_SDM_ISO_EN	RG_ARMPLL_B_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	RG_ARMPLL_B_SDM_PWR_ACK	armpll_b power ack
1	RG_ARMPLL_B_SDM_ISO_EN	armpll_b iso enable
0	RG_ARMPLL_B_SDM_PWR_ON	armpll_b power on

1001E214	CCIPLL2_B_CON0							CCIPLL2_B control 0					00650114				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	RG_CCIPLL2_B_DIG_DIV2_EN	RG_CCIPLL2_B_DIG_DIV3_EN	RG_CCIPLL2_B_DIG_DIV4_EN	RG_CCIPLL2_B_DIG_DIV5_EN	RG_CCIPLL2_B_DIG_DIV6_EN	RG_CCIPLL2_B_DIG_DIV7_EN	RG_CCIPLL2_B_DIG_DIV8_EN	RG_CCIPLL2_B_DIG_DIV9_EN	RG_CCIPLL2_B_DIV_RSTB	RG_CCIPLL2_B_BP	RG_CCIPLL2_B_BR	RG_CCIPLL2_B_LVROD_EN	RG_CCIPLL2_B_RST_DLY		RG_CCIPLL2_B_GLITCH_FREE_EN	RG_CCIPLL2_B_BLP	
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name								RG_CCIPLL2_B_SDM_FRA_EN		RG_CCIPLL2_B_POSDIV				RG_CCIPLL2_B_SDM_PCW_CFG		RG_CCIPLL2_B_EN	
Type								RW		RW				RW		RW	
Reset								1		0	0	1		1		0	

Bit(s)	Name	Description
31	RG_CCIPLL2_B_DIG_DIV2_EN	Enables ccipll2_b div2
30	RG_CCIPLL2_B_DIG_DIV3_EN	Enables ccipll2_b div3
29	RG_CCIPLL2_B_DIG_DIV4_EN	Enables ccipll2_b div4
28	RG_CCIPLL2_B_DIG_DIV5_EN	Enables ccipll2_b div5
27	RG_CCIPLL2_B_DIG_DIV6_EN	Enables ccipll2_b div6
26	RG_CCIPLL2_B_DIG_DIV7_EN	Enables ccipll2_b div7
25	RG_CCIPLL2_B_DIG_DIV8_EN	Enables ccipll2_b div8
24	RG_CCIPLL2_B_DIG_DIV9_EN	Enables ccipll2_b div9
23	RG_CCIPLL2_B_DIV_RSTB	PLL divider reset bar
22	RG_CCIPLL2_B_BP	LPF pole control register 1'b0: 40-MHz 1'b1: 20-MHz
21	RG_CCIPLL2_B_BR	LPF pole control register 1'b0: 40-MHz 1'b1: 20-MHz
20	RG_CCIPLL2_B_LVROD_EN	Overdrive LDO
19:18	RG_CCIPLL2_B_RST_DLY	CCIPLL2_B reset sequence delay control
17	RG_CCIPLL2_B_GLITCH_FREE_EN	CCIPLL2_B glitch free enable 1'b0: Disable 1'b1: Enable
16	RG_CCIPLL2_B_BLP	LPF pole control register

Bit(s)	Name	Description
		1'b0: 40-MHz
		1'b1: 20-MHz
8	RG_CCIPLL2_B_SDM_FRA_EN	CCIPLL2_B fraction mode enable 1'b0: Integer mode 1'b1: Fraction mode
6:4	RG_CCIPLL2_B_POSDIV	Post divide ratio 3'b000: /1 3'b001: /2 3'b010: /4 3'b011: /8 3'b100: /16 Others: Clock Gating
2	RG_CCIPLL2_B_SDM_PCW_CHG	Feedback divide ratio update signal
0	RG_CCIPLL2_B_EN	CCIPLL2_B enable 1'b0: Disable 1'b1: Enable

1001E218 CCIPLL2_B_CON1 CCIPLL2_B control 1 60000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CCIPLL2_B_SDM_PCW															
Type	RW															
Reset	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_CCIPLL2_B_SDM_PCW															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RG_CCIPLL2_B_SDM_PCW	Feedback divide ratio 8-bit integer + 24-bit fractional divider ratio = PCW[31:0]/16777216

1001E220 CCIPLL2_B_CON3 CCIPLL2_B control 3 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_CCIPLL2_B_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_CCIPLL2_B_SDM_ISO_EN	RG_CCIPLL2_B_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	RG_CCIPLL2_B_SDM_PWR_ACK	ccipll2_b power ack
1	RG_CCIPLL2_B_SDM_ISO_EN	ccipll2_b iso enable
0	RG_CCIPLL2_B_SDM_PWR_ON	ccipll2_b power on

1001E300 AP_PLLGP_2X_2_CON0 AP_PLLGP_2X_2 control 0 00000005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_PLLGP_2X_TST_SEL		RG_PLLGP_2X_TST_EN	RG_PLLGP_2X_TSTOP_EN	RG_PLLGP_2X_TSTOD_VOD_EN	RG_PLLGP_2X_TSTOD_EN	RG_PLLGP_2X_TSTOD_A2DCK_EN	RG_PLLGP_2X_TSTCK_EN	RG_PLLGP_2X_RESERVE							
Type	RW		RW	RW	RW	RW	RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit(s)	Name	Description
15:14	RG_PLLGP_2X_TST_SEL	Test mux selection
13	RG_PLLGP_2X_TST_EN	Testing mode enable
12	RG_PLLGP_2X_TSTOP_EN	Overdrive open drain LDO
11	RG_PLLGP_2X_TSTOD_VOD_EN	Overdrive open drain LDO
10	RG_PLLGP_2X_TSTOD_EN	Enables open drain
9	RG_PLLGP_2X_TSTOD_A2DCK_EN	LPF pole control register 1'b0: 40-MHz 1'b1: 20-MHz
8	RG_PLLGP_2X_TSTCK_EN	PLL output clock testing mode enable
7:0	RG_PLLGP_2X_RESERVE	bit7~4: Reserved register bit3~2: ARMPLL_RSV reference clock divide option bit1~0: MSDCPLL reference clock divide option 2'b01: Divided by 2 2'b11: Divided by 4

1001E304 ARMPLL_RSV_CON0 ARMPLL_RSV control 0 00650124

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_ARMPLL_RSV_DIV2_EN	RG_ARMPLL_RSV_DIV3_EN	RG_ARMPLL_RSV_DIV4_EN	RG_ARMPLL_RSV_DIV5_EN	RG_ARMPLL_RSV_DIV6_EN	RG_ARMPLL_RSV_DIV7_EN	RG_ARMPLL_RSV_DIV8_EN	RG_ARMPLL_RSV_DIV9_EN	RG_ARMPLL_RSV_DIV_RSTB	RG_ARMPLL_RSV_BP	RG_ARMPLL_RSV_BR	RG_ARMPLL_RSV_LVROD_EN	RG_ARMPLL_RSV_RST_DLY		RG_ARMPLL_RSV_GLITCH_FREE_EN	RG_ARMPLL_RSV_BLP
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_ARMPLL_RSV_SDM_FRA_EN		RG_ARMPLL_RSV_POSDIV				RG_ARMPLL_RSV_SDM_PCW_CHG		RG_ARMPLL_RSV_EN
Type								RW		RW				RW		RW
Reset								1		0	1	0		1		0

Bit(s)	Name	Description
31	RG_ARMPLL_RSV_DIV2_EN	Enables armppll_rsv div2
30	RG_ARMPLL_RSV_DIV3_EN	Enables armppll_rsv div3
29	RG_ARMPLL_RSV_DIV4_EN	Enables armppll_rsv div4
28	RG_ARMPLL_RSV_DIV5_EN	Enables armppll_rsv div5
27	RG_ARMPLL_RSV_DIV6_EN	Enables armppll_rsv div6
26	RG_ARMPLL_RSV_DIV7_EN	Enables armppll_rsv div7
25	RG_ARMPLL_RSV_DIV8_EN	Enables armppll_rsv div8
24	RG_ARMPLL_RSV_DIV9_EN	Enables armppll_rsv div9
23	RG_ARMPLL_RSV_DIV_RSTB	PLL divider reset bar
22	RG_ARMPLL_RSV_BP	LPF pole control register 1'b0: 40-MHz 1'b1: 20-MHz
21	RG_ARMPLL_RSV_BR	LPF pole control register 1'b0: 40-MHz 1'b1: 20-MHz
20	RG_ARMPLL_RSV_LVROD_EN	Overdrive LDO
19:18	RG_ARMPLL_RSV_RST_DLY	ARMPLL_RSV reset sequence delay control
17	RG_ARMPLL_RSV_GLITCH_FREE_EN	ARMPLL_RSV glitch free enable 1'b0: Disable 1'b1: Enable
16	RG_ARMPLL_RSV_BLP	LPF pole control register

Bit(s)	Name	Description
		1'b0: 40-MHz
		1'b1: 20-MHz
8	RG_ARMPLL_RSV_SDM_FRA_EN	ARMPLL_RSV fraction mode enable 1'b0: Integer mode 1'b1: Fraction mode
6:4	RG_ARMPLL_RSV_POSDIV	Post divide ratio 3'b000: /1 3'b001: /2 3'b010: /4 3'b011: /8 3'b100: /16 Others: Clock Gating
2	RG_ARMPLL_RSV_SDM_PCW_CHG	Feedback divide ratio update signal
0	RG_ARMPLL_RSV_EN	ARMPLL_RSV enable 1'b0: Disable 1'b1: Enable

1001E308 ARMPLL_RSV_CON1 ARMPLL_RSV control 1 80E80000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_ARMPLL_RSV_SDM_PCW															
Type	RW															
Reset	1	0	0	0	0	0	0	0	1	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ARMPLL_RSV_SDM_PCW															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RG_ARMPLL_RSV_SDM_PCW	Feedback divide ratio 8-bit integer + 24-bit fractional divider ratio = PCW[31:0]/16777216

1001E310 ARMPLL_RSV_CON3 ARMPLL_RSV control 3 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_ARMPLL_RSV_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_ARMPLL_RSV_SDM_ISO_EN	RG_ARMPLL_RSV_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	RG_ARMPLL_RSV_SDM_PWR_ACK	armpll_rsv power ack
1	RG_ARMPLL_RSV_SDM_ISO_EN	armpll_rsv iso enable
0	RG_ARMPLL_RSV_SDM_PWR_ON	armpll_rsv power on

1001E314	MSDCPLL_CON0				MSDCPLL control 0								00650124			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										RG_MS DCPLL_ BP	RG_MS DCPLL_ BR	RG_MS DCPLL_ LVROD_ _EN	RG_MSDCPLL_ RST_DLY		RG_MS DCPLL_ GLITCH_ FREE_ _EN	RG_MS DCPLL_ BLP
Type										RW	RW	RW	RW		RW	RW
Reset										1	1	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_MS DCPLL_ SDM_F RA_EN		RG_MSDCPLL_POSDIV				RG_MS DCPLL_ SDM_P CW_CH G		RG_MS DCPLL_ EN
Type								RW		RW				RW		RW
Reset								1		0	1	0		1		0

Bit(s)	Name	Description
22	RG_MSDCPLL_BP	LPF pole control register 1'b0: 40-MHz 1'b1: 20-MHz
21	RG_MSDCPLL_BR	LPF pole control register 1'b0: 40-MHz 1'b1: 20-MHz
20	RG_MSDCPLL_LVROD_EN	Overdrive LDO
19:18	RG_MSDCPLL_RST_DLY	MSDCPLL reset sequence delay control
17	RG_MSDCPLL_GLITCH_FREE_EN	MSDCPLL glitch free enable 1'b0: Disable 1'b1: Enable
16	RG_MSDCPLL_BLP	LPF pole control register 1'b0: 40-MHz 1'b1: 20-MHz
8	RG_MSDCPLL_SDM_FRA_EN	MSDCPLL fraction mode enable 1'b0: Integer mode 1'b1: Fraction mode
6:4	RG_MSDCPLL_POSDIV	Post divide ratio 3'b000: /1 3'b001: /2 3'b010: /4

Bit(s)	Name	Description
		3'b011: /8
		3'b100: /16
		Others: Clock Gating
2	RG_MSDCPLL_SDM_PCW_CHG	Feedback divide ratio update signal
0	RG_MSDCPLL_EN	MSDCPLL enable
		1'b0: Disable
		1'b1: Enable

1001E318 **MSDCPLL_CON1** **MSDCPLL control 1** **50000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_MSDCPLL_SDM_PCW															
Type	RW															
Reset	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_MSDCPLL_SDM_PCW															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RG_MSDCPLL_SDM_PCW	Feedback divide ratio 8-bit integer + 24-bit fractional divider ratio = PCW[31:0]/16777216

1001E320 **MSDCPLL_CON3** **MSDCPLL control 3** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RG_MSDCPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_MSDCPLL_SDM_ISO_EN	RG_MSDCPLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	RG_MSDCPLL_SDM_PWR_ACK	msdcpll power ack
1	RG_MSDCPLL_SDM_ISO_EN	msdcpll iso enable
0	RG_MSDCPLL_SDM_PWR_ON	msdcpll power on

1001E400 AP_CLKSQ_CON0 AP_CLKSQ control 0 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_CLKSQ_IFCK_52MHZ	RG_CLKSQ_BIAS_LPF_EN	RG_CLKSQ_VOD_EN	RG_CLKSQ_LPF_EN	RG_CLKSQ_HYS_EN	RG_CLKSQ_EN
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	1	1

Bit(s)	Name	Description
5	RG_CLKSQ_IFCK_52MHZ	Whether output clock is divided by 2 1'b0: Direct output 1'b1: Divided by 2
4	RG_CLKSQ_BIAS_LPF_EN	Low-pass filter V2I's output
3	RG_CLKSQ_VOD_EN	Reserved
2	RG_CLKSQ_LPF_EN	Clock square low-pass filter enable 1'b0: Disable 1'b1: Enable
1	RG_CLKSQ_HYS_EN	Clock square hysteresis enable
0	RG_CLKSQ_EN	Clock square enable 1'b0: Disable 1'b1: Enable

1001E600 AP_XTAL_40M_CON0 AP_XTAL_40M control 0 01FFC00F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								RG_AD_XTAL40M_CKM_EN	RG_AD_XTAL40M_USXGMII_EN	RG_AD_XTAL40M_2P5GBE_EN	RG_AD_XTAL40M_GBUSB_EN	RG_AD_XTAL40M_SSUSB_EN	RG_AD_XTAL40M_CKM_EN	RG_AD_XTAL40M_USXGMII_EN	RG_AD_XTAL40M_2P5GBE_EN	RG_AD_XTAL40M_GBUSB_EN
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AD_XTAL40M_SSUSB_EN	RG_XTAL_EN	RG_XTAL_RESERVED								RG_XTAL_LDO_SEL		RG_XTAL_GM			
Type	RW	RW	RW								RW		RW			
Reset	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit(s)	Name	Description
24	RG_AD_XTAL40M_CKM_EN	CKM analog to digital crystal clock enable 1'b1: Disable 1'b0: Enable
23	RG_AD_XTAL40M_USXGMII_EN	USXGMII analog to digital crystal clock enable 1'b1: Disable 1'b0: Enable
22	RG_AD_XTAL40M_2P5GBE_EN	2P5GBE analog to digital crystal clock enable 1'b1: Disable 1'b0: Enable
21	RG_AD_XTAL40M_GBUSB_EN	GBE analog to digital crystal clock enable 1'b1: Disable 1'b0: Enable
20	RG_AD_XTAL40M_SSUSB_EN	SSUSB analog to digital crystal clock enable 1'b1: Disable 1'b0: Enable
19	RG_AD_XTAL40M_CKM_EN	CKM analog direct to analog crystal clock enable 1'b1: Disable 1'b0: Enable
18	RG_AD_XTAL40M_USXGMII_EN	USXGMII analog direct to analog crystal clock enable 1'b1: Disable 1'b0: Enable

Bit(s)	Name	Description
17	RG_ADA_XTAL40M_2P5GBE_EN	2P5GBE analog direct to analog crystal clock enable 1'b1: Disable 1'b0: Enable
16	RG_ADA_XTAL40M_GBE_EN	GBE analog direct to analog crystal clock enable 1'b1: Disable 1'b0: Enable
15	RG_ADA_XTAL40M_SSUSB_EN	SSUSB analog direct to analog crystal clock enable 1'b1: Disable 1'b0: Enable
14	RG_XTAL_EN	XTAL Enable. If choose RF_CLK_IN --> XTAL Off, or always On 1'b1: Disable 1'b0: Enable
13:6	RG_XTAL_RESERVED	XTAL AAC AMP Select and reserved registers [1:0]: Adjust amplitude ladder 2'b11: Larger swing 2'b00: Smaller swing [2]: Improve phase noise (test pin) [7:3]: N/A
5:4	RG_XTAL_LDO_SEL	XTAL LDO output Combine the following two bits to adjust XTAL LDO voltage. [1:0]: 2'b00: 0.84V 2'b01: 0.88V 2'b10: 0.80V 2'b11: 0.76V
3:0	RG_XTAL_GM	XTAL Gm control Without AAC, XTALO swing increases with increasing Gm. With AAC, XTALO swing is controlled to an adaptive value. With AAC, please set RG_XTAL_GM[3:0]=4'b1111. Current weighting table: basic: 80uA current

Bit(s)	Name	Description
		[0]: Additional 100uA current
		[1]: Additional 120uA current
		[2]: Additional 200uA current
		[3]: Additional 480uA current
		Example:
		4'b0000: 80uA current (Neg. R=50ohm)
		4'b0001: 180uA current (Neg. R=100ohm)
		4'b0011: 300uA current (Neg. R=150ohm)
		4'b0111: 500uA current (Neg. R=200ohm)
		4'b1111: 980uA current (Neg. R=250ohm)

1001E604 AP_XTAL_40M_CON1 AP_XTAL_40M control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_CLK _SEL_R SV	RG_XT AL_TES TOD_V OD_EN	RG_XT AL_TST _EN	RG_XT AL_TST CK_EN	RG_XTAL_TST_ SEL		RG_XT AL_TST OD_EN	RG_XT AL_TST OP_EN	RG_XT AL_TES TOD_A 2DCK_ EN
Type								RW	RW	RW	RW	RW		RW	RW	RW
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	RG_CLK_SEL_RSV	Not used
7	RG_XTAL_TESTOD_VOD_EN	Overdrive open drain LDO
6	RG_XTAL_TST_EN	Overdrive open drain LDO
5	RG_XTAL_TSTCK_EN	Output clock testing mode enable
4:3	RG_XTAL_TST_SEL	Test Mux selection
2	RG_XTAL_TSTOD_EN	Enables open drain
1	RG_XTAL_TSTOP_EN	Overdrives open drain LDO
0	RG_XTAL_TESTOD_A2DCK_EN	LPF pole control register
		1'b0: 40-MHz
		1'b1 :20-MHz

1001E700 APLL2_CON4 APLL2 control register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															APLL2_TUNER_EN	APLL2_CKOUT_ON
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	APLL2_TUNER_EN	Enable APLL2 tuning function
0	APLL2_CKOUT_ON	Not used

1001E704 APLL2_CON5 APLL2 control register 5 4EA4A8C1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	APLL2_TUNER_SDM_PCW															
Type	RW															
Reset	0	1	0	0	1	1	1	0	1	0	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	APLL2_TUNER_SDM_PCW															
Type	RW															
Reset	1	0	1	0	1	0	0	0	1	1	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	APLL2_TUNER_SDM_PCW	Tune divider ratio

1001E72C MMPLL_D3_CON0 MMPLL D3 control register 0 10000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMPLL_D3_DIV2_EN	MMPLL_D3_DIV3_EN	MMPLL_D3_DIV4_EN	MMPLL_D3_DIV5_EN	MMPLL_D3_DIV6_EN	MMPLL_D3_DIV7_EN	MMPLL_D3_DIV8_EN	MMPLL_D3_DIV9_EN								
Type	RW	RW	RW	RW	RW	RW	RW	RW								
Reset	0	0	0	1	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	MMPLL_D3_DIV2_EN	Enables MMPLL_D3 divide 2
30	MMPLL_D3_DIV3_EN	Enables MMPLL_D3 divide 3
29	MMPLL_D3_DIV4_EN	Enables MMPLL_D3 divide 4
28	MMPLL_D3_DIV5_EN	Enables MMPLL_D3 divide 5
27	MMPLL_D3_DIV6_EN	Enables MMPLL_D3 divide 6
26	MMPLL_D3_DIV7_EN	Enables MMPLL_D3 divide 7
25	MMPLL_D3_DIV8_EN	Enables MMPLL_D3 divide 8
24	MMPLL_D3_DIV9_EN	Enables MMPLL_D3 divide 9

1001E730 **DRAMC_CON** **DRAMC PLL setting** 00005209

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RG_RPHYPLL_FBKSEL	RG_RPHYPLL_EN	RG_RPHYPLL_RESETB	RG_OCCCLK_FORM_MEMPLL								
Type					RW	RW	RW	RW								
Reset					0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_RPHYPLL_SDM_PCW															
Type	RW															
Reset	0	1	0	1	0	0	1	0	0	0	0	0	1	0	0	1

Bit(s)	Name	Description
27	RG_RPHYPLL_FBKSEL	RPHYPLL_FBK select
26	RG_RPHYPLL_EN	RPHYPLL enable
25	RG_RPHYPLL_RESETB	RPHYPLL resetb
24	RG_OCCCLK_FORM_MEMPLL	OCCCLK_FORM_MEMPLL select
15:0	RG_RPHYPLL_SDM_PCW	Feedback divide ratio 8-bit integer + 24-bit fractional divider ratio = PCW[31:0]/16777216

1001E734 **POR_CON1** **POR control register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AD_PM U_RST B_STAT US				AD_BG RDY_ST ATUS				AD_OT _STAT US				AD_UV LO_ST ATUS
Type				RO				RO				RO				RO
Reset				0				0				0				0

Bit(s)	Name	Description
12	AD_PMU_RSTB_STATUS	PMU debug signal
8	AD_BGRDY_STATUS	PMU debug signal
4	AD_OT_STATUS	PMU debug signal
0	AD_UVLO_STATUS	PMU debug signal

1001E74C **MCU_CLK_CTRL0** **MCUSYS clock control 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								mcu_m p2_pll1 _ck_off								mcu_m p2_ar mppll_c k_off
Type								RW								RW
Reset								0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								mcu_m p2_fca 9_clock _off			mcu_mp2_occ_ctl					
Type								RW			RW					
Reset								0			0	0	0	0	0	0

Bit(s)	Name	Description
24	mcu_mp2_pll1_ck_off	MCU mp2 pll1 clock off
16	mcu_mp2_armpll_ck_off	MCU mp2 armppll clock off
8	mcu_mp2_fca9_clock_off	MCU mp2 fca9 clock off
5:0	mcu_mp2_occ_ctl	MCU mp2 occ control

1001E750 MCU_CLK_CTRL1 MCUSYS clock control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								mcu_b us_pll1 _ck_off								mcu_b us_arm pll_ck_ off
Type								RW								RW
Reset								0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								mcu_b us_fca9 _clock_ off			mcu_bus_occ_ctl					
Type								RW			RW					
Reset								0			0	0	0	0	0	0

Bit(s)	Name	Description
24	mcu_bus_pll1_ck_off	MCU bus pll1 clock off
16	mcu_bus_armpll_ck_off	MCU bus armpll clock off
8	mcu_bus_fca9_clock_off	MCU bus fca9 clock off
5:0	mcu_bus_occ_ctl	MCU bus occ control

1001E754 MCU_MON_CLK_SEL MCUSYS monitor clock select 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																mcu_m on_ck_ sel
Type																RW
Reset																0

Bit(s)	Name	Description
0	mcu_mon_ck_sel	MCU monitor clock select

3 Peripherals

3.1 MSDC (MMC and SD Card Controller)

3.1.1 Register Definition

Module name: MSDC0 Base address: (+0x11230000)

Address	Name	Width	Register Function
11230000	<u>MSDC_CFG</u>	32	MSDC configuration register
11230004	<u>MSDC_IOCON</u>	32	MSDC IO configuration register
11230008	<u>MSDC_PS</u>	32	MSDC pin status register
1123000C	<u>MSDC_INT</u>	32	MSDC interrupt register
11230010	<u>MSDC_INTEN</u>	32	MSDC interrupt enable register
11230014	<u>MSDC_FIFOCS</u>	32	MSDC FIFO control and status register
11230018	<u>MSDC_TXDATA</u>	32	MSDC TX data port register
1123001C	<u>MSDC_RXDATA</u>	32	MSDC RX data port register
11230030	<u>SDC_CFG</u>	32	SD configuration register
11230034	<u>SDC_CMD</u>	32	SD command register. Writing to SDC_CMD register begins protocol sequence
11230038	<u>SDC_ARG</u>	32	SD argument register
1123003C	<u>SDC_STS</u>	32	SD status register
11230040	<u>SDC_RESP0</u>	32	SD response register 0
11230044	<u>SDC_RESP1</u>	32	SD response register 1
11230048	<u>SDC_RESP2</u>	32	SD response register 2
1123004C	<u>SDC_RESP3</u>	32	SD response register 3
11230050	<u>SDC_BLK_NUM</u>	32	SD block number register
11230054	<u>SDC_VOL_CHG</u>	32	SD voltage change wait time register
11230058	<u>SDC_CSTS</u>	32	SD card status register
1123005C	<u>SDC_CSTS_EN</u>	32	SD card status enable register
11230060	<u>SDC_DATCRC_STS</u>	32	SD card data CRC status register
11230064	<u>SDC_ADV_CFG0</u>	32	SDC advanced configuration 0
11230068	<u>MSDC_NEW_RX_CFG</u>	32	MSDC new RX path configuration
11230070	<u>EMMC_CFG0</u>	32	eMMC configuration register 0
11230074	<u>EMMC_CFG1</u>	32	eMMC configuration register 1
11230078	<u>EMMC_STS</u>	32	eMMC status register
1123007C	<u>EMMC_IOCON</u>	32	eMMC IO control register
11230080	<u>SD_ACMD_RESP</u>	32	SD ACMD response register
11230084	<u>SD_ACMD19_TRG</u>	32	SD ACMD19 target register
11230088	<u>SD_ACMD19_STS</u>	32	SD ACMD19 status register
1123008C	<u>DMA_SA_HIGH4BIT</u>	32	DMA start address register of the high 4 bits
11230090	<u>DMA_SA</u>	32	DMA start address register
11230094	<u>DMA_CA</u>	32	DMA current address register
11230098	<u>DMA_CTRL</u>	32	DMA control register
1123009C	<u>DMA_CFG</u>	32	DMA configuration register
112300A0	<u>SW_DBG_SEL</u>	32	MSDC software debug selection register
112300A4	<u>SW_DBG_OUT</u>	32	MSDC software debug output register
112300A8	<u>DMA_LENGTH</u>	32	DMA length register
112300B0	<u>PATCH_BIT0</u>	32	MSDC patch bit register 0

Address	Name	Width	Register Function
112300B4	<u>PATCH_BIT1</u>	32	MSDC patch bit register 1
112300B8	<u>PATCH_BIT2</u>	32	MSDC patch bit register 2
112300F0	<u>PAD_TUNE0</u>	32	MSDC pad tuning register 0
11230110	<u>HW_DBG_SEL</u>	32	MSDC hardware debug selection register
11230114	<u>MAIN_VER</u>	32	MSDC main version register
11230118	<u>ECO_VER</u>	32	MSDC ECO version register
11230120	<u>DMA_CFG_TD</u>	32	MSDC CQDMA descriptor configuration register
11230204	<u>SW_CMDQ_CFG0</u>	32	SW CMDQ configuration register 0
11230208	<u>EMMC50_CFG0</u>	32	eMMC50 configuration register 0
1123020C	<u>EMMC50_CFG1</u>	32	eMMC50 configuration register 1
1123021C	<u>EMMC50_CFG2</u>	32	AHB2AXI wrapper control register
11230220	<u>EMMC50_CFG3</u>	32	AHB2AXI wrapper control register
11230224	<u>EMMC50_CFG4</u>	32	AHB2AXI wrapper control register
11230228	<u>SDC_FIFO_CFG</u>	32	1KB FIFO configuration
112307FC	<u>CQHCI_SETTING</u>	32	eMMC51 CQHCI features
11230800	<u>CQVER</u>	32	eMMC51 CQHCI features
11230804	<u>CQCAP</u>	32	eMMC51 CQHCI features
11230808	<u>CQCFG</u>	32	eMMC51 CQHCI features
1123080C	<u>CQCTL</u>	32	eMMC51 CQHCI features
11230810	<u>CQIS</u>	32	eMMC51 CQHCI features
11230814	<u>CQISTE</u>	32	eMMC51 CQHCI features
11230818	<u>CQISGE</u>	32	eMMC51 CQHCI features
1123081C	<u>CQIC</u>	32	eMMC51 CQHCI features
11230820	<u>CQTDLBA</u>	32	eMMC51 CQHCI features
11230824	<u>CQTDLBAU</u>	32	eMMC51 CQHCI features
11230828	<u>CQTDBR</u>	32	eMMC51 CQHCI features
1123082C	<u>CQTCN</u>	32	eMMC51 CQHCI features
11230830	<u>CQDQS</u>	32	eMMC51 CQHCI features
11230834	<u>CQDPT</u>	32	eMMC51 CQHCI features
11230838	<u>CQTCLR</u>	32	eMMC51 CQHCI features
1123083C	<u>CQTDPE</u>	32	eMMC51 CQHCI features
11230840	<u>CQSSC1</u>	32	eMMC51 CQHCI features
11230844	<u>CQSSC2</u>	32	eMMC51 CQHCI features
11230848	<u>CQCRDCT</u>	32	eMMC51 CQHCI features
11230850	<u>CQRMEM</u>	32	eMMC51 CQHCI features
11230854	<u>CQTERRI</u>	32	eMMC51 CQHCI features
11230858	<u>CQCRI</u>	32	eMMC51 CQHCI features
1123085C	<u>CQCRA</u>	32	eMMC51 CQHCI features

11230000 **MSDC_CFG** **MSDC configuration register** **02400099**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			BW_SEL				SCLK_STOP_SEL	START_BIT		HS400_CK_MODE	CARD_CK_MODE		CARD_CK_DIV			
Type			RW				RW	RW		RW	RW		RW			
Reset			0				1	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CARD_CK_DIV								CARD_CK_STABLE	BV_1P8_PASS	BV_1P8_START_DET	Reserved0	PIO_MODE	RST	CARD_CK_PWDN	MSDC
Type	RW								RU	RU	RW	RW	RW	A0	RW	RW
Reset	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1

Bit(s)	Name	Description
29	BW_SEL	Saves power for low throughput requirement 1'b0: Memory provides different throughputs for different MSDC speed modes. 1'b1: Memory provides the highest throughput for all speed modes.
25	SCLK_STOP_SEL	In DDR mode, decides whether to check SCLK phase or not when SCLK is stopped 1'b0: Do not check SCLK phase 1'b1: Check SCLK phase
24:23	START_BIT	Selects read data start bit in DDR mode 2'b00: Rising edge 2'b01: Falling edge 2'b10: Rising & falling edge 2'b11: Rising falling edge
22	HS400_CK_MODE	Selects HS400 clock mode 1'b0: HS400 source clock is 800 MHz. 1'b1: HS400 source clock is 400 MHz.
21:20	CARD_CK_MODE	Selects the clock mode of host controller 2'b00: Use clock divider output divided by msdc_src_ck as msdc_ck. Bit [19] to bit [8] should be programmed. 2'b01: Use msdc_src_ck as msdc_ck. Bit [19] to bit [8] are ignored. 2'b10: DDR mode. Also use clock divider output divided by msdc_src_ck as msdc_ck. Bit [19] to bit [8] should be programmed. 2'b11: HS400 mode. Also use clock divider output or msdc_src_ck as msdc_ck. When HS400_CK_MODE is set to 0, bit [19] to bit [8] should be programmed. When HS400_CK_MODE is set to 1, bit [19] to bit [8] are ignored.

Bit(s)	Name	Description
19:8	CARD_CK_DIV	MMC/SD card clock divider The register field controls clock frequency of serial clock on MMC/SD bus $12'h0: msdc\_ck = msdc\_src\_ck * 1/2$ $others: msdc\_ck = msdc\_src\_ck * 1/(4 * value)$
7	CARD_CK_STABLE	Whether MMC/SD card clock is stable or not After programming CARD_CK_MODE or CARD_CK_DIV, this bit will immediately become 0 and return to 1 if being stable. Poll this register to ensure safety control of MSDC. $1'b0$: Clock output is not stable. $1'b1$: Clock output is stable.
6	BV_1P8_PASS	For SD, MSDC bus voltage 1.8V detection status SW should check this bit after BUS_VOL_18V_START_DET is changed from 1 to 0. $1'b0$: Error occurs during voltage detection. $1'b1$: No error occurs during voltage detection.
5	BV_1P8_START_DET	For SD, MSDC bus voltage 1.8V detection sequence start event SW writes this bit to 1 to trigger 1.8V detection sequence event. HW will clear this bit to 0 after the detection has finished. The passed or failed status is stored in bit [6] BUS_VOL_18V_PASS.
4	Reserved0	Please don't modify reserved bit field in order to avoid affecting normal function. Please keep it as default value for MSDC operation.
3	PIO_MODE	MMC/SD PIO mode PIO mode selection. It is in PIO mode by default. $1'b0$: DMA mode $1'b1$: PIO mode
2	RST	Software reset Writing 1 to this register will cause internal synchronous reset of MMC/SD controller, and it will not reset register settings and DMA controller. The reset sequence will be done when this bit becomes 0. SW should wait for this bit to return to 0 after writing 1. $1'b0$: MMC/SD controller is not in reset state. $1'b1$: MMC/SD controller is in reset state.
1	CARD_CK_PWDN	MSDC bus clock power down mode This bit controls the card clock power down mode. $1'b0$: Clock will be gated to 0 if no command or data is transmitted.

Bit(s)	Name	Description
0	MSDC	1'b1: Clock will be running freely even if no command or data is transmitted. (The clock may still be stopped when MSDC write data are not enough or there is no space for the next read data) Selects MMC/SD mode The default value configures the controller as the host of MMC/SD memory card. 1'b0: Disable MSDC working 1'b1: Configure the controller as the host of MMC/SD memory card

11230004	MSDC IOCON			MSDC IO configuration register												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name									R_D7_S	R_D6_S	R_D5_S	R_D4_S	R_D3_S	R_D2_S	R_D1_S	R_D0_S	
Type									MPL	MPL	MPL	MPL	MPL	MPL	MPL	SMPL	
Reset									0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name			W_D3	W_D2	W_D1	W_D0	W_D_S	W_D_S			R_D_S	DDR50	D_DLY	R_D_S	R_SMP	SDR10	
Type			SMPL	SMPL	SMPL	SMPL	MPL_S	MPL			MPL_S	DLY_S	INE_SE	MPL	L	4_CLK_SEL	
Reset			0	0	0	0	0	0			0	0	0	0	0	0	

Bit(s)	Name	Description
23	R_D7_SMPL	Selects read data 7 sample This bit will only be valid when bit5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
22	R_D6_SMPL	Selects read data 6 sample This bit will only be valid when bit5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
21	R_D5_SMPL	Selects read data 5 sample This bit will only be valid when bit5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
20	R_D4_SMPL	Selects read data 4 sample This bit will only be valid when bit5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
19	R_D3_SMPL	Selects read data 3 sample This bit will only be valid when bit5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
18	R_D2_SMPL	Selects read data 2 sample This bit will only be valid when bit5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge

Bit(s)	Name	Description
17	R_D1_SMPL	Selects read data 1 sample This bit will only be valid when bit5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
16	R_D0_SMPL	Selects read data 0 sample This bit will only be valid when bit5 is on. 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
13	W_D3_SMPL	Selects SDIO interrupt sample This bit will only be valid when bit9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
12	W_D2_SMPL	Selects SDIO interrupt sample This bit will only be valid when bit9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
11	W_D1_SMPL	Selects SDIO interrupt sample This bit will only be valid when bit9 is on. 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
10	W_D0_SMPL	Selects CRC status and SDIO interrupt sample This bit will only be valid when bit9 is on. 1'b0: Sample CRC status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC status and SDIO interrupt by external bus clock falling edge
9	W_D_SMPL_SEL	Selects data line rising/falling latch fine-tuning in write transaction 1'b0: All data lines share one value indicated by MSDC_IOCON.W_D_SMPL. 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.W_D0_SMPL Data line 1: MSDC_IOCON.W_D1_SMPL Data line 2: MSDC_IOCON.W_D2_SMPL Data line 3: MSDC_IOCON.W_D3_SMPL

Bit(s)	Name	Description
8	W_D_SMPL	Selects CRC status and SDIO interrupt sample 1'b0: Sample CRC status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC status and SDIO interrupt by external bus clock falling edge
5	R_D_SMPL_SEL	Selects data line rising/falling latch fine-tuning in read transaction 1'b0: All data lines share one value indicated by MSDC_IOCON.R_D_SMPL. 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.R_D0_SMPL Data line 1: MSDC_IOCON.R_D1_SMPL Data line 2: MSDC_IOCON.R_D2_SMPL Data line 3: MSDC_IOCON.R_D3_SMPL Data line 4: MSDC_IOCON.R_D4_SMPL Data line 5: MSDC_IOCON.R_D5_SMPL Data line 6: MSDC_IOCON.R_D6_SMPL Data line 7: MSDC_IOCON.R_D7_SMPL
4	DDR50_DLY_SEL	Selects DDR50 output clock delay 1'b0: Use default clock output 1'b1: Delay 1T msdc_src_ck for clock output
3	D_DLYLINE_SEL	Selects data line delay line fine-tuning 1'b0: All data lines share one delay selection value indicated by PAD_TUNE.PAD_DAT_RD_RXDLY. 1'b1: Each data line has its own delay selection value indicated by Data line 0: DAT_RD_DLY0.DAT0_RD_DLY Data line 1: DAT_RD_DLY0.DAT1_RD_DLY Data line 2: DAT_RD_DLY0.DAT2_RD_DLY Data line 3: DAT_RD_DLY0.DAT3_RD_DLY Data line 4: DAT_RD_DLY1.DAT4_RD_DLY Data line 5: DAT_RD_DLY1.DAT5_RD_DLY Data line 6: DAT_RD_DLY1.DAT6_RD_DLY Data line 7: DAT_RD_DLY1.DAT7_RD_DLY
2	R_D_SMPL	Selects read data sample 1'b0: Sample read data by external bus clock rising edge

Bit(s)	Name	Description
1	R_SMPL	1'b1: Sample read data by external bus clock falling edge Selects command response sample 1'b0: Sample response by external bus clock rising edge 1'b1: Sample response by external bus clock falling edge
0	SDR104_CLK_SEL	SDR104 SCLK output clock control This bit is only used when MSDC_CFG[17:16] CARD_CK_MODE is 2'b01. 1'b0: Bus clock output equals inverted msdc_src_ck 1'b1: Bus clock output equals msdc_src_ck

11230008	MSDC_PS				MSDC pin status register											81FF0002		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	Reserved3							CMD	DAT									
Type	RU							RU	RU									
Reset	1							1	1	1	1	1	1	1	1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	Reserved2														Reserved1	Reserved0		
Type	RW														RU	RW		
Reset	0	0	0	0											1	0		

Bit(s)	Name	Description
31	Reserved3	Please don't modify reserved bit field in order to avoid affecting normal function. Please keep it as default value for MSDC operation.
24	CMD	Command line status This bit reflects the command line value of MSDC bus.
23:16	DAT	Data line status This bit reflects the data line value of MSDC bus (8-bit).
15:12	Reserved2	Please don't modify reserved bit field in order to avoid affecting normal function. Please keep it as default value for MSDC operation.
1	Reserved1	Please don't modify reserved bit field in order to avoid affecting normal function. Please keep it as default value for MSDC operation.
0	Reserved0	Please don't modify reserved bit field in order to avoid affecting normal function. Please keep it as default value for MSDC operation.

1123000C MSDC_INT MSDC interrupt register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved0			CQHCI_IRQ					AXI_RESP_ERR				DMA_PROTECT	GPD_CS_ERR	BD_CS_ERR	AUTOCMD19_DONE
Type	RO			W1C					W1C				W1C	W1C	W1C	W1C
Reset	0	0	0	0					0				0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SD_DATA_CRCERR	SD_DATTO	DMA_XFER_DONE	SD_XFER_COMPLETE	SD_CSTS	SD_RESP_CRCERR	SD_CMDTO	SD_CMDRDY	SD_SDI_OIRQ	DMA_QEMPTY	SD_AU_TOCD_RESP_CRCERR	SD_AU_TOCD_CMDTO	SD_AU_TOCD_CMDRDY		MSDC_CDSC	MMC_IRQ
Type	W1C	W1C	W1C	W1C	RU	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C		W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Name	Description
31:29	Reserved0	Command queuing interrupt
28	CQHCI_IRQ	Command queuing interrupt
23	AXI_RESP_ERR	AXI BUS response error status
19	DMA_PROTECT	There is write operation to DMA start address, length, start bit or last buffer bit.
18	GPD_CS_ERR	Detects GPD checksum error
17	BD_CS_ERR	Detects BD checksum error
16	AUTOCMD19_DONE	SD auto command 19 status register When auto-command 19 is enabled, HW will clear this register to 0. As the tuning sequence is finished (32 times), this register will be set to 1 by HW. SW should check the AUTOCMD_STS0 and SUTOCMD_STS1 only when this bit is on.
15	SD_DATA_CRCERR	SD data CRC error interrupt Indicates that MMC/SD controller detects a CRC error after reading a block of data from the DAT line or MMC/SD signals a CRC error after writing a block of data to the DAT line. 1'b0: Otherwise 1'b1: MMC/SD controller detects a CRC error after reading a block of data from the DAT line or MMC/SD signals a CRC error after writing a block of data to the DAT line.
14	SD_DATTO	SD data timeout interrupt Indicates that MMC/SD controller detects a timeout condition while waiting for data token on the DAT line. This bit is for both data read and data write. For SD data read, timeout will occur when the read data is not presented.

Bit(s)	Name	Description
		For SD data write, timeout will occur when the write data CRC status is not presented if PATCH_BIT[30] DETECT_WR_CRC_TIMEOUT = 1
		1'b0: Otherwise
		1'b1: MMC/SD controller detects a timeout condition while waiting for data token on the DAT line.
13	DMA_XFER_DONE	DMA transfer done interrupt The register bit indicates the status of data block transfer. 1'b0: Otherwise 1'b1: A data block is successfully transferred.
12	SD_XFER_COMPLETE	SD data transfer complete interrupt This bit indicates the transaction (which contains data) has completed. When performing tuning procedure (Execute Tuning is set to 1), SD_XFER_COMPLETE is not set to 1.
11	SD_CSTS	SD CSTA update interrupt The register bit indicates if any bit in the register SDC_CSTS is active, the register bit will be set to 1. SW should clear the SDC_CSTS and this bit will be de-asserted automatically. 1'b0: No SD memory card interrupt 1'b1: SD memory card interrupt exists.
10	SD_RESP_CRCERR	SD command CRC error interrupt Indicates that MMC/SD controller has detected a CRC error after reading a response from the CMD line. 1'b0: Otherwise 1'b1: MMC/SD controller detects a CRC error after reading a response from the CMD line.
9	SD_CMDTO	SD command timeout interrupt Indicates that MMC/SD controller has detected a timeout condition while waiting for a response on the CMD line. 1'b0: Otherwise 1'b1: MMC/SD controller detects a timeout condition while waiting for a response on the CMD line.
8	SD_CMDRDY	SD command ready interrupt For the command without response, the register bit will be 1 once the command is completed on MMC/SD bus. For response without busy, the register bit will be 1 whenever the command is issued onto MMC/SD bus and its corresponding response is received without CRC error.

Bit(s)	Name	Description
		For response with "busy" from DAT0, the register bit will be 1 whenever the command is issued onto MMC/SD bus and its corresponding response is received without CRC error and the state of DAT0 is changed from busy to idle.
		1'b0: Otherwise
		1'b1: Command is finished successfully without a CRC error.
7	SD_SDIOIRQ	SD SDIO interrupt This bit indicates the interrupt is sensed in the SDIO bus. 1'b0: No interrupt on SDIO bus 1'b1: Interrupt on SDIO bus
6	DMA_Q_EMPTY	DMA queue empty interrupt This bit indicates the current DMA queue is empty. Only for Descriptor mode and Enhance mode.
5	SD_AUTOCMD_RESP_CRCERR	SD auto command CRC error interrupt This bit is set when detecting a CRC error in the Auto command response.
4	SD_AUTOCMD_CMDTO	SD auto command timeout interrupt This bit will be set if no response is returned within the specified cycles (64T in spec) from the end bit of auto command.
3	SD_AUTOCMD_CMDRDY	SD auto command ready interrupt This bit is set if auto command is executed without CRC error or time out.
1	MSDC_CDSC	MSDC card detection status change interrupt The register bit indicates if any interrupt for memory card insertion/removal exists. Whenever memory card is inserted or removed and card detection circuit is enabled, i.e. when register bit CDEN in the register MSDC_PS is set to 1, the register bit will be set to 1. It will be reset when the register is read. 1'b0: Otherwise 1'b1: Card is inserted or removed.
0	MMC_IRQ	eMMC card interrupt 1'b0: Otherwise 1'b1: eMMC card interrupt event occurs.

11230010	MSDC_INTEN				MSDC interrupt enable register										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				EN_CQHCI_IRQ					EN_AXI_RESP_ERR				EN_DMA_PROTECT	EN_GPD_CS_ERR	EN_BD_CS_ERR	EN_AUTOCMD19_DONE
Type				RW					RW				RW	RW	RW	RW
Reset				0					0				0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SD_DATA_CRCERR	EN_SD_DATA_CRCERR	EN_SD_DMA_XFER_DONE	EN_SD_XFER_COMPLETE	EN_SD_CSTAKE	EN_SD_RESP_CRCERR	EN_SD_CMDT_O	EN_SD_CMDRDY	EN_SD_SDIORQ	EN_DMA_AQ_EMPTY	EN_SD_AUTO_CMD_RSP_CERR	EN_SD_AUTO_CMD_RDY	EN_AUTOCMD_RDY		EN_MSDC_CDSC	EN_MC_IRQ
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Name	Description
28	EN_CQHCI_IRQ	Enables command queuing interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt
23	EN_AXI_RESP_ERR	Enables AXI BUS response error status interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt
19	EN_DMA_PROTECT	Enables DMA protection interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt
18	EN_GPD_CS_ERR	Enables GPD checksum error interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt
17	EN_BD_CS_ERR	Enables BD checksum error interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt
16	EN_AUTOCMD19_DONE	Enables auto-command 19 complete interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt
15	EN_SD_DATA_CRCERR	Enables SD data CRC error interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt

Bit(s)	Name	Description
14	EN_SD_DATTO	Enables SD data timeout interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt
13	EN_SD_DMA_XFER_DONE	Enables DMA transfer done interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt
12	EN_SD_XFER_COMPLETE	Enables SD data transfer complete interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt
11	EN_SD_CSTA	Enables SD CSTA update interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt
10	EN_SD_RESP_CRCERR	Enables SD command CRC error interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt
9	EN_SD_CMDTO	Enables SD command timeout interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt
8	EN_SD_CMDRDY	Enables SD command ready interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt
7	EN_SD_SDIOIRQ	Enables SD SDIO interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt
6	EN_DMA_Q_EMPTY	Enables DMA queue empty interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt
5	EN_SD_AUTOCMD_RESP_CRCERR	Enables SD auto command CRC error interrupt 1'b0: Disable interrupt 1'b1: Enable interrupt
4	EN_SD_AUTOCMD_CMDTO	Enables SD auto command timeout interrupt 1'b0: Disable interrupt

Bit(s)	Name	Description
3	EN_AUTOCMD_CMDDRDY	1'b1: Enable interrupt
		Enables SD auto command ready interrupt
		1'b0: Disable interrupt
1	EN_MSDC_CDSC	1'b1: Enable interrupt
		Enables MSDC card detection status change interrupt
		1'b0: Disable interrupt
0	EN_MMC_IRQ	1'b1: Enable interrupt
		Enables MMC card interrupt
		1'b0: Disable interrupt
		1'b1: Enable interrupt

11230014 MSDC_FIFOCS MSDC FIFO control and status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFOCLR								TXFIFOCNT							
Type	A0								RU							
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXFIFOCNT							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	FIFOCLR	Clears embedded FIFO Writing 1 to this bit will clear FIFO. It will become 0 when FIFO is cleared. SW needs to check this bit to make sure clearing the FIFO sequence is done. This bit can be used when the data read/write sequence contains an error, and clearing HW FIFO is needed.
23:16	TXFIFOCNT	TX FIFO count for MSDC write 8'd0: No data in FIFO 8'd1: 1-byte data in FIFO 8'd2: 2-byte data in FIFO 8'd3~8'd130: And so on 8'd131: Maximum 131-byte data in FIFO Others: Reserved
7:0	RXFIFOCNT	RX FIFO count for MSDC read 8'd0: No data in FIFO 8'd1: 1-byte data in FIFO 8'd2: 2-byte data in FIFO 8'd3~8'd130: And so on 8'd131: Maximum 131-byte data in FIFO Others: Reserved

11230018 **MSDC_TXDATA** **MSDC TX data port register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIO_TXDATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIO_TXDATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PIO_TXDATA	PIO mode TXDATA port This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

1123001C **MSDC_RXDATA** **MSDC RX data port register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIO_RXDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIO_RXDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PIO_RXDATA	PIO mode RXDATA port This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

11230030 SDC_CFG SD configuration register 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DTC								WAKEUP_INT	WAKEUP_PULSE_EN	INT_AT_BLOCK_GAP	SDIO_INTERRUPT_EN	SDIO		BUSWIDTH	
Type	RW								W1C	RW	RW	RW	RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		WRDTC													WAKEUP_INTERRUPT_EN	WAKEUP_SDIO_INTERRUPT_EN
Type		RW													RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DTC	Data timeout counter The period from the end of the initial host read command or the last read data block in a multiple block read operation to the start bit of the next read data block requires at least two serial clock cycles. The counter is used to extend the period (Read Data Access Time). Unit: 1048576 serial clocks 8'b00000000: Extend 1048576 more serial clock cycles 8'b00000001: Extend 1048576*2 more serial clock cycles 8'b00000010: Extend 1048576*3 more serial clock cycles 8'b11111111: Extend 1048576*256 more serial clock cycles
23	WAKEUP_INT	SDIO wakeup interrupt occurs. 1'b0: No SDIO wakeup interrupt occurs. 1'b1: SDIO wakeup interrupt occurs.
22	WAKEUP_PULSE_EN	SDIO wakeup interrupt level or pulse enable bit 1'b0: Enable SDIO wakeup interrupt level 1'b1: Enable SDIO wakeup interrupt pulse
21	INT_AT_BLOCK_GAP	Interrupt at block gap This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting this bit to 1 enables interrupt detection at the block gap for a multiple block transfer. Setting this bit to 0 disables interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the Host Driver detects an SD card insertion, it should set this bit according to the CCCR of the SDIO card. 1'b0: Disable interrupt detection at block gap 1'b1: Enable interrupt detection at block gap
20	SDIO_INTERRUPT_EN	Enables SDIO interrupt detection

Bit(s)	Name	Description
		This bit informs the SD controller to sense the SDIO interrupt.
		1'b0: Disable SDIO interrupt detection
		1'b1: Enable SDIO interrupt detection if the SDIO bit is also on
19	SDIO	SDIO mode enable bit
		This bit enables the support to sense the SDIO interrupt and disables the R4 response CRC check for SDIO card.
		1'b0: Disable SDIO mode
		1'b1: Enable SDIO mode
17:16	BUSWIDTH	Configures bus width
		This field defines MMC/SD bus width.
		2'b00: 1-bit mode
		2'b01: 4-bit mode
		2'b10: 8-bit mode
		2'b11: Reserved
14:2	WRDTOC	Data timeout counter
		Timeout counter for programming. The counter is used to extend the period (Write Data Access Time). Unit: 1048576 serial clocks.
		13'b00000000000000: Extend 1048576 more serial clock cycles
		13'b00000000000001: Extend 1048576*2 more serial clock cycles
		13'b00000000000010: Extend 1048576*3 more serial clock cycles
		13'b11111111111111: Extend 1048576*8192 more serial clock cycles
1	WAKEUP_INS_EN	Card status change wakeup event enable bit
		1'b0: Disable wakeup event for card status change
		1'b1: Enable wakeup event for card status change
0	WAKEUP_SDIOINT_EN	SDIO card interrupt wakeup event enable bit
		1'b0: Disable wakeup event for SDIO card interrupt
		1'b1: Enable wakeup event for SDIO card interrupt

11230034

SDC_CMD

SD command register. Writing to SDC_CMD
register begins protocol sequence

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		VOL_S WTH	AUTO_CMD		LEN											
Type		RW	RW		RW											
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GO_IR Q	STOP	RW	DTYPE			RSPTYP			BREAK	CMD					
Type	RW	RW	RW	RW			RW			RW	RW					
Reset	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	VOL_SWTH	For SD, voltage switch command 1'b0: Disable voltage switch detection 1'b1: Enable voltage switch detection
29:28	AUTO_CMD	Enables auto command This field determines the use of auto command functions. This function can be used in all modes including PIO/Basic DMA/Descriptor DMA/Enhanced Mode. There are two methods to stop multiple-block read and write operation. (1) Enable Auto CMD12 Multiple-block read and write commands for memory require CMD12 to stop the operation. When ACMD-12 is used, MSDC will issue CMD12 automatically when the last block transfer is completed. Auto CMD12 error is indicated to the MSDC_INT register. The host driver should not set this bit if the command does not require CMD12. In particular, secure commands defined in the Part 3 File Security specification do not require CMD12. (2) Enable Auto CMD23 When ACMD-23 is used, MSDC will issue a CMD23 automatically before issuing a command specified in the CMD field. The host controller Version 3.00 and later versions should support this function. By writing the command register, MSDC will first issue a CMD23 then a command specified by the CMD field in SDC_CMD register. If response errors of CMD23 are detected, the second command will not be issued. A CMD23 error is indicated in the MSDC_INT register. The 32-bit block count value for CMD23 is set to SDC_BLOCK_NUM register. (3) Re-tuning CMD19 not used 2'b00: Disable Auto Command 2'b01: Enable Auto CMD12 2'b10: Enable Auto CMD23

Bit(s)	Name	Description
		2'b11: Enable re-tuning CMD19
27:16	LEN	Length The register field defines the length of one block in unit of byte in a data transaction of block mode or the data length in unit of byte in data transaction of byte mode. The maximal value of block length is 2048 bytes. 12'b000000000000: Reserved 12'b000000000001: Block length is 1 byte. 12'b000000000010: Block length is 2 bytes. 12'b000000000011~12'b011111111110: And so on. 12'b011111111111: Block length is 2047 bytes. 12'b100000000000: Block length is 2048 bytes.
15	GO_IRQ	GO_IRQ command The register bit indicates if the command is GO_IRQ_STATE (CMD40) which is used only for MMC protocol. If the command is GO_IRQ_STATE, the period between command token and response token will not be limited. 1'b0: The command is not GO_IRQ_STATE. 1'b1: The command is GO_IRQ_STATE.
14	STOP	Stop command The register bit indicates if the command is a stop transmission command. It should be set to 1 when CMD12 (MMC/SD) or CMD52 with I/O abort (SDIO) is to be issued. 1'b0: The command is not a stop transmission command. 1'b1: The command is a stop transmission command.
13	RW	Selects command read/write The register bit defines the command as a read command or write command. When the register bit is valid, the command will cause a transaction with data token. 1'b0: The command is a read command. 1'b1: The command is a write command.
12:11	DTYPE	Selects data block The register field defines data token type for the command. 2'b00: No data token for the command 2'b01: Single block transaction (only available in block mode) 2'b10: Multiple block transaction (only available in block mode)

Bit(s)	Name	Description
9:7	RSPTYP	2'b11: Stream operation. It should only be used in MMC protocol (only available in block mode). Command response type 3'b000: This command has no response. 3'b001: The command has R1/R5/R6/R7 response. The response token is 48-bit with CRC check (for MMC/SD/SDIO) (not including SDIO abort command). 3'b010: The command has R2 response. The response token is 136-bit (for MMC/SD). 3'b011: The command has R3 response. The response token is 48-bit response, no CRC check (for MMC/SD). 3'b100: The command has R4 response. The response token is 48-bit without CRC check (for SDIO). The response token is 48-bit with CRC check (for MMC). 3'b111: The command has R1b response. The response token is 48-bit (for MMC/SD/SDIO).
6	BREAK	Aborts a pending MMC GO_IRQ command It is only valid for a pending GO_IRQ_MODE command waiting for MMC interrupt response. 1'b0: Not a break command 1'b1: Break a pending MMC GO_IRQ_MODE command in the controller
5:0	CMD	SD memory card command

11230038	SDC_ARG				SD argument register												00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	ARG																			
Type	RW																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	ARG																			
Type	RW																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:0	ARG	Memory card controller argument register

1123003C SDC_STS SD status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved											CMD_TIMEOUT_TYPE		DATA_TIMEOUT_TYPE		CMD_WR_BUSY
Type	RU											RU		RU		W1C
Reset	0											0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														START_BIT_CRCERR	CMDDBUSY	SDCBUSY
Type														RU	RU	RU
Reset														0	0	0

Bit(s)	Name	Description
31	Reserved	Reserved
20:19	CMD_TIMEOUT_TYPE	MSDC CMD timeout type For debugging, host misses the start bit of r1b cmd response or data 0 busy is too long. 2'b00: Reserved 2'b01: Data 0 busy timeout 2'b10: Response start bit timeout 2'b11: Reserved
18:17	DATA_TIMEOUT_TYPE	Data timeout error type For Debugging and Error Handling. 2'b00: Read data timeout 2'b01: Write CRC status timeout 2'b10: Write programming timeout 2'b11: Reserved
16	CMD_WR_BUSY	Reflects whether MMC/SD controller is busy or not when PATCH_BIT0.DIS_REFLECT_CMDWR_WHEN_BSY is 0 1'b0: MMC/SD controller is not busy 1'b1: MMC/SD controller is busy
2	START_BIT_CRCERR	Status to reflect whether the host misses start bit or not 1'b0: Start bit check pass 1'b1: Start bit missing error
1	CMDDBUSY	SD command line busy status SW should always read this bit to make sure the command line is not busy before sending the next command.

Bit(s)	Name	Description
		If the command is R1B or data read/write command, SW should check SDCBUSY bit too.
		Note: When Auto command 12 is enabled, this bit will be asserted immediately after SDC_CMD is written and de-asserted after auto-command 12 is finished.
		1'b0: No transmission is ongoing for CMD line on SD bus.
		1'b1: There is ongoing transmission for CMD line on SD bus.
0	SDCBUSY	SD controller busy status
		1'b0: SD controller is idle.
		1'b1: SD controller is busy.

11230040	SDC_RESP0			SD response register 0												00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	RESP0																	
Type	RU																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	RESP0																	
Type	RU																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:0	RESP0	Memory card controller response register 0

11230044	<u>SDC RESP1</u>			SD response register 1												00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	RESP1																	
Type	RU																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	RESP1																	
Type	RU																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:0	RESP1	Memory card controller response register 1

11230048 **SDC_RESP2** **SD response register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESP2	Memory card controller response register 2

1123004C **SDC_RESP3** **SD response register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESP3	Memory card controller response register 3

11230050 SDC_BLK_NUM SD block number register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BLOCK_NUMBER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BLOCK_NUMBER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	BLOCK_NUMBER	Memory card controller block number This field indicates the block number of data transaction. 32'd0: Reserved 32'd1: 1 data block 32'd2: 2 data blocks 32'd3: 3 data blocks 32'hffffff: 4GB-1 data blocks

11230054 SDC_VOL_CHG SD voltage change wait time register 00000145

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VOL_CHG_WAIT_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1

Bit(s)	Name	Description
15:0	VOL_CHG_WAIT_CNT	Defines SD voltage change check wait time Wait time is clock frequency multiplied by VOL_WAIT_TIME.

11230058 **SDC_CSTS** **SD card status register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSTS	CSTS The card status field in the response R1 or R1b field. Each bit can be cleared by writing 1 to it.

1123005C **SDC_CSTS_EN** **SD card status enable register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CSTS_EN	CSTS_EN This register controls which bit of the CSTA will generate the MSDC_INT.SDCSTA.

11230060 **SDC_DATCRC_STS** SD card data CRC status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT_CRCSTS_NEG								DAT_CRCSTS_POS							
Type	RU								RU							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	DAT_CRCSTS_NEG	This register reflects the negative edge CRC status of data line[7:0] in DDR mode. The positive edge CRC status is shown in DAT_CRC_STS[7:0]. This register is only for MSDC read. 1'b0: No CRC error 1'b1: CRC error
7:0	DAT_CRCSTS_POS	This register reflects the CRC status of data line[7:0]. This register is only for MSDC read. 1'b0: No CRC error 1'b1: CRC error

11230064	SDC_ADV_CFG0			SDC advanced configuration 0								3808E000				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												SDC_RX_ENHANCE_EN	SDIO_IRQ_ENHANCE_EN			
Type												RW	RW			
Reset												0	1			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMD_ENDBIT_CHECK	CMD_INDEX_CHECK	CMD_RESP_ENDBIT	CMD_RESP_INDEX						CMD_RESP_CRC						
Type	RW	RW	RU	RU						RU						
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20	SDC_RX_ENHANCE_EN	Enables enhance RX check for TA removal and gap IRQ check 1'b0: Normal RX path 1'b1: Enhance RX path
19	SDIO_IRQ_ENHANCE_EN	Enables enhance SDIO IRQ check 1'b0: Normal SDIO IRQ check 1'b1: Enhance SDIO IRQ check
15	CMD_ENDBIT_CHECK	Decides whether hardware checks end-bit in response or not 1'b0: Software checks end-bit. 1'b1: Hardware checks end-bit.
14	CMD_INDEX_CHECK	Decides whether hardware checks cmd-index in response or not 1'b0: Software checks index. 1'b1: Hardware checks index.
13	CMD_RESP_ENDBIT	CMD end-bit in cmd response
12:7	CMD_RESP_INDEX	CMD index in cmd response
6:0	CMD_RESP_CRC	CMD CRC in cmd response

11230068 **MSDC_NEW_RX_CFG** **MSDC new RX path configuration** 00000036

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										MSDC_NEW_RX_CMD_FIFOWATER			MSDC_NEW_RX_DATA_FIFOWATER			MSDC_NEW_RX_PATH_SEL
Type										RW			RW			RW
Reset										0	1	1	0	1	1	0

Bit(s)	Name	Description
6:4	MSDC_NEW_RX_CMD_FIFOWATER	Sets new RX cmd FIFO pop water
3:1	MSDC_NEW_RX_DATA_FIFOWATER	Sets new RX dat FIFO pop water
0	MSDC_NEW_RX_PATH_SEL	Selects MSDC new RX path 1'b0: Deselect MSDC new RX path 1'b1: Select MSDC new RX path

11230070 EMMC_CFG0 eMMC configuration register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BOOT_SUPPORT	BOOT_WAIT_DELAY											BOOT_ACK_CHK_DIS	BOOT_MODE	BOOT_STOP	BOOT_START
Type	RW	RW											RW	RW	WO	WO
Reset	0	0	0	0									0	0	0	0

Bit(s)	Name	Description
15	BOOT_SUPPORT	Supports eMMC boot-up The register bit indicates whether boot mode is supported or not. 1'b0: Not supported 1'b1: Supported
14:12	BOOT_WAIT_DELAY	eMMC wait delay time The register bit sets the delay time to wait for MMC device to exit boot-up mode after boot stop bit is set. 3'b000: 0x1024 clock cycles 3'b001: 1x1024 clock cycles 3'b010: 2x1024 clock cycles 3'b111: 7x1024 clock cycles
3	BOOT_ACK_CHK_DIS	Disables eMMC boot-up mode ACK check 1'b0: Do ACK pattern check 1'b1: Bypass ACK pattern check
2	BOOT_MODE	eMMC boot-up mode There are two kinds of boot-up mode supported by eMMC 4.4. Reset CMD mode is an option for eMMC 4.3. 1'b0: Pull low CMD mode 1'b1: Reset CMD mode
1	BOOT_STOP	Stops eMMC boot-up mode The register bit indicates the boot stop signal. Read always returns 0.
0	BOOT_START	Triggers eMMC boot-up start signal The register bit indicates that boot-up begins. Read always returns 0.

11230074 EMMC_CFG1 eMMC configuration register 1 00200003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BOOT_ACK_TOC												BOOT_DAT_TOC			
Type	RW												RW			
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BOOT_DAT_TOC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
31:20	BOOT_ACK_TOC	eMMC ack pattern timeout counter Unit: 2 ¹⁶ serial clock. SW cannot set it to 12'hFFF.
19:0	BOOT_DAT_TOC	eMMC read boot data timeout counter Unit: 2 ¹⁶ serial clock. SW cannot set it to 20'hFFFF.

11230078 EMMC_STS eMMC status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BOOT_DAT_R ECV	BOOT_ACK_R ECV	BOOT_UP_ST ATE	BOOT_ACK_T O	BOOT_DAT_T O	BOOT_ACK_E RR	BOOT_CRC_E RR
Type										RU	W1C	RU	W1C	W1C	W1C	W1C
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	BOOT_DAT_RECV	eMMC boot data is received This register is for SW to check whether the first 4-byte boot data are received or not. For other data after the first 4B data, this bit should not be referenced. SW should check RXFIFOCNT instead. 1'b0: No data in RXFIFO 1'b1: The first 4B data are in RXFIFO.
5	BOOT_ACK_RECV	eMMC ack is received Also check BOOT_ACK_ERR to determine whether it is passed or failed. 1'b0: No ACK pattern is received. 1'b1: ACK pattern has been received.
4	BOOT_UP_STATE	eMMC boot-up mode status The register bit indicates whether MMC device is operating in boot-up mode state or not. 1'b0: Not in boot-up state 1'b1: Boot-up state is on-going.
3	BOOT_ACK_TO	eMMC ack timeout The register bit indicates the controller detects a timeout condition while waiting for an ack pattern on DAT0. 1'b0: No ACK pattern timeout error 1'b1: ACK pattern timeout error
2	BOOT_DAT_TO	eMMC data timeout The register bit indicates the controller detects a timeout condition while waiting for boot data. 1'b0: No data timeout error 1'b1: Data timeout error
1	BOOT_ACK_ERR	eMMC ack error

Bit(s)	Name	Description
		The register bit indicates the status of ack pattern checking result. The bit will be set to 1 when there is ack pattern error.
		1'b0: No ACK pattern check error
		1'b1: ACK pattern check error
0	BOOT_CRC_ERR	eMMC CRC error The register bit indicates the CRC status of boot data. The bit will be set to 1 when there is data CRC error.
		1'b0: No data CRC error
		1'b1: Data CRC error

1123007C	EMMC_IOCON				eMMC IO control register											00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BOOT_RST
Type																RW
Reset																0

Bit(s)	Name	Description
0	BOOT_RST	Resets eMMC device boot-up mode The register bit triggers HW reset. eMMC device enters pre-idle state.
		1'b0: De-assert RST_n to eMMC card
		1'b1: Assert RST_n to eMMC card

11230080 SD_ACMD_RESP SD ACMD response register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUTOCMD_RESP															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCMD_RESP															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AUTOCMD_RESP	SD auto command response register This register stores the response[39:8] of ACMD12/ACMD23/ACMD19.

11230084	SD_ACMD19_TRG				SD ACMD19 target register								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FINE_TUNE_SEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	FINE_TUNE_SEL	Selects SD auto command 19 test target After auto-command 19 is triggered, MSDC will only change the phase of the selected one and keep the value of other tuning registers. SW can get the result from AUTOCMD_STS. There are a total of 32 phases for each delay line. 4'd0: Select PAD_CLK_TXDLY[5:0] as the target to run auto-command19 4'd1: Select PAD_CMD_RXDLY[5:0] as the target to run auto-command19 4'd2: Select PAD_DAT_RD_RXDLY[5:0] as the target to run auto-command19 4'd3: Select PAD_DAT_WR_RXDLY[5:0] as the target to run auto-command19 4'd4: Select DAT0_RD_DLY[5:0] as the target to run auto-command19 4'd5: Select DAT1_RD_DLY[5:0] as the target to run auto-command19 4'd6: Select DAT2_RD_DLY[5:0] as the target to run auto-command19 4'd7: Select DAT3_RD_DLY[5:0] as the target to run auto-command19 4'd8: Select DAT4_RD_DLY[5:0] as the target to run auto-command19 4'd9: Select DAT5_RD_DLY[5:0] as the target to run auto-command19 4'd10: Select DAT6_RD_DLY[5:0] as the target to run auto-command19 4'd11: Select DAT7_RD_DLY[5:0] as the target to run auto-command19 4'd12: Select CMD_RESP_RXDLY[5:0] as the target to run auto-command19 Others: Reserved

11230088 **SD_ACMD19_STS** **SD ACMD19 status register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUTOCMD19_STS															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCMD19_STS															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AUTOCMD19_STS	SD auto command 19 test result register When auto-command 19 is enabled, HW will automatically try 32 times of command-19 and store the result into this register. This register contains the 1st to the 32nd results in bit [0:31].

1123008C **DMA_SA_HIGH4BIT** **DMA start address register of the high 4 bits** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_SURR_ADDR_HIGH4BIT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DMA_SURR_ADDR_HIGH4BIT	Sets up high 4 bits address of start address because 64G DRAM needs 36-bit address

11230090 DMA_SA DMA start address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DMA_STR_ADDR	Start address of the DMA address This register sets the start address of DMA. In DMA basic mode, this field indicates the source or destination address of the data transfer which depends on the command. In descriptor base DMA, this is the descriptor chain start address.

11230094 DMA_CA DMA current address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_CURR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_CURR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DMA_CURR_ADDR	Current address of the DMA address This register reads the current address of the DMA descriptor chain.

11230098	DMA_CTRL				DMA control register								00006008				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name		BURST_SIZE				DMA_ALIGN	LAST_BUF	DMA_SPLIT_1K	DMA_MODE					AHB_READYM	DMA_RESUME	DMA_STOP	DMA_START
Type		RW				RW	RW	RW	RW					RO	WO	AO	WO
Reset		1	1	0	0	0	0	0	0					1	0	0	0

Bit(s)	Name	Description
14:12	BURST_SIZE	DMA burst size This field specifies the maximum transfer bytes allowed at the device per DMA burst. This field cannot be modified when the DMA status is 1. 3'd3: 8 bytes 3'd4: 16 bytes 3'd5: 32 bytes 3'd6: 64 bytes Other: Reserved
11	DMA_ALIGN	Specifies whether the DMA address is aligned with burst size. 1'b0: No DMA burst size alignment 1'b1: DMA burst size alignment
10	LAST_BUF	Last buffer of the basic DMA mode This field indicates the last buffer in the basic DMA mode.
9	DMA_SPLIT_1K	Specifies whether to split burst when crossing 1K boundary address 1'b0: Does not split 1K boundary 1'b1: Split 1K boundary
8	DMA_MODE	DMA operation mode This field indicates operation mode of DMA. 1'b0: Basic DMA mode 1'b1: Descriptor base DMA mode
3	AHB_READYM	Only for debugging when DMA hangs SW can check if the AHB bus is normal when GDMA hangs. 1'b0: Bus is not normal. 1'b1: Bus is normal.

Bit(s)	Name	Description
2	DMA_RESUME	DMA resume control register This bit resumes the DMA transaction. Read always returns 0.
1	DMA_STOP	DMA stop control register This bit stops the DMA transaction. When SW issues STOP command, SW must wait for this bit to be de-asserted or wait for DMA to be inactive to guarantee stop is done.
0	DMA_START	DMA start control register This bit starts the DMA transaction. Read always returns 0.

1123009C	DMA_CFG				DMA configuration register												00000004	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																DMA_CHK_SUM_12B		
Type																RW		
Reset																0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name			MSDC_ACTIVE_EN				AHB_HPROT_2_EN							LOCK_DISABLE	DMA_DSCP_CS_EN	DMA_STATUS		
Type			RW				RW							RW	RW	RU		
Reset			0	0			0	0						1	0	0		

Bit(s)	Name	Description
16	DMA_CHK_SUM_12B	Indicates GPD/BD checksum covers 16 bytes or 12 bytes 1'b0: GPD/BD checksum covers 16 bytes. 1'b1: GPD/BD checksum only covers 12 bytes.
13:12	MSDC_ACTIVE_EN	Indicates how to control msdc_active 2'b00: Dynamic control msdc_active 2'b01: msdc_active = 0 2'b10: msdc_active = 1 2'b11: Reserved
9:8	AHB_HPROT_2_EN	Determines how to control hprot_2 pin of AHB bus 1) AHB_HPROT_2_EN = 2'b00 and in Basic DMA mode, all write transfers of a burst will be accessed by bufferable mode except for the last burst of DMA. 2) AHB_HPROT2_2_EN=2'b00 and in Descriptor DMA mode, all write transfers of a burst will be accessed by bufferable mode except for HW's own update transfer. 2'b00: Dynamic control hprot_2 2'b01: hprot_2 = 0 2'b10: hprot_2 = 1
2	LOCK_DISABLE	Disables lock to improve EMI efficiency 1'b0: Enable AHB lock 1'b1: Disable AHB lock
1	DMA_DSCP_CS_EN	Enables DMA descriptor checksum This bit enables or disables the descriptor checksum validation function for the descriptor. This field cannot be modified when the DMA status is 1.

Bit(s)	Name	Description
0	DMA_STATUS	DMA status This bit indicates the status of the DMA. 1'b0: DMA engine is inactive. 1'b1: DMA engine is active.

112300A0	SW_DBG_SEL				MSDC software debug selection register										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_SEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DBG_SEL	Selects MSDC debug

112300A4 SW_DBG_OUT MSDC software debug output register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DBG_OUT	MSDC debug output 32-bit output selected by SW_DBG_SEL register

112300A8 DMA_LENGTH DMA length register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	XFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	XFER_SIZE	DMA total transfer size This field specifies the number of DMA transfer byte required for the movement of source data through DMA. This field is only valid in basic DMA mode.

112300B0 PATCH_BIT0 MSDC patch bit register 0 403C0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_MMC_DRV_RESP	DETECT_WR_CRC_TIMEOUT	SPC_ALWAYS_PUSH	SDIO_INT_DLY_SEL	SDC_CMD_CMDFAIL_SEL	SDC_CMD_IDRT_SEL	SDC_CFG_WDOD				SDC_CFG_BSYDLY				SDIO_CFG_INT_C_SEL	MSDC_BLKNUM_SEL
Type	RW	RW	RW	RW	RW	RW	RW				RW				RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC_FIFO_RD_DIS	CKGEN_MSDC_DLY_SEL				INT_DAT_LATCH_CHECK_SEL		DESC_UP_SEL					RD_DATA_T_SEL	DIS_RELECT_CMDWR_WHE_N_BSY	EN_SD_C_ODD_8BIT_SUP	EN_ST_ART_BIT_CHK_SUP
Type	RW	RW				RW		RW					RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0				0	1	1

Bit(s)	Name	Description
31	EN_MMC_DRV_RESP	Enables MSDC to always drive bus when wakeup response is output (BREAK) 1'b0: Disable 1'b1: Enable
30	DETECT_WR_CRC_TIMEOUT	Detects MSDC write data CRC phase timeout 1'b0: Does not detect CRC phase timeout 1'b1: Detect CRC phase timeout
29	SPC_ALWAYS_PUSH	SPC buffer push mechanism 1'b0: Push the buffer only when read transfer is on-going 1'b1: Always push the buffer
28	SDIO_INT_DLY_SEL	Selects SDIO interrupt latch time 1'b0: Latch the data line value in internal SDIO interrupt period 1'b1: Latch the data line value in 1 clock delay of internal SDIO interrupt period
27	SDC_CMD_CMDFAIL_SEL	Selects SDIO interrupt period recovery 1'b0: SDIO interrupt period will re-start after a CMD12 or CMD52 command is issued. 1'b1: SDIO interrupt period starts whenever DAT line is not busy.
26	SDC_CMD_IDRT_SEL	Selects SD identification response time The register bit indicates whether the command has a response time of NID clock cycles (i.e. 5 serial clock cycles as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 1.0). The register bit is valid only when the command has a response token in it. Thus, the register bit must be set to 1 for CMD2 (ALL_SEND_CID) and ACMD41 (SD_APP_OP_CMD).

Bit(s)	Name	Description
		1'b0: Otherwise
		1'b1: The command has a response time with NID clock cycles.
25:22	SDC_CFG_WDOD	SD write data output delay The period from finish of the response for the initial host write command or the last write data block in a multiple block write operation to the start bit of the next write data block requires at least two serial clock cycles. The register field extends the period (Write Data Output Delay) in unit of one serial clock. 4'b0000: No extension 4'b0001: Extend 1 more serial clock cycle 4'b0010: Extend 2 more serial clock cycles 4'b1111: Extend 15 more serial clock cycles
21:18	SDC_CFG_BSYDLY	SD R1B busy detection mode The register field is only valid for the commands with R1b response. If the command has a response of R1b type, MMC/SD controller must monitor the data line 0 for card busy status from the bit time that is two serial clock cycles after the command end bit to check if operations in MMC/SD memory card have finished. The register field expands the time between the command end bit and end of detection period to detect card busy status. If time is up and there is no card busy status on data line 0, the controller will abandon the detection. 4'b0000: No extension 4'b0001: Extend 1 more serial clock cycle 4'b0010: Extend 2 more serial clock cycles 4'b1111: Extend 15 more serial clock cycles
17	SDIO_CFG_INTC_SEL	Selects SDIO Interrupt model 1'b0: Only if data line [1] = 0, then it triggers SDIO interrupt event. 1'b1: Only if data line [3:0] = 4'b1101, then it triggers SDIO interrupt event.
16	MSDC_BLKNUM_SEL	Supports ACMD23 reliable/force programming features 1'b0: Supports ACMD23 reliable/force programming features 1'b1: Does not support ACMD23 reliable/force programming features
15	MSDC_FIFO_RD_DIS	Disables MSDC RXFIFO read 1'b0: Enable FIFO read permission to RXFIFO in PIO mode 1'b1: Disable FIFO read permission to RXFIFO in PIO mode
14:10	CKGEN_MSDC_DLY_SEL	Selects CKBUF in CKGEN Delay 32 stages in total
9:7	INT_DAT_LATCH_CK_SEL	Selects Internal MSDC clock phase

Bit(s)	Name	Description
6	DESC_UP_SEL	8 stages in total. Each stage can delay 1 clock period of msdc_src_ck. SD transfer done interrupt should be issued when GPD has been updated. 1'b1: Enable new function for generating SD transfer done interrupt 1'b0: Use old function for generating SD transfer done interrupt
3	RD_DAT_SEL	Defines whether to use rising or falling buffer data for SDR mode 1'b0: Use rising buffer data for SDR mode 1'b1: Use falling buffer data for SDR mode
2	DIS_REFLECT_CMDWR_WHEN_BSY	Enables SD command register write monitor 1'b0: Enable monitor function 1'b1: Disable monitor function
1	EN_SDC_ODD_8BIT_SUP	Enables SD odd number support for 8-bit data bus 1'b0: Disable 1'b1: Enable
0	EN_START_BIT_CHK_SUP	Enables SD start bit check function 1'b0: Disable 1'b1: Enable

112300B4 PATCH_BIT1 MSDC patch bit register 1 FFE64309

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSDC_CK_SHBFF_CKEN	MSDC_CK_RCTL_CKEN	MSDC_CK_WCTL_CKEN	MSDC_CK_SD_CKEN	MSDC_CK_ACMD_CKEN	MSDC_CK_VOLDET_CKEN	MSDC_CK_PSC_CKEN	MSDC_CK_SPC_CKEN	AHB_CK_GDMA_CKEN	AXI_WRAP_CKEN	DCM_EN	POP_MARK_WATER	STATE_CLEAR	Reserved0	FORCE_STOP_GDMA	ENABLE_SINGLED_BURST
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESET_GDMA	DDR_CMD_FIFO_SEL	Reserved1	BIAS_EN18IO28NM	STOP_DLY_SEL				BUSY_CHECK_SEL	GET_BUSY_MARGIN	CMD_RSP_TA_CNTR			WRDAT_CRCS_TACNT_R		
Type	RW	RW	RW	RW	RW				RW	RW	RW			RW		
Reset	0	1	0	0	0	0	1	1	0	0	0	0	1	0	0	1

Bit(s)	Name	Description
31	MSDC_CK_SHBFF_CKEN	msdc_src_ck clock enable bit for SHBFF 1'b0: Disable 1'b1: Enable
30	MSDC_CK_RCTL_CKEN	msdc_src_ck clock enable bit for RCTL 1'b0: Disable 1'b1: Enable
29	MSDC_CK_WCTL_CKEN	msdc_src_ck clock enable bit for WCTL 1'b0: Disable 1'b1: Enable
28	MSDC_CK_SD_CKEN	msdc_src_ck clock enable bit for SD 1'b0: Disable 1'b1: Enable
27	MSDC_CK_ACMD_CKEN	msdc_src_ck clock enable bit for ACMD 1'b0: Disable 1'b1: Enable
26	MSDC_CK_VOLDET_CKEN	msdc_src_ck clock enable bit for VOLDET 1'b0: Disable 1'b1: Enable
25	MSDC_CK_PSC_CKEN	msdc_src_ck clock enable bit for PSC 1'b0: Disable 1'b1: Enable
24	MSDC_CK_SPC_CKEN	msdc_src_ck clock enable bit for SPC 1'b0: Disable

Bit(s)	Name	Description
		1'b1: Enable
23	AHB_CK_GDMA_CKEN	hclk_ck clock enable bit for GDMA 1'b0: Disable 1'b1: Enable
22	AXI_WRAP_CKEN	axi_ck and ahb_ck enable bit for ahb2axi wrapper Must set this bit to 1 when in DMA mode for emmc50 spec, or this bit will be reserved. 1'b0: Disable 1'b1: Enable
21	DCM_EN	Host enables DCM for low power When there is no transfer, ahb_ck and msdc_src_ck will be divided from source clk. 1'b0: Enable 1'b1: Disable
20	POP_MARK_WATER	SW should set this bit to 1 when using block gap stop clk feature. 1'b0: Pop with water 1'b1: Mark pop water
19	STATE_CLEAR	Auto clears multi-bit sync state when set to 1 1'b0: Does not clear multi sync state 1'b1: Auto clear multi sync state
18	Reserved0	Please don't modify reserved bit field in order to avoid affecting normal function. Please keep it as default value for MSDC operation.
17	FORCE_STOP_GDMA	Forces state from WDMI_LAST_DATA to WDMI_IDLE with stop DMA bit 1'b0: Disable 1'b1: Enable this bit to stop wdm_i_cs when state hangs in WDMI_LAST_DATA and DMA_STOP is valid
16	ENABLE_SINGLE_BURST	This will only affect AHB bus MSDC design, but not AXI bus design. 1'b0: HW will send incr1 burst type. 1'b1: HW will send single burst type instead of incr1 type.
15	RESET_GDMA	SW can reset GDMA when design hangs. 1'b0: Does not reset GDMA 1'b1: Reset GDMA
14	DDR_CMD_FIX_SEL	Adds T/4 margin for DDR mode cmd 1'b0: Does not fix

Bit(s)	Name	Description
		1'b1: Fix DDR/HS400 mode CMD timing
13	Reserved1	Please don't modify reserved bit field in order to avoid affecting normal function. Please keep it as default value for MSDC operation.
12	BIAS_EN18IO_28NM	28NM BIAS controller register 1
11:8	STOP_DLY_SEL	Configuration read data clock stops at block gap
7	BUSY_CHECK_SEL	R1b checks data 0 then generates IRQ; write programming timeout check 1'b0: Does not check data 0 status when R1b cmd's cmdrdy interrupt is generated; does not check write programming timeout 1'b1: Check data 0 status when R1b cmd's cmdrdy interrupt is generated; check write programming timeout
6	GET_BUSY_MARGIN	Add margin for getting busy state of data 0 1'b0: 1 cycle reserved for getting busy state from CRC status end bit 1'b1: 3 cycles reserved for getting busy state from CRC status end bit
5:3	CMD_RSP_TA_CNTR	CMD response turnaround period Turnaround cycle = CMD_RSP_TA_CNTR + 2 In UHS104 mode, this register should be set to 1; in non-UHS104 mode, this register should be set to 0.
2:0	WRDAT_CRCS_TA_CNTR	Write data and CRC status turnaround period Turnaround cycle = WRDAT_CRCS_TA_CNTR + 2 In UHS104 mode, this register should be set to 1; in non-UHS104 mode, this register should be set to 0.

112300B8 PATCH_BIT2 MSDC patch bit register 2 14881803

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRCSTS_LATCH_EN_SEL			CFG_CRCSTS	CFG_CRCSTS_CNT		CFG_CRCSTS_EDGE	CFG_CRCSTS_SEL	POP_EN_CNT				DDR50_SEL	RESP_LATCH_EN_SEL		
Type	RW			RW	RW		RW	RW	RW				RW	RW		
Reset	0	0	0	1	0	1	0	0	1	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG_RESP	CFG_RESP_CNT			INTC_RESP_SEL		CFG_RDAT	CFG_RDAT_CNT					RESP_WAIT_CNT	SUPPORT_64G	ENHANCE_WAIT_GPD	
Type	RW	RW			RW		RW	RW					RW	RW	RW	
Reset	0	0	0	1	1		0	0	0	0	0	0	0	0	1	1

Bit(s)	Name	Description
31:29	CRCSTS_LATCH_EN_SEL	Configures latch CRC status enable signal for async FIFO in eMMC45 3'b000: Latch CRC status enables signal does not delay. 3'b001: Latch CRC status enables signal delays 1T msdc_ck. 3'b010: Latch CRC status enables signal delays 2T msdc_ck. 3'b011: Latch CRC status enables signal delays 3T msdc_ck. 3'b111: Latch CRC status enables signal delays 7T msdc_ck.
28	CFG_CRCSTS	Configures CRC status path selection This setting only uses eMMC4.5 features. 1'b0: Latch CRC status by selecting delay-line path 1'b1: Latch CRC status by selecting async FIFO path
27:26	CFG_CRCSTS_CNT	Configures how many data to be pushed into async FIFO until starting to pop out data from async FIFO The min. setting is 1. Do not set it to 0. This setting only uses eMMC4.5 features. 2'b00: Push 0 data in async FIFO when starting to pop out data from async FIFO 2'b01: Push 1 data in async FIFO when starting to pop out data from async FIFO 2'b10: Push 2 data in async FIFO when starting to pop out data from async FIFO 2'b11: Push 3 data in async FIFO when starting to pop out data from async FIFO
25	CFG_CRCSTS_EDGE	Configures this bit to select rising async FIFO or falling async FIFO 1'b0: Async FIFO latch CRC status uses rising async FIFO. 1'b1: Async FIFO latch CRC status uses falling async FIFO.
24	CFG_CRCSTS_SEL	Configures async FIFO path selection

Bit(s)	Name	Description
		1'b0: Use normal path in async FIFO
		1'b1: Use 2DFF path in async FIFO
23:20	POP_EN_CNT	Pop enable counter This field defines how many write pointer and read pointer margins begin to pop data transfer.
19	DDR50_SEL	New path can avoid byte swap issues. 1'b0: Old path for rising and falling data 1'b1: New path for rising data to rising FIFO and falling data to falling FIFO
18:16	RESP_LATCH_EN_SEL	Configures latch CMD response enable signal for async FIFO in eMMC45 3'b000: Latch CMD response enable signal does not delay. 3'b001: Latch CMD response enable signal delays 1T msdc_ck. 3'b010: Latch CMD response enable signal delays 2T msdc_ck. 3'b011: Latch CMD response enable signal delays 3T msdc_ck. 3'b111: Latch CMD response enable signal delays 7T msdc_ck.
15	CFG_RESP	Configures CMD response path selection This setting only uses eMMC4.5 features. 1'b0: Latch CMD response selects async FIFO path. 1'b1: Latch CMD response selects delay-line path.
14:12	CFG_RESP_CNT	Configures how many data to be pushed into async FIFO until starting to pop out data from async FIFO The min. setting is 1. Do not set it to 0. This setting only uses eMMC4.5 features. 3'b000: Push 0 data in async FIFO when starting to pop out data from async FIFO 3'b001: Push 1 data in async FIFO when starting to pop out data from async FIFO 3'b111: Push 7 data in async FIFO when starting to pop out data from async FIFO
11	INTC_RESP_SEL	Configures BREAK command async FIFO path 1'b0: Use normal path in async FIFO 1'b1: Use 2DFF path in async FIFO
9	CFG_RDAT	Configures read data path 1'b0: Read data path bypasses delay line. 1'b1: Read data path goes through delay line.
8:4	CFG_RDAT_CNT	Configures read data path delay line

Bit(s)	Name	Description
3:2	RESP_WAIT_CNT	Configures CMD response timeout Timeout cycle = $65T + 16 * RESP\_WAIT\_CNT$ 2'b00: CMD response timeout is 65T. 2'b01: CMD response timeout is $65T + 16 * 1T$. 2'b10: CMD response timeout is $65T + 16 * 2T$. 2'b11: CMD response timeout is $65T + 16 * 3T$.
1	SUPPORT_64G	Which project supports high 64G DRAM space access 1'b0: Do not support 64G DRAM access 1'b1: Support 64G DRAM access
0	ENHANCE_WAIT_GPD	If SW clears interrupt when GPD is not updated, the design will hang. Set this bit to 1 to avoid this issue in enhance write mode. 1'b0: Use old HW code 1'b1: Use new HW code for updating GPD in enhance mode

112300F0 PAD_TUNE0 MSDC pad tuning register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						PAD_CMD_RESP_RXDLY										
Type						RW										
Reset						0	0	0	0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DELAY_EN			PAD_DAT_WR_RXDLY				
Type									RW			RW				
Reset									0			0	0	0	0	0

Bit(s)	Name	Description
26:22	PAD_CMD_RESP_RXDLY	Controls CMD response internal delay line This register fine-tunes response phase latched by MSDC internal clock. 32 stages in total
7	DELAY_EN	Enables all delay cells to toggle when power-on 1'b0: Disable delay cell toggle 1'b1: Enable delay cell toggle
4:0	PAD_DAT_WR_RXDLY	Controls write data status internal delay line This register fine-tunes write status phase latched by MSDC internal clock. 32 stages in total

11230110 HW_DBG_SEL MSDC hardware debug selection register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HW_DBG_WRAP_SEL	HW_DBG_WRAP_TYPE_SEL		HW_DBG3_SEL					HW_DBG2_SEL							
Type	RW	RW		RW					RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_DBG1_SEL								HW_DBG0_SEL							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HW_DBG_WRAP_SEL	Selects HW debug output for wrapper 1'b0: Select original debug pins 1'b1: Select wrapper debug pins
30:29	HW_DBG_WRAP_TYPE_SEL	Selects HW debug output type for wrapper 2'b00: Select DRAM bus debug signal 2'b01: Select RISC bus debug signal 2'b10: select AHBM bus debug signal 2'b11: select AHBS bus debug signal
28:24	HW_DBG3_SEL	Selects HW debug output
23:16	HW_DBG2_SEL	Selects HW debug output
15:8	HW_DBG1_SEL	Selects HW debug output
7:0	HW_DBG0_SEL	Selects HW debug output

11230114 MAIN_VER MSDC main version register 20210706

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAIN_VER															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAIN_VER															
Type	RO															
Reset	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	0

Bit(s)	Name	Description
31:0	MAIN_VER	Main version

11230118 ECO_VER MSDC ECO version register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ECO_VER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ECO_VER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ECO_VER	ECO version

11230120 DMA_CFG_TD MSDC CQDMA descriptor configuration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SPLIT_LENGTH			
Type													RW			
Reset													0	0	0	

Bit(s)	Name	Description
3:1	SPLIT_LENGTH	CQDMA split length selection. This register shows a task descriptor which can be fetched after how many data have been transferred. 3'b000: 512 bytes 3'b001: 1K bytes 3'b010: 2K bytes 3'b011: 4K bytes others: 512 bytes

11230204 SW_CMDQ_CFG0 SW CMDQ configuration register 0 2D0B4000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CMDQ_WDAT_CNT										CMDQ_RDAT_CNT					
Type	RW										RW					
Reset	0	0	1	0	1	1	0	1	0	0	0	0	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMDQ_RDAT_CNT				CMDQ_DTYPE		CMDQ_RSPTYP			CMDQ_NUM					CMDQ_EN	
Type	RW				RW		RW			RW					RW	
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:22	CMDQ_WDAT_CNT	Sends cmdq window during write data transfer in one block HW will send cmd to device when data transfer of one block is smaller than 180T.
21:12	CMDQ_RDAT_CNT	Sends cmdq window during read data transfer in one block HW will send cmd to device when data transfer of one block is smaller than 180T.
11:10	CMDQ_DTYPE	This register should be configured 2'b00 when cmdq is enabled. 2'b00: No data token for the command
9:7	CMDQ_RSPTYP	This register should be configured as R1 response when cmdq is enabled. 3'b000: The command has no response. 3'b001: The command has R1/R5/R6/R7 response. The response token is 48-bit with CRC check (for MMC/SD/SDIO) (not including the SDIO abort command)
6:1	CMDQ_NUM	This register can only program cmd13/44/45 when cmdq is enabled. 6'b001101: cmd13 6'b101100: cmd44 6'b101101: cmd45
0	CMDQ_EN	Enables CMD queue 1'b0: Disable cmdq 1'b1: Enable cmdq

11230208 EMMC50_CFG0 eMMC50 configuration register 0 00E88822

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			MSDC_TXSKEW_SEL					EMMC50_MON_SEL	READ_DAT_CNT			ENDBIT_CNT				
Type			RW					RW	RW			RW				
Reset			0					0	1	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENDBIT_CNT					CMD_EDGE_SEL	CMD_RESP_SEL	END_BIT_CHK_CNT				CRC_STS_SEL	CRC_STS_EDGE	CRC_STS_CNT		PAD_CMD_LATCH_CLK
Type	RW					RW	RW	RW				RW	RW	RW		RW
Reset	1	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0

Bit(s)	Name	Description
29	MSDC_TXSKEW_SEL	1'b0: clk/cmd/data output does not pass through DFF in HS400 mode 1'b1: clk/cmd/data output passes through DFF in HS400 mode
24	EMMC50_MON_SEL	Debug emmc50 signals by setting this bit to 1 when debugging 1'b0: Select emmc50 debug signals to debug pin 1'b1: Does not select emmc50 debug signals to debug pins
23:21	READ_DAT_CNT	Sets latching how many data in RCLK domain switch pop condition.
20:11	ENDBIT_CNT	Sets end bit check value in RCLK domain
10	CMD_EDGE_SEL	Selects CMD response edge 1'b0: CMD response from RCLK rising edge latch 1'b1: CMD response from RCLK falling edge latch
9	CMD_RESP_SEL	Selects CMD response output 1'b0: CMD response from delay line; same as eMMC4.5 spec 1'b1: CMD response from FIFO; this is design for eMMC5.0 spec
8:5	END_BIT_CHK_CNT	Sets the number of cycles to check device busy status after CRC status
4	CRC_STS_SEL	Selects CRC status output 1'b0: CRC status data from 2-DFF before eMMC5.0 is used 1'b1: CRC status data from FIFO since eMMC5.0 is used
3	CRC_STS_EDGE	Selects CRC status edge in HS400 mode 1'b0: Select rising edge 1'b1: Select falling edge
2:1	CRC_STS_CNT	CRC status count
0	PAD_CMD_LATCH_CLK	Selects PAD CMD latch clock in HS400 mode 1'b0: Select internal clock as pad cmd latch clock in HS400 mode

Bit(s)	Name	Description
		1'b1: Select DS(RCLK) as pad cmd latch clock in HS400 mode

1123020C EMMC50_CFG1 eMMC50 configuration register 1 01000300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved0			DS_CFG	PSH_PS_SEL	PSH_CNT			EMMC50_DEBUG_SEL							
Type	RW			RW	RW	RW			RW							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAIT_8_CLK_CNT			RD_DATA_STOP	LATCH_CLK_SWITCH_CNT											
Type	RW				RW	RW										
Reset	0	0	0		0	0	0	1	1							

Bit(s)	Name	Description
31:29	Reserved0	Reserved for backup2
28	DS_CFG	Defines whether to mask the redundant DS clock or not 1'b0: Not mask redundant DS clock 1'b1: Mask redundant DS clock for enhance strobe mode
27	PSH_PS_SEL	Defines using rising or falling edge of push pulse 1'b0: Select rising edge 1'b1: Select falling edge
26:24	PSH_CNT	Defines starting to sync pop pulse to pop data after the push count is reached.
23:16	EMMC50_DEBUG_SEL	Selects eMMC50 debug signal out
15:12	WAIT_8_CLK_CNT	Configures 8 clock counter
11	RD_DAT_STOP	Selects eMMC50 read data stop signals 1'b0: Select rising signal 1'b1: Select falling signal
10:8	LATCH_CLK_SWITCH_CNT	Sets up latch clock switch counter after CRC status

1123021C EMMC50_CFG2 AHB2AXI wrapper control register 0F0C0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		AXI_BUSY	AXI_RESP_ERR_TYPE		AXI_SET_LEN				AXI_RD_OUTSTANDING_NUM					AXI_BOUND_4K	AXI_BOUND_2K	AXI_BOUND_1K
Type		RU	RO		RW				RW					RW	RW	RW
Reset		0	0	0	1	1	1	1	0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_BOUND_512B	AXI_BOUND_256B	AXI_BOUND_128B					AXI_SHARE_EMI	AXI_IOMMU_RD_EMI	Reserved0				AXI_SHARE_EMI	AXI_IOMMU_WR_EMI	
Type	RW	RW	RW					RW	RW	RW				RW	RW	
Reset	0	0	0					0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
30	AXI_BUSY	Checks if AXI bus is busy or idle 1'b0: AXI wrapper is idle. 1'b1: AXI wrapper is busy.
29:28	AXI_RESP_ERR_TYPE	When SW gets AXI response error interrupt, check this bit to know which type of error has occurred. 2'b00: No error 2'b01: Do not care 2'b10: Slave error 2'b11: Decode error
27:24	AXI_SET_LEN	SW can program this bit to set the transfer number in one AXI burst both for read and write. For performance, this bit can be set to 4'hf. 4'b0000: 1 beat per burst 4'b0001: 2 beats per burst 4'b0010: 3 beats per burst 4'b0011-4'b1110: And so on 4'b1111: 16 beats per burst
23:19	AXI_RD_OUTSTANDING_NUM	AXI supports outstanding transaction, i.e., when there is no response, send AXI cmd. For performance, SW can set this bit up to 13. 5'd1: Support 1 outstanding transaction 5'd2: Support 2 outstanding transactions 5'd3: Support 3 outstanding transactions 5'b4-5'd12: And so on 5'd13: Support 13 outstanding transactions
18	AXI_BOUND_4K	Default is 4K in AXI spec.

Bit(s)	Name	Description
		1'b0: Does not select 4K boundary 1'b1: Select 4K boundary
17	AXI_BOUND_2K	For future project option 1'b0: Does not select 2K boundary 1'b1: Select 2K boundary
16	AXI_BOUND_1K	For future project option 1'b0: Does not select 1K boundary 1'b1: Select 1K boundary
15	AXI_BOUND_512B	For future project option 1'b0: Does not select 512B boundary 1'b1: Select 512B boundary
14	AXI_BOUND_256B	For future project option 1'b0: Does not select 256B boundary 1'b1: Select 256B boundary
13	AXI_BOUND_128B	For future project option 1'b0: Does not select 128B boundary 1'b1: Select 128B boundary
8	AXI_SHARE_EN_RD_EMI	1'b0: Disable share 1'b1: Enable share
7	AXI_IOMMU_RD_EMI	1'b0: Does not pass through IOMMU 1'b1: Through IOMMU
6:3	Reserved0	Reserved
2	AXI_SHARE_EN_WR_EMI	1'b0: Disable share 1'b1: Enable share
1	AXI_IOMMU_WR_EMI	1'b0: Does not pass through iommu 1'b1: Through iommu

11230220 EMMC50_CFG3 AHB2AXI wrapper control register 0F28A3C1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved0	AXI_ARPROT	AXI_AWPROT	PREULTRA_SET_RD					ULTRA_SET_RD							PREULTRA_SET_WR
Type	RO	RW	RW	RW					RW							RW
Reset	0	0	0	0	1	1	1	1	0	0	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PREULTRA_SET_WR					ULTRA_SET_WR					OUT_STANDING_WR					
Type	RW					RW					RW					
Reset	1	0	1	0	0	0	1	1	1	1	0	0	0	0	0	1

Bit(s)	Name	Description
31	Reserved0	Reserved
30	AXI_ARPROT	Only secure user can write this bit. AXI supports secure/non-secure protection of a transaction when the transaction is a data access. 1'b1: Non-secure access 1'b0: Secure access
29	AXI_AWPROT	Only secure user can write this bit. AXI supports secure/non-secure protection of a transaction when the transaction is a data access. 1'b1: Non-secure access 1'b0: Secure access
28:23	PREULTRA_SET_RD	MSDC GDMA has higher priority when these bits are set bigger.
22:17	ULTRA_SET_RD	MSDC GDMA has higher priority when these bits are set bigger.
16:11	PREULTRA_SET_WR	MSDC GDMA has higher priority when these bits are set smaller.
10:5	ULTRA_SET_WR	MSDC GDMA has higher priority when these bits are set smaller.
4:0	OUT_STANDING_WR	AXI supports outstanding transaction, i.e. when there is no response, send AXI command. To improve performance, software can set this bit to up to 13.

11230224 EMMC50_CFG4 AHB2AXI wrapper control register 0001281E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved0									wrap_sel					ULTRA_EN	
Type	RO									RW					RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMPR_ULTRA_SET_RD									IMPR_ULTRA_SET_WR						
Type	RW									RW						
Reset	0	0	1	0	1	0	0	0	0	0	0	1	1	1	1	0

Bit(s)	Name	Description
31:23	Reserved0	Reserved
22:18	wrap_sel	For HW to select debug signal
17:16	ULTRA_EN	This cannot be set to high priority, if the high priority reduces other module's performance. 2'b00: Lowest priority 2'b01: Lower priority 2'b10: Middle priority 2'b11: High priority
15:8	IMPR_ULTRA_SET_RD	MSDC GDMA has higher priority when these bits are set bigger. The host can improve priority by setting up ULTRA_SET_RD.
7:0	IMPR_ULTRA_SET_WR	MSDC GDMA has higher priority when these bits are set smaller. The host can improve priority by setting up ULTRA_SET_WR.

11230228 SDC_FIFO_CFG 1KB FIFO configuration 070C0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RD_VALID	WR_VALID	RD_VALID_SEL	WR_VALID_SEL	WR_PTR_MARGIN							
Type					RU	RU	RW	RW	RW							
Reset					0	1	1	1	0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								EMMC50_BLOCK_LENGTH								
Type								RW								
Reset								0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
27	RD_VALID	The host transfers data to device till it has the whole block length data in FIFO. 1'b0: SD FIFO is not valid to read for writing device. 1'b1: SD FIFO is valid to read for writing device.
26	WR_VALID	The host has enough space for storing a block length data read from device. 1'b0: SD FIFO is not valid for reading data from device. 1'b1: SD FIFO is valid for reading data from device.
25	RD_VALID_SEL	Configures read data valid case during read data transfer 1'b0: Read data are valid only when host has enough space for storing a block length data read from device. 1'b1: Read data are always valid.
24	WR_VALID_SEL	Configures write data valid case during write data transfer 1'b0: Write data are valid only when host has the whole block length data in FIFO when host is to transfer data to device. 1'b1: Write data are always valid.
23:16	WR_PTR_MARGIN	Write pointer margin
8:0	EMMC50_BLOCK_LENGTH	SW sets the FIFO water level for stop clk in different block lengths. If device block length is 512B, set this register to 9'd128. If device block length is 256B, set this register to 9'd64. If device block length is 128B, set this register to 9'd32. If device block length is 64B, set this register to 9'd16. If device block length is 32B, set this register to 9'd8.

112307FC CQHCI_SETTING eMMC51 CQHCI features 0001C200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															CQHCI_TCN_ERR_MASK	
Type															RW	
Reset															0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CQHCI_BLOCK_LEN											
Type					RW											
Reset					0	0	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	CQHCI_TCN_ERR_MASK	Indicates whether mask error for CQTCN (i.e., this bit indicates whether task error is showed when CQTCN is asserted.) 1'b0: Do not mask error for CQTCN 1'b1: Mask error for CQTCN
11:0	CQHCI_BLOCK_LEN	Block length set for CQE

11230800 CQVER eMMC51 CQHCI features 00000510

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved				CQHCI_VER_MAJOR				CQHCI_VER_MINOR1				CQHCI_VER_MINOR2			
Type	RO				RO				RO				RO			
Reset	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:12	Reserved	Reserved
11:8	CQHCI_VER_MAJOR	eMMC Major Version Number (digit left of decimal point), in BCD format
7:4	CQHCI_VER_MINOR1	eMMC Minor Version Number (digit right of decimal point), in BCD format
3:0	CQHCI_VER_MINOR2	eMMC Version Suffix (2nd digit right of decimal point), in BCD format

11230804 **CQCAP** eMMC51 CQHCI features 000020B6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved2				Reserved1											
Type	RO				RO											
Reset	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQHCI_CAP_ITCFMUL				Reserved0		CQHCI_CAP_ITCFVAL									
Type	RO				RO		RO									
Reset	0	0	1	0	0	0	0	0	1	0	1	1	0	1	1	0

Bit(s)	Name	Description
31:29	Reserved2	Reserved
27:16	Reserved1	Reserved
15:12	CQHCI_CAP_ITCFMUL	Internal Timer Clock Frequency Multiplier (ITCFMUL) ITCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for determining the SQS polling period. 4'd0: 0.001 MHz 4'd1: 0.01 MHz 4'd2: 0.1 MHz 4'd3: 1 MHz 4'd4: 10 MHz Others: Other values are reserved
11:10	Reserved0	Reserved
9:0	CQHCI_CAP_ITCFVAL	Internal Timer Clock Frequency Value (ITCFVAL) ITCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for determining the polling period when using periodic SEND_QUEUE_STATUS (CMD13) polling. The clock frequency is calculated as ITCFVAL * ITCFMUL. For example, to encode 19.2 MHz, ITCFVAL shall be C0h (= 192 decimal) and ITCFMUL shall be 2h (0.1 MHz): 192 * 0.1 MHz = 19.2 MHz.

11230808 CQCFG eMMC51 CQHCI features 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved3			CQHCI_DCMD	Reserved2	Reserved1		CQHCI_TASK_DESC_SZ	Reserved0							CQHCI_ENABLE
Type	RO			RW	RO	RO		RO	RO							RW
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0		0

Bit(s)	Name	Description
31:13	Reserved3	Reserved
12	CQHCI_DCMD	Direct Command (DCMD) Enable This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a Data Transfer Task Descriptor, or a Direct Command Task Descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. 1'b1: Task descriptor in slot #31 is a DCMD Task Descriptor 1'b0: Task descriptor in slot #31 is a Data Transfer Task Descriptor
11	Reserved2	Reserved
10:9	Reserved1	Reserved
8	CQHCI_TASK_DESC_SZ	Task Descriptor Size This bit indicates whether the task descriptor size is 128 bits or 64 bits as detailed in Data Structures section. 1'b1: Task descriptor size is 128 bits 1'b0: Task descriptor size is 64 bits
7:2	Reserved0	Reserved
0	CQHCI_ENABLE	Command Queuing Enable This bit shall be set to 1 in order to enable command queuing mode (i.e., enable CQE). When this bit is 0, CQE is disabled and software controls the eMMC bus using the legacy eMMC host controller. Before software writes 1 to this bit, software shall verify that the eMMC host controller is in idle state and there are no commands or data transfers ongoing. When software wants to exit command queuing mode, it shall clear all previous tasks if such tasks exist before setting this bit to 0. 1'b0: Disable CQ

Bit(s)	Name	Description
		1'b1: Enable CQ

1123080C CQCTL eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved1							CQHCI_CLEAR_ALL_TASKS	Reserved0							CQHCI_HALT
Type	RO							AO	RO							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0

Bit(s)	Name	Description
31:9	Reserved1	Reserved
8	CQHCI_CLEAR_ALL_TASKS	Clear All Tasks This bit shall be set to 1 when it wants to clear all the tasks sent to the device. This bit can only be written when CQE is in halt state (i.e., Halt bit is 1). When software writes 1, the value of the register is updated to 1, and CQE shall reset CQTDBR register and all other context information for all unfinished tasks. Then CQE will clear this bit. Software should poll on this bit until it is set back to 0 and may then resume normal operation, by clearing the Halt bit. CQE does not inform the device that the tasks are cleared. It is software's responsibility to order the device to discard the tasks in its queue using CMDQ_TASK_MGMT command. Writing 0 to this register shall have no effect.
7:2	Reserved0	Reserved
0	CQHCI_HALT	Halt The bit shall be set to 1 when it wants to acquire software control over the eMMC bus and disable CQE from issuing commands on the bus. CQE shall complete the ongoing task if such a task is in progress. Once the task is completed and CQE is in idle state, CQE shall not issue new commands and shall indicate so to software by setting this bit to 1. In order to exit halt state (i.e., resume CQE activity), software shall clear this bit (write 0). Writing 0 when the value is already 0 shall have no effect.

11230810 CQIS eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved1								CQHCI_IS_HCFE	CQHCI_IS_DEE	CQHCI_IS_ICCE	Reserved0	CQHCI_IS_TCL	CQHCI_IS_RED	CQHCI_IS_TCC	CQHCI_IS_HAC
Type	RO								W1C	W1C	W1C	RO	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	Reserved1	Reserved
7	CQHCI_IS_HCFE	Host Controller Fatal Error (HCFE) This status bit indicates (if CQISTE.HCFE=1) that the hardware has encountered a fatal error from which it cannot recover. When this interrupt is generated, software is expected to reset the host controller.
6	CQHCI_IS_DEE	Device Exception Event (DEE) This status bit is asserted (if CQISTE.DEE=1) when an R1 response is received to any command (except CMD13-SQS) where EXCEPTION_EVENT bit (bit 6) is set, indicating an exception by the device.
5	CQHCI_IS_ICCE	Invalid Crypto Configuration Error (ICCE) If cryptographic operations are supported by the host controller (as indicated in CQCAP.CS), this status bit is asserted (if CQISTE.ICCE=1) when the TD.CE=1 and the value in TD.CCI points to a CRYPTOCFG which is not enabled. If cryptographic operations are not supported, this status bit is reserved.
4	Reserved0	General Crypto Error (GCE) If cryptographic operations are supported by the host controller (as indicated in CQCAP.CS), this status bit is asserted (if CQISTE.GCE=1) when the crypto hardware encounters an error in the processing of a transaction. If cryptographic operations are not supported, this status bit is reserved.
3	CQHCI_IS_TCL	Task Cleared (TCL) This status bit is asserted (if CQISTE.TCL=1) when a task clear operation is completed by CQE. The completed task clear operation is either an individual task clear (CQTCLR) or clearing of all tasks (CQCTL).
2	CQHCI_IS_RED	Response Error Detected Interrupt (RED) This status bit is asserted (if CQISTE.RED=1) when a response is received with an error bit set in the device status field. Software uses CQRMEM register to configure which device status bit fields may trigger an interrupt, and which are masked.

Bit(s)	Name	Description
1	CQHCI_IS_TCC	Task Complete Interrupt (TCC) This status bit is asserted (if CQISTE.TCC=1) when at least one of the following two conditions are met: 1) A task is completed and the INT bit is set in its Task Descriptor 2) Interrupt caused by Interrupt Coalescing logic
0	CQHCI_IS_HAC	Halt Complete Interrupt (HAC) This status bit is asserted (if CQISTE.HAC=1) when HALT or HOEQ bit in CQCTL register transitions from 0 to 1 indicating that host controller has completed its current ongoing task and has entered halt state.

11230814 CQISTE eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved1								CQHCI_ISTE_H_CFE	CQHCI_ISTE_D_EE	CQHCI_ISTE_IC_CE	Reserved0	CQHCI_ISTE_T_CL	CQHCI_ISTE_R_ED	CQHCI_ISTE_T_CC	CQHCI_ISTE_HAC
Type	RO								RW	RW	RW	RO	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	Reserved1	Reserved
7	CQHCI_ISTE_H_CFE	Host Controller Fatal Error Status Enable (HCFE) 1'b1: CQIS.HCFE will be set when its interrupt condition is active 1'b0: CQIS.HCFE is disabled
6	CQHCI_ISTE_DEE	Device Exception Event Status Enable (DEE) 1'b1: CQIS.DEE will be set when its interrupt condition is active 1'b0: CQIS.DEE is disabled
5	CQHCI_ISTE_ICCE	Invalid Crypto Configuration Error Status Enable (ICCE) 1'b1: CQIS.ICCE will be set when its interrupt condition is active 1'b0: CQIS.ICCE is disabled
4	Reserved0	General Crypto Error Status Enable (GCE) 1'b1: CQIS.GCE will be set when its interrupt condition is active 1'b0: CQIS.GCE is disabled
3	CQHCI_ISTE_TCL	Task Cleared Status Enable (TCL) 1'b1: CQIS.TCL will be set when its interrupt condition is active 1'b0: CQIS.TCL is disabled
2	CQHCI_ISTE_RED	Response Error Detected Status Enable (RED) 1'b1: CQIS.RED will be set when its interrupt condition is active 1'b0: CQIS.RED is disabled
1	CQHCI_ISTE_TCC	Task Complete Status Enable (TCC) 1'b1: CQIS.TCC will be set when its interrupt condition is active 1'b0: CQIS.TCC is disabled
0	CQHCI_ISTE_HAC	Halt Complete Status Enable (HAC) 1'b1: CQIS.HAC will be set when its interrupt condition is active

Bit(s)	Name	Description
		1'b0: CQIS.HAC is disabled

11230818 CQISGE eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved1								CQHCI_ISGE_H_CFE	CQHCI_ISGE_D_EE	CQHCI_ISGE_IC_CE	Reserved0	CQHCI_ISGE_T_CL	CQHCI_ISGE_R_ED	CQHCI_ISGE_T_CC	CQHCI_ISGE_T_HAC
Type	RO								RW	RW	RW	RO	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	Reserved1	Reserved
7	CQHCI_ISGE_H_CFE	Host Controller Fatal Error Signal Enable (HCFE) When set and CQIS.HCFE is asserted, the CQE shall generate an interrupt 1'b1: Enable the generation of interrupt to host software 1'b0: Disable the generation of interrupt to host software
6	CQHCI_ISGE_DEE	Device Exception Event Signal Enable (DEE) When set and CQIS.DEE is asserted, the CQE shall generate an interrupt 1'b1: Enable the generation of interrupt to host software 1'b0: Disable the generation of interrupt to host software
5	CQHCI_ISGE_ICCE	Invalid Crypto Configuration Error Signal Enable (ICCE) When set and CQIS.ICCE is asserted, the CQE shall generate an interrupt 1'b1: Enable the generation of interrupt to host software 1'b0: Disable the generation of interrupt to host software
4	Reserved0	General Crypto Error Signal Enable (GCE) When set and CQIS.GCE is asserted, the CQE shall generate an interrupt 1'b1: Enable the generation of interrupt to host software 1'b0: Disable the generation of interrupt to host software
3	CQHCI_ISGE_TCL	Task Cleared Signal Enable (TCL) When set and CQIS.TCL is asserted, the CQE shall generate an interrupt 1'b1: Enable the generation of interrupt to host software 1'b0: Disable the generation of interrupt to host software
2	CQHCI_ISGE_RED	Response Error Detected Signal Enable (RED) When set and CQIS.RED is asserted, the CQE shall generate an interrupt 1'b1: Enable the generation of interrupt to host software

Bit(s)	Name	Description
1	CQHCI_ISGE_TCC	1'b0: Disable the generation of interrupt to host software Task Complete Signal Enable (TCC) When set and CQIS.TCC is asserted, the CQE shall generate an interrupt 1'b1: Enable the generation of interrupt to host software 1'b0: Disable the generation of interrupt to host software
0	CQHCI_ISGE_HAC	Halt Complete Signal Enable (HAC) When set and CQIS.HAC is asserted, the CQE shall generate an interrupt 1'b1: Enable the generation of interrupt to host software 1'b0: Disable the generation of interrupt to host software

1123081C CQIC eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CQHCI_IC_ENABLE	Reserved2										CQHCI_IC_ICSB	Reserved1			CQHCI_IC_RESET
Type	RW	RO										RO	RO			WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQHCI_IC_ICCTHWE_N	Reserved0		CQHCI_IC_ICCTH				CQHCI_IC_ICCTHWE_N	CQHCI_IC_ICCTHVAL							
Type	WO	RO		RW				WO	RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	CQHCI_IC_ENABLE	Interrupt Coalescing Enable/Disable: When set to 0 by software, command responses are neither counted nor timed. Interrupts are still triggered by completion of tasks with INT=1 in the Task Descriptor. When set to 1, the interrupt coalescing mechanism is enabled and coalesced interrupts are generated 1'b1: Enable the interrupt coalescing 1'b0: Disable the interrupt coalescing
30:21	Reserved2	Reserved
20	CQHCI_IC_ICSB	Interrupt Coalescing Status Bit (ICSB): This bit indicates to software whether any tasks (with INT=0) have completed and counted towards interrupt coalescing (i.e., ICSB is set if and only if IC counter > 0). 1'b1: At least one task completion has been counted (IC counter > 0) 1'b0: No task completions have occurred since last counter reset (IC counter = 0)
19:17	Reserved1	Reserved
16	CQHCI_IC_RESET	Counter and Timer Reset (ICCTR): When host driver writes 1, the interrupt coalescing timer and counter are reset
15	CQHCI_IC_ICCTHWE_N	Interrupt Coalescing Counter Threshold Write Enable (ICCTHWE_N): When software writes 1, the value ICCTH is updated with the contents written at the same cycle. When software writes 0, the value in ICCTH is not updated. Note: Write operations to ICCTH are only allowed when the task queue is empty.
14:13	Reserved0	Reserved

Bit(s)	Name	Description
12:8	CQHCL_IC_ICCTH	Interrupt Coalescing Counter Threshold (ICCTH): Software uses this field to configure the number of task completions (only tasks with INT=0 in the Task Descriptor) which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT= 0 are completed, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in ICCTH. The maximum allowed value is 31 Note: When ICCTH is 0, task completions are not counted, and counting-based interrupts are not generated. In order to write to this field, the ICCTHWEN bit must be set at the same write operation.
7	CQHCL_IC_ICTOVALWEN	Interrupt Coalescing Timeout Value Write Enable (ICTOVALWEN): When software writes 1, the value ICTOVAL is updated with the contents written at the same cycle. When software writes 0, the value in ICTOVAL is not updated. Note: Write operations to ICTOVAL are only allowed when the task queue is empty.
6:0	CQHCL_IC_ICTOVAL	Interrupt Coalescing Timeout Value (ICTOVAL): Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when a data transfer task with INT=0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field, it generates an interrupt and stops. The timer unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. The minimum value is 01h (1024 clock periods) and the maximum value is 7Fh (127*1024 clock periods). For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in ICTOVAL is 10h, the calculated polling period is $16*1024*52.08\text{ ns} = 853.33\text{ }\mu\text{s}$ Note: When ICTOVAL is 0, the timer is not running, and timer-based interrupts are not generated. In order to write to this field, the ICTOVALWEN bit must be set at the same write operation.

Bit(s)	Name	Description

11230820 **CQTDLBA** eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CQHCI_TDLBA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQHCI_TDLBA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQHCI_TDLBA	Task Descriptor List Base Address (TDLBA) This register stores the LSB bits (bits 31:0) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This address shall be set on 1 KB boundary: The lower 10 bits of this register shall be set to 0 by software and shall be ignored by CQE.

11230824 **CQTDLBAU** eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CQHCI_TDLBAU															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQHCI_TDLBAU															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQHCI_TDLBAU	Task Descriptor List Base Address (TDLBA) This register stores the MSB bits (bits 63:32) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This register is reserved when using 32-bit addressing mode.

11230828 **CQTDBR** eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CQHCI_TDBR															
Type	A0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQHCI_TDBR															
Type	A0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQHCI_TDBR	Command Queuing Task Doorbell Software shall configure TDLBA and TDLBAU, and enable CQE in CQCFG before using this register. Writing 1 to bit n of this register triggers CQE to start processing the task encoded in slot n of the TDL. CQE always processes tasks in-order according to the order submitted to the list by CQTDBR write transactions. CQE processes Data Transfer tasks by reading the Task Descriptor and sending QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) commands to the device. CQE processes DCMD tasks (in slot 31, when enabled) by reading the Task Descriptor, and generating the command encoded by its index and argument. The corresponding bit is cleared to 0 by CQE in one of the following events: a) When a task execution is completed (with success or error) b) The task is cleared using CQTCLR register c) All tasks are cleared using CQCTL register d) CQE is disabled using CQCFG register Software may initiate multiple tasks at the same time (batch submission) by writing 1 to multiple bits of this register in the same transaction. In the case of batch submission: CQE shall process the tasks in order of the task index, starting with the lowest index. If one or more tasks in the batch are marked with QBR, the ordering of execution will be based on said processing order. Writing 0 by software shall have no impact on the hardware, and will not change the value of the register bit.

1123082C CQTCN eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CQHCI_TCN															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQHCI_TCN															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQHCI_TCN	Task Complete Notification CQE shall set bit n of this register (at the same time it clears bit n of CQTDBR) when a task execution is completed (with success or error). When receiving interrupt for task completion, software may read this register to know which tasks have finished. After reading this register, software may clear the relevant bit fields by writing 1 to the corresponding bits.

11230830 CQDQS eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CQHCI_DQS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQHCI_DQS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQHCI_DQS	Device Queue Status Every time the Host controller receives a queue status register (QSR) from the device, it updates this register with the response of status command, i.e., the device queue status.

11230834 CQDPT eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CQHCI_DPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQHCI_DPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQHCI_DPT	Device Pending Tasks Bit n of this register is set if and only if QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) are sent for this specific task and if this task has not been executed yet. CQE shall set this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution. Software needs to read this register in the task-discard procedure, when the controller is halted, to determine if the task is queued in the device. If the task is queued, the driver sends a CMDQ_TASK_MGMT (CMD48) to the device ordering it to discard the task. Then software clears the task in the CQE. Only then the software orders CQE to resume its operation using CQCTL register.

11230838 CQTCLR eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CQHCI_TCLR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQHCI_TCLR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQHCI_TCLR	Command Queuing Task Clear Writing 1 to bit n of this register orders CQE to clear a task which software has previously issued. This bit can only be written when CQE is in Halt state as indicated in CQCTL register Halt bit. When software writes 1 to a bit in this register, CQE updates the value to 1, and starts clearing the data structures related to the task. CQE clears the bit fields (sets a value of 0) in CQTCLR and in CQTDDBR once clear operation is completed. Software should poll on the CQTCLR until it is cleared to verify clear operation was completed. Writing to this register only clears the task in the CQE and does not have impact on the device. In order to discard the task in the device, host software shall send CMDQ_TASK_MGMT while CQE is still in Halt state. Host driver is not allowed to use this register to clear multiple tasks at the same time. Clearing multiple tasks can be done using CQCTL register. Writing 0 to a register bit shall have no impact.

1123083C CQTDPE eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CQHCI_TDP_ERR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQHCI_TDP_ERR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQHCI_TDP_ERR	Task Descriptor Processing Error Bit n of this register indicates that an error was detected when processing a Task Descriptor with Task ID = n. When fetching a TD with Task ID = n from system memory, bit n is set, and CQIS.ICCE interrupt is generated, if the following conditions are met: Cryptographic operations are supported (CQCAP.CS=1) and enabled (CQCFG.GCE=1), Encryption/Decryption is enabled in the TD (TD.CE=1), CRYPTOCFG is disabled (x-CRYPTOCFG[TD.CCI]=0) or is nonexistent (TD.CCI >= CRCAP.CFGC). Bit n is cleared by the hardware when software clears task n in CQTCLR register

11230840 CQSSC1 eMMC51 CQHCI features 00001000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQHCI_SSC1_CIT															
Type	RW															
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	Reserved0	Reserved
15:0	CQHCI_SSC1_CIT	Send Status Command Idle Timer (CIT) This field indicates to CQE the polling period to use when using periodic SEND_QUEUE_STATUS (CMD13) polling. Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicating that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS. Timer units are clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. The minimum value is 0001h (1 clock period) and the maximum value is FFFFh (65535 clock periods). Default interval is 4096 clock periods. For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in CQSSC1.CIT is 1000h, the calculated polling period is $4096 * 52.08 \text{ ns} = 213.33 \mu\text{s}$

11230844 **CQSSC2** eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQHCI_SSC2_RCA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	Reserved0	Reserved
15:0	CQHCI_SSC2_RCA	Send Queue Status RCA This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_STATUS (CMD13) command argument. CQE shall copy this field to bits 31:16 of the argument when transmitting SEND_QUEUE_STATUS (CMD13) command.

11230848 **CQCRDCT** eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CQHCI_CRDCT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQHCI_CRDCT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQHCI_CRDCT	Direct Command Last Response This register contains the response of the command generated by the last direct-command (DCMD) task which was sent. CQE shall update this register when it receives the response for a DCMD task. This register is considered valid only after bit 31 of CQTDBR register is cleared by CQE.

11230850 CQRMEM eMMC51 CQHCI features FDF9A080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CQHCI_RMEM															
Type	RW															
Reset	1	1	1	1	1	1	0	1	1	1	1	1	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQHCI_RMEM															
Type	RW															
Reset	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQHCI_RMEM	Response Mode Error Mask This bit is used as interrupt mask on the device status field which is received in R1/R1b responses. Bit Value Description (for any bit i): 1 = When a R1/R1b response is received, with bit i in the device status set, a RED interrupt is generated 0 = When a R1/R1b response is received, bit i in the device status is ignored The reset value of this register is set to trigger an interrupt on all Error type bits in the device status Note: Responses to CMD13 (SQS) encode the QSR, so they are ignored by this logic.

11230854 CQTERRI eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CQHCI_TERRI_D_VALID	Reserved3		CQHCI_TERRI_D_TASK					Reserved2		CQHCI_TERRI_D_INDEX					
Type	RO	RO		RO					RO		RO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQHCI_TERRI_C_VALID	Reserved1		CQHCI_TERRI_C_TASK					Reserved0		CQHCI_TERRI_C_INDEX					
Type	RO	RO		RO					RO		RO					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	CQHCI_TERRI_D_VALID	Data Transfer Error Fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a data transfer is in progress when the error is detected/indicated, the bit is set to 1. If a no data transfer is in progress when the error is detected/indicated, the bit is cleared to 0.
30:29	Reserved3	Reserved
28:24	CQHCI_TERRI_D_TASK	Data Transfer Error Task ID This field indicates the ID of the task which was executed on the data lines when an error occurred. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
23:22	Reserved2	Reserved
21:16	CQHCI_TERRI_D_INDEX	Data Transfer Error Command Index This field indicates the index of the command which was executed on the data lines when an error occurred. The index shall be set to EXECUTE_READ_TASK (CMD46) or EXECUTE_WRITE_TASK (CMD47) according to the data direction. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
15	CQHCI_TERRI_C_VALID	Response Mode Error Fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a command transaction is in progress when the error is detected/indicated, the bit is set to 1. If a no command transaction is in progress when the error is detected/indicated, the bit is cleared to 0.

Bit(s)	Name	Description
14:13	Reserved1	Reserved
12:8	CQHCI_TERRI_C_TASK	Response Mode Error Task ID This field indicates the ID of the task which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.
7:6	Reserved0	Reserved
5:0	CQHCI_TERRI_C_INDEX	Response Mode Error Command Index This field indicates the index of the command which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.

11230858	<u>CQCRI</u>			eMMC51 CQHCI features												00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	Reserved0																	
Type	RO																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	Reserved0										CQHCI_CRI							
Type	RO										RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:6	Reserved0	Reserved
5:0	CQHCI_CRI	Last Command Response index This field stores the index of the last received command response. CQE shall update the value every time a command response is received.

1123085C CQCRA eMMC51 CQHCI features 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CQHCI_CRA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CQHCI_CRA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CQHCI_CRA	Last Command Response Argument This field stores the argument of the last received command. CQE shall update the value every time a command response is received.

3.2 Serial Peripheral Interface (SPI) Master

3.2.1 Register Definition

Module name: spi0 Base address: (+0x11007000)

Module name: spi1 Base address: (+0x11008000)

Module name: spi2 Base address: (+0x11009000)

Address	Name	Width	Register Function
11007000	<u>SPI_CFG0</u>	32	SPI configuration 0 register
11007004	<u>SPI_CFG1</u>	32	SPI configuration 1 register
11007008	<u>SPI_TX_SRC</u>	32	SPI TX source address register
1100700C	<u>SPI_RX_DST</u>	32	SPI RX destination address register
11007010	<u>SPI_TX_DATA</u>	32	SPI TX data FIFO
11007014	<u>SPI_RX_DATA</u>	32	SPI RX data FIFO
11007018	<u>SPI_CMD</u>	32	SPI command register
1100701C	<u>SPI_IRQ</u>	32	SPI IRQ register
11007020	<u>SPI_STATUS</u>	32	SPI status register
11007028	<u>SPI_CFG2</u>	32	SPI configuration 2 register
1100702C	<u>SPI_TX_EXT_ADDR</u>	32	SPI DMA TX source extend address
11007030	<u>SPI_RX_EXT_ADDR</u>	32	SPI DMA RX source extend address
11007040	<u>SPI_CFG3</u>	32	SPI configuration 3 register

11007000 SPI_CFG0 SPI configuration 0 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CS_SETUP_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CS_HOLD_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	CS_SETUP_COUNT	Chip select setup time = (CS_SETUP_COUNT + 1)*CLK_PERIOD; CLK_PERIOD is the cycle time of the clock SPI engine adopts.
15:0	CS_HOLD_COUNT	Chip select hold time = (CS_HOLD_COUNT+1)*CLK_PERIOD

11007004 SPI_CFG1 SPI configuration 1 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PACKET_LENGTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PACKET_LOOP_CNT								CS_IDLE_COUNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PACKET_LENGTH	Packet length The transmission on the SPI bus consists up unit bytes. Hence, PACKET_LENGTH[15:0] define the number of bytes in one packet. Number of bytes in one packet = PACKET_LENGTH + 1
15:8	PACKET_LOOP_CNT	PACKET_LENGTH[15:0] define the number of bytes in one packet; PACKET_LOOP_CNT[7:0] define the number of packets within one transaction. Number of bytes in one packet = PACKET_LENGTH + 1 Number of packets in one transaction = PACKET_LOOP_CNT + 1 Total bytes of one transaction = (PACKET_LENGTH + 1)*(PACKET_LOOP_CNT + 1)
7:0	CS_IDLE_COUNT	Chip select idle time between consecutive transaction = (CS_IDLE_COUNT + 1)*CLK_PERIOD

11007008 SPI_TX_SRC SPI TX source address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_TX_SRC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_TX_SRC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPI_TX_SRC	If TX_DMA_EN is set, the data to be put on the MOSI line will be kept in memory in advance, and the SPI controller will automatically read the data from memory. SPI_TX_SRC defines the memory address from which SPI controller starts to read data.

1100700C SPI_RX_DST SPI RX destination address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_RX_DST															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_RX_DST															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPI_RX_DST	If RX_DMA_EN is set, the received data from the MISO line will be moved to memory automatically by the SPI controller. SPI_RX_DST defines the memory address to which the SPI controller starts to store data.

11007010 SPI_TX_DATA SPI TX data FIFO 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_TX_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_TX_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPI_TX_DATA	The depth of the TX FIFO is 32*4 bytes. Write to this register will write 4 bytes to TX FIFO. The TX FIFO pointer will automatically move towards the next four bytes. Read from this register will read 4 bytes from FIFO, and the TX FIFO pointer will automatically move towards the next four bytes.

11007014 SPI_RX_DATA SPI RX data FIFO 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_RX_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_RX_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPI_RX_DATA	The depth of the RX FIFO is 32*4 bytes. Read from this register will read 4 bytes from RX FIFO. The RX FIFO pointer will automatically move towards the next four bytes. Write to this register will write 4 bytes to FIFO, and the RX FIFO pointer will automatically move towards the next four bytes.

11007018 SPI_CMD SPI command register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								GET_TICK_DLY			SPIM_LOOP		NONIDLE_MODE	CS_PIN_SEL	PAUSE_IE	FINISH_IE
Type								RW			RW		RW	RW	RW	RW
Reset								0	0	0	0		0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_ENDIAN	RX_ENDIAN	RXMSBF	TXMSBF	TX_DMA_EN	RX_DMA_EN	CPOL	CPHA	CS_POL	SAMPLE_SEL	CS_DEASSERT_EN	PAUSE_EN		RST	RESUME	CMD_ACT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
24:22	GET_TICK_DLY	If the speed of SPI is not fast enough, these three bits can help tolerate get_tick timing. The timing range between get_tick is one cycle depending on the SPI system clock.
21	SPIM_LOOP	Set up SPM_LOOP, and MISO will connect to MOSI.
19	NONIDLE_MODE	Set NONIDLE_MODE = 1, and SPI will transfer without idle time until the packet length is done.
18	CS_PIN_SEL	Selects the CS pin to use If enabled, the CS pin will depend on reg_CS_POL. 0: Select CS_N 1: Select GPIO
17	PAUSE_IE	Interrupt enable bit of the pause flag in SPI status register
16	FINISH_IE	Interrupt enable bit of the finish flag in SPI status register
15	TX_ENDIAN	Defines whether to reverse the endian order of the data DMA from memory Only supported in DMA mode. 0: Not reverse (default)
14	RX_ENDIAN	Defines whether to reverse the endian order of the data DMA to memory 0: Not reverse (default)
13	RXMSBF	Indicates data received from MISO line is MSB first or not Set RXMSBF to 1 for MSB first; otherwise set it to 0.
12	TXMSBF	Indicates data sent on MOSI line is MSB first or not Set TXMSBF to 1 for MSB first; otherwise set it to 0.
11	TX_DMA_EN	DMA mode enable bit of the data to be transmitted 0: Not enabled (default)

Bit(s)	Name	Description
10	RX_DMA_EN	DMA mode enable bit of the data received 0: Not enabled (default)
9	CPOL	Control bit of SCK polarity 0: CPOL = 0 1: CPOL = 1
8	CPHA	Defines SPI Clock Format 0 or SPI Clock Format 1 during transmission 0: CPHA = 0 1: CPHA = 1
7	CS_POL	Control bit of chip select polarity revert 0: Active low 1: Active high
6	SAMPLE_SEL	Control bit of sample edge of MISO 0: Positive edge 1: Negative edge
5	CS_DEASSERT_EN	Enable bit of chip select deassertion mode Set this to 1 to enable this mode.
4	PAUSE_EN	Enable bit of pause mode Set this to 1 to enable this mode.
2	RST	Software reset bit When this is active, all modules of SPI except for SPI registers will be reset. When this bit is 1, software reset will be active high. Default: 0
1	RESUME	Used when controller is in PAUSE IDLE state Write 1 to this bit to trigger the SPI controller to resume transfer from PAUSE IDLE state.
0	CMD_ACT	Command activate bit Write 1 to this bit to trigger the SPI controller to start the transaction.

1100701C **SPI_IRQ** **SPI IRQ register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	FINISH
Type															RC	RC
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	Interrupt status bit in pause mode Will be set by the SPI controller when it completes the transaction, entering the PAUSE IDLE state.
0	FINISH	Interrupt status bit in non-pause mode Will be set by the SPI controller when it completes the transaction, entering the IDLE state.

11007020 **SPI_STATUS** **SPI status register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BUSY
Type																RO
Reset																1

Bit(s)	Name	Description
0	BUSY	Status flag reflecting SPI controller is busy or not This bit is low active; 0 means the SPI controller is busy now. 1'b0: Busy 1'b1: Idle

11007028 **SPI_CFG2** **SPI configuration 2 register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SCK_LOW_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCK_HIGH_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SCK_LOW_COUNT	SCK clock low time = (SCK_LOW_COUNT + 1)*CLK_PERIOD
15:0	SCK_HIGH_COUNT	SCK clock high time = (SCK_HIGH_COUNT + 1)*CLK_PERIOD

1100702C **SPI_TX_EXT_ADDR** **SPI DMA TX source extend address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_TX_EXTEND_ADDR			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DMA_TX_EXTEND_ADDR	SPI DMA read extend base address

11007030 SPI_RX_EXT_ADDR SPI DMA RX source extend address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_RX_EXTEND_ADDR			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DMA_RX_EXTEND_ADDR	SPI DMA write extend base address

11007040 SPI_CFG3 SPI configuration 3 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SPI_DUMMY_BITLEN			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_ADDR_BYTELEN				SPI_CMD_BYTELEN						SPI_NO DATA_ FLAG	SPI_XM ODE_E N	SPI_HA LF_DUP LEX_EN	SPI_HA LF_DUP LEX_DI R	SPI_PIN_MODE	
Type	RW				RW						RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
19:16	SPI_DUMMY_BITLEN	SPI dummy data bit length If you set 0, there will be no dummy data transferred. This register is valid only when SPI_CMD_BYTELEN is not 0.
15:12	SPI_ADDR_BYTELEN	SPI address byte length If you set 0, there will be no address transferred. This register is valid only when SPI_CMD_BYTELEN is not 0.
11:8	SPI_CMD_BYTELEN	SPI command byte length If you set 0, there will be no command transferred.
5	SPI_NODATA_FLAG	SPI data phase flag bit If you set 1, there will be no data phase transferred when packet_length is 0.
4	SPI_XMODE_EN	SPI XMODE enable bit If XMODE is enabled, the address phase and dummy data phase will be transferred in single mode. Otherwise, they will be transferred in the same pin mode as data phase. 0: Disable 1: Enable
3	SPI_HALF_DUPLEX_EN	SPI half-duplex mode enable bit 0: Disable 1: Enable
2	SPI_HALF_DUPLEX_DIR	SPI transfer direction for half-duplex mode This bit is valid for single, dual or quad mode half-duplex. 0: TX 1: RX
1:0	SPI_PIN_MODE	SPI pin mode 0: Single mode

Bit(s)	Name	Description
		1: Dual mode
		2: Quad mode

3.3 NAND Flash Interface (NFI)

3.3.1 Register Definition

Module name: NFI Base address: (+0x1100_1000)

Address	Name	Width	Register Function
11001000	<u>NFI_CNFG</u>	16	NFI configuration
11001004	<u>NFI_PAGEFMT</u>	32	NFI page format control register
11001008	<u>NFI_CON</u>	32	NFI operation control register
1100100C	<u>NFI_ACCCON</u>	32	NAND flash access Timing control register
11001010	<u>NFI_INTR_EN</u>	32	NFI interrupt enable register
11001014	<u>NFI_INTR</u>	32	NFI interrupt status register
11001020	<u>NFI_CMD</u>	32	NFI command register
11001030	<u>NFI_ADDRNOB</u>	32	NFI address length register
11001034	<u>NFI_COLADDR</u>	32	NFI column address register
11001038	<u>NFI_ROWADDR</u>	32	NFI row address register
11001040	<u>NFI_STRDATA</u>	16	NFI data transfer start trigger register
11001044	<u>NFI_CNRNB</u>	16	NFI check NAND ready/busy register
11001050	<u>NFI_DATAW</u>	32	NFI Write data buffer
11001054	<u>NFI_DATAR</u>	32	NFI read data buffer
11001058	<u>NFI_PIO_DIRDY</u>	16	PIO_mode data ready register
11001060	<u>NFI_STA</u>	32	NFI state
11001064	<u>NFI_FIFOSTA</u>	16	NFI FIFO status
11001070	<u>NFI_ADDR CNTR</u>	32	NFI page address counter register
11001080	<u>NFI_STRADDR</u>	32	NFI AHB start address register
11001084	<u>NFI_BYTELEN</u>	32	NFI DMA byte length register
11001090	<u>NFI_CSEL</u>	16	NFI device select register
11001094	<u>NFI_IOCON</u>	32	NFI IO control register
110010A0	<u>NFI_FDM0L</u>	32	NFI least FDM data for sector 0 register
110010A4	<u>NFI_FDM0M</u>	32	NFI most FDM data for sector 0 register
110010A8	<u>NFI_FDM1L</u>	32	NFI least FDM data for sector 1 register
110010AC	<u>NFI_FDM1M</u>	32	NFI most FDM data for sector 1 register
110010B0	<u>NFI_FDM2L</u>	32	NFI least FDM data for sector 2 register
110010B4	<u>NFI_FDM2M</u>	32	NFI most FDM data for sector 2 register
110010B8	<u>NFI_FDM3L</u>	32	NFI least FDM data for sector 3 register
110010BC	<u>NFI_FDM3M</u>	32	NFI most FDM data for sector 3 register
110010C0	<u>NFI_FDM4L</u>	32	NFI least FDM data for sector 4 register
110010C4	<u>NFI_FDM4M</u>	32	NFI most FDM data for sector 4 register
110010C8	<u>NFI_FDM5L</u>	32	NFI least FDM data for sector 5 register
110010CC	<u>NFI_FDM5M</u>	32	NFI most FDM data for sector 5 register
110010D0	<u>NFI_FDM6L</u>	32	NFI least FDM data for sector 6 register
110010D4	<u>NFI_FDM6M</u>	32	NFI most FDM data for sector 6 register
110010D8	<u>NFI_FDM7L</u>	32	NFI least FDM data for sector 7 register
110010DC	<u>NFI_FDM7M</u>	32	NFI most FDM data for sector 7 register
110010E0	<u>NFI_FDM8L</u>	32	NFI least FDM data for sector 8 register
110010E4	<u>NFI_FDM8M</u>	32	NFI most FDM data for sector 8 register
110010E8	<u>NFI_FDM9L</u>	32	NFI least FDM data for sector 9 register
110010EC	<u>NFI_FDM9M</u>	32	NFI most FDM data for sector 9 register
110010F0	<u>NFI_FDMAL</u>	32	NFI least FDM data for sector A register

Address	Name	Width	Register Function
110010F4	<u>NFI_FDMAM</u>	32	NFI most FDM data for sector A register
110010F8	<u>NFI_FDMBL</u>	32	NFI least FDM data for sector B register
110010FC	<u>NFI_FDMBM</u>	32	NFI most FDM data for sector B register
11001100	<u>NFI_FDMCL</u>	32	NFI least FDM data for sector C register
11001104	<u>NFI_FDMCM</u>	32	NFI most FDM data for sector C register
11001108	<u>NFI_FDMDL</u>	32	NFI least FDM data for sector D register
1100110C	<u>NFI_FDMDM</u>	32	NFI most FDM data for sector D register
11001110	<u>NFI_FDMEL</u>	32	NFI least FDM data for sector E register
11001114	<u>NFI_FDMEM</u>	32	NFI most FDM data for sector E register
11001118	<u>NFI_FDMFL</u>	32	NFI least FDM data for sector F register
1100111C	<u>NFI_FDMFM</u>	32	NFI most FDM data for sector F register
11001120	<u>NFI_CRC01</u>	32	NFI CRC data for sectors 0 and 1 register
11001124	<u>NFI_CRC23</u>	32	NFI CRC data for sectors 2 and 3 register
11001128	<u>NFI_CRC45</u>	32	NFI CRC data for sectors 4 and 5 register
1100112C	<u>NFI_CRC67</u>	32	NFI CRC data for sectors 6 and 7 register
11001130	<u>NFI_CRC89</u>	32	NFI CRC data for sectors 8 and 9 register
11001134	<u>NFI_CRCAB</u>	32	NFI CRC data for sectors A and B register
11001138	<u>NFI_CRC CD</u>	32	NFI CRC data for sectors C and D register
1100113C	<u>NFI_CRCEF</u>	32	NFI CRC data for sectors E and F register
11001190	<u>NFI_FIFODATA0</u>	32	NFI FIFO content data 0
11001194	<u>NFI_FIFODATA1</u>	32	NFI FIFO content data 1
11001198	<u>NFI_FIFODATA2</u>	32	NFI FIFO content data 2
1100119C	<u>NFI_FIFODATA3</u>	32	NFI FIFO content data 3
11001200	<u>NFI_MCON</u>	16	NFI LCD monitor control register
11001204	<u>NFI_TOTALCNT</u>	32	NFI LCD monitor total cycle count
11001208	<u>NFI_RQCNT</u>	32	NFI LCD monitor request cycle count
1100120C	<u>NFI_ACCNT</u>	32	NFI LCD monitor access cycle count
11001220	<u>NFI_DEBUG_CON1</u>	32	NFI debug register
11001224	<u>NFI_MASTER_STA</u>	32	NFI master status
11001228	<u>NFI_MASTER_RST</u>	32	NFI master control register
1100122C	<u>NFI_SECCUS_SIZE</u>	32	Customized size for the last sector
11001230	<u>NFI_SPIADDR CNTR</u>	32	NFI AHB start address register
11001234	<u>NFI_SPIBYTELEN</u>	32	NFI DMA byte length register
11001238	<u>NFI_RANDOM_CNFG</u>	32	Randomizer configuration
1100123C	<u>NFI_ENMPTY_THRESH</u>	32	Empty threshold setting
11001240	<u>NFI_NAND_TYPE_CNFG</u>	32	Asynchronous interface and timing mode setting
1100124C	<u>RANDOM_TSB_SEED0</u>	32	TOSHIBA seed0
11001250	<u>RANDOM_TSB_SEED1</u>	32	TOSHIBA seed1
11001254	<u>RANDOM_TSB_SEED2</u>	32	TOSHIBA seed2
11001258	<u>RANDOM_TSB_SEED3</u>	32	TOSHIBA seed3
1100125C	<u>RANDOM_TSB_SEED4</u>	32	TOSHIBA seed4
11001260	<u>RANDOM_TSB_SEED5</u>	32	TOSHIBA seed5
11001264	<u>RANDOM_TSB_SEED6</u>	32	TOSHIBA seed6
11001268	<u>RANDOM_TSB_SEED7</u>	32	TOSHIBA seed7
1100126C	<u>RANDOM_TSB_SEED8</u>	32	TOSHIBA seed8
11001270	<u>RANDOM_TSB_SEED9</u>	32	TOSHIBA seed9
11001274	<u>RANDOM_TSB_SEED10</u>	32	TOSHIBA seed10
11001278	<u>RANDOM_TSB_SEED11</u>	32	TOSHIBA seed11
1100127C	<u>RANDOM_TSB_SEED12</u>	32	TOSHIBA seed12

Address	Name	Width	Register Function
11001280	<u>RANDOM_TSB_SEED13</u>	32	TOSHIBA seed13
11001284	<u>RANDOM_TSB_SEED14</u>	32	TOSHIBA seed14
11001288	<u>RANDOM_TSB_SEED15</u>	32	TOSHIBA seed15
11001298	<u>NFI_BUS_CFG</u>	32	NFI BUS configure register
11001490	<u>NFI_FLUSH</u>	32	NFI software reset status
11001500	<u>SNF_MAC_CTL</u>	32	Serial NAND flash MAC mode control
11001504	<u>SNF_MAC_OUTL</u>	32	Serial NAND flash MAC mode output data length
11001508	<u>SNF_MAC_INL</u>	32	Serial NAND flash MAC mode input data length
1100150C	<u>SNF_RD_CTL1</u>	32	Serial NAND flash read control 1
11001510	<u>SNF_RD_CTL2</u>	32	Serial NAND flash read control 2
11001514	<u>SNF_RD_CTL3</u>	32	Serial NAND flash read control 3
11001518	<u>SNF_GF_CTL1</u>	32	Serial NAND flash get feature control 1
11001520	<u>SNF_GF_CTL3</u>	32	Serial NAND flash get feature control3
11001524	<u>SNF_PG_CTL1</u>	32	Serial NAND flash program control1
11001528	<u>SNF_PG_CTL2</u>	32	Serial NAND flash program control2
1100152C	<u>SNF_PG_CTL3</u>	32	Serial NAND flash program control3
11001530	<u>SNF_ER_CTL</u>	32	Serial NAND flash erase control
11001534	<u>SNF_ER_CTL2</u>	32	Serial NAND flash erase control 2
11001538	<u>SNF_MISC_CTL</u>	32	Serial NAND flash MISC control
1100153C	<u>SNF_MISC_CTL2</u>	32	Serial NAND flash MISC control 2
11001540	<u>SNF_DLY_CTL1</u>	32	Serial NAND flash delay control setting 1
11001544	<u>SNF_DLY_CTL2</u>	32	Serial NAND flash delay control setting 2
11001548	<u>SNF_DLY_CTL3</u>	32	Serial NAND flash control setting 3
1100154C	<u>SNF_DLY_CTL4</u>	32	Serial NAND flash delay control setting 4
11001550	<u>SNF_STA_CTL1</u>	32	Serial NAND flash status1 register
11001554	<u>SNF_STA_CTL2</u>	32	Serial NAND flash status2 register
11001558	<u>SNF_STA_CTL3</u>	32	Serial NAND flash status3 register
1100155C	<u>SNF_SNF_CNFG</u>	32	SPI/Parallel NAND selection
11001560	<u>SNF_DEBUG_SEL</u>	32	DEBUG MUX selection
11001800	<u>SPI_GPRAM_ADDR</u>	32	GPRAM start address

11001000		NFI_CNFG			NFI configuration												00000020		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name																			
Type																			
Reset																			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name		OP_MODE						AUTO_FMT_EN	HW_EC_C_EN	CRC_EN	BYTE_RW		RESEED_SEC_EN		DMA_BURST_EN	READ_MODE	DMA_MODE		
Type		RW						RW	RW	RW	RW		RW		RW	RW	RW		
Reset		0	0	0			0	0	0	0		0		0	0	0			

Bit(s)	Name	Description
14:12	OP_MODE	The field controls the operating process flow of FSM for NFI. 000b: Idle state. 001b: Read Process. Recommend for basic read operation. 010b: Single Read Process. Recommend for read ID and read status. 011b: Program Process. Recommend for basic program operation. 100b: Erase Process. Recommend for basic erase operation. 101b: Reset Process. Recommend for basic reset operation. 110b: Custom Process. Recommend for all advance operations. Others: Reserved.
9	AUTO_FMT_EN	Automatic HW ECC encode or decode enable. If enabled, the ECC parity from HW ECC engine and FDM data from Register are written automatically to the spare area. If disabled, the spare data all come from PIO register, like DATAR, DATAW, (PIO Mode) or come from the memory (DMA Mode) as main area data.
8	HW_ECC_EN	This field is used to enable encoding or decoding operation of HW ECC engine. If the bit is enabled, the data is transferring to ECC engine for encoding and decoding. The ECC Engine should be configured as NFI encoding mode; otherwise, the NFI will hang.
7	CRC_EN	Enables CRC data auto generation after main data and FDM data.
6	BYTE_RW	Enables byte access. The valid bytes read from NFI_DATAR and NFI_DATAW are only DR0 and DW0 if BYTE_RW is enabled.
4	RESEED_SEC_EN	If this bit is enabled, HW will reload initial seed to randomizer for each sector; otherwise reload seed for each page 0: Reseed for each page 1: Reseed for each sector
2	DMA_BURST_EN	When NFI is in DMA mode, single and burst (incremental) trans type are used. If start address is not aligned, single trans will be auto issued till address is alignment when DMA_BURST_EN is enabled in DMA mode.

Bit(s)	Name	Description
		0: DMA burst transaction disable 1: DMA burst transaction enable
1	READ_MODE	This field is used to control the activity of read or write transfer. 0: Write operation of DMA or PIO. 1: Read operation of DMA or PIO.
0	DMA_MODE	This field is used to control the operation mode. 0: PIO mode. All data (include read or write) are moved by MCU through APB access. 1: DMA mode. All data (include read or write) are moved by HW automation through AHB.

11001004 NFI_PAGEFMT NFI page format control register 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											SPARE_SIZE					
Type											RW					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM_ECC_NUM				FDM_NUM								DBYTE EN	SEC_SE L_512	DATA_AREA_P AGE_SIZE	
Type	RW				RW								RW	RW	RW	
Reset	0	0	0	0	0	0	0	0					0	1	0	0

Bit(s)	Name	Description
21:16	SPARE_SIZE	The fields represent the spare size value for each sector. If sec_size is 1K (sel_sec_512 is 0), spare size will be doubled. 0000b: 16 bytes 0001b: 26 bytes 0010b: 27 bytes 0011b: 28 bytes 0100b: 32 bytes 0101b: 36 bytes 0110b: 40 bytes 0111b: 44 bytes 1000b: 48 bytes 1001b: 49 bytes 1010b: 50 bytes 1011b: 51 bytes 1100b: 52 bytes 1101b: 62 bytes 1110b: 61 bytes 1111b: 63 bytes 10000b: 64 bytes 10001b: 67 bytes 10010b: 74 bytes
15:12	FDM_ECC_NUM	The number of each FDM data for HW ECC protection. The valid number of bytes ranges is from 0 to 8.
11:8	FDM_NUM	The FDM data number for each spare area. The valid number of bytes is from 0 to 8.

Bit(s)	Name	Description
3	DBYTE_EN	16-bit I/O bus interface enable. 1: 16bits IOBUS 0: 8bits IOBUS
2	SEC_SEL_512	sec_size select. 1: Sec size 512B 0: Sec size 1024B
1:0	DATA_AREA_PAGE_SIZE	Page Size of Data area. (The real page size will including data area and (spare_size* sec_num) bytes spare area). The field specifies the size of one page for the device. Some most widely used page size are supported. 00b: The page size is 512B if sel_sec_size is 1, otherwise page size is 2 KB. 01b: The page size is 2KB if sel_sec_size is 1, otherwise page size is 4 KB. 10b: The page size is 4KB if sel_sec_size is 1, otherwise page size is 8 KB. 11b: Reserved if sel_sec_size is 1, otherwise page size is 16 KB.

11001008 NFI_CON NFI operation control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SEC_NUM
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEC_NUM						BWR	BRD	NOB			SRD			NFI_RST	FIFO_FLUSH
Type	RW						RW	RW	RW			WO			WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Name	Description
16:12	SEC_NUM	The field represents the sector number to be retrieved from the device or DMA Master. The valid number ranges from 1 to 16.
9	BWR	Burst write mode. Setting to be logic-1 enables the data burst write operation.
8	BRD	Burst read mode. Setting this field to be logic-1 enables the data read operation. The NFI core will issue read cycles to retrieve data from the device when the data FIFO is not full or the device is not in the busy state. The NFI core supports consecutive page reading.
7:5	NOB	The field represents the number of bytes to be retrieved from the device in single mode, and the number of bytes per APB transaction in both single and burst mode. 0: Read 8 bytes from the device. 1: Read 1 byte from the device. 2: Read 2 bytes from the device. 3: Read 3 bytes from the device. 4: Read 4 bytes from the device. 5: Read 5 byte from the device. 6: Read 6 bytes from the device. 7: Read 7 bytes from the device.
4	SRD	Setting to be logic-1 initializes the one-shot data read operation. It's mainly used for read ID and read status command, which requires no more than 4 read cycles to retrieve data from the device. It used when FIFO is empty or after reset nfc core.
1	NFI_RST	Resets state machines, data FIFO (0x0000) and FDM data (0xffff) One pulse valid.
0	FIFO_FLUSH	Flushes data FIFO. One pulse valid.

1100100C NFI_ACCCON NAND flash access Timing control register F3FFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	POECS				PRECS						C2R					
Type	RW				RW						RW					
Reset	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W2R				WH				WST				RLT			
Type	RW				RW				RW				RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:28	POECS	The field represents the minimum required time for CS post-pulling down after the access to device. Minimum required time = $\text{PRECS}[1:0] + \text{PRECS}[2]*8 + \text{PRECS}[3]*64$ (T)
27:22	PRECS	The field represents the minimum required time for CS pre-pulling down before any access to device. Minimum required time = $\text{PRECS}[1:0] + \text{PRECS}[3:2]*8 + \text{PRECS}[5:4]*128$ (T)
21:16	C2R	The field represents the minimum required time from NCEB low to NREB low. It's in unit of 2T. Minimum required time = $\text{C2R}[5:0]*2 + 1$ (T)
15:12	W2R	The field represents the minimum required time from NWEB high to NREB low. It's in unit of 2T. So the actual time ranges from 0T to 30T in step of 2T. Minimum required time = $\text{W2R}[3:0]*2 + 1$ (T)
11:8	WH	Write-enable hold-time. The field specifies the hold time of NALE, NCLE, NCEB signals relative to the rising edge of NWEB. This field is associated with WST to expand the write cycle time, and is associated with RLT to expand the read cycle time. 00b: No wait state. 01b: 1T wait state. 10b: 2T wait state. 11b: 3T wait state.
7:4	WST	Write Wait State The field specifies the wait states to be inserted to meet the requirement of the pulse width of the NWEB signal. 00b: No wait state. 01b: 1T wait state. 10b: 2T wait state. 11b: 3T wait state.

Bit(s)	Name	Description
3:0	RLT	Read Latency Time The field specifies how many wait states to be inserted to meet the requirement of the read access time (tREA) for the device. 00b: No wait state. 01b: 1T wait state. 10b: 2T wait state. 11b: 3T wait state.

11001010 NFI_INTR_EN NFI interrupt enable register 80000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NFI_IRQ_INTR_EN															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ALL_READ_INTR_EN	EARLY_READ_INTR_EN	AUTO_BLK_ERASE_INTR_EN	AUTO_READ_INTR_EN	AUTO_PROGRAM_INTR_EN	CUSTOM_READ_INTR_EN	CUSTOM_PROGRAM_INTR_EN	AHB_DONE_EN	ACCESS_LOCK_EN	BUSY_RETURN_EN	ERASE_DONE_EN	RESET_DONE_EN	WR_DONE_EN	RD_DONE_EN
Type			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	NFI_IRQ_INTR_EN	For enable NFI all IRQ event can trigger CPU IRQ process; if 0, you can only get NFI IRQ status by read register.
13	ALL_READ_INTR_EN	The all read interrupt enable.
12	EARLY_READ_INTR_EN	The early read interrupt enable.
11	AUTO_BLK_ERASE_INTR_EN	The done interrupt enable for SPI auto block erase
10	AUTO_READ_INTR_EN	The done interrupt enable for SPI auto read
9	AUTO_PROGRAM_INTR_EN	The done interrupt enable for SPI auto program
8	CUSTOM_READ_INTR_EN	The done interrupt enable for SPI custom read
7	CUSTOM_PROGRAM_INTR_EN	The done interrupt enable for SPI custom program
6	AHB_DONE_EN	The done interrupt enable for DMA mode.
5	ACCESS_LOCK_EN	The NFI access locked interrupt enable.
4	BUSY_RETURN_EN	The busy return interrupt enable.
3	ERASE_DONE_EN	The erase completion interrupt enable.
2	RESET_DONE_EN	The reset completion interrupt enable.
1	WR_DONE_EN	The single page write completion interrupt enable.
0	RD_DONE_EN	The single page read completion interrupt enable.

11001014 NFI_INTR NFI interrupt status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ALL_READ_INTR	EARLY_READ_INTR	AUTO_BLK_ERASE_INTR	AUTO_READ_INTR	AUTO_PROGRAM_INTR	CUSTOM_READ_INTR	CUSTOM_PROGRAM_INTR	AHB_DONE	ACCESS_LOCK	BUSY_RETURN	ERASE_DONE	RESET_DONE	WR_DONE	RD_DONE
Type			RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	ALL_READ_INTR	Indicates that the all reads are completed.
12	EARLY_READ_INTR	Indicates that the early read is completed.
11	AUTO_BLK_ERASE_INTR	Indicates that the SPI auto erase is completed.
10	AUTO_READ_INTR	Indicates that the SPI auto read is completed.
9	AUTO_PROGRAM_INTR	Indicates that the SPI auto program is completed.
8	CUSTOM_READ_INTR	Indicates that the SPI custom read is completed.
7	CUSTOM_PROGRAM_INTR	Indicates that the SPI custom program is completed.
6	AHB_DONE	Indicates that the AHB operation is completed.
5	ACCESS_LOCK	Indicates that the NFI access locked operation is completed.
4	BUSY_RETURN	Indicates that the device state returns from busy by inspecting the R/B# pin.
3	ERASE_DONE	Indicates that the erase operation is completed.
2	RESET_DONE	Indicates that the reset operation is completed.
1	WR_DONE	Indicates that the write operation is completed.
0	RD_DONE	Indicates that the single page read operation is completed.

11001020 NFI_CMD NFI command register 00004545

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PROG_CMD2								CMD							
Type	RW								RW							
Reset	0	1	0	0	0	1	0	1	0	1	0	0	0	1	0	1

Bit(s)	Name	Description
15:8	PROG_CMD2	Program Command word (Only used in program IRQ improvement)
7:0	CMD	Command word.

11001030 NFI_ADDRNOB NFI address length register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										ROW_ADDR_NOB				COL_ADDR_NOB		
Type										RW				RW		
Reset										0	0	0		0	0	0

Bit(s)	Name	Description
6:4	ROW_ADDR_NOB	Number of bytes for the row address
2:0	COL_ADDR_NOB	Number of bytes for the column address

11001034 NFI_COLADDR NFI column address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COL_ADDR3								COL_ADDR2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COL_ADDR1								COL_ADDR0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	COL_ADDR3	The 3-th column address byte.
23:16	COL_ADDR2	The 2-th column address byte.
15:8	COL_ADDR1	The 1-th column address byte.
7:0	COL_ADDR0	The 0-th column address byte.

11001038 NFI_ROWADDR NFI row address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ROW_ADDR3								ROW_ADDR2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ROW_ADDR1								ROW_ADDR0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	ROW_ADDR3	The 3-th row address byte.
23:16	ROW_ADDR2	The 2-th row address byte.
15:8	ROW_ADDR1	The 1-th row address byte.
7:0	ROW_ADDR0	The 0-th row address byte.

11001040 NFI_STRDATA NFI data transfer start trigger register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STR_D ATA
Type																WO
Reset																0

Bit(s)	Name	Description
0	STR_DATA	This signal triggers the data transfer for read or write. It only takes effect as custom operation mode.

11001044 NFI_CNRNB NFI check NAND ready/busy register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CB2R_TIME							STR_C NRNB
Type									RW							WO
Reset									0	0	0	0				0

Bit(s)	Name	Description
7:4	CB2R_TIME	This time-out registers for polling the NAND busy/ready signal. The unit is 16T clock cycles. The clock rate is 61.44 MHz in normal mode. It will be slowed down after enabling HW DCM mode.
0	STR_CNRNB	This signal triggers NFI to poll the status of the NAND busy/ready signal after CB2R_TIME*16 cycles. This function is used to avoid the fail function of "BUSY2READY" status or "BUSY_RETURN" interrupt when NAND is operating at very low frequency (<7MHz). If NAND is operating in lower frequency, the sampling for the event, NAND busy/ready signal from low to high, may be failed and NFI will be hung in busy state. This signal is a time-out register to check the NAND status. The results will be reported to "BUSY2READY" status and "BUSY_RETURN" interrupt.

11001050 NFI_DATAW NFI Write data buffer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DW3								DW2							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW1								DW0							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DW3	Write data byte 3.
23:16	DW2	Write data byte 2.
15:8	DW1	Write data byte 1.
7:0	DW0	Write data byte 0.

11001054 NFI_DATAW NFI read data buffer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DR3								DR2							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DR1								DR0							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DR3	Read data byte 3.
23:16	DR2	Read data byte 2.
15:8	DR1	Read data byte 1.
7:0	DR0	Read data byte 0.

11001058 NFI_PIO_DIRDY PIO_mode data ready register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PIO_DI_RDY
Type																RO
Reset																1

Bit(s)	Name	Description
0	PIO_DI_RDY	Indicates the PIO mode is ready for read data in read mode and ready for write data in write mode. 0: NFI_DATAR and NFI_DATAW should not be read or written (not ready). 1: NFI is ready for reading data in ready mode and writing data in write mode.

11001060			NFI_STA		NFI state										00001020			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	NAND_FSM_TY PE		NAND_FSM										NFI_FSM					
Type	RO		RO										RO					
Reset	0	0	0	0	0	0	0	0	0				0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name				READ_emptY			BUSY2_READY	BUSY			FLASH_MACRO_IDLE	ACCESS_LOCK	DATA_W	DATAR	ADDR	CMD		
Type				RO			RO	RO			RO	RO	RO	RO	RO	RO		
Reset				1			0	0			1	0	0	0	0	0		

Bit(s)	Name	Description
31:30	NAND_FSM_TYPE	The field represents the state of NAND interface FSM type: Async state(eif_state[8:7]). 00b: Async_FSM 01b: Reserved 10b: Reserved 11b: Reserved
29:23	NAND_FSM	The field represents the state of NAND interface FSM (eif_state[6:0]). 000000b: IDLE. idle. 111000b: PRE_CS. Pre CS state. 001001b: CMD_WRST. Command write set up 001010b: CMD_WR. Command write enable. 001011b: CMD_WRHD. Command write hold. 001000b: CMD_WRRDY 010001b: ADDR_WRST. Address write set up 0100010b: ADDR_WR. Address write enable 0100011b: ADDR_WRHD. Address write hold 0101111b: ADDR_WRRDY. 0111111b: CA2DEXT. Command address write extension. 1001100b: DATA_RDST. Data read set up. 1000010b: DATA_RD. Data read enable. 1000011b: DATA_RDHD. Data read hold. 1101100b: DATA_WRST. Data write set up. 1100010b: DATA_WR. Data write enable. 1100011b: DATA_WRHD. Data write hold.

Bit(s)	Name	Description
		Others: Reserved
19:16	NFI_FSM	The field represents the state of NFI internal FSM (nfi_state[3:0]). 0000b: Idle. 0001b: Reset. Reset command to ready 0010b: Read busy. 0011b: Read data. 0100b: Program busy 0101b: Program data. Input data command to program command 1000b: Erase busy. Erase command to ready 1001b: Erase data. Erase command 1 to erase command 2 1111b: Custom mode 1110b: Custom mode for data access Others: Reserved
12	READ_EMPTY	Empty page indication during read operation, include all data, FDM and parity for all sectors
9	BUSY2READY	It's read-only. This signal indicates NAND from busy to ready state and it will be reset after nfi_reset or write command/address.
8	BUSY	~lat_nrb which synchronized busy signal from the NAND flash device. It's read-only. This signal is sampled from device.
5	FLASH_MACRO_IDLE	This signal indicates flash macro is in idle. Note: Only flash macro is idle, sw reset or NAND interface change can be issued. 1: Idle 0: Non idle
4	ACCESS_LOCK	The access range is locked for erase or program.
3	DATAW	The NFI core is in data write mode (program state[3:0] which is based on eif_state[6:4]).
2	DATAR	The NFI core is in data read mode (program state[3:0] which is based on eif_state[6:4]).
1	ADDR	The NFI core is in address mode (program state[3:0] which is based on eif_state[6:4]).
0	CMD	The NFI core is in command mode (program state[3:0] which is based on eif_state[6:4]).

11001064 NFI_FIFOSTA NFI FIFO status 00004040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WR_FULL	WR_EMPTY	WR_REMAIN						RD_FULL	RD_EMPTY	RD_REMAIN					
Type	RO	RO	RO						RO	RO	RO					
Reset	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
15	WR_FULL	Data FIFO full in burst write mode.
14	WR_EMPTY	Data FIFO empty in burst write mode.
13:8	WR_REMAIN	Data FIFO remaining byte number in burst write mode.
7	RD_FULL	Data FIFO full in burst read mode.
6	RD_EMPTY	Data FIFO empty in burst read mode.
5:0	RD_REMAIN	Data FIFO remaining byte number in burst read mode.

11001070 NFI_ADDR_CNTR NFI page address counter register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SEC_CNTR
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEC_CNTR				SEC_ADDR											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:12	SEC_CNTR	The sector count.
11:0	SEC_ADDR	The address count of 512 main data and spare data for each sector.

11001080 NFI_STRADDR NFI AHB start address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	STR_ADDR	The start address of EMI for both read or write in DMA mode. If start address of any sector data is not 4-byte aligned, the transfer will be automatically split into byte and word transaction by NFI DMA. Non 4-byte aligned data will be transferred in single-byte transaction. Non 16-byte aligned data will be transferred in single-word transaction. 16-byte aligned data will be transferred by 4 word incrementing burst if the NFI_CNFG->DMA_BURST_EN is enabled.

11001084 NFI_BYTELEN NFI DMA byte length register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																BUS_SEC_CNTR
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUS_SEC_CNTR				BUS_SEC_ADDR											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:12	BUS_SEC_CNTR	The sector count.
11:0	BUS_SEC_ADDR	The address count of 512 main data and spare data for each sector.

11001090 NFI_CSEL NFI device select register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CSEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	CSEL	Chip select. The value defaults to 0. 0: Device 0 is selected. 1: Device 1 is selected.

11001094 NFI_IOCON NFI IO control register 00000006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														L2NW	L2NR	NLD_PD
Type														RW	RW	RW
Reset														1	1	0

Bit(s)	Name	Description
2	L2NW	Enables 1T latency for the arbitration from LCD to NAND write operation, this is used to prevent bus contention between chip, NAND flash and LCD device.
1	L2NR	Enables 1T latency for the arbitration from LCD to NAND read operation, this is used to prevent bus contention between chip, NAND flash and LCD device.
0	NLD_PD	Data bus pull down when no use. 0: Disable 1: Enable

110010A0 **NFI_FDM0L** **NFI least FDM data for sector 0 register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM0_3								FDM0_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM0_1								FDM0_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM0_3	The 3-th FDM byte data for sector 0.
23:16	FDM0_2	The 2-th FDM byte data for sector 0.
15:8	FDM0_1	The 1-th FDM byte data for sector 0.
7:0	FDM0_0	The 0-th FDM byte data for sector 0.

110010A4 **NFI_FDM0M** **NFI most FDM data for sector 0 register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM0_7								FDM0_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM0_5								FDM0_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM0_7	The 3-th FDM byte data for sector 0.
23:16	FDM0_6	The 2-th FDM byte data for sector 0.
15:8	FDM0_5	The 1-th FDM byte data for sector 0.
7:0	FDM0_4	The 0-th FDM byte data for sector 0.

110010A8 NFI_FDM1L NFI least FDM data for sector 1 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM1_3								FDM1_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM1_1								FDM1_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM1_3	The 3-th FDM byte data for sector 1.
23:16	FDM1_2	The 2-th FDM byte data for sector 1.
15:8	FDM1_1	The 1-th FDM byte data for sector 1.
7:0	FDM1_0	The 0-th FDM byte data for sector 1.

110010AC NFI_FDM1M NFI most FDM data for sector 1 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM1_7								FDM1_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM1_5								FDM1_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM1_7	The 7-th FDM byte data for sector 1.
23:16	FDM1_6	The 6-th FDM byte data for sector 1.
15:8	FDM1_5	The 5-th FDM byte data for sector 1.
7:0	FDM1_4	The 4-th FDM byte data for sector 1.

110010B0 **NFI_FDM2L** **NFI least FDM data for sector 2 register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM2_3								FDM2_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM2_1								FDM2_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM2_3	The 3-th FDM byte data for sector 2.
23:16	FDM2_2	The 2-th FDM byte data for sector 2.
15:8	FDM2_1	The 1-th FDM byte data for sector 2.
7:0	FDM2_0	The 0-th FDM byte data for sector 2.

110010B4 **NFI_FDM2M** **NFI most FDM data for sector 2 register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM2_7								FDM2_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM2_5								FDM2_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM2_7	The 7-th FDM byte data for sector 2.
23:16	FDM2_6	The 6-th FDM byte data for sector 2.
15:8	FDM2_5	The 5-th FDM byte data for sector 2.
7:0	FDM2_4	The 4-th FDM byte data for sector 2.

110010B8 NFI_FDM3L NFI least FDM data for sector 3 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM3_3								FDM3_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM3_1								FDM3_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM3_3	The 3-th FDM byte data for sector 3.
23:16	FDM3_2	The 2-th FDM byte data for sector 3.
15:8	FDM3_1	The 1-th FDM byte data for sector 3.
7:0	FDM3_0	The 0-th FDM byte data for sector 3.

110010BC NFI_FDM3M NFI most FDM data for sector 3 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM3_7								FDM3_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM3_5								FDM3_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM3_7	The 4-th FDM byte data for sector 3.
23:16	FDM3_6	The 6-th FDM byte data for sector 3.
15:8	FDM3_5	The 5-th FDM byte data for sector 3.
7:0	FDM3_4	The 4-th FDM byte data for sector 3.

110010C0 **NFI_FDM4L** **NFI least FDM data for sector 4 register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM4_3								FDM4_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM4_1								FDM4_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM4_3	The 3-th FDM byte data for sector 4.
23:16	FDM4_2	The 2-th FDM byte data for sector 4.
15:8	FDM4_1	The 1-th FDM byte data for sector 4.
7:0	FDM4_0	The 0-th FDM byte data for sector 4.

110010C4 **NFI_FDM4M** **NFI most FDM data for sector 4 register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM4_7								FDM4_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM4_5								FDM4_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM4_7	The 7-th FDM byte data for sector 4.
23:16	FDM4_6	The 6-th FDM byte data for sector 4.
15:8	FDM4_5	The 5-th FDM byte data for sector 4.
7:0	FDM4_4	The 4-th FDM byte data for sector 4.

110010C8 **NFI_FDM5L** **NFI least FDM data for sector 5 register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM5_3								FDM5_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM5_1								FDM5_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM5_3	The 3-th FDM byte data for sector 5.
23:16	FDM5_2	The 2-th FDM byte data for sector 5.
15:8	FDM5_1	The 1-th FDM byte data for sector 5.
7:0	FDM5_0	The 0-th FDM byte data for sector 5.

110010CC **NFI_FDM5M** **NFI most FDM data for sector 5 register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM5_7								FDM5_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM5_5								FDM5_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM5_7	The 7-th FDM byte data for sector 5.
23:16	FDM5_6	The 6-th FDM byte data for sector 5.
15:8	FDM5_5	The 5-th FDM byte data for sector 5.
7:0	FDM5_4	The 4-th FDM byte data for sector 5.

110010D0 NFI_FDM6L NFI least FDM data for sector 6 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM6_3								FDM6_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM6_1								FDM6_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM6_3	The 3-th FDM byte data for sector 6.
23:16	FDM6_2	The 2-th FDM byte data for sector 6.
15:8	FDM6_1	The 1-th FDM byte data for sector 6.
7:0	FDM6_0	The 0-th FDM byte data for sector 6.

110010D4 NFI_FDM6M NFI most FDM data for sector 6 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM6_7								FDM6_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM6_5								FDM6_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM6_7	The 7-th FDM byte data for sector 6.
23:16	FDM6_6	The 6-th FDM byte data for sector 6.
15:8	FDM6_5	The 5-th FDM byte data for sector 6.
7:0	FDM6_4	The 4-th FDM byte data for sector 6.

110010D8 NFI_FDM7L NFI least FDM data for sector 7 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM7_3								FDM7_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM7_1								FDM7_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM7_3	The 3-th FDM byte data for sector 7.
23:16	FDM7_2	The 2-th FDM byte data for sector 7.
15:8	FDM7_1	The 1-th FDM byte data for sector 7.
7:0	FDM7_0	The 0-th FDM byte data for sector 7.

110010DC NFI_FDM7M NFI most FDM data for sector 7 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM7_7								FDM7_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM7_5								FDM7_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM7_7	The 7-th FDM byte data for sector 7.
23:16	FDM7_6	The 6-th FDM byte data for sector 7.
15:8	FDM7_5	The 5-th FDM byte data for sector 7.
7:0	FDM7_4	The 4-th FDM byte data for sector 7.

110010E0 NFI_FDM8L NFI least FDM data for sector 8 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM8_3								FDM8_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM8_1								FDM8_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM8_3	The 3-th FDM byte data for sector 8.
23:16	FDM8_2	The 2-th FDM byte data for sector 8.
15:8	FDM8_1	The 1-th FDM byte data for sector 8.
7:0	FDM8_0	The 0-th FDM byte data for sector 8.

110010E4 NFI_FDM8M NFI most FDM data for sector 8 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM8_7								FDM8_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM8_5								FDM8_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM8_7	The 7-th FDM byte data for sector 8.
23:16	FDM8_6	The 6-th FDM byte data for sector 8.
15:8	FDM8_5	The 5-th FDM byte data for sector 8.
7:0	FDM8_4	The 4-th FDM byte data for sector 8.

110010E8 NFI_FDM9L NFI least FDM data for sector 9 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM9_3								FDM9_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM9_1								FDM9_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM9_3	The 3-th FDM byte data for sector 9.
23:16	FDM9_2	The 2-th FDM byte data for sector 9.
15:8	FDM9_1	The 1-th FDM byte data for sector 9.
7:0	FDM9_0	The 0-th FDM byte data for sector 9.

110010EC NFI_FDM9M NFI most FDM data for sector 9 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM9_7								FDM9_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM9_5								FDM9_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM9_7	The 7-th FDM byte data for sector 9.
23:16	FDM9_6	The 6-th FDM byte data for sector 9.
15:8	FDM9_5	The 5-th FDM byte data for sector 9.
7:0	FDM9_4	The 4-th FDM byte data for sector 9.

110010F0 **NFI_FDMAL** **NFI least FDM data for sector A register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMA_3								FDMA_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMA_1								FDMA_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMA_3	The 3-th FDM byte data for sector A.
23:16	FDMA_2	The 2-th FDM byte data for sector A.
15:8	FDMA_1	The 1-th FDM byte data for sector A.
7:0	FDMA_0	The 0-th FDM byte data for sector A.

110010F4 **NFI_FDMAM** **NFI most FDM data for sector A register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMA_7								FDMA_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMA_5								FDMA_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMA_7	The 7-th FDM byte data for sector A.
23:16	FDMA_6	The 6-th FDM byte data for sector A.
15:8	FDMA_5	The 5-th FDM byte data for sector A.
7:0	FDMA_4	The 4-th FDM byte data for sector A.

110010F8 **NFI_FDMBL** **NFI least FDM data for sector B register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMB_3								FDMB_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMB_1								FDMB_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMB_3	The 3-th FDM byte data for sector B.
23:16	FDMB_2	The 2-th FDM byte data for sector B.
15:8	FDMB_1	The 1-th FDM byte data for sector B.
7:0	FDMB_0	The 0-th FDM byte data for sector B.

110010FC **NFI_FDMBM** **NFI most FDM data for sector B register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMB_7								FDMB_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMB_5								FDMB_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMB_7	The 7-th FDM byte data for sector B.
23:16	FDMB_6	The 6-th FDM byte data for sector B.
15:8	FDMB_5	The 5-th FDM byte data for sector B.
7:0	FDMB_4	The 4-th FDM byte data for sector B.

11001100 NFI_FDMCL NFI least FDM data for sector C register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMC_3								FDMC_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMC_1								FDMC_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMC_3	The 3-th FDM byte data for sector C.
23:16	FDMC_2	The 2-th FDM byte data for sector C.
15:8	FDMC_1	The 1-th FDM byte data for sector C.
7:0	FDMC_0	The 0-th FDM byte data for sector C.

11001104 NFI_FDMCM NFI most FDM data for sector C register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMC_7								FDMC_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMC_5								FDMC_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMC_7	The 7-th FDM byte data for sector C.
23:16	FDMC_6	The 6-th FDM byte data for sector C.
15:8	FDMC_5	The 5-th FDM byte data for sector C.
7:0	FDMC_4	The 4-th FDM byte data for sector C.

11001108 NFI_FDMDL NFI least FDM data for sector D register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMD_3								FDMD_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMD_1								FDMD_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMD_3	The 3-th FDM byte data for sector D.
23:16	FDMD_2	The 2-th FDM byte data for sector D.
15:8	FDMD_1	The 1-th FDM byte data for sector D.
7:0	FDMD_0	The 0-th FDM byte data for sector D.

1100110C NFI_FDMDM NFI most FDM data for sector D register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMD_7								FDMD_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMD_5								FDMD_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMD_7	The 7-th FDM byte data for sector D.
23:16	FDMD_6	The 6-th FDM byte data for sector D.
15:8	FDMD_5	The 5-th FDM byte data for sector D.
7:0	FDMD_4	The 4-th FDM byte data for sector D.

11001110 NFI_FDMEL NFI least FDM data for sector E register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDME_3								FDME_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDME_1								FDME_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDME_3	The 3-th FDM byte data for sector E.
23:16	FDME_2	The 2-th FDM byte data for sector E.
15:8	FDME_1	The 1-th FDM byte data for sector E.
7:0	FDME_0	The 0-th FDM byte data for sector E.

11001114 NFI_FDMEM NFI most FDM data for sector E register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDME_7								FDME_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDME_5								FDME_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDME_7	The 7-th FDM byte data for sector E.
23:16	FDME_6	The 6-th FDM byte data for sector E.
15:8	FDME_5	The 5-th FDM byte data for sector E.
7:0	FDME_4	The 4-th FDM byte data for sector E.

11001118 **NFI_FDMFL** **NFI least FDM data for sector F register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMF_3								FDMF_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMF_1								FDMF_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMF_3	The 3-th FDM byte data for sector F.
23:16	FDMF_2	The 2-th FDM byte data for sector F.
15:8	FDMF_1	The 1-th FDM byte data for sector F.
7:0	FDMF_0	The 0-th FDM byte data for sector F.

1100111C **NFI_FDMFM** **NFI most FDM data for sector F register** **FFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMF_7								FDMF_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMF_5								FDMF_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMF_7	The 7-th FDM byte data for sector F.
23:16	FDMF_6	The 6-th FDM byte data for sector F.
15:8	FDMF_5	The 5-th FDM byte data for sector F.
7:0	FDMF_4	The 4-th FDM byte data for sector F.

11001120 NFI_CRC01 NFI CRC data for sectors 0 and 1 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRC1_M								CRC1_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRC0_M								CRC0_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	CRC1_M	The Most CRC byte for sector 1.
23:16	CRC1_L	The Least CRC byte for sector 1.
15:8	CRC0_M	The Most CRC byte for sector 0
7:0	CRC0_L	The Least CRC byte for sector 0.

11001124 NFI_CRC23 NFI CRC data for sectors 2 and 3 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRC3_M								CRC3_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRC2_M								CRC2_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	CRC3_M	The Most CRC byte for sector 1.
23:16	CRC3_L	The Least CRC byte for sector 1.
15:8	CRC2_M	The Most CRC byte for sector 0
7:0	CRC2_L	The Least CRC byte for sector 0.

11001128 NFI_CRC45 NFI CRC data for sectors 4 and 5 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRC5_M								CRC5_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRC4_M								CRC4_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	CRC5_M	The Most CRC byte for sector 1.
23:16	CRC5_L	The Least CRC byte for sector 1.
15:8	CRC4_M	The Most CRC byte for sector 0
7:0	CRC4_L	The Least CRC byte for sector 0.

1100112C NFI_CRC67 NFI CRC data for sectors 6 and 7 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRC7_M								CRC7_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRC6_M								CRC6_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	CRC7_M	The Most CRC byte for sector 1.
23:16	CRC7_L	The Least CRC byte for sector 1.
15:8	CRC6_M	The Most CRC byte for sector 0
7:0	CRC6_L	The Least CRC byte for sector 0.

11001130 NFI_CRC89 NFI CRC data for sectors 8 and 9 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRC9_M								CRC9_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRC8_M								CRC8_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	CRC9_M	The Most CRC byte for sector 1.
23:16	CRC9_L	The Least CRC byte for sector 1.
15:8	CRC8_M	The Most CRC byte for sector 0
7:0	CRC8_L	The Least CRC byte for sector 0.

11001134 NFI_CRCAB NFI CRC data for sectors A and B register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRCB_M								CRCB_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRCA_M								CRCA_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	CRCB_M	The Most CRC byte for sector 1.
23:16	CRCB_L	The Least CRC byte for sector 1.
15:8	CRCA_M	The Most CRC byte for sector 0
7:0	CRCA_L	The Least CRC byte for sector 0.

11001138 NFI_CRCCD NFI CRC data for sectors C and D register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRCD_M								CRCD_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRCC_M								CRCC_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	CRCD_M	The Most CRC byte for sector 1.
23:16	CRCD_L	The Least CRC byte for sector 1.
15:8	CRCC_M	The Most CRC byte for sector 0
7:0	CRCC_L	The Least CRC byte for sector 0.

1100113C NFI_CRCEF NFI CRC data for sectors E and F register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRCE_M								CRCE_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRCE_M								CRCE_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	CRCE_M	The Most CRC byte for sector 1.
23:16	CRCE_L	The Least CRC byte for sector 1.
15:8	CRCE_M	The Most CRC byte for sector 0
7:0	CRCE_L	The Least CRC byte for sector 0.

11001190 NFI_FIFODATA0 NFI FIFO content data 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FIFO_DATA0	NFI Data FIFO Content Data 0

11001194 NFI_FIFODATA1 NFI FIFO content data 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FIFO_DATA1	NFI DATA FIFO Content Data 1

11001198 NFI_FIFODATA2 NFI FIFO content data 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FIFO_DATA2	NFI DATA FIFO Content Data 2

1100119C NFI_FIFODATA3 NFI FIFO content data 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FIFO_DATA3	NFI DATA FIFO Content Data 3

11001200 NFI_MCON NFI LCD monitor control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BMCLR	BMSTR
Type															WO	RW
Reset															0	0

Bit(s)	Name	Description
1	BMCLR	Clears NFI-LCD bandwidth monitor register counter
0	BMSTR	Enables NFI-LCD bandwidth monitor
		0: Disable
		1: Enable

11001204 NFI_TOTALCNT NFI LCD monitor total cycle count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NFI_TOTALCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NFI_TOTALCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	NFI_TOTALCNT	The total clock cycle count during enabling NFI-LCD bandwidth monitor

11001208 NFI_RQCNT NFI LCD monitor request cycle count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NFI_RQCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NFI_RQCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	NFI_RQCNT	The request clock cycle count during enabling NFI-LCD bandwidth monitor

1100120C NFI_ACCNT NFI LCD monitor access cycle count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NFI_ACCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NFI_ACCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	NFI_ACCNT	The access clock cycle count during enabling NFI-LCD bandwidth monitor

11001220	NFI_DEBUG_CON1				NFI debug register								00000085			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					rg_cust om_m ode_ir q_imp	rg_early_read_sec_num					rg_pro g_irq_i mp	rg_nre _b_low _dly_e n				
Type					RW	RW					RW	RW				
Reset					0	0	0	0	0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		REG_C E_HOL D	CLK_H OLD					AUTOC _HPRO T_EN	HWDC M_SW CON_E N_VAL		STROBE_SEL			WBUF _EN	HWDC M_SW CON_O N	HWDC M_SW CON_E N
Type		RW	RW					RW	RW		RW			RW	RW	RW
Reset		0	0					0	1		0	0	0	1	0	1

Bit(s)	Name	Description
27	rg_custom_mode_irq_imp	Enables custom mode IRQ improvement, default disable
26:22	rg_early_read_sec_num	This signal indicates that when controller sends early read IRQ, how many sectors are left in one page.
21	rg_prog_irq_imp	Enables program IRQ improvement, default disable
20	rg_nre_b_low_dly_en	To make nre_b low pull low after nce_b low pull low when read mode.
14	REG_CE_HOLD	This bit is used for keeping ce low if there are no data driven out during program data 1'b1: When program data, ce will keep low 1'b0: When program data, ce may release low if no data are driven out
13	CLK_HOLD	This bit is used for keeping ONFI clock active. 1'b1: Non-stop ONFI NAND clock during idle state 1'b0: Stop ONFI clock during idle state
8	AUTOC_HPROT_EN	This reg is used for enable ECC autoc bufferable which is an option for DMA operation of NFI mode. 0: Autoc no bufferable 1: Autoc bufferable
7	HWDCM_SWCON_EN_VAL	When HWDCM_SWCON_EN is enabled, this bit is used to select swcon enable value. 0: NFI is busy. 1: NFI is idle.
5:3	STROBE_SEL	Strobe select 3'b000: Sampling at the rising edge of NREB 3'b001: Sampling at 1 cycle delay of the rising edge of NREB 3'b010: Sampling at 2 cycles delay of the rising edge of NREB

Bit(s)	Name	Description
		3'b011: Sampling at 3 cycles delay of the rising edge of NREB
		3'b100: Sampling at 4 cycles delay of the rising edge of NREB
		3'b101: Sampling at 5 cycles delay of the rising edge of NREB
		3'b110: Sampling at 6 cycles delay of the rising edge of NREB
		3'b111: Sampling at 7 cycles delay of the rising edge of NREB
2	WBUF_EN	Used for enabling AHB hprot[2] for bufferable. 1: Enable hprot control 0: Disable hprot control
1	HWDCM_SWCON_ON	ECC clock gating control while nfiicc is idle and NAND is busy. 1'b0: ECC clock gating disable, ECC clock will not be closed while NFI is working 1'b1: ECC clock gating enable, ECC clock will be closed while ECC is idle and NAND is busy
0	HWDCM_SWCON_EN	Hardware DCM control enable 0: Hardware auto control 1: Software controls DCM by HWDCM_SWCON_EN_VAL

11001224 NFI_MASTER_STA NFI master status 00018044

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														grant_state		
Type														RO		
Reset														0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					hburst_cnt										ahb_bu s_busy	bus_bu sy
Type					RO										RO	RO
Reset					0	0	0	0							0	0

Bit(s)	Name	Description
18:16	grant_state	grant_state means current AHB arb_master states. 3'b001: NFI access 3'b010: autoc access 3'b100: ecc_r access
11:8	hburst_cnt	hburst_cnt means current burst cnt for AHB operation
1	ahb_bus_busy	ahb_bus_busy which means for each AHB burst access busy or not.
0	bus_busy	bus_busy which means NFI internal related req bus busy or not

11001228 NFI_MASTER_RST NFI master control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															macro_ sw_rst	dma_ master _sw_rs t
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	macro_sw_rst	For sw resetting pad_macro whose circuit closes to external device.
0	dma_master_sw_rst	For sw resetting DMA master interface status such as AHB.

1100122C **NFI_SECCUS_SIZE** Customized size for the last sector **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CUS_LAST_SEC_SIZE													CUS_LAST_SEC_SIZE_EN	SECCUS_SIZE_EN	SECCUS_SPIDMA_EN
Type	RW													RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CUS_SEC_SIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	CUS_LAST_SEC_SIZE	The last sector size can be programmable independently when bit 18 is asserted.
18	CUS_LAST_SEC_SIZE_EN	Enables Customized last sector size. Note: The spare_size will be ignored if this feature is enabled.
17	SECCUS_SIZE_EN	Enables Customized sector size. Note: The spare_size will be ignored if this feature is enabled.
16	SECCUS_SPIDMA_EN	Enables Customized sector size for SPI NAND only.
12:0	CUS_SEC_SIZE	The sector size can be programmable when bit 17 is asserted;

11001230 **NFI_SPIADDRCNTR** NFI AHB start address register **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												NF_TSF_SEC				
Type												RO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				NF_TSF_ADDR												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:16	NF_TSF_SEC	The register represents the start address for DMA to access EMI. These memory from the start address is used to put read data from NAND or write data to NAND in DMA mode.
12:0	NF_TSF_ADDR	NF_TSF address

11001234 NFI SPIBYTELEN NFI DMA byte length register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BUS_TSF_SEC			
Type													RO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BUS_TSF_ADDR												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:16	BUS_TSF_SEC	The register represents the current transfer length for DMA to access EMI.
12:0	BUS_TSF_ADDR	BUS_TSF address

11001238 NFI_RANDOM_CNFG Randomizer configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DECODED_SEED															DECODED_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENCODED_SEED															ENCODED_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:17	DECODED_SEED	Randomize decoded seed (for Samsung)
16	DECODED_EN	Randomize decoded enable
15:1	ENCODED_SEED	Randomize encoded seed (for Samsung)
0	ENCODED_EN	Randomize encoded enable (for Samsung and Toshiba)

1100123C NFI_EMPTY_THRESH Empty threshold setting 0000000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ZERO_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EMPTY_THRESH							
Type									RW							
Reset									0	0	0	0	1	0	1	0

Bit(s)	Name	Description
31:16	ZERO_CNT	Zero counter of read data in each read operation (sector/page)
7:0	EMPTY_THRESH	Empty threshold

11001240 NFI NAND TYPE CNFG Asynchronous interface and timing mode setting 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SLC_TY PE	INTERFACE_TY PE	
Type														RO	RW	
Reset														1	0	0

Bit(s)	Name	Description
2	SLC_TYPE	When INTERFACE_TYPE = 2'b00 or 2'b11, then slc_type is 1. 1'b0: MLC 1'b1: SLC
1:0	INTERFACE_TYPE	Interface type configuration 2'b00: Async 2'b01: Toggle 2'b10: Sync 2'b11: Reserved

1100124C RANDOM TSB_SEED0 TOSHIBA seed0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED0	TOSHIBA randomizer seed0

11001250 RANDOM TSB_SEED1 TOSHIBA seed1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED1	TOSHIBA randomizer seed1

11001254 RANDOM TSB_SEED2 TOSHIBA seed2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED2	TOSHIBA randomizer seed2

11001258 RANDOM TSB_SEED3 TOSHIBA seed3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED3	TOSHIBA randomizer seed3

1100125C RANDOM TSB_SEED4 TOSHIBA seed4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED4	TOSHIBA randomizer seed4

11001260 RANDOM TSB_SEED5 TOSHIBA seed5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED5	TOSHIBA randomizer seed5

11001264 RANDOM TSB_SEED6 TOSHIBA seed6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED6	TOSHIBA randomizer seed6

11001268 **RANDOM TSB_SEED7** **TOSHIBA seed7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED7	TOSHIBA randomizer seed7

1100126C **RANDOM TSB_SEED8** **TOSHIBA seed8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED8	TOSHIBA randomizer seed8

11001270 **RANDOM TSB_SEED9** **TOSHIBA seed9** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED9	TOSHIBA randomizer seed9

11001274 RANDOM TSB_SEED10 TOSHIBA seed10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED10	TOSHIBA randomizer seed10

11001278 RANDOM TSB_SEED11 TOSHIBA seed11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED11	TOSHIBA randomizer seed11

1100127C RANDOM TSB_SEED12 TOSHIBA seed12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED12	TOSHIBA randomizer seed12

11001280 RANDOM TSB_SEED13 TOSHIBA seed13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED13	TOSHIBA randomizer seed13

11001284 RANDOM TSB_SEED14 TOSHIBA seed14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED14	TOSHIBA randomizer seed14

11001288 RANDOM TSB_SEED15 TOSHIBA seed15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED15	TOSHIBA randomizer seed15

11001298 NFI_BUS_CFG NFI BUS configure register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					STR_ADDR_EXT											
Type					RW											
Reset					0	0	0	0								

Bit(s)	Name	Description
11:8	STR_ADDR_EXT	Used to extend the NFI_STRADDR register. Indicates the highest 4 bits of start address of EMI for both read or write in DMA mode.

11001490 NFI_FLUSH NFI software reset status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLASH_RESET_ACT
Type																RO
Reset																0

Bit(s)	Name	Description
0	FLASH_RESET_ACT	Controlled by flush_fifo or nfi_reset; reset AHB related status

11001500 SNF_MAC_CTL Serial NAND flash MAC mode control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												MAC_X IO_SEL	SF_MA C_EN	SF_TRI G	WIP_R EADY	WIP
Type												RW	RW	RW	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	MAC_XIO_SEL	MAC mode for QPI/SPI setting 0: SPI 1: QPI
3	SF_MAC_EN	Switches the serial flash control to update the macro. Please set up this bit before triggering the update macro (It is suggested to run MAC mode in internal sysram code because DIRECT/MAC cannot run at the same time. Another way to switch to hardware auto switch mode by setting up MAC_MASK_OP) 0: MAC_MODE Disable 1: MAC MODE Enable (Direct read is forbidden when SF_MAC_EN = 1)
2	SF_TRIG	Serial flash write macro trigger 0: Disable 1: Enable (Fill command sequence I/O length before SF_TRIG)
1	WIP_READY	WIP register status ready for access. WIP_READY exits due to asynchronous latency delay before flash responds to WIP 0: WIP is not ready for read. 1: WIP is ready for read. (Check if WIP_READY = 1 before the next command sequence)
0	WIP	Serial flash command write in process 0: Flash update finished (Check if WIP = 0 before the next command sequence) 1: Not finished

11001504 SNF_MAC_OUTL Serial NAND flash MAC mode output data length 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SNF_MAC_OUT_LENGTH							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SNF_MAC_OUT_LENGTH	Serial flash write data length (unit: byte)

11001508 SNF_MAC_INL Serial NAND flash MAC mode input data length 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SNF_MAC_IN_LENGTH							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SNF_MAC_IN_LENGTH	Serial flash read data length (unit: byte)

1100150C **SNF_RD_CTL1** **Serial NAND flash read control 1** **13000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PAGE_READ_CMD								PAGE_READ_ADDRESS							
Type	RW								RW							
Reset	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAGE_READ_ADDRESS															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	PAGE_READ_CMD	Page read command setting
23:0	PAGE_READ_ADDRESS	Page Read Address

11001510 **SNF_RD_CTL2** **Serial NAND flash read control 2** **0000080B**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DATA_READ_DUMMY				DATA_READ_CMD							
Type					RW				RW							
Reset					1	0	0	0	0	0	0	0	1	0	1	1

Bit(s)	Name	Description
11:8	DATA_READ_DUMMY	Dummy Cycle when read from cache, setting the dummy cycles according to read command of datasheet.
7:0	DATA_READ_CMD	Data Read command

11001514 SNF_RD_CTL3 Serial NAND flash read control 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_READ_CMD_DUMMY_OUT				DATA_READ_ADDRESS											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	DATA_READ_CMD_DUMMY_OUT	Data read command output in dummy cycle [3:0]
11:0	DATA_READ_ADDRESS	Data read address setting [11:0]

11001518 SNF_GF_CTL1 Serial NAND flash get feature control 1 0FC00101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GF_CMD								GF_ADDR							
Type	RW								RW							
Reset	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GF_BUSY_MASK								GF_STATUS							
Type	RW								RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:24	GF_CMD	Get Feature command setting
23:16	GF_ADDR	Get Feature address setting
15:8	GF_BUSY_MASK	Get Feature Status busy mask bits setting e.g. flag[7:0] = get_feature_status[7:0] & get_feature_busy [7:0]; If (flag[7:0] == 0) done; Else, continue. 0: Mask this bit. Do not check it 1: Check this bit
7:0	GF_STATUS	Get Feature status result [7:0]

11001520 SNF_GF_CTL3 Serial NAND flash get feature control3 000F0320

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LOOP_LIMIT			
Type													RW			
Reset													1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	POOLING_CYCLE															
Type	RW															
Reset	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
19:16	LOOP_LIMIT	Get Feature loop setting for status read and compare NOTE: 4'b1111 for no limit setting
15:0	POOLING_CYCLE	Polling cycle setting for standby period between issue Get Feature commands Standby period = polling_cycle X base_time_slot Base_time_slot = spi-nand clock cycle X 128. e.g. spi-nand clock=100M, 1T=10ns, then base_time_slot = 1.28us. And the polling cycle value should be set to meet the Standby_period ~= spec time.

11001524 SNF_PG_CTL1 Serial NAND flash program control1 00100206

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PG_EXE_CMD							
Type									RW							
Reset									0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PG_LOAD_CMD								WRITE_EN_CMD							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0

Bit(s)	Name	Description
23:16	PG_EXE_CMD	Program execute command [7:0]
15:8	PG_LOAD_CMD	Program load command [7:0]
7:0	WRITE_EN_CMD	Write Enable command [7:0]

11001528 SNF_PG_CTL2 Serial NAND flash program control2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PG_LOAD_CMD_DUMMY_OUT								PG_LOAD_ADDR							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	PG_LOAD_CMD_DUMMY_OUT	Program load command output in dummy cycle [3:0]
7:0	PG_LOAD_ADDR	Program load address [7:0]

1100152C SNF_PG_CTL3 Serial NAND flash program control3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PG_EXE_ADDR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PG_EXE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	PG_EXE_ADDR	Program execute address [23:0]

11001530 SNF_ER_CTL Serial NAND flash erase control 0000D800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERASE_CMD															AUTO_ERASE_TRIGGER
Type	RW															RW
Reset	1	1	0	1	1	0	0	0								0

Bit(s)	Name	Description
15:8	ERASE_CMD	Erase command setting [7:0]
0	AUTO_ERASE_TRIGGER	Auto Erase trigger bit

11001534 SNF_ER_CTL2 Serial NAND flash erase control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERASE_ADDR	Erase address setting [23:0]

11001538 SNF_MISC_CTL Serial NAND flash MISC control 0400000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			MACRO_RST_EN	SW_RST	SFIO_EN_SEL	FIFO_RD_LTC	_4FIFO_EN	FBCLK_SEL	SMPCK_INV	CLK_INV	PG_LOAD_X4_EN			DATA_READ_MODE		
Type			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW		
Reset			0	0	0	1	0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SF2CS_DUAL_EN	SF2CS_SEL	SF2CS_EN				LATCH_LAT	PG_LOAD_CUSTOM_EN	DATAR_CUSTOM_EN				CS_DESELECT_CYC		
Type		RW	RW	RW				RW	RW	RW				RW		
Reset		0	0	0				0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
29	MACRO_RST_EN	MACRO reset fifo enable
28	SW_RST	SW reset controller: 1 for reset on, 0 for reset off.
27	SFIO_EN_SEL	IO PAD Enable signal align with clock positive edge select
26:25	FIFO_RD_LTC	FIFO read latency
24	_4FIFO_EN	4Tap FIFO read enable
23	FBCLK_SEL	Feedback clock select
22	SMPCK_INV	Inner sample clock inverter select
21	CLK_INV	Output serial clock inverter select
20	PG_LOAD_X4_EN	Program load data x4 mode enable.
18:16	DATA_READ_MODE	Data Read mode select. Bit[1:0] for data mode, Bit[2] for IO mode. 000: X1 data mode 001: X2 data mode 010: X4 data mode 011: Reserved 100: Reserved 101: Dual IO mode 110: Quad IO mode 111: Reserved
14	SF2CS_DUAL_EN	Both CS1/CS2 enable/select for first/second SPI-NAND device.
13	SF2CS_SEL	SF 2CS select for first/second SPI-NAND device.
12	SF2CS_EN	SF 2CS enable for second SPI-NAND device.
9:8	LATCH_LAT	Data read latch latency for auto mode
7	PG_LOAD_CUSTOM_EN	Program load custom mode enable

Bit(s)	Name	Description
6	DATARD_CUSTOM_EN	Data read custom mode enable
4:0	CS_DESELECT_CYC	CS deselect cycle setting

1100153C **SNF_MISC_CTL2** Serial NAND flash MISC control 2 02100210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					PROGRAM_LOAD_BYTE_NUM											
Type					RW											
Reset					0	0	1	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					READ_DATA_BYTE_NUM											
Type					RW											
Reset					0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
27:16	PROGRAM_LOAD_BYTE_NUM	NOTE: Setting value should be sync with NFI Write byte length. <pre> if (NFI_SECCUS_SIZE.CUS_SEC_SIZE.SECCUS_SIZE_EN==0) { (512 + PAGEFMT.spare_size) * NFI_CON.sec_num == Transfer Data Length == SNF_MISC_CTL2.PROGRAM_LOAD_BYTE_NUM } else { (NFI_SECCUS_SIZE.CUS_SEC_SIZE) * NFI_CON.sec_num == Transfer Data Length == SNF_MISC_CTL2.PROGRAM_LOAD_BYTE_NUM </pre>
11:0	READ_DATA_BYTE_NUM	NOTE: Setting value should be sync with NFI Read byte length. <pre> if (NFI_SECCUS_SIZE.CUS_SEC_SIZE.SECCUS_SIZE_EN==0) { (512 + PAGEFMT.spare_size) * NFI_CON.sec_num == Transfer Data Length == SNF_MISC_CTL2.READ_DATA_BYTE_NUM } else { (NFI_SECCUS_SIZE.CUS_SEC_SIZE) * NFI_CON.sec_num == Transfer Data Length == SNF_MISC_CTL2.READ_DATA_BYTE_NUM </pre>

11001540 SNF_DLY_CTL1 Serial NAND flash delay control setting 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SFIO3_OUT_DLY										SFIO2_OUT_DLY			
Type			RW										RW			
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			SFIO1_OUT_DLY										SFIO0_OUT_DLY			
Type			RW										RW			
Reset			0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
29:24	SFIO3_OUT_DLY	Serial flash SFIO3 pin IO output delay setting
21:16	SFIO2_OUT_DLY	Serial flash SFIO2 pin IO output delay setting
13:8	SFIO1_OUT_DLY	Serial flash SFIO1 pin IO output delay setting
3:0	SFIO0_OUT_DLY	Serial flash SFIO0 pin IO output delay setting

11001544 SNF_DLY_CTL2 Serial NAND flash delay control setting 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SFIO3_IN_DLY										SFIO2_IN_DLY			
Type			RW										RW			
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			SFIO1_IN_DLY										SFIO0_IN_DLY			
Type			RW										RW			
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
29:24	SFIO3_IN_DLY	Serial flash SFIO3 pin IO input delay setting
21:16	SFIO2_IN_DLY	Serial flash SFIO2 pin IO input delay setting
13:8	SFIO1_IN_DLY	Serial flash SFIO1 pin IO input delay setting
5:0	SFIO0_IN_DLY	Serial flash SFIO0 pin IO input delay setting

11001548 SNF_DLY_CTL3 Serial NAND flash control setting 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SFIFO_WR_EN_DLY_SEL										SFCS_DLY			
Type			RW										RW			
Reset			0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SFCK_OUT_DLY						SFCK_SAM_DLY					
Type					RW						RW					
Reset					0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
29:24	SFIFO_WR_EN_DLY_SEL	Serial flash FIFO write enable delay select setting
19:16	SFCS_DLY	Serial flash SFCS pin IO output delay setting
11:8	SFCK_OUT_DLY	Serial flash CK pin IO output delay setting
5:0	SFCK_SAM_DLY	Serial flash sample clock delay setting

1100154C SNF_DLY_CTL4 Serial NAND flash delay control setting 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SFCS2_DLY			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	SFCS2_DLY	Serial flash SFCS2 pin IO output delay setting

11001550 SNF_STA_CTL1 Serial NAND flash status1 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			GF_LOOP_TIMEOUT	CUS_PG_DONE	CUS_READ_DONE	AUTO_PG_DONE	AUTO_READ_DONE	AUTO_BLK_ERASE_DONE		DATARD_STATE			PGREAD_STATE			PGEXE_STATE
Type			RO	W1C	W1C	W1C	W1C	W1C		RO			RO			RO
Reset			0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PGEXE_STATE		PGLOAD_STATE			GF_STATE			BLKER_STATE			WREN_STATE	SPI_STATE			
Type	RO		RO			RO			RO			RO	RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29	GF_LOOP_TIMEOUT	Get Feature read status time out flag
28	CUS_PG_DONE	Custom program mode Clear setting and Status Status read(R): Custom program mode done flag. Clear(W): Set 1 and then 0 to clear this flag.
27	CUS_READ_DONE	Custom read mode Clear setting and Status Status read(R): Custom read mode done flag. Clear(W): Set 1 and then 0 to clear this flag.
26	AUTO_PG_DONE	Auto program mode Clear setting and Status Status read(R): Auto program mode done flag. Clear(W): Set 1 and then 0 to clear this flag.
25	AUTO_READ_DONE	Auto read mode Clear setting and Status Status read(R): Auto read mode done flag. Clear(W): Set 1 and then 0 to clear this flag.
24	AUTO_BLK_ERASE_DONE	Auto block erase mode Clear setting and Status Status read(R): Auto block erase mode done flag. Clear(W): Set 1 and then 0 to clear this flag.
22:20	DATARD_STATE	State machine of custom read 0: IDLE 1: CMD 2: ADDR1 3: ADDR2 4: DUMMY 5: DATA 6: BUFOUT

Bit(s)	Name	Description
		7: WAIT
19:17	PGREAD_STATE	State machine of auto read
		0: IDLE
		1: CMD
		2: ADDR1
		3: ADDR2
		4: ADDR3
16:14	PGEXE_STATE	State machine of program execution
		0: IDLE
		1: CMD
		2: ADDR1
		3: ADDR2
		4: ADDR3
13:11	PGLOAD_STATE	State machine of program load
		0: IDLE
		1: CMD
		2: ADDR1
		3: ADDR2
		4: BUFIN
		5: DATA
10:8	GF_STATE	State machine of get feature
		0: IDLE
		1: GF_CMD
		2: GF_ADDR
		3: GF_DATA
		4: GF_CMP
		5: GF_WAIT
7:5	BLKER_STATE	State machine of auto block erase
		0: IDLE
		1: CMD
		2: ADDR1
		3: ADDR2

Bit(s)	Name	Description
4: ADDR3		
4	WREN_STATE	State machine of write enable
0: IDLE		
1: CMD		
3:0	SPI_STATE	State machine SPI main Controller
0: IDLE		
1: Write Enable		
2: Block Erase		
3: Get Feature		
4: Program Load		
5: Program Execution		
6: Page Read		
7: Custom Data Read		

11001554 SNF_STA_CTL2 Serial NAND flash status2 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DATARD_BYTE_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PGLOAD_BTTE_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DATARD_BYTE_CNT	Data Read Transfer byte count
12:0	PGLOAD_BTTE_CNT	Program Load Transfer byte count

11001558 SNF_STA_CTL3 Serial NAND flash status3 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										GF_BASE_CNT						
Type										RO						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GF_WAIT_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
22:16	GF_BASE_CNT	Get feature base counter
15:0	GF_WAIT_CNT	Get feature wait counter
When GF_BASE_CNT==8'hff, GF_WAIT_CNT plus 1; When GF_WAIT_CNT= Polling_Cycle, issue get feature command.		

1100155C SNF_SNF_CNFG SPI/Parallel NAND selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SPI_MODE
Type																RW
Reset																0

Bit(s)	Name	Description
0	SPI_MODE	Switch for Parallel NAND or Serial NAND
0: NFI		
1: SPI NAND		

11001560 SNF_DEBUG_SEL DEBUG MUX selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_SEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DEBUG_SEL	Debug monitor select

11001800 SPI_GPRAM_ADDR GPRAM start address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPRAM_SEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPRAM_SEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GPRAM_SEL	When using MAC mode, put data into SRAM.

Module name: NFIECC Base address: (+0x1100_2000)

Address	Name	Width	Register Function
11002000	<u>NFIECC_ENCCON</u>	32	NFIECC encoder control register
11002004	<u>NFIECC_ENCCNFG</u>	32	NFIECC configure register
11002008	<u>NFIECC_ENCDIADDR</u>	32	NFIECC encoder DI memory address register
1100200C	<u>NFIECC_ENCIDLE</u>	32	NFIECC encoder idle status register
1100207C	<u>NFIECC_ENCSTA</u>	32	NFIECC encoder status register
11002080	<u>NFIECC_ENCIRQEN</u>	32	NFIECC encoder IRQ enable register
11002084	<u>NFIECC_ENCIRQSTA</u>	32	NFIECC encoder IRQ status register
11002090	<u>NFIECC_PIO_DIRDY</u>	32	NFIECC PIO data ready register
11002094	<u>NFIECC_PIO_DI</u>	32	NFIECC PIO data register
11002100	<u>NFIECC_DECCON</u>	32	NFIECC decoder control register
11002104	<u>NFIECC_DECCNFG</u>	32	NFIECC decoder configure register
11002108	<u>NFIECC_DECDIADDR</u>	32	NFIECC decoder DI memory address register
1100210C	<u>NFIECC_DECIDLE</u>	16	NFIECC decoder idle status register
11002110	<u>NFIECC_DECFER</u>	16	NFIECC decoder Found error status register
11002114	<u>NFIECC_DECENUM0</u>	32	NFIECC decode error number register
11002118	<u>NFIECC_DECENUM1</u>	32	NFIECC decode error number register
1100211C	<u>NFIECC_DECENUM2</u>	32	NFIECC decode error number register
11002120	<u>NFIECC_DECENUM3</u>	32	NFIECC decode error number register
11002124	<u>NFIECC_DECDONE</u>	16	NFIECC decoder error status register
11002200	<u>NFIECC_DECIRQEN</u>	32	NFIECC decoder IRQ enable register
11002204	<u>NFIECC_DECIRQSTA</u>	32	NFIECC_DECIRQSTA
11002208	<u>NFIECC_DECFSM</u>	32	NFIECC decoder FSM
11002210	<u>NFI_MASTER_STA</u>	32	NFI master status
11002220	<u>NFIECC_BUS_CFG</u>	32	NFIECC_BUS configuration
11002300	<u>NFIECC_ENCPAR0</u>	32	NFIECC Parity0 register
11002304	<u>NFIECC_ENCPAR1</u>	32	NFIECC Parity1 register
11002308	<u>NFIECC_ENCPAR2</u>	32	NFIECC Parity2 register
1100230C	<u>NFIECC_ENCPAR3</u>	32	NFIECC Parity3 register
11002310	<u>NFIECC_ENCPAR4</u>	32	NFIECC Parity4 register
11002314	<u>NFIECC_ENCPAR5</u>	32	NFIECC Parity5 register
11002318	<u>NFIECC_ENCPAR6</u>	32	NFIECC Parity6 register
1100231C	<u>NFIECC_ENCPAR7</u>	32	NFIECC Parity7 register
11002320	<u>NFIECC_ENCPAR8</u>	32	NFIECC Parity8 register
11002324	<u>NFIECC_ENCPAR9</u>	32	NFIECC Parity9 register
11002328	<u>NFIECC_ENCPAR10</u>	32	NFIECC Parity10 register
11002500	<u>NFIECC_DECEL0</u>	32	NFIECC decoder error location0 register
11002504	<u>NFIECC_DECEL1</u>	32	NFIECC decoder error location1 register
11002508	<u>NFIECC_DECEL2</u>	32	NFIECC decoder error location2 register
1100250C	<u>NFIECC_DECEL3</u>	32	NFIECC decoder error location3 register
11002510	<u>NFIECC_DECEL4</u>	32	NFIECC decoder error location4 register
11002514	<u>NFIECC_DECEL5</u>	32	NFIECC decoder error location5 register
11002518	<u>NFIECC_DECEL6</u>	32	NFIECC decoder error location6 register
1100251C	<u>NFIECC_DECEL7</u>	32	NFIECC decoder error location7 register
11002520	<u>NFIECC_DECEL8</u>	32	NFIECC decoder error location8 register
11002524	<u>NFIECC_DECEL9</u>	32	NFIECC decoder error location9 register
11002528	<u>NFIECC_DECEL10</u>	32	NFIECC decoder error location10 register
1100252C	<u>NFIECC_DECEL11</u>	32	NFIECC decoder error location11 register

11002000 NFI ECC ENCCON NFI ECC encoder control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ENC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	ENC_EN	Indicates the encoder can work in NFI mode and AHB mode. In AHB mode, parity bits remain in the PAR0~PAR4 register field until the ENC_EN is deasserted to 0. 0: Disable the Encode block. 1: Enable the Encode block. In AHB mode, the Encoder starts to fetch data when the register changes from 0 to 1. In NFI mode, the register enables the Encode block, and then the Encoder module waits for start signal and data from NFI.

11002004 NFI_ECC_ENCCNFG NFI_ECC configure register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			ENC_MS													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ENC_BURST_EN		ENC_MODE			ENC_TNUM			
Type								RW		RW			RW			
Reset								0		0	0		0	0	0	0

Bit(s)	Name	Description
29:19	ENC_MS	Indicates the total bytes size of message block including main data and control (FDM) data in the NFI mode. The message block can only be in byte unit. The spare_ECC_num parameter in old version has been merged into the message_block_size parameter. If the block_size is equal to zero, the NFIECC performs nothing. The acceptable coded block size, which includes data and parity bits size of 1~16383bits. Different ENC_TNUM results in different parity bits, and also results in different maximum message block size.
8	ENC_BURST_EN	Indicates the burst enable. 1'b0: DMA mode uses single read. 1'b1: DMA mode uses burst read.
6:5	ENC_MODE	Indicates the data source from AHB or from NFI. 2'b00: Source data from AHB. (DMA mode) 2'b01: Source data from NFI module. (NFI mode) 2'b10: Source data is written by MCU. (PIO mode) 2'b11: Reserved mode.
3:0	ENC_TNUM	Indicates the correction capability in one block size. 4'd0: The NFIECC is capable of correcting 4 bits in one block size. 4'd1: The NFIECC is capable of correcting 6 bits in one block size. 4'd2: The NFIECC is capable of correcting 8 bits in one block size. 4'd3: The NFIECC is capable of correcting 10 bits in one block size. 4'd4: The NFIECC is capable of correcting 12 bits in one block size. 4'd5: The NFIECC is capable of correcting 14 bits in one block size. 4'd6: The NFIECC is capable of correcting 16 bits in one block size. 4'd7: The NFIECC is capable of correcting 18 bits in one block size.

Bit(s)	Name	Description
		4'd8: The NFIECC is capable of correcting 20 bits in one block size.
		4'd9: The NFIECC is capable of correcting 22 bits in one block size.
		4'd10: The NFIECC is capable of correcting 24 bits in one block size.

11002008 NFIECC ENCDIADDR NFIECC encoder DI memory address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_DIADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_DIADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	ENC_DIADDR	Indicates the memory address of input data to Encoder block in AHB mode. (4-byte align)

1100200C NFIECC ENCIDLE NFIECC encoder idle status register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ENC_IDLE
Type																RO
Reset																1

Bit(s)	Name	Description
0	ENC_IDLE	Indicates the Encode block in idle state and ready for new message block.
		0: The Encode block is under working.
		1: The Encode block is in Idle state and available for new message block.

1100207C **NFIECC_ENCSTA** **NFIECC encoder status register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			COUNT_MS													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														ENC_FSM		
Type														RO		
Reset														0	0	1

Bit(s)	Name	Description
29:19	COUNT_MS	Indicates the remaining un-processing message bytes.
2:0	ENC_FSM	3'd1: IDLE 3'd2: DATA 3'd4: DONE

11002080 NFI_ECC_ENCIRQEN NFI_ECC encoder IRQ enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PG_ENCIRQ_SEL	ENC_IRQEN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PG_ENCIRQ_SEL	Select IRQ valid one time each page or not, if not selected, then IRQ will generate each sector. 0: Disable IRQ valid one time each page 1: Enable IRQ valid one time each page
0	ENC_IRQEN	Encoder IRQ mask: triggered when Encoder operation is completed. 0: Disable 1: Enable

11002084 NFI_ECC_ENCIRQSTA NFI_ECC encoder IRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ENC_IRQSTA
Type																RC
Reset																0

Bit(s)	Name	Description
0	ENC_IRQSTA	Indicates interrupt status for Encoder processing. 0: No interrupt is generated. 1: An interrupt is pending and waiting for service. Active when Encoder processing is done.

11002090 **NFIECC PIO DIRDY** **NFIECC PIO data ready register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PIO_DI_RDY
Type																RO
Reset																0

Bit(s)	Name	Description
0	PIO_DI_RDY	Indicates the PIO mode (Encoder/Decoder) is ready for input data. 0: ECC is busy. During busy state, NFIECC_PIO_DI should not be over-write. 1: ECC is ready for input data. In PIO mode, write next PIO_DI when pio_di_rdy is equal to 1.

11002094 **NFIECC PIO DI** **NFIECC PIO data register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIO_DI															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIO_DI															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PIO_DI	Indicates the PIO mode data input.

11002100 NFI_ECC_DECCON NFI_ECC decoder control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DEC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	DEC_EN	Indicates the enable in NFI mode and start to work in AHB mode. In AHB mode, the decode-status FER and error number registers and error location registers will be reset to 0 when DEC_EN is deasserted. 0: Disable the Decode block. 1: Enable the Decode block. In AHB mode, the Decoder starts to fetch data when the register changes from 0 to 1. In NFI mode, the register enables the Decode block, and then the Decoder module waits for start signal and data from NFI.

11002104 NFI ECC DECCNFG NFI ECC decoder configure register 00003000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEC_EMPTY_EN		DEC_CS													
Type	RW		RW													
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEC_CON					DEC_BURST_EN		DEC_MODE			DEC_TNUM			
Type			RW					RW		RW			RW			
Reset			1	1				0		0	0		0	0	0	0

Bit(s)	Name	Description
31	DEC_EMPTY_EN	Indicates the Decoder automatically detects the empty source data and bypass the auto-correction block (data are all equal to 1). (ignore in AHB_mode) 0: Disable the detection of empty source data. 1: Enable the detection of empty source data.
29:16	DEC_CS	Indicates the total bit size of coded block including protected data and parity bits. The acceptable coded block size is 1~8191 bits. If the coded block size is equal to zero, the decoder performs nothing.
13:12	DEC_CON	Indicates the bypass configuration in decoding processor. 0: Reserved 1: Only active syndrome calculator for error detecting purpose. ECC reports DONE and FER status after syndrome calculator is done. 2: Error-correction module is bypassed for being aware of error location purpose. ECC reports DONE, FER, EL and ERRNUM status after Chien search is done. 3: The ECC processor decoded data and auto-correction error data. The data address is signaled by DEC_DIADDR register in AHB mode and NFI_DIADDR in NFI mode. ECC reports DONE, FER, EL and ERRNUM status after error-correction is done.
8	DEC_BURST_EN	Indicates the burst enable. 1'b0: DMA mode uses single read. 1'b1: DMA mode uses burst read.
6:5	DEC_MODE	Indicates the data source from access AHB, NFI controller or MCU. 2'b00: Source data from access through Bus. (DMA mode) 2'b01: Source data from NFI module. (NFI mode) 2'b10: Source data is written by MCU. (PIO mode) 2'b11: Reserved mode.
3:0	DEC_TNUM	Indicates the correction capability in one block size.

Bit(s)	Name	Description
		4'd0: Means capable of correcting 4 bits in one block size.
		4'd1: Means capable of correcting 6 bits in one block size.
		4'd2: Means capable of correcting 8 bits in one block size.
		4'd3: Means capable of correcting 10 bits in one block size.
		4'd4: Means capable of correcting 12 bits in one block size.
		4'd5: Means capable of correcting 14 bits in one block size.
		4'd6: Means capable of correcting 16 bits in one block size.
		4'd7: Means capable of correcting 18 bits in one block size.
		4'd8: Means capable of correcting 20 bits in one block size.
		4'd9: Means capable of correcting 22 bits in one block size.
		4'd10: Means capable of correcting 24 bits in one block size.

11002108	NFIECC_DECDIADDR				NFIECC decoder DI memory address register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	DEC_DIADDR																
Type	RW																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	DEC_DIADDR																
Type	RW																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:2	DEC_DIADDR	Indicates the memory address of input data to the Decoder block in AHB mode. (4-byte alignment).

1100210C **NFIECC_DECIDLE** **NFIECC decoder idle status register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DEC_IDLE
Type																RO
Reset																1

Bit(s)	Name	Description
0	DEC_IDLE	0: Means the Decode block is under working. 1: Means the Decode block is in idle state and available for new coded block.

11002110 NFI ECC DEC FER NFI ECC decoder Found error status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FER15	FER14	FER13	FER12	FER11	FER10	FER9	FER8	FER7	FER6	FER5	FER4	FER3	FER2	FER1	FER0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	FER15	Indicates whether the error is found or not in the coded block. The FER are numbered by NFI sector number in NFI mode; otherwise in AHB mode always use the FER0. The signal is reset when DEC_EN is deasserted in both NFI and AHB mode. 0: There is no error detected in the coded block. 1: There is (are) error (s) detected in the coded block.
14	FER14	Indicates the error is found or not in the coded block. The FER numbered by NFI sector number in NFI mode; otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode. 0: There is no error detected in the coded block. 1: There is (are) error(s) detected in the coded block.
13	FER13	Indicates the error is found or not in the coded block. The FER numbered by NFI sector number in NFI mode; otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode. 0: There is no error detected in the coded block. 1: There is (are) error(s) detected in the coded block.
12	FER12	Indicates the error is found or not in the coded block. The FER numbered by NFI sector number in NFI mode; otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode. 0: There is no error detected in the coded block. 1: There is (are) error(s) detected in the coded block.
11	FER11	Indicates the error is found or not in the coded block. The FER numbered by NFI sector number in NFI mode; otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode. 0: There is no error detected in the coded block. 1: There is (are) error(s) detected in the coded block.
10	FER10	Indicates the error is found or not in the coded block. The FER numbered by NFI sector number in NFI mode; otherwise, in AHB mode,

Bit(s)	Name	Description
		always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode.
		0: There is no error detected in the coded block.
		1: There is (are) error(s) detected in the coded block.
9	FER9	Indicates the error is found or not in the coded block. The FER numbered by NFI sector number in NFI mode; otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode.
		0: There is no error detected in the coded block.
		1: There is (are) error(s) detected in the coded block.
8	FER8	Indicates the error is found or not in the coded block. The FER numbered by NFI sector number in NFI mode; otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode.
		0: There is no error detected in the coded block.
		1: There is (are) error(s) detected in the coded block.
7	FER7	Indicates the error is found or not in the coded block. The FER numbered by NFI sector number in NFI mode; otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode.
		0: There is no error detected in the coded block.
		1: There is (are) error(s) detected in the coded block.
6	FER6	Indicates the error is found or not in the coded block. The FER numbered by NFI sector number in NFI mode; otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode.
		0: means there is no error detected in the coded block.
		1: means there is (are) error(s) detected in the coded block.
5	FER5	Indicates the error is found or not in the coded block. The FER numbered by NFI sector number in NFI mode; otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode.
		0: There is no error detected in the coded block.
		1: There is (are) error(s) detected in the coded block.
4	FER4	Indicates the error is found or not in the coded block. The FER numbered by NFI sector number in NFI mode; otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode.
		0: There is no error detected in the coded block.
		1: There is (are) error(s) detected in the coded block.

Bit(s)	Name	Description
3	FER3	Indicates the error is found or not in the coded block. The FER numbered by NFI sector number in NFI mode; otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode. 0: There is no error detected in the coded block. 1: There is (are) error(s) detected in the coded block.
2	FER2	Indicates the error is found or not in the coded block. The FER numbered by NFI sector number in NFI mode; otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode. 0: There is no error detected in the coded block. 1: There is (are) error(s) detected in the coded block.
1	FER1	Indicates the error is found or not in the coded block. The FER numbered by NFI sector number in NFI mode; otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode. 0: There is no error detected in the coded block. 1: There is (are) error(s) detected in the coded block.
0	FER0	Indicates the error is found or not in the coded block. The FER numbered by NFI sector number in NFI mode; otherwise, in AHB mode, always use the FER0. The signal reset when DEC_EN is deasserted in both NFI and AHB mode. 0: There is no error detected in the coded block. 1: There is (are) error(s) detected in the coded block.

11002114 NFI_ECC_DECENUM0 NFI_ECC decode error number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ERRNUM3									ERRNUM2			
Type				RO									RO			
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ERRNUM1									ERRNUM0			
Type				RO									RO			
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
28:24	ERRNUM3	Indicates the error numbers of coded block3 in one start signal. 5'h1f means the error is uncorrectable. But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
20:16	ERRNUM2	Indicates the error numbers of coded block2 in one start signal. 5'h1f means the error is uncorrectable. But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
12:8	ERRNUM1	Indicates the error numbers of coded block1 in one start signal. 5'h1f means the error is uncorrectable. But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
4:0	ERRNUM0	Indicates the error numbers of coded block0 in one start signal. 5'h1f means the error is uncorrectable. But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.

11002118 NFI_ECC_DECENUM1 NFI_ECC decode error number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ERRNUM7								ERRNUM6				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ERRNUM5								ERRNUM4				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
28:24	ERRNUM7	Indicates the error numbers of coded block7 in one start signal. 5'h1f means the error is uncorrectable. But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
20:16	ERRNUM6	Indicates the error numbers of coded block6 in one start signal. 5'h1f means the error is uncorrectable. But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
12:8	ERRNUM5	Indicates the error numbers of coded block5 in one start signal. 5'h1f means the error is uncorrectable. But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
4:0	ERRNUM4	Indicates the error numbers of coded block4 in one start signal. 5'h1f means the error is uncorrectable. But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.

1100211C NFI ECC DECE NUM2 NFI ECC decode error number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ERRNUM11								ERRNUM10				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ERRNUM9								ERRNUM8				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
28:24	ERRNUM11	Indicates the error numbers of coded block11 in one start signal. 5'h1f means the error is uncorrectable. But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
20:16	ERRNUM10	Indicates the error numbers of coded block10 in one start signal. 5'h1f means the error is uncorrectable. But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
12:8	ERRNUM9	Indicates the error numbers of coded block9 in one start signal. 5'h1f means the error is uncorrectable. But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
4:0	ERRNUM8	Indicates the error numbers of coded block8 in one start signal. 5'h1f means the error is uncorrectable. But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.

11002120 NFI ECC DECE NUM3 NFI ECC decode error number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				ERRNUM15									ERRNUM14			
Type				RO									RO			
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ERRNUM13									ERRNUM12			
Type				RO									RO			
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
28:24	ERRNUM15	Indicates the error numbers of coded block15 in one start signal. 5'h1f means the error is uncorrectable. But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
20:16	ERRNUM14	Indicates the error numbers of coded block14 in one start signal. 5'h1f means the error is uncorrectable. But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
12:8	ERRNUM13	Indicates the error numbers of coded block13 in one start signal. 5'h1f means the error is uncorrectable. But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.
4:0	ERRNUM12	Indicates the error numbers of coded block12 in one start signal. 5'h1f means the error is uncorrectable. But ECC only can partially detect uncorrectable error. If the error number exceeds the error capability, ECC only can partially detect the situation.

11002124 NFI_ECC_DECDONE NFI_ECC decoder error status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DONE15	DONE14	DONE13	DONE12	DONE11	DONE10	DONE9	DONE8	DONE7	DONE6	DONE5	DONE4	DONE3	DONE2	DONE1	DONE0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	DONE15	Indicates the Decoding procedure is done. 0: The Decode block is under working. 1: The Decode block is finished. For different DEC_CON and EMPTY_EN in NFI_ECC_DECCNFG register, decoder done has different meaning.
14	DONE14	Indicates the Decoding procedure is done. 0: The Decode block is under working. 1: The Decode block is finished. For different DEC_CON and EMPTY_EN in NFI_ECC_DECCNFG register, decoder done has different meaning.
13	DONE13	Indicates the Decoding procedure is done. 0: The Decode block is under working. 1: The Decode block is finished. For different DEC_CON and EMPTY_EN in NFI_ECC_DECCNFG register, decoder done has different meaning.
12	DONE12	Indicates the Decoding procedure is done. 0: The Decode block is under working. 1: The Decode block is finished. For different DEC_CON and EMPTY_EN in NFI_ECC_DECCNFG register, decoder done has different meaning.
11	DONE11	Indicates the Decoding procedure is done. 0: The Decode block is under working. 1: The Decode block is finished. For different DEC_CON and EMPTY_EN in NFI_ECC_DECCNFG register, decoder done has different meaning.
10	DONE10	Indicates the Decoding procedure is done. 0: The Decode block is under working. 1: The Decode block is finished. For different DEC_CON and EMPTY_EN in NFI_ECC_DECCNFG register, decoder done has different meaning.
9	DONE9	Indicates the Decoding procedure is done. 0: The Decode block is under working. 1: The Decode block is finished. For different DEC_CON and EMPTY_EN in NFI_ECC_DECCNFG register, decoder done has different meaning.

Bit(s)	Name	Description
8	DONE8	Indicates the Decoding procedure is done. 0: The Decode block is under working. 1: The Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning.
7	DONE7	Indicates the Decoding procedure is done. 0: The Decode block is under working. 1: The Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning.
6	DONE6	Indicates the Decoding procedure is done. 0: The Decode block is under working. 1: The Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning.
5	DONE5	Indicates the Decoding procedure is done. 0: The Decode block is under working. 1: The Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning.
4	DONE4	Indicates the decoding procedure is done. 0: The Decode block is under working. 1: The Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning.
3	DONE3	Indicates the Decoding procedure is done. 0: The Decode block is under working. 1: The Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning.
2	DONE2	Indicates the Decoding procedure is done. 0: The Decode block is under working. 1: The Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning.
1	DONE1	Indicates the Decoding procedure is done. 0: The Decode block is under working. 1: The Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning.
0	DONE0	Indicates the Decoding procedure is done. 0: The Decode block is under working. 1: The Decode block is finished. For different DEC_CON and EMPTY_EN in NFIECC_DECCNFG register, decoder done has different meaning.

Bit(s)	Name	Description

11002200 NFIECC_DECIRQEN NFIECC decoder IRQ enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SEC_DONE_CNT											PG_DE CIRQ_S EL	DEC_IR QEN
Type				RO											RW	RW
Reset				0	0	0	0	0							0	0

Bit(s)	Name	Description
12:8	SEC_DONE_CNT	sec_done_cnt for ecc.auto clear when page_ecc_done. Should not be used for judgment.
1	PG_DECIRQ_SEL	Select IRQ valid one time each page or not. If not selected, then IRQ will generate each sector. 0: Disable IRQ valid one time each page 1: Enable IRQ valid one time each page
0	DEC_IRQEN	Decoder IRQ mask: triggered when Decoder operation is completed. 0: Disable 1: Enable

11002204 NFIECC_DECIRQSTA NFIECC_DECIRQSTA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DEC_IRQSTA
Type																RC
Reset																0

Bit(s)	Name	Description
0	DEC_IRQSTA	Indicates Interrupt status for Decoder processing. 0: No interrupt is generated. 1: An interrupt is pending and waiting for service. Active when Decoder processing is done.

11002208 NFIECC_DECFSM NFIECC decoder FSM 01011101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			AUTOC_FSM								AUTO_FDM_FSM					
Type			RO								RO					
Reset			0	0	0	0	0	1			0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHIEN_FSM				BMA_FSM								SYN_FSM			
Type	RO				RO								RO			
Reset	0	0	0	1	0	0	0	1					0	0	0	1

Bit(s)	Name	Description
29:24	AUTOC_FSM	Indicates the status of auto-correction stage. 6'd1: IDLE 6'd2: COUNT 6'd4: READ_PRE 6'd8: READ 6'd16: WRITE 6'd32: DONE
21:16	AUTO_FDM_FSM	Indicates the status of Chien search stage. 6'd1: IDLE 6'd2: COUNT 6'd4: READ_PRE 6'd8: READ 6'd16: WRITE 6'd32: WAITAC
15:12	CHIEN_FSM	Indicates the status of Chien search stage. 4'd1: IDLE 4'd2: BUSY 4'd4: DONE 4'd8: WAITC
11:8	BMA_FSM	Indicates the status of BMA stage. 4'd1: IDLE 4'd2: BUSY 4'd4: DONE
3:0	SYN_FSM	Indicates the status of syndrome stage. 4'd1: IDLE

Bit(s)	Name	Description
		4'd2: DATA
		4'd4: DONE
		4'd8: WAITBM

11002210	NFI MASTER STA				NFI master status										00018044	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														grant_state		
Type														RO		
Reset														0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					hburst_cnt										ahb_bu s_busy	bus_bu sy
Type					RO										RO	RO
Reset					0	0	0	0							0	0

Bit(s)	Name	Description
18:16	grant_state	grant_state means current AHB arb_master states. 3'b001: NFI access 3'b010: autoc access 3'b100: ecc_r access
11:8	hburst_cnt	hburst_cnt means current burst cnt for AHB operation
1	ahb_bus_busy	ahb_bus_busy means whether each AHB burst access is busy or not.
0	bus_busy	bus_busy means whether NFI internal related req bus is busy or not

11002220 NFI ECC BUS_CFG NFI ECC_BUS configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					ENC_DIADDR_EXT											
Type					RW											
Reset					0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DEC_DIADDR_EXT											
Type					RW											
Reset					0	0	0	0								

Bit(s)	Name	Description
27:24	ENC_DIADDR_EXT	used to extend ENC_DIADDR register. Indicates the highest 4 bits of memory address of input data to the Encoder block in AHB mode.
11:8	DEC_DIADDR_EXT	used to extend DEC_DIADDR register. Indicates the highest 4 bits of memory address of input data to the Decoder block in AHB mode.

11002300 NFI ECC ENCPAR0 NFI ECC Parity0 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR0	Indicates the highest order of output parity bits and the bit 0 is the highest order of parity bit. The PAR0~PAR34 registers remain the last message block parity bits until ENC_EN is deasserted. The parity bits should append after main data by order of {PAR0[7:0], PAR0[15:8], PAR0[23:16], PAR0[31:24], PAR1[7:0], PAR1[15:8], PAR1[23:16], PAR1[31:24], ...}, The redundant bit of parity bit will be padded by 1.

11002304 NFIECC_ENCPAR1 NFIECC Parity1 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR1	Indicates the parity bits and the bit 0 is the highest order of parity bit.

11002308 NFIECC_ENCPAR2 NFIECC Parity2 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR2	Indicates the parity bits and the bit 0 is the highest order of parity bit.

1100230C NFIECC_ENCPAR3 NFIECC Parity3 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR3	Indicates the parity bits and the bit 0 is the highest order of parity bit.

11002310 NFIECC_ENCPAR4 NFIECC Parity4 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR4	Indicates the parity bits and the bit 0 is the highest order of parity bit.

11002314 NFIECC_ENCPAR5 NFIECC Parity5 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR5	Indicates the parity bits and the bit 0 is the highest order of parity bit.

11002318 NFIECC_ENCPAR6 NFIECC Parity6 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR6	Indicates the parity bits and the bit 0 is the highest order of parity bit.

1100231C NFIECC_ENCPAR7 NFIECC Parity7 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR7	Indicates the parity bits and the bit 0 is the highest order of parity bit.

11002320 NFIECC_ENCPAR8 NFIECC Parity8 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR8															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR8															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR8	Indicates the parity bits and the bit 0 is the highest order of parity bit.

11002324 NFIECC_ENCPAR9 NFIECC Parity9 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR9															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR9															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR9	Indicates the parity bits and the bit 0 is the highest order of parity bit.

11002328 NFIECC_ENCPAR10 NFIECC Parity10 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENC_PAR10															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENC_PAR10															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ENC_PAR10	Indicates the parity bits and the bit 0 is the highest order of parity bit.

11002500 NFIECC_DECELO NFIECC decoder error location0 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DEC_EL1													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEC_ELO													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	DEC_EL1	Indicates the error location 1 of the decoding result.
13:0	DEC_ELO	Indicates the error location 1 of the decoding result.

11002504 NFIECC_DECEL1 NFIECC decoder error location1 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DEC_EL3													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEC_EL2													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	DEC_EL3	Indicates the error location 1 of the decoding result.
13:0	DEC_EL2	Indicates the error location 1 of the decoding result.

11002508 NFIECC_DECEL2 NFIECC decoder error location2 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DEC_EL5													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEC_EL4													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	DEC_EL5	Indicates the error location 1 of the decoding result.
13:0	DEC_EL4	Indicates the error location 1 of the decoding result.

1100250C NFIECC_DECEL3 NFIECC decoder error location3 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DEC_EL7													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEC_EL6													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	DEC_EL7	Indicates the error location 1 of the decoding result.
13:0	DEC_EL6	Indicates the error location 1 of the decoding result.

11002510 NFIECC_DECEL4 NFIECC decoder error location4 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DEC_EL9													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEC_EL8													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	DEC_EL9	Indicates the error location 1 of the decoding result.
13:0	DEC_EL8	Indicates the error location 1 of the decoding result.

11002514 NFIECC_DECEL5 NFIECC decoder error location5 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DEC_EL11													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEC_EL10													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	DEC_EL11	Indicates the error location 1 of the decoding result.
13:0	DEC_EL10	Indicates the error location 1 of the decoding result.

11002518 NFIECC_DECEL6 NFIECC decoder error location6 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DEC_EL13													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEC_EL12													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	DEC_EL13	Indicates the error location 1 of the decoding result.
13:0	DEC_EL12	Indicates the error location 1 of the decoding result.

1100251C NFI ECC DECEL7 NFI ECC decoder error location7 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DEC_EL15													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEC_EL14													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	DEC_EL15	Indicates the error location 1 of the decoding result.
13:0	DEC_EL14	Indicates the error location 1 of the decoding result.

11002520 NFI ECC DECEL8 NFI ECC decoder error location8 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DEC_EL17													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEC_EL16													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	DEC_EL17	Indicates the error location 1 of the decoding result.
13:0	DEC_EL16	Indicates the error location 1 of the decoding result.

11002524 NFIECC_DECEL9 NFIECC decoder error location9 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DEC_EL19													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEC_EL18													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	DEC_EL19	Indicates the error location 1 of the decoding result.
13:0	DEC_EL18	Indicates the error location 1 of the decoding result.

11002528 NFIECC_DECEL10 NFIECC decoder error location10 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DEC_EL21													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEC_EL20													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	DEC_EL21	Indicates the error location 1 of the decoding result.
13:0	DEC_EL20	Indicates the error location 1 of the decoding result.

1100252C NFIECC_DECEL11 NFIECC decoder error location11 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DEC_EL23													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEC_EL22													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:16	DEC_EL23	Indicates the error location 1 of the decoding result.
13:0	DEC_EL22	Indicates the error location 1 of the decoding result.

3.4 Inter-Integrated Circuit (I2C)

3.4.1 Register Definition

Module name: `imp_iic_wrap` Base address: `(+0x11000000)`

Address	Name	Width	Register Function
11003000	<u>I2C0_CHN_DATA_PORT</u>	16	Data port register
11003094	<u>I2C0_CHN_SLAVE_ADDR</u>	16	Slave address register
11003008	<u>I2C0_CHN_INTR_MASK</u>	16	Interrupt mask register
1100300C	<u>I2C0_CHN_INTR_STAT</u>	16	Interrupt status register
11003010	<u>I2C0_CHN_CONTROL</u>	16	Control register
11003014	<u>I2C0_CHN_TRANSFER_LEN</u>	16	Transfer length register
11003018	<u>I2C0_CHN_TRANSAC_LEN</u>	16	Transaction length register (Number of transfers per transaction)
1100301C	<u>I2C0_CHN_DELAY_LEN</u>	16	Inter delay length register
11003020	<u>I2C0_CHN_HTIMING</u>	16	SCL high timing control register
11003024	<u>I2C0_CHN_START</u>	16	Start register
11003028	<u>I2C0_CHN_EXT_CONF</u>	16	Extension configuration register
1100302C	<u>I2C0_CHN_LTIMING</u>	16	SCL low timing control register
11003030	<u>I2C0_CHN_HS</u>	16	High speed mode register
11003034	<u>I2C0_CHN_IO_CONFIG</u>	16	IO configuration register
11003038	<u>I2C0_CHN_FIFO_ADDR_CLR</u>	16	FIFO address clear register
1100303C	<u>I2C0_CHN_DATA_TIMING</u>	16	Data receive time adjust
11003040	<u>I2C0_CHN_MCU_INTR</u>	16	MCU interrupt
11003044	<u>I2C0_CHN_TRANSFER_LEN_A UX</u>	16	Transfer length register (Number of bytes per transfer)
11003048	<u>I2C0_CHN_CLOCK_DIV</u>	16	Clock divider
1100304C	<u>I2C0_CHN_TIMEOUT_DIV</u>	16	Hardware timeout target
11003050	<u>I2C0_CHN_SOFTRESET</u>	16	Soft reset register
110030D4	<u>I2C0_CHN_DELAY_STEP</u>	16	For time stamp (I3C_EN==1)
110030D8	<u>I2C0_CHN_DELAY_SAMPLE</u>	16	For time stamp (I3C_EN==1)
110030E4	<u>I2C0_CHN_DEBUGSTAT</u>	16	Debug Status register
110030E8	<u>I2C0_CHN_DEBUGCTRL</u>	16	Debug control register
110030EC	<u>I2C0_CHN_DMA_FSM_DEBUG</u>	16	Multi-DMA channel debug
110030F0	<u>I2C0_CHN_MULTIMAS</u>	16	Multi-master control register
110030F4	<u>I2C0_CHN_FIFO_STAT</u>	16	FIFO Status register
110030F8	<u>I2C0_CHN_FIFO_THRESH</u>	16	FIFO Thresh register
11007F00	<u>I2C0_CHN_SEC_CONTROL</u>	16	Security control
11007F80	<u>I2C0_CHN_CHANNEL_LOCK</u>	16	Channel lock
11007F84	<u>I2C0_CHN_CHANNEL_SEC</u>	16	Channel security enable
11007F88	<u>I2C0_CHN_HW_CG_EN</u>	16	HW DCM Enable
11007F8C	<u>I2C0_CHN_MULTI_DMA</u>	16	Multi-DMA channel mode
11007F90	<u>I2C0_CHN_DMA_REQ</u>	16	Multi-DMA channel request
11007F94	<u>I2C0_CHN_DMA_NREQ</u>	16	Multi-DMA channel request canceled
11004000	<u>I2C1_CHN_DATA_PORT</u>	16	Data port register
11004094	<u>I2C1_CHN_SLAVE_ADDR</u>	16	Slave address register
11004008	<u>I2C1_CHN_INTR_MASK</u>	16	Interrupt mask register
1100400C	<u>I2C1_CHN_INTR_STAT</u>	16	Interrupt status register
11004010	<u>I2C1_CHN_CONTROL</u>	16	Control register
11004014	<u>I2C1_CHN_TRANSFER_LEN</u>	16	Transfer length register

Address	Name	Width	Register Function
11004018	<u>I2C1_CHN_TRANSAC_LEN</u>	16	Transaction length register (Number of transfers per transaction)
1100401C	<u>I2C1_CHN_DELAY_LEN</u>	16	Inter delay length register
11004020	<u>I2C1_CHN_HTIMING</u>	16	SCL high timing control register
11004024	<u>I2C1_CHN_START</u>	16	Start register
11004028	<u>I2C1_CHN_EXT_CONF</u>	16	Extension configuration register
1100402C	<u>I2C1_CHN_LTIMING</u>	16	SCL low timing control register
11004030	<u>I2C1_CHN_HS</u>	16	High speed mode register
11004034	<u>I2C1_CHN_IO_CONFIG</u>	16	IO configuration register
11004038	<u>I2C1_CHN_FIFO_ADDR_CLR</u>	16	FIFO address clear register
1100403C	<u>I2C1_CHN_DATA_TIMING</u>	16	Data receive time adjust
11004040	<u>I2C1_CHN_MCU_INTR</u>	16	MCU interrupt
11004044	<u>I2C1_CHN_TRANSFER_LEN_AUX</u>	16	Transfer length register (Number of bytes per transfer)
11004048	<u>I2C1_CHN_CLOCK_DIV</u>	16	Clock divider
1100404C	<u>I2C1_CHN_TIMEOUT_DIV</u>	16	Hardware timeout target
11004050	<u>I2C1_CHN_SOFTRESET</u>	16	Soft reset register
110040D4	<u>I2C1_CHN_DELAY_STEP</u>	16	For time stamp (I3C_EN==1)
110040D8	<u>I2C1_CHN_DELAY_SAMPLE</u>	16	For time stamp (I3C_EN==1)
110040E4	<u>I2C1_CHN_DEBUGSTAT</u>	16	Debug Status Register
110040E8	<u>I2C1_CHN_DEBUGCTRL</u>	16	Debug Control Register
110040EC	<u>I2C1_CHN_DMA_FSM_DEBUG</u>	16	Multi-DMA channel debug.
110040F0	<u>I2C1_CHN_MULTIMAS</u>	16	Multi-master control register
110040F4	<u>I2C1_CHN_FIFO_STAT</u>	16	FIFO Status Register
110040F8	<u>I2C1_CHN_FIFO_THRESH</u>	16	FIFO Thresh Register
11007F000	<u>I2C1_CHN_SEC_CONTROL</u>	16	Security Control
11007F800	<u>I2C1_CHN_CHANNEL_LOCK</u>	16	Channel lock.
11007F840	<u>I2C1_CHN_CHANNEL_SEC</u>	16	Channel security enable.
11007F880	<u>I2C1_CHN_HW_CG_EN</u>	16	HW DCM Enable
11007F8C0	<u>I2C1_CHN_MULTI_DMA</u>	16	Multi-DMA channel mode.
11007F900	<u>I2C1_CHN_DMA_REQ</u>	16	Multi-DMA channel request
11007F940	<u>I2C1_CHN_DMA_NREQ</u>	16	Multi-DMA channel request canceled.
11005000	<u>I2C2_CHN_DATA_PORT</u>	16	Data port register
11005094	<u>I2C2_CHN_SLAVE_ADDR</u>	16	Slave address register
11005008	<u>I2C2_CHN_INTR_MASK</u>	16	Interrupt mask register
1100500C	<u>I2C2_CHN_INTR_STAT</u>	16	Interrupt status register
11005010	<u>I2C2_CHN_CONTROL</u>	16	Control register
11005014	<u>I2C2_CHN_TRANSFER_LEN</u>	16	Transfer length register
11005018	<u>I2C2_CHN_TRANSAC_LEN</u>	16	Transaction length register (Number of transfers per transaction)
1100501C	<u>I2C2_CHN_DELAY_LEN</u>	16	Inter delay length register
11005020	<u>I2C2_CHN_HTIMING</u>	16	SCL high timing control register
11005024	<u>I2C2_CHN_START</u>	16	Start register
11005028	<u>I2C2_CHN_EXT_CONF</u>	16	Extension configuration register
1100502C	<u>I2C2_CHN_LTIMING</u>	16	SCL low timing control register
11005030	<u>I2C2_CHN_HS</u>	16	High speed mode register
11005034	<u>I2C2_CHN_IO_CONFIG</u>	16	IO configuration register
11005038	<u>I2C2_CHN_FIFO_ADDR_CLR</u>	16	FIFO address clear register
1100503C	<u>I2C2_CHN_DATA_TIMING</u>	16	Data receive time adjust
11005040	<u>I2C2_CHN_MCU_INTR</u>	16	MCU interrupt

Address	Name	Width	Register Function
11005044	<u>I2C2_CHN_TRANSFER_LEN_A</u> <u>UX</u>	16	Transfer length register (Number of bytes per transfer)
11005048	<u>I2C2_CHN_CLOCK_DIV</u>	16	Clock divider
1100504C	<u>I2C2_CHN_TIMEOUT_DIV</u>	16	Hardware timeout target
11005050	<u>I2C2_CHN_SOFTRESET</u>	16	Soft reset register
110050D4	<u>I2C2_CHN_DELAY_STEP</u>	16	For time stamp (I3C_EN==1)
110050D8	<u>I2C2_CHN_DELAY_SAMPLE</u>	16	For time stamp (I3C_EN==1)
110050E4	<u>I2C2_CHN_DEBUGSTAT</u>	16	Debug Status Register
110050E8	<u>I2C2_CHN_DEBUGCTRL</u>	16	Debug Control Register
110050EC	<u>I2C2_CHN_DMA_FSM_DEBUG</u>	16	Multi-DMA channel debug.
110050F0	<u>I2C2_CHN_MULTIMAS</u>	16	Multi-master control register
110050F4	<u>I2C2_CHN_FIFO_STAT</u>	16	FIFO Status Register
110050F8	<u>I2C2_CHN_FIFO_THRESH</u>	16	FIFO Thresh Register
11007F001	<u>I2C2_CHN_SEC_CONTROL</u>	16	Security Control
11007F801	<u>I2C2_CHN_CHANNEL_LOCK</u>	16	Channel lock.
11007F841	<u>I2C2_CHN_CHANNEL_SEC</u>	16	Channel security enable.
11007F881	<u>I2C2_CHN_HW_CG_EN</u>	16	HW DCM Enable
11007F8C1	<u>I2C2_CHN_MULTI_DMA</u>	16	Multi-DMA channel mode.
11007F901	<u>I2C2_CHN_DMA_REQ</u>	16	Multi-DMA channel request
11007F941	<u>I2C2_CHN_DMA_NREQ</u>	16	Multi-DMA channel request canceled.
11006000	<u>I2C_INTB</u>	16	I2C interrupt
11006004	<u>LATCH_ADDR</u>	16	Latch address
11006008	<u>RST_EN</u>	16	Reset enable
1100600C	<u>ABORT_STATUS</u>	16	Abort status
11006010	<u>SEC_EN</u>	16	Secure enable
11006014	<u>GLOBAL_SEC_EN</u>	16	Global secure enable
11006018	<u>ASYNC_CTRL</u>	16	ASYNC control
11006E00	<u>AP_CLOCK_CG_EST</u>	16	AP CLOCK CG register
11006E04	<u>AP_CLOCK_CG_CLEAR_EST</u>	16	AP CLOCK CG clear register
11006E08	<u>AP_CLOCK_CG_SET_EST</u>	16	AP CLOCK CG set register
11006E10	<u>CCU_CLOCK_CG_RO</u>	16	CCU CLOCK CG read-only register
11006E14	<u>CCU_CLOCK_CG_W1C</u>	16	CCU CLOCK CG write-1-to-clear register
11006E18	<u>CCU_CLOCK_CG_W1S</u>	16	CCU CLOCK CG write-1-to-set register
11006E20	<u>SSPM_CLOCK_CG_RO</u>	16	SSPM CLOCK CG read-only register
11006E24	<u>SSPM_CLOCK_CG_W1C</u>	16	SSPM CLOCK CG write-1-to-clear register
11006E28	<u>SSPM_CLOCK_CG_W1S</u>	16	SSPM CLOCK CG write-1-to-set register
11006E30	<u>CLOCK_SEL_RO</u>	16	CLOCK Select read-only register
11006E34	<u>CLOCK_SEL_W1C</u>	16	CLOCK Select write-1-to-clear register
11006E38	<u>CLOCK_SEL_W1S</u>	16	CLOCK Select write-1-to-set register
11006EF4	<u>CCU_INT_EN</u>	16	CCU Interrupt enable register
11006EF8	<u>CCU_INT_INV</u>	16	CCU Interrupt Inverter enable register
11006F10	<u>SEMAPHORE_0_RO</u>	16	SEMAPHORE_0 read-only register
11006F14	<u>SEMAPHORE_0_W1C</u>	16	SEMAPHORE_0 write-1-to-clear register
11006F18	<u>SEMAPHORE_0_W1S</u>	16	SEMAPHORE_0 write-1-to-set register
11006F20	<u>SEMAPHORE_1_RO</u>	16	SEMAPHORE_1 read-only register
11006F24	<u>SEMAPHORE_1_W1C</u>	16	SEMAPHORE_1 write-1-to-clear register
11006F28	<u>SEMAPHORE_1_W1S</u>	16	SEMAPHORE_1 write-1-to-set register
11006F30	<u>SEMAPHORE_2_RO</u>	16	SEMAPHORE_2 read-only register
11006F34	<u>SEMAPHORE_2_W1C</u>	16	SEMAPHORE_2 write-1-to-clear register

Address	Name	Width	Register Function
11006F38	<u>SEMAPHORE_2_W1S</u>	16	SEMAPHORE_2 write-1-to-set register
11006F00	<u>SEC_SLV_0</u>	16	Secure slave_0 register
11006F04	<u>SEC_SLV_1</u>	16	Secure slave_1 register
11006F08	<u>SEC_CCC_0</u>	16	Secure CCC_0 register
11006F0C	<u>SEC_CCC_1</u>	16	Secure CCC_1 register
11006100	<u>I2C0_SEC_SLV_EN</u>	16	I2C0 secure slave enable
11006104	<u>I2C1_SEC_SLV_EN</u>	16	I2C1 secure slave enable
11006108	<u>I2C2_SEC_SLV_EN</u>	16	I2C2 secure slave enable

11003000 I2C0_CHN_DATA_PORT Data port register 0000FF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_CONFIG_LEN								DATA_PORT							
Type	RO								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	DMA_CONFIG_LEN	DMA config length. Setting this for DMA_CONFIG_LEN*4 length.
7:0	DATA_PORT	This is the FIFO access port. During master write sequences (slave_addr[0] = 0), this port can be written by APB, and during master read sequences (slave_addr[0] = 1), this port can be read by APB. (NOTE) Slave_addr must be set correctly before accessing the FIFO. (DEBUG ONLY) If the fifo_APB_debug bit is set, then the FIFO can be read and write by the APB

11003094 I2C0_CHN_SLAVE_ADDR Slave address register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SLAVE_ADDR							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	SLAVE_ADDR	This specifies the slave address of the device to be accessed. Bit 0 is defined by the I2C protocol as a bit that indicates the direction of transfer. 1 = master read, 0 = master write.

11003008 I2C0_CHN_INTR_MASK Interrupt mask register 000001FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MAS_ERR	MAS_IBI	MAS_DMA_ERR	MAS_TIMEOUT	MAS_RS_MULTIPLE	MAS_ARB_LOST	MAS_HS_NACKER	MAS_ACKERR	MAS_TRANSAC_COMP
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
8	MAS_ERR	Setting this value to 0 will mask bus error interrupt signal.
7	MAS_IBI	Setting this value to 0 will mask IN-BAND interrupt signal.
6	MAS_DMA_ERR	Setting this value to 0 will mask DMA hand-shake error interrupt signal.
5	MAS_TIMEOUT	Setting this value to 0 will mask TIMEOUT interrupt signal.
4	MAS_RS_MULTIPLE	Setting this value to 0 will mask RS_MULTIPLE interrupt signal.
3	MAS_ARB_LOST	Setting this value to 0 will mask ARB_LOST interrupt signal.
2	MAS_HS_NACKER	Setting this value to 0 will mask HS_NACKERR interrupt signal.
1	MAS_ACKERR	Setting this value to 0 will mask ACK_ERR interrupt signal.
0	MAS_TRANSAC_COMP	Setting this value to 0 will mask TRANSAC_COMP interrupt signal.

1100300C I2C0_CHN_INTR_STAT Interrupt status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ERR	IBI	DMA_ERR	TIMEOUT	RS_MULTIPLE	ARB_LOST	HS_NACKERR	ACKERR	TRANSAC_COMP
Type								W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	ERR	This status is asserted if the I2C bus error has occurred.
7	IBI	This status is asserted if the I2C bus in-band interrupt has occurred.
6	DMA_ERR	This status is asserted if the DMA hand-shake error has occurred.
5	TIMEOUT	This status is asserted if the I2C bus time-out occurred.
4	RS_MULTIPLE	This status is asserted if the I2C controller user trigger done occurred.
3	ARB_LOST	This status is asserted if the I2C controller loses arbitration.
2	HS_NACKERR	This status is asserted if HS master code nack error detection is enabled. If enabled, HS master code nack error will cause transaction to end and stop will be issued.
1	ACKERR	This status is asserted if ACK error detection is enabled. If enabled, ackerr will cause transaction to end and stop will be issued.
0	TRANSAC_COMP	This status is asserted when a transaction has completed successfully.

11003010 I2C0_CHN_CONTROL Control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									irq_sel	TRANSFER_LENGTH	ACKERR_DET_EN	DIR_CHANGE	CLK_EXT_EN	DMA_EN	RS_STOP	forc_hs
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	irq_sel	This option controls when nack error or ack error occurs. 0: Disable 1: Enable
6	TRANSFER_LENGTH	This option specifies whether or not to change the transfer length after the first transfer completes. If enabled, the transfers after the first transfer will use the transfer_len_aux parameter.
5	ACKERR_DET_EN	This option enables slave ack error detection. When enabled, if slave ack error is detected, the master shall terminate the transaction by issuing a STOP condition and then asserts ackerr interrupt. MCU shall handle this case appropriately and then resets the FIFO address before reissuing transaction again. If this option is disabled, the controller will ignore slave ack error and keep on scheduled transaction. 0: Disable 1: Enable
4	DIR_CHANGE	This option is used for combined transfer format, where the direction of transfer is to be changed from write to read after the FIRST RS condition. Note: when set to 1, the transfers after the direction change will be based on the transfer_len_aux parameter. 0: Disable 1: Enable
3	CLK_EXT_EN	I2C spec allows slaves to hold the SCL line low if it is not yet ready for further processing. Therefore, if this bit is set to 1, master controller will enter a high wait state until the slave releases the SCL line.
2	DMA_EN	By default, this is disabled, and FIFO data shall be manually prepared by MCU. This default setting should be used for transfer sizes of less than 8 data bytes and no multiple transfer is configured. When enabled, DMA requests are turned on, and the FIFO data should be prepared in memory.
1	RS_STOP	In LS/FS mode, this bit affects multi-transfer transaction only. It controls whether or not REPEATED-START condition is used between transfers. The last ending transfer always ends with a STOP.

Bit(s)	Name	Description
		In HS mode, this bit must be set to 1.
		0: Use STOP
		1: Use REPEATED-START
0	forc_hs	Forces using high-speed timing.
		0: Disable
		1: Enable

11003014 I2C0_CHN_TRANSFER_LEN Transfer length register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSFER_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TRANSFER_LEN	This indicates the number of DATA BYTES to be transferred in 1 transfer unit (excluding slave address byte)
		(NOTE) The value must be set greater than 1; otherwise, no transfer will take place.

11003018 **I2C0_CHN_TRANSAC_LEN** Transaction length register (Number of transfers per transaction) **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TRANSAC_LEN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	TRANSAC_LEN	This indicates the number of TRANSFERS to be transferred in 1 transaction (NOTE) The value must be set greater than 1; otherwise, no transfer will take place.

1100301C **I2C0_CHN_DELAY_LEN** Inter delay length register **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DELAY_LEN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DELAY_LEN	This sets the wait delay between consecutive transfers when RS_STOP bit is set to 0. Time unit: SCL_H_TIME

11003020 I2C0_CHN_HTIMING SCL high timing control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TIMEOUT_EN	HSAMPLE_CNT_DIV			DELAY_TIME_DET		HSTEP_CNT_DIV					
Type					RW	RW			RW		RW					
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	TIMEOUT_EN	Enables hardware timeout.
10:8	HSAMPLE_CNT_DIV	Used for scl high LS/FS only. This adjusts the width of each sample. $SCL\_H\_SAMPLE\_RATE = SAMPLE\_CLK / (HSAMPLE\_CNT\_DIV + 1)$.
7:6	DELAY_TIME_DET	Used for round-trip delay detection. 0: Disable 3: Enable
5:0	HSTEP_CNT_DIV	This specifies the number of samples scl high pulse width $SCL\_H\_TIME = (HSTEP\_CNT\_DIV + 1) / SCL\_H\_SAMPLE\_RATE$.

11003024 I2C0_CHN_START Start register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RS_STOP_MULTIPLE_CONFIG	RS_STOP_MULTIPLE_TRIG	RS_STOP_MULTIPLE_TRIG_CLR												KICK_OFF	START
Type	RW	RW	RO												WO	RW
Reset	0	0	0												0	0

Bit(s)	Name	Description
15	RS_STOP_MULTIPLE_CONFIG	Enables multiple r/w & length & slave address with rs_stop transfer
14	RS_STOP_MULTIPLE_TRIG	Trigger next transfer when enable multiple r/w & length & slave address with rs_stop transfer
13	RS_STOP_MULTIPLE_TRIG_CLR	Clears the rs_stop_mul_trig for next transfer
1	KICK_OFF	Arbitration kick-off.
0	START	This register starts the transaction on the bus. It is auto deasserted at the end of the transaction.

11003028 I2C0_CHN_EXT_CONF Extension configuration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXT_TIME															EXT_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
15:8	EXT_TIME	Used for tSU;STA, tHD;STA and tSU;STO. Configurable extension time of start condition. Time unit: bclk/ (CLOCK_DIV+1)
0	EXT_EN	Used for tSU;STA, tHD;STA and tSU;STO. This option decides to perform the extension of start/stop condition. If enabled, perform the extension; otherwise, do not perform. 0: Disable 1: Enable

1100302C I2C0_CHN_LTIMING SCL low timing control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HS_HOLD_SEL	LHS_SAMPLE_CNT_DIV			LHS_STEP_CNT_DIV			LSAMPLE_CNT_DIV			LSTEP_CNT_DIV					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	HS_HOLD_SEL	High-Speed hold time control selection. 0: Disable 1: Enable
14:12	LHS_SAMPLE_CNT_DIV	Used for scl low HS only. This adjusts the width of each sample. $SCL\_L\_SAMPLE\_RATE = HS\_SAMPLE\_CLK / (LHS\_SAMPLE\_CNT\_DIV + 1)$.
11:9	LHS_STEP_CNT_DIV	This specifies the number of samples for scl low width and for HS only. $SCL\_L\_TIME = (LHS\_STEP\_CNT\_DIV + 1) / HS\_SCL\_L\_SAMPLE\_RATE$.
8:6	LSAMPLE_CNT_DIV	Used for scl low LS/FS only. This adjusts the width of each sample. $SCL\_L\_SAMPLE\_RATE = SAMPLE\_CLK / (LSAMPLE\_CNT\_DIV + 1)$.
5:0	LSTEP_CNT_DIV	This specifies the number of samples for scl low width $SCL\_L\_TIME = (LSTEP\_CNT\_DIV + 1) / SCL\_L\_SAMPLE\_RATE$.

11003030 I2C0_CHN_HS High speed mode register 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HS_HOLD_EN	HHS_SAMPLE_CNT_DIV			HS_NO_HOLD	HHS_STEP_CNT_DIV			HS_SPEED	HS_FC_STEP			HS_HOLD_TIME	HS_NACKERR_DET_EN	HS_EN	
Type	RW	RW			RW	RW			RW	RW			RW	RW	RW	
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	HS_HOLD_EN	Used for high speed mode THD;DAT only. Can be off by default. 0: Enable 1: Disable
14:12	HHS_SAMPLE_CNT_DIV	Used for scl low HS only. This adjusts the width of each sample. $SCL\_H\_SAMPLE\_RATE = HS\_SAMPLE\_CLK / (HHS\_SAMPLE\_CNT\_DIV + 1)$.
11	HS_NO_HOLD	High-Speed zero hold at ACK bit.
10:8	HHS_STEP_CNT_DIV	This specifies the number of samples for scl low width and for HS only. $SCL\_H\_TIME = (HHS\_STEP\_CNT\_DIV + 1) / HHS\_SCL\_L\_SAMPLE\_RATE$.
7	HS_SPEED	Uses high speed after common command code. 0: Disable 1: Enable
6:4	HS_FC_STEP	This register is for pad control in high speed mode.
3:2	HS_HOLD_TIME	This register is for when to sample data in high speed mode.
1	HS_NACKERR_DET_EN	This enables NACKERR detection during the master code transmission. When enabled, if NACK is not received after master code has been transmitted, the transaction will be terminated with a STOP condition.
0	HS_EN	This enables the high speed transaction. (note: rs_stop must be set to 1 as well)

11003034 I2C0_CHN_IO_CONFIG IO configuration register 00000093

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													IDLE_OE_EN	IO_SYNC_EN	SDA_IO_CONFIG	SCL_IO_CONFIG
Type													RW	RW	RW	RW
Reset													0	0	1	1

Bit(s)	Name	Description
3	IDLE_OE_EN	0: Do not drive bus in idle state 1: Drive bus in idle state
2	IO_SYNC_EN	DEBUG ONLY: When set to 1, scl and sda inputs will be first dual synced by bclk_ck. This should not be needed. Only reserved for debugging.
1	SDA_IO_CONFIG	0: Normal tristate io mode 1: Open-drain mode 0: Normal tristate io mode 1: Open-drain mode
0	SCL_IO_CONFIG	0: Normal tristate io mode 1: Open-drain mode 0: Normal tristate io mode 1: Open-drain mode

11003038 I2C0_CHN_FIFO_ADDR_CLR FIFO address clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HFIFO_ADDR_CLR	FIFO_ADDR_CLR
Type															WO	WO
Reset															0	0

Bit(s)	Name	Description
1	HFIFO_ADDR_CLR	When written with a 1, a 1 pulse fifo_addr_clr is generated to clear the FIFO address to back to 0.
0	FIFO_ADDR_CLR	When written with a 1, a 1 pulse fifo_addr_clr is generated to clear the FIFO address to back to 0.

1100303C I2C0_CHN_DATA_TIMING Data receive time adjust 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										DATA_READ_ADJ_EN	DATA_READ_ADJ					
Type										RW	RW					
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	DATA_READ_ADJ_EN	Enables data read timing adjust. 0: Disable 1: Enable
5:0	DATA_READ_ADJ	Adjusts data read timing.

11003040 I2C0_CHN_MCU_INTR MCU interrupt 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MCU_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	MCU_EN	0: Disable 1: Enable

11003044 I2C0_CHN_TRANSFER_LEN_AUX Transfer length register (Number of bytes per transfer) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSFER_LEN_AUX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TRANSFER_LEN_AUX	This field is valid only when <code>dir_change</code> or <code>transfer_len_change</code> is set to 1. Indicates the number of data bytes to be transferred in 1 transfer unit (excluding slave address byte) for the transfers following the direction change. That is, if <code>dir_change</code> =1, then the first write transfer length will depend on <code>transfer_len</code>, while the second read transfer length depend on <code>transfer_len_aux</code>. Dir change is always after the first transfer. Note: The value must be set to be bigger than 1; otherwise no transfer will take place.

11003048 I2C0_CHN_CLOCK_DIV Clock divider 0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLOCK_DIV				
Type												RW				
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:0	CLOCK_DIV	Clock divider. It will create SAMPLE_CLK which equals to (I2C module clock/ (CLOCK_DIV+1)). Default: all 1 for low-power.

1100304C I2C0_CHN_TIMEOUT_DIV Hardware timeout target 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_TIMEOUT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HW_TIMEOUT	Timeout target. Hardware will timeout when reach this number. Time unit: SCL_L_TIME

11003050 I2C0_CHN_SOFTRESET Soft reset register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													ERROR_RESET	GRANT_RESET	FSM_RESET	SOFT_RESET
Type													WO	WO	WO	WO
Reset													0	0	0	0

Bit(s)	Name	Description
3	ERROR_RESET	Resets error flag.
2	GRANT_RESET	Resets authority.
1	FSM_RESET	Resets state machine only.
0	SOFT_RESET	When written with 1, 1 pulse soft reset is used as synchronous reset to reset the I2C internal hardware circuits. This reset will cause bus charge.

110030D4 I2C0_CHN_DELAY_STEP For time stamp (I3C_EN==1) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DELAY_STEP															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DELAY_STEP	Total delay time = DELAY_STEP/SCL_H_STEP_RATE + Sample delay time

110030D8 I2C0_CHN_DELAY_SAMPLE For time stamp (I3C_EN==1) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DELAY_SAMPLE					
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	DELAY_SAMPLE	Sample delay time = (DELAY_SAMPLE+1)/SCL_H_SAMPLE_RATE

110030E4 I2C0_CHN_DEBUGSTAT Debug Status register 00006800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SDA_IN_SYNC	SCL_IN_SYNC	WR_FULL	RD_EMPTY	BUS_BUSY	MASTER_WRITE	MASTER_READ	MASTER_STATE							
Type		RO	RO	RO	RO	RO	RO	RO	RO							
Reset		1	1	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	SDA_IN_SYNC	BUS SDA status.
13	SCL_IN_SYNC	BUS SCL status.
12	WR_FULL	This indicates that the FIFO is full.
11	RD_EMPTY	This indicates that the FIFO is empty.
10	BUS_BUSY	DEBUG ONLY: valid when bus_detect_en is 1. bus_busy = 1 indicates a start transaction has been detected and no stop condition has been detected yet.
9	MASTER_WRITE	DEBUG ONLY: 1 = current transfer is in the master write dir
8	MASTER_READ	DEBUG ONLY: 1 = current transfer is in the master read dir
7:0	MASTER_STATE	DEBUG ONLY: reads back the current master_state. 0: idle state; 1: I2C master is preparing sending out the start bit, SCL=1, SDA=1; 2: I2C master is sending out the start bit, SCL=1, SDA=0; 3: I2C master/slave is preparing transmitting data bit, SCL=0, SDA=data bit (data bit can be changed when SCL=0); 4: I2C master/slave is transmitting data bit, SCL=1, SDA=data bit (data bit is stable when SCL=1); 5: I2C master/slave is preparing transmitting ack bit, SCL=0, SDA=ack (ack bit can be changed when SCL=0); 6: I2C master/slave is transmitting ack bit, SCL=1, SDA=0 (ack bit is stable when SCL=1); 7: I2C master is preparing sending out stop bit or repeated-start bit, SCL=0, SDA=0/1 (0: means stop bit; 1: means repeated-start bit); 8: I2C master is sending out stop bit or repeated-start bit, SCL=1, SDA=1/0 (1: means stop bit; 0: means repeated-start bit); 9: I2C master is in delay start between two transfers, SCL=1, SDA=1; 10: I2C master is in FIFO wait state; For writing transaction, it means FIFO is empty and I2C master is waiting for DMA controller writing data into FIFO; For reading transaction, it means FIFO is full and I2C master is

Bit(s)	Name	Description
		waiting for DMA controller reading data from FIFO, SCL=0, SDA=do not care;
		12: I2C master is preparing sending out data bit of master code. This state is used only in high-speed transaction, SCL=0, SDA=data bit of master code (data bit of master code can be changed when SCL=0);
		13: I2C master is sending out data bit of master code. This state is used only in high-speed transaction, SCL=1, SDA=data bit of master code (data bit of master code is stable when SCL=1);
		14: I2C master/slave is preparing transmitting nack bit, SCL=0, SDA=nack bit (nack bit can be changed when SCL=0); This state is used only in high-speed transaction;
		15: I2C master/slave is transmitting nack bit, SCL=1, SDA=1; This state is used only in high-speed transaction;

110030E8 I2C0_CHN_DEBUGCTRL Debug control register 0000001C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RELIABILITY	DMAACK_ENABLE		OLT_MODE	FIFO_APB_DEBUG
Type												RW	RW		RW	RW
Reset												1	1		0	0

Bit(s)	Name	Description
4	RELIABILITY	0: Disable 1: Enable
3	DMAACK_ENABLE	Snoop DMA ack for early terminate DMA request. 0: Disable 1: Enable
1	OLT_MODE	Use for olt only. 0: Disable 1: Enable
0	FIFO_APB_DEBUG	This is used for trace32 debug purposes. When using trace32, and the memory map is shown, turning this bit on will block the normal APB read access. APB read access to the FIFO is then enabled by writing to APB_debug_rd. 0: Disable 1: Enable

110030EC I2C0_CHN_DMA_FSM_DEBU Multi-DMA channel debug

00000000

G

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I3C_EN	APB_ID											FSM_STAT			
Type	RO	RO											RO			
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	I3C_EN	I3C enable 0: I2C 1: I3C
14:8	APB_ID	If (APB_ID < 32), this design is in perisys. Else, this design is in other HW domain.
3:0	FSM_STAT	FSM status. 0x7: Wait for IRQ clean 0xc: Wait for kick-off

110030F0 I2C0_CHN_MULTIMAS Multi-master control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														BUS_DETECT_EN	CLK_SYNC_EN	ARB_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	BUS_DETECT_EN	When enabled, the bus status is monitored. If bus is currently busy, no new transaction can proceed. 0: Disable 1: Enable
1	CLK_SYNC_EN	When enabled, clk sync will be performed. 0: Disable 1: Enable
0	ARB_EN	When enabled, multi-master arbitration will be performed. 0: Disable 1: Enable

110030F4 I2C0_CHN_FIFO_STAT FIFO Status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RD_ADDR					WR_ADDR					FIFO_OFFSET				
Type		RO					RO					RO				
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:10	RD_ADDR	The current rd address pointer. (only bit [2:0] has physical meaning)
9:5	WR_ADDR	The current wr address pointer. (only bit [2:0] has physical meaning)
4:0	FIFO_OFFSET	wr_addr[3:0] - rd_addr[3:0]

110030F8 I2C0_CHN_FIFO_THRESH FIFO Thresh register 00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_TRIG_THRESH								RX_TRIG_THRESH			
Type					RW								RW			
Reset					1	1	1	1					0	0	0	0

Bit(s)	Name	Description
11:8	TX_TRIG_THRESH	When TX FIFO level is below this value, TX DMA request is asserted.
3:0	RX_TRIG_THRESH	When RX FIFO level is above this value, RX DMA request is asserted.

11007F00 I2C0_CHN_SEC_CONTROL Security control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SKIP_S LAVE_ ADDR_ OFF	DAA_E N_OFF
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	SKIP_SLAVE_ADDR_OFF	Forces skip slave address off.
0	DAA_EN_OFF	Forces daa enable off.

11007F80 I2C0_CHN_CHANNEL_LOCK Channel lock 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CHANNEL_LOCK				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	CHANNEL_LOCK	Channel has been locked since security issue.
		0: Disable
		1: Enable

11007F84 I2C0_CHN_CHANNEL_SEC Channel security enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CHANNEL_SEC				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	CHANNEL_SEC	Channel which should be protected. 0: Disable 1: Enable

11007F88 I2C0_CHN_HW.CG_EN HW DCM Enable 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DCM_ULPOWER	DCM_13M_EN	DCM_INTF_EN	DCM_EN
Type													RW	RW	RW	RW
Reset													1	1	1	1

Bit(s)	Name	Description
3	DCM_ULPOWER	When enabled, most register clock will be set to 4 * scl. 0: Disable 1: Enable
2	DCM_13M_EN	When enable, it's aligned to DCM_EN. 0: Disable 1: Enable
1	DCM_INTF_EN	DCM for DMA interface. 0: Disable 1: Enable
0	DCM_EN	Enables HW DCM function. Default is disable. 0: Disable 1: Enable

11007F8C I2C0_CHN_MULTI_DMA Multi-DMA channel mode 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	APB_SET				SIDE_SET				IRQ_SET_EN					DMA_CONFIG_MODE	SHADOW_REG_MODE	TRIGGER_ENABLE
Type	RO				RO				RO					RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0					0	0	0

Bit(s)	Name	Description
15:12	APB_SET	APB setting register
11:8	SIDE_SET	SIDE setting register
7	IRQ_SET_EN	Interrupt setting enable register
2	DMA_CONFIG_MODE	Enables multi-DMA channel mode. 0: Disable 1: Enable
1	SHADOW_REG_MODE	Enables shadow register configuration mode. 0: Disable 1: Enable
0	TRIGGER_ENABLE	Enables side-band trigger I2C. 0: Disable 1: Enable

11007F90 **I2C0_CHN_DMA_REQ** **Multi-DMA channel request** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_REQ			
Type													RO			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DMA_REQ	Request for relative DMA channel.

11007F94 **I2C0_CHN_DMA_NREQ** **Multi-DMA channel request canceled** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_NREQ			
Type													RO			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DMA_NREQ	Cancel request for relative DMA channel.

11004000 I2C1_CHN_DATA_PORT Data port register 0000FF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_CONFIG_LEN								DATA_PORT							
Type	RO								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	DMA_CONFIG_LEN	DMA config length. Setting this for DMA_CONFIG_LEN*4 length.
7:0	DATA_PORT	This is the FIFO access port. During master write sequences (slave_addr[0] = 0), this port can be written by APB, and during master read sequences (slave_addr[0] = 1), this port can be read by APB. (NOTE) Slave_addr must be set correctly before accessing the FIFO. (DEBUG ONLY) If the fifo_APB_debug bit is set, then the FIFO can be read and write by the APB

11004094 I2C1_CHN_SLAVE_ADDR Slave address register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SLAVE_ADDR							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	SLAVE_ADDR	This specifies the slave address of the device to be accessed. Bit 0 is defined by the I2C protocol as a bit that indicates the direction of transfer. 1 = master read, 0 = master write.

11004008 I2C1_CHN_INTR_MASK Interrupt mask register 000001FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MAS_ERR	MAS_IBI	MAS_DMA_ERR	MAS_TIMEOUT	MAS_RS_MULTIPLE	MAS_ARB_LOST	MAS_HS_NACKER	MAS_ACKERR	MAS_TRANSAC_COMP
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
8	MAS_ERR	Setting this value to 0 will mask bus error interrupt signal.
7	MAS_IBI	Setting this value to 0 will mask IN-BAND interrupt signal.
6	MAS_DMA_ERR	Setting this value to 0 will mask DMA hand-shake error interrupt signal.
5	MAS_TIMEOUT	Setting this value to 0 will mask TIMEOUT interrupt signal.
4	MAS_RS_MULTIPLE	Setting this value to 0 will mask RS_MULTIPLE interrupt signal.
3	MAS_ARB_LOST	Setting this value to 0 will mask ARB_LOST interrupt signal.
2	MAS_HS_NACKER	Setting this value to 0 will mask HS_NACKERR interrupt signal.
1	MAS_ACKERR	Setting this value to 0 will mask ACK_ERR interrupt signal.
0	MAS_TRANSAC_COMP	Setting this value to 0 will mask TRANSAC_COMP interrupt signal.

1100400C I2C1_CHN_INTR_STAT Interrupt status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ERR	IBI	DMA_ERR	TIMEOUT	RS_MULTIPLE	ARB_LOST	HS_NACKERR	ACKERR	TRANSAC_COMP
Type								W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	ERR	This status is asserted if the I2C bus error has occurred.
7	IBI	This status is asserted if the I2C bus in-band interrupt has occurred.
6	DMA_ERR	This status is asserted if the DMA hand-shake error has occurred.
5	TIMEOUT	This status is asserted if the I2C bus time-out occurred.
4	RS_MULTIPLE	This status is asserted if the I2C controller user trigger done occurred.
3	ARB_LOST	This status is asserted if the I2C controller loses arbitration.
2	HS_NACKERR	This status is asserted if HS master code nack error detection is enabled. If enabled, HS master code nack error will cause transaction to end and stop will be issued.
1	ACKERR	This status is asserted if ACK error detection is enabled. If enabled, ackerr will cause transaction to end and stop will be issued.
0	TRANSAC_COMP	This status is asserted when a transaction has completed successfully.

11004010 I2C1_CHN_CONTROL Control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									irq_sel	TRANSFER_LENGTH	ACKERR_DET_EN	DIR_CHANGE	CLK_EXT_EN	DMA_EN	RS_STOP	forc_hs
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	irq_sel	This option controls when nack error or ack error occurs. 0: Disable 1: Enable
6	TRANSFER_LENGTH	This option specifies whether or not to change the transfer length after the first transfer completes. If enabled, the transfers after the first transfer will use the transfer_len_aux parameter.
5	ACKERR_DET_EN	This option enables slave ack error detection. When enabled, if slave ack error is detected, the master shall terminate the transaction by issuing a STOP condition and then asserts ackerr interrupt. MCU shall handle this case appropriately and then resets the FIFO address before reissuing transaction again. If this option is disabled, the controller will ignore slave ack error and keep on scheduled transaction. 0: Disable 1: Enable
4	DIR_CHANGE	This option is used for combined transfer format, where the direction of transfer is to be changed from write to read after the FIRST RS condition. Note: when set to 1, the transfers after the direction change will be based on the transfer_len_aux parameter. 0: Disable 1: Enable
3	CLK_EXT_EN	I2C spec allows slaves to hold the SCL line low if it is not yet ready for further processing. Therefore, if this bit is set to 1, master controller will enter a high wait state until the slave releases the SCL line.
2	DMA_EN	By default, this is disabled, and FIFO data shall be manually prepared by MCU. This default setting should be used for transfer sizes of less than 8 data bytes and no multiple transfer is configured. When enabled, DMA requests are turned on, and the FIFO data should be prepared in memory.
1	RS_STOP	In LS/FS mode, this bit affects multi-transfer transaction only. It controls whether or not REPEATED-START condition is used between transfers. The last ending transfer always ends with a STOP.

Bit(s)	Name	Description
		In HS mode, this bit must be set to 1.
		0: Use STOP
		1: Use REPEATED-START
0	forc_hs	Forces using high-speed timing.
		0: Disable
		1: Enable

11004014 I2C1_CHN_TRANSFER_LEN Transfer length register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSFER_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TRANSFER_LEN	This indicates the number of DATA BYTES to be transferred in 1 transfer unit (excluding slave address byte)
		(NOTE) The value must be set greater than 1; otherwise, no transfer will take place.

11004018 **I2C1_CHN_TRANSAC_LEN** Transaction length register (Number of transfers per transaction) **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TRANSAC_LEN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	TRANSAC_LEN	This indicates the number of TRANSFERS to be transferred in 1 transaction (NOTE) The value must be set greater than 1; otherwise, no transfer will take place.

1100401C **I2C1_CHN_DELAY_LEN** Inter delay length register **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DELAY_LEN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DELAY_LEN	This sets the wait delay between consecutive transfers when RS_STOP bit is set to 0. Time unit: SCL_H_TIME

11004020 I2C1_CHN_HTIMING SCL high timing control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TIMEOUT_EN	HSAMPLE_CNT_DIV			DELAY_TIME_DET		HSTEP_CNT_DIV					
Type					RW	RW			RW		RW					
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	TIMEOUT_EN	Enables hardware timeout.
10:8	HSAMPLE_CNT_DIV	Used for scl high LS/FS only. This adjusts the width of each sample. $SCL\_H\_SAMPLE\_RATE = SAMPLE\_CLK / (HSAMPLE\_CNT\_DIV + 1)$.
7:6	DELAY_TIME_DET	Used for round-trip delay detection. 0: Disable 3: Enable
5:0	HSTEP_CNT_DIV	This specifies the number of samples scl high pulse width $SCL\_H\_TIME = (HSTEP\_CNT\_DIV + 1) / SCL\_H\_SAMPLE\_RATE$.

11004024 I2C1_CHN_START Start register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RS_STOP_MULTIPLE_CONFIG	RS_STOP_MULTIPLE_TRIG	RS_STOP_MULTIPLE_TRIG_CLR												KICK_OFF	START
Type	RW	RW	RO												WO	RW
Reset	0	0	0												0	0

Bit(s)	Name	Description
15	RS_STOP_MULTIPLE_CONFIG	Enables multiple r/w & length & slave address with rs_stop transfer
14	RS_STOP_MULTIPLE_TRIG	Trigger next transfer when enable multiple r/w & length & slave address with rs_stop transfer
13	RS_STOP_MULTIPLE_TRIG_CLR	Clears the rs_stop_mul_trig for next transfer
1	KICK_OFF	Arbitration kick-off.
0	START	This register starts the transaction on the bus. It is auto deasserted at the end of the transaction.

11004028 I2C1_CHN_EXT_CONF Extension configuration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXT_TIME															EXT_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
15:8	EXT_TIME	Used for tSU;STA, tHD;STA and tSU;STO. Configurable extension time of start condition. Time unit: bclk/ (CLOCK_DIV+1)
0	EXT_EN	Used for tSU;STA, tHD;STA and tSU;STO. This option decides to perform the extension of start/stop condition. If enabled, perform the extension; otherwise, do not perform. 0: Disable 1: Enable

1100402C **I2C1_CHN_LTIMING** **SCL low timing control register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HS_HOLD_SEL	LHS_SAMPLE_CNT_DIV			LHS_STEP_CNT_DIV			LSAMPLE_CNT_DIV			LSTEP_CNT_DIV					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	HS_HOLD_SEL	High-Speed hold time control selection. 0: Disable 1: Enable
14:12	LHS_SAMPLE_CNT_DIV	Used for scl low HS only. This adjusts the width of each sample. $SCL\_L\_SAMPLE\_RATE = HS\_SAMPLE\_CLK / (LHS\_SAMPLE\_CNT\_DIV + 1)$.
11:9	LHS_STEP_CNT_DIV	This specifies the number of samples for scl low width and for HS only. $SCL\_L\_TIME = (LHS\_STEP\_CNT\_DIV + 1) / HS\_SCL\_L\_SAMPLE\_RATE$.
8:6	LSAMPLE_CNT_DIV	Used for scl low LS/FS only. This adjusts the width of each sample. $SCL\_L\_SAMPLE\_RATE = SAMPLE\_CLK / (LSAMPLE\_CNT\_DIV + 1)$.
5:0	LSTEP_CNT_DIV	This specifies the number of samples for scl low width $SCL\_L\_TIME = (LSTEP\_CNT\_DIV + 1) / SCL\_L\_SAMPLE\_RATE$.

11004030 I2C1_CHN_HS High speed mode register 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HS_HOLD_EN	HHS_SAMPLE_CNT_DIV			HS_NO_HOLD	HHS_STEP_CNT_DIV			HS_SPEED	HS_FC_STEP			HS_HOLD_TIME		HS_NACKERR_DET_EN	HS_EN
Type	RW	RW			RW	RW			RW	RW			RW		RW	RW
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	HS_HOLD_EN	Used for high speed mode THD;DAT only. Can be off by default. 0: Enable 1: Disable
14:12	HHS_SAMPLE_CNT_DIV	Used for scl low HS only. This adjusts the width of each sample. $SCL\_H\_SAMPLE\_RATE = HS\_SAMPLE\_CLK / (HHS\_SAMPLE\_CNT\_DIV + 1)$.
11	HS_NO_HOLD	High-Speed zero hold at ACK bit.
10:8	HHS_STEP_CNT_DIV	This specifies the number of samples for scl low width and for HS only. $SCL\_H\_TIME = (HHS\_STEP\_CNT\_DIV + 1) / HHS\_SCL\_L\_SAMPLE\_RATE$.
7	HS_SPEED	Uses high speed after common command code. 0: Disable 1: Enable
6:4	HS_FC_STEP	This register is for pad control in high speed mode.
3:2	HS_HOLD_TIME	This register is for when to sample data in high speed mode.
1	HS_NACKERR_DET_EN	This enables NACKERR detection during the master code transmission. When enabled, if NACK is not received after master code has been transmitted, the transaction will be terminated with a STOP condition.
0	HS_EN	This enables the high speed transaction. (note: rs_stop must be set to 1 as well)

11004034 I2C1_CHN_IO_CONFIG IO configuration register 00000093

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													IDLE_OE_EN	IO_SYNC_EN	SDA_IO_CONFIG	SCL_IO_CONFIG
Type													RW	RW	RW	RW
Reset													0	0	1	1

Bit(s)	Name	Description
3	IDLE_OE_EN	0: Do not drive bus in idle state 1: Drive bus in idle state
2	IO_SYNC_EN	DEBUG ONLY: When set to 1, scl and sda inputs will be first dual synced by bclk_ck. This should not be needed. Only reserved for debugging.
1	SDA_IO_CONFIG	0: Normal tristate io mode 1: Open-drain mode 0: Normal tristate io mode 1: Open-drain mode
0	SCL_IO_CONFIG	0: Normal tristate io mode 1: Open-drain mode 0: Normal tristate io mode 1: Open-drain mode

11004038 I2C1_CHN_FIFO_ADDR_CLR FIFO address clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HFIFO_ADDR_CLR	FIFO_ADDR_CLR
Type															WO	WO
Reset															0	0

Bit(s)	Name	Description
1	HFIFO_ADDR_CLR	When written with a 1, a 1 pulse fifo_addr_clr is generated to clear the FIFO address to back to 0.
0	FIFO_ADDR_CLR	When written with a 1, a 1 pulse fifo_addr_clr is generated to clear the FIFO address to back to 0.

1100403C I2C1_CHN_DATA_TIMING Data receive time adjust 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										DATA_READ_ADJ_EN	DATA_READ_ADJ					
Type										RW	RW					
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	DATA_READ_ADJ_EN	Enables data read timing adjust. 0: Disable 1: Enable
5:0	DATA_READ_ADJ	Adjusts data read timing.

11004040 I2C1_CHN_MCU_INTR MCU interrupt 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MCU_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	MCU_EN	0: Disable 1: Enable

11004044 I2C1_CHN_TRANSFER_LEN_AUX Transfer length register (Number of bytes per transfer) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSFER_LEN_AUX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TRANSFER_LEN_AUX	This field is valid only when dir_change or transfer_len_change is set to 1. Indicates the number of data bytes to be transferred in 1 transfer unit (excluding slave address byte) for the transfers following the direction change. That is, if dir_change =1, then the first write transfer length will depend on transfer_len, while the second read transfer length depend on transfer_len_aux. Dir change is always after the first transfer. Note: The value must be set to be bigger than 1; otherwise no transfer will take place.

11004048 I2C1_CHN_CLOCK_DIV Clock divider 0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLOCK_DIV				
Type												RW				
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:0	CLOCK_DIV	Clock divider. It will create SAMPLE_CLK which equals to (I2C module clock/ (CLOCK_DIV+1)). Default: all 1 for low-power.

1100404C I2C1_CHN_TIMEOUT_DIV Hardware timeout target 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_TIMEOUT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HW_TIMEOUT	Timeout target. Hardware will timeout when reach this number. Time unit: SCL_L_TIME

11004050 I2C1_CHN_SOFTRESET Soft reset register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													ERROR _RESET	GRANT _RESET	FSM_R ESET	SOFT_ RESET
Type													WO	WO	WO	WO
Reset													0	0	0	0

Bit(s)	Name	Description
3	ERROR_RESET	Resets error flag.
2	GRANT_RESET	Resets authority.
1	FSM_RESET	Resets state machine only.
0	SOFT_RESET	When written with 1, 1 pulse soft reset is used as synchronous reset to reset the I2C internal hardware circuits. This reset will cause bus charge.

110040D4 I2C1_CHN_DELAY_STEP For time stamp (I3C_EN==1) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DELAY_STEP															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DELAY_STEP	Total delay time = DELAY_STEP/SCL_H_STEP_RATE + Sample delay time

110040D8 I2C1_CHN_DELAY_SAMPLE For time stamp (I3C_EN==1) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DELAY_SAMPLE					
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	DELAY_SAMPLE	Sample delay time = (DELAY_SAMPLE+1)/SCL_H_SAMPLE_RATE

110040E4 I2C1_CHN_DEBUGSTAT Debug Status Register 00006800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SDA_IN_SYNC	SCL_IN_SYNC	WR_FULL	RD_EMPTY	BUS_BUSY	MASTER_WRITE	MASTER_READ	MASTER_STATE							
Type		RO	RO	RO	RO	RO	RO	RO	RO							
Reset		1	1	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	SDA_IN_SYNC	BUS SDA status.
13	SCL_IN_SYNC	BUS SCL status.
12	WR_FULL	This indicates that the FIFO is full.
11	RD_EMPTY	This indicates that the FIFO is empty.
10	BUS_BUSY	DEBUG ONLY: valid when bus_detect_en is 1. bus_busy = 1 indicates a start transaction has been detected and no stop condition has been detected yet.
9	MASTER_WRITE	DEBUG ONLY: 1 = current transfer is in the master write dir
8	MASTER_READ	DEBUG ONLY: 1 = current transfer is in the master read dir
7:0	MASTER_STATE	DEBUG ONLY: reads back the current master_state. 0: idle state; 1: I2C master is preparing sending out the start bit, SCL=1, SDA=1; 2: I2C master is sending out the start bit, SCL=1, SDA=0; 3: I2C master/slave is preparing transmitting data bit, SCL=0, SDA=data bit (data bit can be changed when SCL=0); 4: I2C master/slave is transmitting data bit, SCL=1, SDA=data bit (data bit is stable when SCL=1); 5: I2C master/slave is preparing transmitting ack bit, SCL=0, SDA=ack (ack bit can be changed when SCL=0); 6: I2C master/slave is transmitting ack bit, SCL=1, SDA=0 (ack bit is stable when SCL=1); 7: I2C master is preparing sending out stop bit or repeated-start bit, SCL=0, SDA=0/1 (0: means stop bit; 1: means repeated-start bit); 8: I2C master is sending out stop bit or repeated-start bit, SCL=1, SDA=1/0 (1: means stop bit; 0: means repeated-start bit); 9: I2C master is in delay start between two transfers, SCL=1, SDA=1; 10: I2C master is in FIFO wait state; For writing transaction, it means FIFO is empty and I2C master is waiting for DMA controller writing data into FIFO; For reading transaction, it means FIFO is full and I2C master is

Bit(s)	Name	Description
		waiting for DMA controller reading data from FIFO, SCL=0, SDA=do not care;
		12: I2C master is preparing sending out data bit of master code. This state is used only in high-speed transaction, SCL=0, SDA=data bit of master code (data bit of master code can be changed when SCL=0);
		13: I2C master is sending out data bit of master code. This state is used only in high-speed transaction, SCL=1, SDA=data bit of master code (data bit of master code is stable when SCL=1);
		14: I2C master/slave is preparing transmitting nack bit, SCL=0, SDA=nack bit (nack bit can be changed when SCL=0); This state is used only in high-speed transaction;
		15: I2C master/slave is transmitting nack bit, SCL=1, SDA=1; This state is used only in high-speed transaction;

110040E8 I2C1_CHN_DEBUGCTRL Debug Control Register 0000001C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RELIABILITY	DMAACK_ENABLE		OLT_MODE	FIFO_APB_DEBUG
Type												RW	RW		RW	RW
Reset												1	1		0	0

Bit(s)	Name	Description
4	RELIABILITY	0: Disable 1: Enable
3	DMAACK_ENABLE	Snoop DMA ack for early terminate DMA request. 0: Disable 1: Enable
1	OLT_MODE	Use for olt only. 0: Disable 1: Enable
0	FIFO_APB_DEBUG	This is used for trace32 debug purposes. When using trace32, and the memory map is shown, turning this bit on will block the normal APB read access. APB read access to the FIFO is then enabled by writing to APB_debug_rd. 0: Disable 1: Enable

110040EC I2C1_CHN_DMA_FSM_DEBU Multi-DMA channel debug.

00000000

G

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I3C_EN	APB_ID											FSM_STAT			
Type	RO	RO											RO			
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	I3C_EN	I3C enable 0: I2C 1: I3C
14:8	APB_ID	If (APB_ID < 32), this design is in perisys. Else, this design is in other HW domain.
3:0	FSM_STAT	FSM status. 0x7: Wait for IRQ clean 0xc: Wait for kick-off

110040F0 I2C1_CHN_MULTIMAS Multi-master control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														BUS_DETECT_EN	CLK_SYNC_EN	ARB_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	BUS_DETECT_EN	When enabled, the bus status is monitored. If bus is currently busy, no new transaction can proceed. 0: Disable 1: Enable
1	CLK_SYNC_EN	When enabled, clk sync will be performed. 0: Disable 1: Enable
0	ARB_EN	When enabled, multi-master arbitration will be performed. 0: Disable 1: Enable

110040F4 I2C1_CHN_FIFO_STAT FIFO Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RD_ADDR					WR_ADDR					FIFO_OFFSET				
Type		RO					RO					RO				
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:10	RD_ADDR	The current rd address pointer. (only bit [2:0] has physical meaning)
9:5	WR_ADDR	The current wr address pointer. (only bit [2:0] has physical meaning)
4:0	FIFO_OFFSET	wr_addr[3:0] - rd_addr[3:0]

110040F8 I2C1_CHN_FIFO_THRESH FIFO Thresh Register 00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_TRIG_THRESH								RX_TRIG_THRESH			
Type					RW								RW			
Reset					1	1	1	1					0	0	0	0

Bit(s)	Name	Description
11:8	TX_TRIG_THRESH	When TX FIFO level is below this value, TX DMA request is asserted.
3:0	RX_TRIG_THRESH	When RX FIFO level is above this value, RX DMA request is asserted.

11007F000 I2C1_CHN_SEC_CONTROL Security Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SKIP_S LAVE_ ADDR_ OFF	DAA_E N_OFF
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	SKIP_SLAVE_ADDR_OFF	Forces skip slave address off.
0	DAA_EN_OFF	Forces daa enable off.

11007F800 I2C1_CHN_CHANNEL_LOCK Channel lock. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CHANNEL_LOCK				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	CHANNEL_LOCK	Channel has been locked since security issue. 0: Disable 1: Enable

11007F840 I2C1_CHN_CHANNEL_SEC Channel security enable. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CHANNEL_SEC				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	CHANNEL_SEC	Channel which should be protected. 0: Disable 1: Enable

11007F880 I2C1_CHN_HW.CG_EN HW DCM Enable 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DCM_ULPOWER	DCM_13M_EN	DCM_INTF_EN	DCM_EN
Type													RW	RW	RW	RW
Reset													1	1	1	1

Bit(s)	Name	Description
3	DCM_ULPOWER	When enabled, most register clock will be set to 4 * scl. 0: Disable 1: Enable
2	DCM_13M_EN	When enable, it's aligned to DCM_EN. 0: Disable 1: Enable
1	DCM_INTF_EN	DCM for DMA interface. 0: Disable 1: Enable
0	DCM_EN	Enables HW DCM function. Default is disable. 0: Disable 1: Enable

11007F8C0 I2C1_CHN_MULTI_DMA Multi-DMA channel mode. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	APB_SET				SIDE_SET				IRQ_SET_EN					DMA_CONFIG_MODE	SHADOW_REG_MODE	TRIGGER_ENABLE
Type	RO				RO				RO					RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0					0	0	0

Bit(s)	Name	Description
15:12	APB_SET	APB setting register
11:8	SIDE_SET	SIDE setting register
7	IRQ_SET_EN	Interrupt setting enable register
2	DMA_CONFIG_MODE	Enables multi-DMA channel mode. 0: Disable 1: Enable
1	SHADOW_REG_MODE	Enables shadow register configuration mode. 0: Disable 1: Enable
0	TRIGGER_ENABLE	Enables side-band trigger I2C. 0: Disable 1: Enable

11007F900 I2C1_CHN_DMA_REQ Multi-DMA channel request 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_REQ			
Type													RO			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DMA_REQ	Request for relative DMA channel.

11007F940 I2C1_CHN_DMA_NREQ Multi-DMA channel request canceled. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_NREQ			
Type													RO			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DMA_NREQ	Cancel request for relative DMA channel.

11005000 I2C2_CHN_DATA_PORT Data port register 0000FF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_CONFIG_LEN								DATA_PORT							
Type	RO								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	DMA_CONFIG_LEN	DMA config length. Setting this for DMA_CONFIG_LEN*4 length.
7:0	DATA_PORT	This is the FIFO access port. During master write sequences (slave_addr[0] = 0), this port can be written by APB, and during master read sequences (slave_addr[0] = 1), this port can be read by APB. (NOTE) Slave_addr must be set correctly before accessing the FIFO. (DEBUG ONLY) If the fifo_APB_debug bit is set, then the FIFO can be read and write by the APB

11005094 I2C2_CHN_SLAVE_ADDR Slave address register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SLAVE_ADDR							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	SLAVE_ADDR	This specifies the slave address of the device to be accessed. Bit 0 is defined by the I2C protocol as a bit that indicates the direction of transfer. 1 = master read, 0 = master write.

11005008 I2C2_CHN_INTR_MASK Interrupt mask register 000001FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MAS_ERR	MAS_IBI	MAS_DMA_ERR	MAS_TIMEOUT	MAS_RS_MULTIPLE	MAS_ARB_LOST	MAS_HS_NACKER	MAS_ACKERR	MAS_TRANSAC_COMP
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
8	MAS_ERR	Setting this value to 0 will mask bus error interrupt signal.
7	MAS_IBI	Setting this value to 0 will mask IN-BAND interrupt signal.
6	MAS_DMA_ERR	Setting this value to 0 will mask DMA hand-shake error interrupt signal.
5	MAS_TIMEOUT	Setting this value to 0 will mask TIMEOUT interrupt signal.
4	MAS_RS_MULTIPLE	Setting this value to 0 will mask RS_MULTIPLE interrupt signal.
3	MAS_ARB_LOST	Setting this value to 0 will mask ARB_LOST interrupt signal.
2	MAS_HS_NACKER	Setting this value to 0 will mask HS_NACKERR interrupt signal.
1	MAS_ACKERR	Setting this value to 0 will mask ACK_ERR interrupt signal.
0	MAS_TRANSAC_COMP	Setting this value to 0 will mask TRANSAC_COMP interrupt signal.

1100500C I2C2_CHN_INTR_STAT Interrupt status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ERR	IBI	DMA_ERR	TIMEOUT	RS_MULTIPLE	ARB_LOST	HS_NACKERR	ACKERR	TRANSACTION_COMPLETED
Type								W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	ERR	This status is asserted if the I2C bus error has occurred.
7	IBI	This status is asserted if the I2C bus in-band interrupt has occurred.
6	DMA_ERR	This status is asserted if the DMA hand-shake error has occurred.
5	TIMEOUT	This status is asserted if the I2C bus time-out occurred.
4	RS_MULTIPLE	This status is asserted if the I2C controller user trigger done occurred.
3	ARB_LOST	This status is asserted if the I2C controller loses arbitration.
2	HS_NACKERR	This status is asserted if HS master code nack error detection is enabled. If enabled, HS master code nack error will cause transaction to end and stop will be issued.
1	ACKERR	This status is asserted if ACK error detection is enabled. If enabled, ackerr will cause transaction to end and stop will be issued.
0	TRANSACTION_COMPLETED	This status is asserted when a transaction has completed successfully.

11005010 I2C2_CHN_CONTROL Control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									irq_sel	TRANSFER_LENGTH	ACKERR_DET_EN	DIR_CHANGE	CLK_EXT_EN	DMA_EN	RS_STOP	forc_hs
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	irq_sel	This option controls when nack error or ack error occurs. 0: Disable 1: Enable
6	TRANSFER_LENGTH_CHANGE	This option specifies whether or not to change the transfer length after the first transfer completes. If enabled, the transfers after the first transfer will use the transfer_len_aux parameter.
5	ACKERR_DET_EN	This option enables slave ack error detection. When enabled, if slave ack error is detected, the master shall terminate the transaction by issuing a STOP condition and then asserts ackerr interrupt. MCU shall handle this case appropriately and then resets the fifo address before reissuing transaction again. If this option is disabled, the controller will ignore slave ack error and keep on scheduled transaction. 0: Disable 1: Enable
4	DIR_CHANGE	This option is used for combined transfer format, where the direction of transfer is to be changed from write to read after the FIRST RS condition. Note: when set to 1, the transfers after the direction change will be based on the transfer_len_aux parameter. 0: Disable 1: Enable
3	CLK_EXT_EN	I2C spec allows slaves to hold the SCL line low if it is not yet ready for further processing. Therefore, if this bit is set to 1, master controller will enter a high wait state until the slave releases the SCL line.
2	DMA_EN	By default, this is disabled, and fifo data shall be manually prepared by MCU. This default setting should be used for transfer sizes of less than 8 data bytes and no multiple transfer is configured. When enabled, DMA requests are turned on, and the fifo data should be prepared in memory.
1	RS_STOP	In LS/FS mode, this bit affects multi-transfer transaction only. It controls whether or not REPEATED-START condition is used between transfers. The last ending transfer always ends with a STOP.

Bit(s)	Name	Description
		In HS mode, this bit must be set to 1.
		0: Use STOP
		1: Use REPEATED-START
0	forc_hs	Forces using high-speed timing.
		0: Disable
		1: Enable

11005014 I2C2_CHN_TRANSFER_LEN Transfer length register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSFER_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TRANSFER_LEN	This indicates the number of DATA BYTES to be transferred in 1 transfer unit (excluding slave address byte)
		(NOTE) The value must be set greater than 1; otherwise, no transfer will take place.

11005018 **I2C2_CHN_TRANSAC_LEN** Transaction length register (Number of transfers per transaction) **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TRANSAC_LEN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	TRANSAC_LEN	This indicates the number of TRANSFERS to be transferred in 1 transaction (NOTE) The value must be set greater than 1; otherwise, no transfer will take place.

1100501C **I2C2_CHN_DELAY_LEN** Inter delay length register **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DELAY_LEN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DELAY_LEN	This sets the wait delay between consecutive transfers when RS_STOP bit is set to 0. Time unit: SCL_H_TIME

11005020 I2C2_CHN_HTIMING SCL high timing control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TIMEOUT_EN	HSAMPLE_CNT_DIV			DELAY_TIME_DET		HSTEP_CNT_DIV					
Type					RW	RW			RW		RW					
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	TIMEOUT_EN	Enables hardware timeout.
10:8	HSAMPLE_CNT_DIV	Used for scl high LS/FS only. This adjusts the width of each sample. $SCL\_H\_SAMPLE\_RATE = SAMPLE\_CLK / (HSAMPLE\_CNT\_DIV + 1)$.
7:6	DELAY_TIME_DET	Used for round-trip delay detection. 0: Disable 3: Enable
5:0	HSTEP_CNT_DIV	This specifies the number of samples scl high pulse width $SCL\_H\_TIME = (HSTEP\_CNT\_DIV + 1) / SCL\_H\_SAMPLE\_RATE$.

11005024 I2C2_CHN_START Start register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RS_STOP_MULTIPLE_CONFIG	RS_STOP_MULTIPLE_TRIG	RS_STOP_MULTIPLE_TRIG_CLR												KICK_OFF	START
Type	RW	RW	RO												WO	RW
Reset	0	0	0												0	0

Bit(s)	Name	Description
15	RS_STOP_MULTIPLE_CONFIG	Enables multiple r/w & length & slave address with rs_stop transfer
14	RS_STOP_MULTIPLE_TRIG	Trigger next transfer when enable multiple r/w & length & slave address with rs_stop transfer
13	RS_STOP_MULTIPLE_TRIG_CLR	Clears the rs_stop_mul_trig for next transfer
1	KICK_OFF	Arbitration kick-off.
0	START	This register starts the transaction on the bus. It is auto deasserted at the end of the transaction.

11005028 I2C2_CHN_EXT_CONF Extension configuration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXT_TIME															EXT_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
15:8	EXT_TIME	Used for tSU;STA, tHD;STA and tSU;STO. Configurable extension time of start condition. Time unit: bclk/ (CLOCK_DIV+1)
0	EXT_EN	Used for tSU;STA, tHD;STA and tSU;STO. This option decides to perform the extension of start/stop condition. If enabled, perform the extension; otherwise, do not perform. 0: Disable 1: Enable

1100502C I2C2_CHN_LTIMING SCL low timing control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HS_HOLD_SEL	LHS_SAMPLE_CNT_DIV			LHS_STEP_CNT_DIV			LSAMPLE_CNT_DIV			LSTEP_CNT_DIV					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	HS_HOLD_SEL	High-Speed hold time control selection. 0: Disable 1: Enable
14:12	LHS_SAMPLE_CNT_DIV	Used for scl low HS only. This adjusts the width of each sample. $SCL\_L\_SAMPLE\_RATE = HS\_SAMPLE\_CLK / (LHS\_SAMPLE\_CNT\_DIV + 1)$.
11:9	LHS_STEP_CNT_DIV	This specifies the number of samples for scl low width and for HS only. $SCL\_L\_TIME = (LHS\_STEP\_CNT\_DIV + 1) / HS\_SCL\_L\_SAMPLE\_RATE$.
8:6	LSAMPLE_CNT_DIV	Used for scl low LS/FS only. This adjusts the width of each sample. $SCL\_L\_SAMPLE\_RATE = SAMPLE\_CLK / (LSAMPLE\_CNT\_DIV + 1)$.
5:0	LSTEP_CNT_DIV	This specifies the number of samples for scl low width $SCL\_L\_TIME = (LSTEP\_CNT\_DIV + 1) / SCL\_L\_SAMPLE\_RATE$.

11005030 I2C2_CHN_HS High speed mode register 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HS_HOLD_EN	HHS_SAMPLE_CNT_DIV			HS_NO_HOLD	HHS_STEP_CNT_DIV			HS_SPEED	HS_FC_STEP			HS_HOLD_TIME		HS_NACKERR_DET_EN	HS_EN
Type	RW	RW			RW	RW			RW	RW			RW		RW	RW
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	HS_HOLD_EN	Used for high speed mode THD;DAT only. Can be off by default. 0: Enable 1: Disable
14:12	HHS_SAMPLE_CNT_DIV	Used for scl low HS only. This adjusts the width of each sample. $SCL\_H\_SAMPLE\_RATE = HS\_SAMPLE\_CLK / (HHS\_SAMPLE\_CNT\_DIV + 1)$.
11	HS_NO_HOLD	High-Speed zero hold at ACK bit.
10:8	HHS_STEP_CNT_DIV	This specifies the number of samples for scl low width and for HS only. $SCL\_H\_TIME = (HHS\_STEP\_CNT\_DIV + 1) / HHS\_SCL\_L\_SAMPLE\_RATE$.
7	HS_SPEED	Uses high speed after common command code. 0: Disable 1: Enable
6:4	HS_FC_STEP	This register is for pad control in high speed mode.
3:2	HS_HOLD_TIME	This register is for when to sample data in high speed mode.
1	HS_NACKERR_DET_EN	This enables NACKERR detection during the master code transmission. When enabled, if NACK is not received after master code has been transmitted, the transaction will be terminated with a STOP condition.
0	HS_EN	This enables the high speed transaction. (note: rs_stop must be set to 1 as well)

11005034 I2C2_CHN_IO_CONFIG IO configuration register 00000093

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													IDLE_OE_EN	IO_SYNC_EN	SDA_IO_CONFIG	SCL_IO_CONFIG
Type													RW	RW	RW	RW
Reset													0	0	1	1

Bit(s)	Name	Description
3	IDLE_OE_EN	0: Do not drive bus in idle state 1: Drive bus in idle state
2	IO_SYNC_EN	DEBUG ONLY: When set to 1, scl and sda inputs will be first dual synced by bclk_ck. This should not be needed. Only reserved for debugging.
1	SDA_IO_CONFIG	0: Normal tristate io mode 1: Open-drain mode 0: Normal tristate io mode 1: Open-drain mode
0	SCL_IO_CONFIG	0: Normal tristate io mode 1: Open-drain mode 0: Normal tristate io mode 1: Open-drain mode

11005038 I2C2_CHN_FIFO_ADDR_CLR FIFO address clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HFIFO_ADDR_CLR	FIFO_ADDR_CLR
Type															WO	WO
Reset															0	0

Bit(s)	Name	Description
1	HFIFO_ADDR_CLR	When written with a 1, a 1 pulse fifo_addr_clr is generated to clear the FIFO address to back to 0.
0	FIFO_ADDR_CLR	When written with a 1, a 1 pulse fifo_addr_clr is generated to clear the FIFO address to back to 0.

1100503C I2C2_CHN_DATA_TIMING Data receive time adjust 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										DATA_READ_ADJ_EN	DATA_READ_ADJ					
Type										RW	RW					
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	DATA_READ_ADJ_EN	Enables data read timing adjust. 0: Disable 1: Enable
5:0	DATA_READ_ADJ	Adjusts data read timing.

11005040 I2C2_CHN_MCU_INTR MCU interrupt 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MCU_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	MCU_EN	0: Disable 1: Enable

11005044 I2C2_CHN_TRANSFER_LEN_AUX Transfer length register (Number of bytes per transfer) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSFER_LEN_AUX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TRANSFER_LEN_AUX	This field is valid only when <code>dir_change</code> or <code>transfer_len_change</code> is set to 1. Indicates the number of data bytes to be transferred in 1 transfer unit (excluding slave address byte) for the transfers following the direction change. That is, if <code>dir_change</code> =1, then the first write transfer length will depend on <code>transfer_len</code>, while the second read transfer length depend on <code>transfer_len_aux</code>. Dir change is always after the first transfer. Note: The value must be set to be bigger than 1; otherwise no transfer will take place.

11005048 I2C2_CHN_CLOCK_DIV Clock divider 0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLOCK_DIV				
Type												RW				
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:0	CLOCK_DIV	Clock divider. It will create SAMPLE_CLK which equals to (I2C module clock/ (CLOCK_DIV+1)). Default: all 1 for low-power.

1100504C I2C2_CHN_TIMEOUT_DIV Hardware timeout target 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_TIMEOUT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HW_TIMEOUT	Timeout target. Hardware will timeout when reach this number. Time unit: SCL_L_TIME

11005050 I2C2_CHN_SOFTRESET Soft reset register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													ERROR_RESET	GRANT_RESET	FSM_RESET	SOFT_RESET
Type													WO	WO	WO	WO
Reset													0	0	0	0

Bit(s)	Name	Description
3	ERROR_RESET	Resets error flag.
2	GRANT_RESET	Resets authority.
1	FSM_RESET	Resets state machine only.
0	SOFT_RESET	When written with 1, 1 pulse soft reset is used as synchronous reset to reset the I2C internal hardware circuits. This reset will cause bus charge.

110050D4 I2C2_CHN_DELAY_STEP For time stamp (I3C_EN==1) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DELAY_STEP															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DELAY_STEP	Total delay time = DELAY_STEP/SCL_H_STEP_RATE + Sample delay time

110050D8 I2C2_CHN_DELAY_SAMPLE For time stamp (I3C_EN==1) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DELAY_SAMPLE					
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	DELAY_SAMPLE	Sample delay time = (DELAY_SAMPLE+1)/SCL_H_SAMPLE_RATE

110050E4 I2C2_CHN_DEBUGSTAT Debug Status Register 00006800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SDA_IN_SYNC	SCL_IN_SYNC	WR_FULL	RD_EMPTY	BUS_BUSY	MASTER_WRITE	MASTER_READ	MASTER_STATE							
Type		RO	RO	RO	RO	RO	RO	RO	RO							
Reset		1	1	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	SDA_IN_SYNC	BUS SDA status.
13	SCL_IN_SYNC	BUS SCL status.
12	WR_FULL	This indicates that the fifo is full.
11	RD_EMPTY	This indicates that the fifo is empty.
10	BUS_BUSY	DEBUG ONLY: valid when bus_detect_en is 1. bus_busy = 1 indicates a start transaction has been detected and no stop condition has been detected yet.
9	MASTER_WRITE	DEBUG ONLY: 1 = current transfer is in the master write dir
8	MASTER_READ	DEBUG ONLY: 1 = current transfer is in the master read dir
7:0	MASTER_STATE	DEBUG ONLY: reads back the current master_state. 0: idle state; 1: I2C master is preparing sending out the start bit, SCL=1, SDA=1; 2: I2C master is sending out the start bit, SCL=1, SDA=0; 3: I2C master/slave is preparing transmitting data bit, SCL=0, SDA=data bit (data bit can be changed when SCL=0); 4: I2C master/slave is transmitting data bit, SCL=1, SDA=data bit (data bit is stable when SCL=1); 5: I2C master/slave is preparing transmitting ack bit, SCL=0, SDA=ack (ack bit can be changed when SCL=0); 6: I2C master/slave is transmitting ack bit, SCL=1, SDA=0 (ack bit is stable when SCL=1); 7: I2C master is preparing sending out stop bit or repeated-start bit, SCL=0, SDA=0/1 (0: means stop bit; 1: means repeated-start bit); 8: I2C master is sending out stop bit or repeated-start bit, SCL=1, SDA=1/0 (1: means stop bit; 0: means repeated-start bit); 9: I2C master is in delay start between two transfers, SCL=1, SDA=1; 10: I2C master is in FIFO wait state; For writing transaction, it means FIFO is empty and I2C master is waiting for DMA controller writing data into FIFO; For reading transaction, it means FIFO is full and I2C master is

Bit(s)	Name	Description
		waiting for DMA controller reading data from FIFO, SCL=0, SDA=do not care;
		12: I2C master is preparing sending out data bit of master code. This state is used only in high-speed transaction, SCL=0, SDA=data bit of master code (data bit of master code can be changed when SCL=0);
		13: I2C master is sending out data bit of master code. This state is used only in high-speed transaction, SCL=1, SDA=data bit of master code (data bit of master code is stable when SCL=1);
		14: I2C master/slave is preparing transmitting nack bit, SCL=0, SDA=nack bit (nack bit can be changed when SCL=0); This state is used only in high-speed transaction;
		15: I2C master/slave is transmitting nack bit, SCL=1, SDA=1; This state is used only in high-speed transaction;

110050E8 I2C2_CHN_DEBUGCTRL Debug Control Register 0000001C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RELIABILITY	DMAACK_ENABLE		OLT_MODE	FIFO_APB_DEBUG
Type												RW	RW		RW	RW
Reset												1	1		0	0

Bit(s)	Name	Description
4	RELIABILITY	0: Disable 1: Enable
3	DMAACK_ENABLE	Snoop DMA ack for early terminate DMA request. 0: Disable 1: Enable
1	OLT_MODE	Use for olt only. 0: Disable 1: Enable
0	FIFO_APB_DEBUG	This is used for trace32 debug purposes. When using trace32, and the memory map is shown, turning this bit on will block the normal APB read access. APB read access to the fifo is then enabled by writing to APB_debug_rd. 0: Disable 1: Enable

110050EC I2C2_CHN_DMA_FSM_DEBU Multi-DMA channel debug.

00000000

G

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I3C_EN	APB_ID											FSM_STAT			
Type	RO	RO											RO			
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	I3C_EN	I3C enable 0: I2C 1: I3C
14:8	APB_ID	If (APB_ID < 32), this design is in perisys. Else, this design is in other HW domain.
3:0	FSM_STAT	FSM status. 0x7: Wait for IRQ clean 0xc: Wait for kick-off

110050F0 I2C2_CHN_MULTIMAS Multi-master control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														BUS_DETECT_EN	CLK_SYNC_EN	ARB_EN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	BUS_DETECT_EN	When enabled, the bus status is monitored. If bus is currently busy, no new transaction can proceed. 0: Disable 1: Enable
1	CLK_SYNC_EN	When enabled, clk sync will be performed. 0: Disable 1: Enable
0	ARB_EN	When enabled, multi-master arbitration will be performed. 0: Disable 1: Enable

110050F4 I2C2_CHN_FIFO_STAT FIFO Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RD_ADDR					WR_ADDR					FIFO_OFFSET				
Type		RO					RO					RO				
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:10	RD_ADDR	The current rd address pointer. (only bit [2:0] has physical meaning)
9:5	WR_ADDR	The current wr address pointer. (only bit [2:0] has physical meaning)
4:0	FIFO_OFFSET	wr_addr[3:0] - rd_addr[3:0]

110050F8 I2C2_CHN_FIFO_THRESH FIFO Thresh Register 00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_TRIG_THRESH								RX_TRIG_THRESH			
Type					RW								RW			
Reset					1	1	1	1					0	0	0	0

Bit(s)	Name	Description
11:8	TX_TRIG_THRESH	When TX fifo level is below this value, TX DMA request is asserted.
3:0	RX_TRIG_THRESH	When RX fifo level is above this value, RX DMA request is asserted.

11007F001 I2C2_CHN_SEC_CONTROL Security Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SKIP_S LAVE_ ADDR_ OFF	DAA_E N_OFF
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	SKIP_SLAVE_ADDR_OFF	Forces skip slave address off.
0	DAA_EN_OFF	Forces daa enable off.

11007F801 I2C2_CHN_CHANNEL_LOCK Channel lock. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CHANNEL_LOCK				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	CHANNEL_LOCK	Channel has been locked since security issue. 0: Disable 1: Enable

11007F841 I2C2_CHN_CHANNEL_SEC Channel security enable. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CHANNEL_SEC				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	CHANNEL_SEC	Channel which should be protected. 0: Disable 1: Enable

11007F881 I2C2_CHN_HW.CG_EN HW DCM Enable 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DCM_ULPOWER	DCM_13M_EN	DCM_INTF_EN	DCM_EN
Type													RW	RW	RW	RW
Reset													1	1	1	1

Bit(s)	Name	Description
3	DCM_ULPOWER	When enabled, most register clock will be set to 4 * scl. 0: Disable 1: Enable
2	DCM_13M_EN	When enable, it's aligned to DCM_EN. 0: Disable 1: Enable
1	DCM_INTF_EN	DCM for DMA interface. 0: Disable 1: Enable
0	DCM_EN	Enables HW DCM function. Default is disable. 0: Disable 1: Enable

11007F8C1 I2C2_CHN_MULTI_DMA Multi-DMA channel mode. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	APB_SET				SIDE_SET				IRQ_SET_EN					DMA_CONFIG_MODE	SHADOW_REG_MODE	TRIGGER_ENABLE
Type	RO				RO				RO					RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0					0	0	0

Bit(s)	Name	Description
15:12	APB_SET	APB setting register
11:8	SIDE_SET	SIDE setting register
7	IRQ_SET_EN	Interrupt setting enable register
2	DMA_CONFIG_MODE	Enables multi-DMA channel mode. 0: Disable 1: Enable
1	SHADOW_REG_MODE	Enables shadow register configuration mode. 0: Disable 1: Enable
0	TRIGGER_ENABLE	Enables side-band trigger I2C. 0: Disable 1: Enable

11007F901 I2C2_CHN_DMA_REQ Multi-DMA channel request 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_REQ			
Type													RO			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DMA_REQ	Request for relative DMA channel.

11007F941 I2C2_CHN_DMA_NREQ Multi-DMA channel request canceled. 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_NREQ			
Type													RO			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DMA_NREQ	Cancel request for relative DMA channel.

11006000	I2C_INTB				I2C interrupt										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														IIC_INTB		
Type														RO		
Reset														0	0	0

Bit(s)	Name	Description
2:0	IIC_INTB	I2C interrupt. 0: Interrupt 1: Normal

11006004	LATCH_ADDR				Latch address										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LATCH_ADDR											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	LATCH_ADDR	Aborts APB offset address.

11006008	<u>RST_EN</u>		Reset enable											00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RST_EN		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	RST_EN	SW resets I2C. Need toggle by SW. 0: Normal 1: Reset

1100600C **ABORT_STATUS** **Abort status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ABORT_STATUS								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	ABORT_STATUS	Abort status. 0: Normal 1: Abort

11006010 **SEC_EN** **Secure enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SEC_EN		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	SEC_EN	Secures the whole 4KB address. 0: Normal 1: Secured

11006014 **GLOBAL SEC_EN** Global secure enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GLOCK	LOCK	DLOCK									SEC_CCC_EN				GSEC_EN
Type	RW	RW	RW									RW				RW
Reset	0	0	0									0	0	0	0	0

Bit(s)	Name	Description
15	GLOCK	0: Unlock 1: Lock
14	LOCK	Locks the secure bit 0: Unlock channel secure bit write 1: Lock channel secure bit
13	DLOCK	Locks the domain registers 0: Unlock channel domain register write 1: Lock channel domain register write
4:1	SEC_CCC_EN	0: Disable 1: Smaller than 2: Larger than 3: Between
0	GSEC_EN	Controls global security enabling When this bit is set to 0, the overall channel will be treated as non-security channel. When this bit is set to 1, the security property will depend on each channel's sec_en. 0: Disable 1: Enable

11006018 ASYNC_CTRL ASYNC control 00000029

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ASYNC_CTRL					
Type											RW					
Reset											1	0	1	0	0	1

Bit(s)	Name	Description
5:0	ASYNC_CTRL	ASYNC control

11006E00 AP_CLOCK.CG_EST AP CLOCK CG register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														AP_CLOCK_I2C2_CG	AP_CLOCK_I2C1_CG	AP_CLOCK_I2C0_CG
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	AP_CLOCK_I2C2_CG	0: Normal 1: No clock
1	AP_CLOCK_I2C1_CG	0: Normal 1: No clock
0	AP_CLOCK_I2C0_CG	0: Normal 1: No clock

11006E04 AP_CLOCK.CG_CLEAR_EST AP CLOCK CG clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														AP_CLOCK_I2C2.CG_CLEAR	AP_CLOCK_I2C1.CG_CLEAR	AP_CLOCK_I2C0.CG_CLEAR
Type														WO	WO	WO
Reset														0	0	0

Bit(s)	Name	Description
2	AP_CLOCK_I2C2.CG_CLEAR	0: No effect 1: Clear clock gating
1	AP_CLOCK_I2C1.CG_CLEAR	0: No effect 1: Clear clock gating
0	AP_CLOCK_I2C0.CG_CLEAR	0: No effect 1: Clear clock gating

11006E08 AP_CLOCK.CG.SET.EST AP CLOCK CG set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														AP_CLOCK_I2C2.CG.SET	AP_CLOCK_I2C1.CG.SET	AP_CLOCK_I2C0.CG.SET
Type														WO	WO	WO
Reset														0	0	0

Bit(s)	Name	Description
2	AP_CLOCK_I2C2.CG.SET	0: No effect 1: Set clock gating
1	AP_CLOCK_I2C1.CG.SET	0: No effect 1: Set clock gating
0	AP_CLOCK_I2C0.CG.SET	0: No effect 1: Set clock gating

11006E10 CCU_CLOCK.CG.RO CCU CLOCK CG read-only register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CCU_CLOCK.CG.RO		
Type														RO		
Reset														1	1	1

Bit(s)	Name	Description
2:0	CCU_CLOCK.CG.RO	0: Normal 1: No clock

11006E14 CCU_CLOCK.CG.W1C CCU CLOCK CG write-1-to-clear register 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CCU_CLOCK.CG.W1C		
Type														W1C		
Reset														1	1	1

Bit(s)	Name	Description
2:0	CCU_CLOCK.CG.W1C	0: Normal 1: No clock

11006E18 **CCU_CLOCK.CG.W1S** **CCU CLOCK CG write-1-to-set register** **00000007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CCU_CLOCK.CG.W1S		
Type														W1S		
Reset														1	1	1

Bit(s)	Name	Description
2:0	CCU_CLOCK.CG.W1S	0: Normal 1: No clock

11006E20 **SSPM_CLOCK.CG.RO** **SSPM CLOCK CG read-only register** **00000007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SSPM_CLOCK.CG.RO		
Type														RO		
Reset														1	1	1

Bit(s)	Name	Description
2:0	SSPM_CLOCK.CG.RO	0: Normal 1: No clock

11006E24 **SSPM_CLOCK.CG.W1C** **SSPM CLOCK CG write-1-to-clear register** **00000007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SSPM_CLOCK.CG.W1C		
Type														W1C		
Reset														1	1	1

Bit(s)	Name	Description
2:0	SSPM_CLOCK.CG.W1C	0: Normal 1: No clock

11006E28 **SSPM_CLOCK.CG.W1S** **SSPM CLOCK CG write-1-to-set register** **00000007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SSPM_CLOCK.CG.W1S		
Type														W1S		
Reset														1	1	1

Bit(s)	Name	Description
2:0	SSPM_CLOCK.CG.W1S	0: Normal 1: No clock

11006E30 **CLOCK_SEL RO** **CLOCK Select read-only register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CLOCK_SEL		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	CLOCK_SEL	0: Normal 1: No clock

11006E34 **CLOCK_SEL_W1C** **CLOCK Select write-1-to-clear register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CLOCK_SEL_W1C		
Type														W1C		
Reset														0	0	0

Bit(s)	Name	Description
2:0	CLOCK_SEL_W1C	0: Normal 1: No clock

11006E38 **CLOCK_SEL_W1S** **CLOCK Select write-1-to-set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CLOCK_SEL_W1S		
Type														W1S		
Reset														0	0	0

Bit(s)	Name	Description
2:0	CLOCK_SEL_W1S	0: Normal 1: No clock

11006EF4 **CCU_INT_EN** **CCU Interrupt enable register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CCU_INT_EN		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	CCU_INT_EN	0: Off 1: On

11006EF8 **CCU_INT_INV** **CCU Interrupt Inverter enable register** **00000007**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CCU_INV_EN		
Type														RW		
Reset														1	1	1

Bit(s)	Name	Description
2:0	CCU_INV_EN	0: Off 1: On

11006F10 **SEMAPHORE_0_RO** **SEMAPHORE_0** read-only register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SEMAPHORE_0_RO		
Type														RO		
Reset														0	0	0

Bit(s)	Name	Description
2:0	SEMAPHORE_0_RO	0: Normal 1: No clock

11006F14 SEMAPHORE_0_W1C SEMAPHORE_0 write-1-to-clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SEMAPHORE_0_W1C		
Type														W1C		
Reset														0	0	0

Bit(s)	Name	Description
2:0	SEMAPHORE_0_W1C	0: Normal 1: No clock

11006F18 SEMAPHORE_0_W1S SEMAPHORE_0 write-1-to-set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SEMAPHORE_0_W1S		
Type														W1C		
Reset														0	0	0

Bit(s)	Name	Description
2:0	SEMAPHORE_0_W1S	0: Normal 1: No clock

11006F20 SEMAPHORE_1_RO SEMAPHORE_1 read-only register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SEMAPHORE_1_RO		
Type														RO		
Reset														0	0	0

Bit(s)	Name	Description
2:0	SEMAPHORE_1_RO	0: Normal 1: No clock

11006F24 SEMAPHORE_1_W1C SEMAPHORE_1 write-1-to-clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SEMAPHORE_1_W1C		
Type														W1C		
Reset														0	0	0

Bit(s)	Name	Description
2:0	SEMAPHORE_1_W1C	0: Normal 1: No clock

11006F28 **SEMAPHORE_1_W1S** **SEMAPHORE_1 write-1-to-set register** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SEMAPHORE_1_W1S		
Type														W1C		
Reset														0	0	0

Bit(s)	Name	Description
2:0	SEMAPHORE_1_W1S	0: Normal 1: No clock

11006F30 SEMAPHORE_2_RO SEMAPHORE_2 read-only register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SEMAPHORE_2_RO		
Type														RO		
Reset														0	0	0

Bit(s)	Name	Description
2:0	SEMAPHORE_2_RO	0: Normal 1: No clock

11006F34 SEMAPHORE_2_W1C SEMAPHORE_2 write-1-to-clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SEMAPHORE_2_W1C		
Type														W1C		
Reset														0	0	0

Bit(s)	Name	Description
2:0	SEMAPHORE_2_W1C	0: Normal 1: No clock

11006F38 SEMAPHORE_2_W1S SEMAPHORE_2 write-1-to-set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SEMAPHORE_2_W1S		
Type														W1C		
Reset														0	0	0

Bit(s)	Name	Description
2:0	SEMAPHORE_2_W1S	0: Normal 1: No clock

11006F00 SEC_SLV_0 Secure slave_0 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEC_SLV_ADDR_1							SEC_SLV_ADDR_EN_1	SEC_SLV_ADDR_0							SEC_SLV_ADDR_EN_0
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:9	SEC_SLV_ADDR_1	Secure slave ADDR_1
8	SEC_SLV_ADDR_EN_1	0: Disable 1: Enable
7:1	SEC_SLV_ADDR_0	Secure slave ADDR_0
0	SEC_SLV_ADDR_EN_0	0: Disable 1: Enable

11006F04 SEC_SLV_1 Secure slave_1 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEC_SLV_ADDR_3							SEC_SLV_ADDR_EN_3	SEC_SLV_ADDR_2							SEC_SLV_ADDR_EN_2
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:9	SEC_SLV_ADDR_3	Secure slave ADDR_3
8	SEC_SLV_ADDR_EN_3	0: Disable 1: Enable
7:1	SEC_SLV_ADDR_2	Secure slave ADDR_2
0	SEC_SLV_ADDR_EN_2	0: Disable 1: Enable

11006F08 SEC_CCC_0 Secure CCC_0 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEC_CCC_ADDR_3							SEC_CCC_ADDR_2								
Type	WO							WO								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	SEC_CCC_ADDR_3	Use for range.
7:0	SEC_CCC_ADDR_2	Use for range.

11006F0C SEC_CCC_1 Secure CCC_1 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEC_CCC_ADDR_1								SEC_CCC_ADDR_0							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	SEC_CCC_ADDR_1	Use for exact.
7:0	SEC_CCC_ADDR_0	Use for exact.

11006100 I2C0_SEC_SLV_EN I2C0 secure slave enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BUS_SEC_SLV_EN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	BUS_SEC_SLV_EN	0: Disable 1: Enable

11006104 I2C1_SEC_SLV_EN I2C1 secure slave enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BUS_SEC_SLV_EN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	BUS_SEC_SLV_EN	0: Disable 1: Enable

11006108 I2C2_SEC_SLV_EN I2C2 secure slave enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BUS_SEC_SLV_EN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	BUS_SEC_SLV_EN	0: Disable 1: Enable

3.5 Universal Asynchronous Receiver/Transmitter (UART)

3.5.1 Register Definition

Module name: uart0 Base address: (+0x11000000)

Module name: uart1 Base address: (+0x11000100)

Module name: uart2 Base address: (+0x11000200)

Address	Name	Width	Register Function
11000000	<u>RBR</u>	8	RX buffer register. If FEATURE_SEL=0, LCR[7]=1, this address points to DLL
11000000	<u>THR</u>	8	TX holding register. If FEATURE_SEL=0, LCR[7]=1, this address points to DLL
11000004	<u>IER</u>	8	Interrupt enable register. If FEATURE_SEL=0, LCR[7]=1, this address points to DLM
11000008	<u>IIR</u>	8	Interrupt Identification register. If FEATURE_SEL=0, LCR=8'hbf, this address points to EFR
11000008	<u>FCR</u>	8	FIFO control register. If LCR=8'hbf, this address points to EFR.
1100000C	<u>LCR</u>	8	Line control register
11000010	<u>MCR</u>	8	Modem control register. If FEATURE_SEL=0, LCR=8'hbf, this address points to XON1
11000014	<u>LSR</u>	8	Line status register. If FEATURE_SEL=0, LCR=8'hbf, this address points to XON2
11000018	<u>MSR</u>	8	Modem status register. If FEATURE_SEL=0, LCR=8'hbf, this address points to XOFF1
1100001C	<u>SCR</u>	8	Scratch register. If FEATURE_SEL=0, LCR=8'hbf, this address points to XOFF2
11000020	<u>AUTOBAUD_EN</u>	8	Auto baud detect enable register
11000024	<u>HIGHSPEED</u>	8	High speed Mode register
11000028	<u>SAMPLE_COUNT</u>	8	Sample counter register
1100002C	<u>SAMPLE_POINT</u>	8	Sample point register
11000030	<u>AUTOBAUD_REG</u>	8	Auto baud monitor register
11000034	<u>RATEFIX_AD</u>	8	Clock rate fix register
11000038	<u>AUTOBAUDSAMPLE</u>	8	Auto baud Sample register
1100003C	<u>GUARD</u>	8	Guard time added register
11000040	<u>ESCAPE_DAT</u>	8	Escape character register
11000044	<u>ESCAPE_EN</u>	8	Escape enable register
11000048	<u>SLEEP_EN</u>	8	Sleep enable register
1100004C	<u>DMA_EN</u>	8	DMA enable register
11000050	<u>RXTRI_AD</u>	8	RX Trigger address
11000054	<u>FRACDIV_L</u>	8	Fractional divider LSB address
11000058	<u>FRACDIV_M</u>	8	Fractional divider MSB address
1100005C	<u>FCR_RD</u>	8	FIFO control register
11000088	<u>RTO_CFG</u>	8	RX timeout configuration register
11000090	<u>DLL</u>	8	Divisor Latch (LS); If FEATURE_SEL=1, this address points to DLL
11000094	<u>DLM</u>	8	Divisor Latch (MS); If FEATURE_SEL=1, this address points to DLM
11000098	<u>EFR</u>	8	Enhanced feature register. If FEATURE_SEL=1, this address points to EFR

Address	Name	Width	Register Function
1100009C	<u>FEATURE_SEL</u>	8	UART feature select register
110000A0	<u>XON1</u>	8	XON1 char register. If FEATURE_SEL=1, this address points to XON1
110000A4	<u>XON2</u>	8	XON2 char register. If FEATURE_SEL=1, this address points to XON2
110000A8	<u>XOFF1</u>	8	XOFF1 char register. If FEATURE_SEL=1, this address points to XOFF1
110000AC	<u>XOFF2</u>	8	XOFF2 char register. If FEATURE_SEL=1, this address points to XOFF2
110000B0	<u>USB_RX_SEL</u>	8	UART USB RX pin selection register
110000B4	<u>SLEEP_REQ</u>	8	UART sleep request register
110000B8	<u>SLEEP_ACK</u>	8	UART idle register

11000000

RBRRX buffer register. If FEATURE_SEL=0, LCR[7]=1,
this address points to DLL

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RBR							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RBR	Read-only The received data can be read by accessing this register.

11000000

THRTX holding register. If FEATURE_SEL=0, LCR[7]=1,
this address points to DLL

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									THR							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	THR	TX holding register Write-only. The data to be transmitted are written to this register and then sent to PC via serial communication.

11000004

IERInterrupt enable register. If FEATURE_SEL=0,
LCR[7]=1, this address points to DLM

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CTSI	RTSI	XOFFI		EDSSI	ELSI	ETBEI	ERBFI
Type									RW	RW	RW		RW	RW	RW	RW
Reset									0	0	0		0	0	0	0

Bit(s)	Name	Description
7	CTSI	Masks an interrupt that is generated when a rising edge is detected on the CTS modem control line. Note: This interrupt is only enabled when hardware flow control is enabled. 0: Mask an interrupt generated when a rising edge is detected on the CTS modem control line. 1: Unmask an interrupt generated when a rising edge is detected on the CTS modem control line.
6	RTSI	Masks an interrupt that is generated when a rising edge is detected on the RTS modem control line. Note: This interrupt is only enabled when hardware flow control is enabled. 0: Mask an interrupt generated when a rising edge is detected on the RTS modem control line. 1: Unmask an interrupt generated when a rising edge is detected on the RTS modem control line.
5	XOFFI	Masks an interrupt that is generated when an XOFF character is received. Note: This interrupt is only enabled when software flow control is enabled. 0: Mask an interrupt generated when an XOFF character is received. 1: Unmask an interrupt generated when an XOFF character is received.
3	EDSSI	When this bit is set to 1, an interrupt will be generated if DCTS (MSR[0]) becomes set. 0: No interrupt is generated if DCTS (MSR[0]) becomes set. 1: An interrupt is generated if DCTS (MSR[0]) becomes set.
2	ELSI	When this bit is set to 1, an interrupt will be generated if BI, FE, PE or OE (LSR[4:1]) becomes set. 0: No interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set. 1: An interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.

Bit(s)	Name	Description
1	ETBEI	When this bit is set to 1, an interrupt will be generated if the TX holding register is empty or the contents of TX FIFO are reduced to their trigger level. 0: No interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level. 1: An interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level
0	ERBFI	When this bit is set to 1, an interrupt will be generated if RX data are placed in the RX buffer register or the RX trigger level is reached. 0: No interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached. 1: An interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached.

11000008

IIR

Interrupt Identification register. If
FEATURE_SEL=0, LCR=8'hbf, this address points
to EFR

00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOE		ID					
Type									RO		RU					
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:6	FIFOE	FIFO enable status 00: FIFO is enabled 11: FIFO is disabled
5:0	ID	IIR[5:0] Priority Level Interrupt Source 000001 - No interrupt pending 000110 1 Line Status Interrupt: BI, FE, PE or OE set in LSR. (Under IER[2]=1) 001100 2 RX Data Timeout: Timeout on character in RX FIFO. (Under IER[0]=1) 000100 3 RX Data Received: RX Data received or RX Trigger Level reached. (Under IER[0]=1) 000010 4 TX Holding Register Empty: TX Holding Register empty or TX FIFO Trigger Level reached. (Under IER[1]=1) 000000 5 Modem Status change: DDCD, TERI, DDSR or DCTS set in MSR. (Under IER[3]=1) 010000 6 Software Flow Control: XOFF Character received. (Under IER[5]=1) 100000 7 Hardware Flow Control: CTS or RTS Rising Edge. (Under IER[7]=1 or IER[6]=1)
Line Status Interrupt: A RX Line Status Interrupt (IIR[5:0] == 000110b) is generated if ELSI (IER[2]) is set and any of BI, FE, PE or OE (LSR[4:1]) becomes set. The interrupt is cleared by reading the Line Status Register.		

Bit(s)	Name	Description
		RX Data Timeout Interrupt: When virtual FIFO mode is disabled, RX Data Timeout Interrupt is generated if all of the following apply: 1. FIFO contains at least one character; 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits); 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted on receipt of a new byte from the RX Shift Register, or on a CPU read from the RX FIFO. The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading RX FIFO. When virtual FIFO mode is enabled, RX Data Timeout Interrupt is generated if all of the following apply: 1. FIFO is empty; 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits); 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted on receipt of a new byte from the RX Shift Register or reading DMA_EN register. The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading DMA_EN register.
		RX Data Received Interrupt: A RX Received interrupt (IER[5:0] == 000100b) is generated if EFRBI (IER[0]) is set and either RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached. The interrupt is cleared by reading the RX Buffer Register or the RX FIFO (if enabled).
		TX Holding Register Empty Interrupt: A TX Holding Register Empty Interrupt (IIR[5:0] = 000010b) is generated if ETRBI (IER[1]) is set and either the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level. The interrupt is cleared by writing data to the TX Holding Register or TX FIFO if FIFO is enabled.
		Modem Status Change Interrupt: A Modem Status Change Interrupt (IIR[5:0] = 000000b) is generated if EDSSI (IER[3]) is set and either DDCD, TERI, DDSR or DCTS (MSR[3:0]) becomes set. The interrupt is cleared by reading the Modem Status Register.
		Software Flow Control Interrupt: A Software Flow Control Interrupt (IIR[5:0] = 010000b) is generated if Software Flow Control is enabled and XOFFI (IER[5]) becomes set, indicating that an XOFF character has been

Bit(s)	Name	Description
		received. The interrupt is cleared by reading the Interrupt Identification Register.
		Hardware Flow Control Interrupt: A Hardware Flow Control Interrupt (IER[5:0] = 100000b) is generated if Hardware Flow Control is enabled and either RTSI (IER[6]) or CTSI (IER[7]) becomes set, indicating that a rising edge has been detected on either the RTS/CTS Modem Control line. The interrupt is cleared by reading the Interrupt Identification Register.

11000008

FCR

FIFO control register. If LCR=8'hbf, this address points to EFR.

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RFTL1_RFTLO		TFTL1_TFTLO			CLRT	CLRR	FIFOE
Type									WO		WO			WO	WO	WO
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:6	RFTL1_RFTLO	RX FIFO trigger threshold RX FIFO contains total 32 bytes. 0: 1 1: 6 2: 12 3: RXTRIG
5:4	TFTL1_TFTLO	TX FIFO trigger threshold TX FIFO contains a total 32 bytes. 0: 1 1: 4 2: 8 3: 14
2	CLRT	Control bit to clear TX FIFO 0: No effect 1: Clear TX FIFO
1	CLRR	Control bit to clear RX FIFO 0: No effect 1: Clear RX FIFO
0	FIFOE	Enables FIFO This bit must be set to 1 for any of other bits in the registers to take effect. 0: Disable both RX and TX FIFO 1: Enable both RX and TX FIFO

1100000C		LCR		Line control register												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name									DLAB	SB	SP	EPS	PEN	STB	WLS1_WLS0		
Type									RW	RW	RW	RW	RW	RW	RW		
Reset									0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
7	DLAB	Divisor latch access bit 0: RX and TX registers are read/written at Address 0 and IER register is read/written at Address 4. 1: Divisor Latch LS is read/written at Address 0 and the Divisor Latch MS is read/written at Address 4.
6	SB	Sets up break 0: No effect 1: SOUT signal is forced to "0" state.
5	SP	Stick parity 0: No effect. 1: The Parity bit is forced to a defined state, depending on the states of EPS and PEN: If EPS=1 & PEN=1, the Parity bit will be set and checked=0. If EPS=0 & PEN=1, the Parity bit will be set and checked=1.
4	EPS	Selects even parity 0: When EPS=0, an odd number of ones is sent and checked. 1: When EPS=1, an even number of ones is sent and checked.
3	PEN	Enables parity 0: The Parity is neither transmitted nor checked. 1: The Parity is transmitted and checked.
2	STB	Number of STOP bits 0: One STOP bit is always added. 1: Two STOP bits are added after each character is sent; unless the character length is 5 when 1 STOP bit is added.
1:0	WLS1_WLS0	Selects word length. 0: 5 bits 1: 6 bits 2: 7 bits

Bit(s)	Name	Description
		3: 8 bits

11000010

MCRModem control register. If FEATURE_SEL=0,
LCR=8'hbf, this address points to XON1

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF_S TATUS			Loop			RTS	
Type									RU			RW			RW	
Reset									0			0			0	

Bit(s)	Name	Description
7	XOFF_STATUS	Detect XOFF from RX in soft flow control 0: When an XON character is received. 1: When an XOFF character is received.
4	Loop	Loopback control bit 0: No loopback is enabled. 1: Loopback mode is enabled.
1	RTS	Controls the state of the output NRTS, even in loop mode. 0: RTS always outputs 1. 1: RTSs output is controlled by flow control condition.

11000014

LSR

Line status register. If FEATURE_SEL=0,
LCR=8'hbf, this address points to XON2

00000060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOERR	TEMT	THRE	BI	FE	PE	OE	DR
Type									RU	RU	RU	RU	RU	RU	RU	RU
Reset									0	1	1	0	0	0	0	0

Bit(s)	Name	Description
7	FIFOERR	RX FIFO error indicator 0: No PE, FE and BI is in RX FIFO. 1: Set to 1 when there is at least one PE, FE or BI in RX FIFO.
6	TEMT	TX holding register (or TX FIFO) and TX shift register are empty. 0: Empty conditions below are not met. 1: If FIFOs are enabled, the bit will be set whenever TX FIFO and the TX shift register are empty. If FIFOs are disabled, the bit will be set whenever TX holding register and TX shift register are empty.
5	THRE	Indicates if there is room for TX holding register or TX FIFO is reduced to its trigger level. 0: Reset whenever the contents of TX FIFO are more than its trigger level (FIFOs are enabled), or whenever TX holding register is not empty (FIFOs are disabled). 1: Set whenever the contents of TX FIFO are reduced to its trigger level (FIFOs are enabled), or whenever TX holding register is empty and ready to accept new data (FIFOs are disabled).
4	BI	Break interrupt 0: Reset by CPU reading this register 1: If FIFOs are disabled, this bit will be set whenever SIN is held in 0 state for more than one transmission time (START bit + DATA bits + PARITY + STOP bits). If FIFOs are enabled, this error will be associated with a corresponding character in FIFO and is flagged when this byte is at top of FIFO. When a break occurs, only one zero character will be loaded to the FIFO: The next character transfer will be enabled when SIN enters the marking state and receives the next valid start bit.
3	FE	Framing error 0: Reset by CPU reading this register 1: If the FIFOs are disabled, this bit will be set if the received data do not have a valid STOP bit. If FIFOs are enabled, the state of this bit will be revealed when the byte it refers to is the next to be read.
2	PE	Parity error

Bit(s)	Name	Description
		0: Reset by CPU reading this register
		1: If FIFOs are disabled, this bit will be set if the received data do not have a valid parity bit. If FIFOs are enabled, the state of this bit will be revealed when the referred byte is the next to be read.
1	OE	Overrun error 0: Reset by CPU reading this register. 1: If FIFOs are disabled, this bit will be set if RX buffer is not read by CPU before new data from RX shift register overwrites the previous contents. If FIFOs are enabled, an overrun error will occur when RX FIFO is full and RX shift register becomes full. OE is set as soon as this happens. The character in the shift register will then be overwritten but not transferred to the FIFO.
0	DR	Data ready 0: Cleared by CPU reading RX buffer or by reading all FIFO bytes. 1: Set by RX buffer becoming full or by FIFO becoming not empty.

11000018

MSRModem status register. If FEATURE_SEL=0,
LCR=8'hbf, this address points to XOFF1

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CTS				DCTS
Type												RU				RW
Reset												0				0

Bit(s)	Name	Description
4	CTS	Clear to send When Loop = "0", this value is the complement of the NCTS input signal. When Loop = "1", this value is equal to the RTS bit in the modem control register.
0	DCTS	Delta clear to send 0: Cleared if the state of CTS has not changed since this register is last read. 1: Set if the state of CTS has changed since this register is last read.

1100001C

SCRScratch register. If FEATURE_SEL=0, LCR=8'hbf,
this address points to XOFF2

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SCR							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SCR	General purpose read/write register. After reset, its value will be undefined.

11000020		AUTOBAUD_EN				Auto baud detect enable register										00000000	
Bit		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																	
Type																	
Reset																	
Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																AUTOB AUD_S EL	AUTOB AUD_E N
Type																RW	RW
Reset																0	0

Bit(s)	Name	Description
1	AUTOBAUD_SEL	Selects auto-baud 0: Support standard baud rate detection 1: Support non_standard baud rate detection (only baud from 300 to 115,200; using 52MHZ to auto fix is recommended)
0	AUTOBAUD_EN	Auto-baud enabling signal 0: Disable auto-baud function 1: Enable auto-baud function (UARTn+0024h SPEED should be set 0) Note: When AUTOBAUD_EN is active, there should not be A*/a* char before auto baud char AT/at. If A*/a* is inevitable, autobaud will fail and please disable AUTOBAUD_EN to reset autobaud feature and autobaud_en.

11000024 HIGHSPEED High speed Mode register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SPEED	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	SPEED	UART sample counter base 0: Based on $16 * \text{baud\_pulse}$, $\text{baud\_rate} = \text{System clock frequency} / 16 / \{\text{DLH}, \text{DLL}\}$ 1: Based on $8 * \text{baud\_pulse}$, $\text{baud\_rate} = \text{System clock frequency} / 8 / \{\text{DLH}, \text{DLL}\}$ 2: Based on $4 * \text{baud\_pulse}$, $\text{baud\_rate} = \text{System clock frequency} / 4 / \{\text{DLH}, \text{DLL}\}$ 3: Based on $\text{sample\_count} * \text{baud\_pulse}$, $\text{baud\_rate} = \text{System clock frequency} / (\text{sample\_count} + 1) / \{\text{DLM}, \text{DLL}\}$

11000028 SAMPLE_COUNT Sample counter register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLECOUNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SAMPLECOUNT	Only useful when HIGHSPEED mode=3

1100002C	<u>SAMPLE_POINT</u>				Sample point register								000000FF			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLEPOINT							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	SAMPLEPOINT	SAMPLE_POINT is usually $(\text{SAMPLE\_COUNT}-1)/2$ without decimal. Sample point is effective only when HIGHSPEED=3.

11000030	AUTOBAUD_REG				Auto baud monitor register								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BAUD_STAT				BAUD_RATE			
Type									RU				RU			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:4	BAUD_STAT	Autobaud format 0: Autobaud is detecting. 1: AT_7N1 2: AT_7O1 3: AT_7E1 4: AT_8N1 5: AT_8O1 6: AT_8E1 7: at_7N1 8: at_7E1 9: at_7O1 10: at_8N1 11: at_8E1 12: at_8O1 13: Autobaud detection fails.
3:0	BAUD_RATE	Autobaud baud rate 0: 115,200 1: 57,600 2: 38,400 3: 19,200 4: 9,600 5: 4,800 6: 2,400 7: 1,200

Bit(s)	Name	Description
8: 300		
9: 110		

11000034 **RATEFIX_AD** Clock rate fix register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FREQ_SEL	AUTOBAUD_RATE_FIX	RATE_FIX
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FREQ_SEL	0: System clock = UART_CLK_SRC/2 1: System clock = UART_CLK_SRC/4
1	AUTOBAUD_RATE_FIX	0: System clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz) 1: System clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depending on FREQ_SEL)
0	RATE_FIX	0: System clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz) 1: System clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depending on FREQ_SEL)

11000038 AUTOBAUDSAMPLE Auto baud Sample register 0000000D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											AUTOBAUDSAMPLE					
Type											RW					
Reset											0	0	1	1	0	1

Bit(s)	Name	Description
5:0	AUTOBAUDSAMPLE	CLK division for autobaud rate detection For standard baud rate detection. System clk 52m:'d 27 System clk 26m:'d 13 System clk 13m:'d 6 For non-standard baud rate detection: 15

1100003C GUARD Guard time added register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												GUARD_EN	GUARD_CNT			
Type												RW	RW			
Reset												0	1	1	1	1

Bit(s)	Name	Description
4	GUARD_EN	Guard interval add enabling signal 0: No guard interval added 1: Add guard interval after stop bit
3:0	GUARD_CNT	Guard interval count value Guard interval = $\lceil 1/(\text{system clock}/\text{div\_step}/\text{div}) \rceil * \text{GUARD\_CNT}$

11000040		ESCAPE_DAT								Escape character register								000000FF	
Bit		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																			
Type																			
Reset																			
Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name										ESCAPE_DAT									
Type										RW									
Reset										1	1	1	1	1	1	1	1		

Bit(s)	Name	Description
7:0	ESCAPE_DAT	Escape character added before software flow control data and escape character If TX data are xon (31h) with esc_en =1, UART transmits data as esc + CEh (~xon).

11000044		ESCAPE_EN								Escape enable register								00000000	
Bit		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																			
Type																			
Reset																			
Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name																		ESC_EN	
Type																		RW	
Reset																		0	

Bit(s)	Name	Description
0	ESC_EN	Adds escape character in transmitter and removes escape character in receiver by UART 0: Does not deal with escape character 1: Add escape character in transmitter and remove escape character in receiver

11000048	<u>SLEEP_EN</u>															Sleep enable register															00000000																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	

Bit(s)	Name	Description
0	SLEEP_EN	For sleep mode issue 0: Does not deal with sleep mode indicate signal 1: Activate hardware flow control or software control according to software initial setting when chip enters sleep mode. Release hardware flow when chip wakes up. For software control, UART sends XON when the system is awakened and when FIFO does not reach threshold level.

1100004C DMA_EN DMA enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FIFO_Isr_sel	TO_CNT_AUTORST	TX_DMA_EN	RX_DMA_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	FIFO_Isr_sel	Selects FIFO LSR mode 0: LSR updates automatically with read data from RX FIFO. 1: LSR holds the first line status error state until you read the LSR register.
2	TO_CNT_AUTORST	Timeout counter auto reset register 0: After RX timeout happens, SW shall reset the interrupt by reading UART 0x4C. 1: The timeout counter will be auto reset.
1	TX_DMA_EN	TX_DMA mechanism enabling signal 0: Does not use DMA in TX 1: Use DMA in TX. When this register is enabled, the flow control is based on the DMA threshold and generates a timeout interrupt for DMA.
0	RX_DMA_EN	RX_DMA mechanism enabling signal 0: Does not use DMA in RX 1: Use DMA in RX. When this register is enabled, the flow control is based on the DMA threshold and generates a timeout interrupt.

11000050 **RXTRI_AD** **RX Trigger address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RXTRIG			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RXTRIG	When {rtm,rtl}=2'b11, RX FIFO threshold will be RXtrig. The value is suggested to be less than half of RX FIFO size, which is 32 bytes.

11000054 **FRACDIV_L** **Fractional divider LSB address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FRACDIV_L							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FRACDIV_L	Adds sampling count (+1) from state data7 to data0 in order to contribute fractional divisor. Only when high_speed==3.

11000058	FRACDIV_M														Fractional divider MSB address		00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name															FRACDIV_M		
Type															RW		
Reset															0	0	

Bit(s)	Name	Description
1:0	FRACDIV_M	Adds sampling count from the state of stop to parity in order to contribute fractional divisor. Only valid in high_speed==3 mode.

1100005C	FCR_RD		FIFO control register												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RFTL1_RFTL0		TFTL1_TFTL0			CLRT	CLRR	FIFOE
Type									RO		RO			RO	RO	RO
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:6	RFTL1_RFTL0	RX FIFO trigger threshold RX FIFO contains a total of 32 bytes. 0: 1 1: 6 2: 12 3: RXTRIG
5:4	TFTL1_TFTL0	TX FIFO trigger threshold TX FIFO contains a total of 32 bytes. 0: 1 1: 4 2: 8 3: 14
2	CLRT	Clears UART TX FIFO 0: TX FIFO is not cleared. 1: TX FIFO is cleared.
1	CLRR	Clears UART RX FIFO 0: RX FIFO is not cleared. 1: RX FIFO is cleared.
0	FIFOE	Enables FIFO This bit must be set to 1 for any other bits in the registers to take effect. 0: RX and TX FIFOs are not enabled. 1: RX and TX FIFOs are enabled.

11000088 **RTO_CFG** **RX timeout configuration register** **00000024**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RTO_SEL	RTO_LENGTH					
Type										RW	RW					
Reset										0	1	0	0	1	0	0

Bit(s)	Name	Description
6	RTO_SEL	Selects the trigger method of RX timeout 0: Timeout value selected by old method 1: Timeout value selected by FW program value
5:0	RTO_LENGTH	Timeout value programmed by FW Unit: Bit numbers based on current UART baud rate

11000090 **DLL** **Divisor Latch (LS); If FEATURE_SEL=1, this address points to DLL** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLL							
Type									RW							
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:0	DLL	Divisor latch low 8-bit data

11000094

DLMDivisor Latch (MS); If FEATURE_SEL=1, this
address points to DLM

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLM							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DLM	Divisor latch high 8-bit data Note: Division by 1 generates a BAUD signal that is constantly high. DLL & DLM setting formula is {DLH, DLL}=(system clock frequency/ baud_pulse/ baud_rate). When RATE_FIX(RATEFIX_AD[0])=0, system clock frequency = 52MHz. When RATE_FIX(RATEFIX_AD[0])=1 and RATE_FIX(RATEFIX_AD[2])=0, system clock frequency = 26MHz. When RATE_FIX(RATEFIX_AD[0])=1 and RATE_FIX(RATEFIX_AD[2])=1, system clock frequency = 13MHz. For baud_pulse value refer to HIGH_SPEED(offset=24H) register, e.g. when the source clock is 52MHz, default speed mode is used and 115200 baud rate need to be configured, {DLH, DLL}=52MHz/16/115200=28.

11000098

EFREnhanced feature register. If FEATURE_SEL=1,
this address points to EFR

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AUTO_CTS	AUTO_RTS		ENABL E_E	SW_FLOW_CONT			
Type									RW	RW		RW	RW			
Reset									0	0		0	0	0	0	0

Bit(s)	Name	Description
7	AUTO_CTS	Enables hardware transmission flow control 0: Disable 1: Enable
6	AUTO_RTS	Enables hardware reception flow control 0: Disable 1: Enable
4	ENABLE_E	Enables enhancement feature 0: Disable 1: Enable
3:0	SW_FLOW_CONT	Software flow control bits 00xx: No TX flow control 10xx: Transmit XON1/XOFF1 as flow control bytes 01xx: Transmit XON2/XOFF2 as flow control bytes xx00: No RX flow control xx10: Receive XON1/XOFF1 as flow control bytes xx01: Receive XON2/XOFF2 as flow control bytes

1100009C	FEATURE_SEL															UART feature select register															00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16															
Name																															
Type																															
Reset																															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
Name																FEATURERE_SEL															
Type																RW															
Reset																0															

Bit(s)	Name	Description
0	FEATURE_SEL	For AP MCU side UART, if new UART register map is used, feature_sel should be kept at 1. 0: Disable new register map 1: Enable new register map

110000A0

XON1XON1 char register. If FEATURE_SEL=1, this
address points to XON1

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON1	XON1 character for software flow control

110000A4

XON2XON2 char register. If FEATURE_SEL=1, this
address points to XON2

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON2	XON2 character for software flow control

110000A8

XOFF1

XOFF1 char register. If FEATURE_SEL=1, this address points to XOFF1

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF1	XOFF1 character for software flow control

110000AC

XOFF2

XOFF2 char register. If FEATURE_SEL=1, this address points to XOFF2

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF2	XOFF2 character for software flow control

110000B0 USB_RX_SEL UART USB RX pin selection register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																USB_RX_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	USB_RX_SEL	Enables UART RX from USB 0: Select UART RX pin 1: Select USB RX pin

110000B4 **SLEEP_REQ** **UART sleep request register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_REQ
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_REQ	System can set UART sleep request to check UART active status 0: Cancel sleep request to UART (after wake-up sent by CPU) 1: Send sleep request to UART (before sleep sent by CPU)

110000B8 **SLEEP_ACK** **UART idle register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_ACK
Type																RU
Reset																1

Bit(s)	Name	Description
0	SLEEP_ACK	System can check UART sleep ACK to check UART active status 0: UART is not in idle state. (CPU can poll this register to get the UART state.) 1: UART is in idle state. (CPU can poll this register to get the UART state.)

3.6 Pulse Width Modulators (PWMs)

3.6.1 Register Definition

Module name: PWM Base address: (+0x10048000)

Address	Name	Width	Register Function
10048080	<u>PWM0_CON</u>	32	PWM control register
10048084	<u>PWM0_HIGH_DURATION</u>	32	PWM high duration register
10048088	<u>PWM0_LOW_DURATION</u>	32	PWM low duration register
1004808C	<u>PWM0_DG_DURATION</u>	32	PWM delay/guard duration register
10048090	<u>PWM0_BUF0_BASE_ADDR</u>	32	PWM buffer 0 base address register
10048094	<u>PWM0_BUF0_SIZE</u>	32	PWM buffer size register
10048098	<u>PWM0_BUF1_BASE_ADDR</u>	32	PWM buffer 1 base address register
1004809C	<u>PWM0_BUF1_SIZE</u>	32	PWM buffer size register
100480A0	<u>PWM0_SEND_DATA0</u>	32	PWM send data 0 register
100480A4	<u>PWM0_SEND_DATA1</u>	32	PWM send data 1 register
100480A8	<u>PWM0_WAVE_NUM</u>	32	PWM wave number register
100480AC	<u>PWM0_DATA_WIDTH</u>	32	PWM data width register
100480B0	<u>PWM0_THRESH</u>	32	PWM threshold width register
100480B4	<u>PWM0_SEND_WAVENUM</u>	32	PWM wave number register
100480B8	<u>PWM0_VALID</u>	32	PWM wave number register
100480BC	<u>PWM0_BUF_BASE_ADDR2</u>	32	PWM buffer base address 2 register
100480C0	<u>PWM1_CON</u>	32	PWM control register
100480C4	<u>PWM1_HIGH_DURATION</u>	32	PWM high duration register
100480C8	<u>PWM1_LOW_DURATION</u>	32	PWM low duration register
100480CC	<u>PWM1_DG_DURATION</u>	32	PWM delay/guard duration register
100480D0	<u>PWM1_BUF0_BASE_ADDR</u>	32	PWM buffer 0 base address register
100480D4	<u>PWM1_BUF0_SIZE</u>	32	PWM buffer size register
100480D8	<u>PWM1_BUF1_BASE_ADDR</u>	32	PWM buffer 1 base address register
100480DC	<u>PWM1_BUF1_SIZE</u>	32	PWM buffer size register
100480E0	<u>PWM1_SEND_DATA0</u>	32	PWM send data 0 register
100480E4	<u>PWM1_SEND_DATA1</u>	32	PWM send data 1 register
100480E8	<u>PWM1_WAVE_NUM</u>	32	PWM wave number register
100480EC	<u>PWM1_DATA_WIDTH</u>	32	PWM data width register
100480F0	<u>PWM1_THRESH</u>	32	PWM threshold width register
100480F4	<u>PWM1_SEND_WAVENUM</u>	32	PWM wave number register
100480F8	<u>PWM1_VALID</u>	32	PWM wave number register
100480FC	<u>PWM1_BUF_BASE_ADDR2</u>	32	PWM buffer base address 2 register
10048100	<u>PWM2_CON</u>	32	PWM control register
10048104	<u>PWM2_HIGH_DURATION</u>	32	PWM high duration register
10048108	<u>PWM2_LOW_DURATION</u>	32	PWM low duration register
1004810C	<u>PWM2_DG_DURATION</u>	32	PWM delay/guard duration register
10048110	<u>PWM2_BUF0_BASE_ADDR</u>	32	PWM buffer 0 base address register
10048114	<u>PWM2_BUF0_SIZE</u>	32	PWM buffer size register
10048118	<u>PWM2_BUF1_BASE_ADDR</u>	32	PWM buffer 1 base address register
1004811C	<u>PWM2_BUF1_SIZE</u>	32	PWM buffer size register
10048120	<u>PWM2_SEND_DATA0</u>	32	PWM send data 0 register
10048124	<u>PWM2_SEND_DATA1</u>	32	PWM send data 1 register
10048128	<u>PWM2_WAVE_NUM</u>	32	PWM wave number register

Address	Name	Width	Register Function
1004812C	<u>PWM2_DATA_WIDTH</u>	32	PWM data width register
10048130	<u>PWM2_THRESH</u>	32	PWM threshold width register
10048134	<u>PWM2_SEND_WAVENUM</u>	32	PWM wave number register
10048138	<u>PWM2_VALID</u>	32	PWM wave number register
1004813C	<u>PWM2_BUF_BASE_ADDR2</u>	32	PWM buffer base address 2 register
10048140	<u>PWM3_CON</u>	32	PWM control register
10048144	<u>PWM3_HIGH_DURATION</u>	32	PWM high duration register
10048148	<u>PWM3_LOW_DURATION</u>	32	PWM low duration register
1004814C	<u>PWM3_DG_DURATION</u>	32	PWM delay/guard duration register
10048150	<u>PWM3_BUF0_BASE_ADDR</u>	32	PWM buffer 0 base address register
10048154	<u>PWM3_BUF0_SIZE</u>	32	PWM buffer size register
10048158	<u>PWM3_BUF1_BASE_ADDR</u>	32	PWM buffer 1 base address register
1004815C	<u>PWM3_BUF1_SIZE</u>	32	PWM buffer size register
10048160	<u>PWM3_SEND_DATA0</u>	32	PWM send data 0 register
10048164	<u>PWM3_SEND_DATA1</u>	32	PWM send data 1 register
10048168	<u>PWM3_WAVE_NUM</u>	32	PWM wave number register
1004816C	<u>PWM3_DATA_WIDTH</u>	32	PWM data width register
10048170	<u>PWM3_THRESH</u>	32	PWM threshold width register
10048174	<u>PWM3_SEND_WAVENUM</u>	32	PWM wave number register
10048178	<u>PWM3_VALID</u>	32	PWM wave number register
1004817C	<u>PWM3_BUF_BASE_ADDR2</u>	32	PWM buffer base address 2 register
10048180	<u>PWM4_CON</u>	32	PWM control register
10048184	<u>PWM4_HIGH_DURATION</u>	32	PWM high duration register
10048188	<u>PWM4_LOW_DURATION</u>	32	PWM low duration register
1004818C	<u>PWM4_DG_DURATION</u>	32	PWM delay/guard duration register
10048190	<u>PWM4_BUF0_BASE_ADDR</u>	32	PWM buffer 0 base address register
10048194	<u>PWM4_BUF0_SIZE</u>	32	PWM buffer size register
10048198	<u>PWM4_BUF1_BASE_ADDR</u>	32	PWM buffer 1 base address register
1004819C	<u>PWM4_BUF1_SIZE</u>	32	PWM buffer size register
100481A0	<u>PWM4_SEND_DATA0</u>	32	PWM send data 0 register
100481A4	<u>PWM4_SEND_DATA1</u>	32	PWM send data 1 register
100481A8	<u>PWM4_WAVE_NUM</u>	32	PWM wave number register
100481AC	<u>PWM4_DATA_WIDTH</u>	32	PWM data width register
100481B0	<u>PWM4_THRESH</u>	32	PWM threshold width register
100481B4	<u>PWM4_SEND_WAVENUM</u>	32	PWM wave number register
100481B8	<u>PWM4_VALID</u>	32	PWM wave number register
100481BC	<u>PWM4_BUF_BASE_ADDR2</u>	32	PWM buffer base address 2 register
100481C0	<u>PWM5_CON</u>	32	PWM control register
100481C4	<u>PWM5_HIGH_DURATION</u>	32	PWM high duration register
100481C8	<u>PWM5_LOW_DURATION</u>	32	PWM low duration register
100481CC	<u>PWM5_DG_DURATION</u>	32	PWM delay/guard duration register
100481D0	<u>PWM5_BUF0_BASE_ADDR</u>	32	PWM buffer 0 base address register
100481D4	<u>PWM5_BUF0_SIZE</u>	32	PWM buffer size register
100481D8	<u>PWM5_BUF1_BASE_ADDR</u>	32	PWM buffer 1 base address register
100481DC	<u>PWM5_BUF1_SIZE</u>	32	PWM buffer size register
100481E0	<u>PWM5_SEND_DATA0</u>	32	PWM send data 0 register
100481E4	<u>PWM5_SEND_DATA1</u>	32	PWM send data 1 register
100481E8	<u>PWM5_WAVE_NUM</u>	32	PWM wave number register
100481EC	<u>PWM5_DATA_WIDTH</u>	32	PWM data width register

Address	Name	Width	Register Function
100481F0	<u>PWM5_THRESH</u>	32	PWM threshold width register
100481F4	<u>PWM5_SEND_WAVENUM</u>	32	PWM wave number register
100481F8	<u>PWM5_VALID</u>	32	PWM wave number register
100481FC	<u>PWM5_BUF_BASE_ADDR2</u>	32	PWM buffer base address 2 register
10048200	<u>PWM6_CON</u>	32	PWM control register
10048204	<u>PWM6_HIGH_DURATION</u>	32	PWM high duration register
10048208	<u>PWM6_LOW_DURATION</u>	32	PWM low duration register
1004820C	<u>PWM6_DG_DURATION</u>	32	PWM delay/guard duration register
10048210	<u>PWM6_BUF0_BASE_ADDR</u>	32	PWM buffer 0 base address register
10048214	<u>PWM6_BUF0_SIZE</u>	32	PWM buffer size register
10048218	<u>PWM6_BUF1_BASE_ADDR</u>	32	PWM buffer 1 base address register
1004821C	<u>PWM6_BUF1_SIZE</u>	32	PWM buffer size register
10048220	<u>PWM6_SEND_DATA0</u>	32	PWM send data 0 register
10048224	<u>PWM6_SEND_DATA1</u>	32	PWM send data 1 register
10048228	<u>PWM6_WAVE_NUM</u>	32	PWM wave number register
1004822C	<u>PWM6_DATA_WIDTH</u>	32	PWM data width register
10048230	<u>PWM6_THRESH</u>	32	PWM threshold width register
10048234	<u>PWM6_SEND_WAVENUM</u>	32	PWM wave number register
10048238	<u>PWM6_VALID</u>	32	PWM wave number register
1004823C	<u>PWM6_BUF_BASE_ADDR2</u>	32	PWM buffer base address 2 register
10048240	<u>PWM7_CON</u>	32	PWM control register
10048244	<u>PWM7_HIGH_DURATION</u>	32	PWM high duration register
10048248	<u>PWM7_LOW_DURATION</u>	32	PWM low duration register
1004824C	<u>PWM7_DG_DURATION</u>	32	PWM delay/guard duration register
10048250	<u>PWM7_BUF0_BASE_ADDR</u>	32	PWM buffer 0 base address register
10048254	<u>PWM7_BUF0_SIZE</u>	32	PWM buffer size register
10048258	<u>PWM7_BUF1_BASE_ADDR</u>	32	PWM buffer 1 base address register
1004825C	<u>PWM7_BUF1_SIZE</u>	32	PWM buffer size register
10048260	<u>PWM7_SEND_DATA0</u>	32	PWM send data 0 register
10048264	<u>PWM7_SEND_DATA1</u>	32	PWM send data 1 register
10048268	<u>PWM7_WAVE_NUM</u>	32	PWM wave number register
1004826C	<u>PWM7_DATA_WIDTH</u>	32	PWM data width register
10048270	<u>PWM7_THRESH</u>	32	PWM threshold width register
10048274	<u>PWM7_SEND_WAVENUM</u>	32	PWM wave number register
10048278	<u>PWM7_VALID</u>	32	PWM wave number register
1004827C	<u>PWM7_BUF_BASE_ADDR2</u>	32	PWM buffer base address 2 register
10048000	<u>PWM_ENABLE</u>	32	PWM enable register
10048004	<u>PWM_INT_ENABLE_FIN</u>	32	PWM finish interrupt enable register
10048008	<u>PWM_INT_ENABLE_UDF</u>	32	PWM underflow interrupt enable register
1004800C	<u>PWM_INT_STATUS_FIN</u>	32	PWM finish interrupt status register
10048010	<u>PWM_INT_STATUS_UDF</u>	32	PWM underflow interrupt status register
10048014	<u>PWM_INT_ACK_FIN</u>	32	PWM finish interrupt acknowledge register
10048018	<u>PWM_INT_ACK_UDF</u>	32	PWM underflow interrupt acknowledge register
1004801C	<u>PWM_EN_STATUS_UDF</u>	32	PWM enable status register
10048020	<u>PWM_LOOP_BACK_TEST</u>	32	PWM loopback test

10048080 PWM0_CON PWM control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PWM_INT_STA_UDF	PWM_INT_STA_FIN	PWM_INT_EN_UDF	PWM_INT_EN_FIN							DELAY_EN	DELAY_CKSRC	PWM0_3DLCM	PWM0_3DLCM_BASE	PWM0_3DLCM_INV	PWM0_EN_CHN
Type	RO	RO	RW	RW							RW	RW	RW	RW	RW	RW
Reset	0	0	0	0							0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PWM_INT_STA_UDF	PWM interrupt for underflow. Write 1 to clear.
30	PWM_INT_STA_FIN	PWM interrupt for finish. Write 1 to clear.
29	PWM_INT_EN_UDF	PWM interrupt enable presents for underflow. 1: Enable 0: Disable
28	PWM_INT_EN_FIN	PWM interrupt enable presents for finish. 1: Enable 0: Disable
21	DELAY_EN	Sequential mode enable 1: Enable 0: Disable
20	DELAY_CKSRC	Sequential mode clock source divisor: 1625 0: CLK = CLKSRC 1: CLK = CLKSRC/1625
19	PWM0_3DLCM	This channel invert or not in 3dlcm mode
18	PWM0_3DLCM_BASE	This channel is as 3dlcm base channel
17	PWM0_3DLCM_INV	This channel enable 3dlcm mode or not
16	PWM0_EN_CHN	PWM0_EN at channel side. This bit will work if and only if CHANNEL_LOCK of this channel is enabled.
15	OLD_PWM_MODE	Uses Standard PWM mode Note: Using Standard PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. However, only Standard PWM mode with 32-kHz clock cannot work in system sleep mode.

Bit(s)	Name	Description
		(Legacy PWM mode indicates non-old mode; Standard PWM mode indicates old mode)
		0: Legacy PWM mode
		1: Standard PWM mode
14:9	STOP_BITPOS	Stop bit position for source data in periodical mode In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	PWM0 output value during guard time
7	IDLE_VALUE	PWM0 output value in idle state
6	MODE	Selects random generator mode 0: Periodical PWM mode. 1: Random PWM mode
5	SRCSEL	Selects PWM0 data source 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	Old Mode select 32-kHz clock 0: CLK = 32-kHz; CLK is not used. 1: CLK = 32-kHz; CLK can be used.
3	CLKSEL	Clock source divisor: 1625 (old/FIFO/memory/random/kick/SMC mode) 0: CLK = CLKSRC 1: CLK = CLKSRC/1625
2:0	CLKDIV	Selects PWM0 clock scale 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

10048084 PWM0_HIGH_DURATION PWM high duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HDURATION	PWM0 pulse duration based on the current clock when PWM0 output is high If duration =N, program N-1 in this register. Note: The duration of PWM0 must not be 0.

10048088 PWM0_LOW_DURATION PWM low duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	LDURATION	PWM0 pulse duration based on the current clock when PWM0 output is low If duration =N, program N-1 in this register. Note: The duration of PWM0 must not be 0.

1004808C PWM0_DG_DURATION PWM delay/guard duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DELAY_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DELAY_DURATION	Guarding interval between individual waveforms and the output is decided by GUARD_VALUE If it equals N, program N-1 in this register. Note: 1. If this duration is 0, it means there is no guarding interval. 2. The guard duration of standard mode is set by PWM_DATA_WIDTH.
15:0	GUARD_DURATION	Guarding interval between individual waveforms and the output is decided by GUARD_VALUE

10048090 PWM0_BUF0_BASE_ADDR PWM buffer 0 base address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of memory buffer0 for PWM0's waveform data

10048094 **PWM0 BUF0_SIZE** **PWM buffer size register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	Length of waveform data in memory buffer0 PWM0 should generate If it equals N, program N-1 in this register. Note: The size is in unit of 32-bit data.

10048098 **PWM0 BUF1_BASE_ADDR** **PWM buffer 1 base address register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	Base address of memory buffer1 for PWM0's waveform data Note: The memory buffer1 is useless in periodical mode.

1004809C **PWM0 BUF1_SIZE** **PWM buffer size register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	Length of waveform data in memory buffer1 PWM0 should generate If it equals N, program N-1 in this register.

100480A0 **PWM0 SEND_DATA0** **PWM send data 0 register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	PWM0 local buffer0 of pulse sequence data to be generated Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

100480A4 PWM0_SEND_DATA1 PWM send data 1 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	PWM0 local buffer0 of pulse sequence data to be generated Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

100480A8 PWM0_WAVE_NUM PWM wave number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	Number by which PWM0 will generate from pulse data repeatedly Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.

100480AC **PWM0 DATA WIDTH** **PWM data width register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_WIDTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DATA_WIDTH	PWM0 pulse data width in Standard PWM mode

100480B0 **PWM0 THRESH** **PWM threshold width register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	THRESH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	THRESH	PWM0 pulse data high/low switching threshold in Standard PWM mode

100480B4 PWM0_SEND_WAVENUM PWM wave number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HSEC_USAGE															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HSEC_USAGE	Memory mode, random mode security usage
15:0	SEND_WAVENUM	Number by which PWM0 has already generated from specified data source in periodical mode

100480B8 PWM0_VALID PWM wave number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready. 0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready.
0	BUF0_VALID	When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready. 0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready.

100480BC **PWM0 BUF BASE ADDR2** PWM buffer base address 2 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BUF1_BS_ADDR2			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BUF0_BS_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
19:16	BUF1_BS_ADDR2	Base address over 32 bits of memory buffer1 for PWM0's waveform data Note: The memory buffer1 is useless in periodical mode.
3:0	BUF0_BS_ADDR2	Base address over 32 bits of memory buffer0 for PWM0's waveform data Note: The memory buffer1 is useless in periodical mode.

100480C0	PWM1_CON				PWM control register								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PWM_INT_STA_UDF	PWM_INT_STA_FIN	PWM_INT_EN_UDF	PWM_INT_EN_FIN							DELAY_EN	DELAY_CKSRC	PWM1_3DLCM	PWM1_3DLCM_BASE	PWM1_3DLCM_INV	PWM1_EN_CHN
Type	RO	RO	RW	RW							RW	RW	RW	RW	RW	RW
Reset	0	0	0	0							0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PWM_INT_STA_UDF	PWM interrupt for underflow. Write 1 to clear.
30	PWM_INT_STA_FIN	PWM interrupt for finish. Write 1 to clear.
29	PWM_INT_EN_UDF	PWM interrupt enable presents for underflow. 1: Enable 0: Disable
28	PWM_INT_EN_FIN	PWM interrupt enable presents for finish. 1: Enable 0: Disable
21	DELAY_EN	Sequential mode enable
20	DELAY_CKSRC	Sequential mode clock source divisor: 1625
19	PWM1_3DLCM	This channel invert or not in 3dlcm mode
18	PWM1_3DLCM_BASE	This channel is as 3dlcm base channel
17	PWM1_3DLCM_INV	This channel enable 3dlcm mode or not
16	PWM1_EN_CHN	PWM1_EN at channel side. This bit will work if and only if CHANNEL_LOCK of this channel is enabled.
15	OLD_PWM_MODE	Uses Standard PWM mode Note: Using Standard PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. However, only Standard PWM mode with 32-kHz clock cannot work in system sleep mode. (Legacy PWM mode indicates non-old mode; Standard PWM mode indicates old mode) 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	Stop bit position for source data in periodical mode

Bit(s)	Name	Description
		In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	PWM1 output value during guard time
7	IDLE_VALUE	PWM1 output value in idle state
6	MODE	Selects random generator mode 0: Periodical PWM mode. 1: Random PWM mode
5	SRCSEL	Selects PWM1 data source 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	Old Mode select 32-kHz clock 0: CLK = 32-kHz; CLK is not used. 1: CLK = 32-kHz; CLK can be used.
3	CLKSEL	Clock source divisor: 1625 (old/FIFO/memory/random/kick/SMC mode) 0: CLK = CLKSRC 1: CLK = CLKSRC/1625
2:0	CLKDIV	Selects PWM1 clock scale 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

100480C4 PWM1_HIGH_DURATION PWM high duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HDURATION	PWM1 pulse duration based on the current clock when PWM1 output is high If duration =N, program N-1 in this register. Note: The duration of PWM1 must not be 0.

100480C8 PWM1_LOW_DURATION PWM low duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	LDURATION	PWM1 pulse duration based on the current clock when PWM1 output is low If duration =N, program N-1 in this register. Note: The duration of PWM1 must not be 0.

100480CC PWM1_DG_DURATION PWM delay/guard duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DELAY_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DELAY_DURATION	Guarding interval between individual waveforms and the output is decided by GUARD_VALUE If it equals N, program N-1 in this register. Note: 1. If this duration is 0, it means there is no guarding interval. 2. The guard duration of standard mode is set by PWM_DATA_WIDTH.
15:0	GUARD_DURATION	Guarding interval between individual waveforms and the output is decided by GUARD_VALUE

100480D0 PWM1_BUF0_BASE_ADDR PWM buffer 0 base address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of memory buffer0 for PWM1's waveform data

100480D4 PWM1 BUF0_SIZE PWM buffer size register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	Length of waveform data in memory buffer0 PWM1 should generate If it equals N, program N-1 in this register. Note: The size is in unit of 32-bit data.

100480D8 PWM1 BUF1_BASE_ADDR PWM buffer 1 base address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	Base address of memory buffer1 for PWM1's waveform data Note: The memory buffer1 is useless in periodical mode.

100480DC **PWM1 BUF1_SIZE** **PWM buffer size register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	Length of waveform data in memory buffer1 PWM1 should generate If it equals N, program N-1 in this register.

100480E0 **PWM1 SEND_DATA0** **PWM send data 0 register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	PWM1 local buffer0 of pulse sequence data to be generated Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

100480E4 PWM1_SEND_DATA1 PWM send data 1 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	PWM1 local buffer0 of pulse sequence data to be generated Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

100480E8 PWM1_WAVE_NUM PWM wave number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	Number by which PWM0 will generate from pulse data repeatedly Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.

100480EC PWM1 DATA WIDTH PWM data width register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_WIDTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DATA_WIDTH	PWM1 pulse data width in Standard PWM mode

100480F0 PWM1 THRESH PWM threshold width register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	THRESH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	THRESH	PWM1 pulse data high/low switching threshold in Standard PWM mode

100480F4 **PWM1_SEND_WAVENUM** PWM wave number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HSEC_USAGE															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HSEC_USAGE	Memory mode, random mode security usage
15:0	SEND_WAVENUM	Number by which PWM1 has already generated from specified data source in periodical mode

100480F8	<u>PWM1_VALID</u>				PWM wave number register										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready. 0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready.
0	BUF0_VALID	When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready. 0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready.

100480FC **PWM1 BUF BASE ADDR2** PWM buffer base address 2 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BUF1_BS_ADDR2			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BUF0_BS_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
19:16	BUF1_BS_ADDR2	Base address over 32 bits of memory buffer1 for PWM1's waveform data Note: The memory buffer1 is useless in periodical mode.
3:0	BUF0_BS_ADDR2	Base address over 32 bits of memory buffer0 for PWM1's waveform data Note: The memory buffer1 is useless in periodical mode.

10048100 PWM2_CON PWM control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PWM_INT_STA_UDF	PWM_INT_STA_FIN	PWM_INT_EN_UDF	PWM_INT_EN_FIN							DELAY_EN	DELAY_CKSRC	PWM2_3DLCM	PWM2_3DLCM_BASE	PWM2_3DLCM_INV	PWM2_EN_CHN
Type	RO	RO	RW	RW							RW	RW	RW	RW	RW	RW
Reset	0	0	0	0							0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PWM_INT_STA_UDF	PWM interrupt for underflow. Write 1 to clear.
30	PWM_INT_STA_FIN	PWM interrupt for finish. Write 1 to clear.
29	PWM_INT_EN_UDF	PWM interrupt enable presents for underflow. 1: Enable 0: Disable
28	PWM_INT_EN_FIN	PWM interrupt enable presents for finish. 1: Enable 0: Disable
21	DELAY_EN	Sequential mode enable
20	DELAY_CKSRC	Sequential mode clock source divisor: 1625
19	PWM2_3DLCM	This channel invert or not in 3dlcm mode
18	PWM2_3DLCM_BASE	This channel is as 3dlcm base channel
17	PWM2_3DLCM_INV	This channel enable 3dlcm mode or not
16	PWM2_EN_CHN	PWM2_EN at channel side. This bit will work if and only if CHANNEL_LOCK of this channel is enabled.
15	OLD_PWM_MODE	Uses Standard PWM mode Note: Using Standard PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. However, only Standard PWM mode with 32-kHz clock cannot work in system sleep mode. (Legacy PWM mode indicates non-old mode; Standard PWM mode indicates old mode) 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	Stop bit position for source data in periodical mode

Bit(s)	Name	Description
		In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	PWM2 output value during guard time
7	IDLE_VALUE	PWM2 output value in idle state
6	MODE	Selects random generator mode 0: Periodical PWM mode. 1: Random PWM mode
5	SRCSEL	Selects PWM2 data source 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	Old Mode select 32-kHz clock 0: CLK = 32-kHz; CLK is not used. 1: CLK = 32-kHz; CLK can be used.
3	CLKSEL	Clock source divisor: 1625 (old/FIFO/memory/random/kick/SMC mode) 0: CLK = CLKSRC 1: CLK = CLKSRC/1625
2:0	CLKDIV	Selects PWM2 clock scale 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

10048104 PWM2_HIGH_DURATION PWM high duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HDURATION	PWM2 pulse duration based on the current clock when PWM2 output is high If duration =N, program N-1 in this register. Note: The duration of PWM2 must not be 0.

10048108 PWM2_LOW_DURATION PWM low duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	LDURATION	PWM2 pulse duration based on the current clock when PWM2 output is low If duration =N, program N-1 in this register. Note: The duration of PWM2 must not be 0.

1004810C PWM2_DG_DURATION PWM delay/guard duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DELAY_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DELAY_DURATION	Guarding interval between individual waveforms and the output is decided by GUARD_VALUE If it equals N, program N-1 in this register. Note: 1. If this duration is 0, it means there is no guarding interval. 2. The guard duration of standard mode is set by PWM_DATA_WIDTH.
15:0	GUARD_DURATION	Guarding interval between individual waveforms and the output is decided by GUARD_VALUE

10048110 PWM2_BUF0_BASE_ADDR PWM buffer 0 base address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of memory buffer0 for PWM2's waveform data

10048114 **PWM2 BUF0_SIZE** **PWM buffer size register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	Length of waveform data in memory buffer0 PWM2 should generate If it equals N, program N-1 in this register. Note: The size is in unit of 32-bit data.

10048118 **PWM2 BUF1_BASE_ADDR** **PWM buffer 1 base address register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	Base address of memory buffer1 for PWM2's waveform data Note: The memory buffer1 is useless in periodical mode.

1004811C **PWM2_BUF1_SIZE** **PWM buffer size register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	Length of waveform data in memory buffer1 PWM2 should generate If it equals N, program N-1 in this register.

10048120 **PWM2_SEND_DATA0** **PWM send data 0 register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	PWM2 local buffer0 of pulse sequence data to be generated Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

10048124 PWM2_SEND_DATA1 PWM send data 1 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	PWM2 local buffer0 of pulse sequence data to be generated Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

10048128 PWM2_WAVE_NUM PWM wave number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	Number by which PWM0 will generate from pulse data repeatedly Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.

1004812C PWM2_DATA_WIDTH PWM data width register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_WIDTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DATA_WIDTH	PWM2 pulse data width in Standard PWM mode

10048130 PWM2_THRESH PWM threshold width register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	THRESH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	THRESH	PWM2 pulse data high/low switching threshold in Standard PWM mode

10048134 PWM2_SEND_WAVENUM PWM wave number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HSEC_USAGE															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HSEC_USAGE	Memory mode, random mode security usage
15:0	SEND_WAVENUM	Number by which PWM2 has already generated from specified data source in periodical mode

10048138 PWM2_VALID PWM wave number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready. 0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready.
0	BUF0_VALID	When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready. 0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready.

1004813C **PWM2 BUF BASE ADDR2** PWM buffer base address 2 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BUF1_BS_ADDR2			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BUF0_BS_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
19:16	BUF1_BS_ADDR2	Base address over 32 bits of memory buffer1 for PWM2's waveform data Note: The memory buffer1 is useless in periodical mode.
3:0	BUF0_BS_ADDR2	Base address over 32 bits of memory buffer0 for PWM2's waveform data Note: The memory buffer1 is useless in periodical mode.

10048140 PWM3_CON PWM control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PWM_INT_STA_UDF	PWM_INT_STA_FIN	PWM_INT_EN_UDF	PWM_INT_EN_FIN							DELAY_EN	DELAY_CKSRC	PWM3_3DLCM	PWM3_3DLCM_BASE	PWM3_3DLCM_INV	PWM3_EN_CHN
Type	RO	RO	RW	RW							RW	RW	RW	RW	RW	RW
Reset	0	0	0	0							0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PWM_INT_STA_UDF	PWM interrupt for underflow. Write 1 to clear.
30	PWM_INT_STA_FIN	PWM interrupt for finish. Write 1 to clear.
29	PWM_INT_EN_UDF	PWM interrupt enable presents for underflow. 1: Enable 0: Disable
28	PWM_INT_EN_FIN	PWM interrupt enable presents for finish. 1: Enable 0: Disable
21	DELAY_EN	Sequential mode enable
20	DELAY_CKSRC	Sequential mode clock source divisor: 1625
19	PWM3_3DLCM	This channel invert or not in 3dlcm mode
18	PWM3_3DLCM_BASE	This channel is as 3dlcm base channel
17	PWM3_3DLCM_INV	This channel enable 3dlcm mode or not
16	PWM3_EN_CHN	PWM3_EN at channel side. This bit will work if and only if CHANNEL_LOCK of this channel is enabled.
15	OLD_PWM_MODE	Uses Standard PWM mode Note: Using Standard PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. However, only Standard PWM mode with 32-kHz clock cannot work in system sleep mode. (Legacy PWM mode indicates non-old mode; Standard PWM mode indicates old mode) 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	Stop bit position for source data in periodical mode

Bit(s)	Name	Description
		In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	PWM3 output value during guard time
7	IDLE_VALUE	PWM3 output value in idle state
6	MODE	Selects random generator mode 0: Periodical PWM mode. 1: Random PWM mode
5	SRCSEL	Selects PWM3 data source 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	Old Mode select 32-kHz clock 0: CLK = 32-kHz; CLK is not used. 1: CLK = 32-kHz; CLK can be used.
3	CLKSEL	Clock source divisor: 1625 (old/FIFO/memory/random/kick/SMC mode) 0: CLK = CLKSRC 1: CLK = CLKSRC/1625
2:0	CLKDIV	Selects PWM3 clock scale 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

10048144 PWM3_HIGH_DURATION PWM high duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HDURATION	PWM3 pulse duration based on the current clock when PWM3 output is high If duration =N, program N-1 in this register. Note: The duration of PWM3 must not be 0.

10048148 PWM3_LOW_DURATION PWM low duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	LDURATION	PWM3 pulse duration based on the current clock when PWM3 output is low If duration =N, program N-1 in this register. Note: The duration of PWM3 must not be 0.

1004814C PWM3_DG_DURATION PWM delay/guard duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DELAY_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DELAY_DURATION	Guarding interval between individual waveforms and the output is decided by GUARD_VALUE If it equals N, program N-1 in this register. Note: 1. If this duration is 0, it means there is no guarding interval. 2. The guard duration of standard mode is set by PWM_DATA_WIDTH.
15:0	GUARD_DURATION	Guarding interval between individual waveforms and the output is decided by GUARD_VALUE

10048150 PWM3_BUF0_BASE_ADDR PWM buffer 0 base address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of memory buffer0 for PWM3's waveform data

10048154 PWM3 BUF0_SIZE PWM buffer size register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	Length of waveform data in memory buffer0 PWM3 should generate If it equals N, program N-1 in this register. Note: The size is in unit of 32-bit data.

10048158 PWM3 BUF1_BASE_ADDR PWM buffer 1 base address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	Base address of memory buffer1 for PWM3's waveform data Note: The memory buffer1 is useless in periodical mode.

1004815C PWM3 BUF1_SIZE PWM buffer size register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	Length of waveform data in memory buffer1 PWM3 should generate If it equals N, program N-1 in this register.

10048160 PWM3 SEND_DATA0 PWM send data 0 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	PWM3 local buffer0 of pulse sequence data to be generated Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

10048164 **PWM3_SEND_DATA1** **PWM send data 1 register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	PWM3 local buffer0 of pulse sequence data to be generated Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

10048168 **PWM3_WAVE_NUM** **PWM wave number register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	Number by which PWM0 will generate from pulse data repeatedly Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.

1004816C PWM3 DATA WIDTH PWM data width register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_WIDTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DATA_WIDTH	PWM3 pulse data width in Standard PWM mode

10048170 PWM3 THRESH PWM threshold width register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	THRESH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	THRESH	PWM3 pulse data high/low switching threshold in Standard PWM mode

10048174 **PWM3_SEND_WAVENUM** PWM wave number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HSEC_USAGE															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HSEC_USAGE	Memory mode, random mode security usage
15:0	SEND_WAVENUM	Number by which PWM3 has already generated from specified data source in periodical mode

10048178 **PWM3_VALID** **PWM wave number register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready. 0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready.
0	BUF0_VALID	When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready. 0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready.

1004817C PWM3 BUF BASE ADDR2 PWM buffer base address 2 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BUF1_BS_ADDR2			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BUF0_BS_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
19:16	BUF1_BS_ADDR2	Base address over 32 bits of memory buffer1 for PWM3's waveform data Note: The memory buffer1 is useless in periodical mode.
3:0	BUF0_BS_ADDR2	Base address over 32 bits of memory buffer0 for PWM3's waveform data Note: The memory buffer1 is useless in periodical mode.

10048180 PWM4_CON PWM control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PWM_INT_STA_UDF	PWM_INT_STA_FIN	PWM_INT_EN_UDF	PWM_INT_EN_FIN							DELAY_EN	DELAY_CKSRC	PWM4_3DLCM	PWM4_3DLCM_BASE	PWM4_3DLCM_INV	PWM4_EN_CHN
Type	RO	RO	RW	RW							RW	RW	RW	RW	RW	RW
Reset	0	0	0	0							0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PWM_INT_STA_UDF	PWM interrupt for underflow. Write 1 to clear.
30	PWM_INT_STA_FIN	PWM interrupt for finish. Write 1 to clear.
29	PWM_INT_EN_UDF	PWM interrupt enable presents for underflow. 1: Enable 0: Disable
28	PWM_INT_EN_FIN	PWM interrupt enable presents for finish. 1: Enable 0: Disable
21	DELAY_EN	Sequential mode enable
20	DELAY_CKSRC	Sequential mode clock source divisor: 1625
19	PWM4_3DLCM	This channel invert or not in 3dlcm mode
18	PWM4_3DLCM_BASE	This channel is as 3dlcm base channel
17	PWM4_3DLCM_INV	This channel enable 3dlcm mode or not
16	PWM4_EN_CHN	PWM4_EN at channel side. This bit will work if and only if CHANNEL_LOCK of this channel is enabled.
15	OLD_PWM_MODE	Uses Standard PWM mode Note: Using Standard PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. However, only Standard PWM mode with 32-kHz clock cannot work in system sleep mode. (Legacy PWM mode indicates non-old mode; Standard PWM mode indicates old mode) 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	Stop bit position for source data in periodical mode

Bit(s)	Name	Description
		In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	PWM4 output value during guard time
7	IDLE_VALUE	PWM4 output value in idle state
6	MODE	Selects random generator mode 0: Periodical PWM mode. 1: Random PWM mode
5	SRCSEL	Selects PWM4 data source 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	Old Mode select 32-kHz clock 0: CLK = 32-kHz; CLK is not used. 1: CLK = 32-kHz; CLK can be used.
3	CLKSEL	Clock source divisor: 1625 (old/FIFO/memory/random/kick/SMC mode) 0: CLK = CLKSRC 1: CLK = CLKSRC/1625
2:0	CLKDIV	Selects PWM4 clock scale 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

10048184 PWM4_HIGH_DURATION PWM high duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HDURATION	PWM4 pulse duration based on the current clock when PWM4 output is high If duration =N, program N-1 in this register. Note: The duration of PWM4 must not be 0.

10048188 PWM4_LOW_DURATION PWM low duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	LDURATION	PWM4 pulse duration based on the current clock when PWM4 output is low If duration =N, program N-1 in this register. Note: The duration of PWM4 must not be 0.

1004818C PWM4_DG_DURATION PWM delay/guard duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DELAY_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DELAY_DURATION	Guarding interval between individual waveforms and the output is decided by GUARD_VALUE If it equals N, program N-1 in this register. Note: 1. If this duration is 0, it means there is no guarding interval. 2. The guard duration of standard mode is set by PWM_DATA_WIDTH.
15:0	GUARD_DURATION	Guarding interval between individual waveforms and the output is decided by GUARD_VALUE

10048190 PWM4_BUF0_BASE_ADDR PWM buffer 0 base address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of memory buffer0 for PWM4's waveform data

10048194 **PWM4 BUF0_SIZE** **PWM buffer size register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	Length of waveform data in memory buffer0 PWM4 should generate If it equals N, program N-1 in this register. Note: The size is in unit of 32-bit data.

10048198 **PWM4 BUF1_BASE_ADDR** **PWM buffer 1 base address register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	Base address of memory buffer1 for PWM4's waveform data Note: The memory buffer1 is useless in periodical mode.

1004819C **PWM4 BUF1_SIZE** **PWM buffer size register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	Length of waveform data in memory buffer1 PWM4 should generate If it equals N, program N-1 in this register.

100481A0 **PWM4 SEND_DATA0** **PWM send data 0 register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	PWM4 local buffer0 of pulse sequence data to be generated Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

100481A4 **PWM4_SEND_DATA1** **PWM send data 1 register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	PWM4 local buffer0 of pulse sequence data to be generated Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

100481A8 **PWM4_WAVE_NUM** **PWM wave number register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	Number by which PWM0 will generate from pulse data repeatedly Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.

100481AC **PWM4 DATA WIDTH** **PWM data width register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_WIDTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DATA_WIDTH	PWM4 pulse data width in Standard PWM mode

100481B0 **PWM4 THRESH** **PWM threshold width register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	THRESH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	THRESH	PWM4 pulse data high/low switching threshold in Standard PWM mode

100481B4 **PWM4_SEND_WAVENUM** PWM wave number register **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HSEC_USAGE															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HSEC_USAGE	Memory mode, random mode security usage
15:0	SEND_WAVENUM	Number by which PWM4 has already generated from specified data source in periodical mode

100481B8 **PWM4_VALID** PWM wave number register **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready. 0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready.
0	BUF0_VALID	When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready. 0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready.

100481BC **PWM4 BUF BASE ADDR2** PWM buffer base address 2 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BUF1_BS_ADDR2			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BUF0_BS_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
19:16	BUF1_BS_ADDR2	Base address over 32 bits of memory buffer1 for PWM4's waveform data Note: The memory buffer1 is useless in periodical mode.
3:0	BUF0_BS_ADDR2	Base address over 32 bits of memory buffer0 for PWM4's waveform data Note: The memory buffer1 is useless in periodical mode.

100481C0 PWM5_CON PWM control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PWM_INT_STA_UDF	PWM_INT_STA_FIN	PWM_INT_EN_UDF	PWM_INT_EN_FIN							DELAY_EN	DELAY_CKSRC	PWM5_3DLCM	PWM5_3DLCM_BASE	PWM5_3DLCM_INV	PWM5_EN_CHN
Type	RO	RO	RW	RW							RW	RW	RW	RW	RW	RW
Reset	0	0	0	0							0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PWM_INT_STA_UDF	PWM interrupt for underflow. Write 1 to clear.
30	PWM_INT_STA_FIN	PWM interrupt presents for finish. Write 1 to clear.
29	PWM_INT_EN_UDF	PWM interrupt enable presents for underflow. 1: Enable 0: Disable
28	PWM_INT_EN_FIN	PWM interrupt enable presents for finish. 1: Enable 0: Disable
21	DELAY_EN	Sequential mode enable
20	DELAY_CKSRC	Sequential mode clock source divisor: 1625
19	PWM5_3DLCM	This channel invert or not in 3dlcm mode
18	PWM5_3DLCM_BASE	This channel is as 3dlcm base channel
17	PWM5_3DLCM_INV	This channel enable 3dlcm mode or not
16	PWM5_EN_CHN	PWM5_EN at channel side. This bit will work if and only if CHANNEL_LOCK of this channel is enabled.
15	OLD_PWM_MODE	Uses Standard PWM mode Note: Using Standard PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. However, only Standard PWM mode with 32-kHz clock cannot work in system sleep mode. (Legacy PWM mode indicates non-old mode; Standard PWM mode indicates old mode) 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	Stop bit position for source data in periodical mode

Bit(s)	Name	Description
		In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	PWM5 output value during guard time
7	IDLE_VALUE	PWM5 output value in idle state
6	MODE	Selects random generator mode 0: Periodical PWM mode. 1: Random PWM mode
5	SRCSEL	Selects PWM5 data source 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	Old Mode select 32-kHz clock 0: CLK = 32-kHz; CLK is not used. 1: CLK = 32-kHz; CLK can be used.
3	CLKSEL	Clock source divisor: 1625 (old/FIFO/memory/random/kick/SMC mode) 0: CLK = CLKSRC 1: CLK = CLKSRC/1625
2:0	CLKDIV	Selects PWM5 clock scale 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

100481C4 PWM5_HIGH_DURATION PWM high duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HDURATION	PWM5 pulse duration based on the current clock when PWM5 output is high If duration =N, program N-1 in this register. Note: The duration of PWM5 must not be 0.

100481C8 PWM5 LOW DURATION PWM low duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	LDURATION	PWM5 pulse duration based on the current clock when PWM5 output is low If duration = N, program N-1 in this register. Note: The duration of PWM5 must not be 0.

100481CC PWM5 DG DURATION PWM delay/guard duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DELAY_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DELAY_DURATION	Guarding interval between individual waveforms and the output is decided by GUARD_VALUE If it equals N, program N-1 in this register. Note: 1. If this duration is 0, it means there is no guarding interval. 2. The guard duration of standard mode is set by PWM_DATA_WIDTH.
15:0	GUARD_DURATION	Guarding interval between individual waveforms and the output is decided by GUARD_VALUE

100481D0 **PWM5_BUF0_BASE_ADDR** PWM buffer 0 base address register **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of memory buffer0 for PWM5's waveform data

100481D4 **PWM5_BUF0_SIZE** PWM buffer size register **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	Length of waveform data in memory buffer0 PWM5 should generate If it equals N, program N-1 in this register. Note: The size is in unit of 32-bit data.

100481D8 PWM5 BUF1 BASE_ADDR PWM buffer 1 base address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	Base address of memory buffer1 for PWM5's waveform data Note: The memory buffer1 is useless in periodical mode.

100481DC PWM5 BUF1_SIZE PWM buffer size register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	Length of waveform data in memory buffer1 PWM5 should generate If it equals N, program N-1 in this register.

100481E0 **PWM5_SEND_DATA0** **PWM send data 0 register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	PWM5 local buffer0 of pulse sequence data to be generated Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

100481E4 **PWM5_SEND_DATA1** **PWM send data 1 register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	PWM5 local buffer0 of pulse sequence data to be generated Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

100481E8 **PWM5_WAVE_NUM** **PWM wave number register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	Number by which PWM0 will generate from pulse data repeatedly Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.

100481EC **PWM5_DATA_WIDTH** **PWM data width register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_WIDTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DATA_WIDTH	PWM5 pulse data width in Standard PWM mode

100481F0 **PWM5_THRESH** **PWM threshold width register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	THRESH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	THRESH	PWM5 pulse data high/low switching threshold in Standard PWM mode

100481F4 **PWM5_SEND_WAVENUM** **PWM wave number register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HSEC_USAGE															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HSEC_USAGE	Memory mode, random mode security usage
15:0	SEND_WAVENUM	Number by which PWM5 has already generated from specified data source in periodical mode

100481F8	<u>PWM5_VALID</u>				PWM wave number register										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready. 0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready.
0	BUF0_VALID	When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready. 0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready.

100481FC **PWM5 BUF BASE ADDR2** PWM buffer base address 2 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BUF1_BS_ADDR2			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BUF0_BS_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
19:16	BUF1_BS_ADDR2	Base address over 32 bits of memory buffer1 for PWM5's waveform data Note: The memory buffer1 is useless in periodical mode.
3:0	BUF0_BS_ADDR2	Base address over 32 bits of memory buffer0 for PWM5's waveform data Note: The memory buffer1 is useless in periodical mode.

10048200	PWM6_CON				PWM control register								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PWM_INT_STA_UDF	PWM_INT_STA_FIN	PWM_INT_EN_UDF	PWM_INT_EN_FIN							DELAY_EN	DELAY_CKSRC	PWM6_3DLCM	PWM6_3DLCM_BASE	PWM6_3DLCM_INV	PWM6_EN_CHN
Type	RO	RO	RW	RW							RW	RW	RW	RW	RW	RW
Reset	0	0	0	0							0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PWM_INT_STA_UDF	PWM interrupt for underflow. Write 1 to clear.
30	PWM_INT_STA_FIN	PWM interrupt for finish. Write 1 to clear.
29	PWM_INT_EN_UDF	PWM interrupt enable presents for underflow. 1: Enable 0: Disable
28	PWM_INT_EN_FIN	PWM interrupt enable presents for finish. 1: Enable 0: Disable
21	DELAY_EN	Sequential mode enable
20	DELAY_CKSRC	Sequential mode clock source divisor: 1625
19	PWM6_3DLCM	This channel invert or not in 3dlcm mode
18	PWM6_3DLCM_BASE	This channel is as 3dlcm base channel
17	PWM6_3DLCM_INV	This channel enable 3dlcm mode or not
16	PWM6_EN_CHN	PWM6_EN at channel side. This bit will work if and only if CHANNEL_LOCK of this channel is enabled.
15	OLD_PWM_MODE	Uses Standard PWM mode Note: Using Standard PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. However, only Standard PWM mode with 32-kHz clock cannot work in system sleep mode. (Legacy PWM mode indicates non-old mode; Standard PWM mode indicates old mode) 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	Stop bit position for source data in periodical mode

Bit(s)	Name	Description
		In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	PWM6 output value during guard time
7	IDLE_VALUE	PWM6 output value in idle state
6	MODE	Selects random generator mode 0: Periodical PWM mode. 1: Random PWM mode
5	SRCSEL	Selects PWM6 data source 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	Old Mode select 32-kHz clock 0: CLK = 32-kHz; CLK is not used. 1: CLK = 32-kHz; CLK can be used.
3	CLKSEL	Clock source divisor: 1625 (old/FIFO/memory/random/kick/SMC mode) 0: CLK = CLKSRC 1: CLK = CLKSRC/1625
2:0	CLKDIV	Selects PWM6 clock scale 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

10048204 PWM6_HIGH_DURATION PWM high duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HDURATION	PWM6 pulse duration based on the current clock when PWM6 output is high If duration =N, program N-1 in this register. Note: The duration of PWM6 must not be 0.

10048208 PWM6_LOW_DURATION PWM low duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	LDURATION	PWM6 pulse duration based on the current clock when PWM6 output is low If duration =N, program N-1 in this register. Note: The duration of PWM6 must not be 0.

1004820C PWM6_DG_DURATION PWM delay/guard duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DELAY_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DELAY_DURATION	Guarding interval between individual waveforms and the output is decided by GUARD_VALUE If it equals N, program N-1 in this register. Note: 1. If this duration is 0, it means there is no guarding interval. 2. The guard duration of standard mode is set by PWM_DATA_WIDTH.
15:0	GUARD_DURATION	Guarding interval between individual waveforms and the output is decided by GUARD_VALUE

10048210 PWM6_BUF0_BASE_ADDR PWM buffer 0 base address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of memory buffer0 for PWM6's waveform data

10048214 **PWM6 BUF0_SIZE** **PWM buffer size register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	Length of waveform data in memory buffer0 PWM6 should generate If it equals N, program N-1 in this register. Note: The size is in unit of 32-bit data.

10048218 **PWM6 BUF1_BASE_ADDR** **PWM buffer 1 base address register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	Base address of memory buffer1 for PWM6's waveform data Note: The memory buffer1 is useless in periodical mode.

1004821C **PWM6 BUF1_SIZE** **PWM buffer size register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	Length of waveform data in memory buffer1 PWM6 should generate If it equals N, program N-1 in this register.

10048220 **PWM6 SEND_DATA0** **PWM send data 0 register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	PWM6 local buffer0 of pulse sequence data to be generated Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

10048224 **PWM6_SEND_DATA1** **PWM send data 1 register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	PWM6 local buffer0 of pulse sequence data to be generated Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

10048228 **PWM6_WAVE_NUM** **PWM wave number register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	Number by which PWM0 will generate from pulse data repeatedly Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.

1004822C PWM6 DATA WIDTH PWM data width register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_WIDTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DATA_WIDTH	PWM6 pulse data width in Standard PWM mode

10048230 PWM6 THRESH PWM threshold width register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	THRESH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	THRESH	PWM6 pulse data high/low switching threshold in Standard PWM mode

10048234 PWM6_SEND_WAVENUM PWM wave number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HSEC_USAGE															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HSEC_USAGE	Memory mode, random mode security usage
15:0	SEND_WAVENUM	Number by which PWM6 has already generated from specified data source in periodical mode

10048238 PWM6_VALID PWM wave number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready. 0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready.
0	BUF0_VALID	When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready. 0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready.

1004823C PWM6 BUF BASE ADDR2 PWM buffer base address 2 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BUF1_BS_ADDR2			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BUF0_BS_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
19:16	BUF1_BS_ADDR2	Base address over 32 bits of memory buffer1 for PWM6's waveform data Note: The memory buffer1 is useless in periodical mode.
3:0	BUF0_BS_ADDR2	Base address over 32 bits of memory buffer0 for PWM6's waveform data Note: The memory buffer1 is useless in periodical mode.

10048240 PWM7_CON PWM control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PWM_INT_STA_UDF	PWM_INT_STA_FIN	PWM_INT_EN_UDF	PWM_INT_EN_FIN							DELAY_EN	DELAY_CKSRC	PWM7_3DLCM	PWM7_3DLCM_BASE	PWM7_3DLCM_INV	PWM7_EN_CHN
Type	RO	RO	RW	RW							RW	RW	RW	RW	RW	RW
Reset	0	0	0	0							0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PWM_INT_STA_UDF	PWM interrupt for underflow. Write 1 to clear.
30	PWM_INT_STA_FIN	PWM interrupt for finish. Write 1 to clear.
29	PWM_INT_EN_UDF	PWM interrupt enable presents for underflow. 1: Enable 0: Disable
28	PWM_INT_EN_FIN	PWM interrupt enable presents for finish. 1: Enable 0: Disable
21	DELAY_EN	Sequential mode enable
20	DELAY_CKSRC	Sequential mode clock source divisor: 1625
19	PWM7_3DLCM	This channel invert or not in 3dlcm mode
18	PWM7_3DLCM_BASE	This channel is as 3dlcm base channel
17	PWM7_3DLCM_INV	This channel enable 3dlcm mode or not
16	PWM7_EN_CHN	PWM7_EN at channel side. This bit will work if and only if CHANNEL_LOCK of this channel is enabled.
15	OLD_PWM_MODE	Uses Standard PWM mode Note: Using Standard PWM mode also means using periodical mode. Therefore, SRCSEL and MODE are ignored in this situation. However, only Standard PWM mode with 32-kHz clock cannot work in system sleep mode. (Legacy PWM mode indicates non-old mode; Standard PWM mode indicates old mode) 0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	Stop bit position for source data in periodical mode

Bit(s)	Name	Description
		In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	PWM7 output value during guard time
7	IDLE_VALUE	PWM7 output value in idle state
6	MODE	Selects random generator mode 0: Periodical PWM mode. 1: Random PWM mode
5	SRCSEL	Selects PWM7 data source 0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	Old Mode select 32-kHz clock 0: CLK = 32-kHz; CLK is not used. 1: CLK = 32-kHz; CLK can be used.
3	CLKSEL	Clock source divisor: 1625 (old/FIFO/memory/random/kick/SMC mode) 0: CLK = CLKSRC 1: CLK = CLKSRC/1625
2:0	CLKDIV	Selects PWM7 clock scale 000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

10048244 PWM7_HIGH_DURATION PWM high duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HDURATION	PWM7 pulse duration based on the current clock when PWM7 output is high If duration =N, program N-1 in this register. Note: The duration of PWM7 must not be 0.

10048248 PWM7_LOW_DURATION PWM low duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	LDURATION	PWM7 pulse duration based on the current clock when PWM7 output is low If duration =N, program N-1 in this register. Note: The duration of PWM7 must not be 0.

1004824C PWM7_DG_DURATION PWM delay/guard duration register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DELAY_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DELAY_DURATION	Guarding interval between individual waveforms and the output is decided by GUARD_VALUE If it equals N, program N-1 in this register. Note: 1. If this duration is 0, it means there is no guarding interval. 2. The guard duration of standard mode is set by PWM_DATA_WIDTH.
15:0	GUARD_DURATION	Guarding interval between individual waveforms and the output is decided by GUARD_VALUE

10048250 PWM7_BUF0_BASE_ADDR PWM buffer 0 base address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	Base address of memory buffer0 for PWM7's waveform data

10048254 PWM7 BUF0_SIZE PWM buffer size register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	Length of waveform data in memory buffer0 PWM7 should generate If it equals N, program N-1 in this register. Note: The size is in unit of 32-bit data.

10048258 PWM7 BUF1_BASE_ADDR PWM buffer 1 base address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	Base address of memory buffer1 for PWM7's waveform data Note: The memory buffer1 is useless in periodical mode.

1004825C PWM7 BUF1_SIZE PWM buffer size register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	Length of waveform data in memory buffer1 PWM7 should generate If it equals N, program N-1 in this register.

10048260 PWM7 SEND_DATA0 PWM send data 0 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	PWM7 local buffer0 of pulse sequence data to be generated Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

10048264 **PWM7_SEND_DATA1** **PWM send data 1 register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	PWM7 local buffer0 of pulse sequence data to be generated Note: This value should be written only in periodically FIFO mode. In other modes, this buffer is for internal memory access.

10048268 **PWM7_WAVE_NUM** **PWM wave number register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	Number by which PWM0 will generate from pulse data repeatedly Note: If WAVE_NUM=0, the waveform generation will not stop until it is disabled.

1004826C **PWM7_DATA_WIDTH** **PWM data width register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_WIDTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DATA_WIDTH	PWM7 pulse data width in Standard PWM mode

10048270 **PWM7_THRESH** **PWM threshold width register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	THRESH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	THRESH	PWM7 pulse data high/low switching threshold in Standard PWM mode

10048274 **PWM7_SEND_WAVENUM** PWM wave number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HSEC_USAGE															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HSEC_USAGE	Memory mode, random mode security usage
15:0	SEND_WAVENUM	Number by which PWM7 has already generated from specified data source in periodical mode

10048278 **PWM7_VALID** PWM wave number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready. 0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready.
0	BUF0_VALID	When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready. 0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready.

1004827C PWM7 BUF BASE ADDR2 PWM buffer base address 2 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BUF1_BS_ADDR2			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BUF0_BS_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
19:16	BUF1_BS_ADDR2	Base address over 32 bits of memory buffer1 for PWM7's waveform data Note: The memory buffer1 is useless in periodical mode.
3:0	BUF0_BS_ADDR2	Base address over 32 bits of memory buffer0 for PWM7's waveform data Note: The memory buffer1 is useless in periodical mode.

10048000 PWM_ENABLE PWM enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PWM_EN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	PWM_EN	PWM enable at global side if CHANNEL_LOCK of that channel is disabled PWM_EN[0] points to PWM0 enable PWM_EN[1] points to PWM1 enable PWM_EN[n] points to PWMn enable

10048004 PWM_INT_ENABLE_FIN PWM finish interrupt enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PWM_INT_EN_FIN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	PWM_INT_EN_FIN	PWM interrupt enable for finish PWM_INT_EN_FIN[0] points to PWM0 finish interrupt enable PWM_INT_EN_FIN[1] points to PWM1 finish interrupt enable PWM_INT_EN_FIN[n] points to PWMn finish interrupt enable 1: Enable 0: Disable

10048008 PWM_INT_ENABLE_UDF PWM underflow interrupt enable register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PWM_INT_EN_UDF							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	PWM_INT_EN_UDF	PWM interrupt enable for underflow PWM_INT_EN_UDF[0] points to PWM0 underflow interrupt enable PWM_INT_EN_UDF[1] points to PWM1 underflow interrupt enable PWM_INT_EN_UDF[n] points to PWMn underflow interrupt enable 1: Enable 0: Disable

1004800C PWM_INT_STATUS_FIN PWM finish interrupt status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PWM_INT_STA_FIN							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	PWM_INT_STA_FIN	PWM interrupt for finish Condition 1: Number of wave sent reaches WAVE_NUM (old/FIFO/memory mode) Condition 2: Memory 0 or 1 is read empty (random mode) PWM_INT_STA_FIN[0] points to PWM0 finish interrupt status PWM_INT_STA_FIN[1] points to PWM1 finish interrupt status PWM_INT_STA_FIN[n] points to PWMn finish interrupt status

10048010 PWM_INT_STATUS_UDF PWM underflow interrupt status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PWM_INT_STA_UDF							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	PWM_INT_STA_UDF	PWM interrupt for underflow Condition: This interrupt occurs if current buffer data has been sent but another buffer data is not ready (memory/random mode AHB bandwidth limit) PWM_INT_STA_UDF[0] points to PWM0 underflow interrupt status PWM_INT_STA_UDF[1] points to PWM1 underflow interrupt status PWM_INT_STA_UDF[n] points to PWMn underflow interrupt status

10048014 PWM_INT_ACK_FIN PWM finish interrupt acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PWM_INT_ACK_FIN							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	PWM_INT_ACK_FIN	PWM interrupt clear for finish PWM_INT_ACK_FIN[0] points to PWM0 finish interrupt clear PWM_INT_ACK_FIN[1] points to PWM1 finish interrupt clear PWM_INT_ACK_FIN[n] points to PWMn finish interrupt clear

10048018 PWM_INT_ACK_UDF PWM underflow interrupt acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PWM_INT_ACK_UDF							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	PWM_INT_ACK_UDF	PWM interrupt clear for underflow PWM_INT_ACK_UDF[0] points to PWM0 underflow interrupt clear PWM_INT_ACK_UDF[1] points to PWM1 underflow interrupt clear PWM_INT_ACK_UDF[n] points to PWMn underflow interrupt clear

1004801C **PWM_EN_STATUS_UDF** **PWM enable status register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PWM_EN_STA							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	PWM_EN_STA	PWM enable status

10048020 **PWM_LOOP_BACK_TEST** **PWM loopback test** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									PWM_OUT							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	PWM_OUT	PWM_OUT monitor by APB

3.7 System Timer (sys_timer)

3.7.1 Register Definition

Module name: sys_timer Base address: (+0x1001_7000)

Address	Name	Width	Register Function
10017000	<u>CNTCR</u>	32	System counter control register
10017004	<u>CNTSR</u>	32	System counter status register
10017008	<u>CNTCV_L</u>	32	System counter count value low
1001700C	<u>CNTCV_H</u>	32	System counter count value high
10017010	<u>CNTWACR</u>	32	System counter write access control register
10017014	<u>CNTRACR</u>	32	System counter read access control register
10017018	<u>CNTACR_LOCK</u>	32	System counter access control lock register
1001701C	<u>CHICKEN</u>	32	Spare register
10017020	<u>CNTFID0</u>	32	System counter frequency table entry 0
10017024	<u>CNTFID1</u>	32	System counter frequency table entry 1
10017028	<u>CNTFID2</u>	32	System counter frequency table entry 2
1001702C	<u>CNTFIDE</u>	32	System counter frequency table entry end of line
10017030	<u>VERSION</u>	32	Version of system timer
10017034	<u>CNTR_32K_L</u>	32	Low part of 64-bit 32K counter
10017038	<u>CNTR_32K_H</u>	32	High part of 64-bit 32K counter
1001703C	<u>CNT_RCON</u>	32	Latch-value read control register
10017040	<u>CNTTVAL0_CON</u>	32	System counter timer 0 control register
10017044	<u>CNTTVAL0</u>	32	System counter timer 0 value register
10017048	<u>CNTTVAL1_CON</u>	32	System counter timer 1 control register
1001704C	<u>CNTTVAL1</u>	32	System counter timer 1 value register
10017050	<u>CNTTVAL2_CON</u>	32	System counter timer 2 control register
10017054	<u>CNTTVAL2</u>	32	System counter timer 2 value register
10017058	<u>CNTTVAL3_CON</u>	32	System counter timer 3 control register
1001705C	<u>CNTTVAL3</u>	32	System counter timer 3 value register
10017060	<u>CNTTVAL4_CON</u>	32	System counter timer 4 control register
10017064	<u>CNTTVAL4</u>	32	System counter timer 4 value register
10017068	<u>CNTTVAL5_CON</u>	32	System counter timer 5 control register
1001706C	<u>CNTTVAL5</u>	32	System counter timer 5 value register
10017070	<u>CNTTVAL6_CON</u>	32	System counter timer 6 control register
10017074	<u>CNTTVAL6</u>	32	System counter timer 6 value register
10017078	<u>CNTTVAL7_CON</u>	32	System counter timer 7 control register
1001707C	<u>CNTTVAL7</u>	32	System counter timer 7 value register
10017080	<u>DOMAIN_DIS</u>	32	Domain disable
10017084	<u>DOMAIN_VAL</u>	32	Domain value
10017090	<u>CNTRV_L_0</u>	32	Low-32-bit timer value set 0
10017094	<u>CNTRV_H_0</u>	32	High-32-bit timer value set 0
10017098	<u>CNTRV_L_1</u>	32	Low-32-bit timer value set 1
1001709C	<u>CNTRV_H_1</u>	32	High-32-bit timer value set 1
100170A0	<u>CNTRV_L_2</u>	32	Low-32-bit timer value set 2
100170A4	<u>CNTRV_H_2</u>	32	High-32-bit timer value set 2
100170A8	<u>CNTRV_L_3</u>	32	Low-32-bit timer value set 3
100170AC	<u>CNTRV_H_3</u>	32	High-32-bit timer value set 3
100170B0	<u>CNTRV_L_4</u>	32	Low-32-bit timer value set 4

Address	Name	Width	Register Function
100170B4	<u>CNTRV_H_4</u>	32	High-32-bit timer value set 4
100170B8	<u>CNTRV_L_5</u>	32	Low-32-bit timer value set 5
100170BC	<u>CNTRV_H_5</u>	32	High-32-bit timer value set 5
100170C0	<u>CNTRV_L_6</u>	32	Low-32-bit timer value set 6
100170C4	<u>CNTRV_H_6</u>	32	High-32-bit timer value set 6
100170C8	<u>CNTRV_L_7</u>	32	Low-32-bit timer value set 7
100170CC	<u>CNTRV_H_7</u>	32	High-32-bit timer value set 7

10017000		CNTCR		System counter control register												00001815	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name		R_32K_DEBEN															
Type		RW															
Reset		0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name			KP_LSB_9b_EN	COMP_25_EN	COMP_20_EN	COMP_15_EN							TIE_0_EN	CNT_32K_AS_EN	HDBG_EN	CNT_EN	
Type			RW	RW	RW	RW							RW	RW	RW	RW	
Reset			0	1	1	0							0	1	0	1	

Bit(s)	Name	Description
30	R_32K_DEBEN	Enables reading 32K counter for debugging 0: Disable 1: Enable
13	KP_LSB9b_EN	The 10 LSB will be 0 when the clock switches to 32 kHz if this bit is set. 0: Disable 1: Enable
12	COMP_25_EN	v2.5 solves dis-continuity of v2.0. v2.5 and v2.0 need to be enabled together. v2.0 can be enabled alone. 0: Disable 1: Enable
11	COMP_20_EN	v2.0 is only based on 32K to tick sys_timer. However, this architecture causes dis-continuity of sys_timer value. Some v8.0 CPUs need continuous values. HPT implements an option to eliminate this limitation in some v8.0 CPUs and all v8.2 CPUs. 0: Disable 1: Enable
10	COMP_15_EN	v1.5 is based on 13M and 32K to tick sys_timer. 0: Disable 1: Enable
3	TIE_0_EN	No need to enable it when v2.5 is enabled 0: Disable 1: Enable
2	CNT_32K_AS_EN	Enables 32K auto-switch function of system timer counter 0: Disable

Bit(s)	Name	Description
1	HDBG_EN	1: Enable Enables halt-on debug function of system timer counter 0: Disable
0	CNT_EN	1: Enable Enables system timer counter 0: Disable 1: Enable

10017004 **CNTSR** System counter status register 00000101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						clk_sel									DBGACK	
Type						RO									RO	
Reset						0									0	

Bit(s)	Name	Description
10	clk_sel	Selects system timer frequency 0: 26M 1: 32K
1	DBGACK	Timer is halted in debug mode. 0: Run 1: Halt

10017008 CNTCV_L System counter count value low 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTCV_L															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTCV_L															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTCV_L	Low part of 64-bit system timer counter

1001700C CNTCV_H System counter count value high 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTCV_H															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTCV_H															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTCV_H	High part of 64-bit system timer counter

10017010 CNTWACR System counter write access control register 0000FFF0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTWACR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTWACR															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
31:0	CNTWACR	Configures write access permission for each register Bit0: CNTCR Bit1: CNTSR Bit2: CNTCV_L Bit3: CNTCV_H Bit8: CNTFID0 Bit9: CNTFID1 Bit10: CNTFID2 Bit11: CNTFIDE Bit16: CNTTVAL0_CON & CNTTVAL0 Bit17: CNTTVAL1_CON & CNTTVAL1 Bit18: CNTTVAL2_CON & CNTTVAL2 Bit19: CNTTVAL3_CON & CNTTVAL3 Bit20: CNTTVAL4_CON & CNTTVAL4 Bit21: CNTTVAL5_CON & CNTTVAL5 Bit22: CNTTVAL6_CON & CNTTVAL6 Bit23: CNTTVAL7_CON & CNTTVAL7 Bit24: CNTTVAL8_CON & CNTTVAL8 Bit25: CNTTVAL9_CON & CNTTVAL9 0: Disable NS access 1: Enable NS access

10017014 CNTRACR System counter read access control register 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTWACR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTWACR															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	CNTWACR	Configures read access permission for each register Bit0: CNTCR Bit1: CNTSR Bit2: CNTCV_L Bit3: CNTCV_H Bit8: CNTFID0 Bit9: CNTFID1 Bit10: CNTFID2 Bit11: CNTFIDE Bit16: CNTTVAL0_CON & CNTTVAL0 Bit17: CNTTVAL1_CON & CNTTVAL1 Bit18: CNTTVAL2_CON & CNTTVAL2 Bit19: CNTTVAL3_CON & CNTTVAL3 Bit20: CNTTVAL4_CON & CNTTVAL4 Bit21: CNTTVAL5_CON & CNTTVAL5 Bit22: CNTTVAL6_CON & CNTTVAL6 Bit23: CNTTVAL7_CON & CNTTVAL7 Bit24: CNTTVAL8_CON & CNTTVAL8 Bit25: CNTTVAL9_CON & CNTTVAL9 0: Disable NS access 1: Enable NS access

10017018 CNTACR_LOCK System counter access control lock register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTACR_LOCK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTACR_LOCK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTACR_LOCK	Locks corresponding CNTRACR and CNTWACR bits This bit can program once only. 0: Unlock 1: Lock

1001701C CHICKEN Spare register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHICKEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHICKEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CHICKEN	Spare register

10017020 **CNTFID0** **System counter frequency table entry 0** **018CBA80**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTFID0															
Type	RO															
Reset	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTFID0															
Type	RO															
Reset	1	0	1	1	1	0	1	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTFID0	Frequency table entry 0

10017024 **CNTFID1** **System counter frequency table entry 1** **00C65D40**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTFID1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTFID1															
Type	RO															
Reset	0	1	0	1	1	1	0	1	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTFID1	Frequency table entry 1

10017028 **CNTFID2** **System counter frequency table entry 2** **00632EA0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTFID2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTFID2															
Type	RO															
Reset	0	0	1	0	1	1	1	0	1	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTFID2	Frequency table entry 2

1001702C CNTFIDE System counter frequency table entry end of line 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTFIDE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTFIDE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTFIDE	Frequency table entry - end of line

10017030 VERSION Version of system timer 00000209

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VERSION															
Type	RO															
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1

Bit(s)	Name	Description
15:0	VERSION	Version of system timer

10017034 CNTR_32K_L Low part of 64-bit 32K counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTR_32K_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTR_32K_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTR_32K_L	Low part of 64-bit 32K counter

10017038 **CNTR_32K_H** **High part of 64-bit 32K counter** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTR_32K_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTR_32K_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTR_32K_H	High part of 64-bit 32K counter

1001703C **CNT_RCON** **Latch-value read control register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNT_RCON															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT_RCON															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNT_RCON	0: Disable 1: Enable

10017040 CNTTVAL0_CON System counter timer 0 control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												IRQ0_STA			IRQ0_EN	CNTTVAL0_EN
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	IRQ0_STA	Enables system timer 0 interrupt status Write 0 to clear interrupt event. 0: Clear IRQ event 1: Assert IRQ
1	IRQ0_EN	Enables system timer 0 interrupt 0: Disable 1: Enable
0	CNTTVAL0_EN	Enables system timer 0 0: Disable 1: Enable

10017044 **CNTTVAL0** **System counter timer 0 value register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTTVAL0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTTVAL0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTTVAL0	System timer 0 down counter Write to set timeout value; read as 32-bit down counter.

10017048 **CNTTVAL1_CON** **System counter timer 1 control register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												IRQ1_STA			IRQ1_EN	CNTTVAL1_EN
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	IRQ1_STA	Enables system timer 1 interrupt status Write 0 to clear interrupt event. 0: Clear IRQ event 1: Assert IRQ
1	IRQ1_EN	Enable system timer 1 interrupt 0: Disable 1: Enable
0	CNTTVAL1_EN	Enables system timer 1 0: Disable 1: Enable

1001704C CTTVAL1 System counter timer 1 value register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CTTVAL1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTTVAL1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CTTVAL1	System timer 1 down counter Write to set timeout value; read as 32-bit down counter.

10017050 CTTVAL2_CON System counter timer 2 control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												IRQ2_STA			IRQ2_EN	CTTVAL2_EN
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	IRQ2_STA	Enables system timer 2 interrupt status Write 0 to clear interrupt event. 0: Clear IRQ event 1: Assert IRQ
1	IRQ2_EN	Enables system timer 2 interrupt 0: Disable 1: Enable
0	CTTVAL2_EN	Enables system timer 2 0: Disable 1: Enable

10017054 **CNTTVAL2** **System counter timer 2 value register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTTVAL2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTTVAL2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTTVAL2	System timer 3 down counter Write to set timeout value; read as 32-bit down counter.

10017058 **CNTTVAL3_CON** **System counter timer 3 control register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												IRQ3_STA			IRQ3_EN	CNTTVAL3_EN
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	IRQ3_STA	Enables system timer 3 interrupt status Write 0 to clear interrupt event. 0: Clear IRQ event 1: Assert IRQ
1	IRQ3_EN	Enables system timer 3 interrupt 0: Disable 1: Enable
0	CNTTVAL3_EN	Enables system timer 3 0: Disable 1: Enable

1001705C CTTVAL3 System counter timer 3 value register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CTTVAL3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTTVAL3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CTTVAL3	System timer 3 down counter Write to set timeout value; read as 32-bit down counter.

10017060 CTTVAL4_CON System counter timer 4 control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												IRQ4_STA			IRQ4_EN	CTTVAL4_EN
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	IRQ4_STA	Enables system timer 4 interrupt status Write 0 to clear interrupt event. 0: Clear IRQ event 1: Assert IRQ
1	IRQ4_EN	Enables system timer 4 interrupt 0: Disable 1: Enable
0	CTTVAL4_EN	Enables system timer 4 0: Disable 1: Enable

10017064 **CNTTVAL4** **System counter timer 4 value register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTTVAL4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTTVAL4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTTVAL4	System timer 4 down counter Write to set timeout value; read as 32-bit down counter.

10017068 **CNTTVAL5_CON** **System counter timer 5 control register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												IRQ5_STA			IRQ5_EN	CNTTVAL5_EN
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	IRQ5_STA	Enables system timer 5 interrupt status Write 0 to clear interrupt event. 0: Clear IRQ event 1: Assert IRQ
1	IRQ5_EN	Enables system timer 5 interrupt 0: Disable 1: Enable
0	CNTTVAL5_EN	Enables system timer 5 0: Disable 1: Enable

1001706C **CNTTVAL5** **System counter timer 5 value register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTTVAL5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTTVAL5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTTVAL5	System timer 5 down counter Write to set timeout value; read as 32-bit down counter.

10017070 **CNTTVAL6_CON** **System counter timer 6 control register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												IRQ6_STA			IRQ6_EN	CNTTVAL6_EN
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	IRQ6_STA	Enables system timer 6 interrupt status Write 0 to clear interrupt event. 0: Clear IRQ event 1: Assert IRQ
1	IRQ6_EN	Enables system timer 6 interrupt 0: Disable 1: Enable
0	CNTTVAL6_EN	Enables system timer 6 0: Disable 1: Enable

10017074 **CNTTVAL6** **System counter timer 6 value register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTTVAL6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTTVAL6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTTVAL6	System timer 6 down counter Write to set timeout value; read as 32-bit down counter.

10017078 **CNTTVAL7_CON** **System counter timer 7 control register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												IRQ7_STA			IRQ7_EN	CNTTVAL7_EN
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	IRQ7_STA	Enables system timer 7 interrupt status Write 0 to clear interrupt event. 0: Clear IRQ event 1: Assert IRQ
1	IRQ7_EN	Enables system timer 7 interrupt 0: Disable 1: Enable
0	CNTTVAL7_EN	Enables system timer 7 0: Disable 1: Enable

1001707C CTTVAL7 System counter timer 7 value register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CTTVAL7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CTTVAL7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CTTVAL7	System timer 8 down counter Write to set timeout value; read as 32-bit down counter.

10017080 DOMAIN_DIS Domain disable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WR_DOMAIN_DIS								RD_DOMAIN_DIS							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	WR_DOMAIN_DIS	Disables domain check for writing control registers of interrupts. Bit7~0 are for interrupt 7~0. 1: Disable domain check for write
7:0	RD_DOMAIN_DIS	Disables domain check for reading control registers of interrupts. Bit7~0 are for interrupt 7~0. 1: Disable domain check for read

10017084 DOMAIN_VAL Domain value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOMAIN_VAL_7				DOMAIN_VAL_6				DOMAIN_VAL_5				DOMAIN_VAL_4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOMAIN_VAL_3				DOMAIN_VAL_2				DOMAIN_VAL_1				DOMAIN_VAL_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	DOMAIN_VAL_7	Domain value of interrupt 7
27:24	DOMAIN_VAL_6	Domain value of interrupt 6
23:20	DOMAIN_VAL_5	Domain value of interrupt 5
19:16	DOMAIN_VAL_4	Domain value of interrupt 4
15:12	DOMAIN_VAL_3	Domain value of interrupt 3
11:8	DOMAIN_VAL_2	Domain value of interrupt 2
7:4	DOMAIN_VAL_1	Domain value of interrupt 1
3:0	DOMAIN_VAL_0	Domain value of interrupt 0

10017090 CNTRV_L_0 Low-32-bit timer value set 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_low_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_low_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_low_0	Low-32 binary values of timer. 8 sets are created for multicores.

10017094 CNTRV_H_0 High-32-bit timer value set 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_high_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_high_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_high_0	High-32 binary values of timer

10017098 CNTRV_L_1 Low-32-bit timer value set 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_low_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_low_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_low_1	Low-32 binary values of timer. 8 sets are created for multicores.

1001709C CNTRV_H_1 High-32-bit timer value set 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_high_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_high_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_high_1	High-32 binary values of timer

100170A0 **CNTRV_L_2** **Low-32-bit timer value set 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_low_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_low_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_low_2	Low-32 binary values of timer. 8 sets are created for multicores.

100170A4 **CNTRV_H_2** **High-32-bit timer value set 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_high_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_high_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_high_2	High-32 binary values of timer

100170A8 **CNTRV_L_3** **Low-32-bit timer value set 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_low_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_low_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_low_3	Low-32 binary values of timer. 8 sets are created for multicores.

100170AC CNTRV_H_3 High-32-bit timer value set 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_high_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_high_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_high_3	High-32 binary values of timer

100170B0 CNTRV_L_4 Low-32-bit timer value set 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_low_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_low_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_low_4	Low-32 binary values of timer. 8 sets are created for multicores.

100170B4 CNTRV_H_4 High-32-bit timer value set 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_high_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_high_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_high_4	High-32 binary values of timer

100170B8 **CNTRV_L_5** **Low-32-bit timer value set 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_low_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_low_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_low_5	Low-32 binary values of timer. 8 sets are created for multicores.

100170BC **CNTRV_H_5** **High-32-bit timer value set 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_high_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_high_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_high_5	High-32 binary values of timer

100170C0 **CNTRV_L_6** **Low-32-bit timer value set 6** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_low_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_low_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_low_6	Low-32 binary values of timer. 8 sets are created for multicores.

100170C4 CNTRV_H_6 High-32-bit timer value set 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_high_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_high_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_high_6	High-32 binary values of timer

100170C8 CNTRV_L_7 Low-32-bit timer value set 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_low_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_low_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_low_7	Low-32 binary values of timer. 8 sets are created for multicores.

100170CC CNTRV_H_7 High-32-bit timer value set 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_high_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_high_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_high_7	High-32 binary values of timer

3.8 LVTS (Low Voltage Thermal Sensing) Thermal Controller

3.8.1 Register Definition

Module name: ptp_therm_ctrl_AP Base address: (+0x1100_A000)

Address	Name	Width	Register Function
1100A000	<u>LVTSMONCTL0_0</u>	32	LVTS temperature monitoring control 0
1100A004	<u>LVTSMONCTL1_0</u>	32	LVTS temperature monitoring control 1
1100A008	<u>LVTSMONCTL2_0</u>	32	LVTS temperature monitoring control 2
1100A00C	<u>LVTSMONINT_0</u>	32	LVTS temperature monitoring interrupt enable
1100A010	<u>LVTSMONINTSTS_0</u>	32	LVTS temperature monitoring interrupt status
1100A014	<u>LVTSMONIDET0_0</u>	32	Sensing point 0 LVTS temperature monitoring detection
1100A018	<u>LVTSMONIDET1_0</u>	32	Sensing point 1 LVTS temperature monitoring detection
1100A01C	<u>LVTSMONIDET2_0</u>	32	Sensing point 2 LVTS temperature monitoring detection
1100A020	<u>LVTSMONIDET3_0</u>	32	Sensing point 3 LVTS temperature monitoring detection
1100A024	<u>LVTS_H2NTHRE_0</u>	32	LVTS temperature HOT2NORMAL threshold
1100A028	<u>LVTS_HTHRE_0</u>	32	LVTS temperature HOT threshold
1100A02C	<u>LVTS_CTHRE_0</u>	32	LVTS temperature COLD threshold
1100A030	<u>LVTSOFFSETH_0</u>	32	LVTS temperature HIGH OFFSET threshold
1100A034	<u>LVTSOFFSETL_0</u>	32	LVTS temperature LOW OFFSET threshold
1100A038	<u>LVTSMSRCTL0_0</u>	32	LVTS temperature measure control 0
1100A03C	<u>LVTSMSRCTL1_0</u>	32	LVTS temperature measure control 1
1100A040	<u>LVTSSEL_0</u>	32	LVTS sense point-3 number
1100A044	<u>LVTSDEVICETO_0</u>	32	LVTS temperature polling timeout
1100A048	<u>LVTS_CALSCALE_0</u>	32	ADC_VOLTAGEROUND
1100A04C	<u>LVTS_ID_0</u>	32	LVTS body ID valid
1100A050	<u>LVTS_CONFIG_0</u>	32	LVTS device take SCK only
1100A054	<u>LVTS_EDATA00_0</u>	32	ADC eFuse reference value for sensing point-0
1100A058	<u>LVTS_EDATA01_0</u>	32	ADC eFuse reference value for sensing point-1
1100A05C	<u>LVTS_EDATA02_0</u>	32	ADC eFuse reference value for sensing point-2
1100A060	<u>LVTS_EDATA03_0</u>	32	ADC eFuse reference value for sensing point-3
1100A090	<u>LVTSMSR0_0</u>	32	LVTS temperature measure reading 0
1100A094	<u>LVTSMSR1_0</u>	32	LVTS temperature measure reading 1
1100A098	<u>LVTSMSR2_0</u>	32	LVTS temperature measure reading 2
1100A09C	<u>LVTSMSR3_0</u>	32	LVTS temperature measure reading 3
1100A0A0	<u>LVTSIMMD0_0</u>	32	LVTS temperature IMMD measure reading 0
1100A0A4	<u>LVTSIMMD1_0</u>	32	LVTS temperature IMMD measure reading 1
1100A0A8	<u>LVTSIMMD2_0</u>	32	LVTS temperature IMMD measure reading 2
1100A0AC	<u>LVTSIMMD3_0</u>	32	LVTS temperature IMMD measure reading 3
1100A0B0	<u>LVTSRDATA0_0</u>	32	ADC direct read data for sensing point-0 or ANA_LVTS portal
1100A0B4	<u>LVTSRDATA1_0</u>	32	ADC direct read data for sensing point-1
1100A0B8	<u>LVTSRDATA2_0</u>	32	ADC direct read data for sensing point-2
1100A0BC	<u>LVTSRDATA3_0</u>	32	ADC direct read data for sensing point-3
1100A0C0	<u>LVTS_PROTCTL_0</u>	32	Thermal protection sensor selection
1100A0C4	<u>LVTS_PROTTA_0</u>	32	LVTS temperature protection stage 1

Address	Name	Width	Register Function
1100A0C8	<u>LVTSPROTTB_0</u>	32	LVTS temperature protection stage 2
1100A0CC	<u>LVTSPROTTTC_0</u>	32	LVTS temperature protection stage 3
1100A0E4	<u>LVTCLKEN_0</u>	32	LVTS clock enable
1100A0E8	<u>LVTSDBGSEL_0</u>	32	HWDBG selection
1100A0EC	<u>LVTSDBGSIG_0</u>	32	HWDBG signals
1100A0F0	<u>LVTSSPARE0_0</u>	32	Spare register for debug 0
1100A0F4	<u>LVTSSPARE1_0</u>	32	Spare register for debug 1
1100A0F8	<u>LVTSSPARE2_0</u>	32	Spare register for debug 2
1100A0FC	<u>LVTSSPARE3_0</u>	32	REV_ID
1100A100	<u>LVTSMONCTL0_1</u>	32	LVTS temperature monitoring control 0
1100A104	<u>LVTSMONCTL1_1</u>	32	LVTS temperature monitoring control 1
1100A108	<u>LVTSMONCTL2_1</u>	32	LVTS temperature monitoring control 2
1100A10C	<u>LVTSMONINT_1</u>	32	LVTS temperature monitoring interrupt enable
1100A110	<u>LVTSMONINTSTS_1</u>	32	LVTS temperature monitoring interrupt status
1100A114	<u>LVTSMONIDET0_1</u>	32	Sensing point 0 LVTS temperature monitoring detection
1100A118	<u>LVTSMONIDET1_1</u>	32	Sensing point 1 LVTS temperature monitoring detection
1100A11C	<u>LVTSMONIDET2_1</u>	32	Sensing point 2 LVTS temperature monitoring detection
1100A120	<u>LVTSMONIDET3_1</u>	32	Sensing point 3 LVTS temperature monitoring detection
1100A124	<u>LVTSH2NTHRE_1</u>	32	LVTS temperature HOT2NORMAL threshold
1100A128	<u>LVTSHTHRE_1</u>	32	LVTS temperature HOT threshold
1100A12C	<u>LVTSCTHRE_1</u>	32	LVTS temperature COLD threshold
1100A130	<u>LVTSOFFSETH_1</u>	32	LVTS temperature HIGH OFFSET threshold
1100A134	<u>LVTSOFFSETL_1</u>	32	LVTS temperature LOW OFFSET threshold
1100A138	<u>LVTSMRCTL0_1</u>	32	LVTS temperature measure control 0
1100A13C	<u>LVTSMRCTL1_1</u>	32	LVTS temperature measure control 1
1100A140	<u>LVTSTSEL_1</u>	32	LVTS sense point-3 number
1100A144	<u>LVTSEVICETO_1</u>	32	LVTS temperature polling timeout
1100A148	<u>LVTSCALSCALE_1</u>	32	LVTS CALSCALE 1
1100A14C	<u>LVTS_ID_1</u>	32	LVTS body ID 1
1100A150	<u>LVTS_CONFIG_1</u>	32	LVTS configuration 1
1100A154	<u>LVTSADATA00_1</u>	32	ADC eFuse reference value for sensing point-0
1100A158	<u>LVTSADATA01_1</u>	32	ADC eFuse reference value for sensing point-1
1100A15C	<u>LVTSADATA02_1</u>	32	ADC eFuse reference value for sensing point-2
1100A160	<u>LVTSADATA03_1</u>	32	ADC eFuse reference value for sensing point-3
1100A190	<u>LVTSMR0_1</u>	32	LVTS temperature measure reading 0
1100A194	<u>LVTSMR1_1</u>	32	LVTS temperature measure reading 1
1100A198	<u>LVTSMR2_1</u>	32	LVTS temperature measure reading 2
1100A19C	<u>LVTSMR3_1</u>	32	LVTS temperature measure reading 3
1100A1A0	<u>LVTSIMMD0_1</u>	32	LVTS temperature IMMD measure reading 0
1100A1A4	<u>LVTSIMMD1_1</u>	32	LVTS temperature IMMD measure reading 1
1100A1A8	<u>LVTSIMMD2_1</u>	32	LVTS temperature IMMD measure reading 2
1100A1AC	<u>LVTSIMMD3_1</u>	32	LVTS temperature IMMD measure reading 3
1100A1B0	<u>LVTSRDATA0_1</u>	32	ADC direct read data for sensing point-0 or ANA_LVTS portal
1100A1B4	<u>LVTSRDATA1_1</u>	32	ADC direct read data for sensing point-1
1100A1B8	<u>LVTSRDATA2_1</u>	32	ADC direct read data for sensing point-2

Address	Name	Width	Register Function
1100A1BC	<u>LVTSRDATA3_1</u>	32	ADC direct read data for sensing point-3
1100A1C0	<u>LVTSPROTCTL_1</u>	32	Thermal protection sensor selection
1100A1C4	<u>LVTSPROTTA_1</u>	32	LVTS temperature protection stage 1
1100A1C8	<u>LVTSPROTTB_1</u>	32	LVTS temperature protection stage 2
1100A1CC	<u>LVTSPROTTC_1</u>	32	LVTS temperature protection stage 3
1100A1E4	<u>LVTSCLKEN_1</u>	32	LVTS clock enable
1100A1E8	<u>LVTSDBGSEL_1</u>	32	HWDBG selection
1100A1EC	<u>LVTSDBGSIG_1</u>	32	HWDBG signals
1100A1F0	<u>LVTSSPARE0_1</u>	32	Spare register for debug 0
1100A1F4	<u>LVTSSPARE1_1</u>	32	Spare register for debug 1
1100A1F8	<u>LVTSSPARE2_1</u>	32	Spare register for debug 2
1100A1FC	<u>LVTSSPARE3_1</u>	32	REV_ID

1100A000 LVTSMONCTL0_0 LVTS temperature monitoring control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															PNP_TSSEL_DLY	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AUTORCK_MODE			SINGLE_SENSE	BROADCAST_SENSE					SENSE3_EN	SENSE2_EN	SENSE1_EN	SENSE0_EN
Type				RW			RW	RW					RW	RW	RW	RW
Reset				0			0	0					0	0	0	0

Bit(s)	Name	Description
17:16	PNP_TSSEL_DLY	State Machine inserts settle time when device TSSEL changes Delay time after TSSEL changes (counted in 26-MHz clock source): 00: 8us 01: 12us 10: 16us 11: 30us
12	AUTORCK_MODE	Applies multiplexor instead of divider for device AutoRCK operation 0: Device Legacy Mode (counting data converted with divider) 1: Device enables AutoRCK Mode (counting data converted with multiplexor)
9	SINGLE_SENSE	Enables periodic LVTS temperature measurement with single point access flow 0: Continue Mode 1: Single Mode
8	BROADCAST_SENSE	Enables periodic LVTS temperature measurement with broadcast address 0: LVTS access according to device ID 1: Force device ID to be broadcast ID (6'h0)
3	SENSE3_EN	Enables periodic LVTS temperature measurement on sense point 3 0: Disable 1: Enable
2	SENSE2_EN	Enables periodic LVTS temperature measurement on sense point 2 0: Disable 1: Enable
1	SENSE1_EN	Enables periodic LVTS temperature measurement on sense point 1

Bit(s)	Name	Description
		0: Disable
		1: Enable
0	SENSE0_EN	Enables periodic LVTS temperature measurement on sense point 0
		0: Disable
		1: Enable

1100A004 LVTSMONCTL1_0 LVTS temperature monitoring control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			GROUP_INTRVAL													HOTINT_SEL3
Type			RW													RW
Reset			0	0	0	0	0	0	0	0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HOTINT_T_SEL2	HOTINT_T_SEL1	HOTINT_T_SEL0				PERIOD_UNIT									
Type	RW	RW	RW				RW									
Reset	0	0	0				0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:20	GROUP_INTRVAL	Group access delay between all sensing points and all next sensing points (Interval unit in PERIOD_UNIT)
16	HOTINT_SEL3	Hot interrupt select for sensing point 3 0: All when normal to over hot threshold 1: Only the first time when normal to over hot threshold
15	HOTINT_SEL2	Hot interrupt select for sensing point 2 0: All when normal to over hot threshold 1: Only the first time when normal to over hot threshold
14	HOTINT_SEL1	Hot interrupt select for sensing point 1 0: All when normal to over hot threshold 1: Only the first time when normal to over hot threshold
13	HOTINT_SELO	Hot interrupt select for sensing point 0 0: All when normal to over hot threshold 1: Only the first time when normal to over hot threshold
9:0	PERIOD_UNIT	Calculating period unit in 26M clock with x256 scaling-up (i.e. period_unit * 26M_clock_period * 256)

1100A008 LVTSMONCTL2_0 LVTS temperature monitoring control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FILT_INTRVAL									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEN_INTRVAL									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	FILT_INTRVAL	Interval unit in PERIOD_UNIT (between samples within the same sensing point)
9:0	SEN_INTRVAL	Interval unit in PERIOD_UNIT (between sensing points)

1100A00C **LVTSMONINT_0** **LVTS temperature monitoring interrupt enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAGE3_INT_EN	STAGE2_INT_EN	STAGE1_INT_EN	FILTER_INT_EN_3	IMMD_INT_EN_3	NOHOTINTEN3	HOFSINTEN3	LOFSINTEN3	HINTEN3	CINTEN3	FILTER_INT_EN_2	FILTER_INT_EN_1	FILTER_INT_EN_0	IMMD_INT_EN_2	IMMD_INT_EN_1	IMMD_INT_EN_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIME_OUT_INT_EN	NOHOTINTEN2	HOFSINTEN2	LOFSINTEN2	HINTEN2	CINTEN2	NOHOTINTEN1	HOFSINTEN1	LOFSINTEN1	HINTEN1	CINTEN1	NOHOTINTEN0	HOFSINTEN0	LOFSINTEN0	HINTEN0	CINTEN0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STAGE3_INT_EN	Interrupt enable for thermal protection stage 3 0: Disable 1: Enable
30	STAGE2_INT_EN	Interrupt enable for thermal protection stage 2 0: Disable 1: Enable
29	STAGE1_INT_EN	Interrupt enable for thermal protection stage 1 0: Disable 1: Enable
28	FILTER_INT_EN_3	Filter sense interrupt enable for sensing point 3 0: Disable 1: Enable
27	IMMD_INT_EN_3	Immediate sense interrupt enable for sensing point 3 0: Disable 1: Enable
26	NOHOTINTEN3	Hot to normal interrupt enable for sensing point 3 0: Disable 1: Enable
25	HOFSINTEN3	High offset interrupt enable for sensing point 3 0: Disable 1: Enable
24	LOFSINTEN3	Low offset interrupt enable for sensing point 3 0: Disable

Bit(s)	Name	Description
		1: Enable
23	HINTEN3	Hot threshold interrupt enable for sensing point 3
		0: Disable
		1: Enable
22	CINTEN3	Cold threshold interrupt enable for sensing point 3
		0: Disable
		1: Enable
21	FILTER_INT_EN_2	Filter sense interrupt enable for sensing point 2
		0: Disable
		1: Enable
20	FILTER_INT_EN_1	Filter sense interrupt enable for sensing point 1
		0: Disable
		1: Enable
19	FILTER_INT_EN_0	Filter sense interrupt enable for sensing point 0
		0: Disable
		1: Enable
18	IMMD_INT_EN_2	Immediate sense interrupt enable for sensing point 2
		0: Disable
		1: Enable
17	IMMD_INT_EN_1	Immediate sense interrupt enable for sensing point 1
		0: Disable
		1: Enable
16	IMMD_INT_EN_0	Immediate sense interrupt enable for sensing point 0
		0: Disable
		1: Enable
15	TIME_OUT_INT_EN	Device access timeout interrupt enable
		0: Disable
		1: Enable
14	NOHOTINTEN2	Hot to normal interrupt enable for sensing point 2
		0: Disable
		1: Enable
13	HOFSENTEN2	High offset interrupt enable for sensing point 2

Bit(s)	Name	Description
		0: Disable
		1: Enable
12	LOFSINTEN2	Low offset interrupt enable for sensing point 2
		0: Disable
		1: Enable
11	HINTEN2	Hot threshold interrupt enable for sensing point 2
		0: Disable
		1: Enable
10	CINTEN2	Cold threshold interrupt enable for sensing point 2
		0: Disable
		1: Enable
9	NOHOTINTEN1	Hot to normal interrupt enable for sensing point 1
		0: Disable
		1: Enable
8	HOFSENTEN1	High offset interrupt enable for sensing point 1
		0: Disable
		1: Enable
7	LOFSINTEN1	Low offset interrupt enable for sensing point 1
		0: Disable
		1: Enable
6	HINTEN1	Hot threshold interrupt enable for sensing point 1
		0: Disable
		1: Enable
5	CINTEN1	Cold threshold interrupt enable for sensing point 1
		0: Disable
		1: Enable
4	NOHOTINTEN0	Hot to normal interrupt enable for sensing point 0
		0: Disable
		1: Enable
3	HOFSENTEN0	High offset interrupt enable for sensing point 0
		0: Disable
		1: Enable

Bit(s)	Name	Description
2	LOFSINTEN0	Low offset interrupt enable for sensing point 0 0: Disable 1: Enable
1	HINTEN0	Hot threshold interrupt enable for sensing point 0 0: Disable 1: Enable
0	CINTEN0	Cold threshold interrupt enable for sensing point 0 0: Disable 1: Enable

1100A010 **LVTSMONINTSTS_0** **LVTS temperature monitoring interrupt status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAGE3_INT_STAT	STAGE2_INT_STAT	STAGE1_INT_STAT	FILTER_INT_STAT_3	IMMD_INT_STAT_3	NOHOT_INTSTS_3	HOFSTSTS3	LOFSINTSTS3	HINTSTS3	LINTSTS3	FILTER_INT_STAT_2	FILTER_INT_STAT_1	FILTER_INT_STAT_0	IMMD_INT_STAT_2	IMMD_INT_STAT_1	IMMD_INT_STAT_0
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIMEOUT_INTSTS	NOHOT_INTSTS_2	HOFSTSTS2	LOFSINTSTS2	HINTSTS2	LINTSTS2	NOHOT_INTSTS_1	HOFSTSTS1	LOFSINTSTS1	HINTSTS1	LINTSTS1	NOHOT_INTSTS_0	HOFSTSTS0	LOFSINTSTS0	HINTSTS0	LINTSTS0
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STAGE3_INT_STAT	Interrupt status for thermal protection stage 3 0: Disable 1: Enable
30	STAGE2_INT_STAT	Interrupt status for thermal protection stage 2 0: Disable 1: Enable
29	STAGE1_INT_STAT	Interrupt status for thermal protection stage 1 0: Disable 1: Enable
28	FILTER_INT_STAT_3	Filter sense interrupt status for sensing point 3 0: Disable 1: Enable
27	IMMD_INT_STAT_3	Immediate sense interrupt status for sensing point 3 0: Disable 1: Enable
26	NOHOTINTSTS3	Hot to normal interrupt status for sensing point 3 0: No interrupt 1: Interrupt exists
25	HOFSTSTS3	High offset interrupt status for sensing point 3 0: No interrupt 1: Interrupt exists
24	LOFSINTSTS3	Low offset interrupt status for sensing point 3 0: No interrupt

Bit(s)	Name	Description
23	HINTSTS3	1: Interrupt exists Hot threshold interrupt status for sensing point 3 0: No interrupt
22	LINTSTS3	1: Interrupt exists Cold threshold interrupt status for sensing point 3 0: No interrupt
21	FILTER_INT_STAT_2	1: Interrupt exists Filter sense interrupt status for sensing point 2 0: Disable 1: Enable
20	FILTER_INT_STAT_1	Filter sense interrupt status for sensing point 1 0: Disable 1: Enable
19	FILTER_INT_STAT_0	Filter sense interrupt status for sensing point 0 0: Disable 1: Enable
18	IMMD_INT_STAT_2	Immediate sense interrupt status for sensing point 2 0: Disable 1: Enable
17	IMMD_INT_STAT_1	Immediate sense interrupt status for sensing point 1 0: Disable 1: Enable
16	IMMD_INT_STAT_0	Immediate sense interrupt status for sensing point 0 0: Disable 1: Enable
15	TIMEOUTINTSTS	Device access timeout interrupt status 0: No interrupt 1: Interrupt exists
14	NOHOTINTSTS2	High to normal offset interrupt status for sensing point 2 0: No interrupt 1: Interrupt exists
13	HOFINTSTS2	High offset interrupt status for sensing point 2

Bit(s)	Name	Description
		0: No interrupt 1: Interrupt exists
12	LOFSINTSTS2	Low offset interrupt status for sensing point 2 0: No interrupt 1: Interrupt exists
11	HINTSTS2	Hot threshold interrupt status for sensing point 2 0: No interrupt 1: Interrupt exists
10	LINTSTS2	Cold threshold interrupt status for sensing point 2 0: No interrupt 1: Interrupt exists
9	NOHOTINTSTS1	Hot to normal interrupt status for sensing point 1 0: No interrupt 1: Interrupt exists
8	HOFSTSTS1	High offset interrupt status for sensing point 1 0: No interrupt 1: Interrupt exists
7	LOFSINTSTS1	Low offset interrupt status for sensing point 1 0: No interrupt 1: Interrupt exists
6	HINTSTS1	Hot threshold interrupt status for sensing point 1 0: No interrupt 1: Interrupt exists
5	LINTSTS1	Cold threshold interrupt status for sensing point 1 0: No interrupt 1: Interrupt exists
4	NOHOTINTSTS0	Hot to normal interrupt status for sensing point 0 0: No interrupt 1: Interrupt exists
3	HOFSTSTS0	High offset interrupt status for sensing point 0 0: No interrupt 1: Interrupt exists

Bit(s)	Name	Description
2	LOFSINTST0	Low offset interrupt status for sensing point 0 0: No interrupt 1: Interrupt exists
1	HINTST0	Hot threshold interrupt status for sensing point 0 0: No interrupt 1: Interrupt exists
0	LINTST0	Cold threshold interrupt status for sensing point 0 0: No interrupt 1: Interrupt exists

1100A014 LVTSMONIDET0_0Sensing point 0 LVTS temperature monitoring
detection

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							NOHOTIMES		HOTIMES		LOTIMES		HTIMES		CTIMES	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:8	NOHOTIMES	How many times hot to normal interrupt occurs 00: 1 01: 2 10: 3 11: 4
7:6	HOTIMES	How many times high offset interrupt occurs 00: 1 01: 2 10: 3 11: 4
5:4	LOTIMES	How many times low offset interrupt occurs 00: 1 01: 2 10: 3 11: 4
3:2	HTIMES	How many times hot threshold interrupt occurs 00: 1 01: 2 10: 3 11: 4
1:0	CTIMES	How many times cold threshold interrupt occurs 00: 1 01: 2 10: 3

Bit(s)	Name	Description
		11: 4

1100A018

LVTSMONIDET1_0Sensing point 1 LVTS temperature monitoring
detection

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							NOHOTIMES		HOTIMES		LOTIMES		HTIMES		CTIMES	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:8	NOHOTIMES	How many times hot to normal interrupt occurs 00: 1 01: 2 10: 3 11: 4
7:6	HOTIMES	How many times high offset interrupt occurs 00: 1 01: 2 10: 3 11: 4
5:4	LOTIMES	How many times low offset interrupt occurs 00: 1 01: 2 10: 3 11: 4
3:2	HTIMES	How many times hot threshold interrupt occurs 00: 1 01: 2 10: 3 11: 4
1:0	CTIMES	How many times cold threshold interrupt occurs 00: 1 01: 2 10: 3

Bit(s)	Name	Description
		11: 4

1100A01C LVTSMONIDET2_0Sensing point 2 LVTS temperature monitoring
detection

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							NOHOTIMES		HOTIMES		LOTIMES		HTIMES		CTIMES	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:8	NOHOTIMES	How many times hot to normal interrupt occurs 00: 1 01: 2 10: 3 11: 4
7:6	HOTIMES	How many times high offset interrupt occurs 00: 1 01: 2 10: 3 11: 4
5:4	LOTIMES	How many times low offset interrupt occurs 00: 1 01: 2 10: 3 11: 4
3:2	HTIMES	How many times hot threshold interrupt occurs 00: 1 01: 2 10: 3 11: 4
1:0	CTIMES	How many times cold threshold interrupt occurs 00: 1 01: 2 10: 3

Bit(s)	Name	Description
		11: 4

1100A020

LVTSMONIDET3_0

Sensing point 3 LVTS temperature monitoring
detection

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							NOHOTIMES		HOTIMES		LOTIMES		HTIMES		CTIMES	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:8	NOHOTIMES	How many times hot to normal interrupt occurs 00: 1 01: 2 10: 3 11: 4
7:6	HOTIMES	How many times high offset interrupt occurs 00: 1 01: 2 10: 3 11: 4
5:4	LOTIMES	How many times low offset interrupt occurs 00: 1 01: 2 10: 3 11: 4
3:2	HTIMES	How many times hot threshold interrupt occurs 00: 1 01: 2 10: 3 11: 4
1:0	CTIMES	How many times cold threshold interrupt occurs 00: 1 01: 2 10: 3

Bit(s)	Name	Description
		11: 4

1100A024 LVTSH2NTHRE_0 LVTS temperature HOT2NORMAL threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HOT2NORMAL_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HOT2NORMAL_THRE	Threshold for hot to normal

1100A028 LVTSHTHRE_0 LVTS temperature HOT threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HOT_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HOT_THRE	Threshold for hot LVTS TEMPERATURE

1100A02C LVTSCTHRE_0 LVTS temperature COLD threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COLD_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	COLD_THRE	Threshold for cold LVTS TEMPERATURE

1100A030 **LVTSOFFSETH_0** LVTS temperature HIGH OFFSET threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SLOPE_OFFSET															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIGH_OFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	SLOPE_OFFSET	High/Low offset for monitoring with Adaptive reference data 0: Absolute offset detection, 1: Adaptive offset detection
15:0	HIGH_OFFSET	High offset for monitoring LVTS TEMPERATURE

1100A034 **LVTSOFFSETL_0** LVTS temperature LOW OFFSET threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LOW_OFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	LOW_OFFSET	Low offset for monitoring LVTS TEMPERATURE

1100A038 LVTSMRCTL0_0 LVTS temperature measure control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MSRCTL3			MSRCTL2			MSRCTL1			MSRCTL0		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:9	MSRCTL3	LVTS temperature measurement control for sensing point 3 000: One sample 001: Calculate the average of 2 samples 010: 4 samples. Drop max and min, and then calculate the average of 2 samples 011: 6 samples. Drop max and min, and then calculate the average of 4 samples 100: 10 samples. Drop max and min, and then calculate the average of 8 samples 101: 18 samples. Drop max and min, and then calculate the average of 16 samples Others: One sample
8:6	MSRCTL2	LVTS temperature measurement control for sensing point 2 000: One sample 001: Calculate the average of 2 samples 010: 4 samples. Drop max and min, and then calculate the average of 2 samples 011: 6 samples. Drop max and min, and then calculate the average of 4 samples 100: 10 samples. Drop max and min, and then calculate the average of 8 samples 101: 18 samples. Drop max and min, and then calculate the average of 16 samples Others: One sample
5:3	MSRCTL1	LVTS temperature measurement control for sensing point 1 000: One sample 001: Calculate the average of 2 samples 010: 4 samples. Drop max and min, and then calculate the average of 2 samples

Bit(s)	Name	Description
		011: 6 samples. Drop max and min, and then calculate the average of 4 samples
		100: 10 samples. Drop max and min, and then calculate the average of 8 samples
		101: 18 samples. Drop max and min, and then calculate the average of 16 samples
		Others: One sample
2:0	MSRCTLO	LVTS temperature measurement control for sensing point 0
		000: One sample
		001: Calculate the average of 2 samples
		010: 4 samples. Drop max and min, and then calculate the average of 2 samples
		011: 6 samples. Drop max and min, and then calculate the average of 4 samples
		100: 10 samples. Drop max and min, and then calculate the average of 8 samples
		101: 18 samples. Drop max and min, and then calculate the average of 16 samples
		Others: One sample

1100A03C LVTSMRCTL1_0 LVTS temperature measure control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						MSRSTS2	MSR3IMM	PAUSE3	MSRSTS1	MSR2IMM	MSR1IMM	MSR0IMM	PAUSE2	PAUSE1	PAUSE0	MSRSTS0
Type						RU	RW	RW	RU	RW	RW	RW	RW	RW	RW	RU
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	MSRSTS2	LVTS temperature measurement bus status[1] 000: Idle 001: Write transaction 010: Waiting for read after write 011: Disable continue fetching on device 100: Read transaction 101: Set device special register for voltage threshold 111: Set TSMCU number for fetch
9	MSR3IMM	Sense point 3 immediate measurement disregards LVTSMONCTL0 0: Disable 1: Enable
8	PAUSE3	Pauses periodic LVTS temperature measurement for sensing point 3 0: Release pause 1: Pause
7	MSRSTS1	LVTS temperature measurement bus status[1] 000: Idle 001: Write transaction 010: Waiting for read after write 011: Disable continue fetching on device 100: Read transaction 101: Set device special register for voltage threshold 111: Set TSMCU number for fetch
6	MSR2IMM	Sense point 2 immediate measurement disregards LVTSMONCTL0 0: Disable

Bit(s)	Name	Description
		1: Enable
5	MSR1IMM	Sense point 1 immediate measurement disregards LVTSMONCTL0 0: Disable
		1: Enable
4	MSR0IMM	Sense point 0 immediate measurement disregards LVTSMONCTL0 0: Disable
		1: Enable
3	PAUSE2	Pauses periodic LVTS temperature measurement for sensing point 2 0: Release pause
		1: Pause
2	PAUSE1	Pauses periodic LVTS temperature measurement for sensing point 1 0: Release pause
		1: Pause
1	PAUSE0	Pauses periodic LVTS temperature measurement for sensing point 0 0: Release pause
		1: Pause
0	MSRSTS0	LVTS temperature measurement bus status[0] 000: Idle 001: Write transaction 010: Waiting for read after write 011: Disable continue fetching on device 100: Read transaction 101: Set device special register for voltage threshold 111: Set TSMCU number for fetch

1100A040 LVTSTSEL_0 LVTS sense point-3 number 03020100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_SENSE3_PNP								ADC_SENSE2_PNP							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_SENSE1_PNP								ADC_SENSE0_PNP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	ADC_SENSE3_PNP	TSMCU sense point-3 selection number
23:16	ADC_SENSE2_PNP	TSMCU sense point-2 selection number
15:8	ADC_SENSE1_PNP	TSMCU sense point-1 selection number
7:0	ADC_SENSE0_PNP	TSMCU sense point-0 selection number

1100A044 LVTSDVICETO_0 LVTS temperature polling timeout FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_TIMEOUT															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_TIMEOUT															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	ADC_TIMEOUT	Timeout time for polling LVTS temperature voltage without getting any response. Unit is 26M.

1100A048 LVTSCALSCALE_0 ADCVOLTAGEROUND 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																ADC_VOLTAGE_ROUND
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ADC_VOLTAGE_PTP_SHIFT				ADC_VOLTAGE_DIV_SHIFT				ADC_VOLTAGE_SHIFT			
Type					RW				RW				RW			
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	ADC_VOLTAGE_ROUND	Rounding option for padding number on raw data normalization
11:8	ADC_VOLTAGE_PTP_SHIFT	Shifts report data to align PTP controller. Default is 0.
7:4	ADC_VOLTAGE_DIV_SHIFT	Right shifts normalized data for report. Default is 0.
3:0	ADC_VOLTAGE_SHIFT	Right shifts raw data before normalization. Default is 0.

1100A04C LVTS_ID_0 LVTS body ID valid 00000098

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BODY_ID_VALID		BODY_ID_NUMBER					
Type									RU		RU					
Reset									1		0	1	1	0	0	0

Bit(s)	Name	Description
7	BODY_ID_VALID	LVTS body ID valid. Check after device plug and play initial
5:0	BODY_ID_NUMBER	LVTS body ID number

1100A050 **LVTS_CONFIG_0** LVTS device take SCK only 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SCK_ONLY	CK26M_ACTIVE				BROADCAST_ID_UPDATE	DEVICE_SENSING_STATUS	DEVICE_ACCESS_START	DEVICE_ADDRESS						READ_32BIT_ACCESS	WRITE_ACCESS
Type	RW	RW				RW	RU	RU	RW						RW	RW
Reset	0	0				0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEVICE_REG_INDEX								DEVICE_REG_DATA							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	SCK_ONLY	Enables periodic LVTS temperature measurement with SCK active only (gated 26M clock signal) 0: Disable 1: Enable
30	CK26M_ACTIVE	Enables periodic LVTS temperature measurement with 26M always active 0: Disable 1: Enable
26	BROADCAST_ID_UPDATE	Updates device ID (LVTS_ID) with Broadcast access 0: Disable 1: Enable
25	DEVICE_SENSING_STATUS	Device is sensing (26M or SCK clock is active) 0: Devices are not sensing 1: Devices are sensing (Busy state)
24	DEVICE_ACCESS_START	Kick-off ASIF access command. Auto clear when access transaction finished 0: Device bus is idle 1: Device access is not complete (Busy state)
23:18	DEVICE_ADDRESS	Device ID for specific device access
17	READ_32BIT_ACCESS	32-bit Read access on devices
16	WRITE_ACCESS	Write access on devices
15:8	DEVICE_REG_INDEX	Register index of device access
7:0	DEVICE_REG_DATA	Register write data of device access

1100A054 LVTSEDA00 0 ADC eFuse reference value for sensing point-0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												LVTSEDA00				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LVTSEDA00															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	LVTSEDA00	eFuse value for sense point-0 normalization

1100A058 LVTSEDA01 0 ADC eFuse reference value for sensing point-1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												LVTSEDA01				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LVTSEDA01															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	LVTSEDA01	eFuse value for sense point-1 normalization

1100A05C LVTSEDA02 0 ADC eFuse reference value for sensing point-2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												LVTSEDA02				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LVTSEDA02															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	LVTSEDA02	eFuse value for sense point-2 normalization

1100A060 **LVTSEDA03_0** ADC eFuse reference value for sensing point-3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												LVTSEDA03				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LVTSEDA03															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	LVTSEDA03	eFuse value for sense point-3 normalization

1100A090 **LVTSMR0_0** LVTS temperature measure reading 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MSRVALID0
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSRREADING0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	MSRVALID0	LVTS new temperature measurement reading valid of sense point 0
15:0	MSRREADING0	LVTS temperature measurement reading of sense point 0

1100A094 **LVTSMSR1_0** **LVTS temperature measure reading 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MSRVA LID1
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSRREADING1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	MSRVALID1	LVTS new temperature measurement reading valid of sense point 1
15:0	MSRREADING1	LVTS temperature measurement reading of sense point 1

1100A098 **LVTSMSR2_0** **LVTS temperature measure reading 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MSRVA LID2
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSRREADING2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	MSRVALID2	LVTS new temperature measurement reading valid of sense point 2
15:0	MSRREADING2	LVTS temperature measurement reading of sense point 2

1100A09C LVTSMSR3_0 LVTS temperature measure reading 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MSRVA LID3
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSRREADING3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	MSRVALID3	LVTS new temperature measurement reading valid of sense point 3
15:0	MSRREADING3	LVTS temperature measurement reading of sense point 3

1100A0A0 LVTSIMMD0_0 LVTS temperature IMMD measure reading 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																IMMD MSRVA LID0
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMMDMSRREADING0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	IMMDMSRVALID0	Immediate LVTS new temperature measurement reading valid of sense point 0
15:0	IMMDMSRREADING0	Immediate LVTS temperature measurement reading of sense point 0

1100A0A4 **LVTSIMMD1_0** LVTS temperature IMMD measure reading 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																IMMD MSRVA LID1
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMMDMSRREADING1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	IMMDMSRVALID1	Immediate LVTS new temperature measurement reading valid of sense point 1
15:0	IMMDMSRREADING1	Immediate LVTS temperature measurement reading of sense point 1

1100A0A8 **LVTSIMMD2_0** LVTS temperature IMMD measure reading 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																IMMD MSRVA LID2
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMMDMSRREADING2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	IMMDMSRVALID2	Immediate LVTS new temperature measurement reading valid of sense point 2
15:0	IMMDMSRREADING2	Immediate LVTS temperature measurement reading of sense point 2

1100A0AC LVTSIMMD3_0 LVTS temperature IMMD measure reading 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																IMMDMSRVALID3
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMMDMSRREADING3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	IMMDMSRVALID3	Immediate LVTS new temperature measurement reading valid of sense point 3
15:0	IMMDMSRREADING3	Immediate LVTS temperature measurement reading of sense point 3

1100A0B0 LVTSRDATA0_0 ADC direct read data for sensing point-0 or ANA_LVTS portal 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LVTSRDATA0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LVTSRDATA0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LVTSRDATA0	Direct data from LVTS of sensing point-0

1100A0B4 LVTSRDATA1_0 ADC direct read data for sensing point-1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LVTSRDATA1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LVTSRDATA1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LVTSRDATA1	Direct data from LVTS of sensing point-1

1100A0B8 LVTSRDATA2_0 ADC direct read data for sensing point-2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LVTSRDATA2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LVTSRDATA2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LVTSRDATA2	Direct data from LVTS of sensing point-2

1100A0BC LVTSRDATA3_0 ADC direct read data for sensing point-3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LVTSRDATA3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LVTSRDATA3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LVTSRDATA3	Direct data from LVTS of sensing point-3

1100A0C0 LVTS_PROTCTL_0 Thermal protection sensor selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													PROTSELECTION		PROTSTRATEGY	
Type													RW		RW	
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PROTOFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:18	PROTSELECTION	Thermal protection selection 00: Sensing point 0 01: Sensing point 1 10: Sensing point 2 11: Sensing point 3
17:16	PROTSTRATEGY	Thermal protection strategy 00: Average of 4 sensing point 01: Maximum of 4 sensing point 10: Selected sensing point 11: Reserved
15:0	PROTOFFSET	Thermal protection LVTS temperature offset

1100A0C4 LVTS_PROTTA_0 LVTS temperature protection stage 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PROTSTAGE1THRES															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PROTSTAGE1THRES	Thermal protection stage 1 threshold

1100A0C8 LVTSPROTTB_0 LVTS temperature protection stage 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PROTSTAGE2THRES															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PROTSTAGE2THRES	Thermal protection stage 2 threshold

1100A0CC LVTSPROTTTC_0 LVTS temperature protection stage 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PROTSTAGE3THRES															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PROTSTAGE3THRES	Thermal protection stage 3 threshold

1100A0E4 **LVTSCLEN 0** LVTS clock enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																LVTSCLEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	LVTSCLEN	Enable LVTS Block Clock 0: Disable 1: Enable

1100A0E8 **LVTDBGSEL 0** HWDBG selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													HWDBGSEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	HWDBGSEL	Hardware Debug Signals selector 4'h1: Select debug signals of Device Master 4'h2: Select debug signals of Bus Controller 4'h3: Select debug signals of Monitor Controller 4'h4: Select debug signals of ADC Controller Other: 32'h0

1100A0EC LVTSDBSIG_0 HWDBG signals 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HWDBGSIG															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HWDBGSIG															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	HWDBGSIG	Hardware Debug Signals

1100A0F0 LVTSSPARE0_0 Spare register for debug 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE0	Debug register 0

1100A0F4 LVTSSPARE1_0 Spare register for debug 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE1	Debug register 1

1100A0F8 LVTSSPARE2_0 Spare register for debug 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE2	Debug register 2

1100A0FC LVTSSPARE3_0 REV_ID B0000009

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE3															
Type	RO															
Reset	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bit(s)	Name	Description
31:0	SPARE3	REV_ID

1100A100 LVTSMONCTL0_1 LVTS temperature monitoring control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															PNP_TSSEL_DLY	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AUTORCK_MODE			SINGLE_SENSE	BROADCAST_SENSE					SENSE3_EN	SENSE2_EN	SENSE1_EN	SENSE0_EN
Type				RW			RW	RW					RW	RW	RW	RW
Reset				0			0	0					0	0	0	0

Bit(s)	Name	Description
17:16	PNP_TSSEL_DLY	State Machine insert settle time for device TSSEL changed Delay time after TSSEL changed (counted in 26-MHz clock source): 00: 8us 01: 12us 10: 16us 11: 30us
12	AUTORCK_MODE	Applies multiplexor instead of divider for device AutoRCK operation 0: Device Legacy Mode (counting data covert with divider) 1: Device enable AutoRCK Mode (counting data covert with multiplexor)
9	SINGLE_SENSE	Enables periodic LVTS temperature measurement with single point access flow 0: Continue Mode 1: Single Mode
8	BROADCAST_SENSE	Enables periodic LVTS temperature measurement with broadcast address 0: LVTS access according to device ID 1: Force Device ID to be broadcast ID (6'h0)
3	SENSE3_EN	Enables periodic LVTS temperature measurement on sense point 3 0: Disable 1: Enable
2	SENSE2_EN	Enables periodic LVTS temperature measurement on sense point 2 0: Disable 1: Enable
1	SENSE1_EN	Enables periodic LVTS temperature measurement on sense point 1

Bit(s)	Name	Description
		0: Disable
		1: Enable
0	SENSE0_EN	Enables periodic LVTS temperature measurement on sense point 0
		0: Disable
		1: Enable

1100A104 LVTSMONCTL1_1 LVTS temperature monitoring control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			GROUP_INTRVAL													HOTINT_SEL3
Type			RW													RW
Reset			0	0	0	0	0	0	0	0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HOTINT_T_SEL2	HOTINT_T_SEL1	HOTINT_T_SELO				PERIOD_UNIT									
Type	RW	RW	RW				RW									
Reset	0	0	0				0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:20	GROUP_INTRVAL	Group access delay between all sensing points and all next sensing points (Interval unit in PERIOD_UNIT)
16	HOTINT_SEL3	Hot interrupt select for sensing point 3 0: All when normal to over hot threshold 1: Only the first time when normal to over hot threshold
15	HOTINT_SEL2	Hot interrupt select for sensing point 2 0: All when normal to over hot threshold 1: Only the first time when normal to over hot threshold
14	HOTINT_SEL1	Hot interrupt select for sensing point 1 0: All when normal to over hot threshold 1: Only the first time when normal to over hot threshold
13	HOTINT_SELO	Hot interrupt select for sensing point 0 0: All when normal to over hot threshold 1: Only the first time when normal to over hot threshold
9:0	PERIOD_UNIT	Calculating period unit in 26M clock with x256 scaling-up (i.e. period_unit * 26M_clock_period * 256)

1100A108 LVTSMONCTL2_1 LVTS temperature monitoring control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FILT_INTRVAL									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEN_INTRVAL									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	FILT_INTRVAL	Interval unit in PERIOD_UNIT (between samples within the same sensing point)
9:0	SEN_INTRVAL	Interval unit in PERIOD_UNIT (between sensing points)

1100A10C LVTSMONINT_1 LVTS temperature monitoring interrupt enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAGE3_INT_EN	STAGE2_INT_EN	STAGE1_INT_EN	FILTER_INT_EN_3	IMMD_INT_EN_3	NOHOTINTEN3	HOFSINTEN3	LOFSINTEN3	HINTEN3	CINTEN3	FILTER_INT_EN_2	FILTER_INT_EN_1	FILTER_INT_EN_0	IMMD_INT_EN_2	IMMD_INT_EN_1	IMMD_INT_EN_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIME_OUT_INT_EN	NOHOTINTEN2	HOFSINTEN2	LOFSINTEN2	HINTEN2	CINTEN2	NOHOTINTEN1	HOFSINTEN1	LOFSINTEN1	HINTEN1	CINTEN1	NOHOTINTEN0	HOFSINTEN0	LOFSINTEN0	HINTEN0	CINTEN0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STAGE3_INT_EN	Interrupt enable for thermal protection stage 3 0: Disable 1: Enable
30	STAGE2_INT_EN	Interrupt enable for thermal protection stage 2 0: Disable 1: Enable
29	STAGE1_INT_EN	Interrupt enable for thermal protection stage 1 0: Disable 1: Enable
28	FILTER_INT_EN_3	Filter sense interrupt enable for sensing point 3 0: Disable 1: Enable
27	IMMD_INT_EN_3	Immediate sense interrupt enable for sensing point 3 0: Disable 1: Enable
26	NOHOTINTEN3	Hot to normal interrupt enable for sensing point 3 0: Disable 1: Enable
25	HOFSINTEN3	High offset interrupt enable for sensing point 3 0: Disable 1: Enable
24	LOFSINTEN3	Low offset interrupt enable for sensing point 3 0: Disable

Bit(s)	Name	Description
		1: Enable
23	HINTEN3	Hot threshold interrupt enable for sensing point 3
		0: Disable
		1: Enable
22	CINTEN3	Cold threshold interrupt enable for sensing point 3
		0: Disable
		1: Enable
21	FILTER_INT_EN_2	Filter sense interrupt enable for sensing point 2
		0: Disable
		1: Enable
20	FILTER_INT_EN_1	Filter sense interrupt enable for sensing point 1
		0: Disable
		1: Enable
19	FILTER_INT_EN_0	Filter sense interrupt enable for sensing point 0
		0: Disable
		1: Enable
18	IMMD_INT_EN_2	Immediate sense interrupt enable for sensing point 2
		0: Disable
		1: Enable
17	IMMD_INT_EN_1	Immediate sense interrupt enable for sensing point 1
		0: Disable
		1: Enable
16	IMMD_INT_EN_0	Immediate sense interrupt enable for sensing point 0
		0: Disable
		1: Enable
15	TIME_OUT_INT_EN	Device access timeout interrupt enable
		0: Disable
		1: Enable
14	NOHOTINTEN2	Hot to normal interrupt enable for sensing point 2
		0: Disable
		1: Enable
13	HOFSENTEN2	High offset interrupt enable for sensing point 2

Bit(s)	Name	Description
		0: Disable
		1: Enable
12	LOFSINTEN2	Low offset interrupt enable for sensing point 2
		0: Disable
		1: Enable
11	HINTEN2	Hot threshold interrupt enable for sensing point 2
		0: Disable
		1: Enable
10	CINTEN2	Cold threshold interrupt enable for sensing point 2
		0: Disable
		1: Enable
9	NOHOTINTEN1	Hot to normal interrupt enable for sensing point 1
		0: Disable
		1: Enable
8	HOFSENTEN1	High offset interrupt enable for sensing point 1
		0: Disable
		1: Enable
7	LOFSINTEN1	Low offset interrupt enable for sensing point 1
		0: Disable
		1: Enable
6	HINTEN1	Hot threshold interrupt enable for sensing point 1
		0: Disable
		1: Enable
5	CINTEN1	Cold threshold interrupt enable for sensing point 1
		0: Disable
		1: Enable
4	NOHOTINTEN0	Hot to normal interrupt enable for sensing point 0
		0: Disable
		1: Enable
3	HOFSENTEN0	High offset interrupt enable for sensing point 0
		0: Disable
		1: Enable

Bit(s)	Name	Description
2	LOFSINTEN0	Low offset interrupt enable for sensing point 0 0: Disable 1: Enable
1	HINTEN0	Hot threshold interrupt enable for sensing point 0 0: Disable 1: Enable
0	CINTEN0	Cold threshold interrupt enable for sensing point 0 0: Disable 1: Enable

1100A110 LVTSMONINTSTS_1 LVTS temperature monitoring interrupt status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAGE3_INT_STAT	STAGE2_INT_STAT	STAGE1_INT_STAT	FILTER_INT_STAT_3	IMMD_INT_STAT_3	NOHOT_INTSTS_3	HOFSTSTS3	LOFSINTSTS3	HINTSTS3	LINTSTS3	FILTER_INT_STAT_2	FILTER_INT_STAT_1	FILTER_INT_STAT_0	IMMD_INT_STAT_2	IMMD_INT_STAT_1	IMMD_INT_STAT_0
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIMEOUT_INTSTS	NOHOT_INTSTS_2	HOFSTSTS2	LOFSINTSTS2	HINTSTS2	LINTSTS2	NOHOT_INTSTS_1	HOFSTSTS1	LOFSINTSTS1	HINTSTS1	LINTSTS1	NOHOT_INTSTS_0	HOFSTSTS0	LOFSINTSTS0	HINTSTS0	LINTSTS0
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STAGE3_INT_STAT	Interrupt status for thermal protection stage 3 0: Disable 1: Enable
30	STAGE2_INT_STAT	Interrupt status for thermal protection stage 2 0: Disable 1: Enable
29	STAGE1_INT_STAT	Interrupt status for thermal protection stage 1 0: Disable 1: Enable
28	FILTER_INT_STAT_3	Filter sense interrupt status for sensing point 3 0: Disable 1: Enable
27	IMMD_INT_STAT_3	Immediate sense interrupt status for sensing point 3 0: Disable 1: Enable
26	NOHOTINTSTS3	Hot to normal interrupt status for sensing point 3 0: No interrupt 1: Interrupt exists
25	HOFSTSTS3	High offset interrupt status for sensing point 3 0: No interrupt 1: Interrupt exists
24	LOFSINTSTS3	Low offset interrupt status for sensing point 3 0: No interrupt

Bit(s)	Name	Description
23	HINTSTS3	1: Interrupt exists Hot threshold interrupt status for sensing point 3 0: No interrupt
22	LINTSTS3	1: Interrupt exists Cold threshold interrupt status for sensing point 3 0: No interrupt
21	FILTER_INT_STAT_2	1: Interrupt exists Filter sense interrupt status for sensing point 2 0: Disable 1: Enable
20	FILTER_INT_STAT_1	Filter sense interrupt status for sensing point 1 0: Disable 1: Enable
19	FILTER_INT_STAT_0	Filter sense interrupt status for sensing point 0 0: Disable 1: Enable
18	IMMD_INT_STAT_2	Immediate sense interrupt status for sensing point 2 0: Disable 1: Enable
17	IMMD_INT_STAT_1	Immediate sense interrupt status for sensing point 1 0: Disable 1: Enable
16	IMMD_INT_STAT_0	Immediate sense interrupt status for sensing point 0 0: Disable 1: Enable
15	TIMEOUTINTSTS	Device access timeout interrupt status 0: No interrupt 1: Interrupt exists
14	NOHOTINTSTS2	High to normal offset interrupt status for sensing point 2 0: No interrupt 1: Interrupt exists
13	HOFINTSTS2	High offset interrupt status for sensing point 2

Bit(s)	Name	Description
		0: No interrupt 1: Interrupt exists
12	LOFSINTSTS2	Low offset interrupt status for sensing point 2 0: No interrupt 1: Interrupt exists
11	HINTSTS2	Hot threshold interrupt status for sensing point 2 0: No interrupt 1: Interrupt exists
10	LINTSTS2	Cold threshold interrupt status for sensing point 2 0: No interrupt 1: Interrupt exists
9	NOHOTINTSTS1	Hot to normal interrupt status for sensing point 1 0: No interrupt 1: Interrupt exists
8	HOFSINTSTS1	High offset interrupt status for sensing point 1 0: No interrupt 1: Interrupt exists
7	LOFSINTSTS1	Low offset interrupt status for sensing point 1 0: No interrupt 1: Interrupt exists
6	HINTSTS1	Hot threshold interrupt status for sensing point 1 0: No interrupt 1: Interrupt exists
5	LINTSTS1	Cold threshold interrupt status for sensing point 1 0: No interrupt 1: Interrupt exists
4	NOHOTINTSTS0	Hot to normal interrupt status for sensing point 0 0: No interrupt 1: Interrupt exists
3	HOFSINTSTS0	High offset interrupt status for sensing point 0 0: No interrupt 1: Interrupt exists

Bit(s)	Name	Description
2	LOFSINTST0	Low offset interrupt status for sensing point 0 0: No interrupt 1: Interrupt exists
1	HINTST0	Hot threshold interrupt status for sensing point 0 0: No interrupt 1: Interrupt exists
0	LINTST0	Cold threshold interrupt status for sensing point 0 0: No interrupt 1: Interrupt exists

1100A114

LVTSMONIDET0_1Sensing point 0 LVTS temperature monitoring
detection

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							NOHOTIMES		HOTIMES		LOTIMES		HTIMES		CTIMES	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:8	NOHOTIMES	How many times hot to normal interrupt occurs 00: 1 01: 2 10: 3 11: 4
7:6	HOTIMES	How many times high offset interrupt occurs 00: 1 01: 2 10: 3 11: 4
5:4	LOTIMES	How many times low offset interrupt occurs 00: 1 01: 2 10: 3 11: 4
3:2	HTIMES	How many times hot threshold interrupt occurs 00: 1 01: 2 10: 3 11: 4
1:0	CTIMES	How many times cold threshold interrupt occurs 00: 1 01: 2 10: 3

Bit(s)	Name	Description
		11: 4

1100A118 LVTSMONIDET1_1Sensing point 1 LVTS temperature monitoring
detection

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							NOHOTIMES		HOTIMES		LOTIMES		HTIMES		CTIMES	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:8	NOHOTIMES	How many times hot to normal interrupt occurs 00: 1 01: 2 10: 3 11: 4
7:6	HOTIMES	How many times high offset interrupt occurs 00: 1 01: 2 10: 3 11: 4
5:4	LOTIMES	How many times low offset interrupt occurs 00: 1 01: 2 10: 3 11: 4
3:2	HTIMES	How many times hot threshold interrupt occurs 00: 1 01: 2 10: 3 11: 4
1:0	CTIMES	How many times cold threshold interrupt occurs 00: 1 01: 2 10: 3

Bit(s)	Name	Description
		11: 4

1100A11C

LVTSMONIDET2_1

Sensing point 2 LVTS temperature monitoring
detection

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							NOHOTIMES		HOTIMES		LOTIMES		HTIMES		CTIMES	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:8	NOHOTIMES	How many times hot to normal interrupt occurs 00: 1 01: 2 10: 3 11: 4
7:6	HOTIMES	How many times high offset interrupt occurs 00: 1 01: 2 10: 3 11: 4
5:4	LOTIMES	How many times low offset interrupt occurs 00: 1 01: 2 10: 3 11: 4
3:2	HTIMES	How many times hot threshold interrupt occurs 00: 1 01: 2 10: 3 11: 4
1:0	CTIMES	How many times cold threshold interrupt occurs 00: 1 01: 2 10: 3

Bit(s)	Name	Description
		11: 4

1100A120

LVTSMONIDET3_1

Sensing point 3 LVTS temperature monitoring
detection

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							NOHOTIMES		HOTIMES		LOTIMES		HTIMES		CTIMES	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:8	NOHOTIMES	How many times hot to normal interrupt occurs 00: 1 01: 2 10: 3 11: 4
7:6	HOTIMES	How many times high offset interrupt occurs 00: 1 01: 2 10: 3 11: 4
5:4	LOTIMES	How many times low offset interrupt occurs 00: 1 01: 2 10: 3 11: 4
3:2	HTIMES	How many times hot threshold interrupt occurs 00: 1 01: 2 10: 3 11: 4
1:0	CTIMES	How many times cold threshold interrupt occurs 00: 1 01: 2 10: 3

Bit(s)	Name	Description
11: 4		

1100A124 **LVTSH2NTHRE_1** **LVTS temperature HOT2NORMAL threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HOT2NORMAL_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HOT2NORMAL_THRE	Threshold for hot to normal

1100A128 **LVTSHTHRE_1** **LVTS temperature HOT threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HOT_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HOT_THRE	Threshold for hot LVTS TEMPERATURE

1100A12C LVTSCTHRE_1 LVTS temperature COLD threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COLD_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	COLD_THRE	Threshold for cold LVTS TEMPERATURE

1100A130 LVTSOFFSETH_1 LVTS temperature HIGH OFFSET threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SLOPE_OFFSET															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HIGH_OFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	SLOPE_OFFSET	High/Low offset for monitoring with Adaptive reference data 0: Absolute offset detection, 1: Adaptive offset detection
15:0	HIGH_OFFSET	High offset for monitoring LVTS TEMPERATURE

1100A134 LVTSOFFSETL_1 LVTS temperature LOW OFFSET threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LOW_OFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	LOW_OFFSET	Low offset for monitoring LVTS TEMPERATURE

1100A138 LVTSMSRCTL0_1 LVTS temperature measure control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MSRCTL3			MSRCTL2			MSRCTL1			MSRCTL0		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:9	MSRCTL3	LVTS temperature measurement control for sensing point 3 000: One sample 001: Calculate the average of 2 samples 010: 4 samples. Drop max and min, and then calculate the average of 2 samples 011: 6 samples. Drop max and min, and then calculate the average of 4 samples 100: 10 samples. Drop max and min, and then calculate the average of 8 samples 101: 18 samples. Drop max and min, and then calculate the average of 16 samples Others: One sample
8:6	MSRCTL2	LVTS temperature measurement control for sensing point 2 000: One sample 001: Calculate the average of 2 samples 010: 4 samples. Drop max and min, and then calculate the average of 2 samples 011: 6 samples. Drop max and min, and then calculate the average of 4 samples 100: 10 samples. Drop max and min, and then calculate the average of 8 samples 101: 18 samples. Drop max and min, and then calculate the average of 16 samples Others: One sample
5:3	MSRCTL1	LVTS temperature measurement control for sensing point 1 000: One sample 001: Calculate the average of 2 samples 010: 4 samples. Drop max and min, and then calculate the average of 2 samples

Bit(s)	Name	Description
		011: 6 samples. Drop max and min, and then calculate the average of 4 samples
		100: 10 samples. Drop max and min, and then calculate the average of 8 samples
		101: 18 samples. Drop max and min, and then calculate the average of 16 samples
		Others: One sample
2:0	MSRCTLO	LVTS temperature measurement control for sensing point 0
		000: One sample
		001: Calculate the average of 2 samples
		010: 4 samples. Drop max and min, and then calculate the average of 2 samples
		011: 6 samples. Drop max and min, and then calculate the average of 4 samples
		100: 10 samples. Drop max and min, and then calculate the average of 8 samples
		101: 18 samples. Drop max and min, and then calculate the average of 16 samples
		Others: One sample

1100A13C LVTSMRCTL1_1 LVTS temperature measure control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						MSRSTS2	MSR3IMM	PAUSE3	MSRSTS1	MSR2IMM	MSR1IMM	MSR0IMM	PAUSE2	PAUSE1	PAUSE0	MSRSTS0
Type						RU	RW	RW	RU	RW	RW	RW	RW	RW	RW	RU
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	MSRSTS2	LVTS temperature measurement bus status[1] 000: Idle 001: Write transaction 010: Waiting for read after write 011: Disable continue fetching on device 100: Read transaction 101: Set device special register for voltage threshold 111: Set TSMCU number for fetch
9	MSR3IMM	Sense point 3 immediate measurement disregards LVTSMONCTL0 0: Disable 1: Enable
8	PAUSE3	Pauses periodic LVTS temperature measurement for sensing point 3 0: Release pause 1: Pause
7	MSRSTS1	LVTS temperature measurement bus status[1] 000: Idle 001: Write transaction 010: Waiting for read after write 011: Disable continue fetching on device 100: Read transaction 101: Set device special register for voltage threshold 111: Set TSMCU number for fetch
6	MSR2IMM	Sense point 2 immediate measurement disregards LVTSMONCTL0 0: Disable

Bit(s)	Name	Description
		1: Enable
5	MSR1IMM	Sense point 1 immediate measurement disregards LVTSMONCTL0 0: Disable
		1: Enable
4	MSR0IMM	Sense point 0 immediate measurement disregards LVTSMONCTL0 0: Disable
		1: Enable
3	PAUSE2	Pauses periodic LVTS temperature measurement for sensing point 2 0: Release pause
		1: Pause
2	PAUSE1	Pauses periodic LVTS temperature measurement for sensing point 1 0: Release pause
		1: Pause
1	PAUSE0	Pauses periodic LVTS temperature measurement for sensing point 0 0: Release pause
		1: Pause
0	MSRSTS0	LVTS temperature measurement bus status[0] 000: IDLE 001: Write transaction 010: Waiting for read after write 011: Disable continue fetching on device 100: Read transaction 101: Set device special register for voltage threshold 111: Set TSMCU number for fetch

1100A140 **LVTSTSEL_1** **LVTS sense point-3 number** **03020100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_SENSE3_PNP								ADC_SENSE2_PNP							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_SENSE1_PNP								ADC_SENSE0_PNP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	ADC_SENSE3_PNP	TSMCU sense point-3 selection Number
23:16	ADC_SENSE2_PNP	TSMCU sense point-2 selection number
15:8	ADC_SENSE1_PNP	TSMCU sense point-1 selection number
7:0	ADC_SENSE0_PNP	TSMCU sense point-0 selection Number

1100A144 **LVTSDDEVICETO_1** **LVTS temperature polling timeout** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_TIMEOUT															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_TIMEOUT															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	ADC_TIMEOUT	Timeout time for polling LVTS temperature voltage without getting any response. Unit is 26M.

1100A148 LVTS_CALSCALE_1 LVTS CALSCALE 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																ADC_VOLTAGE_ROUND
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ADC_VOLTAGE_PTP_SHIFT				ADC_VOLTAGE_DIV_SHIFT				ADC_VOLTAGE_SHIFT			
Type					RW				RW				RW			
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	ADC_VOLTAGE_ROUND	Rounding option for padding number on raw data normalization
11:8	ADC_VOLTAGE_PTP_SHIFT	Shifts report data to align PTP controller. Default is 0.
7:4	ADC_VOLTAGE_DIV_SHIFT	Right shifts normalized data for report. Default is 0.
3:0	ADC_VOLTAGE_SHIFT	Right shifts raw data before normalization. Default is 0.

1100A14C LVTS_ID_1 LVTS body ID 1 00000098

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BODY_ID_VALID		BODY_ID_NUMBER					
Type									RU		RU					
Reset									1		0	1	1	0	0	0

Bit(s)	Name	Description
7	BODY_ID_VALID	LVTS body ID valid. Check after device plug and play initial
5:0	BODY_ID_NUMBER	LVTS body ID number

1100A150 LVTS_CONFIG_1 LVTS configuration 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SCK_ONLY	CK26M_ACTIVE				BROADCAST_ID_UPDATE	DEVICE_SENSING_STATUS	DEVICE_ACCESS_START	DEVICE_ADDRESS						READ_32BIT_ACCESS	WRITE_ACCESS
Type	RW	RW				RW	RU	RU	RW						RW	RW
Reset	0	0				0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEVICE_REG_INDEX								DEVICE_REG_DATA							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	SCK_ONLY	Enables periodic LVTS temperature measurement with SCK active only (gated 26M clock signal) 0: Disable 1: Enable
30	CK26M_ACTIVE	Enables periodic LVTS temperature measurement with 26M always active 0: Disable 1: Enable
26	BROADCAST_ID_UPDATE	Updates Device ID (LVTS_ID) with Broadcast access 0: Disable 1: Enable
25	DEVICE_SENSING_STATUS	Device is sensing (26M or SCK is active) 0: Devices are not sensing 1: Devices are sensing (Busy state)
24	DEVICE_ACCESS_START	Kick-off ASIF access command. Auto clear when access transaction finishes 0: Device bus is idle 1: Device access is not complete (Busy state)
23:18	DEVICE_ADDRESS	Device ID for specific device access
17	READ_32BIT_ACCESS	32-bit Read access on devices
16	WRITE_ACCESS	Write access on devices
15:8	DEVICE_REG_INDEX	Register index of device access
7:0	DEVICE_REG_DATA	Register write data of device access

1100A154 **LVTSEDA00 1** **ADC eFuse reference value for sensing point-0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												LVTSEDA00				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LVTSEDA00															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	LVTSEDA00	eFuse value for sense point-0 normalization

1100A158 **LVTSEDA01 1** **ADC eFuse reference value for sensing point-1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												LVTSEDA01				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LVTSEDA01															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	LVTSEDA01	eFuse value for sense point-1 normalization

1100A15C **LVTSEDA02 1** **ADC eFuse reference value for sensing point-2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												LVTSEDA02				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LVTSEDA02															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	LVTSEDA02	eFuse value for sense point-2 normalization

1100A160 LVTSEDA03 1 ADC eFuse reference value for sensing point-3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												LVTSEDA03				
Type												RW				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LVTSEDA03															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:0	LVTSEDA03	eFuse value for sense point-3 normalization

1100A190 LVTSMR0 1 LVTS temperature measure reading 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MSRVALID0
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSRREADING0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	MSRVALID0	LVTS new temperature measurement reading valid of sense point 0
15:0	MSRREADING0	LVTS temperature measurement reading of sense point 0

1100A194 **LVTSMR1_1** **LVTS temperature measure reading 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MSRVA LID1
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSRREADING1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	MSRVALID1	LVTS new temperature measurement reading valid of sense point 1
15:0	MSRREADING1	LVTS temperature measurement reading of sense point 1

1100A198 **LVTSMR2_1** **LVTS temperature measure reading 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MSRVA LID2
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSRREADING2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	MSRVALID2	LVTS new temperature measurement reading valid of sense point 2
15:0	MSRREADING2	LVTS temperature measurement reading of sense point 2

1100A19C LVTSMR3_1 LVTS temperature measure reading 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MSRVA LID3
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSRREADING3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	MSRVALID3	LVTS new temperature measurement reading valid of sense point 3
15:0	MSRREADING3	LVTS temperature measurement reading of sense point 3

1100A1A0 LVTSIMMD0_1 LVTS temperature IMMD measure reading 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																IMMD MSRVA LID0
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMMDMSRREADING0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	IMMDMSRVALID0	Immediate LVTS new temperature measurement reading valid of sense point 0
15:0	IMMDMSRREADING0	Immediate LVTS temperature measurement reading of sense point 0

1100A1A4 LVTSIMMD1 1 LVTS temperature IMMD measure reading 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																IMMD MSRVA LID1
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMMDMSRREADING1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	IMMDMSRVALID1	Immediate LVTS new temperature measurement reading valid of sense point 1
15:0	IMMDMSRREADING1	Immediate LVTS temperature measurement reading of sense point 1

1100A1A8 LVTSIMMD2 1 LVTS temperature IMMD measure reading 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																IMMD MSRVA LID2
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMMDMSRREADING2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	IMMDMSRVALID2	Immediate LVTS new temperature measurement reading valid of sense point 2
15:0	IMMDMSRREADING2	Immediate LVTS temperature measurement reading of sense point 2

1100A1AC LVTSIMMD3_1 LVTS temperature IMMD measure reading 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																IMMDMSRVALID3
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMMDMSRREADING3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	IMMDMSRVALID3	Immediate LVTS new temperature measurement reading valid of sense point 3
15:0	IMMDMSRREADING3	Immediate LVTS temperature measurement reading of sense point 3

1100A1B0 LVTSRDATA0_1 ADC direct read data for sensing point-0 or ANA_LVTS portal 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LVTSRDATA0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LVTSRDATA0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LVTSRDATA0	Direct data from LVTS of device-0

1100A1B4 LVTSRDATA1_1 ADC direct read data for sensing point-1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LVTSRDATA1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LVTSRDATA1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LVTSRDATA1	Direct data from LVTS of device-1

1100A1B8 LVTSRDATA2_1 ADC direct read data for sensing point-2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LVTSRDATA2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LVTSRDATA2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LVTSRDATA2	Direct data from LVTS of device-2

1100A1BC LVTSRDATA3_1 ADC direct read data for sensing point-3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LVTSRDATA3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LVTSRDATA3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	LVTSRDATA3	Direct data from LVTS of device-3

1100A1C0 **LVTSPROTCTL 1** **Thermal protection sensor selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													PROTSELECTION		PROTSTRATEGY	
Type													RW		RW	
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PROTOFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:18	PROTSELECTION	Thermal protection selection 00: Sensing point 0 01: Sensing point 1 10: Sensing point 2 11: Sensing point 3
17:16	PROTSTRATEGY	Thermal protection strategy 00: Average of 4 sensing points 01: Maximum of 4 sensing points 10: Selected sensing point 11: Reserved
15:0	PROTOFFSET	Thermal protection LVTS temperature offset

1100A1C4 **LVTSPROTTA 1** **LVTS temperature protection stage 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PROTSTAGE1THRES															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PROTSTAGE1THRES	Thermal protection stage 1 threshold

1100A1C8 LVTSPROTTB_1 LVTS temperature protection stage 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PROTSTAGE2THRES															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PROTSTAGE2THRES	Thermal protection stage 2 threshold

1100A1CC LVTSPROTTTC_1 LVTS temperature protection stage 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PROTSTAGE3THRES															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PROTSTAGE3THRES	Thermal protection stage 3 threshold

1100A1E4 LVTSCLEN 1 LVTS clock enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																LVTSCKEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	LVTSCKEN	Enables LVTS block clock 0: Disable 1: Enable

1100A1E8 LWTSDBGSEL 1 HWDBG selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													HWDBGSEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	HWDBGSEL	Hardware debug signals selector 4'h1: Select debug signals of device master 4'h2: Select debug signals of bus controller 4'h3: Select debug signals of monitor controller 4'h4: Select debug signals of ADC controller Other: 32'h0

1100A1EC LVTSDBSIG 1 HWDBG signals 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HWDBGSIG															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HWDBGSIG															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	HWDBGSIG	Hardware Debug Signals

1100A1F0 LVTSSPARE0 1 Spare register for debug 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE0	Debug register 0

1100A1F4 LVTSSPARE1 1 Spare register for debug 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE1	Debug register 1

1100A1F8 LVTSSPARE2_1 Spare register for debug 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE2	Debug register 2

1100A1FC LVTSSPARE3_1 REV_ID B0000009

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE3															
Type	RO															
Reset	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bit(s)	Name	Description
31:0	SPARE3	REV_ID

3.9 Audio

3.9.1 Register Definition

Module name: AFE Base address: (+0x1121_0000)

Address	Name	Width	Register Function
11210000	<u>AUDIO_TOP_CON0</u>	32	Audio top control register 0
11210008	<u>AUDIO_TOP_CON2</u>	32	Audio top control register 2
11210010	<u>AUDIO_TOP_CON4</u>	32	Audio top control register 4
11210014	<u>AUDIO_ENGEN_CON0</u>	32	Audio engen control register 0
11210020	<u>AFE_SINEGEN_CON0</u>	32	AFE sine-wave gen configuration 0
11210024	<u>AFE_SINEGEN_CON1</u>	32	AFE sine-wave gen configuration 1
11210028	<u>AFE_SINEGEN_CON2</u>	32	AFE sine-wave gen configuration 2
1121002C	<u>AFE_SINEGEN_CON3</u>	32	AFE sine-wave gen configuration 3
11210038	<u>AFE_APLL2_TUNER_CFG</u>	32	AFE TUNER2 control register
1121003C	<u>AFE_APLL2_TUNER_MON0</u>	32	AFE TUNER2 monitor
1121006C	<u>AUDIO_TOP_IP_VERSION</u>	32	Audio top IP version
11210100	<u>AFE_IRQ_MCU_EN</u>	32	AFE IRQ MCU enable0 register
11210120	<u>AFE_IRQ_MCU_STATUS</u>	32	AFE IRQ MCU status register
11210124	<u>AFE_CUSTOM_IRQ_MCU_STATUS</u>	32	AFE CUSTOM IRQ MCU status register
11210128	<u>AFE_IRQ_MCU_CLR</u>	32	AFE IRQ clear register
1121012C	<u>AFE_IRQ_MCU_MISS_CLR</u>	32	AFE IRQ miss flag clear register
11210130	<u>AFE_CUSTOM_IRQ_MCU_CLR</u>	32	AFE CUSTOM IRQ clear register
11210134	<u>AFE_CUSTOM_IRQ_MCU_MISS_CLR</u>	32	AFE CUSTOM IRQ miss flag clear register
11210140	<u>AFE_IRQ0_MCU_CFG0</u>	32	AFE IRQ0 MCU control register 0
11210144	<u>AFE_IRQ0_MCU_CFG1</u>	32	AFE IRQ0 MCU control register 1
11210148	<u>AFE_IRQ1_MCU_CFG0</u>	32	AFE IRQ1 MCU control register 0
1121014C	<u>AFE_IRQ1_MCU_CFG1</u>	32	AFE IRQ1 MCU control register 1
11210150	<u>AFE_IRQ2_MCU_CFG0</u>	32	AFE IRQ2 MCU control register 0
11210154	<u>AFE_IRQ2_MCU_CFG1</u>	32	AFE IRQ2 MCU control register 1
11210308	<u>AFE_IRQ_MCU_MON2</u>	32	AFE IRQ MCU monitor register 2
11210310	<u>AFE_IRQ0_CNT_MON</u>	32	AFE IRQ0 count monitor register
11210314	<u>AFE_IRQ1_CNT_MON</u>	32	AFE IRQ1 count monitor register
11210318	<u>AFE_IRQ2_CNT_MON</u>	32	AFE IRQ2 count monitor register
112113F0	<u>ETDM_IN5_CON0</u>	32	ETDM_IN5 control register 0
112113F4	<u>ETDM_IN5_CON1</u>	32	ETDM_IN5 control register 1
112113F8	<u>ETDM_IN5_CON2</u>	32	ETDM_IN5 control register 2
112113FC	<u>ETDM_IN5_CON3</u>	32	ETDM_IN5 control register3
11211400	<u>ETDM_IN5_CON4</u>	32	ETDM_IN5 control register4
11211404	<u>ETDM_IN5_CON5</u>	32	ETDM_IN5 control register5
11211410	<u>ETDM_IN5_CON8</u>	32	ETDM_IN5 control register8
11211418	<u>ETDM_IN5_MON</u>	32	ETDM IN5 monitor
11211464	<u>ETDM_OUT5_MON</u>	32	ETDM OUT5 monitor
11211570	<u>ETDM_OUT5_CON0</u>	32	ETDM_OUT5 control register 0
11211574	<u>ETDM_OUT5_CON1</u>	32	ETDM_OUT5 control register 1
11211578	<u>ETDM_OUT5_CON2</u>	32	ETDM_OUT5 control register 2
1121157C	<u>ETDM_OUT5_CON3</u>	32	ETDM_OUT5 control register 3
11211580	<u>ETDM_OUT5_CON4</u>	32	ETDM_OUT5 control register 4

Address	Name	Width	Register Function
11211584	<u>ETDM_OUT5_CON5</u>	32	ETDM_OUT5 control register 5
11211590	<u>ETDM_OUT5_CON8</u>	32	ETDM_OUT5 control register 8
112115E0	<u>ETDM_4_7_COWORK_CON0</u>	32	ETDM_4_7 co-work control register 0
112115E4	<u>ETDM_4_7_COWORK_CON1</u>	32	ETDM_4_7 co-work control register 1
11213900	<u>AFE_CONN_MON_CFG</u>	32	AFE connection monitor control register
11213904	<u>AFE_CONN_MON0</u>	32	AFE connection monitor0
11213908	<u>AFE_CONN_MON1</u>	32	AFE connection monitor1
1121390C	<u>AFE_CONN_MON2</u>	32	AFE connection monitor2
11213910	<u>AFE_CONN_MON3</u>	32	AFE connection monitor3
11213914	<u>AFE_CONN_MON4</u>	32	AFE connection monitor4
11213918	<u>AFE_CONN_MON5</u>	32	AFE connection monitor5
11213920	<u>AFE_CONN_RS_0</u>	32	AFE connection right shift register
1121392C	<u>AFE_CONN_RS_3</u>	32	AFE connection right shift register
11213960	<u>AFE_CONN_16BIT_0</u>	32	AFE connection 16-bit register
1121396C	<u>AFE_CONN_16BIT_3</u>	32	AFE connection 16-bit register
11213980	<u>AFE_CONN_24BIT_0</u>	32	AFE connection 24-bit register
1121398C	<u>AFE_CONN_24BIT_3</u>	32	AFE connection 24-bit register
11213D80	<u>AFE_CBIP_CFG0</u>	32	AFE CBIP configuration
11213D98	<u>AFE_MEMIF_CON0</u>	32	MEMIF related configuration
11211B44	<u>AFE_CONN018_1</u>	32	AFE connection register 018_1
11211B50	<u>AFE_CONN018_4</u>	32	AFE connection register 018_4
11211B64	<u>AFE_CONN019_1</u>	32	AFE connection register 019_1
11211B70	<u>AFE_CONN019_4</u>	32	AFE connection register 019_4
11212884	<u>AFE_CONN124_1</u>	32	AFE connection register 124_1
11212890	<u>AFE_CONN124_4</u>	32	AFE connection register 124_4
112128A4	<u>AFE_CONN125_1</u>	32	AFE connection register 125_1
112128B0	<u>AFE_CONN125_4</u>	32	AFE connection register 125_4
11213E40	<u>AFE_DL0_BASE_MSB</u>	32	AFE DL0 base address register MSB
11213E44	<u>AFE_DL0_BASE</u>	32	AFE DL0 base address register
11213E48	<u>AFE_DL0_CUR_MSB</u>	32	AFE DL0 cursor register MSB
11213E4C	<u>AFE_DL0_CUR</u>	32	AFE DL0 cursor register
11213E50	<u>AFE_DL0_END_MSB</u>	32	AFE DL0 end address register MSB
11213E54	<u>AFE_DL0_END</u>	32	AFE DL0 end address register
11213E58	<u>AFE_DL0_RCH_MON</u>	32	AFE memory Interface monitor register RCH
11213E5C	<u>AFE_DL0_LCH_MON</u>	32	AFE memory Interface monitor register LCH
11213E60	<u>AFE_DL0_CON0</u>	32	AFE DL0 agent control register
11214220	<u>AFE_VUL0_BASE_MSB</u>	32	AFE VUL0 base address register MSB
11214224	<u>AFE_VUL0_BASE</u>	32	AFE VUL0 base address register
11214228	<u>AFE_VUL0_CUR_MSB</u>	32	AFE VUL0 cursor register MSB
1121422C	<u>AFE_VUL0_CUR</u>	32	AFE VUL0 cursor register
11214230	<u>AFE_VUL0_END_MSB</u>	32	AFE VUL0 end address register MSB
11214234	<u>AFE_VUL0_END</u>	32	AFE VUL0 end address register
11214238	<u>AFE_VUL0_CON0</u>	32	AFE VUL0 agent control register

11210000 AUDIO_TOP_CON0 Audio top control register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															pdn_m emif_h op_clk	pdn_m emif_i ntbus_ clk
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	pdn_memif_hop_clk	Powers down memif hopping clock 0: Do not power down memif hopping clk 1: Power down memif hopping clk
0	pdn_memif_intbus_clk	Powers down memif intbus clock 0: Do not power down memif intbus clk 1: Power down memif intbus clk

11210008 **AUDIO_TOP_CON2** Audio top control register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		pdn_etdm_out5							pdn_etdm_in5							
Type		RW							RW							
Reset		0							0							

Bit(s)	Name	Description
14	pdn_etdm_out5	Sets to 1 to gated eTDM OUT5 engine clock 0: Not clock-gated 1: Clock-gated
7	pdn_etdm_in5	Sets to 1 to gated eTDM IN5 engine clock 0: Not clock-gated 1: Clock-gated

11210010 AUDIO_TOP_CON4 Audio top control register 4 00003FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PDN_A PLL_TU NER2									CG_AP LL2_CK		CG_AU DIO_F2 6M_CK	CG_AU DIO_H OPPIN G_CK
Type				RW									RW		RW	RW
Reset				1									1		1	1

Bit(s)	Name	Description
12	PDN_APLL_TUNER2	PDN control for apll2 tuner. 0: Power on apll_tuner clock. 1: Power down apll_tuner clock.
3	CG_APLL2_CK	PDN control for 49M. 0: Power on apll2 49M clock. 1: Power down apll2 49M clock.
1	CG_AUDIO_F26M_CK	PDN control for F26M CLK. 0: Power on fix 26M clock. 1: Power down fix 26M clock.
0	CG_AUDIO_HOPPING_CK	PDN control for HOPPING CLK. 0: Power on hopping clock. 1: Power down hopping clock.

11210014 AUDIO_ENGEN_CON0 Audio engen control register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								AUDIO_F26M_EN_RST					AUDIO_APLL2_EN_ON			AUDIO_26M_EN_ON
Type								RW					RW			RW
Reset								0					0			0

Bit(s)	Name	Description
8	AUDIO_F26M_EN_RST	SW resets the enabling of the f26m en 0: Off 1: On
3	AUDIO_APLL2_EN_ON	Controls the enabling of the ap1l2 en 0: Off 1: On
0	AUDIO_26M_EN_ON	Controls the enabling of the 26m en 0: Off 1: On

11210020 AFE_SINEGEN_CON0 AFE sine-wave gen configuration 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						dac_en	tie_sw_ch2	tie_sw_ch1		amp_div_ch2						freq_div_ch2
Type						RW	RW	RW		RW						RW
Reset						0	0	0		0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	freq_div_ch2					amp_div_ch1						freq_div_ch1				
Type	RW					RW						RW				
Reset	0	0	0	0		0	0	0				0	0	0	0	0

Bit(s)	Name	Description
26	dac_en	Enables sinewave generator 0: Untie sigen 1: Tie sigen
25	tie_sw_ch2	Sinewave generator tie constant for ch2 0: Untie sigen 1: Tie sigen
24	tie_sw_ch1	Sinewave generator tie constant for ch1 0: Unmute sigen 1: Mute sigen
22:20	amp_div_ch2	Selects sinewave generator amplitude for ch2 0: Sinewave_out/128 1: Sinewave_out/64 2: Sinewave_out/32 3: Sinewave_out/16 4: Sinewave_out/8 5: Sinewave_out/4 6: Sinewave_out/2 7: Sinewave_out/1
16:12	freq_div_ch2	sinewave generator frequency selection for ch2 sampled by signal timing generator selection bit[23:20] (or bit[31:28]) for ch2 0: DC output 1: 64/1 samples/period 2: 64/2 samples/period 3: 64/3 samples/period 4: 64/4 samples/period

Bit(s)	Name	Description
		5: 64/5 samples/period
		6: 64/6 samples/period
		x: 64/x samples/period
		31: 64/31 samples/period
10:8	amp_div_ch1	Selects sinewave generator amplitude for ch1
		0: Sinewave_out/128
		1: Sinewave_out/64
		2: Sinewave_out/32
		3: Sinewave_out/16
		4: Sinewave_out/8
		5: Sinewave_out/4
		6: Sinewave_out/2
		7: Sinewave_out/1
4:0	freq_div_ch1	sinewave generator frequency selection for ch2 sampled by signal timing generator selection bit[23:20] (or bit[31:28]) for ch1
		0: DC output
		1: 64/1 samples/period
		2: 64/2 samples/period
		3: 64/3 samples/period
		4: 64/4 samples/period
		5: 64/5 samples/period
		6: 64/6 samples/period
		x: 64/x samples/period
		31: 64/31 samples/period

11210024 AFE_SINEGEN_CON1 AFE sine-wave gen configuration 1 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										sine_domain						sine_m ode
Type										RW						RW
Reset										0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sine_mode							INNER LOOP_ BACKI SEL	INNER_LOOP_BACK_MODE							
Type	RW							RW	RW							
Reset	0	0	0	0				0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
22:20	sine_domain	Enables sinewave generator domain selection 0: fix 26m domain 1: apll domain 2: spdif domain 3: hdmi domain 4: earc domain 5: linein domain 6: slave domain
16:12	sine_mode	Enables sinewave generator timing selection 0: 8k 1: 11.025k 2: 12k 4: 16k 5: 22.05k 6: 24k 8: 32k 9: 44.1k 10: 48k 13: 88.2k 14: 96k 17: 176.4k 18: 192k 21: 352.8k

Bit(s)	Name	Description
		22: 384k
8	INNER_LOOP_BACKI_SEL	sinewave generator inner loopback input output selection 0: Force interconn input port 1: Force interconn output port
7:0	INNER_LOOP_BACK_MODE	Loopback mode testing for audio_conn. 0: Sine generator ch1/ch2 force at interconn port 0/1 1: Sine generator ch1/ch2 force at interconn port 2/3 2: Sine generator ch1/ch2 force at interconn port 4/5 3: Sine generator ch1/ch2 force at interconn port 6/7 4: Sine generator ch1/ch2 force at interconn port 8/9 x: Sine generator ch1/ch2 force at interconn port 2x/2x-1

11210028 **AFE_SINEGEN_CON2** **AFE sine-wave gen configuration 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	tie_ch1_constent															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tie_ch1_constent															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	tie_ch1_constent	Constant value for tie ch1

1121002C **AFE_SINEGEN_CON3** **AFE sine-wave gen configuration 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	tie_ch2_constent															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tie_ch2_constent															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	tie_ch2_constent	Constant value for tie ch2

11210038 AFE_APLL2_TUNER_CFG AFE_TUNER2 control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	upper_bound								apll_div					xtal_en_128fs_sel	freq_tuner_en	
Type	RW								RW					RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
15:8	upper_bound	Upper bound setting for changing PCW
7:4	apll_div	Divider setting of apll 128fs
2:1	xtal_en_128fs_sel	Tuner clock sample rate select 2'b00: 32kHz*128 2'b01: 44.1kHz*128 2'b10: 48kHz*128 2'b11: 0
0	freq_tuner_en	apll tuner enable control 1: Enable apll tuner

1121003C AFE_APLL2_TUNER_MON0 AFE TUNER2 monitor 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	tuner_mon															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tuner_mon															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	tuner_mon	Frequency difference count value [9:0]: freq_diff [16]: lower_freq_sel [20]: trig_pcw_chg

1121006C AUDIO_TOP_IP_VERSION Audio top IP version 10000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	audio_top_ip_version															
Type	RO															
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	audio_top_ip_version															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	audio_top_ip_version	IP version

11210100 AFE_IRQ_MCU_EN AFE IRQ MCU enable0 register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_IRQ_MCU_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ_MCU_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	AFE_IRQ_MCU_EN	IRQ to MCU enable control 0: Disable IRQ 1: Enable IRQ

11210120 AFE_IRQ_MCU_STATUS AFE_IRQ MCU status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						IRQ26_MCU	IRQ25_MCU	IRQ24_MCU	IRQ23_MCU	IRQ22_MCU	IRQ21_MCU	IRQ20_MCU	IRQ19_MCU	IRQ18_MCU	IRQ17_MCU	IRQ16_MCU
Type						RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ15_MCU	IRQ14_MCU	IRQ13_MCU	IRQ12_MCU	IRQ11_MCU	IRQ10_MCU	IRQ9_MCU	IRQ8_MCU	IRQ7_MCU	IRQ6_MCU	IRQ5_MCU	IRQ4_MCU	IRQ3_MCU	IRQ2_MCU	IRQ1_MCU	IRQ0_MCU
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	IRQ26_MCU	This bit reads the status of IRQ26_MCU 0: No interrupt 1: IRQ26 interrupt
25	IRQ25_MCU	This bit reads the status of IRQ25_MCU 0: No interrupt 1: IRQ25 interrupt
24	IRQ24_MCU	This bit reads the status of IRQ24_MCU 0: No interrupt 1: IRQ24 interrupt
23	IRQ23_MCU	This bit reads the status of IRQ23_MCU 0: No interrupt 1: IRQ23 interrupt
22	IRQ22_MCU	This bit reads the status of IRQ22_MCU 0: No interrupt 1: IRQ22 interrupt
21	IRQ21_MCU	This bit reads the status of IRQ21_MCU 0: No interrupt 1: IRQ21 interrupt
20	IRQ20_MCU	This bit reads the status of IRQ20_MCU 0: No interrupt 1: IRQ20 interrupt
19	IRQ19_MCU	This bit reads the status of IRQ19_MCU 0: No interrupt 1: IRQ19 interrupt

Bit(s)	Name	Description
18	IRQ18_MCU	This bit reads the status of IRQ18_MCU 0: No interrupt 1: IRQ18 interrupt
17	IRQ17_MCU	This bit reads the status of IRQ17_MCU 0: No interrupt 1: IRQ17 interrupt
16	IRQ16_MCU	This bit reads the status of IRQ16_MCU 0: No interrupt 1: IRQ16 interrupt
15	IRQ15_MCU	This bit reads the status of IRQ15_MCU 0: No interrupt 1: IRQ15 interrupt
14	IRQ14_MCU	This bit reads the status of IRQ14_MCU 0: No interrupt 1: IRQ14 interrupt
13	IRQ13_MCU	This bit reads the status of IRQ13_MCU 0: No interrupt 1: IRQ13 interrupt
12	IRQ12_MCU	This bit reads the status of IRQ12_MCU 0: No interrupt 1: IRQ12 interrupt
11	IRQ11_MCU	This bit reads the status of IRQ11_MCU 0: No interrupt 1: IRQ11 interrupt
10	IRQ10_MCU	This bit reads the status of IRQ10_MCU 0: No interrupt 1: IRQ10 interrupt
9	IRQ9_MCU	This bit reads the status of IRQ9_MCU 0: No interrupt 1: IRQ9 interrupt
8	IRQ8_MCU	This bit reads the status of IRQ8_MCU 0: No interrupt

Bit(s)	Name	Description
		1: IRQ8 interrupt
7	IRQ7_MCU	This bit reads the status of IRQ7_MCU 0: No interrupt 1: IRQ7 interrupt
6	IRQ6_MCU	This bit reads the status of IRQ6_MCU 0: No interrupt 1: IRQ6 interrupt
5	IRQ5_MCU	This bit reads the status of IRQ5_MCU 0: No interrupt 1: IRQ5 interrupt
4	IRQ4_MCU	This bit reads the status of IRQ4_MCU 0: No interrupt 1: IRQ4 interrupt
3	IRQ3_MCU	This bit reads the status of IRQ3_MCU 0: No interrupt 1: IRQ3 interrupt
2	IRQ2_MCU	This bit reads the status of IRQ2_MCU 0: No interrupt 1: IRQ2 interrupt
1	IRQ1_MCU	This bit reads the status of IRQ1_MCU 0: No interrupt 1: IRQ1 interrupt
0	IRQ0_MCU	This bit reads the status of IRQ0_MCU 0: No interrupt 1: IRQ0 interrupt

11210124 **AFE_CUSTOM_IRQ_MCU_STA** AFE_CUSTOM_IRQ_MCU status register
TUS

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CUSTOM_IRQ21_MCU	CUSTOM_IRQ20_MCU	CUSTOM_IRQ19_MCU	CUSTOM_IRQ18_MCU	CUSTOM_IRQ17_MCU	CUSTOM_IRQ16_MCU
Type											RU	RU	RU	RU	RU	RU
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CUSTOM_IRQ7_MCU	CUSTOM_IRQ6_MCU	CUSTOM_IRQ5_MCU	CUSTOM_IRQ4_MCU	CUSTOM_IRQ3_MCU	CUSTOM_IRQ2_MCU	CUSTOM_IRQ1_MCU	CUSTOM_IRQ0_MCU
Type									RU	RU	RU	RU	RU	RU	RU	RU
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	CUSTOM_IRQ21_MCU	This bit reads the status of CUSTOM_IRQ21_MCU 0: No interrupt 1: CUSTOM_IRQ21 interrupt
20	CUSTOM_IRQ20_MCU	This bit reads the status of CUSTOM_IRQ20_MCU 0: No interrupt 1: CUSTOM_IRQ20 interrupt
19	CUSTOM_IRQ19_MCU	This bit reads the status of CUSTOM_IRQ19_MCU 0: No interrupt 1: CUSTOM_IRQ19 interrupt
18	CUSTOM_IRQ18_MCU	This bit reads the status of CUSTOM_IRQ18_MCU 0: No interrupt 1: CUSTOM_IRQ18 interrupt
17	CUSTOM_IRQ17_MCU	This bit reads the status of CUSTOM_IRQ17_MCU 0: No interrupt 1: CUSTOM_IRQ17 interrupt
16	CUSTOM_IRQ16_MCU	This bit reads the status of CUSTOM_IRQ16_MCU 0: No interrupt 1: CUSTOM_IRQ16 interrupt
7	CUSTOM_IRQ7_MCU	This bit reads the status of CUSTOM_IRQ7_MCU 0: No interrupt 1: CUSTOM_IRQ7 interrupt
6	CUSTOM_IRQ6_MCU	This bit reads the status of CUSTOM_IRQ6_MCU

Bit(s)	Name	Description
		0: No interrupt
		1: CUSTOM_IRQ6 interrupt
5	CUSTOM_IRQ5_MCU	This bit reads the status of CUSTOM_IRQ5_MCU
		0: No interrupt
		1: CUSTOM_IRQ5 interrupt
4	CUSTOM_IRQ4_MCU	This bit reads the status of CUSTOM_IRQ4_MCU
		0: No interrupt
		1: CUSTOM_IRQ4 interrupt
3	CUSTOM_IRQ3_MCU	This bit reads the status of CUSTOM_IRQ3_MCU
		0: No interrupt
		1: CUSTOM_IRQ3 interrupt
2	CUSTOM_IRQ2_MCU	This bit reads the status of CUSTOM_IRQ2_MCU
		0: No interrupt
		1: CUSTOM_IRQ2 interrupt
1	CUSTOM_IRQ1_MCU	This bit reads the status of CUSTOM_IRQ1_MCU
		0: No interrupt
		1: CUSTOM_IRQ1 interrupt
0	CUSTOM_IRQ0_MCU	This bit reads the status of CUSTOM_IRQ0_MCU
		0: No interrupt
		1: CUSTOM_IRQ0 interrupt

11210128 AFE_IRQ_MCU_CLR AFE_IRQ clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						IRQ26_MCU_CLR	IRQ25_MCU_CLR	IRQ24_MCU_CLR	IRQ23_MCU_CLR	IRQ22_MCU_CLR	IRQ21_MCU_CLR	IRQ20_MCU_CLR	IRQ19_MCU_CLR	IRQ18_MCU_CLR	IRQ17_MCU_CLR	IRQ16_MCU_CLR
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ15_MCU_CLR	IRQ14_MCU_CLR	IRQ13_MCU_CLR	IRQ12_MCU_CLR	IRQ11_MCU_CLR	IRQ10_MCU_CLR	IRQ9_MCU_CLR	IRQ8_MCU_CLR	IRQ7_MCU_CLR	IRQ6_MCU_CLR	IRQ5_MCU_CLR	IRQ4_MCU_CLR	IRQ3_MCU_CLR	IRQ2_MCU_CLR	IRQ1_MCU_CLR	IRQ0_MCU_CLR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	IRQ26_MCU_CLR	Clears the status of IRQ26_MCU, only work at write action. 0: No operation 1: Clear IRQ26 Interrupt
25	IRQ25_MCU_CLR	Clears the status of IRQ25_MCU. Only works at write action. 0: No operation 1: Clear IRQ25 Interrupt
24	IRQ24_MCU_CLR	Clears the status of IRQ24_MCU. Only works at write action. 0: No operation 1: Clear IRQ24 Interrupt
23	IRQ23_MCU_CLR	Clears the status of IRQ23_MCU. Only works at write action. 0: No operation 1: Clear IRQ23 Interrupt
22	IRQ22_MCU_CLR	Clears the status of IRQ22_MCU. Only works at write action. 0: No operation 1: Clear IRQ22 Interrupt
21	IRQ21_MCU_CLR	Clears the status of IRQ21_MCU. Only works at write action. 0: No operation 1: Clear IRQ21 Interrupt
20	IRQ20_MCU_CLR	Clears the status of IRQ20_MCU. Only works at write action. 0: No operation 1: Clear IRQ20 Interrupt
19	IRQ19_MCU_CLR	Clears the status of IRQ19_MCU. Only works at write action. 0: No operation

Bit(s)	Name	Description
		1: Clear IRQ19 Interrupt
18	IRQ18_MCU_CLR	Clears the status of IRQ18_MCU. Only works at write action. 0: No operation
		1: Clear IRQ18 Interrupt
17	IRQ17_MCU_CLR	Clears the status of IRQ17_MCU. Only works at write action. 0: No operation
		1: Clear IRQ17 Interrupt
16	IRQ16_MCU_CLR	Clears the status of IRQ16_MCU. Only works at write action. 0: No operation
		1: Clear IRQ16 Interrupt
15	IRQ15_MCU_CLR	Clears the status of IRQ15_MCU. Only works at write action. 0: No operation
		1: Clear IRQ15 Interrupt
14	IRQ14_MCU_CLR	Clears the status of IRQ14_MCU. Only works at write action. 0: No operation
		1: Clear IRQ14 Interrupt
13	IRQ13_MCU_CLR	Clears the status of IRQ13_MCU. Only works at write action. 0: No operation
		1: Clear IRQ13 Interrupt
12	IRQ12_MCU_CLR	Clears the status of IRQ12_MCU. Only works at write action. 0: No operation
		1: Clear IRQ12 Interrupt
11	IRQ11_MCU_CLR	Clears the status of IRQ11_MCU. Only works at write action. 0: No operation
		1: Clear IRQ11 Interrupt
10	IRQ10_MCU_CLR	Clears the status of IRQ10_MCU. Only works at write action. 0: No operation
		1: Clear IRQ10 Interrupt
9	IRQ9_MCU_CLR	Clears the status of IRQ9_MCU. Only works at write action. 0: No operation
		1: Clear IRQ9 Interrupt
8	IRQ8_MCU_CLR	Clears the status of IRQ8_MCU. Only works at write action.

Bit(s)	Name	Description
		0: No operation
		1: Clear IRQ8 Interrupt
7	IRQ7_MCU_CLR	Clears the status of IRQ7_MCU. Only works at write action.
		0: No operation
		1: Clear IRQ7 Interrupt
6	IRQ6_MCU_CLR	Clears the status of IRQ6_MCU. Only works at write action.
		0: No operation
		1: Clear IRQ6 interrupt
5	IRQ5_MCU_CLR	Clears the status of IRQ5_MCU. Only works at write action.
		0: No operation
		1: Clear IRQ5 interrupt
4	IRQ4_MCU_CLR	Clears the status of IRQ4_MCU. Only works at write action.
		0: No operation
		1: Clear IRQ4 interrupt
3	IRQ3_MCU_CLR	Clears the status of IRQ3_MCU. Only works at write action.
		0: No operation
		1: Clear IRQ3 interrupt
2	IRQ2_MCU_CLR	Clears the status of IRQ2_MCU. Only works at write action.
		0: No operation
		1: Clear IRQ2 interrupt
1	IRQ1_MCU_CLR	Clears the status of IRQ1_MCU. Only works at write action.
		0: No operation
		1: Clear IRQ1 interrupt
0	IRQ0_MCU_CLR	Clears the status of IRQ0_MCU. Only works at write action.
		0: No operation
		1: Clear IRQ0 interrupt

1121012C AFE_IRQ_MCU_MISS_CLR AFE IRQ miss flag clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						IRQ26_MCU_MISS_CNT_CLR	IRQ25_MCU_MISS_CNT_CLR	IRQ24_MCU_MISS_CNT_CLR	IRQ23_MCU_MISS_CNT_CLR	IRQ22_MCU_MISS_CNT_CLR	IRQ21_MCU_MISS_CNT_CLR	IRQ20_MCU_MISS_CNT_CLR	IRQ19_MCU_MISS_CNT_CLR	IRQ18_MCU_MISS_CNT_CLR	IRQ17_MCU_MISS_CNT_CLR	IRQ16_MCU_MISS_CNT_CLR
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ15_MCU_MISS_CNT_CLR	IRQ14_MCU_MISS_CNT_CLR	IRQ13_MCU_MISS_CNT_CLR	IRQ12_MCU_MISS_CNT_CLR	IRQ11_MCU_MISS_CNT_CLR	IRQ10_MCU_MISS_CNT_CLR	IRQ9_MCU_MISS_CNT_CLR	IRQ8_MCU_MISS_CNT_CLR	IRQ7_MCU_MISS_CNT_CLR	IRQ6_MCU_MISS_CNT_CLR	IRQ5_MCU_MISS_CNT_CLR	IRQ4_MCU_MISS_CNT_CLR	IRQ3_MCU_MISS_CNT_CLR	IRQ2_MCU_MISS_CNT_CLR	IRQ1_MCU_MISS_CNT_CLR	IRQ0_MCU_MISS_CNT_CLR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	IRQ26_MCU_MISS_CNT_CLR	Clears the status of IRQ26 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ26 miss count
25	IRQ25_MCU_MISS_CNT_CLR	Clears the status of IRQ25 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ25 miss count
24	IRQ24_MCU_MISS_CNT_CLR	Clears the status of IRQ24 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ24 miss count
23	IRQ23_MCU_MISS_CNT_CLR	Clears the status of IRQ23 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ23 miss count
22	IRQ22_MCU_MISS_CNT_CLR	Clears the status of IRQ22 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ22 miss count
21	IRQ21_MCU_MISS_CNT_CLR	Clears the status of IRQ21 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ21 miss count
20	IRQ20_MCU_MISS_CNT_CLR	Clears the status of IRQ20 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ20 miss count

Bit(s)	Name	Description
19	IRQ19_MCU_MISS_CNT_CLR	Clears the status of IRQ19 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ19 miss count
18	IRQ18_MCU_MISS_CNT_CLR	Clears the status of IRQ18 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ18 miss count
17	IRQ17_MCU_MISS_CNT_CLR	Clears the status of IRQ17 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ17 miss count
16	IRQ16_MCU_MISS_CNT_CLR	Clears the status of IRQ16 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ16 miss count
15	IRQ15_MCU_MISS_CNT_CLR	Clears the status of IRQ15 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ15 miss count
14	IRQ14_MCU_MISS_CNT_CLR	Clears the status of IRQ14 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ14 miss count
13	IRQ13_MCU_MISS_CNT_CLR	Clears the status of IRQ13 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ13 miss count
12	IRQ12_MCU_MISS_CNT_CLR	Clears the status of IRQ12 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ12 miss count
11	IRQ11_MCU_MISS_CNT_CLR	Clears the status of IRQ11 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ11 miss count
10	IRQ10_MCU_MISS_CNT_CLR	Clears the status of IRQ10 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ10 miss count
9	IRQ9_MCU_MISS_CNT_CLR	Clears the status of IRQ9 miss count flag. Only works at write action. 0: No operation

Bit(s)	Name	Description
		1: Clear IRQ9 miss count
8	IRQ8_MCU_MISS_CNT_CLR	Clears the status of IRQ8 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ8 miss count
7	IRQ7_MCU_MISS_CNT_CLR	Clears the status of IRQ7 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ7 miss count
6	IRQ6_MCU_MISS_CNT_CLR	Clears the status of IRQ6 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ6 miss count
5	IRQ5_MCU_MISS_CNT_CLR	Clears the status of IRQ5 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ5 miss count
4	IRQ4_MCU_MISS_CNT_CLR	Clears the status of IRQ4 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ4 miss count
3	IRQ3_MCU_MISS_CNT_CLR	Clears the status of IRQ3 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ3 miss count
2	IRQ2_MCU_MISS_CNT_CLR	Clears the status of IRQ2 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ2 miss count
1	IRQ1_MCU_MISS_CNT_CLR	Clears the status of IRQ1 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ1 miss count
0	IRQ0_MCU_MISS_CNT_CLR	Clears the status of IRQ0 miss count flag. Only works at write action. 0: No operation 1: Clear IRQ0 miss count

11210130 AFE_CUSTOM_IRQ_MCU_CLR AFE_CUSTOM_IRQ clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CUSTOM_IRQ21_MCU_CLR	CUSTOM_IRQ20_MCU_CLR	CUSTOM_IRQ19_MCU_CLR	CUSTOM_IRQ18_MCU_CLR	CUSTOM_IRQ17_MCU_CLR	CUSTOM_IRQ16_MCU_CLR
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CUSTOM_IRQ7_MCU_CLR	CUSTOM_IRQ6_MCU_CLR	CUSTOM_IRQ5_MCU_CLR	CUSTOM_IRQ4_MCU_CLR	CUSTOM_IRQ3_MCU_CLR	CUSTOM_IRQ2_MCU_CLR	CUSTOM_IRQ1_MCU_CLR	CUSTOM_IRQ0_MCU_CLR
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	CUSTOM_IRQ21_MCU_CLR	Clears the status of CUSTOM_IRQ21_MCU. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ21 Interrupt
20	CUSTOM_IRQ20_MCU_CLR	Clears the status of CUSTOM_IRQ20_MCU. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ20 Interrupt
19	CUSTOM_IRQ19_MCU_CLR	Clears the status of CUSTOM_IRQ19_MCU. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ19 Interrupt
18	CUSTOM_IRQ18_MCU_CLR	Clears the status of CUSTOM_IRQ18_MCU. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ18 Interrupt
17	CUSTOM_IRQ17_MCU_CLR	Clears the status of CUSTOM_IRQ17_MCU. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ17 Interrupt
16	CUSTOM_IRQ16_MCU_CLR	Clears the status of CUSTOM_IRQ16_MCU. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ16 Interrupt
7	CUSTOM_IRQ7_MCU_CLR	Clears the status of CUSTOM_IRQ7_MCU. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ7 Interrupt
6	CUSTOM_IRQ6_MCU_CLR	Clears the status of CUSTOM_IRQ6_MCU. Only works at write action.

Bit(s)	Name	Description
		0: No operation
		1: Clear CUSTOM_IRQ6 interrupt
5	CUSTOM_IRQ5_MCU_CLR	Clears the status of CUSTOM_IRQ5_MCU. Only works at write action.
		0: No operation
		1: Clear CUSTOM_IRQ5 interrupt
4	CUSTOM_IRQ4_MCU_CLR	Clears the status of CUSTOM_IRQ4_MCU. Only works at write action.
		0: No operation
		1: Clear CUSTOM_IRQ4 interrupt
3	CUSTOM_IRQ3_MCU_CLR	Clears the status of CUSTOM_IRQ3_MCU. Only works at write action.
		0: No operation
		1: Clear CUSTOM_IRQ3 interrupt
2	CUSTOM_IRQ2_MCU_CLR	Clears the status of CUSTOM_IRQ2_MCU. Only works at write action.
		0: No operation
		1: Clear CUSTOM_IRQ2 interrupt
1	CUSTOM_IRQ1_MCU_CLR	Clears the status of CUSTOM_IRQ1_MCU. Only works at write action.
		0: No operation
		1: Clear CUSTOM_IRQ1 interrupt
0	CUSTOM_IRQ0_MCU_CLR	Clears the status of CUSTOM_IRQ0_MCU. Only works at write action.
		0: No operation
		1: Clear CUSTOM_IRQ0 interrupt

11210134 AFE_CUSTOM_IRQ_MCU_MISAFE_CUSTOM_IRQ_miss_flag_clear_register

00000000

S_CLR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CUSTOM_IRQ21_MCU_MISS_CNT_CLR	CUSTOM_IRQ20_MCU_MISS_CNT_CLR	CUSTOM_IRQ19_MCU_MISS_CNT_CLR	CUSTOM_IRQ18_MCU_MISS_CNT_CLR	CUSTOM_IRQ17_MCU_MISS_CNT_CLR	CUSTOM_IRQ16_MCU_MISS_CNT_CLR
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CUSTOM_IRQ7_MCU_MISS_CNT_CLR	CUSTOM_IRQ6_MCU_MISS_CNT_CLR	CUSTOM_IRQ5_MCU_MISS_CNT_CLR	CUSTOM_IRQ4_MCU_MISS_CNT_CLR	CUSTOM_IRQ3_MCU_MISS_CNT_CLR	CUSTOM_IRQ2_MCU_MISS_CNT_CLR	CUSTOM_IRQ1_MCU_MISS_CNT_CLR	CUSTOM_IRQ0_MCU_MISS_CNT_CLR
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	CUSTOM_IRQ21_MCU_MISS_CNT_CLR	Clears the status of CUSTOM_IRQ21 miss count flag. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ21 miss count
20	CUSTOM_IRQ20_MCU_MISS_CNT_CLR	Clears the status of CUSTOM_IRQ20 miss count flag. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ20 miss count
19	CUSTOM_IRQ19_MCU_MISS_CNT_CLR	Clears the status of CUSTOM_IRQ19 miss count flag. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ19 miss count
18	CUSTOM_IRQ18_MCU_MISS_CNT_CLR	Clears the status of CUSTOM_IRQ18 miss count flag. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ18 miss count
17	CUSTOM_IRQ17_MCU_MISS_CNT_CLR	Clears the status of CUSTOM_IRQ17 miss count flag. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ17 miss count
16	CUSTOM_IRQ16_MCU_MISS_CNT_CLR	Clears the status of CUSTOM_IRQ16 miss count flag. Only works at write action.

Bit(s)	Name	Description
		0: No operation 1: Clear CUSTOM_IRQ16 miss count
7	CUSTOM_IRQ7_MCU_MISS_CNT_CLR	Clears the status of CUSTOM_IRQ7 miss count flag. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ7 miss count
6	CUSTOM_IRQ6_MCU_MISS_CNT_CLR	Clears the status of CUSTOM_IRQ6 miss count flag. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ6 miss count
5	CUSTOM_IRQ5_MCU_MISS_CNT_CLR	Clears the status of CUSTOM_IRQ5 miss count flag. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ5 miss count
4	CUSTOM_IRQ4_MCU_MISS_CNT_CLR	Clears the status of CUSTOM_IRQ4 miss count flag. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ4 miss count
3	CUSTOM_IRQ3_MCU_MISS_CNT_CLR	Clears the status of CUSTOM_IRQ3 miss count flag. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ3 miss count
2	CUSTOM_IRQ2_MCU_MISS_CNT_CLR	Clears the status of CUSTOM_IRQ2 miss count flag. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ2 miss count
1	CUSTOM_IRQ1_MCU_MISS_CNT_CLR	Clears the status of CUSTOM_IRQ1 miss count flag. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ1 miss count
0	CUSTOM_IRQ0_MCU_MISS_CNT_CLR	Clears the status of CUSTOM_IRQ0 miss count flag. Only works at write action. 0: No operation 1: Clear CUSTOM_IRQ0 miss count

11210140 AFE_IRQ0_MCU_CFG0 AFE_IRQ0_MCU control register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AFE_IRQ0_MCU_DOMAIN			AFE_IRQ0_MCU_FS								AFE_IRQ0_MCU_ON
Type					RW			RW								RW
Reset					0	0	0	0	0	0	0	0				0

Bit(s)	Name	Description
11:9	AFE_IRQ0_MCU_DOMAIN	Controls the IRQ0_MCU count domain 3'h0: hopping clk domain 3'h1: apll clk domain 3'h2: spdif clk domain 3'h3: hdmi clk domain 3'h4: earc clk domain 3'h5: linein clk domain 3'h6: slave clk domain
8:4	AFE_IRQ0_MCU_FS	Controls the IRQ0_MCU count unit 5'h00: 8k 5'h01: 11k 5'h02: 12k 5'h04: 16k 5'h05: 22k 5'h06: 24k 5'h08: 32k 5'h09: 44k 5'h0a: 48k 5'h0d: 88k 5'h0e: 96k 5'h11: 176k 5'h12: 192k 5'h15: 352k

Bit(s)	Name	Description
		5'h16: 384k
0	AFE_IRQ0_MCU_ON	Controls the enabling of IRQ0_MCU 0: Off 1: On

11210144 AFE_IRQ0_MCU_CFG1 AFE_IRQ0 MCU control register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AFE_IRQ0_MCU_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ0_MCU_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AFE_IRQ0_MCU_CNT	Sets up the counter value for IRQ0 according to AFE_IRQ0_MCU_FS. The IRQ0 counter in AFE will count down from AFE_IRQ0_MCU_CNT0 and set up IRQ0 while IRQ0 counter reaches 1.

11210148 AFE_IRQ1_MCU_CFG0 AFE_IRQ1_MCU control register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AFE_IRQ1_MCU_DOMAIN			AFE_IRQ1_MCU_FS								AFE_IRQ1_MCU_ON
Type					RW			RW								RW
Reset					0	0	0	0	0	0	0	0				0

Bit(s)	Name	Description
11:9	AFE_IRQ1_MCU_DOMAIN	Controls the IRQ1_MCU count domain 3'h0: hopping clk domain 3'h1: apll clk domain 3'h2: spdif clk domain 3'h3: hdmi clk domain 3'h4: earc clk domain 3'h5: linein clk domain 3'h7: slave clk domain
8:4	AFE_IRQ1_MCU_FS	Controls the IRQ1_MCU count unit 5'h00: 8k 5'h01: 11k 5'h02: 12k 5'h04: 16k 5'h05: 22k 5'h06: 24k 5'h08: 32k 5'h09: 44k 5'h0a: 48k 5'h0d: 88k 5'h0e: 96k 5'h11: 176k 5'h12: 192k 5'h15: 352k

Bit(s)	Name	Description
		5'h16: 385k
0	AFE_IRQ1_MCU_ON	Controls the enabling of IRQ1_MCU 0: Off 1: On

1121014C AFE_IRQ1_MCU_CFG1 AFE_IRQ1_MCU control register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AFE_IRQ1_MCU_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ1_MCU_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AFE_IRQ1_MCU_CNT	Sets up the counter value for IRQ1 according to AFE_IRQ1_MCU_FS. The IRQ1 counter in AFE will count down from AFE_IRQ1_MCU_CNT0 and set up IRQ1 while IRQ1 counter reaches 1.

11210150 AFE_IRQ2_MCU_CFG0 AFE_IRQ2_MCU control register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AFE_IRQ2_MCU_DOMAIN			AFE_IRQ2_MCU_FS								AFE_IRQ2_MCU_ON
Type					RW			RW								RW
Reset					0	0	0	0	0	0	0	0				0

Bit(s)	Name	Description
11:9	AFE_IRQ2_MCU_DOMAIN	Controls the IRQ2_MCU count domain 3'h0: hopping clk domain 3'h1: apll clk domain 3'h2: spdif clk domain 3'h3: hdmi clk domain 3'h4: earc clk domain 3'h5: linein clk domain 3'h8: slave clk domain
8:4	AFE_IRQ2_MCU_FS	Controls the IRQ2_MCU count unit 5'h00: 8k 5'h01: 11k 5'h02: 12k 5'h04: 16k 5'h05: 22k 5'h06: 24k 5'h08: 32k 5'h09: 44k 5'h0a: 48k 5'h0d: 88k 5'h0e: 96k 5'h11: 176k 5'h12: 192k 5'h15: 352k

Bit(s)	Name	Description
		5'h16: 386k
0	AFE_IRQ2_MCU_ON	Controls the enabling of IRQ2_MCU 0: Off 2: On

11210154 AFE_IRQ2_MCU_CFG1 AFE IRQ2 MCU control register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AFE_IRQ2_MCU_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ2_MCU_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AFE_IRQ2_MCU_CNT	Sets up the counter value for IRQ2 according to AFE_IRQ2_MCU_FS. The IRQ2 counter in AFE will count down from AFE_IRQ2_MCU_CNT0 and set up IRQ2 while IRQ2 counter reaches 1.

11210308 AFE_IRQ_MCU_MON2 AFE IRQ MCU monitor register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_CUSTOM_IRQ_MCU_MISS_FLAG_CLR_PHASE	AFE_CUSTOM_IRQ_MCU_CLR_PHASE	AFE_IRQ_MCU_MISS_FLAG_CLR_PHASE	AFE_IRQ_MCU_CLR_PHASE												
Type	RU	RU	RU	RU												
Reset	0	0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	AFE_CUSTOM_IRQ_MCU_MISS_FLAG_CLR_PHASE	Read only register to monitor if custom miss_flag_clr trigger
30	AFE_CUSTOM_IRQ_MCU_CLR_PHASE	Read only register to monitor if custom irq_clr trigger
29	AFE_IRQ_MCU_MISS_FLAG_CLR_PHASE	Read only register to monitor if miss_flag_clr trigger
28	AFE_IRQ_MCU_CLR_PHASE	Read only register to monitor if irq_clr trigger

11210310 AFE_IRQ0_CNT_MON AFE IRQ0 count monitor register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AFE_IRQ0_CNT_MON							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ0_CNT_MON															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AFE_IRQ0_CNT_MON	Monitors the counter value for IRQ0 according to AFE_IRQ0_MODE. The IRQ0 counter in AFE will count down from AFE_IRQ0_CNT.

11210314 AFE_IRQ1_CNT_MON AFE IRQ1 count monitor register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AFE_IRQ1_CNT_MON							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ1_CNT_MON															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AFE_IRQ1_CNT_MON	Monitors the counter value for IRQ1 according to AFE_IRQ1_MODE. The IRQ1 counter in AFE will count down from AFE_IRQ1_CNT.

11210318 AFE_IRQ2_CNT_MON AFE IRQ2 count monitor register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AFE_IRQ2_CNT_MON							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ2_CNT_MON															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AFE_IRQ2_CNT_MON	Monitors the counter value for IRQ2 according to AFE_IRQ2_MODE. The IRQ2 counter in AFE will count down from AFE_IRQ2_CNT.

112113F0 ETDM_IN5_CON0 ETDM_IN5 control register 0 009FF800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_val id_tog ether	reg_relatch_1x_en_do main_sel			reg_ch_num							reg_word_length				
Type	RW	RW			RW							RW				
Reset	0	0	0	0	0	0	0	0	1			1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_bit_length							reg_fmt			reg_sla ve_mo de	reg_sof t_rst	reg_lsb _first		reg_sy nc_mo de	reg_et dm_in _en
Type	RW							RW			RW	RW	RW		RW	RW
Reset	1	1	1	1	1			0	0	0	0	0	0		0	0

Bit(s)	Name	Description
31	reg_valid_together	When reg_bit_length < reg_word_length, the valid data are arranged together or not (If not: Enter 0) 0: Not together 1: Together
30:28	reg_relatch_1x_en_domain_sel	Selects clock domain of re-latch 1x_en. 3'h0: hopping clk domain 3'h1: apll clk domain 3'h2: spdif clk domain 3'h3: hdmi clk domain 3'h4: earc clk domain 3'h5: linein clk domain 3'h6: slave clk domain
27:23	reg_ch_num	The channel number of ETDM in. If ETDM in is multi-IP mode, the channel number should be set as 2ch. 0: 1 1: 2 n: n+1
20:16	reg_word_length	The BCK number in each channel. Reg_word_length should be large than reg_bit_length. 31: 32 bits 30: 31 bits N: N+1 bits 6: 7 bits Others: Not allowed.

Bit(s)	Name	Description
15:11	reg_bit_length	The valid bit number in each channel. 31: 32 bits 30: 31 bits N: N+1 bits 6: 7 bits Others: Not allowed.
8:6	reg_fmt	Sets the interface protocol of ETDM in. 0: I2S 1: LJ 2: RJ 3: EIAJ 4: DSPA/TDM_delay/PCMA(2CH) 5: DSPB/TDM/PCMB(2CH) 6: DSD Others: Not allowed.
5	reg_slave_mode	ETDM in is master mode or slave mode. 0: Master mode 1: Slave mode
4	reg_soft_rst	Reset ETDM in hardware when this bit is high. 0: Normal work 1: Reset valid
3	reg_lsb_first	The first serial data is LSB or MSB. 0: MSB first 1: LSB first
1	reg_sync_mode	Disables or enables sync mode of ETDM in. 0: Disable 1: Enable
0	reg_etdm_in_en	Disables or enables ETDM in. 0: Disable 1: Enable

112113F4 ETDM_IN5_CON1 ETDM_IN5 control register 1 800985CE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		reg_direct_input_master_bck														
Type		RW														
Reset		0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		reg_no_align_1x_en														
Type		RW														
Reset		0														

Bit(s)	Name	Description
30	reg_direct_input_master_bck	Master BCK generated mode. 0: Master BCK generated by 1x_en 1: Master BCK generated by divider
14	reg_no_align_1x_en	ETDM start time will align 1x_en timing or not. 0: Align with 1x_en 1: No align with 1x_en

112113F8 ETDM_IN5_CON2 ETDM_IN5 control register 2 0410C062

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_multi_ip_mode	reg_lrck_delay_bck_inv	reg_lrck_delay_0p5t_en	reg_sdata_delay_bck_inv	reg_sdata_delay_0p5t_en	reg_update_point_auto							reg_multi_ip_total_chnum			
Type	RW	RW	RW	RW	RW	RW							RW			
Reset	0	0	0	0	0	1							0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_multi_ip_total_chnum	reg_lrck_en_sel_auto		reg_clock_source_sel									reg_update_point			
Type	RW	RW		RW									RW			
Reset	1	1		0	0	0							0	0	0	1

Bit(s)	Name	Description
31	reg_multi_ip_mode	ETDM in use multi-IP mode or multi-ch mode. 0: One IP multi-ch mode (one sdata transfer 2ch or multi-ch) 1: Multi-IP 2ch mode (more than one sdata and every sdata transfer 2 channels)
30	reg_lrck_delay_bck_inv	Invert LRCK delay BCK or not. If invert, the LRCK will delay 0.5T BCK; else, the LRCK will delay 1T BCK. 0: No invert BCK 1: Invert BCK
29	reg_lrck_delay_0p5t_en	Whether to add 0.5T BCK delay for input LRCK. 0: Disable 1: Enable
28	reg_sdata_delay_bck_inv	Invert sdata delay BCK or not. If invert, the sdata will delay 0.5T BCK; else, the sdata will delay 1T BCK. 0: No invert BCK 1: Invert BCK
27	reg_sdata_delay_0p5t_en	Whether to add 0.5T BCK delay for input sdata. 0: Disable 1: Enable
26	reg_update_point_auto	Auto selects update point according to reg_fmt and reg_ch_num. 0: Disable 1: Enable
19:15	reg_multi_ip_total_chnum	The total channel number for multi-IP mode. 0: 1

Bit(s)	Name	Description
		1: 2
		n: n+1
14	reg_ck_en_sel_auto	Auto selects timing or not, only valid in engen timing mode. 0: Use manual mode to select timing (ETDM_IN_CON8[25:16]) 1: Auto select timing according to other settings
12:10	reg_clock_source_sel	Selects MCLK source for ETDM. 3'h0: hopping clk domain 3'h1: apll clk domain 3'h2: spdif clk domain 3'h3: hdmi clk domain 3'h4: earc clk domain 3'h5: linein clk domain 3'h6: slave clk domain
4:0	reg_update_point	When latch the data transfer to next stage. Only valid when reg_update_point_auto is 0 0: 0 1: 1 n: n

112113FC ETDM_IN5_CON3 ETDM_IN5 control register3 01F80000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_fs_timing_sel															
Type	RW															
Reset		0	0	0	0	0										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_disable_out															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	reg_fs_timing_sel	Sample rate select. 0: 8kHz 1: 12kHz 2: 16kHz 3: 24kHz 4: 32kHz 5: 48kHz 7: 96kHz 9: 192kHz 11: 384kHz 16: 11.025kHz 17: 22.05kHz 18: 44.1kHz 19: 88.2kHz 20: 176.4kHz 21: 352.8kHz Else: 0
15:0	reg_disable_out	Only valid when the ETDM direct connect to memif agent. Bit 0: Disable out setting for channel 0/1 Bit 1: Disable out setting for channel 2/3 Bit n: Disable out setting for channel 2n/2n+1

11211400	ETDM_IN5_CON4				ETDM_IN5 control register4								00000100			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		reg_wait_last_sample						reg_relatch_1x_en_sel					reg_master_ws_inv	reg_master_bck_inv	reg_slave_lrck_inv	reg_slave_bck_inv
Type		RW						RW					RW	RW	RW	RW
Reset		0						0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					reg_async_reset	reg_repack_word_length		reg_repack_automode								
Type					RW	RW		RW								
Reset					0	0	0	1								

Bit(s)	Name	Description
30	reg_wait_last_sample	Will wait last sample transfer done or not when ETDM off. 0: No wait last sample 1: Wait last sample
24:20	reg_relatch_1x_en_sel	Re-latch stage sample rate select. 0: 8kHz 1: 11.025kHz 2: 12kHz 4: 16kHz 5: 22.05kHz 6: 24kHz 8: 32kHz 9: 44kHz 10: 48kHz 13: 88.2kHz 14: 96kHz 17: 176.4kHz 18: 192kHz 21: 352.8kHz 22: 384kHz Else: 0
19	reg_master_ws_inv	This bit is only valid for output LRCK in master mode. 0: Not inverse

Bit(s)	Name	Description
		1: Inverse
18	reg_master_bck_inv	This bit is only valid for output BCK in master mode. 0: Not inverse 1: Inverse
17	reg_slave_lrck_inv	ETDM slave LRCK inverse or not. 0: Not inverse 1: Inverse
16	reg_slave_bck_inv	ETDM slave BCK inverse or not. 0: Not inverse 1: Inverse
11	reg_async_reset	Software asynchronous reset. 0: Normal work 1: Asynchronous reset valid
10:9	reg_repack_word_length	The valid bit length for data repacking. 0: 32 bits 1: 24 bits 2: 16 bits 3: 8 bits
8	reg_repack_auto_mode	Auto selects repack mode according to others setting or not. 0: Manual mode 1: Auto mode

11211404 ETDM_IN5_CON5 ETDM_IN5 control register5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_lr_swap															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_odd_flag_en															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	reg_lr_swap	Swaps right channel and left channel or not. Bit 0: For channel 0/1 Bit 1: For channel 2/3 Bit n: For channel 2n/2n+1
15:0	reg_odd_flag_en	Only supports multi-ch mode in the case of ETDM direct connects to memif agent. Bit 0: For channel 0/1 Bit 1: For channel 2/3 Bit n: For channel 2n/2n+1

11211410 ETDM_IN5_CON8 ETDM_IN5 control register8 40004000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		reg_afifo_thres hold					reg_ck_en_sel_manual									
Type		RW					RW									
Reset		1	0				0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_afifo_sw_reset	reg_afifo_reset_sel					reg_afifo_auto_reset_dis	reg_etdm_use_afifo	reg_afifo_clock_domain_sel			reg_afifo_mode				
Type	RW	RW					RW	RW	RW			RW				
Reset	0	1					0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:29	reg_afifo_threshold	INTERCONN can read data from AFIFO when AFIFO data number large than this setting, 1 and 2 are recommended value for this setting. 0: 0 1: 1 2: 2 3: 3
25:16	reg_ck_en_sel_manual	When reg_ck_en_sel_auto is 0, this setting will replace the value of {reg_ch_num, reg_word_length}.
15	reg_afifo_sw_reset	Software reset for AFIFO. 0: Normal 1: Software reset
14	reg_afifo_reset_sel	Will reset AFIFO when ETDM on/off. 0: Reset when ETDM on 1: Both reset when ETDM on and ETDM off
9	reg_afifo_auto_reset_dis	When ETDM in off, AFIFO will reset in auto reset mode. Otherwise, AFIFO can only reset by software reset and global hardware reset. 0: Auto reset 1: Disable auto reset
8	reg_etdm_use_afifo	ETDM use AFIFO or not. 0: Disable AFIFO 1: Enable AFIFO
7:5	reg_afifo_clock_domain_sel	Selects the clock domain of AFIFO read 1x_en. 3'h0: hopping clk domain 3'h1: apll clk domain

Bit(s)	Name	Description
		3'h2: spdif clk domain
		3'h3: hdmi clk domain
		3'h4: earc clk domain
		3'h5: linein clk domain
		3'h6: slave clk domain
4:0	reg_afifo_mode	Read sample rate of AFIFO.
		0: 8kHz
		1: 11.025kHz
		2: 12kHz
		4: 16kHz
		5: 22.05kHz
		6: 24kHz
		8: 32kHz
		9: 44kHz
		10: 48kHz
		13: 88.2kHz
		14: 96kHz
		17: 176.4kHz
		18: 192kHz
		21: 352.8kHz
		22: 384kHz
		Else: 0

11211418 ETDM_IN5_MON ETDM IN5 monitor 040500A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					wfull	rempty	etdm_2x_ck_en	etdm_1x_ck_en	sdata0	current_status		bit_point				
Type					RO	RO	RO	RO	RO	RO		RO				
Reset					0	1	0	0	0	0	0	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bit_ch_count					bit_count					ch_count					
Type	RO					RO					RO					
Reset	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bit(s)	Name	Description
27	wfull	Async FIFO write full
26	rempty	Async FIFO read empty
25	etdm_2x_ck_en	2X_CK_EN of ETDM in. ENGEN is enabled if this bit is variable.
24	etdm_1x_ck_en	1X_CK_EN of ETDM in. ENGEN is enabled if this bit is variable.
23	sdata0	Monitors ETDM input serial data
22:21	current_status	ETDM status. 00: ETDM is off 01: ETDM is off to on 10: ETDM is on to off 11: ETDM is on
20:16	bit_point	The bit point of ETDM.
15:10	bit_ch_count	The bit channel counter of ETDM.
9:5	bit_count	The bit counter of ETDM.
4:0	ch_count	The channel counter of ETDM.

11211464 ETDM_OUT5_MON ETDM OUT5 monitor 000600A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							etdm_2x_ck_en	etdm_1x_ck_en	sdata0	current_status		bit_point				
Type							RO	RO	RO	RO		RO				
Reset							0	0	0	0	0	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bit_ch_count						bit_count					ch_count				
Type	RO						RO					RO				
Reset	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bit(s)	Name	Description
25	etdm_2x_ck_en	2X_CK_EN of ETDM in. ENGEN is enabled if this bit is variable.
24	etdm_1x_ck_en	1X_CK_EN of ETDM in. ENGEN is enabled if this bit is variable.
23	sdata0	Monitor ETDM input serial data
22:21	current_status	ETDM status. 00: ETDM is off 01: ETDM is off to on 10: ETDM is on to off 11: ETDM is on
20:16	bit_point	The bit point of ETDM.
15:10	bit_ch_count	The bit channel counter of ETDM.
9:5	bit_count	The bit counter of ETDM.
4:0	ch_count	The channel counter of ETDM.

11211570 ETDM_OUT5_CON0 ETDM_OUT5 control register 0 009FF800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_val id_tog ether	reg_relatc h_domain_sel			reg_ch_num							reg_word_length				
Type	RW	RW			RW							RW				
Reset	0	0	0	0	0	0	0	0	1			1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_bit_length							reg_fmt				reg_sof t_rst	reg_lsb _first		reg_sy nc_mo de	reg_et dm_ou t_en
Type	RW							RW				RW	RW		RW	RW
Reset	1	1	1	1	1			0	0	0		0	0		0	0

Bit(s)	Name	Description
31	reg_valid_together	When reg_bit_length < reg_word_length, the valid data are arranged together or not (If not: Enter 0) 0: Not together 1: Together
30:28	reg_relatc h_domain_sel	Selects clock domain of re-latch 1x_en. 3'h0: hopping clk domain 3'h1: apll clk domain 3'h2: spdif clk domain 3'h3: hdmi clk domain 3'h4: earc clk domain 3'h5: linein clk domain 3'h6: slave clk domain
27:23	reg_ch_num	The channel number of ETDM out. If ETDM out is multi-IP mode, the channel number should be set as 2ch. 0: 1 1: 2 n: n+1
20:16	reg_word_length	The BCK number in each channel. Reg_word_length should be large than reg_bit_length. 31: 32 bits 30: 31 bits N: N+1 bits 6: 7 bits Others: Not allowed.

Bit(s)	Name	Description
15:11	reg_bit_length	The valid bit number in each channel. 31: 32 bits 30: 31 bits N: N+1 bits 6: 7 bits Others: Not allowed.
8:6	reg_fmt	Sets the interface protocol of ETDM out. 0: I2S 1: LJ 2: RJ 3: EIAJ 4: DSPA/TDM_delay/PCMA(2CH) 5: DSPB/TDM/PCMB(2CH) 6: DSD Others: Not allowed.
4	reg_soft_rst	Reset ETDM out hardware when this bit is high. 0: Normal work 1: Reset valid
3	reg_lsb_first	The first serial data is LSB or MSB. 0: MSB first 1: LSB first
1	reg_sync_mode	Disables or enables sync mode of ETDM out. 0: Disable 1: Enable
0	reg_etdm_out_en	Disables or enables ETDM out. 0: Disable 1: Enable

11211574 ETDM_OUT5_CON1 ETDM_OUT5 control register 1 200185CE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_16b_compact_mode	reg_direct_input_master_bck	reg_lrck_auto_mode	reg_lrck_width										reg_output_cr_en		
Type	RW	RW	RW	RW										RW		
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_lrck_reset	reg_no_align_1x_en														
Type	RW	RW														
Reset	1	0														

Bit(s)	Name	Description
31	reg_16b_compact_mode	One 32bit data contains LCH ([15:0]) and RCH ([31:16]) data, only valid when reg_bit_length is less than 16. 0: Disable 1: Enable
30	reg_direct_input_master_bck	Master BCK generated mode. 0: Master BCK generated by 1x_en 1: Master BCK generated by divider
29	reg_lrck_auto_mode	Auto set LRCK high level width according to others setting. 0: Manual mode 1: Auto mode
28:19	reg_lrck_width	Sets the high pulse width of LRCK in master mode. Only valid when reg_lrck_auto_mode is 0. 0: 1 BCK width 1: 2 BCK width n: n+1 BCK width
18	reg_output_cr_en	Output register data for debugging. 0: Output normal data 1: Output register data
15	reg_lrck_reset	Reset ETDM's counters to initial value when LRCK edge comes. 0: Disable 1: Enable
14	reg_no_align_1x_en	ETDM start time will align 1x_en timing or not. 0: Align with 1x_en

Bit(s)	Name	Description
		1: No align with 1x_en

11211578 ETDM_OUT5_CON2 ETDM_OUT5 control register 2 00F02406

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		reg_lrc k_delay_bck_inv	reg_lrc k_delay_0p5t_en	reg_sdata_delay_bck_inv	reg_sdata_delay_0p5t_en		reg_monitor_sel					reg_redundant_0			reg_off_cr_en	
Type		RW	RW	RW	RW		RW					RW			RW	
Reset		0	0	0	0		0	0				1			0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			reg_shift_auto	reg_sdata_shift		reg_mask_auto	reg_mask_num					reg_in2latch_time				
Type			RW	RW		RW	RW					RW				
Reset			1	0	0	1	0	0	0	0	0	0	0	1	1	0

Bit(s)	Name	Description
30	reg_lrc_k_delay_bck_inv	Inverts LRCK delay BCK or not. If invert, the LRCK will delay 0.5T BCK; else, the LRCK will delay 1T BCK. 0: No invert BCK 1: Invert BCK
29	reg_lrc_k_delay_0p5t_en	Whether to add 0.5T BCK delay for output LRCK. 0: Disable 1: Enable
28	reg_sdata_delay_bck_inv	Selects sdata delay BCK or not. If invert, the sdata will delay 0.5T BCK; else, the sdata will delay 1T BCK. 0: No invert BCK 1: Invert BCK
27	reg_sdata_delay_0p5t_en	Whether to add 0.5T BCK delay for output sdata. 0: Disable 1: Enable
25:24	reg_monitor_sel	Selects monitor. 1: Input LCH 0 2: Reorder output LCH 0 Else: ETDM counter
20	reg_redundant_0	If reg_bit_length < reg_word_length , the redundant bit will fill 0 or keep original input parallel data. 0: Keep original input parallel data 1: Fill 0
17	reg_off_cr_en	Output register data after ETDM out disable. 0: Disable

Bit(s)	Name	Description
		1: Enable
13	reg_shift_auto	When this bit is 0, sdata delay times decided by reg_sdata_shift, if this bit is 1 will auto select delay times according to reg_fmt. 0: Manual mode 1: Auto mode
12:11	reg_sdata_shift	Delay sdata before output. Only valid when reg_shift_auto is 0. 0: No delay 1: Delay 1T 2: Delay 2T 3: Delay 3T
10	reg_mask_auto	Auto selects mask number according to reg_bit_length and reg_word_length. 0: Disable 1: Enable
9:5	reg_mask_num	Mask bit number, only valid when reg_mask_auto is invalid. 0: 0 1: 1 n: n 30: 30 31: 31
4:0	reg_in2latch_time	When latched data transfer to next stage. 0: 0 1: 1 n: n

1121157C ETDM_OUT5_CON3 ETDM_OUT5 control register 3 76543210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_start_ch_pair7				reg_start_ch_pair6				reg_start_ch_pair5				reg_start_ch_pair4			
Type	RW				RW				RW				RW			
Reset	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_start_ch_pair3				reg_start_ch_pair2				reg_start_ch_pair1				reg_start_ch_pair0			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	reg_start_ch_pair7	Selects ETDM OUT channel 14/15 start channel. 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is $(2*n)/(2*n+1)$
27:24	reg_start_ch_pair6	Selects ETDM OUT channel 12/13 start channel. 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is $(2*n)/(2*n+1)$
23:20	reg_start_ch_pair5	Selects ETDM OUT channel 10/11 start channel. 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is $(2*n)/(2*n+1)$
19:16	reg_start_ch_pair4	Selects ETDM OUT channel 8/9 start channel. 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is $(2*n)/(2*n+1)$
15:12	reg_start_ch_pair3	Selects ETDM OUT channel 6/7 start channel.

Bit(s)	Name	Description
		0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is $(2*n)/(2*n+1)$
11:8	reg_start_ch_pair2	Selects ETDM OUT channel 4/5 start channel. 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is $(2*n)/(2*n+1)$
7:4	reg_start_ch_pair1	Selects ETDM OUT channel 2/3 start channel. 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is $(2*n)/(2*n+1)$
3:0	reg_start_ch_pair0	Selects ETDM OUT channel 0/1 start channel. 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is $(2*n)/(2*n+1)$

11211580 ETDM_OUT5_CON4 ETDM_OUT5 control register 4 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_always_open_1x_en	reg_wait_last_sample		reg_relatck_en_sel					reg_ck_en_sel_manual							
Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_ck_en_sel_manual				reg_async_reset	reg_ck_en_sel_auto		reg_clock_source_sel				reg_fs_timing_sel				
Type	RW				RW	RW		RW				RW				
Reset	0	0			0	1		0	0	0		0	0	0	0	0

Bit(s)	Name	Description
31	reg_always_open_1x_en	No matter ETDM is enabled or not, ENGEN will always send 1x_en to ETDM to generate master BCK. 0: Disable 1: Enable
30	reg_wait_last_sample	Will wait last sample transfer done or not when ETDM off. 0: Do not wait for last sample 1: Wait for last sample
28:24	reg_relatck_en_sel	Selects sample rate for ETDM out re-latch function. Domain: slave clk domain 0: connsys_i2s_ext_1x_en 1: afe_pcm0_ext_1x_en 2: afe_pcm1_ext_1x_en 4: eTDM IN0 a1sys lrck pulse 5: eTDM IN1 a1sys lrck pulse 6: eTDM IN2 a1sys lrck pulse 7: eTDM IN3 a1sys lrck pulse 8: eTDM IN4 a1sys lrck pulse 9: eTDM IN5 a1sys lrck pulse 10: eTDM IN6 a1sys lrck pulse 11: eTDM IN7 a1sys lrck pulse 12: eTDM OUT0 a1sys lrck pulse 13: eTDM OUT1 a1sys lrck pulse 14: eTDM OUT2 a1sys lrck pulse

Bit(s)	Name	Description
		15: eTDM OUT3 a1sys lrck pulse
		16: eTDM OUT4 a1sys lrck pulse
		17: eTDM OUT5 a1sys lrck pulse
		18: eTDM OUT6 a1sys lrck pulse
		19: eTDM OUT7 a1sys lrck pulse
		Domain: Else
		0: 8kHz
		1: 11.025kHz
		2: 12kHz
		4: 16kHz
		5: 22.05kHz
		6: 24kHz
		8: 32kHz
		9: 44kHz
		10: 48kHz
		13: 88.2kHz
		14: 96kHz
		17: 176.4kHz
		18: 192kHz
		21: 352.8kHz
		22: 384kHz
		Else: 0
23:14	reg_ck_en_sel_manual	When reg_ck_en_sel_auto is 0, this setting will replace the value of {reg_ch_num, reg_word_length}.
11	reg_async_reset	Software asynchronous reset. 0: Normal work 1: Asynchronous reset valid
10	reg_ck_en_sel_auto	Auto selects timing or not, only valid in engen timing mode. 0: Use manual mode to select timing (ETDM_IN_CON8[25:16]) 1: Auto select timing according to other settings
8:6	reg_clock_source_sel	Selects ETDM clock source. 3'h0: hopping clk domain

Bit(s)	Name	Description
		3'h1: apll clk domain
		3'h2: spdif clk domain
		3'h3: hdmi clk domain
		3'h4: earc clk domain
		3'h5: linein clk domain
		3'h6: slave clk domain
4:0	reg_fs_timing_sel	Sample rate select.
		0: 8kHz
		1: 12kHz
		2: 16kHz
		3: 24kHz
		4: 32kHz
		5: 48kHz
		7: 96kHz
		9: 192kHz
		11: 384kHz
		16: 11.025kHz
		17: 22.05kHz
		18: 44.1kHz
		19: 88.2kHz
		20: 176.4kHz
		21: 352.8kHz
		Else: 0

11211584 ETDM_OUT5_CON5 ETDM_OUT5 control register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_lr_swap															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reg_lrck_div_2	reg_repack_24b_msb_align	reg_master_ws_inv	reg_master_bck_inv	reg_slave_lrck_inv	reg_slave_bck_inv		reg_repack_chnum				reg_repack_bitnum	
Type				RW	RW	RW	RW	RW	RW		RW				RW	
Reset				0	0	0	0	0	0		0	0	0	0	0	0

Bit(s)	Name	Description
31:16	reg_lr_swap	Swaps right channel and left channel or not. Bit 0: For channel 0/1 Bit 1: For channel 2/3 Bit n: For channel 2n/2n+1
12	reg_lrck_div_2	Divides LRCK frequency by 2 0: Do not divide by 2 1: Divide by 2
11	reg_repack_24b_msb_align	Selects LSB or MSB alignment. 0: LSB 24 bits are valid 1: MSB 24 bits are valid
10	reg_master_ws_inv	This bit is only valid for output LRCK in master mode. 0: Not inverse 1: Inverse
9	reg_master_bck_inv	This bit is only valid for output BCK in master mode. 0: Not inverse 1: Inverse
8	reg_slave_lrck_inv	ETDM slave LRCK inverse or not. 0: Not inverse 1: Inverse
7	reg_slave_bck_inv	ETDM slave BCK inverse or not. 0: Not inverse 1: Inverse
5:2	reg_repack_chnum	ETDM out repack channel number. 0: 1

Bit(s)	Name	Description
		1: 2
		n: n+1
1:0	reg_repack_bitnum	ETDM out repack bit number.
		0: 8 bits
		1: 16 bits
		2: 24 bits
		3: 32 bits

11211590 ETDM_OUT5_CON8 ETDM_OUT5 control register 8 FEDCBA98

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_start_ch_pair15				reg_start_ch_pair14				reg_start_ch_pair13				reg_start_ch_pair12			
Type	RW				RW				RW				RW			
Reset	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_start_ch_pair11				reg_start_ch_pair10				reg_start_ch_pair9				reg_start_ch_pair8			
Type	RW				RW				RW				RW			
Reset	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0

Bit(s)	Name	Description
31:28	reg_start_ch_pair15	Selects ETDM OUT channel 30/31 start channel. 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is $(2*n)/(2*n+1)$
27:24	reg_start_ch_pair14	Selects ETDM OUT channel 28/29 start channel. 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is $(2*n)/(2*n+1)$
23:20	reg_start_ch_pair13	Selects ETDM OUT channel 26/27 start channel. 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is $(2*n)/(2*n+1)$
19:16	reg_start_ch_pair12	Selects ETDM OUT channel 24/25 start channel. 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is $(2*n)/(2*n+1)$
15:12	reg_start_ch_pair11	Selects ETDM OUT channel 22/23 start channel.

Bit(s)	Name	Description
		0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is $(2*n)/(2*n+1)$
11:8	reg_start_ch_pair10	Selects ETDM OUT channel 20/21 start channel. 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is $(2*n)/(2*n+1)$
7:4	reg_start_ch_pair9	Selects ETDM OUT channel 18/19 start channel. 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is $(2*n)/(2*n+1)$
3:0	reg_start_ch_pair8	Selects ETDM OUT channel 16/17 start channel. 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is $(2*n)/(2*n+1)$

112115E0 ETDM_4_7_COWORK_CON0 ETDM_4_7 co-work control register 0 81B2A908

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									etdm_out5_slave_sel				etdm_out5_sync_sel			
Type									RW				RW			
Reset									1	0	1	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	etdm_out5_data_sel															
Type	RW															
Reset	1	0	1	0												

Bit(s)	Name	Description
23:20	etdm_out5_slave_sel	Selects etdmout5 slave mode source. 0: From etdmin4 master 1: From etdmin4 slave 2: From etdmin5 master 3: From etdmin5 slave 4: From etdmin6 master 5: From etdmin6 slave 6: From etdmin7 master 7: From etdmin7 slave 8: From etdmout4 master 9: From etdmout4 slave 10: 1'b0 11: From etdmout5_slave 12: From etdmout6 master 13: From etdmout6 slave 14: From etdmout7 master 15: From etdmout7 slave
19:16	etdm_out5_sync_sel	Selects etdmout5 sync mode source. 0: From etdmin4 2: From etdmin5 4: From etdmin6 6: From etdmin7 8: From etdmout4 12: From etdmout6

Bit(s)	Name	Description
		14: From etdmout7
		Else: Not allowed.
15:12	etdm_out5_data_sel	Selects etdmout5 data source.
		0: From etdmin4
		2: From etdmin5
		4: From etdmin6
		6: From etdmin7
		8: From etdmout4 downlink
		10: From etdmout5 downlink
		12: From etdmout6 downlink
		14: From etdmout7 downlink
		Else: Not allowed.

112115E4 ETDM_4_7 COWORK_CON1 ETDM_4_7 co-work control register 1 0022A300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									etdm_in5_sdata1_15_sel				etdm_in5_sdata0_sel			
Type									RW				RW			
Reset									0	0	1	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	etdm_in5_sync_sel				etdm_in5_slave_sel											
Type	RW				RW											
Reset	1	0	1	0	0	0	1	1								

Bit(s)	Name	Description
23:20	etdm_in5_sdata1_15_sel	Selects etdmin5 sdata1 ~ sdata15 data source. 0: From etdmin4 2: From etdmin5 4: From etdmin6 6: From etdmin7 8: From etdmout4 10: From etdmout5 12: From etdmout6 14: From etdmout7 Else: Not allowed.
19:16	etdm_in5_sdata0_sel	Selects etdmin5 sdata0 data source. 0: From etdmin4 2: From etdmin5 4: From etdmin6 6: From etdmin7 8: From etdmout4 10: From etdmout5 12: From etdmout6 14: From etdmout7 Else: Not allowed.
15:12	etdm_in5_sync_sel	Selects etdmin5 sync mode source. 0: From etdmin4 4: From etdmin6 6: From etdmin7

Bit(s)	Name	Description
		8: From etdmout4
		10: From etdmout5
		12: From etdmout6
		14: From etdmout7
		Else: Not allowed.
11:8	etdm_in5_slave_sel	Selects etdmin5 slave mode source.
		0: From etdmin4 master
		1: From etdmin4 slave
		2: 1'b0
		3: From etdmin5 slave
		4: From etdmin6 master
		5: From etdmin6 slave
		6: From etdmin7 master
		7: From etdmin7 slave
		8: From etdmout4 master
		9: From etdmout4 slave
		10: From etdmout5_master
		11: From etdmout5_slave
		12: From etdmout6 master
		13: From etdmout6 slave
		14: From etdmout7 master
		15: From etdmout7 slave

11213900 AFE_CONN_MON_CFG AFE connection monitor control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_conn_mon_cfg															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_conn_mon_cfg															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_conn_mon_cfg	AFE connection monitor control register

11213904 AFE_CONN_MON0 AFE connection monitor0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_conn_mon0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_conn_mon0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_conn_mon0	AFE connection monitor 0

11213908 AFE_CONN_MON1 AFE connection monitor1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_conn_mon1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_conn_mon1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_conn_mon1	AFE connection monitor 1

1121390C AFE_CONN_MON2 AFE connection monitor2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_conn_mon2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_conn_mon2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_conn_mon2	AFE connection monitor 2

11213910 AFE_CONN_MON3 AFE connection monitor3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_conn_mon3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_conn_mon3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_conn_mon3	AFE connection monitor 3

11213914 AFE_CONN_MON4 AFE connection monitor4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_conn_mon4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_conn_mon4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_conn_mon4	AFE connection monitor 4

11213918 AFE_CONN_MON5 AFE connection monitor5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_conn_mon5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_conn_mon5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_conn_mon5	AFE connection monitor 5

11213920 AFE_CONN_RS_0 AFE connection right shift register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													O019_RS	O018_RS		
Type													RW	RW		
Reset													0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
19	O019_RS	Interconn right shift control 0: No shift 1: Right shift 1 bit
18	O018_RS	Interconn right shift control 0: No shift 1: Right shift 1 bit

1121392C AFE_CONN_RS_3 AFE connection right shift register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			O125_RS	O124_RS												
Type			RW	RW												
Reset			0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
29	O125_RS	Interconn right shift control 0: No shift 1: Right shift 1 bit
28	O124_RS	Interconn right shift control 0: No shift 1: Right shift 1 bit

11213960 AFE_CONN_16BIT_0 AFE connection 16-bit register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													O019_16BIT	O018_16BIT		
Type													RW	RW		
Reset													0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
19	O019_16BIT	Interconn bit number control 0: 32-bit 1: 16-bit
18	O018_16BIT	Interconn bit number control 0: 32-bit 1: 16-bit

1121396C AFE_CONN_16BIT_3 AFE connection 16-bit register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			O125_16BIT	O124_16BIT												
Type			RW	RW												
Reset			0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
29	O125_16BIT	Interconn bit number control 0: 32-bit 1: 16-bit
28	O124_16BIT	Interconn bit number control 0: 32-bit 1: 16-bit

11213980 AFE_CONN_24BIT_0 AFE connection 24-bit register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													O019_24BIT	O018_24BIT		
Type													RW	RW		
Reset													0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
19	O019_24BIT	Interconn bit number control 0: 32-bit 1: 24-bit
18	O018_24BIT	Interconn bit number control 0: 32-bit 1: 24-bit

1121398C AFE_CONN_24BIT_3 AFE connection 24-bit register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			O125_24BIT	O124_24BIT												
Type			RW	RW												
Reset			0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
29	O125_24BIT	Interconn bit number control 0: 32-bit 1: 24-bit
28	O124_24BIT	Interconn bit number control 0: 32-bit 1: 24-bit

11213D80	AFE_CBIP_CFG0				AFE CBIP configuration								FFFF0021			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CBIP_TOP_SLV_MUX_way_en															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CBIP_ASYNC_MST_RG_FIFO_THRE		CBIP_ASYNC_MST_postwrite_dis		CBIP_ASYNC_SLV_RG_FIFO_THRE		CBIP_ASYNC_SLV_postwrite_dis	audiosys_busy	CBIP_SLV_DECODER_err_flag_en	CBIP_SLV_DECODER_slave_way_en		APB_R2T	APB_W2T	ahb_idle_en	ahb_idle_ext
Type		RW		RW		RW		RW	RW	RW	RW		RW	RW	RW	RW
Reset		0	0	0		0	0	0	0	0	1		0	0	0	1

Bit(s)	Name	Description
31:16	CBIP_TOP_SLV_MUX_way_en	Audio slave mux enable 0: Disable 1: Enable
14:13	CBIP_ASYNC_MST_RG_FIFO_THRE	Audio master FIFO threshold
12	CBIP_ASYNC_MST_postwrite_dis	Audio master write disable 0: Enable 1: Disable
10:9	CBIP_ASYNC_SLV_RG_FIFO_THRE	Audio slave FIFO threshold
8	CBIP_ASYNC_SLV_postwrite_dis	Audio slave write disable 0: Enable 1: Disable
7	audiosys_busy	audiosys_busy 1: busy
6	CBIP_SLV_DECODER_err_flag_en	Audio slave decoder error flag enable 0: Disable 1: Enable
5	CBIP_SLV_DECODER_slave_way_en	Audio slave decoder enable 0: Disable 1: Enable
3	APB_R2T	Read cycle for APB write 0: 1T 1: 2T
2	APB_W2T	Read cycle for APB read

Bit(s)	Name	Description
		0: 1T
		1: 2T
1	ahb_idle_en_int	Enables AHB idle for internal bus clock
		0: Disable
		1: Enable
0	ahb_idle_en_ext	Enables AHB idle for external bus clock
		0: Disable
		1: Enable

11213D98 **AFE_MEMIF_CON0** MEMIF related configuration 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CPU_C OMPA CT_MO DE	CPU_H D_ALIG N	SYSRA M_SIG N
Type														RW	RW	RW
Reset														0	0	1

Bit(s)	Name	Description
2	CPU_COMPACT_MODE	Selects valid 24-bit data from 32-bit write data bus 0: 24-bit uses normal mode 1: 24-bit uses compact mode
1	CPU_HD_ALIGN	Selects valid 24-bit data from 32-bit write data bus 0: {8'b0, 24-bit data} 1: {24-bit data, 8'b0}
0	SYSRAM_SIGN	Signed extension 24-bit data to 32-bit for bus read SYSRAM 0: Append 0 1: bit[23] signed extension

11211B44 AFE_CONN018_1 AFE connection register 018_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															I033_O018_S	I032_O018_S
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	I033_O018_S	Controls the path from I033 to O018. 0: Off 1: On
0	I032_O018_S	Controls the path from I032 to O018. 0: Off 1: On

11211B50 AFE_CONN018_4 AFE connection register 018_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									I151_O018_S	I150_O018_S						
Type									RW	RW						
Reset									0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
23	I151_O018_S	Controls the path from I151 to O018. 0: Off 1: On
22	I150_O018_S	Controls the path from I150 to O018. 0: Off 1: On

11211B64 AFE_CONN019_1 AFE connection register 019_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															I033_O019_S	I032_O019_S
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	I033_O019_S	Controls the path from I033 to O019. 0: Off 1: On
0	I032_O019_S	Controls the path from I032 to O019. 0: Off 1: On

11211B70 AFE_CONN019_4 AFE connection register 019_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									I151_O019_S	I150_O019_S						
Type									RW	RW						
Reset									0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
23	I151_O019_S	Controls the path from I151 to O019. 0: Off 1: On
22	I150_O019_S	Controls the path from I150 to O019. 0: Off 1: On

11212884 AFE_CONN124_1 AFE connection register 124_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															I033_O124_S	I032_O124_S
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	I033_O124_S	Controls the path from I033 to O124. 0: Off 1: On
0	I032_O124_S	Controls the path from I032 to O124. 0: Off 1: On

11212890 AFE_CONN124_4 AFE connection register 124_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									I151_O124_S	I150_O124_S						
Type									RW	RW						
Reset									0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
23	I151_O124_S	Controls the path from I151 to O124. 0: Off 1: On
22	I150_O124_S	Controls the path from I150 to O124. 0: Off 1: On

112128A4 AFE_CONN125_1 AFE connection register 125_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															I033_O125_S	I032_O125_S
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	I033_O125_S	Controls the path from I033 to O125. 0: Off 1: On
0	I032_O125_S	Controls the path from I032 to O125. 0: Off 1: On

112128B0 AFE_CONN125_4 AFE connection register 125_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									I151_O125_S	I150_O125_S						
Type									RW	RW						
Reset									0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
23	I151_O125_S	Controls the path from I151 to O125. 0: Off 1: On
22	I150_O125_S	Controls the path from I150 to O125. 0: Off 1: On

11213E40 AFE_DL0_BASE_MSB AFE DL0 base address register MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DLO_BASE_ADDR_MSB		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	DLO_BASE_ADDR_MSB	Base address MSB of the DL input at master mode.

11213E44 AFE_DL0_BASE AFE DL0 base address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DLO_BASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DLO_BASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	DLO_BASE_ADDR	Base address of the DL input at master mode. Please always set AFE_DL_BASE[3:0] = 4'h0 for the convenience of the hardware implementation

11213E48 AFE_DL0_CUR_MSB AFE DL0 cursor register MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DL0_CUR_PTR_MSB		
Type														RU		
Reset														0	0	0

Bit(s)	Name	Description
2:0	DL0_CUR_PTR_MSB	Current address MSB of the DL input buffer

11213E4C AFE_DL0_CUR AFE DL0 cursor register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DL0_CUR_PTR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL0_CUR_PTR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DL0_CUR_PTR	Indicates the current address of the DL input buffer

11213E50 AFE_DL0_END_MSB AFE DL0 end address register MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DL0_END_ADDR_MSB		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	DL0_END_ADDR_MSB	Ending address MSB of the DL input at master mode.

11213E54 AFE_DL0_END AFE DL0 end address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DL0_END_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL0_END_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	DL0_END_ADDR	Ending address of the DL input at master mode. Please always set AFE_DL_END[3:0] = 4'hf for the convenience of the hardware implementation

11213E58 AFE_DL0_RCH_MON AFE memory Interface monitor register RCH 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DL0_RCH_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL0_RCH_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DL0_RCH_DATA	Monitors RCH memory interface output.

11213E5C AFE_DL0_LCH_MON AFE memory Interface monitor register LCH 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DL0_LCH_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL0_LCH_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DL0_LCH_DATA	Monitors LCH memory interface output.

11213E60	AFE DLO_CON0				AFE DLO agent control register								00310068			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DLO_ON					DLO_MINLEN				DLO_MAXLEN			
Type				RW					RW				RW			
Reset				0					0	0	1	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DLO_SEL_DOMAIN			DLO_SEL_FS					DLO_SW_CLEAR_BUFFER_EMPTY	DLO_PBUF_SIZE		DLO_MONO	DLO_NORMAL_MODE	DLO_HALIGN	DLO_HD_MODE	
Type	RW			RW					RW	RW		RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0

Bit(s)	Name	Description
28	DLO_ON	Controls the enabling of DL memory interface path 0: Off 1: On
23:20	DLO_MINLEN	The minimum number of data remaining in PBUF 0: 0 byte 1: 8 bytes 2: 16 bytes 3: 32 bytes 4~15: Not supported
19:16	DLO_MAXLEN	Burst length selection 0: Not supported 1: 16-byte burst 2: 32-byte burst 3: 64-byte burst 4~15: Not supported
15:13	DLO_SEL_DOMAIN	Controls the sampling domain 3'h0: hopping clk domain 3'h1: apll clk domain 3'h2: spdif clk domain 3'h3: hdmi clk domain 3'h4: earc clk domain 3'h5: linein clk domain

Bit(s)	Name	Description
		3'h6: slave clk domain
12:8	DLO_SEL_FS	Controls the sampling frequency 5'h00: 8k 5'h01: 11k 5'h02: 12k 5'h04: 16k 5'h05: 22k 5'h06: 24k 5'h08: 32k 5'h09: 44k 5'h0a: 48k 5'h0d: 88k 5'h0e: 96k 5'h11: 176k 5'h12: 192k 5'h15: 352k 5'h16: 384k
7	DLO_SW_CLEAR_BUF_EMPTY	Clear the buf_empty monitor
6:5	DLO_PBUF_SIZE	Prefetch buffer size 0: 32 bytes 1: 64 bytes 2: 128 bytes 3: 256 bytes
4	DLO_MONO	Controls the data mode. 0: Stereo 1: Mono
3	DLO_NORMAL_MODE	24-bit compact mode selection 0: 24-bit uses compact mode 1: 24-bit uses normal mode
2	DLO_HALIGN	MSB align or LSB align selection in 24-bit compact mode 0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}

Bit(s)	Name	Description
1:0	DLO_HD_MODE	16-bit mode or 24-bit mode selection 0: 16-bit format 1: 24-bit format 2,3: Not supported

11214220 AFE_VULO_BASE_MSB AFE VULO base address register MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														VULO_BASE_ADDR_MSB		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	VULO_BASE_ADDR_MSB	Base address MSB of the VUL input at master mode.

11214224 AFE_VULO_BASE AFE VULO base address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VULO_BASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VULO_BASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	VULO_BASE_ADDR	Base address of the VUL input at master mode. Please always set AFE_VUL_BASE[3:0] = 4'h0 for the convenience of the hardware implementation

11214228 AFE VULO_CUR_MSB AFE VULO cursor register MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														VULO_CUR_PTR_MSB		
Type														RU		
Reset														0	0	0

Bit(s)	Name	Description
2:0	VULO_CUR_PTR_MSB	Current address MSB of the VUL input buffer.

1121422C AFE VULO_CUR AFE VULO cursor register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VULO_CUR_PTR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VULO_CUR_PTR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VULO_CUR_PTR	Indicates the current address of the VUL input buffer.

11214230 AFE_VULO_END_MSB AFE_VULO end address register MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														VULO_END_ADDR_MSB		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	VULO_END_ADDR_MSB	Ending address MSB of the VUL input at master mode.

11214234 AFE_VULO_END AFE_VULO end address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VULO_END_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VULO_END_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	VULO_END_ADDR	Ending address of the VUL input at master mode. Please always set AFE_VUL_END[3:0] = 4'hf for the convenience of the hardware implementation

11214238 AFE_VULO_CON0 AFE_VULO agent control register 00000048

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VULO_ON												
Type				RW												
Reset				0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VULO_SEL_DOMAIN			VULO_SEL_FS					VULO_SW_CLEAR_BUFFER_FULL	VULO_WR_SIGN	VULO_R_MONO	VULO_MONO	VULO_NORMAL_MODE	VULO_HALIGN	VULO_HD_MODE	
Type	RW			RW					RW	RW	RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0

Bit(s)	Name	Description
28	VULO_ON	Controls the enabling of VUL memory interface path 0: Off 1: On
15:13	VULO_SEL_DOMAIN	Controls the sampling frequency 3'h0: hopping clk domain 3'h1: apll clk domain 3'h2: spdif clk domain 3'h3: hdmi clk domain 3'h4: earc clk domain 3'h5: linein clk domain 3'h6: slave clk domain
12:8	VULO_SEL_FS	Frequency selection 5'h00: 8k 5'h01: 11k 5'h02: 12k 5'h04: 16k 5'h05: 22k 5'h06: 24k 5'h08: 32k 5'h09: 44k 5'h0a: 48k 5'h0d: 88k 5'h0e: 96k

Bit(s)	Name	Description
		5'h11: 176k
		5'h12: 192k
		5'h15: 352k
		5'h16: 384k
7	VULO_SW_CLEAR_BUF_FULL	Clear the buf_full monitor
6	VULO_WR_SIGN	Signed extension 24-bit data to 32-bit for VUL memory agent 0: Append 0 1: bit[23] signed extension
5	VULO_R_MONO	Controls the data mono type for voice uplink memory interface path. 0: Mono uses L channel 1: Mono uses R channel
4	VULO_MONO	Controls the data mode. 0: Stereo 1: Mono
3	VULO_NORMAL_MODE	24-bit compact mode selection 0: 24-bit uses compact mode 1: 24-bit uses normal mode
2	VULO_HALIGN	MSB align or LSB align selection in 24-bit compact mode 0: {8'b0, 24-bit data} 1: {24-bit data, 8'b0}
1:0	VULO_HD_MODE	16-bit mode or 24-bit mode selection 0: 16-bit format 1: 24-bit format 2, 3: Not supported

3.10 GPIO (General-Purpose Input/Output)

3.10.1 Register Definition

Module name: GPIO Base address: (+0x1001_F000)

Address	Name	Width	Register Function
1001F000	<u>GPIO_DIR0</u>	32	GPIO_DIRECTION register for GPIO0~GPIO31
1001F010	<u>GPIO_DIR1</u>	32	GPIO_DIRECTION register for GPIO32~GPIO63
1001F020	<u>GPIO_DIR2</u>	32	GPIO_DIRECTION register for GPIO64~GPIO83; GPIO84~GPIO95: reserved
1001F004	<u>GPIO_DIR0_SET</u>	32	GPIO_DIRECTION register for GPIO0~GPIO31
1001F014	<u>GPIO_DIR1_SET</u>	32	GPIO_DIRECTION register for GPIO32~GPIO63
1001F024	<u>GPIO_DIR2_SET</u>	32	GPIO_DIRECTION register for GPIO64~GPIO83; GPIO84~GPIO95: reserved
1001F008	<u>GPIO_DIR0_CLR</u>	32	GPIO_DIRECTION register for GPIO0~GPIO31
1001F018	<u>GPIO_DIR1_CLR</u>	32	GPIO_DIRECTION register for GPIO32~GPIO63
1001F028	<u>GPIO_DIR2_CLR</u>	32	GPIO_DIRECTION register for GPIO64~GPIO83; GPIO84~GPIO95: reserved
1001F100	<u>GPIO_DOUT0</u>	32	GPIO_DOUT register GPIO0~GPIO31
1001F110	<u>GPIO_DOUT1</u>	32	GPIO_DOUT register GPIO32~GPIO63
1001F120	<u>GPIO_DOUT2</u>	32	GPIO_DOUT register GPIO64~GPIO83; GPIO84~GPIO95: reserved
1001F104	<u>GPIO_DOUT0_SET</u>	32	GPIO_DOUT register GPIO0~GPIO31
1001F114	<u>GPIO_DOUT1_SET</u>	32	GPIO_DOUT register GPIO32~GPIO63
1001F124	<u>GPIO_DOUT2_SET</u>	32	GPIO_DOUT register GPIO64~GPIO83; GPIO84~GPIO95: reserved
1001F108	<u>GPIO_DOUT0_CLR</u>	32	GPIO_DOUT register GPIO0~GPIO31
1001F118	<u>GPIO_DOUT1_CLR</u>	32	GPIO_DOUT register GPIO32~GPIO63
1001F128	<u>GPIO_DOUT2_CLR</u>	32	GPIO_DOUT register GPIO64~GPIO83; GPIO84~GPIO95: reserved
1001F200	<u>GPIO_DIN0</u>	32	GPIO_DIN for GPIO0~GPIO31
1001F210	<u>GPIO_DIN1</u>	32	GPIO_DIN for GPIO32~GPIO63
1001F220	<u>GPIO_DIN2</u>	32	GPIO_DIN for GPIO64~GPIO83; GPIO84~GPIO95: reserved
1001F300	<u>GPIO_MODE0</u>	32	Aux mode of PAD_UART2_RXD
1001F310	<u>GPIO_MODE1</u>	32	Aux mode of PAD_PCIE30_2L_0_CLKREQ_N
1001F320	<u>GPIO_MODE2</u>	32	Aux mode of PAD_PMIC_I2C_SDA
1001F330	<u>GPIO_MODE3</u>	32	Aux mode of PAD_SPI0_CSB
1001F340	<u>GPIO_MODE4</u>	32	Aux mode of PAD_SPI2_CLK
1001F350	<u>GPIO_MODE5</u>	32	Aux mode of PAD_EMMC_CK
1001F360	<u>GPIO_MODE6</u>	32	Aux mode of PAD_EMMC_DATA_1
1001F370	<u>GPIO_MODE7</u>	32	Aux mode of PAD_UART0_TXD
1001F380	<u>GPIO_MODE8</u>	32	Aux mode of PAD_LED_A
1001F390	<u>GPIO_MODE9</u>	32	Aux mode of PAD_I2C_2_SDA
1001F3A0	<u>GPIO_MODE10</u>	32	Aux mode of PAD_UART1_RXD
1001F304	<u>GPIO_MODE0_SET</u>	32	Bitwise SET of Aux mode of PAD_UART2_RXD
1001F314	<u>GPIO_MODE1_SET</u>	32	Bitwise SET of Aux mode of PAD_PCIE30_2L_0_CLKREQ_N
1001F324	<u>GPIO_MODE2_SET</u>	32	Bitwise SET of Aux mode of PAD_PMIC_I2C_SDA
1001F334	<u>GPIO_MODE3_SET</u>	32	Bitwise SET of Aux mode of PAD_SPI0_CSB
1001F344	<u>GPIO_MODE4_SET</u>	32	Bitwise SET of Aux mode of PAD_SPI2_CLK

Address	Name	Width	Register Function
1001F354	<u>GPIO_MODE5_SET</u>	32	Bitwise SET of Aux mode of PAD_EMMC_CK
1001F364	<u>GPIO_MODE6_SET</u>	32	Bitwise SET of Aux mode of PAD_EMMC_DATA_1
1001F374	<u>GPIO_MODE7_SET</u>	32	Bitwise SET of Aux mode of PAD_UART0_TXD
1001F384	<u>GPIO_MODE8_SET</u>	32	Bitwise SET of Aux mode of PAD_LED_A
1001F394	<u>GPIO_MODE9_SET</u>	32	Bitwise SET of Aux mode of PAD_I2C_2_SDA
1001F3A4	<u>GPIO_MODE10_SET</u>	32	Bitwise SET of Aux mode of PAD_UART1_RXD
1001F308	<u>GPIO_MODE0_CLR</u>	32	Bitwise clear of Aux mode of PAD_UART2_RXD
1001F318	<u>GPIO_MODE1_CLR</u>	32	Bitwise clear of Aux mode of PAD_PCIE30_2L_0_CLKREQ_N
1001F328	<u>GPIO_MODE2_CLR</u>	32	Bitwise clear of Aux mode of PAD_PMIC_I2C_SDA
1001F338	<u>GPIO_MODE3_CLR</u>	32	Bitwise clear of Aux mode of PAD_SPI0_CSB
1001F348	<u>GPIO_MODE4_CLR</u>	32	Bitwise clear of Aux mode of PAD_SPI2_CLK
1001F358	<u>GPIO_MODE5_CLR</u>	32	Bitwise clear of Aux mode of PAD_EMMC_CK
1001F368	<u>GPIO_MODE6_CLR</u>	32	Bitwise clear of Aux mode of PAD_EMMC_DATA_1
1001F378	<u>GPIO_MODE7_CLR</u>	32	Bitwise clear of Aux mode of PAD_UART0_TXD
1001F388	<u>GPIO_MODE8_CLR</u>	32	Bitwise clear of Aux mode of PAD_LED_A
1001F398	<u>GPIO_MODE9_CLR</u>	32	Bitwise clear of Aux mode of PAD_I2C_2_SDA
1001F3A8	<u>GPIO_MODE10_CLR</u>	32	Bitwise clear of Aux mode of PAD_UART1_RXD
1001F30C	<u>GPIO_MODE0_MOD</u>	32	Alternative way to set Aux mode of PAD_UART2_RXD
1001F31C	<u>GPIO_MODE1_MOD</u>	32	Alternative way to set Aux mode of PAD_PCIE30_2L_0_CLKREQ_N
1001F32C	<u>GPIO_MODE2_MOD</u>	32	Alternative way to set Aux mode of PAD_PMIC_I2C_SDA
1001F33C	<u>GPIO_MODE3_MOD</u>	32	Alternative way to set Aux mode of PAD_SPI0_CSB
1001F34C	<u>GPIO_MODE4_MOD</u>	32	Alternative way to set Aux mode of PAD_SPI2_CLK
1001F35C	<u>GPIO_MODE5_MOD</u>	32	Alternative way to set Aux mode of PAD_EMMC_CK
1001F36C	<u>GPIO_MODE6_MOD</u>	32	Alternative way to set Aux mode of PAD_EMMC_DATA_1
1001F37C	<u>GPIO_MODE7_MOD</u>	32	Alternative way to set Aux mode of PAD_UART0_TXD
1001F38C	<u>GPIO_MODE8_MOD</u>	32	Alternative way to set Aux mode of PAD_LED_A
1001F39C	<u>GPIO_MODE9_MOD</u>	32	Alternative way to set Aux mode of PAD_I2C_2_SDA
1001F3AC	<u>GPIO_MODE10_MOD</u>	32	Alternative way to set Aux mode of PAD_UART1_RXD
1001F600	<u>MISC</u>	32	Chip related misc options
1001F604	<u>MISC_SET</u>	32	Chip related misc options
1001F608	<u>MISC_CLR</u>	32	Chip related misc options
1001F6D0	<u>DBG</u>	32	dbg_mon control bit
1001F6E0	<u>BANK</u>	32	GPIO reserved control register [0]: test_normal_sel_bypreg
1001F6F0	<u>TPBANK0</u>	32	Trapping force enable
1001F710	<u>AP_GOOD</u>	32	Chip related AP_GPPD control
1001F714	<u>AP_GOOD_SET</u>	32	Chip related AP_GPPD control
1001F718	<u>AP_GOOD_CLR</u>	32	Chip related AP_GPPD control
1001F720	<u>MODE_CFG_CT_REG</u>	32	GPIO reserved control register [0]: test_normal_sel_bypreg
1001F724	<u>MODE_CFG_CT_REG_SET</u>	32	GPIO reserved control register [0]: test_normal_sel_bypreg
1001F728	<u>MODE_CFG_CT_REG_CLR</u>	32	GPIO reserved control register [0]: test_normal_sel_bypreg

1001F000 GPIO_DIR0 GPIO_DIRECTION register for GPIO0~GPIO31 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG0	SRW	GPIO_DIRECTION register for GPIO0~GPIO31 0: GPIO Direction as Input; 1: GPIO Direction as Output

1001F010 GPIO_DIR1 GPIO_DIRECTION register for GPIO32~GPIO63 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG1	SRW	GPIO_DIRECTION register for GPIO32~GPIO63 0: GPIO Direction as Input; 1: GPIO Direction as Output

1001F020

GPIO_DIR2

GPIO_DIRECTION register for GPIO64~GPIO83;
GPIO84~GPIO95: reserved

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CFG2							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
23:0	CFG2	SRW	GPIO_DIRECTION register for GPIO64~GPIO83; GPIO84~GPIO95: reserved
0: GPIO Direction as Input; 1: GPIO Direction as Output			

1001F004

GPIO_DIR0_SET

GPIO_DIRECTION register for GPIO0~GPIO31

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG0	SW	GPIO_DIRECTION register for GPIO0~GPIO31
0: Keep; 1: SET bit			

1001F014 **GPIO DIR1 SET** **GPIO_DIRECTION register for GPIO32~GPIO63** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG1	SW	GPIO_DIRECTION register for GPIO32~GPIO63 0: Keep; 1: SET bit

1001F024 **GPIO DIR2 SET** **GPIO_DIRECTION register for GPIO64~GPIO83;
GPIO84~GPIO95: reserved** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CFG2							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
23:0	CFG2	SW	GPIO_DIRECTION register for GPIO64~GPIO83; GPIO84~GPIO95: reserved 0: Keep; 1: SET bit

1001F008 **GPIO DIR0_CLR** **GPIO_DIRECTION register for GPIO0~GPIO31** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG0	SW	GPIO_DIRECTION register for GPIO0~GPIO31 0: Keep; 1: Clear bit

1001F018 **GPIO DIR1_CLR** **GPIO_DIRECTION register for GPIO32~GPIO63** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG1	SW	GPIO_DIRECTION register for GPIO32~GPIO63 0: Keep; 1: Clear bit

1001F028

GPIO_DIR2_CLR

GPIO_DIRECTION register for GPIO64~GPIO83;
GPIO84~GPIO95: reserved

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CFG2							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
23:0	CFG2	SW	GPIO_DIRECTION register for GPIO64~GPIO83; GPIO84~GPIO95: reserved 0: Keep; 1: Clear bit

1001F100

GPIO_DOUT0

GPIO_DOUT register GPIO0~GPIO31

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG0	SRW	GPIO_DOUT register GPIO0~GPIO31 0: GPIO output low; 1: GPIO output high

1001F110 **GPIO_DOUT1** **GPIO_DOUT register GPIO32~GPIO63** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG1	SRW	GPIO_DOUT register GPIO32~GPIO63 0: GPIO output low; 1: GPIO output high

1001F120 **GPIO_DOUT2** **GPIO_DOUT register GPIO64~GPIO83;
GPIO84~GPIO95: reserved** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CFG2							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
23:0	CFG2	SRW	GPIO_DOUT register GPIO64~GPIO83; GPIO84~GPIO95: reserved 0: GPIO output low; 1: GPIO output high

1001F104 **GPIO_DOUT0_SET** **GPIO_DOUT register GPIO0~GPIO31** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG0	SW	GPIO_DOUT register GPIO0~GPIO31 0: Keep; 1: SET bit

1001F114 **GPIO_DOUT1_SET** **GPIO_DOUT register GPIO32~GPIO63** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG1	SW	GPIO_DOUT register GPIO32~GPIO63 0: Keep; 1: SET bit

1001F124 GPIO_DOUT2_SET GPIO_DOUT register GPIO64~GPIO83;
GPIO84~GPIO95: reserved 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CFG2							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
23:0	CFG2	SW	GPIO_DOUT register GPIO64~GPIO83; GPIO84~GPIO95: reserved 0: Keep; 1: SET bit

1001F108 GPIO_DOUT0_CLR GPIO_DOUT register GPIO0~GPIO31 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG0	SW	GPIO_DOUT register GPIO0~GPIO31 0: Keep; 1: Clear bit

1001F118 **GPIO_DOUT1_CLR** **GPIO_DOUT register GPIO32~GPIO63** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG1	SW	GPIO_DOUT register GPIO32~GPIO63 0: Keep; 1: Clear bit

1001F128 **GPIO_DOUT2_CLR** **GPIO_DOUT register GPIO64~GPIO83;** **00000000**
GPIO84~GPIO95: reserved

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									CFG2							
Type									WO							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
23:0	CFG2	SW	GPIO_DOUT register GPIO64~GPIO83; GPIO84~GPIO95: reserved 0: Keep; 1: Clear bit

1001F200 **GPIO_DIN0** **GPIO_DIN for GPIO0~GPIO31** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DATA0	SRW	GPIO_DIN for GPIO0~GPIO31 [31:0] value of GPIO Input

1001F210 **GPIO_DIN1** **GPIO_DIN for GPIO32~GPIO63** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DATA1	SRW	GPIO_DIN for GPIO32~GPIO63 [31:0] value of GPIO Input

1001F220 GPIO_DIN2 GPIO_DIN for GPIO64~GPIO83; GPIO84~GPIO95: reserved 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DATA2							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
23:0	DATA2	SRW	GPIO_DIN for GPIO64~GPIO83; GPIO84~GPIO95: reserved [31:0] value of GPIO Input

1001F300	GPIO_MODE0				Aux mode of PAD_UART2_RXD								11101111			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO7					GPIO6					GPIO5				GPIO4	
Type	RW					RW					RW				RW	
Reset		0	0	1		0	0	1		0	0	1		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO3					GPIO2					GPIO1				GPIO0	
Type	RW					RW					RW				RW	
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Name	Secure	Description
30:28	GPIO7	SRW	Aux mode of PAD_PCIE30_2L_0_WAKE_N 000:B:GPIO7;001:I1:PCIE30_2L_0_WAKE_N
26:24	GPIO6	SRW	Aux mode of PAD_SMI_0_MDIO 000:B:GPIO6;001:B1:SMI_0_MDIO;010:B1:I2C_0_SDA0;100:B1:I2C_1_SDA
22:20	GPIO5	SRW	Aux mode of PAD_SMI_0_MDC 000:B:GPIO5;001:O:SMI_0_MDC;010:B1:I2C_0_SCL;100:B1:I2C_1_SCL
18:16	GPIO4	SRW	Aux mode of PAD_GPIO_A 000:B:GPIO4;011:O:PWM7
14:12	GPIO3	SRW	Aux mode of PAD_UART2_RTS 000:B:GPIO3;001:O:UART2_RTS
10:8	GPIO2	SRW	Aux mode of PAD_UART2_CTS 000:B:GPIO2;001:I1:UART2_CTS
6:4	GPIO1	SRW	Aux mode of PAD_UART2_TXD 000:B:GPIO1;001:O:UART2_TXD
2:0	GPIO0	SRW	Aux mode of PAD_UART2_RXD 000:B:GPIO0;001:I1:UART2_RXD

1001F310	GPIO_MODE1				Aux mode of PAD_PCIE30_2L_0_CLKREQ_N								10011111			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO15					GPIO14					GPIO13				GPIO12	
Type	RW					RW					RW				RW	
Reset		0	0	1		0	0	0		0	0	0		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO11					GPIO10					GPIO9				GPIO8	
Type	RW					RW					RW				RW	
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Name	Secure	Description
30:28	GPIO15	SRW	Aux mode of PAD_PMIC_I2C_SCL 000:B:GPIO15;001:B1:I2C_0_SCL
26:24	GPIO14	SRW	Aux mode of PAD_GPIO_WPS 000:B:GPIO14
22:20	GPIO13	SRW	Aux mode of PAD_GPIO_RESET 000:B:GPIO13
18:16	GPIO12	SRW	Aux mode of PAD_WATCHDOG 000:B:GPIO12;001:O:WATCHDOG
14:12	GPIO11	SRW	Aux mode of PAD_GPIO_P 000:B:GPIO11
10:8	GPIO10	SRW	Aux mode of PAD_PCIE30_1L_1_CLKREQ_N 000:B:GPIO10;001:B1:PCIE30_1L_1_CLKREQ_N
6:4	GPIO9	SRW	Aux mode of PAD_PCIE30_1L_1_WAKE_N 000:B:GPIO9;001:I1:PCIE30_1L_1_WAKE_N
2:0	GPIO8	SRW	Aux mode of PAD_PCIE30_2L_0_CLKREQ_N 000:B:GPIO8;001:B1:PCIE30_2L_0_CLKREQ_N

1001F320	GPIO_MODE2				Aux mode of PAD_PMIC_I2C_SDA								11111111			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO23					GPIO22					GPIO21				GPIO20
Type		RW					RW					RW				RW
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO19					GPIO18					GPIO17				GPIO16
Type		RW					RW					RW				RW
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Name	Secure	Description
30:28	GPIO23	SRW	Aux mode of PAD_SPI0_HOLD 000:B:GPIO23;001:B0:SPI0_HOLD;010:B0:SNFI_HOLD
26:24	GPIO22	SRW	Aux mode of PAD_SPI0_WP 000:B:GPIO22;001:B0:SPI0_WP;010:B0:SNFI_WP
22:20	GPIO21	SRW	Aux mode of PAD_PWMD1 000:B:GPIO21;001:O:PWMD1;101:O:EMMC_RSTB
18:16	GPIO20	SRW	Aux mode of PAD_PCIE30_1L_1_PRESET_N 000:B:GPIO20;001:O:PCIE30_1L_1_PRESET_N
14:12	GPIO19	SRW	Aux mode of PAD_PCIE30_2L_0_PRESET_N 000:B:GPIO19;001:O:PCIE30_2L_0_PRESET_N
10:8	GPIO18	SRW	Aux mode of PAD_I2C_1_SDA 000:B:GPIO18;001:B1:I2C_1_SDA
6:4	GPIO17	SRW	Aux mode of PAD_I2C_1_SCL 000:B:GPIO17;001:B1:I2C_1_SCL
2:0	GPIO16	SRW	Aux mode of PAD_PMIC_I2C_SDA 000:B:GPIO16;001:B1:I2C_0_SDA

1001F330	GPIO_MODE3				Aux mode of PAD_SPI0_CSB								11111111			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31					GPIO30					GPIO29				GPIO28	
Type	RW					RW					RW				RW	
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO27					GPIO26					GPIO25				GPIO24	
Type	RW					RW					RW				RW	
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Name	Secure	Description
30:28	GPIO31	SRW	Aux mode of PAD_SPI1_CLK 000:B:GPIO31;001:O:SPI1_CLK;010:O:UART2_RTS;101:B1:EMMC_DATA_4
26:24	GPIO30	SRW	Aux mode of PAD_SPI1_MOSI 000:B:GPIO30;001:O:SPI1_MOSI;010:I1:UART2_CTS;101:B1:EMMC_DATA_5
22:20	GPIO29	SRW	Aux mode of PAD_SPI1_MISO 000:B:GPIO29;001:I0:SPI1_MISO;010:O:UART2_TXD;101:B1:EMMC_DATA_6
18:16	GPIO28	SRW	Aux mode of PAD_SPI1_CSB 000:B:GPIO28;001:O:SPI1_CSB;010:I1:UART2_RXD;101:B1:EMMC_DATA_7
14:12	GPIO27	SRW	Aux mode of PAD_SPI0_CLK 000:B:GPIO27;001:O:SPI0_CLK;010:O:SNFI_CLK
10:8	GPIO26	SRW	Aux mode of PAD_SPI0_MOSI 000:B:GPIO26;001:B0:SPI0_MOSI;010:B0:SNFI_MOSI
6:4	GPIO25	SRW	Aux mode of PAD_SPI0_MISO 000:B:GPIO25;001:B0:SPI0_MISO;010:B0:SNFI_MISO
2:0	GPIO24	SRW	Aux mode of PAD_SPI0_CSB 000:B:GPIO24;001:O:SPI0_CSB;010:O:SNFI_CS

1001F340	GPIO_MODE4				Aux mode of PAD_SPI2_CLK								11111111			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO39					GPIO38					GPIO37				GPIO36	
Type	RW					RW					RW				RW	
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO35					GPIO34					GPIO33				GPIO32	
Type	RW					RW					RW				RW	
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Name	Secure	Description
30:28	GPIO39	SRW	Aux mode of PAD_EMMC_DSL 000:B:GPIO39;001:B0:EMMC_DSL
26:24	GPIO38	SRW	Aux mode of PAD_EMMC_RSTB 000:B:GPIO38;001:O:EMMC_RSTB
22:20	GPIO37	SRW	Aux mode of PAD_SPI2_WP 000:B:GPIO37;001:B0:SPI2_WP;101:B1:EMMC_CK
18:16	GPIO36	SRW	Aux mode of PAD_SPI2_HOLD 000:B:GPIO36;001:B0:SPI2_HOLD;101:B1:EMMC_CMD
14:12	GPIO35	SRW	Aux mode of PAD_SPI2_CSB 000:B:GPIO35;001:O:SPI2_CSB;010:O:UART1_RTS;011:O:UART2_RTS;101:B1:EMMC_DATA_0
10:8	GPIO34	SRW	Aux mode of PAD_SPI2_MISO 000:B:GPIO34;001:B0:SPI2_MISO;010:I1:UART1_CTS;011:I1:UART2_CTS;101:B1:EMMC_DATA_1
6:4	GPIO33	SRW	Aux mode of PAD_SPI2_MOSI 000:B:GPIO33;001:B0:SPI2_MOSI;010:O:UART1_TXD;011:O:UART2_TXD;101:B1:EMMC_DATA_2
2:0	GPIO32	SRW	Aux mode of PAD_SPI2_CLK 000:B:GPIO32;001:O:SPI2_CLK;010:I1:UART1_RXD;011:I1:UART2_RXD;101:B1:EMMC_DATA_3

1001F350 GPIO_MODE5 Aux mode of PAD_EMMC_CK 11111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO47				GPIO46				GPIO45				GPIO44		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO43				GPIO42				GPIO41				GPIO40		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Name	Secure	Description
30:28	GPIO47	SRW	Aux mode of PAD_EMMC_DATA_2 000:B:GPIO47;001:B1:EMMC_DATA_2
26:24	GPIO46	SRW	Aux mode of PAD_EMMC_DATA_3 000:B:GPIO46;001:B1:EMMC_DATA_3
22:20	GPIO45	SRW	Aux mode of PAD_EMMC_DATA_4 000:B:GPIO45;001:B1:EMMC_DATA_4
18:16	GPIO44	SRW	Aux mode of PAD_EMMC_DATA_5 000:B:GPIO44;001:B1:EMMC_DATA_5
14:12	GPIO43	SRW	Aux mode of PAD_EMMC_DATA_6 000:B:GPIO43;001:B1:EMMC_DATA_6
10:8	GPIO42	SRW	Aux mode of PAD_EMMC_DATA_7 000:B:GPIO42;001:B1:EMMC_DATA_7
6:4	GPIO41	SRW	Aux mode of PAD_EMMC_CMD 000:B:GPIO41;001:B1:EMMC_CMD
2:0	GPIO40	SRW	Aux mode of PAD_EMMC_CK 000:B:GPIO40;001:B1:EMMC_CK

1001F360	GPIO_MODE6				Aux mode of PAD_EMMC_DATA_1								11111111			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO55					GPIO54					GPIO53				GPIO52	
Type	RW					RW					RW				RW	
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO51					GPIO50					GPIO49				GPIO48	
Type	RW					RW					RW				RW	
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Name	Secure	Description
30:28	GPIO55	SRW	Aux mode of PAD_UART0_RXD 000:B:GPIO55;001:I1:UART0_RXD
26:24	GPIO54	SRW	Aux mode of PAD_PCM_MCK_I2S_MCLK 000:B:GPIO54;001:O:PCM_MCK_I2S_MCLK
22:20	GPIO53	SRW	Aux mode of PAD_PCM_DTX_I2S_DOUT 000:B:GPIO53;001:O:PCM_DTX_I2S_DOUT;010:O:UART2_RTS
18:16	GPIO52	SRW	Aux mode of PAD_PCM_DRX_I2S_DIN 000:B:GPIO52;001:I0:PCM_DRX_I2S_DIN;010:I1:UART2_CTS
14:12	GPIO51	SRW	Aux mode of PAD_PCM_CLK_I2S_BCLK 000:B:GPIO51;001:O:PCM_CLK_I2S_BCLK;010:O:UART2_TXD
10:8	GPIO50	SRW	Aux mode of PAD_PCM_FS_I2S_LRCK 000:B:GPIO50;001:O:PCM_FS_I2S_LRCK;010:I1:UART2_RXD
6:4	GPIO49	SRW	Aux mode of PAD_EMMC_DATA_0 000:B:GPIO49;001:B1:EMMC_DATA_0
2:0	GPIO48	SRW	Aux mode of PAD_EMMC_DATA_1 000:B:GPIO48;001:B1:EMMC_DATA_1

1001F370 GPIO_MODE7 Aux mode of PAD_UART0_TXD 11111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO63					GPIO62					GPIO61				GPIO60	
Type	RW					RW					RW				RW	
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO59					GPIO58					GPIO57				GPIO56	
Type	RW					RW					RW				RW	
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Name	Secure	Description
30:28	GPIO63	SRW	Aux mode of PAD_USB_DRV_VBUS_P1 000:B:GPIO63;001:O:USB_DRV_VBUS_P1
26:24	GPIO62	SRW	Aux mode of PAD_JTAG_JTRST_N 000:B:GPIO62;001:I0:JTAG_JTRST_N;101:O:PWMD6;110:O:2P5G_LED1_P0
22:20	GPIO61	SRW	Aux mode of PAD_JTAG_JTCLK 000:B:GPIO61;001:I1:JTAG_JTCLK;010:O:UART1_RTS;011:O:UART2_RTS;101:O:PWMD5;110:O:GBE_LED1_P3
18:16	GPIO60	SRW	Aux mode of PAD_JTAG_JTMS 000:B:GPIO60;001:B1:JTAG_JTMS;010:I1:UART1_CTS;011:I1:UART2_CTS;101:O:PWMD4;110:O:GBE_LED1_P2
14:12	GPIO59	SRW	Aux mode of PAD_JTAG_JTDO 000:B:GPIO59;001:O:JTAG_JTDO;010:O:UART1_TXD;011:O:UART2_TXD;101:O:PWMD3;110:O:GBE_LED1_P1
10:8	GPIO58	SRW	Aux mode of PAD_JTAG_JTDI 000:B:GPIO58;001:I1:JTAG_JTDI;010:I1:UART1_RXD;011:I1:UART2_RXD;101:O:PWMD2;110:O:GBE_LED1_P0
6:4	GPIO57	SRW	Aux mode of PAD_PWMD0 000:B:GPIO57;001:O:PWMD0
2:0	GPIO56	SRW	Aux mode of PAD_UART0_TXD 000:B:GPIO56;001:O:UART0_TXD

1001F380	GPIO_MODE8				Aux mode of PAD_LED_A								11111111			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO71					GPIO70					GPIO69				GPIO68	
Type	RW					RW					RW				RW	
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO67					GPIO66					GPIO65				GPIO64	
Type	RW					RW					RW				RW	
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Name	Secure	Description
30:28	GPIO71	SRW	Aux mode of PAD_I2C_2_SCL 000:B:GPIO71;001:B1:I2C_2_SCL
26:24	GPIO70	SRW	Aux mode of PAD_GPIO_C 000:B:GPIO70;001:B1:SMI_0_MDIO;010:B1:I2C_1_SDA;011:O:P WMD7;100:B1:I2C_2_SDA
22:20	GPIO69	SRW	Aux mode of PAD_GPIO_B 000:B:GPIO69;001:O:SMI_0_MDC;010:B1:I2C_1_SCL;011:O:PWM D6;100:B1:I2C_2_SCL
18:16	GPIO68	SRW	Aux mode of PAD_LED_E 000:B:GPIO68;001:O:2P5G_LED0_P0
14:12	GPIO67	SRW	Aux mode of PAD_LED_D 000:B:GPIO67;001:O:GBE_LED0_P3
10:8	GPIO66	SRW	Aux mode of PAD_LED_C 000:B:GPIO66;001:O:GBE_LED0_P2
6:4	GPIO65	SRW	Aux mode of PAD_LED_B 000:B:GPIO65;001:O:GBE_LED0_P1
2:0	GPIO64	SRW	Aux mode of PAD_LED_A 000:B:GPIO64;001:O:GBE_LED0_P0

1001F390 GPIO_MODE9 Aux mode of PAD_I2C_2_SDA 11111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO79					GPIO78					GPIO77				GPIO76
Type		RW					RW					RW				RW
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO75					GPIO74					GPIO73				GPIO72
Type		RW					RW					RW				RW
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Name	Secure	Description
30:28	GPIO79	SRW	Aux mode of PAD_USB_DRV_VBUS_P0 000:B:GPIO79;001:O:USB_DRV_VBUS_P0
26:24	GPIO78	SRW	Aux mode of PAD_PCIE30_1L_0_CLKREQ_N 000:B:GPIO78;001:B1:PCIE30_1L_0_CLKREQ_N
22:20	GPIO77	SRW	Aux mode of PAD_PCIE30_1L_0_WAKE_N 000:B:GPIO77;001:I1:PCIE30_1L_0_WAKE_N
18:16	GPIO76	SRW	Aux mode of PAD_PCIE30_2L_1_CLKREQ_N 000:B:GPIO76;001:B1:PCIE30_2L_1_CLKREQ_N
14:12	GPIO75	SRW	Aux mode of PAD_PCIE30_2L_1_WAKE_N 000:B:GPIO75;001:I1:PCIE30_2L_1_WAKE_N
10:8	GPIO74	SRW	Aux mode of PAD_PCIE30_1L_0_PRESET_N 000:B:GPIO74;001:O:PCIE30_1L_0_PRESET_N
6:4	GPIO73	SRW	Aux mode of PAD_PCIE30_2L_1_PRESET_N 000:B:GPIO73;001:O:PCIE30_2L_1_PRESET_N
2:0	GPIO72	SRW	Aux mode of PAD_I2C_2_SDA 000:B:GPIO72;001:B1:I2C_2_SDA

1001F3A0 GPIO_MODE10 Aux mode of PAD_UART1_RXD 00001111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO87				GPIO86				GPIO85				GPIO84		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO83				GPIO82				GPIO81				GPIO80		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Name	Secure	Description
30:28	GPIO87	SRW	Aux mode of Reserved 000:Reserved
26:24	GPIO86	SRW	Aux mode of Reserved 000:Reserved
22:20	GPIO85	SRW	Aux mode of Reserved 000:Reserved
18:16	GPIO84	SRW	Aux mode of Reserved 000:Reserved
14:12	GPIO83	SRW	Aux mode of PAD_UART1_RTS 000:B:GPIO83;001:O:UART1_RTS;010:O:PWMD5
10:8	GPIO82	SRW	Aux mode of PAD_UART1_CTS 000:B:GPIO82;001:I1:UART1_CTS;010:O:PWMD4
6:4	GPIO81	SRW	Aux mode of PAD_UART1_TXD 000:B:GPIO81;001:O:UART1_TXD;010:O:PWMD3
2:0	GPIO80	SRW	Aux mode of PAD_UART1_RXD 000:B:GPIO80;001:I1:UART1_RXD;010:O:PWMD2

1001F304 GPIO_MODE0_SET Bitwise SET of Aux mode of PAD_UART2_RXD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO7					GPIO6					GPIO5				GPIO4	
Type	WO					WO					WO				WO	
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO3					GPIO2					GPIO1				GPIO0	
Type	WO					WO					WO				WO	
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO7	SW	Bitwise SET of Aux mode of PAD_PCIE30_2L_0_WAKE_N 0: Keep; 1: SET bit
26:24	GPIO6	SW	Bitwise SET of Aux mode of PAD_SMI_0_MDIO 0: Keep; 1: SET bit
22:20	GPIO5	SW	Bitwise SET of Aux mode of PAD_SMI_0_MDC 0: Keep; 1: SET bit
18:16	GPIO4	SW	Bitwise SET of Aux mode of PAD_GPIO_A 0: Keep; 1: SET bit
14:12	GPIO3	SW	Bitwise SET of Aux mode of PAD_UART2_RTS 0: Keep; 1: SET bit
10:8	GPIO2	SW	Bitwise SET of Aux mode of PAD_UART2_CTS 0: Keep; 1: SET bit
6:4	GPIO1	SW	Bitwise SET of Aux mode of PAD_UART2_TXD 0: Keep; 1: SET bit
2:0	GPIO0	SW	Bitwise SET of Aux mode of PAD_UART2_RXD 0: Keep; 1: SET bit

1001F314 GPIO_MODE1_SETBitwise SET of Aux mode of
PAD_PCIE30_2L_0_CLKREQ_N

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO15					GPIO14					GPIO13				GPIO12
Type		WO					WO					WO				WO
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO11					GPIO10					GPIO9				GPIO8
Type		WO					WO					WO				WO
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO15	SW	Bitwise SET of Aux mode of PAD_PMIC_I2C_SCL 0: Keep; 1: SET bit
26:24	GPIO14	SW	Bitwise SET of Aux mode of PAD_GPIO_WPS 0: Keep; 1: SET bit
22:20	GPIO13	SW	Bitwise SET of Aux mode of PAD_GPIO_RESET 0: Keep; 1: SET bit
18:16	GPIO12	SW	Bitwise SET of Aux mode of PAD_WATCHDOG 0: Keep; 1: SET bit
14:12	GPIO11	SW	Bitwise SET of Aux mode of PAD_GPIO_P 0: Keep; 1: SET bit
10:8	GPIO10	SW	Bitwise SET of Aux mode of PAD_PCIE30_1L_1_CLKREQ_N 0: Keep; 1: SET bit
6:4	GPIO9	SW	Bitwise SET of Aux mode of PAD_PCIE30_1L_1_WAKE_N 0: Keep; 1: SET bit
2:0	GPIO8	SW	Bitwise SET of Aux mode of PAD_PCIE30_2L_0_CLKREQ_N 0: Keep; 1: SET bit

1001F324 GPIO_MODE2_SET Bitwise SET of Aux mode of PAD_PMIC_I2C_SDA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO23					GPIO22					GPIO21				GPIO20
Type		WO					WO					WO				WO
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO19					GPIO18					GPIO17				GPIO16
Type		WO					WO					WO				WO
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO23	SW	Bitwise SET of Aux mode of PAD_SPI0_HOLD 0: Keep; 1: SET bit
26:24	GPIO22	SW	Bitwise SET of Aux mode of PAD_SPI0_WP 0: Keep; 1: SET bit
22:20	GPIO21	SW	Bitwise SET of Aux mode of PAD_PWMD1 0: Keep; 1: SET bit
18:16	GPIO20	SW	Bitwise SET of Aux mode of PAD_PCIE30_1L_1_PRESET_N 0: Keep; 1: SET bit
14:12	GPIO19	SW	Bitwise SET of Aux mode of PAD_PCIE30_2L_0_PRESET_N 0: Keep; 1: SET bit
10:8	GPIO18	SW	Bitwise SET of Aux mode of PAD_I2C_1_SDA 0: Keep; 1: SET bit
6:4	GPIO17	SW	Bitwise SET of Aux mode of PAD_I2C_1_SCL 0: Keep; 1: SET bit
2:0	GPIO16	SW	Bitwise SET of Aux mode of PAD_PMIC_I2C_SDA 0: Keep; 1: SET bit

1001F334 **GPIO_MODE3_SET** Bitwise SET of Aux mode of PAD_SPI0_CSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO31				GPIO30				GPIO29				GPIO28		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO27				GPIO26				GPIO25				GPIO24		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO31	SW	Bitwise SET of Aux mode of PAD_SPI1_CLK 0: Keep; 1: SET bit
26:24	GPIO30	SW	Bitwise SET of Aux mode of PAD_SPI1_MOSI 0: Keep; 1: SET bit
22:20	GPIO29	SW	Bitwise SET of Aux mode of PAD_SPI1_MISO 0: Keep; 1: SET bit
18:16	GPIO28	SW	Bitwise SET of Aux mode of PAD_SPI1_CSB 0: Keep; 1: SET bit
14:12	GPIO27	SW	Bitwise SET of Aux mode of PAD_SPI0_CLK 0: Keep; 1: SET bit
10:8	GPIO26	SW	Bitwise SET of Aux mode of PAD_SPI0_MOSI 0: Keep; 1: SET bit
6:4	GPIO25	SW	Bitwise SET of Aux mode of PAD_SPI0_MISO 0: Keep; 1: SET bit
2:0	GPIO24	SW	Bitwise SET of Aux mode of PAD_SPI0_CSB 0: Keep; 1: SET bit

1001F344 GPIO_MODE4_SET Bitwise SET of Aux mode of PAD_SPI2_CLK 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO39					GPIO38					GPIO37				GPIO36
Type		WO					WO					WO				WO
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO35					GPIO34					GPIO33				GPIO32
Type		WO					WO					WO				WO
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO39	SW	Bitwise SET of Aux mode of PAD_EMMC_DSL 0: Keep; 1: SET bit
26:24	GPIO38	SW	Bitwise SET of Aux mode of PAD_EMMC_RSTB 0: Keep; 1: SET bit
22:20	GPIO37	SW	Bitwise SET of Aux mode of PAD_SPI2_WP 0: Keep; 1: SET bit
18:16	GPIO36	SW	Bitwise SET of Aux mode of PAD_SPI2_HOLD 0: Keep; 1: SET bit
14:12	GPIO35	SW	Bitwise SET of Aux mode of PAD_SPI2_CSB 0: Keep; 1: SET bit
10:8	GPIO34	SW	Bitwise SET of Aux mode of PAD_SPI2_MISO 0: Keep; 1: SET bit
6:4	GPIO33	SW	Bitwise SET of Aux mode of PAD_SPI2_MOSI 0: Keep; 1: SET bit
2:0	GPIO32	SW	Bitwise SET of Aux mode of PAD_SPI2_CLK 0: Keep; 1: SET bit

1001F354 GPIO_MODE5_SET Bitwise SET of Aux mode of PAD_EMMC_CK 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO47					GPIO46					GPIO45				GPIO44
Type		WO					WO					WO				WO
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO43					GPIO42					GPIO41				GPIO40
Type		WO					WO					WO				WO
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO47	SW	Bitwise SET of Aux mode of PAD_EMMC_DATA_2 0: Keep; 1: SET bit
26:24	GPIO46	SW	Bitwise SET of Aux mode of PAD_EMMC_DATA_3 0: Keep; 1: SET bit
22:20	GPIO45	SW	Bitwise SET of Aux mode of PAD_EMMC_DATA_4 0: Keep; 1: SET bit
18:16	GPIO44	SW	Bitwise SET of Aux mode of PAD_EMMC_DATA_5 0: Keep; 1: SET bit
14:12	GPIO43	SW	Bitwise SET of Aux mode of PAD_EMMC_DATA_6 0: Keep; 1: SET bit
10:8	GPIO42	SW	Bitwise SET of Aux mode of PAD_EMMC_DATA_7 0: Keep; 1: SET bit
6:4	GPIO41	SW	Bitwise SET of Aux mode of PAD_EMMC_CMD 0: Keep; 1: SET bit
2:0	GPIO40	SW	Bitwise SET of Aux mode of PAD_EMMC_CK 0: Keep; 1: SET bit

1001F364 **GPIO_MODE6_SET** Bitwise SET of Aux mode of PAD_EMMC_DATA_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO55				GPIO54				GPIO53				GPIO52		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO51				GPIO50				GPIO49				GPIO48		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO55	SW	Bitwise SET of Aux mode of PAD_UART0_RXD 0: Keep; 1: SET bit
26:24	GPIO54	SW	Bitwise SET of Aux mode of PAD_PCM_MCK_I2S_MCLK 0: Keep; 1: SET bit
22:20	GPIO53	SW	Bitwise SET of Aux mode of PAD_PCM_DTX_I2S_DOUT 0: Keep; 1: SET bit
18:16	GPIO52	SW	Bitwise SET of Aux mode of PAD_PCM_DRX_I2S_DIN 0: Keep; 1: SET bit
14:12	GPIO51	SW	Bitwise SET of Aux mode of PAD_PCM_CLK_I2S_BCLK 0: Keep; 1: SET bit
10:8	GPIO50	SW	Bitwise SET of Aux mode of PAD_PCM_FS_I2S_LRCK 0: Keep; 1: SET bit
6:4	GPIO49	SW	Bitwise SET of Aux mode of PAD_EMMC_DATA_0 0: Keep; 1: SET bit
2:0	GPIO48	SW	Bitwise SET of Aux mode of PAD_EMMC_DATA_1 0: Keep; 1: SET bit

1001F374 GPIO_MODE7_SET Bitwise SET of Aux mode of PAD_UART0_TXD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO63					GPIO62					GPIO61				GPIO60
Type		WO					WO					WO				WO
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO59					GPIO58					GPIO57				GPIO56
Type		WO					WO					WO				WO
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO63	SW	Bitwise SET of Aux mode of PAD_USB_DRV_VBUS_P1 0: Keep; 1: SET bit
26:24	GPIO62	SW	Bitwise SET of Aux mode of PAD_JTAG_JTRST_N 0: Keep; 1: SET bit
22:20	GPIO61	SW	Bitwise SET of Aux mode of PAD_JTAG_JTCLK 0: Keep; 1: SET bit
18:16	GPIO60	SW	Bitwise SET of Aux mode of PAD_JTAG_JTMS 0: Keep; 1: SET bit
14:12	GPIO59	SW	Bitwise SET of Aux mode of PAD_JTAG_JTDO 0: Keep; 1: SET bit
10:8	GPIO58	SW	Bitwise SET of Aux mode of PAD_JTAG_JTDI 0: Keep; 1: SET bit
6:4	GPIO57	SW	Bitwise SET of Aux mode of PAD_PWMD0 0: Keep; 1: SET bit
2:0	GPIO56	SW	Bitwise SET of Aux mode of PAD_UART0_TXD 0: Keep; 1: SET bit

1001F384 GPIO_MODE8_SET Bitwise SET of Aux mode of PAD_LED_A 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO71				GPIO70				GPIO69				GPIO68		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO67				GPIO66				GPIO65				GPIO64		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO71	SW	Bitwise SET of Aux mode of PAD_I2C_2_SCL 0: Keep; 1: SET bit
26:24	GPIO70	SW	Bitwise SET of Aux mode of PAD_GPIO_C 0: Keep; 1: SET bit
22:20	GPIO69	SW	Bitwise SET of Aux mode of PAD_GPIO_B 0: Keep; 1: SET bit
18:16	GPIO68	SW	Bitwise SET of Aux mode of PAD_LED_E 0: Keep; 1: SET bit
14:12	GPIO67	SW	Bitwise SET of Aux mode of PAD_LED_D 0: Keep; 1: SET bit
10:8	GPIO66	SW	Bitwise SET of Aux mode of PAD_LED_C 0: Keep; 1: SET bit
6:4	GPIO65	SW	Bitwise SET of Aux mode of PAD_LED_B 0: Keep; 1: SET bit
2:0	GPIO64	SW	Bitwise SET of Aux mode of PAD_LED_A 0: Keep; 1: SET bit

1001F394 GPIO_MODE9_SET Bitwise SET of Aux mode of PAD_I2C_2_SDA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO79					GPIO78					GPIO77				GPIO76	
Type	WO					WO					WO				WO	
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO75					GPIO74					GPIO73				GPIO72	
Type	WO					WO					WO				WO	
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO79	SW	Bitwise SET of Aux mode of PAD_USB_DRV_VBUS_P0 0: Keep; 1: SET bit
26:24	GPIO78	SW	Bitwise SET of Aux mode of PAD_PCIE30_1L_0_CLKREQ_N 0: Keep; 1: SET bit
22:20	GPIO77	SW	Bitwise SET of Aux mode of PAD_PCIE30_1L_0_WAKE_N 0: Keep; 1: SET bit
18:16	GPIO76	SW	Bitwise SET of Aux mode of PAD_PCIE30_2L_1_CLKREQ_N 0: Keep; 1: SET bit
14:12	GPIO75	SW	Bitwise SET of Aux mode of PAD_PCIE30_2L_1_WAKE_N 0: Keep; 1: SET bit
10:8	GPIO74	SW	Bitwise SET of Aux mode of PAD_PCIE30_1L_0_PRESET_N 0: Keep; 1: SET bit
6:4	GPIO73	SW	Bitwise SET of Aux mode of PAD_PCIE30_2L_1_PRESET_N 0: Keep; 1: SET bit
2:0	GPIO72	SW	Bitwise SET of Aux mode of PAD_I2C_2_SDA 0: Keep; 1: SET bit

1001F3A4 **GPIO_MODE10_SET** Bitwise SET of Aux mode of PAD_UART1_RXD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO87				GPIO86				GPIO85				GPIO84		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO83				GPIO82				GPIO81				GPIO80		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO87	SW	Bitwise SET of Aux mode of Reserved 0: Keep; 1: SET bit
26:24	GPIO86	SW	Bitwise SET of Aux mode of Reserved 0: Keep; 1: SET bit
22:20	GPIO85	SW	Bitwise SET of Aux mode of Reserved 0: Keep; 1: SET bit
18:16	GPIO84	SW	Bitwise SET of Aux mode of Reserved 0: Keep; 1: SET bit
14:12	GPIO83	SW	Bitwise SET of Aux mode of PAD_UART1_RTS 0: Keep; 1: SET bit
10:8	GPIO82	SW	Bitwise SET of Aux mode of PAD_UART1_CTS 0: Keep; 1: SET bit
6:4	GPIO81	SW	Bitwise SET of Aux mode of PAD_UART1_TXD 0: Keep; 1: SET bit
2:0	GPIO80	SW	Bitwise SET of Aux mode of PAD_UART1_RXD 0: Keep; 1: SET bit

1001F308 GPIO_MODE0_CLR Bitwise clear of Aux mode of PAD_UART2_RXD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO7					GPIO6					GPIO5				GPIO4	
Type	WO					WO					WO				WO	
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO3					GPIO2					GPIO1				GPIO0	
Type	WO					WO					WO				WO	
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO7	SW	Bitwise clear of Aux mode of PAD_PCIE30_2L_0_WAKE_N 0: Keep; 1: Clear bit
26:24	GPIO6	SW	Bitwise clear of Aux mode of PAD_SMI_0_MDIO 0: Keep; 1: Clear bit
22:20	GPIO5	SW	Bitwise clear of Aux mode of PAD_SMI_0_MDC 0: Keep; 1: Clear bit
18:16	GPIO4	SW	Bitwise clear of Aux mode of PAD_GPIO_A 0: Keep; 1: Clear bit
14:12	GPIO3	SW	Bitwise clear of Aux mode of PAD_UART2_RTS 0: Keep; 1: Clear bit
10:8	GPIO2	SW	Bitwise clear of Aux mode of PAD_UART2_CTS 0: Keep; 1: Clear bit
6:4	GPIO1	SW	Bitwise clear of Aux mode of PAD_UART2_TXD 0: Keep; 1: Clear bit
2:0	GPIO0	SW	Bitwise clear of Aux mode of PAD_UART2_RXD 0: Keep; 1: Clear bit

1001F318

GPIO_MODE1_CLR

Bitwise clear of Aux mode of
PAD_PCIE30_2L_0_CLKREQ_N

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name		GPIO15					GPIO14				GPIO13				GPIO12		
Type		WO					WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name		GPIO11					GPIO10				GPIO9				GPIO8		
Type		WO					WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0	

Bit(s)	Name	Secure	Description
30:28	GPIO15	SW	Bitwise clear of Aux mode of PAD_PMIC_I2C_SCL 0: Keep; 1: Clear bit
26:24	GPIO14	SW	Bitwise clear of Aux mode of PAD_GPIO_WPS 0: Keep; 1: Clear bit
22:20	GPIO13	SW	Bitwise clear of Aux mode of PAD_GPIO_RESET 0: Keep; 1: Clear bit
18:16	GPIO12	SW	Bitwise clear of Aux mode of PAD_WATCHDOG 0: Keep; 1: Clear bit
14:12	GPIO11	SW	Bitwise clear of Aux mode of PAD_GPIO_P 0: Keep; 1: Clear bit
10:8	GPIO10	SW	Bitwise clear of Aux mode of PAD_PCIE30_1L_1_CLKREQ_N 0: Keep; 1: Clear bit
6:4	GPIO9	SW	Bitwise clear of Aux mode of PAD_PCIE30_1L_1_WAKE_N 0: Keep; 1: Clear bit
2:0	GPIO8	SW	Bitwise clear of Aux mode of PAD_PCIE30_2L_0_CLKREQ_N 0: Keep; 1: Clear bit

1001F328

GPIO_MODE2_CLR

Bitwise clear of Aux mode of
PAD_PMIC_I2C_SDA

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO23				GPIO22				GPIO21				GPIO20		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO19				GPIO18				GPIO17				GPIO16		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO23	SW	Bitwise clear of Aux mode of PAD_SPI0_HOLD 0: Keep; 1: Clear bit
26:24	GPIO22	SW	Bitwise clear of Aux mode of PAD_SPI0_WP 0: Keep; 1: Clear bit
22:20	GPIO21	SW	Bitwise clear of Aux mode of PAD_PWMD1 0: Keep; 1: Clear bit
18:16	GPIO20	SW	Bitwise clear of Aux mode of PAD_PCIE30_1L_1_PRESET_N 0: Keep; 1: Clear bit
14:12	GPIO19	SW	Bitwise clear of Aux mode of PAD_PCIE30_2L_0_PRESET_N 0: Keep; 1: Clear bit
10:8	GPIO18	SW	Bitwise clear of Aux mode of PAD_I2C_1_SDA 0: Keep; 1: Clear bit
6:4	GPIO17	SW	Bitwise clear of Aux mode of PAD_I2C_1_SCL 0: Keep; 1: Clear bit
2:0	GPIO16	SW	Bitwise clear of Aux mode of PAD_PMIC_I2C_SDA 0: Keep; 1: Clear bit

1001F338 GPIO_MODE3_CLR Bitwise clear of Aux mode of PAD_SPI0_CSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO31				GPIO30				GPIO29				GPIO28		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO27				GPIO26				GPIO25				GPIO24		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO31	SW	Bitwise clear of Aux mode of PAD_SPI1_CLK 0: Keep; 1: Clear bit
26:24	GPIO30	SW	Bitwise clear of Aux mode of PAD_SPI1_MOSI 0: Keep; 1: Clear bit
22:20	GPIO29	SW	Bitwise clear of Aux mode of PAD_SPI1_MISO 0: Keep; 1: Clear bit
18:16	GPIO28	SW	Bitwise clear of Aux mode of PAD_SPI1_CSB 0: Keep; 1: Clear bit
14:12	GPIO27	SW	Bitwise clear of Aux mode of PAD_SPI0_CLK 0: Keep; 1: Clear bit
10:8	GPIO26	SW	Bitwise clear of Aux mode of PAD_SPI0_MOSI 0: Keep; 1: Clear bit
6:4	GPIO25	SW	Bitwise clear of Aux mode of PAD_SPI0_MISO 0: Keep; 1: Clear bit
2:0	GPIO24	SW	Bitwise clear of Aux mode of PAD_SPI0_CSB 0: Keep; 1: Clear bit

1001F348 GPIO_MODE4_CLR Bitwise clear of Aux mode of PAD_SPI2_CLK 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO39					GPIO38					GPIO37				GPIO36	
Type	WO					WO					WO				WO	
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO35					GPIO34					GPIO33				GPIO32	
Type	WO					WO					WO				WO	
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO39	SW	Bitwise clear of Aux mode of PAD_EMMC_DSL 0: Keep; 1: Clear bit
26:24	GPIO38	SW	Bitwise clear of Aux mode of PAD_EMMC_RSTB 0: Keep; 1: Clear bit
22:20	GPIO37	SW	Bitwise clear of Aux mode of PAD_SPI2_WP 0: Keep; 1: Clear bit
18:16	GPIO36	SW	Bitwise clear of Aux mode of PAD_SPI2_HOLD 0: Keep; 1: Clear bit
14:12	GPIO35	SW	Bitwise clear of Aux mode of PAD_SPI2_CSB 0: Keep; 1: Clear bit
10:8	GPIO34	SW	Bitwise clear of Aux mode of PAD_SPI2_MISO 0: Keep; 1: Clear bit
6:4	GPIO33	SW	Bitwise clear of Aux mode of PAD_SPI2_MOSI 0: Keep; 1: Clear bit
2:0	GPIO32	SW	Bitwise clear of Aux mode of PAD_SPI2_CLK 0: Keep; 1: Clear bit

1001F358 GPIO_MODE5_CLR Bitwise clear of Aux mode of PAD_EMMC_CK 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO47					GPIO46					GPIO45				GPIO44
Type		WO					WO					WO				WO
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO43					GPIO42					GPIO41				GPIO40
Type		WO					WO					WO				WO
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO47	SW	Bitwise clear of Aux mode of PAD_EMMC_DATA_2 0: Keep; 1: Clear bit
26:24	GPIO46	SW	Bitwise clear of Aux mode of PAD_EMMC_DATA_3 0: Keep; 1: Clear bit
22:20	GPIO45	SW	Bitwise clear of Aux mode of PAD_EMMC_DATA_4 0: Keep; 1: Clear bit
18:16	GPIO44	SW	Bitwise clear of Aux mode of PAD_EMMC_DATA_5 0: Keep; 1: Clear bit
14:12	GPIO43	SW	Bitwise clear of Aux mode of PAD_EMMC_DATA_6 0: Keep; 1: Clear bit
10:8	GPIO42	SW	Bitwise clear of Aux mode of PAD_EMMC_DATA_7 0: Keep; 1: Clear bit
6:4	GPIO41	SW	Bitwise clear of Aux mode of PAD_EMMC_CMD 0: Keep; 1: Clear bit
2:0	GPIO40	SW	Bitwise clear of Aux mode of PAD_EMMC_CK 0: Keep; 1: Clear bit

1001F368

GPIO_MODE6_CLR

Bitwise clear of Aux mode of
PAD_EMMC_DATA_1

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name		GPIO55					GPIO54				GPIO53				GPIO52		
Type		WO					WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name		GPIO51					GPIO50				GPIO49				GPIO48		
Type		WO					WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0	

Bit(s)	Name	Secure	Description
30:28	GPIO55	SW	Bitwise clear of Aux mode of PAD_UART0_RXD 0: Keep; 1: Clear bit
26:24	GPIO54	SW	Bitwise clear of Aux mode of PAD_PCM_MCK_I2S_MCLK 0: Keep; 1: Clear bit
22:20	GPIO53	SW	Bitwise clear of Aux mode of PAD_PCM_DTX_I2S_DOUT 0: Keep; 1: Clear bit
18:16	GPIO52	SW	Bitwise clear of Aux mode of PAD_PCM_DRX_I2S_DIN 0: Keep; 1: Clear bit
14:12	GPIO51	SW	Bitwise clear of Aux mode of PAD_PCM_CLK_I2S_BCLK 0: Keep; 1: Clear bit
10:8	GPIO50	SW	Bitwise clear of Aux mode of PAD_PCM_FS_I2S_LRCK 0: Keep; 1: Clear bit
6:4	GPIO49	SW	Bitwise clear of Aux mode of PAD_EMMC_DATA_0 0: Keep; 1: Clear bit
2:0	GPIO48	SW	Bitwise clear of Aux mode of PAD_EMMC_DATA_1 0: Keep; 1: Clear bit

1001F378 GPIO_MODE7_CLR Bitwise clear of Aux mode of PAD_UART0_TXD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO63					GPIO62					GPIO61				GPIO60
Type		WO					WO					WO				WO
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO59					GPIO58					GPIO57				GPIO56
Type		WO					WO					WO				WO
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO63	SW	Bitwise clear of Aux mode of PAD_USB_DRV_VBUS_P1 0: Keep; 1: Clear bit
26:24	GPIO62	SW	Bitwise clear of Aux mode of PAD_JTAG_JTRST_N 0: Keep; 1: Clear bit
22:20	GPIO61	SW	Bitwise clear of Aux mode of PAD_JTAG_JTCLK 0: Keep; 1: Clear bit
18:16	GPIO60	SW	Bitwise clear of Aux mode of PAD_JTAG_JTMS 0: Keep; 1: Clear bit
14:12	GPIO59	SW	Bitwise clear of Aux mode of PAD_JTAG_JTDO 0: Keep; 1: Clear bit
10:8	GPIO58	SW	Bitwise clear of Aux mode of PAD_JTAG_JTDI 0: Keep; 1: Clear bit
6:4	GPIO57	SW	Bitwise clear of Aux mode of PAD_PWMD0 0: Keep; 1: Clear bit
2:0	GPIO56	SW	Bitwise clear of Aux mode of PAD_UART0_TXD 0: Keep; 1: Clear bit

1001F388 **GPIO_MODE8_CLR** Bitwise clear of Aux mode of PAD_LED_A 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO71				GPIO70				GPIO69				GPIO68		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO67				GPIO66				GPIO65				GPIO64		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO71	SW	Bitwise clear of Aux mode of PAD_I2C_2_SCL 0: Keep; 1: Clear bit
26:24	GPIO70	SW	Bitwise clear of Aux mode of PAD_GPIO_C 0: Keep; 1: Clear bit
22:20	GPIO69	SW	Bitwise clear of Aux mode of PAD_GPIO_B 0: Keep; 1: Clear bit
18:16	GPIO68	SW	Bitwise clear of Aux mode of PAD_LED_E 0: Keep; 1: Clear bit
14:12	GPIO67	SW	Bitwise clear of Aux mode of PAD_LED_D 0: Keep; 1: Clear bit
10:8	GPIO66	SW	Bitwise clear of Aux mode of PAD_LED_C 0: Keep; 1: Clear bit
6:4	GPIO65	SW	Bitwise clear of Aux mode of PAD_LED_B 0: Keep; 1: Clear bit
2:0	GPIO64	SW	Bitwise clear of Aux mode of PAD_LED_A 0: Keep; 1: Clear bit

1001F398 GPIO_MODE9_CLR Bitwise clear of Aux mode of PAD_I2C_2_SDA 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO79					GPIO78					GPIO77				GPIO76	
Type	WO					WO					WO				WO	
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO75					GPIO74					GPIO73				GPIO72	
Type	WO					WO					WO				WO	
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO79	SW	Bitwise clear of Aux mode of PAD_USB_DRV_VBUS_P0 0: Keep; 1: Clear bit
26:24	GPIO78	SW	Bitwise clear of Aux mode of PAD_PCIE30_1L_0_CLKREQ_N 0: Keep; 1: Clear bit
22:20	GPIO77	SW	Bitwise clear of Aux mode of PAD_PCIE30_1L_0_WAKE_N 0: Keep; 1: Clear bit
18:16	GPIO76	SW	Bitwise clear of Aux mode of PAD_PCIE30_2L_1_CLKREQ_N 0: Keep; 1: Clear bit
14:12	GPIO75	SW	Bitwise clear of Aux mode of PAD_PCIE30_2L_1_WAKE_N 0: Keep; 1: Clear bit
10:8	GPIO74	SW	Bitwise clear of Aux mode of PAD_PCIE30_1L_0_PRESET_N 0: Keep; 1: Clear bit
6:4	GPIO73	SW	Bitwise clear of Aux mode of PAD_PCIE30_2L_1_PRESET_N 0: Keep; 1: Clear bit
2:0	GPIO72	SW	Bitwise clear of Aux mode of PAD_I2C_2_SDA 0: Keep; 1: Clear bit

1001F3A8 GPIO_MODE10_CLR Bitwise clear of Aux mode of PAD_UART1_RXD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO87				GPIO86				GPIO85				GPIO84		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO83				GPIO82				GPIO81				GPIO80		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO87	SW	Bitwise clear of Aux mode of Reserved 0: Keep; 1: Clear bit
26:24	GPIO86	SW	Bitwise clear of Aux mode of Reserved 0: Keep; 1: Clear bit
22:20	GPIO85	SW	Bitwise clear of Aux mode of Reserved 0: Keep; 1: Clear bit
18:16	GPIO84	SW	Bitwise clear of Aux mode of Reserved 0: Keep; 1: Clear bit
14:12	GPIO83	SW	Bitwise clear of Aux mode of PAD_UART1_RTS 0: Keep; 1: Clear bit
10:8	GPIO82	SW	Bitwise clear of Aux mode of PAD_UART1_CTS 0: Keep; 1: Clear bit
6:4	GPIO81	SW	Bitwise clear of Aux mode of PAD_UART1_TXD 0: Keep; 1: Clear bit
2:0	GPIO80	SW	Bitwise clear of Aux mode of PAD_UART1_RXD 0: Keep; 1: Clear bit

1001F30C

GPIO_MODE0_MOD

Alternative way to set Aux mode of
PAD_UART2_RXD

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO7				GPIO6				GPIO5				GPIO4			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO3				GPIO2				GPIO1				GPIO0			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO7	SW	Alternative way to set Aux mode of PAD_PCIE30_2L_0_WAKE_N [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
27:24	GPIO6	SW	Alternative way to set Aux mode of PAD_SMI_0_MDIO [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
23:20	GPIO5	SW	Alternative way to set Aux mode of PAD_SMI_0_MDC [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
19:16	GPIO4	SW	Alternative way to set Aux mode of PAD_GPIO_A [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
15:12	GPIO3	SW	Alternative way to set Aux mode of PAD_UART2_RTS [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
11:8	GPIO2	SW	Alternative way to set Aux mode of PAD_UART2_CTS [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
7:4	GPIO1	SW	Alternative way to set Aux mode of PAD_UART2_TXD [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
3:0	GPIO0	SW	Alternative way to set Aux mode of PAD_UART2_RXD [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.

1001F31C

GPIO_MODE1_MOD

Alternative way to set Aux mode of
PAD_PCIE30_2L_0_CLKREQ_N

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO15				GPIO14				GPIO13				GPIO12			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO11				GPIO10				GPIO9				GPIO8			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO15	SW	Alternative way to set Aux mode of PAD_PMIC_I2C_SCL [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
27:24	GPIO14	SW	Alternative way to set Aux mode of PAD_GPIO_WPS [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
23:20	GPIO13	SW	Alternative way to set Aux mode of PAD_GPIO_RESET [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
19:16	GPIO12	SW	Alternative way to set Aux mode of PAD_WATCHDOG [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
15:12	GPIO11	SW	Alternative way to set Aux mode of PAD_GPIO_P [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
11:8	GPIO10	SW	Alternative way to set Aux mode of PAD_PCIE30_1L_1_CLKREQ_N [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
7:4	GPIO9	SW	Alternative way to set Aux mode of PAD_PCIE30_1L_1_WAKE_N [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
3:0	GPIO8	SW	Alternative way to set Aux mode of PAD_PCIE30_2L_0_CLKREQ_N [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.

1001F32C

GPIO_MODE2_MOD

Alternative way to set Aux mode of

00000000

PAD_PMIC_I2C_SDA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO23				GPIO22				GPIO21				GPIO20			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO19				GPIO18				GPIO17				GPIO16			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO23	SW	Alternative way to set Aux mode of PAD_SPI0_HOLD [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
27:24	GPIO22	SW	Alternative way to set Aux mode of PAD_SPI0_WP [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
23:20	GPIO21	SW	Alternative way to set Aux mode of PAD_PWMD1 [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
19:16	GPIO20	SW	Alternative way to set Aux mode of PAD_PCIE30_1L_1_PRESET_N [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
15:12	GPIO19	SW	Alternative way to set Aux mode of PAD_PCIE30_2L_0_PRESET_N [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
11:8	GPIO18	SW	Alternative way to set Aux mode of PAD_I2C_1_SDA [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
7:4	GPIO17	SW	Alternative way to set Aux mode of PAD_I2C_1_SCL [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
3:0	GPIO16	SW	Alternative way to set Aux mode of PAD_PMIC_I2C_SDA [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.

1001F33C

GPIO_MODE3_MOD

Alternative way to set Aux mode of
PAD_SPI0_CSB

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31				GPIO30				GPIO29				GPIO28			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO27				GPIO26				GPIO25				GPIO24			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO31	SW	Alternative way to set Aux mode of PAD_SPI1_CLK [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
27:24	GPIO30	SW	Alternative way to set Aux mode of PAD_SPI1_MOSI [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
23:20	GPIO29	SW	Alternative way to set Aux mode of PAD_SPI1_MISO [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
19:16	GPIO28	SW	Alternative way to set Aux mode of PAD_SPI1_CSB [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
15:12	GPIO27	SW	Alternative way to set Aux mode of PAD_SPI0_CLK [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
11:8	GPIO26	SW	Alternative way to set Aux mode of PAD_SPI0_MOSI [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
7:4	GPIO25	SW	Alternative way to set Aux mode of PAD_SPI0_MISO [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
3:0	GPIO24	SW	Alternative way to set Aux mode of PAD_SPI0_CSB [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.

1001F34C

GPIO_MODE4_MOD

Alternative way to set Aux mode of
PAD_SPI2_CLK

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO39				GPIO38				GPIO37				GPIO36			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO35				GPIO34				GPIO33				GPIO32			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO39	SW	Alternative way to set Aux mode of PAD_EMMC_DSL [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
27:24	GPIO38	SW	Alternative way to set Aux mode of PAD_EMMC_RSTB [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
23:20	GPIO37	SW	Alternative way to set Aux mode of PAD_SPI2_WP [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
19:16	GPIO36	SW	Alternative way to set Aux mode of PAD_SPI2_HOLD [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
15:12	GPIO35	SW	Alternative way to set Aux mode of PAD_SPI2_CSB [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
11:8	GPIO34	SW	Alternative way to set Aux mode of PAD_SPI2_MISO [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
7:4	GPIO33	SW	Alternative way to set Aux mode of PAD_SPI2_MOSI [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
3:0	GPIO32	SW	Alternative way to set Aux mode of PAD_SPI2_CLK [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.

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GPIO_MODE5_MOD

Alternative way to set Aux mode of
PAD_EMMC_CK

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO47				GPIO46				GPIO45				GPIO44			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO43				GPIO42				GPIO41				GPIO40			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO47	SW	Alternative way to set Aux mode of PAD_EMMC_DATA_2 [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
27:24	GPIO46	SW	Alternative way to set Aux mode of PAD_EMMC_DATA_3 [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
23:20	GPIO45	SW	Alternative way to set Aux mode of PAD_EMMC_DATA_4 [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
19:16	GPIO44	SW	Alternative way to set Aux mode of PAD_EMMC_DATA_5 [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
15:12	GPIO43	SW	Alternative way to set Aux mode of PAD_EMMC_DATA_6 [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
11:8	GPIO42	SW	Alternative way to set Aux mode of PAD_EMMC_DATA_7 [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
7:4	GPIO41	SW	Alternative way to set Aux mode of PAD_EMMC_CMD [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
3:0	GPIO40	SW	Alternative way to set Aux mode of PAD_EMMC_CK [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.

1001F36C

GPIO_MODE6_MOD

Alternative way to set Aux mode of

00000000

PAD_EMMC_DATA_1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO55				GPIO54				GPIO53				GPIO52			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO51				GPIO50				GPIO49				GPIO48			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO55	SW	Alternative way to set Aux mode of PAD_UART0_RXD [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
27:24	GPIO54	SW	Alternative way to set Aux mode of PAD_PCM_MCK_I2S_MCLK [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
23:20	GPIO53	SW	Alternative way to set Aux mode of PAD_PCM_DTX_I2S_DOUT [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
19:16	GPIO52	SW	Alternative way to set Aux mode of PAD_PCM_DRX_I2S_DIN [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
15:12	GPIO51	SW	Alternative way to set Aux mode of PAD_PCM_CLK_I2S_BCLK [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
11:8	GPIO50	SW	Alternative way to set Aux mode of PAD_PCM_FS_I2S_LRCK [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
7:4	GPIO49	SW	Alternative way to set Aux mode of PAD_EMMC_DATA_0 [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
3:0	GPIO48	SW	Alternative way to set Aux mode of PAD_EMMC_DATA_1 [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.

1001F37C

GPIO_MODE7_MOD

Alternative way to set Aux mode of
PAD_UART0_TXD

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO63				GPIO62				GPIO61				GPIO60			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO59				GPIO58				GPIO57				GPIO56			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO63	SW	Alternative way to set Aux mode of PAD_USB_DRV_VBUS_P1 [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
27:24	GPIO62	SW	Alternative way to set Aux mode of PAD_JTAG_JTRST_N [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
23:20	GPIO61	SW	Alternative way to set Aux mode of PAD_JTAG_JTCLK [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
19:16	GPIO60	SW	Alternative way to set Aux mode of PAD_JTAG_JTMS [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
15:12	GPIO59	SW	Alternative way to set Aux mode of PAD_JTAG_JTDO [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
11:8	GPIO58	SW	Alternative way to set Aux mode of PAD_JTAG_JTDI [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
7:4	GPIO57	SW	Alternative way to set Aux mode of PAD_PWMD0 [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
3:0	GPIO56	SW	Alternative way to set Aux mode of PAD_UART0_TXD [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.

1001F38C GPIO_MODE8_MOD Alternative way to set Aux mode of PAD_LED_A 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO71				GPIO70				GPIO69				GPIO68			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO67				GPIO66				GPIO65				GPIO64			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO71	SW	Alternative way to set Aux mode of PAD_I2C_2_SCL [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
27:24	GPIO70	SW	Alternative way to set Aux mode of PAD_GPIO_C [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
23:20	GPIO69	SW	Alternative way to set Aux mode of PAD_GPIO_B [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
19:16	GPIO68	SW	Alternative way to set Aux mode of PAD_LED_E [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
15:12	GPIO67	SW	Alternative way to set Aux mode of PAD_LED_D [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
11:8	GPIO66	SW	Alternative way to set Aux mode of PAD_LED_C [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
7:4	GPIO65	SW	Alternative way to set Aux mode of PAD_LED_B [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
3:0	GPIO64	SW	Alternative way to set Aux mode of PAD_LED_A [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.

1001F39C

GPIO_MODE9_MOD

Alternative way to set Aux mode of
PAD_I2C_2_SDA

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO79				GPIO78				GPIO77				GPIO76			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO75				GPIO74				GPIO73				GPIO72			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO79	SW	Alternative way to set Aux mode of PAD_USB_DRV_VBUS_P0 [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
27:24	GPIO78	SW	Alternative way to set Aux mode of PAD_PCIE30_1L_0_CLKREQ_N [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
23:20	GPIO77	SW	Alternative way to set Aux mode of PAD_PCIE30_1L_0_WAKE_N [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
19:16	GPIO76	SW	Alternative way to set Aux mode of PAD_PCIE30_2L_1_CLKREQ_N [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
15:12	GPIO75	SW	Alternative way to set Aux mode of PAD_PCIE30_2L_1_WAKE_N [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
11:8	GPIO74	SW	Alternative way to set Aux mode of PAD_PCIE30_1L_0_PRESET_N [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
7:4	GPIO73	SW	Alternative way to set Aux mode of PAD_PCIE30_2L_1_PRESET_N [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
3:0	GPIO72	SW	Alternative way to set Aux mode of PAD_I2C_2_SDA [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.

1001F3AC

GPIO_MODE10_MOD

Alternative way to set Aux mode of
PAD_UART1_RXD

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO87				GPIO86				GPIO85				GPIO84			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO83				GPIO82				GPIO81				GPIO80			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO87	SW	Alternative way to set Aux mode of Reserved [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
27:24	GPIO86	SW	Alternative way to set Aux mode of Reserved [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
23:20	GPIO85	SW	Alternative way to set Aux mode of Reserved [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
19:16	GPIO84	SW	Alternative way to set Aux mode of Reserved [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
15:12	GPIO83	SW	Alternative way to set Aux mode of PAD_UART1_RTS [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
11:8	GPIO82	SW	Alternative way to set Aux mode of PAD_UART1_CTS [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
7:4	GPIO81	SW	Alternative way to set Aux mode of PAD_UART1_TXD [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.
3:0	GPIO80	SW	Alternative way to set Aux mode of PAD_UART1_RXD [2:0]: Target Aux. mode [3]: Enable mode setting 0: Mode is not set. 1: Mode is set.

1001F600 MISC Chip related misc options 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		Chip related misc options

1001F604 MISC SET Chip related misc options 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		Chip related misc options
			0: Keep; 1: SET bit

1001F608 MISC_CLR Chip related misc options 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		Chip related misc options
			0: Keep; 1: Clear bit

1001F6D0 DBG dbg_mon control bit 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dbg															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dbg															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	dbg		dbg_mon control bit

1001F6E0

BANK

GPIO reserved control register [0]:

00000000

test_normal_sel_bypreg

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	GPIO_REG		GPIO reserved control register [0]: test_normal_sel_bypreg

1001F6F0

TPBANK0

Trapping force enable

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rev1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRAP_LATCH				boot_mode		pkg_type	boot_clk sq_xtal	TRAP_FORCE_VAL				TRAP_FORCE_EN			
Type	RU				RU		RU	RU	RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:16	rev1		reserved bits
15:12	TRAP_LATCH		TRAP_LATCH value
11:10	boot_mode		boot_mode value
9	pkg_type		pkg_type value
8	boot_clk sq_xtal		boot_clk sq_xtal value
7:4	TRAP_FORCE_VAL		Trapping force value
3:0	TRAP_FORCE_EN		Trapping force enable

1001F710 AP_GOOD Chip related AP_GPPD control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		Chip related AP_GPPD control

1001F714 AP_GOOD_SET Chip related AP_GPPD control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		Chip related AP_GPPD control
			0: Keep; 1: SET bit

1001F718 AP_GOOD_CLR Chip related AP_GPPD control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		Chip related AP_GPPD control
			0: Keep; 1: Clear bit

1001F720 MODE_CFG_CT_REG GPIO reserved control register [0]:
test_normal_sel_bypreg 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		GPIO reserved control register [0]: test_normal_sel_bypreg

1001F724 MODE_CFG_CT_REG_SET GPIO reserved control register [0]:
test_normal_sel_bypreg 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		GPIO reserved control register [0]: test_normal_sel_bypreg 0: Keep; 1: SET bit

1001F728 MODE_CFG_CT_REG_CLR GPIO reserved control register [0]:
test_normal_sel_bypreg 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		GPIO reserved control register [0]: test_normal_sel_bypreg 0: Keep; 1: Clear bit

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