

# **MT7988A**

## **Wi-Fi 7 Generation Router**

### **Platform: Registers Part 2**

**Open Version**

**Part 1: Chapter 1 – Chapter 3**

**Part 2: Chapter 4**

**Version: 0.1**

**Release Date: 2023-10-18**

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## Version History

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| Version | Date       | Description     |
|---------|------------|-----------------|
| 0.1     | 2023-10-18 | Initial release |

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## 4 Connectivity

### 4.1 NETSYS

#### 4.1.1 Register Definition

Module name: ETHDMASYS\_SYSCTL Base address: (+0x1500\_0000)

| Address  | Name                      | Width | Register Function                           |
|----------|---------------------------|-------|---------------------------------------------|
| 1500000C | <u>REVISION_ID</u>        | 32    | ETHSYS revision identification              |
| 15000010 | <u>SYSCFG0</u>            | 32    | System configuration register 0             |
| 15000014 | <u>SYSCFG1</u>            | 32    | System configuration register 1             |
| 15000018 | <u>TESTSTAT0</u>          | 32    | Firmware test status 0                      |
| 1500001C | <u>TESTSTAT1</u>          | 32    | Firmware test status 1                      |
| 15000024 | <u>BOOT_RELEASE</u>       | 32    | Release CPU's command to boot from SRAM     |
| 1500002C | <u>CLKCFG0</u>            | 32    | Clock configuration register 0              |
| 15000030 | <u>CLKCFG1</u>            | 32    | Clock configuration register 1              |
| 15000034 | <u>RSTCTL</u>             | 32    | Reset control register                      |
| 15000038 | <u>RSTSTAT</u>            | 32    | Reset status register                       |
| 15000040 | <u>GPIO0_MODE</u>         | 32    | GPIO0 purpose selection                     |
| 15000044 | <u>GPIO1_MODE</u>         | 32    | GPIO1 purpose selection                     |
| 15000048 | <u>MEMO0</u>              | 32    | Memory0                                     |
| 1500004C | <u>MEMO1</u>              | 32    | Memory1                                     |
| 15000050 | <u>MEMO2</u>              | 32    | Memory2                                     |
| 15000054 | <u>MEMO3</u>              | 32    | Memory3                                     |
| 15000058 | <u>MEMO4</u>              | 32    | Memory4                                     |
| 1500005C | <u>MEMO5</u>              | 32    | Memory5                                     |
| 15000060 | <u>IOC_EN</u>             | 32    | NETSYS IO coherence enable register         |
| 15000064 | <u>BIST_CTRL</u>          | 32    | NETSYS Global BIST configuration register   |
| 15000068 | <u>BIST_NETSYS2EMI0</u>   | 32    | NETSYS2EMI_M0 BIST configuration register 0 |
| 1500006C | <u>BIST_NETSYS2EMI1</u>   | 32    | NETSYS2EMI_M0 BIST configuration register 1 |
| 15000070 | <u>BIST_NETSYS2EMI2</u>   | 32    | NETSYS2EMI_M1 BIST configuration register 0 |
| 15000074 | <u>BIST_NETSYS2EMI3</u>   | 32    | NETSYS2EMI_M1 BIST configuration register 1 |
| 15000078 | <u>BIST_NETSYS2INFRA0</u> | 32    | NETSYS2INFRA BIST configuration register 0  |
| 1500007C | <u>BIST_NETSYS2INFRA1</u> | 32    | NETSYS2INFRA BIST configuration register 1  |
| 15000080 | <u>AXICFG0</u>            | 32    | AXI sideband configuration register 0       |
| 15000084 | <u>AXICFG1</u>            | 32    | AXI sideband configuration register 1       |
| 15000088 | <u>GALSCFG0</u>           | 32    | GALS configuration register 0               |
| 1500008C | <u>GALSCFG1</u>           | 32    | GALS configuration register 1               |
| 15000090 | <u>MISTAT</u>             | 32    | NETSYS bus MI status register               |
| 15000094 | <u>SI0STAT0</u>           | 32    | NETSYS bus SI status register 0             |
| 15000098 | <u>SI0STAT1</u>           | 32    | NETSYS bus SI status register 1             |
| 1500009C | <u>SI0STAT2</u>           | 32    | NETSYS bus SI status register 2             |
| 150000A0 | <u>S2PSTAT0</u>           | 32    | NETSYS bus S2P status register 0            |
| 150000A4 | <u>S2PSTAT1</u>           | 32    | NETSYS bus S2P status register 1            |
| 150000A8 | <u>X2SSTAT0</u>           | 32    | NETSYS bus X2S status register 0            |
| 150000AC | <u>X2SSTAT1</u>           | 32    | NETSYS bus X2S status register 1            |
| 150000B0 | <u>R2XCFG0</u>            | 32    | R2X configuration register 0                |
| 150000B4 | <u>R2XCFG1</u>            | 32    | R2X configuration register 1                |



| Address  | Name                           | Width | Register Function                           |
|----------|--------------------------------|-------|---------------------------------------------|
| 150000B8 | <b><u>R2XSTAT0</u></b>         | 32    | R2X status register 0                       |
| 150000BC | <b><u>R2XSTAT1</u></b>         | 32    | R2X status register 1                       |
| 150000C0 | <b><u>APBCFG</u></b>           | 32    | NETSYS_APB configuration register           |
| 150000C4 | <b><u>APBSTAT</u></b>          | 32    | NETSYS_APB status register                  |
| 15000150 | <b><u>BIST_NETSYS2EMI4</u></b> | 32    | NETSYS2EMI_M2 BIST configuration register 0 |
| 15000154 | <b><u>BIST_NETSYS2EMI5</u></b> | 32    | NETSYS2EMI_M2 BIST configuration register 1 |
| 15000180 | <b><u>GALSCFG2</u></b>         | 32    | GALS configuration register 2               |
| 150001C0 | <b><u>SI0STAT3</u></b>         | 32    | NETSYS bus SI status register 3             |
| 150001C4 | <b><u>SI0STAT4</u></b>         | 32    | NETSYS bus SI status register 4             |
| 150001C8 | <b><u>SI0STAT5</u></b>         | 32    | NETSYS bus SI status register 5             |
| 150001CC | <b><u>SI0STAT6</u></b>         | 32    | NETSYS bus SI status register 6             |
| 150001D0 | <b><u>SI0STAT7</u></b>         | 32    | NETSYS bus SI status register 7             |

**1500000C**      **REVISION\_ID**      **ETHSYS revision identification**      **30000000**

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| Name  | ETHSYS_VER |    |    |    |    |    |    |    |               |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |               |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | ETHSYS_VER |    |    |    |    |    |    |    | ETHSYS_ECO_ID |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    | RO            |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                         |
|--------|---------------|-------------------------------------|
| 31:8   | ETHSYS_VER    | ETHSYS revision number              |
| 7:0    | ETHSYS_ECO_ID | ETHSYS ECO ID (IPM version in FPGA) |

**15000010**      **SYSCFG0**      **System configuration register 0**      **00000000**

| Bit   | 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TEST_CODE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |    |    |    |    |    |    |    |
| Bit   | 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| Bit(s) | Name      | Description                                                      |
|--------|-----------|------------------------------------------------------------------|
| 31:24  | TEST_CODE | Default value is from bootstrap and can be modified by software. |

**15000014      SYSCFG1      System configuration register 1      00110014**

| Bit   | 31       | 30 | 29       | 28 | 27       | 26 | 25              | 24              | 23              | 22   | 21 | 20 | 19 | 18 | 17       | 16 |
|-------|----------|----|----------|----|----------|----|-----------------|-----------------|-----------------|------|----|----|----|----|----------|----|
| Name  | RSV1     |    |          |    |          |    |                 |                 |                 |      |    |    |    |    | GE3_MODE |    |
| Type  | RW       |    |          |    |          |    |                 |                 |                 |      |    |    |    |    | RW       |    |
| Reset | 0        | 0  | 0        | 0  | 0        | 0  | 0               | 0               | 0               | 0    | 0  | 1  | 0  | 0  | 0        | 1  |
| Bit   | 15       | 14 | 13       | 12 | 11       | 10 | 9               | 8               | 7               | 6    | 5  | 4  | 3  | 2  | 1        | 0  |
| Name  | GE2_MODE |    | GE1_MODE |    | GE0_MODE |    | SGMII_CONFI_G_0 | SGMII_CONFI_G_1 | SGMII_CONFI_G_2 | RSV0 |    |    |    |    |          |    |
| Type  | RW       |    | RW       |    | RW       |    | RW              | RW              | RW              | RW   |    |    |    |    |          |    |
| Reset | 0        | 0  | 0        | 0  | 0        | 0  | 0               | 0               | 0               | 0    | 0  | 1  | 0  | 1  | 0        | 0  |

| Bit(s) | Name     | Description                                                                                                                                                                                                   |
|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:18  | RSV1     | <b>Reserved</b>                                                                                                                                                                                               |
| 17:16  | GE3_MODE | <b>Gigabit Port #3 Mode</b><br>Sets the interface mode on Gigabit port 3<br>0: RGMII Mode (10/100/1000 Mbps)<br>1: MII Mode (10/100 Mbps)<br>2: Reverse MII Mode (10/100 Mbps)<br>3: Reduced MII (10/100Mbps) |
| 15:14  | GE2_MODE | <b>Gigabit Port #2 Mode</b><br>Sets the interface mode on Gigabit port 2<br>0: RGMII Mode (10/100/1000 Mbps)<br>1: MII Mode (10/100 Mbps)<br>2: Reverse MII Mode (10/100 Mbps)<br>3: Reduced MII (10/100Mbps) |
| 13:12  | GE1_MODE | <b>Gigabit Port #1 Mode</b><br>Sets the interface mode on Gigabit port 1<br>0: RGMII Mode (10/100/1000 Mbps)<br>1: MII Mode (10/100 Mbps)<br>2: Reverse MII Mode (10/100 Mbps)<br>3: Reserved                 |
| 11:10  | GE0_MODE | <b>Gigabit Port #0 Mode</b><br>Sets the interface mode on Gigabit port 0<br>0: RGMII Mode (10/100/1000 Mbps)<br>1: MII Mode (10/100 Mbps)<br>2: Reverse MII Mode (10/100 Mbps)                                |

| Bit(s)      | Name           | Description                                                                  |
|-------------|----------------|------------------------------------------------------------------------------|
| 3: Reserved |                |                                                                              |
| 9           | SGMII_CONFIG_0 | <b>SGMII path enable of GMAC1</b><br><br>0: SGMII disable<br>1: SGMII enable |
| 8           | SGMII_CONFIG_1 | <b>SGMII path enable of GMAC2</b><br><br>0: SGMII disable<br>1: SGMII enable |
| 7           | SGMII_CONFIG_2 | <b>SGMII path enable of GMAC3</b><br><br>0: SGMII disable<br>1: SGMII enable |
| 6:0         | RSV0           | <b>Reserved</b>                                                              |

|          |           |    |    |                        |    |    |    |    |    |    |    |    |    |    |    |          |  |  |
|----------|-----------|----|----|------------------------|----|----|----|----|----|----|----|----|----|----|----|----------|--|--|
| 15000018 | TESTSTAT0 |    |    | Firmware test status 0 |    |    |    |    |    |    |    |    |    |    |    | 00000000 |  |  |
| Bit      | 31        | 30 | 29 | 28                     | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16       |  |  |
| Name     | TESTSTAT0 |    |    |                        |    |    |    |    |    |    |    |    |    |    |    |          |  |  |
| Type     | RW        |    |    |                        |    |    |    |    |    |    |    |    |    |    |    |          |  |  |
| Reset    | 0         | 0  | 0  | 0                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0        |  |  |
| Bit      | 15        | 14 | 13 | 12                     | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0        |  |  |
| Name     | TESTSTAT0 |    |    |                        |    |    |    |    |    |    |    |    |    |    |    |          |  |  |
| Type     | RW        |    |    |                        |    |    |    |    |    |    |    |    |    |    |    |          |  |  |
| Reset    | 0         | 0  | 0  | 0                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0        |  |  |

| Bit(s) | Name      | Description                                                                                          |
|--------|-----------|------------------------------------------------------------------------------------------------------|
| 31:0   | TESTSTAT0 | <b>Firmware Test Status Register 0</b><br><br>NOTE: This register is reset only by a power-on reset. |

1500001C      **TESTSTAT1**      Firmware test status 1      00000000

| Bit   | 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TESTSTAT1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TESTSTAT1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s)                                                 | Name      | Description                     |
|--------------------------------------------------------|-----------|---------------------------------|
| 31:0                                                   | TESTSTAT1 | Firmware Test Status Register 1 |
| NOTE: This register is reset only by a power-on reset. |           |                                 |

15000024      **BOOT\_RELEASE**      Release CPU's command to boot from SRAM      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | BOOT_RELEASE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | BOOT_RELEASE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description |
|--------|--------------|-------------|
| 31:0   | BOOT_RELEASE | Reserved    |

1500002C CLKCFG0 Clock configuration register 0 C4001FE0

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | OSC_1US_DIV |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1           | 1  | 0  | 0  | 0  | 1  |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:26  | OSC_1US_DIV | <p><b>Oscillator 1 usec Divider</b></p> <p>Sets the maximum for the reference clock counter for either a 20 MHz or 40 MHz external XTAL input. The count increments each 1usec (indicating 1 MHz), up to the maximum, before resetting to zero. This counts the frequency of an external XTAL. This count is used to output a 32 kHz frequency to the REFCLK0 pin.</p> <p>0: Automatically generates a 1 usec system tick regardless of whether XTAL frequency is 20 MHz or 40 MHz.</p> <p>49: Default value for a reference 50 MHz clock.</p> <p>39: Default value for an external 40 MHz XTAL.</p> <p>19: Default value for an external 20 MHz XTAL.</p> <p>Others: Manual mode for tick generation.</p> |

| 15000030 |               | CLKCFG1       |               |    | Clock configuration register 1 |            |    |            |            |           |    |    |    |             |             |             | FFFFFFF |  |
|----------|---------------|---------------|---------------|----|--------------------------------|------------|----|------------|------------|-----------|----|----|----|-------------|-------------|-------------|---------|--|
| Bit      | 31            | 30            | 29            | 28 | 27                             | 26         | 25 | 24         | 23         | 22        | 21 | 20 | 19 | 18          | 17          | 16          |         |  |
| Name     |               |               |               |    |                                |            |    |            |            |           |    |    |    |             |             | ESW_CLK_EN  |         |  |
| Type     |               |               |               |    |                                |            |    |            |            |           |    |    |    |             |             | RW          |         |  |
| Reset    |               |               |               |    |                                |            |    |            |            |           |    |    |    |             |             | 1           |         |  |
| Bit      | 15            | 14            | 13            | 12 | 11                             | 10         | 9  | 8          | 7          | 6         | 5  | 4  | 3  | 2           | 1           | 0           |         |  |
| Name     | WOCPU0_CLK_EN | WOCPU1_CLK_EN | WOCPU2_CLK_EN |    |                                | GP3_CLK_EN |    | GP1_CLK_EN | GP2_CLK_EN | FE_CLK_EN |    |    |    | XGP3_CLK_EN | XGP2_CLK_EN | XGP1_CLK_EN |         |  |
| Type     | RW            | RW            | RW            |    |                                | RW         |    | RW         | RW         | RW        |    |    |    | RW          | RW          | RW          |         |  |
| Reset    | 1             | 1             | 1             |    |                                | 1          |    | 1          | 1          | 1         |    |    |    | 1           | 1           | 1           |         |  |

| Bit(s) | Name          | Description                                                                         |
|--------|---------------|-------------------------------------------------------------------------------------|
| 16     | ESW_CLK_EN    | <b>Ethernet switch clock control</b><br><br>1: Clock enable<br><br>0: Clock disable |
| 15     | WOCPU0_CLK_EN | <b>WOCP clock control</b><br><br>1: Clock enable<br><br>0: Clock disable            |
| 14     | WOCPU1_CLK_EN | <b>WOCP clock control</b><br><br>1: Clock enable<br><br>0: Clock disable            |
| 13     | WOCPU2_CLK_EN | <b>WOCP clock control</b><br><br>1: Clock enable<br><br>0: Clock disable            |
| 10     | GP3_CLK_EN    | <b>Giga port 3 clock control</b><br><br>1: Clock enable<br><br>0: Clock disable     |
| 8      | GP1_CLK_EN    | <b>Giga port 1 clock control</b><br><br>1: Clock enable<br><br>0: Clock disable     |
| 7      | GP2_CLK_EN    | <b>Giga port 2 clock control</b><br><br>1: Clock enable<br><br>0: Clock disable     |
| 6      | FE_CLK_EN     | <b>Frame Engine clock control</b><br><br>1: Clock enable                            |

| Bit(s) | Name        | Description                                            |
|--------|-------------|--------------------------------------------------------|
|        |             | 0: Clock disable                                       |
| 2      | XGP3_CLK_EN | <b>10 Giga port 3 clock control</b><br>1: Clock enable |
|        |             | 0: Clock disable                                       |
| 1      | XGP2_CLK_EN | <b>10 Giga port 2 clock control</b><br>1: Clock enable |
|        |             | 0: Clock disable                                       |
| 0      | XGP1_CLK_EN | <b>10 Giga port 1 clock control</b><br>1: Clock enable |
|        |             | 0: Clock disable                                       |



| 15000034 |          |          | <u>RSTCTL</u> |    |    | Reset control register |           |           |          |        |    |    |    |    |    | 00000004 |  |  |
|----------|----------|----------|---------------|----|----|------------------------|-----------|-----------|----------|--------|----|----|----|----|----|----------|--|--|
| Bit      | 31       | 30       | 29            | 28 | 27 | 26                     | 25        | 24        | 23       | 22     | 21 | 20 | 19 | 18 | 17 | 16       |  |  |
| Name     | PPE2_RST | PPE1_RST | PPE0_RST      |    |    | WDMA2_RST              | WDMA1_RST | WDMA0_RST | GMAC_RST |        |    |    |    |    |    |          |  |  |
| Type     | RW       | RW       | RW            |    |    | RW                     | RW        | RW        | RW       |        |    |    |    |    |    |          |  |  |
| Reset    | 0        | 0        | 0             |    |    | 0                      | 0         | 0         | 0        |        |    |    |    |    |    |          |  |  |
| Bit      | 15       | 14       | 13            | 12 | 11 | 10                     | 9         | 8         | 7        | 6      | 5  | 4  | 3  | 2  | 1  | 0        |  |  |
| Name     |          |          |               |    |    |                        |           | PMTR_RST  |          | FE_RST |    |    |    |    |    |          |  |  |
| Type     |          |          |               |    |    |                        |           | RW        |          | RW     |    |    |    |    |    |          |  |  |
| Reset    |          |          |               |    |    |                        |           | 0         |          | 0      |    |    |    |    |    |          |  |  |

| Bit(s) | Name      | Description                                                                 |
|--------|-----------|-----------------------------------------------------------------------------|
| 31     | PPE2_RST  | <b>PPE2 reset control</b><br><br>1: Reset assert<br><br>0: Reset de-assert  |
| 30     | PPE1_RST  | <b>PPE1 reset control</b><br><br>1: Reset assert<br><br>0: Reset de-assert  |
| 29     | PPE0_RST  | <b>PPE0 reset control</b><br><br>1: Reset assert<br><br>0: Reset de-assert  |
| 26     | WDMA2_RST | <b>WDMA2 reset control</b><br><br>1: Reset assert<br><br>0: Reset de-assert |
| 25     | WDMA1_RST | <b>WDMA1 reset control</b><br><br>1: Reset assert<br><br>0: Reset de-assert |
| 24     | WDMA0_RST | <b>WDMA0 reset control</b><br><br>1: Reset assert<br><br>0: Reset de-assert |
| 23     | GMAC_RST  | <b>GMAC reset control</b><br><br>1: Reset assert<br><br>0: Reset de-assert  |
| 8      | PMTR_RST  | <b>PMTR reset control</b><br><br>1: Reset assert<br><br>0: Reset de-assert  |

| Bit(s) | Name   | Description                                                                        |
|--------|--------|------------------------------------------------------------------------------------|
| 6      | FE_RST | <b>Frame Engine reset control</b><br><br>1: Reset assert<br><br>0: Reset de-assert |

15000038      **RSTSTAT**      **Reset status register**      00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18           | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------|----|----|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |              |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |              |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |              |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2            | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    | SWSYS<br>RST |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    | W1C          |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    | 0            |    |    |

| Bit(s) | Name     | Description                                                                                                                                                                                                                                                                                                             |
|--------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2      | SWSYSRST | <b>Software system reset occurred</b><br><br>This bit will be set if software reset the chip by writing to the RSTSYS bit in RSTCTL. Writing a '1' will clear this bit. Writing a '0' has not effect.<br><br>NOTE: This register is reset only by a power on reset.<br><br>0: Have no effect.<br><br>1: Clear this bit. |

**15000040      GPIO0\_MODE      GPIO0 purpose selection      00000000**

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | GPIO0_MODE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | GPIO0_MODE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                                                                                            |
|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | GPIO0_MODE | <p><b>Depend on SB_FIFO_SW_RD_EN.</b></p> <p>If SB_FIFO_SW_RD_EN=0: Reserved</p> <p>If SB_FIFO_SW_RD_EN=1: Side band FIFO read LSB</p> |

**15000044      GPIO1\_MODE      GPIO1 purpose selection      00000000**

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | GPIO1_MODE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | GPIO1_MODE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                                                                                            |
|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | GPIO1_MODE | <p><b>Depend on SB_FIFO_SW_RD_EN.</b></p> <p>If SB_FIFO_SW_RD_EN=0: Reserved</p> <p>If SB_FIFO_SW_RD_EN=1: Side band FIFO read MSB</p> |

15000048      **MEMO0**      **Memory0**      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | MEMO0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MEMO0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description |
|--------|-------|-------------|
| 31:0   | MEMO0 | Memory0     |

1500004C      **MEMO1**      **Memory1**      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | MEMO1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MEMO1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description |
|--------|-------|-------------|
| 31:0   | MEMO1 | Memory1     |

15000050      **MEMO2**      **Memory2**      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | MEMO2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MEMO2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description                  |
|--------|-------|------------------------------|
| 31:0   | MEMO2 | Memory2 (utif_in debug read) |

15000054      **MEMO3**      **Memory3**      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | MEMO3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MEMO3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description                   |
|--------|-------|-------------------------------|
| 31:0   | MEMO3 | Memory3 (utif_out debug read) |

15000058      **MEMO4**      **Memory4**      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | MEMO4 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| Bit(s) | Name  | Description               |
|--------|-------|---------------------------|
| 31     | MEMO4 | Memory4 (MCUSYS_DBG_SEL0) |

1500005C      **MEMO5**      **Memory5**      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | MEMO5 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MEMO5 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description               |
|--------|-------|---------------------------|
| 31:0   | MEMO5 | Memory5 (MCUSYS_DBG_SEL1) |

15000060 **IOC\_EN** **NETSYS IO coherence enable register** 00000000

| Bit   | 31            | 30 | 29 | 28 | 27           | 26          | 25          | 24          | 23           | 22           | 21          | 20           | 19           | 18          | 17          | 16          |
|-------|---------------|----|----|----|--------------|-------------|-------------|-------------|--------------|--------------|-------------|--------------|--------------|-------------|-------------|-------------|
| Name  | GLOBAL_IOC_EN |    |    |    |              |             |             |             |              |              |             |              |              |             |             |             |
| Type  | RW            |    |    |    |              |             |             |             |              |              |             |              |              |             |             |             |
| Reset | 0             |    |    |    |              |             |             |             |              |              |             |              |              |             |             |             |
| Bit   | 15            | 14 | 13 | 12 | 11           | 10          | 9           | 8           | 7            | 6            | 5           | 4            | 3            | 2           | 1           | 0           |
| Name  |               |    |    |    | WOCPU_IOC_EN | WED1_IOC_EN | WED0_IOC_EN | FDMA_IOC_EN | EDMA1_IOC_EN | EDMA0_IOC_EN | MDMA_IOC_EN | WDMA1_IOC_EN | WDMA0_IOC_EN | PPE1_IOC_EN | PPE0_IOC_EN | ADMA_IOC_EN |
| Type  |               |    |    |    | RW           | RW          | RW          | RW          | RW           | RW           | RW          | RW           | RW           | RW          | RW          | RW          |
| Reset |               |    |    |    | 0            | 0           | 0           | 0           | 0            | 0            | 0           | 0            | 0            | 0           | 0           | 0           |

| Bit(s) | Name          | Description                                                                                         |
|--------|---------------|-----------------------------------------------------------------------------------------------------|
| 31     | GLOBAL_IOC_EN | <b>Global IOC enable</b><br><br>0: Disable<br><br>1: Enable                                         |
| 11     | WOCPU_IOC_EN  | <b>WOCPU IOC enable</b><br><br>Only valid when GLOBAL_IOC_EN = 1<br><br>0: Disable<br><br>1: Enable |
| 10     | WED1_IOC_EN   | <b>WED1 IOC enable</b><br><br>Only valid when GLOBAL_IOC_EN = 1<br><br>0: Disable<br><br>1: Enable  |
| 9      | WED0_IOC_EN   | <b>WED0 IOC enable</b><br><br>Only valid when GLOBAL_IOC_EN = 1<br><br>0: Disable<br><br>1: Enable  |
| 8      | FDMA_IOC_EN   | <b>FDMA IOC enable</b><br><br>Only valid when GLOBAL_IOC_EN = 1<br><br>0: Disable<br><br>1: Enable  |
| 7      | EDMA1_IOC_EN  | <b>EDMA1 IOC enable</b><br><br>Only valid when GLOBAL_IOC_EN = 1<br><br>0: Disable<br><br>1: Enable |

| Bit(s) | Name         | Description                                                                                         |
|--------|--------------|-----------------------------------------------------------------------------------------------------|
| 6      | EDMA0_IOC_EN | <b>EDMA0 IOC enable</b><br><br>Only valid when GLOBAL_IOC_EN = 1<br><br>0: Disable<br><br>1: Enable |
| 5      | MDMA_IOC_EN  | <b>MDMA IOC enable</b><br><br>Only valid when GLOBAL_IOC_EN = 1<br><br>0: Disable<br><br>1: Enable  |
| 4      | WDMA1_IOC_EN | <b>WDMA1 IOC enable</b><br><br>Only valid when GLOBAL_IOC_EN = 1<br><br>0: Disable<br><br>1: Enable |
| 3      | WDMA0_IOC_EN | <b>WDMA0 IOC enable</b><br><br>Only valid when GLOBAL_IOC_EN = 1<br><br>0: Disable<br><br>1: Enable |
| 2      | PPE1_IOC_EN  | <b>PPE1 IOC enable</b><br><br>Only valid when GLOBAL_IOC_EN = 1<br><br>0: Disable<br><br>1: Enable  |
| 1      | PPE0_IOC_EN  | <b>PPE0 IOC enable</b><br><br>Only valid when GLOBAL_IOC_EN = 1<br><br>0: Disable<br><br>1: Enable  |
| 0      | ADMA_IOC_EN  | <b>ADMA IOC enable</b><br><br>Only valid when GLOBAL_IOC_EN = 1<br><br>0: Disable<br><br>1: Enable  |

| 15000064 |                        | BIST_CTRL              |                        |                      | NETSYS Global BIST configuration register |                         |                         |                       |    |                         |                         |                       |    |                         | 00000000                |                       |
|----------|------------------------|------------------------|------------------------|----------------------|-------------------------------------------|-------------------------|-------------------------|-----------------------|----|-------------------------|-------------------------|-----------------------|----|-------------------------|-------------------------|-----------------------|
| Bit      | 31                     | 30                     | 29                     | 28                   | 27                                        | 26                      | 25                      | 24                    | 23 | 22                      | 21                      | 20                    | 19 | 18                      | 17                      | 16                    |
| Name     | INFRA2NETSYS_NEAR_FULL |                        |                        |                      |                                           |                         |                         |                       |    |                         |                         |                       |    |                         |                         |                       |
| Type     | RO                     |                        |                        |                      |                                           |                         |                         |                       |    |                         |                         |                       |    |                         |                         |                       |
| Reset    | 0                      |                        |                        |                      |                                           |                         |                         |                       |    |                         |                         |                       |    |                         |                         |                       |
| Bit      | 15                     | 14                     | 13                     | 12                   | 11                                        | 10                      | 9                       | 8                     | 7  | 6                       | 5                       | 4                     | 3  | 2                       | 1                       | 0                     |
| Name     |                        | NETSYS2INFRA_BIST_FAIL | NETSYS2INFRA_BIST_DONE | NETSYS2INFRA_BIST_EN |                                           | NETSYS2EMI_M2_BIST_FAIL | NETSYS2EMI_M2_BIST_DONE | NETSYS2EMI_M2_BIST_EN |    | NETSYS2EMI_M1_BIST_FAIL | NETSYS2EMI_M1_BIST_DONE | NETSYS2EMI_M1_BIST_EN |    | NETSYS2EMI_M0_BIST_FAIL | NETSYS2EMI_M0_BIST_DONE | NETSYS2EMI_M0_BIST_EN |
| Type     |                        | RO                     | RO                     | RW                   |                                           | RO                      | RO                      | RW                    |    | RO                      | RO                      | RW                    |    | RO                      | RO                      | RW                    |
| Reset    |                        | 0                      | 0                      | 0                    |                                           | 0                       | 0                       | 0                     |    | 0                       | 0                       | 0                     |    | 0                       | 0                       | 0                     |

| Bit(s) | Name                    | Description                                                                                 |
|--------|-------------------------|---------------------------------------------------------------------------------------------|
| 31     | INFRA2NETSYS_NEAR_FULL  | INFRA2NETSYS GALS read data FIFO near full flag                                             |
| 14     | NETSYS2INFRA_BIST_FAIL  | Asserted when NETSYS2INFRA BIST test fails.<br>Only valid when NETSYS2INFRA_BIST_DONE = 1   |
| 13     | NETSYS2INFRA_BIST_DONE  | Asserted when NETSYS2INFRA BIST test finishes                                               |
| 12     | NETSYS2INFRA_BIST_EN    | Starts NETSYS2INFRA BIST test<br>0: Disable<br>1: Enable                                    |
| 10     | NETSYS2EMI_M2_BIST_FAIL | Asserted when NETSYS2EMI_M2 BIST test fails.<br>Only valid when NETSYS2EMI_M2_BIST_DONE = 1 |
| 9      | NETSYS2EMI_M2_BIST_DONE | Asserted when NETSYS2EMI_M2 BIST test finishes                                              |
| 8      | NETSYS2EMI_M2_BIST_EN   | Starts NETSYS2EMI_M2 BIST test<br>0: Disable<br>1: Enable                                   |
| 6      | NETSYS2EMI_M1_BIST_FAIL | Asserted when NETSYS2EMI_M1 BIST test fails.<br>Only valid when NETSYS2EMI_M1_BIST_DONE = 1 |
| 5      | NETSYS2EMI_M1_BIST_DONE | Asserted when NETSYS2EMI_M1 BIST test finishes                                              |
| 4      | NETSYS2EMI_M1_BIST_EN   | Starts NETSYS2EMI_M1 BIST test<br>0: Disable<br>1: Enable                                   |
| 2      | NETSYS2EMI_M0_BIST_FAIL | Asserted when NETSYS2EMI_M0 BIST test fails.<br>Only valid when NETSYS2EMI_M0_BIST_DONE = 1 |
| 1      | NETSYS2EMI_M0_BIST_DONE | Asserted when NETSYS2EMI_M0 BIST test finishes                                              |



| Bit(s) | Name                  | Description                                                              |
|--------|-----------------------|--------------------------------------------------------------------------|
| 0      | NETSYS2EMI_M0_BIST_EN | <b>Starts NETSYS2EMI_M0 BIST test</b><br><br>0: Disable<br><br>1: Enable |

15000068      BIST\_NETSYS2EMI0      NETSYS2EMI\_M0 BIST configuration register 0      00000000

| Bit   | 31                      | 30 | 29                      | 28 | 27                       | 26 | 25                       | 24 | 23                      | 22 | 21                      | 20 | 19                       | 18 | 17                        | 16 |
|-------|-------------------------|----|-------------------------|----|--------------------------|----|--------------------------|----|-------------------------|----|-------------------------|----|--------------------------|----|---------------------------|----|
| Name  |                         |    |                         |    |                          |    |                          |    |                         |    |                         |    | NETSYS2EMI_M0_AWULTRA_EN |    | NETSYS2EMI_M0_AWDOMAIN_EN |    |
| Type  |                         |    |                         |    |                          |    |                          |    |                         |    |                         |    | RW                       |    | RW                        |    |
| Reset |                         |    |                         |    |                          |    |                          |    |                         |    |                         |    | 0                        | 0  | 0                         | 0  |
| Bit   | 15                      | 14 | 13                      | 12 | 11                       | 10 | 9                        | 8  | 7                       | 6  | 5                       | 4  | 3                        | 2  | 1                         | 0  |
| Name  | NETSYS2EMI_M0_AWUSER_EN |    | NETSYS2EMI_M0_AWPROT_EN |    | NETSYS2EMI_M0_AWCACHE_EN |    | NETSYS2EMI_M0_AWBURST_EN |    | NETSYS2EMI_M0_AWSIZE_EN |    | NETSYS2EMI_M0_AWADDR_EN |    | NETSYS2EMI_M0_AWLEN_EN   |    | NETSYS2EMI_M0_AWID_EN     |    |
| Type  | RW                      |    | RW                      |    | RW                       |    | RW                       |    | RW                      |    | RW                      |    | RW                       |    | RW                        |    |
| Reset | 0                       | 0  | 0                       | 0  | 0                        | 0  | 0                        | 0  | 0                       | 0  | 0                       | 0  | 0                        | 0  | 0                         | 0  |

| Bit(s) | Name                      | Description                                                                                                                   |
|--------|---------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| 19:18  | NETSYS2EMI_M0_AWULTRA_EN  | <b>Tests NETSYS2EMI_M0 awultra signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable  |
| 17:16  | NETSYS2EMI_M0_AWDOMAIN_EN | <b>Tests NETSYS2EMI_M0 awdomain signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable |
| 15:14  | NETSYS2EMI_M0_AWUSER_EN   | <b>Tests NETSYS2EMI_M0 awuser signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable   |
| 13:12  | NETSYS2EMI_M0_AWPROT_EN   | <b>Tests NETSYS2EMI_M0 awprot signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: 7 enable<br>2'b11: 0 enable   |
| 11:10  | NETSYS2EMI_M0_AWCACHE_EN  | <b>Tests NETSYS2EMI_M0 awcache signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable  |
| 9:8    | NETSYS2EMI_M0_AWBURST_EN  | <b>Tests NETSYS2EMI_M0 awburst signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: INCR(01) enable              |

| Bit(s) | Name                    | Description                               |
|--------|-------------------------|-------------------------------------------|
|        |                         | 2'b10: WRAP(10) enable                    |
|        |                         | 2'b11: FIXED(00) enable                   |
| 7:6    | NETSYS2EMI_M0_AWSIZE_EN | <b>Tests NETSYS2EMI_M0 awsize signal</b>  |
|        |                         | 2'b00: Designed functional pattern enable |
|        |                         | 2'b01: 7 enable                           |
|        |                         | 2'b11: 0 enable                           |
| 5:4    | NETSYS2EMI_M0_AWADDR_EN | <b>Tests NETSYS2EMI_M0 awaddr signal</b>  |
|        |                         | 2'b00: Designed functional pattern enable |
|        |                         | 2'b01: 0xFFFFF800 enable                  |
|        |                         | 2'b10: 0xFFFFFFFF enable                  |
|        |                         | 2'b11: 0x00000000 enable                  |
| 3:2    | NETSYS2EMI_M0_AWLEN_EN  | <b>Tests NETSYS2EMI_M0 awlen signal</b>   |
|        |                         | 2'b00: Designed functional pattern enable |
|        |                         | 2'b01: F enable                           |
|        |                         | 2'b11: 0 enable                           |
| 1:0    | NETSYS2EMI_M0_AWID_EN   | <b>Tests NETSYS2EMI_M0 awid signal</b>    |
|        |                         | 2'b00: Designed functional pattern enable |
|        |                         | 2'b01: F enable                           |
|        |                         | 2'b11: 0 enable                           |

1500006C      BIST\_NETSYS2EMI1      NETSYS2EMI\_M0 BIST configuration register 1      00000000

| Bit   | 31                      | 30 | 29                      | 28 | 27                       | 26 | 25                       | 24 | 23                      | 22 | 21                      | 20 | 19                       | 18 | 17                        | 16 |
|-------|-------------------------|----|-------------------------|----|--------------------------|----|--------------------------|----|-------------------------|----|-------------------------|----|--------------------------|----|---------------------------|----|
| Name  |                         |    | NETSYS2EMI_M0_RRESP_EN  |    | NETSYS2EMI_M0_RDATA_EN   |    | NETSYS2EMI_M0_BRESP_EN   |    | NETSYS2EMI_M0_WSTRB_EN  |    | NETSYS2EMI_M0_WDATA_EN  |    | NETSYS2EMI_M0_ARULTRA_EN |    | NETSYS2EMI_M0_ARDOMAIN_EN |    |
| Type  |                         |    | RW                      |    | RW                       |    | RW                       |    | RW                      |    | RW                      |    | RW                       |    | RW                        |    |
| Reset |                         |    | 0                       | 0  | 0                        | 0  | 0                        | 0  | 0                       | 0  | 0                       | 0  | 0                        | 0  | 0                         | 0  |
| Bit   | 15                      | 14 | 13                      | 12 | 11                       | 10 | 9                        | 8  | 7                       | 6  | 5                       | 4  | 3                        | 2  | 1                         | 0  |
| Name  | NETSYS2EMI_M0_ARUSER_EN |    | NETSYS2EMI_M0_ARPROT_EN |    | NETSYS2EMI_M0_ARCACHE_EN |    | NETSYS2EMI_M0_ARBURST_EN |    | NETSYS2EMI_M0_ARSIZE_EN |    | NETSYS2EMI_M0_ARADDR_EN |    | NETSYS2EMI_M0_ARLEN_EN   |    | NETSYS2EMI_M0_ARID_EN     |    |
| Type  | RW                      |    | RW                      |    | RW                       |    | RW                       |    | RW                      |    | RW                      |    | RW                       |    | RW                        |    |
| Reset | 0                       | 0  | 0                       | 0  | 0                        | 0  | 0                        | 0  | 0                       | 0  | 0                       | 0  | 0                        | 0  | 0                         | 0  |

| Bit(s) | Name                   | Description                                                                                                                                 |
|--------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 29:28  | NETSYS2EMI_M0_RRESP_EN | <b>Tests NETSYS2EMI_M0 rresp signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: 11 enable<br><br>2'b11: 00 enable    |
| 27:26  | NETSYS2EMI_M0_RDATA_EN | <b>Tests NETSYS2EMI_M0 rdata signal</b><br><br>2'b00: 00-FF enable<br><br>2'b01: F enable<br><br>2'b10: 55-AA enable<br><br>2'b11: 0 enable |
| 25:24  | NETSYS2EMI_M0_BRESP_EN | <b>Tests NETSYS2EMI_M0 bresp signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: 11 enable<br><br>2'b11: 00 enable    |
| 23:22  | NETSYS2EMI_M0_WSTRB_EN | <b>Tests NETSYS2EMI_M0 wstrb signal</b><br><br>2'b00: 00-FF enable<br><br>2'b01: F enable<br><br>2'b10: 55-AA enable<br><br>2'b11: 0 enable |
| 21:20  | NETSYS2EMI_M0_WDATA_EN | <b>Tests NETSYS2EMI_M0 wdata signal</b><br><br>2'b00: 00-FF enable<br><br>2'b01: F enable<br><br>2'b10: 55-AA enable<br><br>2'b11: 0 enable |

| Bit(s) | Name                      | Description                                                                                                                                                           |
|--------|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:18  | NETSYS2EMI_M0_ARULTRA_EN  | <b>Tests NETSYS2EMI_M0 arultra signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable                                          |
| 17:16  | NETSYS2EMI_M0_ARDOMAIN_EN | <b>Tests NETSYS2EMI_M0 ardomain signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable                                         |
| 15:14  | NETSYS2EMI_M0_ARUSER_EN   | <b>Tests NETSYS2EMI_M0 aruser signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable                                           |
| 13:12  | NETSYS2EMI_M0_ARPROT_EN   | <b>Tests NETSYS2EMI_M0 arprot signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: 7 enable<br>2'b11: 0 enable                                           |
| 11:10  | NETSYS2EMI_M0_ARCACHE_EN  | <b>Tests NETSYS2EMI_M0 arcache signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable                                          |
| 9:8    | NETSYS2EMI_M0_ARBURST_EN  | <b>Tests NETSYS2EMI_M0 arburst signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: INCR(01) enable<br>2'b10: WRAP(10) enable<br>2'b11: FIXED(00) enable |
| 7:6    | NETSYS2EMI_M0_ARSIZE_EN   | <b>Tests NETSYS2EMI_M0 arsize signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: 7 enable<br>2'b11: 0 enable                                           |
| 5:4    | NETSYS2EMI_M0_ARADDR_EN   | <b>Tests NETSYS2EMI_M0 araddr signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: 0xFFFFF800 enable                                                     |

| Bit(s) | Name                   | Description                               |
|--------|------------------------|-------------------------------------------|
|        |                        | 2'b10: 0xFFFFFFFF enable                  |
|        |                        | 2'b11: 0x00000000 enable                  |
| 3:2    | NETSYS2EMI_M0_ARLEN_EN | <b>Tests NETSYS2EMI_M0 arlen signal</b>   |
|        |                        | 2'b00: Designed functional pattern enable |
|        |                        | 2'b01: F enable                           |
|        |                        | 2'b11: 0 enable                           |
| 1:0    | NETSYS2EMI_M0_ARID_EN  | <b>Tests NETSYS2EMI_M0 arid signal</b>    |
|        |                        | 2'b00: Designed functional pattern enable |
|        |                        | 2'b01: F enable                           |
|        |                        | 2'b11: 0 enable                           |

15000070      BIST\_NETSYS2EMI2      NETSYS2EMI\_M1 BIST configuration register 0      00000000

| Bit   | 31                      | 30 | 29                      | 28 | 27                       | 26 | 25                       | 24 | 23                      | 22 | 21                      | 20 | 19                       | 18 | 17                        | 16 |
|-------|-------------------------|----|-------------------------|----|--------------------------|----|--------------------------|----|-------------------------|----|-------------------------|----|--------------------------|----|---------------------------|----|
| Name  |                         |    |                         |    |                          |    |                          |    |                         |    |                         |    | NETSYS2EMI_M1_AWULTRA_EN |    | NETSYS2EMI_M1_AWDOMAIN_EN |    |
| Type  |                         |    |                         |    |                          |    |                          |    |                         |    |                         |    | RW                       |    | RW                        |    |
| Reset |                         |    |                         |    |                          |    |                          |    |                         |    |                         |    | 0                        | 0  | 0                         | 0  |
| Bit   | 15                      | 14 | 13                      | 12 | 11                       | 10 | 9                        | 8  | 7                       | 6  | 5                       | 4  | 3                        | 2  | 1                         | 0  |
| Name  | NETSYS2EMI_M1_AWUSER_EN |    | NETSYS2EMI_M1_AWPROT_EN |    | NETSYS2EMI_M1_AWCACHE_EN |    | NETSYS2EMI_M1_AWBURST_EN |    | NETSYS2EMI_M1_AWSIZE_EN |    | NETSYS2EMI_M1_AWADDR_EN |    | NETSYS2EMI_M1_AWLEN_EN   |    | NETSYS2EMI_M1_AWID_EN     |    |
| Type  | RW                      |    | RW                      |    | RW                       |    | RW                       |    | RW                      |    | RW                      |    | RW                       |    | RW                        |    |
| Reset | 0                       | 0  | 0                       | 0  | 0                        | 0  | 0                        | 0  | 0                       | 0  | 0                       | 0  | 0                        | 0  | 0                         | 0  |

| Bit(s) | Name                      | Description                                                                                                                   |
|--------|---------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| 19:18  | NETSYS2EMI_M1_AWULTRA_EN  | <b>Tests NETSYS2EMI_M1 awultra signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable  |
| 17:16  | NETSYS2EMI_M1_AWDOMAIN_EN | <b>Tests NETSYS2EMI_M1 awdomain signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable |
| 15:14  | NETSYS2EMI_M1_AWUSER_EN   | <b>Tests NETSYS2EMI_M1 awuser signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable   |
| 13:12  | NETSYS2EMI_M1_AWPROT_EN   | <b>Tests NETSYS2EMI_M1 awprot signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: 7 enable<br>2'b11: 0 enable   |
| 11:10  | NETSYS2EMI_M1_AWCACHE_EN  | <b>Tests NETSYS2EMI_M1 awcache signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable  |
| 9:8    | NETSYS2EMI_M1_AWBURST_EN  | <b>Tests NETSYS2EMI_M1 awburst signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: INCR(01) enable              |

| Bit(s) | Name                    | Description                               |
|--------|-------------------------|-------------------------------------------|
|        |                         | 2'b10: WRAP(10) enable                    |
|        |                         | 2'b11: FIXED(00) enable                   |
| 7:6    | NETSYS2EMI_M1_AWSIZE_EN | <b>Tests NETSYS2EMI_M1 awsize signal</b>  |
|        |                         | 2'b00: Designed functional pattern enable |
|        |                         | 2'b01: 7 enable                           |
|        |                         | 2'b11: 0 enable                           |
| 5:4    | NETSYS2EMI_M1_AWADDR_EN | <b>Tests NETSYS2EMI_M1 awaddr signal</b>  |
|        |                         | 2'b00: Designed functional pattern enable |
|        |                         | 2'b01: 0xFFFFF800 enable                  |
|        |                         | 2'b10: 0xFFFFFFFF enable                  |
|        |                         | 2'b11: 0x00000000 enable                  |
| 3:2    | NETSYS2EMI_M1_AWLEN_EN  | <b>Tests NETSYS2EMI_M1 awlen signal</b>   |
|        |                         | 2'b00: Designed functional pattern enable |
|        |                         | 2'b01: F enable                           |
|        |                         | 2'b11: 0 enable                           |
| 1:0    | NETSYS2EMI_M1_AWID_EN   | <b>Tests NETSYS2EMI_M1 awid signal</b>    |
|        |                         | 2'b00: Designed functional pattern enable |
|        |                         | 2'b01: F enable                           |
|        |                         | 2'b11: 0 enable                           |



**15000074      BIST\_NETSYS2EMI3      NETSYS2EMI\_M1 BIST configuration register 1      00000000**

| Bit   | 31                      | 30 | 29                      | 28 | 27                       | 26 | 25                       | 24 | 23                      | 22 | 21                      | 20 | 19                       | 18 | 17                        | 16 |
|-------|-------------------------|----|-------------------------|----|--------------------------|----|--------------------------|----|-------------------------|----|-------------------------|----|--------------------------|----|---------------------------|----|
| Name  |                         |    | NETSYS2EMI_M1_RRESP_EN  |    | NETSYS2EMI_M1_RDATA_EN   |    | NETSYS2EMI_M1_BRESP_EN   |    | NETSYS2EMI_M1_WSTRB_EN  |    | NETSYS2EMI_M1_WDATA_EN  |    | NETSYS2EMI_M1_ARULTRA_EN |    | NETSYS2EMI_M1_ARDOMAIN_EN |    |
| Type  |                         |    | RW                      |    | RW                       |    | RW                       |    | RW                      |    | RW                      |    | RW                       |    | RW                        |    |
| Reset |                         |    | 0                       | 0  | 0                        | 0  | 0                        | 0  | 0                       | 0  | 0                       | 0  | 0                        | 0  | 0                         | 0  |
| Bit   | 15                      | 14 | 13                      | 12 | 11                       | 10 | 9                        | 8  | 7                       | 6  | 5                       | 4  | 3                        | 2  | 1                         | 0  |
| Name  | NETSYS2EMI_M1_ARUSER_EN |    | NETSYS2EMI_M1_ARPROT_EN |    | NETSYS2EMI_M1_ARCACHE_EN |    | NETSYS2EMI_M1_ARBURST_EN |    | NETSYS2EMI_M1_ARSIZE_EN |    | NETSYS2EMI_M1_ARADDR_EN |    | NETSYS2EMI_M1_ARLEN_EN   |    | NETSYS2EMI_M1_ARID_EN     |    |
| Type  | RW                      |    | RW                      |    | RW                       |    | RW                       |    | RW                      |    | RW                      |    | RW                       |    | RW                        |    |
| Reset | 0                       | 0  | 0                       | 0  | 0                        | 0  | 0                        | 0  | 0                       | 0  | 0                       | 0  | 0                        | 0  | 0                         | 0  |

| Bit(s) | Name                   | Description                                                                                                                                 |
|--------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 29:28  | NETSYS2EMI_M1_RRESP_EN | <b>Tests NETSYS2EMI_M1 rresp signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: 11 enable<br><br>2'b11: 00 enable    |
| 27:26  | NETSYS2EMI_M1_RDATA_EN | <b>Tests NETSYS2EMI_M1 rdata signal</b><br><br>2'b00: 00-FF enable<br><br>2'b01: F enable<br><br>2'b10: 55-AA enable<br><br>2'b11: 0 enable |
| 25:24  | NETSYS2EMI_M1_BRESP_EN | <b>Tests NETSYS2EMI_M1 bresp signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: 11 enable<br><br>2'b11: 00 enable    |
| 23:22  | NETSYS2EMI_M1_WSTRB_EN | <b>Tests NETSYS2EMI_M1 wstrb signal</b><br><br>2'b00: 00-FF enable<br><br>2'b01: F enable<br><br>2'b10: 55-AA enable<br><br>2'b11: 0 enable |
| 21:20  | NETSYS2EMI_M1_WDATA_EN | <b>Tests NETSYS2EMI_M1 wdata signal</b><br><br>2'b00: 00-FF enable<br><br>2'b01: F enable<br><br>2'b10: 55-AA enable<br><br>2'b11: 0 enable |

| Bit(s) | Name                      | Description                                                                                                                                                           |
|--------|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:18  | NETSYS2EMI_M1_ARULTRA_EN  | <b>Tests NETSYS2EMI_M1 arultra signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable                                          |
| 17:16  | NETSYS2EMI_M1_ARDOMAIN_EN | <b>Tests NETSYS2EMI_M1 ardomain signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable                                         |
| 15:14  | NETSYS2EMI_M1_ARUSER_EN   | <b>Tests NETSYS2EMI_M1 aruser signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable                                           |
| 13:12  | NETSYS2EMI_M1_ARPROT_EN   | <b>Tests NETSYS2EMI_M1 arprot signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: 7 enable<br>2'b11: 0 enable                                           |
| 11:10  | NETSYS2EMI_M1_ARCACHE_EN  | <b>Tests NETSYS2EMI_M1 arcache signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable                                          |
| 9:8    | NETSYS2EMI_M1_ARBURST_EN  | <b>Tests NETSYS2EMI_M1 arburst signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: INCR(01) enable<br>2'b10: WRAP(10) enable<br>2'b11: FIXED(00) enable |
| 7:6    | NETSYS2EMI_M1_ARSIZE_EN   | <b>Tests NETSYS2EMI_M1 arsize signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: 7 enable<br>2'b11: 0 enable                                           |
| 5:4    | NETSYS2EMI_M1_ARADDR_EN   | <b>Tests NETSYS2EMI_M1 araddr signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: 0xFFFFF800 enable                                                     |

| Bit(s) | Name                   | Description                               |
|--------|------------------------|-------------------------------------------|
|        |                        | 2'b10: 0xFFFFFFFF enable                  |
|        |                        | 2'b11: 0x00000000 enable                  |
| 3:2    | NETSYS2EMI_M1_ARLEN_EN | <b>Tests NETSYS2EMI_M1 arlen signal</b>   |
|        |                        | 2'b00: Designed functional pattern enable |
|        |                        | 2'b01: F enable                           |
|        |                        | 2'b11: 0 enable                           |
| 1:0    | NETSYS2EMI_M1_ARID_EN  | <b>Tests NETSYS2EMI_M1 arid signal</b>    |
|        |                        | 2'b00: Designed functional pattern enable |
|        |                        | 2'b01: F enable                           |
|        |                        | 2'b11: 0 enable                           |

**15000078      BIST\_NETSYS2INFRA0      NETSYS2INFRA BIST configuration register 0      00000000**

| Bit   | 31                     | 30 | 29                     | 28 | 27                      | 26 | 25                      | 24 | 23                     | 22 | 21                     | 20 | 19                      | 18 | 17                       | 16 |
|-------|------------------------|----|------------------------|----|-------------------------|----|-------------------------|----|------------------------|----|------------------------|----|-------------------------|----|--------------------------|----|
| Name  |                        |    |                        |    |                         |    |                         |    |                        |    |                        |    | NETSYS2INFRA_AWULTRA_EN |    | NETSYS2INFRA_AWDOMAIN_EN |    |
| Type  |                        |    |                        |    |                         |    |                         |    |                        |    |                        |    | RW                      |    | RW                       |    |
| Reset |                        |    |                        |    |                         |    |                         |    |                        |    |                        |    | 0                       | 0  | 0                        | 0  |
| Bit   | 15                     | 14 | 13                     | 12 | 11                      | 10 | 9                       | 8  | 7                      | 6  | 5                      | 4  | 3                       | 2  | 1                        | 0  |
| Name  | NETSYS2INFRA_AWUSER_EN |    | NETSYS2INFRA_AWPROT_EN |    | NETSYS2INFRA_AWCACHE_EN |    | NETSYS2INFRA_AWBURST_EN |    | NETSYS2INFRA_AWSIZE_EN |    | NETSYS2INFRA_AWADDR_EN |    | NETSYS2INFRA_AWLEN_EN   |    | NETSYS2INFRA_AWID_EN     |    |
| Type  | RW                     |    | RW                     |    | RW                      |    | RW                      |    | RW                     |    | RW                     |    | RW                      |    | RW                       |    |
| Reset | 0                      | 0  | 0                      | 0  | 0                       | 0  | 0                       | 0  | 0                      | 0  | 0                      | 0  | 0                       | 0  | 0                        | 0  |

| Bit(s) | Name                     | Description                                                                                                                              |
|--------|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 19:18  | NETSYS2INFRA_AWULTRA_EN  | <b>Tests NETSYS2INFRA awultra signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: F enable<br><br>2'b11: 0 enable  |
| 17:16  | NETSYS2INFRA_AWDOMAIN_EN | <b>Tests NETSYS2INFRA awdomain signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: F enable<br><br>2'b11: 0 enable |
| 15:14  | NETSYS2INFRA_AWUSER_EN   | <b>Tests NETSYS2INFRA awuser signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: F enable<br><br>2'b11: 0 enable   |
| 13:12  | NETSYS2INFRA_AWPROT_EN   | <b>Tests NETSYS2INFRA awprot signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: 7 enable<br><br>2'b11: 0 enable   |
| 11:10  | NETSYS2INFRA_AWCACHE_EN  | <b>Tests NETSYS2INFRA awcache signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: F enable<br><br>2'b11: 0 enable  |
| 9:8    | NETSYS2INFRA_AWBURST_EN  | <b>Tests NETSYS2INFRA awburst signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: INCR(01) enable                  |

| Bit(s) | Name                   | Description                               |
|--------|------------------------|-------------------------------------------|
|        |                        | 2'b10: WRAP(10) enable                    |
|        |                        | 2'b11: FIXED(00) enable                   |
| 7:6    | NETSYS2INFRA_AWSIZE_EN | <b>Tests NETSYS2INFRA awsize signal</b>   |
|        |                        | 2'b00: Designed functional pattern enable |
|        |                        | 2'b01: 7 enable                           |
|        |                        | 2'b11: 0 enable                           |
| 5:4    | NETSYS2INFRA_AWADDR_EN | <b>Tests NETSYS2INFRA awaddr signal</b>   |
|        |                        | 2'b00: Designed functional pattern enable |
|        |                        | 2'b01: 0xFFFFF800 enable                  |
|        |                        | 2'b10: 0xFFFFFFFF enable                  |
|        |                        | 2'b11: 0x00000000 enable                  |
| 3:2    | NETSYS2INFRA_AWLEN_EN  | <b>Tests NETSYS2INFRA awlen signal</b>    |
|        |                        | 2'b00: Designed functional pattern enable |
|        |                        | 2'b01: F enable                           |
|        |                        | 2'b11: 0 enable                           |
| 1:0    | NETSYS2INFRA_AWID_EN   | <b>Tests NETSYS2INFRA awid signal</b>     |
|        |                        | 2'b00: Designed functional pattern enable |
|        |                        | 2'b01: F enable                           |
|        |                        | 2'b11: 0 enable                           |

**1500007C      BIST\_NETSYS2INFRA1      NETSYS2INFRA BIST configuration register 1      00000000**

| Bit   | 31                     | 30 | 29                     | 28 | 27                      | 26 | 25                      | 24 | 23                     | 22 | 21                     | 20 | 19                      | 18 | 17                       | 16 |
|-------|------------------------|----|------------------------|----|-------------------------|----|-------------------------|----|------------------------|----|------------------------|----|-------------------------|----|--------------------------|----|
| Name  |                        |    | NETSYS2INFRA_RRESP_EN  |    | NETSYS2INFRA_RDATA_EN   |    | NETSYS2INFRA_BRESP_EN   |    | NETSYS2INFRA_WSTRB_EN  |    | NETSYS2INFRA_WDATA_EN  |    | NETSYS2INFRA_ARULTRA_EN |    | NETSYS2INFRA_ARDOMAIN_EN |    |
| Type  |                        |    | RW                     |    | RW                      |    | RW                      |    | RW                     |    | RW                     |    | RW                      |    | RW                       |    |
| Reset |                        |    | 0                      | 0  | 0                       | 0  | 0                       | 0  | 0                      | 0  | 0                      | 0  | 0                       | 0  | 0                        | 0  |
| Bit   | 15                     | 14 | 13                     | 12 | 11                      | 10 | 9                       | 8  | 7                      | 6  | 5                      | 4  | 3                       | 2  | 1                        | 0  |
| Name  | NETSYS2INFRA_ARUSER_EN |    | NETSYS2INFRA_ARPROT_EN |    | NETSYS2INFRA_ARCACHE_EN |    | NETSYS2INFRA_ARBURST_EN |    | NETSYS2INFRA_ARSIZE_EN |    | NETSYS2INFRA_ARADDR_EN |    | NETSYS2INFRA_ARLEN_EN   |    | NETSYS2INFRA_ARID_EN     |    |
| Type  | RW                     |    | RW                     |    | RW                      |    | RW                      |    | RW                     |    | RW                     |    | RW                      |    | RW                       |    |
| Reset | 0                      | 0  | 0                      | 0  | 0                       | 0  | 0                       | 0  | 0                      | 0  | 0                      | 0  | 0                       | 0  | 0                        | 0  |

| Bit(s) | Name                  | Description                                                                                                                                |
|--------|-----------------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 29:28  | NETSYS2INFRA_RRESP_EN | <b>Tests NETSYS2INFRA rresp signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: 11 enable<br><br>2'b11: 00 enable    |
| 27:26  | NETSYS2INFRA_RDATA_EN | <b>Tests NETSYS2INFRA rdata signal</b><br><br>2'b00: 00-FF enable<br><br>2'b01: F enable<br><br>2'b10: 55-AA enable<br><br>2'b11: 0 enable |
| 25:24  | NETSYS2INFRA_BRESP_EN | <b>Tests NETSYS2INFRA bresp signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: 11 enable<br><br>2'b11: 00 enable    |
| 23:22  | NETSYS2INFRA_WSTRB_EN | <b>Tests NETSYS2INFRA wstrb signal</b><br><br>2'b00: 00-FF enable<br><br>2'b01: F enable<br><br>2'b10: 55-AA enable<br><br>2'b11: 0 enable |
| 21:20  | NETSYS2INFRA_WDATA_EN | <b>Tests NETSYS2INFRA wdata signal</b><br><br>2'b00: 00-FF enable<br><br>2'b01: F enable<br><br>2'b10: 55-AA enable<br><br>2'b11: 0 enable |

| Bit(s) | Name                     | Description                                                                                                                                                          |
|--------|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:18  | NETSYS2INFRA_ARULTRA_EN  | <b>Tests NETSYS2INFRA arultra signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable                                          |
| 17:16  | NETSYS2INFRA_ARDOMAIN_EN | <b>Tests NETSYS2INFRA ardomain signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable                                         |
| 15:14  | NETSYS2INFRA_ARUSER_EN   | <b>Tests NETSYS2INFRA aruser signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable                                           |
| 13:12  | NETSYS2INFRA_ARPROT_EN   | <b>Tests NETSYS2INFRA arprot signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: 7 enable<br>2'b11: 0 enable                                           |
| 11:10  | NETSYS2INFRA_ARCACHE_EN  | <b>Tests NETSYS2INFRA arcache signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable                                          |
| 9:8    | NETSYS2INFRA_ARBURST_EN  | <b>Tests NETSYS2INFRA arburst signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: INCR(01) enable<br>2'b10: WRAP(10) enable<br>2'b11: FIXED(00) enable |
| 7:6    | NETSYS2INFRA_ARSIZE_EN   | <b>Tests NETSYS2INFRA arsize signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: 7 enable<br>2'b11: 0 enable                                           |
| 5:4    | NETSYS2INFRA_ARADDR_EN   | <b>Tests NETSYS2INFRA araddr signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: 0xFFFFF800 enable                                                     |

| Bit(s) | Name                  | Description                               |
|--------|-----------------------|-------------------------------------------|
|        |                       | 2'b10: 0xFFFFFFFF enable                  |
|        |                       | 2'b11: 0x00000000 enable                  |
| 3:2    | NETSYS2INFRA_ARLEN_EN | <b>Tests NETSYS2INFRA arlen signal</b>    |
|        |                       | 2'b00: Designed functional pattern enable |
|        |                       | 2'b01: F enable                           |
|        |                       | 2'b11: 0 enable                           |
| 1:0    | NETSYS2INFRA_ARID_EN  | <b>Tests NETSYS2INFRA arid signal</b>     |
|        |                       | 2'b00: Designed functional pattern enable |
|        |                       | 2'b01: F enable                           |
|        |                       | 2'b11: 0 enable                           |



15000080      **AXICFG0**      **AXI sideband configuration register 0**      00000000

| Bit   | 31             | 30 | 29             | 28 | 27              | 26 | 25 | 24 | 23             | 22 | 21             | 20 | 19              | 18 | 17 | 16 |
|-------|----------------|----|----------------|----|-----------------|----|----|----|----------------|----|----------------|----|-----------------|----|----|----|
| Name  |                |    |                |    |                 |    |    |    |                |    |                |    |                 |    |    |    |
| Type  |                |    |                |    |                 |    |    |    |                |    |                |    |                 |    |    |    |
| Reset |                |    |                |    |                 |    |    |    |                |    |                |    |                 |    |    |    |
| Bit   | 15             | 14 | 13             | 12 | 11              | 10 | 9  | 8  | 7              | 6  | 5              | 4  | 3               | 2  | 1  | 0  |
| Name  | ADMA_M_ARFLUSH |    | ADMA_M_ARULTRA |    | ADMA_M_ARDOMAIN |    |    |    | ADMA_M_AWFLUSH |    | ADMA_M_AWULTRA |    | ADMA_M_AWDOMAIN |    |    |    |
| Type  | RW             |    | RW             |    | RW              |    |    |    | RW             |    | RW             |    | RW              |    |    |    |
| Reset | 0              | 0  | 0              | 0  | 0               | 0  | 0  | 0  | 0              | 0  | 0              | 0  | 0               | 0  | 0  | 0  |

| Bit(s) | Name            | Description   |
|--------|-----------------|---------------|
| 15:14  | ADMA_M_ARFLUSH  | ADMA arflush  |
| 13:12  | ADMA_M_ARULTRA  | ADMA arultra  |
| 11:8   | ADMA_M_ARDOMAIN | ADMA ardomain |
| 7:6    | ADMA_M_AWFLUSH  | ADMA awflush  |
| 5:4    | ADMA_M_AWULTRA  | ADMA awultra  |
| 3:0    | ADMA_M_AWDOMAIN | ADMA awdomain |

**15000084      AXICFG1      AXI sideband configuration register 1      00000000**

| Bit          | 31             | 30 | 29             | 28 | 27              | 26 | 25 | 24 | 23             | 22 | 21             | 20 | 19              | 18 | 17 | 16 |
|--------------|----------------|----|----------------|----|-----------------|----|----|----|----------------|----|----------------|----|-----------------|----|----|----|
| <b>Name</b>  | PPE1_M_ARFLUSH |    | PPE1_M_ARULTRA |    | PPE1_M_ARDOMAIN |    |    |    | PPE1_M_AWFLUSH |    | PPE1_M_AWULTRA |    | PPE1_M_AWDOMAIN |    |    |    |
| <b>Type</b>  | RW             |    | RW             |    | RW              |    |    |    | RW             |    | RW             |    | RW              |    |    |    |
| <b>Reset</b> | 0              | 0  | 0              | 0  | 0               | 0  | 0  | 0  | 0              | 0  | 0              | 0  | 0               | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13             | 12 | 11              | 10 | 9  | 8  | 7              | 6  | 5              | 4  | 3               | 2  | 1  | 0  |
| <b>Name</b>  | PPE0_M_ARFLUSH |    | PPE0_M_ARULTRA |    | PPE0_M_ARDOMAIN |    |    |    | PPE0_M_AWFLUSH |    | PPE0_M_AWULTRA |    | PPE0_M_AWDOMAIN |    |    |    |
| <b>Type</b>  | RW             |    | RW             |    | RW              |    |    |    | RW             |    | RW             |    | RW              |    |    |    |
| <b>Reset</b> | 0              | 0  | 0              | 0  | 0               | 0  | 0  | 0  | 0              | 0  | 0              | 0  | 0               | 0  | 0  | 0  |

| Bit(s) | Name            | Description   |
|--------|-----------------|---------------|
| 31:30  | PPE1_M_ARFLUSH  | PPE1 arflush  |
| 29:28  | PPE1_M_ARULTRA  | PPE1 arultra  |
| 27:24  | PPE1_M_ARDOMAIN | PPE1 ardomain |
| 23:22  | PPE1_M_AWFLUSH  | PPE1 awflush  |
| 21:20  | PPE1_M_AWULTRA  | PPE1 awultra  |
| 19:16  | PPE1_M_AWDOMAIN | PPE1 awdomain |
| 15:14  | PPE0_M_ARFLUSH  | PPE0 arflush  |
| 13:12  | PPE0_M_ARULTRA  | PPE0 arultra  |
| 11:8   | PPE0_M_ARDOMAIN | PPE0 ardomain |
| 7:6    | PPE0_M_AWFLUSH  | PPE0 awflush  |
| 5:4    | PPE0_M_AWULTRA  | PPE0 awultra  |
| 3:0    | PPE0_M_AWDOMAIN | PPE0 awdomain |

**1500088 GALSCFG0 GALS configuration register 0 21002100**

| Bit   | 31 | 30                      | 29 | 28 | 27 | 26 | 25                       | 24                       | 23                         | 22 | 21                         | 20 | 19                         | 18 | 17                         | 16 |
|-------|----|-------------------------|----|----|----|----|--------------------------|--------------------------|----------------------------|----|----------------------------|----|----------------------------|----|----------------------------|----|
| Name  |    | NETSYS2EMI_M1_IDLE_MASK |    |    |    |    | NETSYS2EMI_M1_OUTPUT_TIE | NETSYS2EMI_M1_SAMPLE_SEL | NETSYS2EMI_M1_SLV_SYNC_SEL |    | NETSYS2EMI_M1_MST_SYNC_SEL |    | NETSYS2EMI_M1_ARFLUSH_THRE |    | NETSYS2EMI_M1_AWFLUSH_THRE |    |
| Type  |    | RW                      |    |    |    |    | RW                       | RW                       | RW                         |    | RW                         |    | RW                         |    | RW                         |    |
| Reset |    | 0                       | 1  | 0  |    |    | 0                        | 1                        | 0                          | 0  | 0                          | 0  | 0                          | 0  | 0                          | 0  |
| Bit   | 15 | 14                      | 13 | 12 | 11 | 10 | 9                        | 8                        | 7                          | 6  | 5                          | 4  | 3                          | 2  | 1                          | 0  |
| Name  |    | NETSYS2EMI_M0_IDLE_MASK |    |    |    |    |                          | NETSYS2EMI_M0_SAMPLE_SEL | NETSYS2EMI_M0_SLV_SYNC_SEL |    | NETSYS2EMI_M0_MST_SYNC_SEL |    | NETSYS2EMI_M0_ARFLUSH_THRE |    | NETSYS2EMI_M0_AWFLUSH_THRE |    |
| Type  |    | RW                      |    |    |    |    |                          | RW                       | RW                         |    | RW                         |    | RW                         |    | RW                         |    |
| Reset |    | 0                       | 1  | 0  |    |    |                          | 1                        | 0                          | 0  | 0                          | 0  | 0                          | 0  | 0                          | 0  |

| Bit(s) | Name                       | Description                                                                                                                           |
|--------|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| 30:28  | NETSYS2EMI_M1_IDLE_MASK    | <b>Idle signal mask</b><br><br>[2]: NETSYS2EMI_M1_BIST_idle<br><br>[1]: NETSYS2EMI_M1_slpprot_idle<br><br>[0]: NETSYS2EMI_M1_axi_idle |
| 25     | NETSYS2EMI_M1_OUTPUT_TIE   | <b>NETSYS2EMI_M1 GALS output ties to 0 for debug power correlation mode</b><br><br>1'b0: disable<br><br>1'b1: enable output ties to 0 |
| 24     | NETSYS2EMI_M1_SAMPLE_SEL   | <b>NETSYS2EMI_M1 GALS select first step of sample clock edge of master &amp; slaver synchronizer</b>                                  |
| 23:22  | NETSYS2EMI_M1_SLV_SYNC_SEL | <b>NETSYS2EMI_M1 GALS slaver synchronizer step</b>                                                                                    |
| 21:20  | NETSYS2EMI_M1_MST_SYNC_SEL | <b>NETSYS2EMI_M1 GALS master synchronizer step</b>                                                                                    |
| 19:18  | NETSYS2EMI_M1_ARFLUSH_THRE | <b>NETSYS2EMI_M1 GALS read FIFO near full threshold</b>                                                                               |
| 17:16  | NETSYS2EMI_M1_AWFLUSH_THRE | <b>NETSYS2EMI_M1 GALS write FIFO near full threshold</b>                                                                              |
| 14:12  | NETSYS2EMI_M0_IDLE_MASK    | <b>Idle signal mask</b><br><br>[2]: NETSYS2EMI_M0_BIST_idle<br><br>[1]: NETSYS2EMI_M0_slpprot_idle<br><br>[0]: NETSYS2EMI_M0_axi_idle |
| 8      | NETSYS2EMI_M0_SAMPLE_SEL   | <b>NETSYS2EMI_M0 GALS select first step of sample clock edge of master &amp; slaver synchronizer</b>                                  |
| 7:6    | NETSYS2EMI_M0_SLV_SYNC_SEL | <b>NETSYS2EMI_M0 GALS slaver synchronizer step</b>                                                                                    |
| 5:4    | NETSYS2EMI_M0_MST_SYNC_SEL | <b>NETSYS2EMI_M0 GALS master synchronizer step</b>                                                                                    |

| Bit(s) | Name                       | Description                                       |
|--------|----------------------------|---------------------------------------------------|
| 3:2    | NETSYS2EMI_M0_ARFLUSH_THRE | NETSYS2EMI_M0 GALS read FIFO near full threshold  |
| 1:0    | NETSYS2EMI_M0_AWFLUSH_THRE | NETSYS2EMI_M0 GALS write FIFO near full threshold |

**150008C GALSCFG1 GALS configuration register 1 01002100**

| Bit   | 31 | 30                     | 29                     | 28 | 27 | 26 | 25                              | 24                      | 23                        | 22 | 21                        | 20 | 19                        | 18 | 17                        | 16 |
|-------|----|------------------------|------------------------|----|----|----|---------------------------------|-------------------------|---------------------------|----|---------------------------|----|---------------------------|----|---------------------------|----|
| Name  |    |                        | INFRA2NETSYS_IDLE_MASK |    |    |    | INFRA2NETSYS_RFIFO_NEAR_FULL_EN | INFRA2NETSYS_SAMPLE_SEL | INFRA2NETSYS_SLV_SYNC_SEL |    | INFRA2NETSYS_MST_SYNC_SEL |    | INFRA2NETSYS_RFIFO_THRE   |    |                           |    |
| Type  |    |                        | RW                     |    |    |    | RW                              | RW                      | RW                        |    | RW                        |    | RW                        |    |                           |    |
| Reset |    |                        | 0                      | 0  |    |    | 0                               | 1                       | 0                         | 0  | 0                         | 0  | 0                         | 0  | 0                         | 0  |
| Bit   | 15 | 14                     | 13                     | 12 | 11 | 10 | 9                               | 8                       | 7                         | 6  | 5                         | 4  | 3                         | 2  | 1                         | 0  |
| Name  |    | NETSYS2INFRA_IDLE_MASK |                        |    |    |    | NETSYS2INFRA_OUTPUT_TIE         | NETSYS2INFRA_SAMPLE_SEL | NETSYS2INFRA_SLV_SYNC_SEL |    | NETSYS2INFRA_MST_SYNC_SEL |    | NETSYS2INFRA_ARFLUSH_THRE |    | NETSYS2INFRA_AWFLUSH_THRE |    |
| Type  |    | RW                     |                        |    |    |    | RW                              | RW                      | RW                        |    | RW                        |    | RW                        |    | RW                        |    |
| Reset |    | 0                      | 1                      | 0  |    |    | 0                               | 1                       | 0                         | 0  | 0                         | 0  | 0                         | 0  | 0                         | 0  |

| Bit(s) | Name                            | Description                                                                                                                  |
|--------|---------------------------------|------------------------------------------------------------------------------------------------------------------------------|
| 29:28  | INFRA2NETSYS_IDLE_MASK          | <b>Idle signal mask</b><br>[1]: INFRA2NETSYS_BIST_idle<br>[0]: INFRA2NETSYS_slpprot_idle                                     |
| 25     | INFRA2NETSYS_RFIFO_NEAR_FULL_EN | <b>INFRA2NETSYS GALS read data FIFO near full control enable</b>                                                             |
| 24     | INFRA2NETSYS_SAMPLE_SEL         | <b>INFRA2NETSYS GALS select first step of sample clock edge of master &amp; slaver synchronizer</b>                          |
| 23:22  | INFRA2NETSYS_SLV_SYNC_SEL       | <b>INFRA2NETSYS GALS slaver synchronizer step</b>                                                                            |
| 21:20  | INFRA2NETSYS_MST_SYNC_SEL       | <b>INFRA2NETSYS GALS master synchronizer step</b>                                                                            |
| 19:16  | INFRA2NETSYS_RFIFO_THRE         | <b>INFRA2NETSYS GALS read data FIFO near full threshold</b>                                                                  |
| 14:12  | NETSYS2INFRA_IDLE_MASK          | <b>Idle signal mask</b><br>[2]: NETSYS2INFRA_BIST_idle<br>[1]: NETSYS2INFRA_slpprot_idle<br>[0]: NETSYS2INFRA_axi_idle       |
| 9      | NETSYS2INFRA_OUTPUT_TIE         | <b>NETSYS2INFRA GALS output ties to 0 for debug power correlation mode</b><br>1'b0: Disable<br>1'b1: Enable output ties to 0 |
| 8      | NETSYS2INFRA_SAMPLE_SEL         | <b>NETSYS2INFRA GALS select first step of sample clock edge of master &amp; slaver synchronizer</b>                          |
| 7:6    | NETSYS2INFRA_SLV_SYNC_SEL       | <b>NETSYS2INFRA GALS slaver synchronizer step</b>                                                                            |
| 5:4    | NETSYS2INFRA_MST_SYNC_SEL       | <b>NETSYS2INFRA GALS master synchronizer step</b>                                                                            |
| 3:2    | NETSYS2INFRA_ARFLUSH_THRE       | <b>NETSYS2INFRA GALS read FIFO near full threshold</b>                                                                       |
| 1:0    | NETSYS2INFRA_AWFLUSH_THRE       | <b>NETSYS2INFRA GALS write FIFO near full threshold</b>                                                                      |

| Bit(s) | Name | Description |
|--------|------|-------------|
|--------|------|-------------|

**15000090      MISTAT      NETSYS bus MI status register      00000000**

| Bit   | 31 | 30                    | 29                      | 28                      | 27 | 26                    | 25                      | 24                      | 23 | 22                    | 21                      | 20                      | 19 | 18                    | 17                      | 16                      |
|-------|----|-----------------------|-------------------------|-------------------------|----|-----------------------|-------------------------|-------------------------|----|-----------------------|-------------------------|-------------------------|----|-----------------------|-------------------------|-------------------------|
| Name  |    |                       |                         |                         |    |                       |                         |                         |    |                       |                         |                         |    | MAS_UP2_ERR_FLGA      | MAS_UP1_ERR_FLGA        | MAS_UP0_ERR_FLGA        |
| Type  |    |                       |                         |                         |    |                       |                         |                         |    |                       |                         |                         |    | RO                    | RO                      | RO                      |
| Reset |    |                       |                         |                         |    |                       |                         |                         |    |                       |                         |                         |    | 0                     | 0                       | 0                       |
| Bit   | 15 | 14                    | 13                      | 12                      | 11 | 10                    | 9                       | 8                       | 7  | 6                     | 5                       | 4                       | 3  | 2                     | 1                       | 0                       |
| Name  |    | SLV_MI1_LOCK_ERR_FLAG | SLV_MI1_ERRMID_SET_RIRQ | SLV_MI1_ERRMID_SET_BIRQ |    | SLV_MI0_LOCK_ERR_FLAG | SLV_MI0_ERRMID_SET_RIRQ | SLV_MI0_ERRMID_SET_BIRQ |    | MAS_MI1_LOCK_ERR_FLAG | MAS_MI1_ERRMID_SET_RIRQ | MAS_MI1_ERRMID_SET_BIRQ |    | MAS_MIO_LOCK_ERR_FLAG | MAS_MIO_ERRMID_SET_RIRQ | MAS_MIO_ERRMID_SET_BIRQ |
| Type  |    | RO                    | RO                      | RO                      |    | RO                    | RO                      | RO                      |    | RO                    | RO                      | RO                      |    | RO                    | RO                      | RO                      |
| Reset |    | 0                     | 0                       | 0                       |    | 0                     | 0                       | 0                       |    | 0                     | 0                       | 0                       |    | 0                     | 0                       | 0                       |

| Bit(s) | Name                    | Description                                       |
|--------|-------------------------|---------------------------------------------------|
| 18     | MAS_UP2_ERR_FLGA        | MAS_UP1 detects error                             |
| 17     | MAS_UP1_ERR_FLGA        | MAS_UP0 detects error                             |
| 16     | MAS_UP0_ERR_FLGA        | MAS_UP0 detects error                             |
| 14     | SLV_MI1_LOCK_ERR_FLAG   | SLV_MI detects lock error                         |
| 13     | SLV_MI1_ERRMID_SET_RIRQ | SLV_MI detects error MID from slave in R channel  |
| 12     | SLV_MI1_ERRMID_SET_BIRQ | SLV_MI detects error MID from slave in B channel  |
| 10     | SLV_MI0_LOCK_ERR_FLAG   | SLV_MI detects lock error                         |
| 9      | SLV_MI0_ERRMID_SET_RIRQ | SLV_MI detects error MID from slave in R channel  |
| 8      | SLV_MI0_ERRMID_SET_BIRQ | SLV_MI detects error MID from slave in B channel  |
| 6      | MAS_MI1_LOCK_ERR_FLAG   | MAS_MI1 detects lock error                        |
| 5      | MAS_MI1_ERRMID_SET_RIRQ | MAS_MI1 detects error MID from slave in R channel |
| 4      | MAS_MI1_ERRMID_SET_BIRQ | MAS_MI1 detects error MID from slave in B channel |
| 2      | MAS_MIO_LOCK_ERR_FLAG   | MAS_MIO detects lock error                        |
| 1      | MAS_MIO_ERRMID_SET_RIRQ | MAS_MIO detects error MID from slave in R channel |
| 0      | MAS_MIO_ERRMID_SET_BIRQ | MAS_MIO detects error MID from slave in B channel |

**15000094      SIOSTAT0      NETSYS bus SI status register 0      00000000**

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21                | 20            | 19            | 18            | 17                | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|-------------------|---------------|---------------|---------------|-------------------|----|
| Name  |               |    |    |    |    |    |    |    |    |    |                   | SLV_SI_VIO_ID |               |               |                   |    |
| Type  |               |    |    |    |    |    |    |    |    |    |                   | RO            |               |               |                   |    |
| Reset |               |    |    |    |    |    |    |    |    |    |                   | 0             | 0             | 0             | 0                 | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5                 | 4             | 3             | 2             | 1                 | 0  |
| Name  | SLV_SI_VIO_ID |    |    |    |    |    |    |    |    |    | SLV_SI_VIO_WAY_EN |               | SLV_SI_VIO_WR | SLV_SI_VIO_RD | SLV_SI_VIO_DECERR |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    | RO                |               | RO            | RO            | RO                |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0             | 0             | 0             | 0                 | 0  |

| Bit(s) | Name              | Description                        |
|--------|-------------------|------------------------------------|
| 20:6   | SLV_SI_VIO_ID     | SLV_SI violation ID                |
| 5:3    | SLV_SI_VIO_WAY_EN | SLV_SI violation way_en            |
| 2      | SLV_SI_VIO_WR     | SLV_SI violation write transaction |
| 1      | SLV_SI_VIO_RD     | SLV_SI violation read transaction  |
| 0      | SLV_SI_VIO_DECERR | SLV_SI violation decode error      |



**15000098**      **SIOSTAT1**      **NETSYS bus SI status register 1**      **00000000**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21                 | 20 | 19 | 18             | 17             | 16                 |
|-------|----------------|----|----|----|----|----|----|----|----|----|--------------------|----|----|----------------|----------------|--------------------|
| Name  |                |    |    |    |    |    |    |    |    |    |                    |    |    |                |                | MAS_SIO_VIO_ID     |
| Type  |                |    |    |    |    |    |    |    |    |    |                    |    |    |                |                | RO                 |
| Reset |                |    |    |    |    |    |    |    |    |    |                    |    |    |                |                | 0                  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5                  | 4  | 3  | 2              | 1              | 0                  |
| Name  | MAS_SIO_VIO_ID |    |    |    |    |    |    |    |    |    | MAS_SIO_VIO_WAY_EN |    |    | MAS_SIO_VIO_WR | MAS_SIO_VIO_RD | MAS_SIO_VIO_DECERR |
| Type  | RO             |    |    |    |    |    |    |    |    |    | RO                 |    |    | RO             | RO             | RO                 |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  | 0  | 0  | 0              | 0              | 0                  |

| Bit(s) | Name               | Description                         |
|--------|--------------------|-------------------------------------|
| 16:6   | MAS_SIO_VIO_ID     | MAS_SIO violation ID                |
| 5:3    | MAS_SIO_VIO_WAY_EN | MAS_SIO violation way_en            |
| 2      | MAS_SIO_VIO_WR     | MAS_SIO violation write transaction |
| 1      | MAS_SIO_VIO_RD     | MAS_SIO violation read transaction  |
| 0      | MAS_SIO_VIO_DECERR | MAS_SIO violation decode error      |

1500009C SI0STAT2 NETSYS bus SI status register 2 00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24             | 23 | 22 | 21                 | 20 | 19 | 18             | 17             | 16                 |
|-------|----|----|----|----|----|----|----|----------------|----|----|--------------------|----|----|----------------|----------------|--------------------|
| Name  |    |    |    |    |    |    |    |                |    |    |                    |    |    |                |                |                    |
| Type  |    |    |    |    |    |    |    |                |    |    |                    |    |    |                |                |                    |
| Reset |    |    |    |    |    |    |    |                |    |    |                    |    |    |                |                |                    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8              | 7  | 6  | 5                  | 4  | 3  | 2              | 1              | 0                  |
| Name  |    |    |    |    |    |    |    | MAS_SI1_VIO_ID |    |    | MAS_SI1_VIO_WAY_EN |    |    | MAS_SI1_VIO_WR | MAS_SI1_VIO_RD | MAS_SI1_VIO_DECERR |
| Type  |    |    |    |    |    |    |    | RO             |    |    | RO                 |    |    | RO             | RO             | RO                 |
| Reset |    |    |    |    |    |    |    | 0              | 0  | 0  | 0                  | 0  | 0  | 0              | 0              | 0                  |

| Bit(s) | Name               | Description                         |
|--------|--------------------|-------------------------------------|
| 8:6    | MAS_SI1_VIO_ID     | MAS_SI1 violation ID                |
| 5:3    | MAS_SI1_VIO_WAY_EN | MAS_SI1 violation way_en            |
| 2      | MAS_SI1_VIO_WR     | MAS_SI1 violation write transaction |
| 1      | MAS_SI1_VIO_RD     | MAS_SI1 violation read transaction  |
| 0      | MAS_SI1_VIO_DECERR | MAS_SI1 violation decode error      |

**150000A0      S2PSTAT0      NETSYS bus S2P status register 0      00000000**

| Bit   | 31                 | 30 | 29 | 28                 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19             | 18             | 17                 | 16                         |
|-------|--------------------|----|----|--------------------|----|----|----|----|----|----|----|----|----------------|----------------|--------------------|----------------------------|
| Name  | SLV_S2P_VIO_ID     |    |    |                    |    |    |    |    |    |    |    |    |                |                |                    | SLV_S2P_VIO_DOMAIN         |
| Type  | RO                 |    |    |                    |    |    |    |    |    |    |    |    |                |                |                    | RO                         |
| Reset | 0                  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0              | 0                  | 0                          |
| Bit   | 15                 | 14 | 13 | 12                 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3              | 2              | 1                  | 0                          |
| Name  | SLV_S2P_VIO_DOMAIN |    |    | SLV_S2P_VIO_WAY_EN |    |    |    |    |    |    |    |    | SLV_S2P_VIO_WR | SLV_S2P_VIO_RD | SLV_S2P_VIO_DECERR | SLV_S2P_VIO_ADDR_unaligned |
| Type  | RO                 |    |    | RO                 |    |    |    |    |    |    |    |    | RO             | RO             | RO                 | RO                         |
| Reset | 0                  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0              | 0                  | 0                          |

| Bit(s) | Name                       | Description                         |
|--------|----------------------------|-------------------------------------|
| 31:17  | SLV_S2P_VIO_ID             | SLV_S2P violation ID                |
| 16:13  | SLV_S2P_VIO_DOMAIN         | SLV_S2P violation domain            |
| 12:4   | SLV_S2P_VIO_WAY_EN         | SLV_S2P violation way_en            |
| 3      | SLV_S2P_VIO_WR             | SLV_S2P violation write transaction |
| 2      | SLV_S2P_VIO_RD             | SLV_S2P violation read transaction  |
| 1      | SLV_S2P_VIO_DECERR         | SLV_S2P violation decode error      |
| 0      | SLV_S2P_VIO_ADDR_unaligned | SLV_S2P violation unaligned address |

**150000A4      S2PSTAT1      NETSYS bus S2P status register 1      00000000**

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | SLV_S2P_VIO_ADDR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | SLV_S2P_VIO_ADDR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description               |
|--------|------------------|---------------------------|
| 31:0   | SLV_S2P_VIO_ADDR | SLV_S2P violation address |

**150000A8      X2SSTAT0      NETSYS bus X2S status register 0      00000000**

| Bit   | 31             | 30 | 29 | 28 | 27             | 26             | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17                 | 16                         |
|-------|----------------|----|----|----|----------------|----------------|----|----|----|----|----|----|----|----|--------------------|----------------------------|
| Name  |                |    |    |    |                | SLV_X2S_VIO_ID |    |    |    |    |    |    |    |    |                    |                            |
| Type  |                |    |    |    |                | RO             |    |    |    |    |    |    |    |    |                    |                            |
| Reset |                |    |    |    |                | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  | 0                          |
| Bit   | 15             | 14 | 13 | 12 | 11             | 10             | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1                  | 0                          |
| Name  | SLV_X2S_VIO_ID |    |    |    | SLV_X2S_VIO_WR | SLV_X2S_VIO_RD |    |    |    |    |    |    |    |    | SLV_X2S_VIO_DECERR | SLV_X2S_VIO_ADDR_unaligned |
| Type  | RO             |    |    |    | RO             | RO             |    |    |    |    |    |    |    |    | RO                 | RO                         |
| Reset | 0              | 0  | 0  | 0  | 0              | 0              |    |    |    |    |    |    |    |    | 0                  | 0                          |

| Bit(s) | Name                       | Description                         |
|--------|----------------------------|-------------------------------------|
| 26:12  | SLV_X2S_VIO_ID             | SLV_X2S violation ID                |
| 11     | SLV_X2S_VIO_WR             | SLV_X2S violation write transaction |
| 10     | SLV_X2S_VIO_RD             | SLV_X2S violation read transaction  |
| 1      | SLV_X2S_VIO_DECERR         | SLV_X2S violation decode error      |
| 0      | SLV_X2S_VIO_ADDR_unaligned | SLV_X2S violation unaligned address |

**150000AC      X2SSTAT1      NETSYS bus X2S status register 1      00000000**

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | SLV_X2S_VIO_ADDR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | SLV_X2S_VIO_ADDR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description               |
|--------|------------------|---------------------------|
| 31:0   | SLV_X2S_VIO_ADDR | SLV_X2S violation address |

| 15000B0 |    | R2XCFG0     |    |    |    | R2X configuration register 0 |    |    |            |    |    |    |    | 000F00FF |    |    |  |
|---------|----|-------------|----|----|----|------------------------------|----|----|------------|----|----|----|----|----------|----|----|--|
| Bit     | 31 | 30          | 29 | 28 | 27 | 26                           | 25 | 24 | 23         | 22 | 21 | 20 | 19 | 18       | 17 | 16 |  |
| Name    |    | R2X_MST_SEL |    |    |    |                              |    |    | R2X_INT_B  |    |    |    |    |          |    |    |  |
| Type    |    | RW          |    |    |    |                              |    |    | RO         |    |    |    |    |          |    |    |  |
| Reset   |    | 0           | 0  | 0  |    |                              |    |    | 0          | 0  | 0  | 0  | 1  | 1        | 1  | 1  |  |
| Bit     | 15 | 14          | 13 | 12 | 11 | 10                           | 9  | 8  | 7          | 6  | 5  | 4  | 3  | 2        | 1  | 0  |  |
| Name    |    |             |    |    |    |                              |    |    | R2X_INT_EN |    |    |    |    |          |    |    |  |
| Type    |    |             |    |    |    |                              |    |    | RW         |    |    |    |    |          |    |    |  |
| Reset   |    |             |    |    |    |                              |    |    | 1          | 1  | 1  | 1  | 1  | 1        | 1  | 1  |  |

| Bit(s) | Name        | Description                                                                                                                                                                                                       |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 30:28  | R2X_MST_SEL | <b>R2X channel debug information select</b><br><br>0: NETSYS ADMA<br><br>1: NETSYS PPE0<br><br>2: NETSYS PPE1                                                                                                     |
| 23:16  | R2X_INT_B   | <b>R2X interrupt status</b><br><br>R2X wrapper interrupt will set 1'b1 when receive len = 0 cmd from rbus master.<br><br>[0]: NETSYS ADMA<br><br>[1]: NETSYS PPE0<br><br>[2]: NETSYS PPE1<br><br>Others: Reserved |
| 7:0    | R2X_INT_EN  | <b>R2X Interrupt Enable</b><br><br>Enable R2X wrapper interrupt when receive len = 0 cmd from rbus master.<br><br>0: Disable<br><br>1: Enable                                                                     |

**15000B4      R2XCFG1      R2X configuration register 1      00000000**

| Bit          | 31            | 30 | 29 | 28 | 27            | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
|--------------|---------------|----|----|----|---------------|----|----|----|---------------|----|----|----|---------------|----|----|----|
| <b>Name</b>  | R2X_DBG_SEL_7 |    |    |    | R2X_DBG_SEL_6 |    |    |    | R2X_DBG_SEL_5 |    |    |    | R2X_DBG_SEL_4 |    |    |    |
| <b>Type</b>  | RW            |    |    |    | RW            |    |    |    | RW            |    |    |    | RW            |    |    |    |
| <b>Reset</b> | 0             | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0             | 0  | 0  | 0  |
| Bit          | 15            | 14 | 13 | 12 | 11            | 10 | 9  | 8  | 7             | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| <b>Name</b>  | R2X_DBG_SEL_3 |    |    |    | R2X_DBG_SEL_2 |    |    |    | R2X_DBG_SEL_1 |    |    |    | R2X_DBG_SEL_0 |    |    |    |
| <b>Type</b>  | RW            |    |    |    | RW            |    |    |    | RW            |    |    |    | RW            |    |    |    |
| <b>Reset</b> | 0             | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0             | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                      |
|--------|---------------|--------------------------------------------------|
| 31:28  | R2X_DBG_SEL_7 | Selects debug information from R2X (Reserved)    |
| 27:24  | R2X_DBG_SEL_6 | Selects debug information from R2X (Reserved)    |
| 23:20  | R2X_DBG_SEL_5 | Selects debug information from R2X (Reserved)    |
| 19:16  | R2X_DBG_SEL_4 | Selects debug information from R2X (Reserved)    |
| 15:12  | R2X_DBG_SEL_3 | Selects debug information from R2X (Reserved)    |
| 11:8   | R2X_DBG_SEL_2 | Selects debug information from R2X (NETSYS PPE1) |
| 7:4    | R2X_DBG_SEL_1 | Selects debug information from R2X (NETSYS PPE0) |
| 3:0    | R2X_DBG_SEL_0 | Selects debug information from R2X (NETSYS ADMA) |
|        |               | 0: r2x interrupt status                          |
|        |               | 1: r2x interrupt enable and Rbus status          |
|        |               | 2: Rbus address                                  |
|        |               | 3: AXI status                                    |
|        |               | 4: AXI write address                             |
|        |               | 5: AXI read address                              |
|        |               | 6: Internal buffer handshake                     |
|        |               | 7: Coherence sequence and Coherence length       |
|        |               | 8: Coherence compare address                     |

**150000B8      R2XSTAT0      R2X status register 0      00000000**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | R2X_INT_STATUS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | R2X_INT_STATUS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                        |
|--------|----------------|----------------------------------------------------------------------------------------------------|
| 31:0   | R2X_INT_STATUS | Records the address when receive len = 0 cmd from R2X selected channel according to R2XCFG0[30:28] |

**150000BC      R2XSTAT1      R2X status register 1      00000000**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | R2X_DBG_INFO |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | R2X_DBG_INFO |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                     |
|--------|--------------|---------------------------------------------------------------------------------|
| 31:0   | R2X_DBG_INFO | Records debug information from R2X selected channel according to R2XCFG0[30:28] |

**150000C0      APBCFG      NETSYS\_APB configuration register      00000000**

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25                 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |                    |    |    |    |    |    |    |    |    | NETSYS_APB_INT_CLR |
| Type  |                    |    |    |    |    |    |                    |    |    |    |    |    |    |    |    | W1C                |
| Reset |                    |    |    |    |    |    |                    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9                  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | NETSYS_APB_ERR_CNT |    |    |    |    |    | NETSYS_APB_INT_CNT |    |    |    |    |    |    |    |    |                    |
| Type  | RO                 |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                                                                                                                                                                                                                                                                                 |
|--------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16     | NETSYS_APB_INT_CLR | <b>NETSYS_APB interrupt clear</b><br><br>Write 1 to clear this interrupt.                                                                                                                                                                                                                                                                   |
| 15:10  | NETSYS_APB_ERR_CNT | <b>NETSYS_APB error counter</b><br><br>Sets a delay timer which begins counting down when an error is detected.<br><br>When the timer reaches zero the interrupt is then triggered.<br><br>10'b0000000000: Disable NETSYS_APB monitoring<br><br>10'b0000000001: 20 us<br><br>10'b0000000010: 40 us<br><br>10'b1000000000: 40 ms             |
| 9:0    | NETSYS_APB_INT_CNT | <b>NETSYS_APB interrupt countdown timer</b><br><br>Sets a delay timer which begins counting down when an error is detected.<br><br>When the timer reaches zero the interrupt is then triggered.<br><br>10'b0000000000: Disable NETSYS_APB monitoring<br><br>10'b0000000001: 20 us<br><br>10'b0000000010: 40 us<br><br>10'b1000000000: 40 ms |

**150000C4      APBSTAT      NETSYS\_APB status register      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | NETSYS_APB_ERR_ADDR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | NETSYS_APB_ERR_ADDR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                               |
|--------|---------------------|-----------------------------------------------------------|
| 31:0   | NETSYS_APB_ERR_ADDR | <b>NETSYS_APB address record for previous error found</b> |



**15000150      BIST\_NETSYS2EMI4      NETSYS2EMI\_M2 BIST configuration register 0      00000000**

| Bit   | 31                      | 30 | 29                      | 28 | 27                       | 26 | 25                       | 24 | 23                      | 22 | 21                      | 20 | 19                       | 18 | 17                        | 16 |
|-------|-------------------------|----|-------------------------|----|--------------------------|----|--------------------------|----|-------------------------|----|-------------------------|----|--------------------------|----|---------------------------|----|
| Name  |                         |    |                         |    |                          |    |                          |    |                         |    |                         |    | NETSYS2EMI_M2_AWULTRA_EN |    | NETSYS2EMI_M2_AWDOMAIN_EN |    |
| Type  |                         |    |                         |    |                          |    |                          |    |                         |    |                         |    | RW                       |    | RW                        |    |
| Reset |                         |    |                         |    |                          |    |                          |    |                         |    |                         |    | 0                        | 0  | 0                         | 0  |
| Bit   | 15                      | 14 | 13                      | 12 | 11                       | 10 | 9                        | 8  | 7                       | 6  | 5                       | 4  | 3                        | 2  | 1                         | 0  |
| Name  | NETSYS2EMI_M2_AWUSER_EN |    | NETSYS2EMI_M2_AWPROT_EN |    | NETSYS2EMI_M2_AWCACHE_EN |    | NETSYS2EMI_M2_AWBURST_EN |    | NETSYS2EMI_M2_AWSIZE_EN |    | NETSYS2EMI_M2_AWADDR_EN |    | NETSYS2EMI_M2_AWLEN_EN   |    | NETSYS2EMI_M2_AWID_EN     |    |
| Type  | RW                      |    | RW                      |    | RW                       |    | RW                       |    | RW                      |    | RW                      |    | RW                       |    | RW                        |    |
| Reset | 0                       | 0  | 0                       | 0  | 0                        | 0  | 0                        | 0  | 0                       | 0  | 0                       | 0  | 0                        | 0  | 0                         | 0  |

| Bit(s) | Name                      | Description                                                                                                                               |
|--------|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 19:18  | NETSYS2EMI_M2_AWULTRA_EN  | <b>Tests NETSYS2EMI_M2 awultra signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: F enable<br><br>2'b11: 0 enable  |
| 17:16  | NETSYS2EMI_M2_AWDOMAIN_EN | <b>Tests NETSYS2EMI_M2 awdomain signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: F enable<br><br>2'b11: 0 enable |
| 15:14  | NETSYS2EMI_M2_AWUSER_EN   | <b>Tests NETSYS2EMI_M2 awuser signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: F enable<br><br>2'b11: 0 enable   |
| 13:12  | NETSYS2EMI_M2_AWPROT_EN   | <b>Tests NETSYS2EMI_M2 awprot signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: 7 enable<br><br>2'b11: 0 enable   |
| 11:10  | NETSYS2EMI_M2_AWCACHE_EN  | <b>Tests NETSYS2EMI_M2 awcache signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: F enable<br><br>2'b11: 0 enable  |
| 9:8    | NETSYS2EMI_M2_AWBURST_EN  | <b>Tests NETSYS2EMI_M2 awburst signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: INCR(01) enable                  |

| Bit(s) | Name                    | Description                               |
|--------|-------------------------|-------------------------------------------|
|        |                         | 2'b10: WRAP(10) enable                    |
|        |                         | 2'b11: FIXED(00) enable                   |
| 7:6    | NETSYS2EMI_M2_AWSIZE_EN | <b>Tests NETSYS2EMI_M2 awsize signal</b>  |
|        |                         | 2'b00: Designed functional pattern enable |
|        |                         | 2'b01: 7 enable                           |
|        |                         | 2'b11: 0 enable                           |
| 5:4    | NETSYS2EMI_M2_AWADDR_EN | <b>Tests NETSYS2EMI_M2 awaddr signal</b>  |
|        |                         | 2'b00: Designed functional pattern enable |
|        |                         | 2'b01: 0xFFFFF800 enable                  |
|        |                         | 2'b10: 0xFFFFFFFF enable                  |
|        |                         | 2'b11: 0x00000000 enable                  |
| 3:2    | NETSYS2EMI_M2_AWLEN_EN  | <b>Tests NETSYS2EMI_M2 awlen signal</b>   |
|        |                         | 2'b00: Designed functional pattern enable |
|        |                         | 2'b01: F enable                           |
|        |                         | 2'b11: 0 enable                           |
| 1:0    | NETSYS2EMI_M2_AWID_EN   | <b>Tests NETSYS2EMI_M2 awid signal</b>    |
|        |                         | 2'b00: Designed functional pattern enable |
|        |                         | 2'b01: F enable                           |
|        |                         | 2'b11: 0 enable                           |

**15000154 BIST\_NETSYS2EMI5 NETSYS2EMI\_M2 BIST configuration register 1 00000000**

| Bit   | 31                      | 30 | 29                      | 28 | 27                       | 26 | 25                       | 24 | 23                      | 22 | 21                      | 20 | 19                       | 18 | 17                        | 16 |
|-------|-------------------------|----|-------------------------|----|--------------------------|----|--------------------------|----|-------------------------|----|-------------------------|----|--------------------------|----|---------------------------|----|
| Name  |                         |    | NETSYS2EMI_M2_RRESP_EN  |    | NETSYS2EMI_M2_RDATA_EN   |    | NETSYS2EMI_M2_BRESP_EN   |    | NETSYS2EMI_M2_WSTRB_EN  |    | NETSYS2EMI_M2_WDATA_EN  |    | NETSYS2EMI_M2_ARULTRA_EN |    | NETSYS2EMI_M2_ARDOMAIN_EN |    |
| Type  |                         |    | RW                      |    | RW                       |    | RW                       |    | RW                      |    | RW                      |    | RW                       |    | RW                        |    |
| Reset |                         |    | 0                       | 0  | 0                        | 0  | 0                        | 0  | 0                       | 0  | 0                       | 0  | 0                        | 0  | 0                         | 0  |
| Bit   | 15                      | 14 | 13                      | 12 | 11                       | 10 | 9                        | 8  | 7                       | 6  | 5                       | 4  | 3                        | 2  | 1                         | 0  |
| Name  | NETSYS2EMI_M2_ARUSER_EN |    | NETSYS2EMI_M2_ARPROT_EN |    | NETSYS2EMI_M2_ARCACHE_EN |    | NETSYS2EMI_M2_ARBURST_EN |    | NETSYS2EMI_M2_ARSIZE_EN |    | NETSYS2EMI_M2_ARADDR_EN |    | NETSYS2EMI_M2_ARLEN_EN   |    | NETSYS2EMI_M2_ARID_EN     |    |
| Type  | RW                      |    | RW                      |    | RW                       |    | RW                       |    | RW                      |    | RW                      |    | RW                       |    | RW                        |    |
| Reset | 0                       | 0  | 0                       | 0  | 0                        | 0  | 0                        | 0  | 0                       | 0  | 0                       | 0  | 0                        | 0  | 0                         | 0  |

| Bit(s) | Name                   | Description                                                                                                                                 |
|--------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 29:28  | NETSYS2EMI_M2_RRESP_EN | <b>Tests NETSYS2EMI_M2 rresp signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: 11 enable<br><br>2'b11: 00 enable    |
| 27:26  | NETSYS2EMI_M2_RDATA_EN | <b>Tests NETSYS2EMI_M2 rdata signal</b><br><br>2'b00: 00-FF enable<br><br>2'b01: F enable<br><br>2'b10: 55-AA enable<br><br>2'b11: 0 enable |
| 25:24  | NETSYS2EMI_M2_BRESP_EN | <b>Tests NETSYS2EMI_M2 bresp signal</b><br><br>2'b00: Designed functional pattern enable<br><br>2'b01: 11 enable<br><br>2'b11: 00 enable    |
| 23:22  | NETSYS2EMI_M2_WSTRB_EN | <b>Tests NETSYS2EMI_M2 wstrb signal</b><br><br>2'b00: 00-FF enable<br><br>2'b01: F enable<br><br>2'b10: 55-AA enable<br><br>2'b11: 0 enable |
| 21:20  | NETSYS2EMI_M2_WDATA_EN | <b>Tests NETSYS2EMI_M2 wdata signal</b><br><br>2'b00: 00-FF enable<br><br>2'b01: F enable<br><br>2'b10: 55-AA enable<br><br>2'b11: 0 enable |

| Bit(s) | Name                      | Description                                                                                                                                                           |
|--------|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:18  | NETSYS2EMI_M2_ARULTRA_EN  | <b>Tests NETSYS2EMI_M2 arultra signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable                                          |
| 17:16  | NETSYS2EMI_M2_ARDOMAIN_EN | <b>Tests NETSYS2EMI_M2 ardomain signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable                                         |
| 15:14  | NETSYS2EMI_M2_ARUSER_EN   | <b>Tests NETSYS2EMI_M2 aruser signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable                                           |
| 13:12  | NETSYS2EMI_M2_ARPROT_EN   | <b>Tests NETSYS2EMI_M2 arprot signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: 7 enable<br>2'b11: 0 enable                                           |
| 11:10  | NETSYS2EMI_M2_ARCACHE_EN  | <b>Tests NETSYS2EMI_M2 arcache signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: F enable<br>2'b11: 0 enable                                          |
| 9:8    | NETSYS2EMI_M2_ARBURST_EN  | <b>Tests NETSYS2EMI_M2 arburst signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: INCR(01) enable<br>2'b10: WRAP(10) enable<br>2'b11: FIXED(00) enable |
| 7:6    | NETSYS2EMI_M2_ARSIZE_EN   | <b>Tests NETSYS2EMI_M2 arsize signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: 7 enable<br>2'b11: 0 enable                                           |
| 5:4    | NETSYS2EMI_M2_ARADDR_EN   | <b>Tests NETSYS2EMI_M2 araddr signal</b><br>2'b00: Designed functional pattern enable<br>2'b01: 0xFFFFF800 enable                                                     |

| Bit(s) | Name                   | Description                               |
|--------|------------------------|-------------------------------------------|
|        |                        | 2'b10: 0xFFFFFFFF enable                  |
|        |                        | 2'b11: 0x00000000 enable                  |
| 3:2    | NETSYS2EMI_M2_ARLEN_EN | <b>Tests NETSYS2EMI_M2 arlen signal</b>   |
|        |                        | 2'b00: Designed functional pattern enable |
|        |                        | 2'b01: F enable                           |
|        |                        | 2'b11: 0 enable                           |
| 1:0    | NETSYS2EMI_M2_ARID_EN  | <b>Tests NETSYS2EMI_M2 arid signal</b>    |
|        |                        | 2'b00: Designed functional pattern enable |
|        |                        | 2'b01: F enable                           |
|        |                        | 2'b11: 0 enable                           |

**15000180      GALSCFG2      GALS configuration register 2      00002100**

| Bit   | 31 | 30                      | 29 | 28 | 27 | 26 | 25 | 24                       | 23                         | 22 | 21                         | 20 | 19                         | 18 | 17                         | 16 |
|-------|----|-------------------------|----|----|----|----|----|--------------------------|----------------------------|----|----------------------------|----|----------------------------|----|----------------------------|----|
| Name  |    |                         |    |    |    |    |    |                          |                            |    |                            |    |                            |    |                            |    |
| Type  |    |                         |    |    |    |    |    |                          |                            |    |                            |    |                            |    |                            |    |
| Reset |    |                         |    |    |    |    |    |                          |                            |    |                            |    |                            |    |                            |    |
| Bit   | 15 | 14                      | 13 | 12 | 11 | 10 | 9  | 8                        | 7                          | 6  | 5                          | 4  | 3                          | 2  | 1                          | 0  |
| Name  |    | NETSYS2EMI_M2_IDLE_MASK |    |    |    |    |    | NETSYS2EMI_M2_SAMPLE_SEL | NETSYS2EMI_M2_SLV_SYNC_SEL |    | NETSYS2EMI_M2_MST_SYNC_SEL |    | NETSYS2EMI_M2_ARFLUSH_THRE |    | NETSYS2EMI_M2_AWFLUSH_THRE |    |
| Type  |    | RW                      |    |    |    |    |    | RW                       | RW                         |    | RW                         |    | RW                         |    | RW                         |    |
| Reset |    | 0                       | 1  | 0  |    |    |    | 1                        | 0                          | 0  | 0                          | 0  | 0                          | 0  | 0                          | 0  |

| Bit(s) | Name                       | Description                                                                                                                           |
|--------|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| 14:12  | NETSYS2EMI_M2_IDLE_MASK    | <b>Idle signal mask</b><br><br>[2]: NETSYS2EMI_M2_BIST_idle<br><br>[1]: NETSYS2EMI_M2_slpprot_idle<br><br>[0]: NETSYS2EMI_M2_axi_idle |
| 8      | NETSYS2EMI_M2_SAMPLE_SEL   | <b>NETSYS2EMI_M2 GALS select first step of sample clock edge of master &amp; slaver synchronizer</b>                                  |
| 7:6    | NETSYS2EMI_M2_SLV_SYNC_SEL | <b>NETSYS2EMI_M2 GALS slaver synchronizer step</b>                                                                                    |
| 5:4    | NETSYS2EMI_M2_MST_SYNC_SEL | <b>NETSYS2EMI_M2 GALS master synchronizer step</b>                                                                                    |
| 3:2    | NETSYS2EMI_M2_ARFLUSH_THRE | <b>NETSYS2EMI_M2 GALS read FIFO near full threshold</b>                                                                               |
| 1:0    | NETSYS2EMI_M2_AWFLUSH_THRE | <b>NETSYS2EMI_M2 GALS write FIFO near full threshold</b>                                                                              |

**150001C0      SIOSTAT3      NETSYS bus SI status register 3      00000000**

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | SLV_SI_VIO_ADDR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | SLV_SI_VIO_ADDR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                     |
|--------|-----------------|---------------------------------|
| 31:0   | SLV_SI_VIO_ADDR | <b>SLV_SI violation address</b> |

**150001C4**      **SI0STAT4**      **NETSYS bus SI status register 4**      **00000000**

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | MAS_SIO_VIO_ADDR_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAS_SIO_VIO_ADDR_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                      |
|--------|--------------------|----------------------------------|
| 31:0   | MAS_SIO_VIO_ADDR_L | MAS_SIO [31:0] violation address |

**150001C8**      **SI0STAT5**      **NETSYS bus SI status register 5**      **00000000**

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | MAS_SIO_VIO_ADDR_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAS_SIO_VIO_ADDR_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                      |
|--------|--------------------|----------------------------------|
| 31:0   | MAS_SIO_VIO_ADDR_H | MAS_SIO [X:32] violation address |

**150001CC**      **SI0STAT6**      **NETSYS bus SI status register 6**      **00000000**

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | MAS_SI1_VIO_ADDR_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAS_SI1_VIO_ADDR_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                      |
|--------|--------------------|----------------------------------|
| 31:0   | MAS_SI1_VIO_ADDR_L | MAS_SI1 [31:0] violation address |

150001D0      SI0STAT7      NETSYS bus SI status register 7      00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | MAS_SI1_VIO_ADDR_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAS_SI1_VIO_ADDR_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                      |
|--------|--------------------|----------------------------------|
| 31:0   | MAS_SI1_VIO_ADDR_H | MAS_SI1 [X:32] violation address |



## 4.2 GSW

### 4.2.1 Register Definition

Module name: GSW Base address: (+0x15020000)

| Address  | Name             | Width | Register Function                     |
|----------|------------------|-------|---------------------------------------|
| 15020004 | <u>CFC</u>       | 32    | CPU forward control                   |
| 15020008 | <u>AISR</u>      | 32    | ACL interrupt status                  |
| 1502000C | <u>AGC</u>       | 32    | ARL global control                    |
| 15020010 | <u>MFC</u>       | 32    | MAC forward control                   |
| 15020014 | <u>VTC</u>       | 32    | VLAN TAG control                      |
| 15020018 | <u>ISC</u>       | 32    | IGMP snooping control                 |
| 1502001C | <u>IMC</u>       | 32    | IGMP/MLD message control              |
| 15020020 | <u>APC</u>       | 32    | ARP and PPPoE control                 |
| 15020024 | <u>BPC</u>       | 32    | BPDU and PAE control                  |
| 15020028 | <u>RGAC1</u>     | 32    | REV_01 and REV_02 control             |
| 1502002C | <u>RGAC2</u>     | 32    | REV_03 and REV_0E control             |
| 15020030 | <u>RGAC3</u>     | 32    | REV_10 and REV_20 control             |
| 15020034 | <u>RGAC4</u>     | 32    | REV_21 and REV_UN control             |
| 15020038 | <u>PMC</u>       | 32    | Protocol match control                |
| 1502003C | <u>PBG1</u>      | 32    | Protocol based group ID-1             |
| 15020040 | <u>PBG2</u>      | 32    | Protocol based group ID-2             |
| 15020058 | <u>PIM1</u>      | 32    | DSCP priority ingress mapping I       |
| 1502005C | <u>PIM2</u>      | 32    | DSCP priority ingress mapping II      |
| 15020060 | <u>PIM3</u>      | 32    | DSCP priority ingress mapping III     |
| 15020064 | <u>PIM4</u>      | 32    | DSCP priority ingress mapping IV      |
| 15020068 | <u>PIM5</u>      | 32    | DSCP priority ingress mapping V       |
| 1502006C | <u>PIM6</u>      | 32    | DSCP priority ingress mapping VI      |
| 15020070 | <u>PIM7</u>      | 32    | DSCP priority ingress mapping VII     |
| 15020074 | <u>ATA1</u>      | 32    | Address table access I                |
| 15020078 | <u>ATA2</u>      | 32    | Address table access II               |
| 1502007C | <u>ATWD</u>      | 32    | Address table write data              |
| 15020080 | <u>ATC</u>       | 32    | Address table control                 |
| 15020084 | <u>TSRA1</u>     | 32    | Table Search read Address I           |
| 15020088 | <u>TSRA2</u>     | 32    | Table Search read Address II          |
| 1502008C | <u>ATRD</u>      | 32    | Address table read data               |
| 15020090 | <u>VTCR</u>      | 32    | VLAN table control                    |
| 15020094 | <u>VAWD1</u>     | 32    | VLAN and ACL write data I             |
| 15020098 | <u>VAWD2</u>     | 32    | VLAN and ACL write data II            |
| 1502009C | <u>TRTCM</u>     | 32    | Two rate three color mark             |
| 150200A0 | <u>AAC</u>       | 32    | Address age control                   |
| 150200A4 | <u>DHCP</u>      | 32    | DHCP control                          |
| 150200A8 | <u>LCP</u>       | 32    | PPPoE LCP control                     |
| 150200AC | <u>MHS</u>       | 32    | MAC table hash seed                   |
| 150200B0 | <u>CPGC</u>      | 32    | Collision pool global control         |
| 150200B4 | <u>CPMONC</u>    | 32    | Collision pool monitor control        |
| 150200B8 | <u>CPMOND1</u>   | 32    | Collision pool entry status monitor 1 |
| 150200BC | <u>CPMOND2</u>   | 32    | Collision pool entry status monitor 2 |
| 150200C0 | <u>CPSTSC</u>    | 32    | Collision pool status counter         |
| 150200C4 | <u>AISR_EXT1</u> | 32    | ACL extension interrupt status I      |

| Address  | Name               | Width | Register Function                                      |
|----------|--------------------|-------|--------------------------------------------------------|
| 150200C8 | <u>AISR_EXT2</u>   | 32    | ACL extension interrupt status II                      |
| 150200CC | <u>AISR_EXT3</u>   | 32    | ACL extension interrupt status III                     |
| 150200D0 | <u>MISR</u>        | 32    | MLDv2 interrupt status                                 |
| 150200D4 | <u>MISR_EXT1</u>   | 32    | MLDv2 extension interrupt status I                     |
| 150200E0 | <u>VAWD3</u>       | 32    | ACL write data III                                     |
| 150200E4 | <u>VAWD4</u>       | 32    | ACL write data IV                                      |
| 150200E8 | <u>VAWD5</u>       | 32    | ACL write data V                                       |
| 150200EC | <u>VAWD6</u>       | 32    | ACL write data VI                                      |
| 150200F0 | <u>VAWD7</u>       | 32    | ACL write data VII                                     |
| 150200F4 | <u>VAWD8</u>       | 32    | ACL write data VIII                                    |
| 15020100 | <u>PTC</u>         | 32    | Port trunking control                                  |
| 15020104 | <u>PTHS</u>        | 32    | Port trunking algorithm seed                           |
| 15020108 | <u>PTGC0</u>       | 32    | Port trunking group control 0                          |
| 1502010C | <u>PTGC1</u>       | 32    | Port trunking group control 1                          |
| 15020110 | <u>PTGC2</u>       | 32    | Port trunking group control 2                          |
| 15020114 | <u>PTGSC0</u>      | 32    | Port trunking group security control 0                 |
| 15020118 | <u>PTGSC1</u>      | 32    | Port trunking group security control 1                 |
| 1502011C | <u>PTGSC2</u>      | 32    | Port trunking group security control 2                 |
| 15020120 | <u>SPTC0</u>       | 32    | Port trunking table control                            |
| 15021000 | <u>MMSCR0_Q0P0</u> | 32    | Max-Min scheduler control register 0 of Queue 0/Port 0 |
| 15021004 | <u>MMSCR1_Q0P0</u> | 32    | Max-Min scheduler control register 1 of Queue 0/Port 0 |
| 15021008 | <u>MMSCR0_Q1P0</u> | 32    | Max-Min scheduler control register 0 of Queue 1/Port 0 |
| 1502100C | <u>MMSCR1_Q1P0</u> | 32    | Max-Min scheduler control register 1 of Queue 1/Port 0 |
| 15021010 | <u>MMSCR0_Q2P0</u> | 32    | Max-Min scheduler control register 0 of Queue 2/Port 0 |
| 15021014 | <u>MMSCR1_Q2P0</u> | 32    | Max-Min scheduler control register 1 of Queue 2/Port 0 |
| 15021018 | <u>MMSCR0_Q3P0</u> | 32    | Max-Min scheduler control register 0 of Queue 3/Port 0 |
| 1502101C | <u>MMSCR1_Q3P0</u> | 32    | Max-Min scheduler control register 1 of Queue 3/Port 0 |
| 15021020 | <u>MMSCR0_Q4P0</u> | 32    | Max-Min scheduler control register 0 of Queue 4/Port 0 |
| 15021024 | <u>MMSCR1_Q4P0</u> | 32    | Max-Min scheduler control register 1 of Queue 4/Port 0 |
| 15021028 | <u>MMSCR0_Q5P0</u> | 32    | Max-Min scheduler control register 0 of Queue 5/Port 0 |
| 1502102C | <u>MMSCR1_Q5P0</u> | 32    | Max-Min scheduler control register 1 of Queue 5/Port 0 |
| 15021030 | <u>MMSCR0_Q6P0</u> | 32    | Max-Min scheduler control register 0 of Queue 6/Port 0 |
| 15021034 | <u>MMSCR1_Q6P0</u> | 32    | Max-Min scheduler control register 1 of Queue 6/Port 0 |
| 15021038 | <u>MMSCR0_Q7P0</u> | 32    | Max-Min scheduler control register 0 of Queue 7/Port 0 |
| 1502103C | <u>MMSCR1_Q7P0</u> | 32    | Max-Min scheduler control register 1 of Queue 7/Port 0 |
| 15021040 | <u>ERLCR_P0</u>    | 32    | Egress rate limit control register of Port 0           |
| 15021050 | <u>MMSCR2_Q0P0</u> | 32    | Max-Min scheduler control register 2 of Queue 0/Port 0 |

| Address  | Name               | Width | Register Function                                      |
|----------|--------------------|-------|--------------------------------------------------------|
| 15021054 | <u>MMSCR3_Q0P0</u> | 32    | Max-Min scheduler control register 3 of Queue 0/Port 0 |
| 15021058 | <u>MMSCR2_Q1P0</u> | 32    | Max-Min scheduler control register 2 of Queue 1/Port 0 |
| 1502105C | <u>MMSCR3_Q1P0</u> | 32    | Max-Min scheduler control register 3 of Queue 1/Port 0 |
| 15021060 | <u>MMSCR2_Q2P0</u> | 32    | Max-Min scheduler control register 2 of Queue 2/Port 0 |
| 15021064 | <u>MMSCR3_Q2P0</u> | 32    | Max-Min scheduler control register 3 of Queue 2/Port 0 |
| 15021068 | <u>MMSCR2_Q3P0</u> | 32    | Max-Min scheduler control register 2 of Queue 3/Port 0 |
| 1502106C | <u>MMSCR3_Q3P0</u> | 32    | Max-Min scheduler control register 3 of Queue 3/Port 0 |
| 15021070 | <u>MMSCR2_Q4P0</u> | 32    | Max-Min scheduler control register 2 of Queue 4/Port 0 |
| 15021074 | <u>MMSCR3_Q4P0</u> | 32    | Max-Min scheduler control register 3 of Queue 4/Port 0 |
| 15021078 | <u>MMSCR2_Q5P0</u> | 32    | Max-Min scheduler control register 2 of Queue 5/Port 0 |
| 1502107C | <u>MMSCR3_Q5P0</u> | 32    | Max-Min scheduler control register 3 of Queue 5/Port 0 |
| 15021080 | <u>MMSCR2_Q6P0</u> | 32    | Max-Min scheduler control register 2 of Queue 6/Port 0 |
| 15021084 | <u>MMSCR3_Q6P0</u> | 32    | Max-Min scheduler control register 3 of Queue 6/Port 0 |
| 15021088 | <u>MMSCR2_Q7P0</u> | 32    | Max-Min scheduler control register 2 of Queue 7/Port 0 |
| 1502108C | <u>MMSCR3_Q7P0</u> | 32    | Max-Min scheduler control register 3 of Queue 7/Port 0 |
| 15021090 | <u>MMSCR_P0</u>    | 32    | Max-Min scheduler control register of Port 0           |
| 150210E0 | <u>GERLCR</u>      | 32    | Global egress rate limit control register              |
| 15021100 | <u>MMSCR0_Q0P1</u> | 32    | Max-Min scheduler control register 0 of Queue 0/Port 1 |
| 15021104 | <u>MMSCR1_Q0P1</u> | 32    | Max-Min scheduler control register 1 of Queue 0/Port 1 |
| 15021108 | <u>MMSCR0_Q1P1</u> | 32    | Max-Min scheduler control register 0 of Queue 1/Port 1 |
| 1502110C | <u>MMSCR1_Q1P1</u> | 32    | Max-Min scheduler control register 1 of Queue 1/Port 1 |
| 15021110 | <u>MMSCR0_Q2P1</u> | 32    | Max-Min scheduler control register 0 of Queue 2/Port 1 |
| 15021114 | <u>MMSCR1_Q2P1</u> | 32    | Max-Min scheduler control register 1 of Queue 2/Port 1 |
| 15021118 | <u>MMSCR0_Q3P1</u> | 32    | Max-Min scheduler control register 0 of Queue 3/Port 1 |
| 1502111C | <u>MMSCR1_Q3P1</u> | 32    | Max-Min scheduler control register 1 of Queue 3/Port 1 |
| 15021120 | <u>MMSCR0_Q4P1</u> | 32    | Max-Min scheduler control register 0 of Queue 4/Port 1 |
| 15021124 | <u>MMSCR1_Q4P1</u> | 32    | Max-Min scheduler control register 1 of Queue 4/Port 1 |
| 15021128 | <u>MMSCR0_Q5P1</u> | 32    | Max-Min scheduler control register 0 of Queue 5/Port 1 |
| 1502112C | <u>MMSCR1_Q5P1</u> | 32    | Max-Min scheduler control register 1 of Queue 5/Port 1 |

| Address  | Name               | Width | Register Function                                      |
|----------|--------------------|-------|--------------------------------------------------------|
| 15021130 | <u>MMSCR0_Q6P1</u> | 32    | Max-Min scheduler control register 0 of Queue 6/Port 1 |
| 15021134 | <u>MMSCR1_Q6P1</u> | 32    | Max-Min scheduler control register 1 of Queue 6/Port 1 |
| 15021138 | <u>MMSCR0_Q7P1</u> | 32    | Max-Min scheduler control register 0 of Queue 7/Port 1 |
| 1502113C | <u>MMSCR1_Q7P1</u> | 32    | Max-Min scheduler control register 1 of Queue 7/Port 1 |
| 15021140 | <u>ERLCR_P1</u>    | 32    | Egress rate limit control register of Port 1           |
| 15021150 | <u>MMSCR2_Q0P1</u> | 32    | Max-Min scheduler control register 2 of Queue 0/Port 1 |
| 15021154 | <u>MMSCR3_Q0P1</u> | 32    | Max-Min scheduler control register 3 of Queue 0/Port 1 |
| 15021158 | <u>MMSCR2_Q1P1</u> | 32    | Max-Min scheduler control register 2 of Queue 1/Port 1 |
| 1502115C | <u>MMSCR3_Q1P1</u> | 32    | Max-Min scheduler control register 3 of Queue 1/Port 1 |
| 15021160 | <u>MMSCR2_Q2P1</u> | 32    | Max-Min scheduler control register 2 of Queue 2/Port 1 |
| 15021164 | <u>MMSCR3_Q2P1</u> | 32    | Max-Min scheduler control register 3 of Queue 2/Port 1 |
| 15021168 | <u>MMSCR2_Q3P1</u> | 32    | Max-Min scheduler control register 2 of Queue 3/Port 1 |
| 1502116C | <u>MMSCR3_Q3P1</u> | 32    | Max-Min scheduler control register 3 of Queue 3/Port 1 |
| 15021170 | <u>MMSCR2_Q4P1</u> | 32    | Max-Min scheduler control register 2 of Queue 4/Port 1 |
| 15021174 | <u>MMSCR3_Q4P1</u> | 32    | Max-Min scheduler control register 3 of Queue 4/Port 1 |
| 15021178 | <u>MMSCR2_Q5P1</u> | 32    | Max-Min scheduler control register 2 of Queue 5/Port 1 |
| 1502117C | <u>MMSCR3_Q5P1</u> | 32    | Max-Min scheduler control register 3 of Queue 5/Port 1 |
| 15021180 | <u>MMSCR2_Q6P1</u> | 32    | Max-Min scheduler control register 2 of Queue 6/Port 1 |
| 15021184 | <u>MMSCR3_Q6P1</u> | 32    | Max-Min scheduler control register 3 of Queue 6/Port 1 |
| 15021188 | <u>MMSCR2_Q7P1</u> | 32    | Max-Min scheduler control register 2 of Queue 7/Port 1 |
| 1502118C | <u>MMSCR3_Q7P1</u> | 32    | Max-Min scheduler control register 3 of Queue 7/Port 1 |
| 15021190 | <u>MMSCR_P1</u>    | 32    | Max-Min scheduler control register of Port 1           |
| 15021200 | <u>MMSCR0_Q0P2</u> | 32    | Max-Min scheduler control register 0 of Queue 0/Port 2 |
| 15021204 | <u>MMSCR1_Q0P2</u> | 32    | Max-Min scheduler control register 1 of Queue 0/Port 2 |
| 15021208 | <u>MMSCR0_Q1P2</u> | 32    | Max-Min scheduler control register 0 of Queue 1/Port 2 |
| 1502120C | <u>MMSCR1_Q1P2</u> | 32    | Max-Min scheduler control register 1 of Queue 1/Port 2 |
| 15021210 | <u>MMSCR0_Q2P2</u> | 32    | Max-Min scheduler control register 0 of Queue 2/Port 2 |
| 15021214 | <u>MMSCR1_Q2P2</u> | 32    | Max-Min scheduler control register 1 of Queue 2/Port 2 |
| 15021218 | <u>MMSCR0_Q3P2</u> | 32    | Max-Min scheduler control register 0 of Queue 3/Port 2 |

| Address  | Name               | Width | Register Function                                      |
|----------|--------------------|-------|--------------------------------------------------------|
| 1502121C | <u>MMSCR1_Q3P2</u> | 32    | Max-Min scheduler control register 1 of Queue 3/Port 2 |
| 15021220 | <u>MMSCR0_Q4P2</u> | 32    | Max-Min scheduler control register 0 of Queue 4/Port 2 |
| 15021224 | <u>MMSCR1_Q4P2</u> | 32    | Max-Min scheduler control register 1 of Queue 4/Port 2 |
| 15021228 | <u>MMSCR0_Q5P2</u> | 32    | Max-Min scheduler control register 0 of Queue 5/Port 2 |
| 1502122C | <u>MMSCR1_Q5P2</u> | 32    | Max-Min scheduler control register 1 of Queue 5/Port 2 |
| 15021230 | <u>MMSCR0_Q6P2</u> | 32    | Max-Min scheduler control register 0 of Queue 6/Port 2 |
| 15021234 | <u>MMSCR1_Q6P2</u> | 32    | Max-Min scheduler control register 1 of Queue 6/Port 2 |
| 15021238 | <u>MMSCR0_Q7P2</u> | 32    | Max-Min scheduler control register 0 of Queue 7/Port 2 |
| 1502123C | <u>MMSCR1_Q7P2</u> | 32    | Max-Min scheduler control register 1 of Queue 7/Port 2 |
| 15021240 | <u>ERLCR_P2</u>    | 32    | Egress rate limit control register of Port 2           |
| 15021250 | <u>MMSCR2_Q0P2</u> | 32    | Max-Min scheduler control register 2 of Queue 0/Port 2 |
| 15021254 | <u>MMSCR3_Q0P2</u> | 32    | Max-Min scheduler control register 3 of Queue 0/Port 2 |
| 15021258 | <u>MMSCR2_Q1P2</u> | 32    | Max-Min scheduler control register 2 of Queue 1/Port 2 |
| 1502125C | <u>MMSCR3_Q1P2</u> | 32    | Max-Min scheduler control register 3 of Queue 1/Port 2 |
| 15021260 | <u>MMSCR2_Q2P2</u> | 32    | Max-Min scheduler control register 2 of Queue 2/Port 2 |
| 15021264 | <u>MMSCR3_Q2P2</u> | 32    | Max-Min scheduler control register 3 of Queue 2/Port 2 |
| 15021268 | <u>MMSCR2_Q3P2</u> | 32    | Max-Min scheduler control register 2 of Queue 3/Port 2 |
| 1502126C | <u>MMSCR3_Q3P2</u> | 32    | Max-Min scheduler control register 3 of Queue 3/Port 2 |
| 15021270 | <u>MMSCR2_Q4P2</u> | 32    | Max-Min scheduler control register 2 of Queue 4/Port 2 |
| 15021274 | <u>MMSCR3_Q4P2</u> | 32    | Max-Min scheduler control register 3 of Queue 4/Port 2 |
| 15021278 | <u>MMSCR2_Q5P2</u> | 32    | Max-Min scheduler control register 2 of Queue 5/Port 2 |
| 1502127C | <u>MMSCR3_Q5P2</u> | 32    | Max-Min scheduler control register 3 of Queue 5/Port 2 |
| 15021280 | <u>MMSCR2_Q6P2</u> | 32    | Max-Min scheduler control register 2 of Queue 6/Port 2 |
| 15021284 | <u>MMSCR3_Q6P2</u> | 32    | Max-Min scheduler control register 3 of Queue 6/Port 2 |
| 15021288 | <u>MMSCR2_Q7P2</u> | 32    | Max-Min scheduler control register 2 of Queue 7/Port 2 |
| 1502128C | <u>MMSCR3_Q7P2</u> | 32    | Max-Min scheduler control register 3 of Queue 7/Port 2 |
| 15021290 | <u>MMSCR_P2</u>    | 32    | Max-Min scheduler control register of Port 2           |
| 15021300 | <u>MMSCR0_Q0P3</u> | 32    | Max-Min scheduler control register 0 of Queue 0/Port 3 |
| 15021304 | <u>MMSCR1_Q0P3</u> | 32    | Max-Min scheduler control register 1 of Queue 0/Port 3 |

| Address  | Name               | Width | Register Function                                      |
|----------|--------------------|-------|--------------------------------------------------------|
| 15021308 | <u>MMSCR0_Q1P3</u> | 32    | Max-Min scheduler control register 0 of Queue 1/Port 3 |
| 1502130C | <u>MMSCR1_Q1P3</u> | 32    | Max-Min scheduler control register 1 of Queue 1/Port 3 |
| 15021310 | <u>MMSCR0_Q2P3</u> | 32    | Max-Min scheduler control register 0 of Queue 2/Port 3 |
| 15021314 | <u>MMSCR1_Q2P3</u> | 32    | Max-Min scheduler control register 1 of Queue 2/Port 3 |
| 15021318 | <u>MMSCR0_Q3P3</u> | 32    | Max-Min scheduler control register 0 of Queue 3/Port 3 |
| 1502131C | <u>MMSCR1_Q3P3</u> | 32    | Max-Min scheduler control register 1 of Queue 3/Port 3 |
| 15021320 | <u>MMSCR0_Q4P3</u> | 32    | Max-Min scheduler control register 0 of Queue 4/Port 3 |
| 15021324 | <u>MMSCR1_Q4P3</u> | 32    | Max-Min scheduler control register 1 of Queue 4/Port 3 |
| 15021328 | <u>MMSCR0_Q5P3</u> | 32    | Max-Min scheduler control register 0 of Queue 5/Port 3 |
| 1502132C | <u>MMSCR1_Q5P3</u> | 32    | Max-Min scheduler control register 1 of Queue 5/Port 3 |
| 15021330 | <u>MMSCR0_Q6P3</u> | 32    | Max-Min scheduler control register 0 of Queue 6/Port 3 |
| 15021334 | <u>MMSCR1_Q6P3</u> | 32    | Max-Min scheduler control register 1 of Queue 6/Port 3 |
| 15021338 | <u>MMSCR0_Q7P3</u> | 32    | Max-Min scheduler control register 0 of Queue 7/Port 3 |
| 1502133C | <u>MMSCR1_Q7P3</u> | 32    | Max-Min scheduler control register 1 of Queue 7/Port 3 |
| 15021340 | <u>ERLCR_P3</u>    | 32    | Egress rate limit control register of Port 3           |
| 15021350 | <u>MMSCR2_Q0P3</u> | 32    | Max-Min scheduler control register 2 of Queue 0/Port 3 |
| 15021354 | <u>MMSCR3_Q0P3</u> | 32    | Max-Min scheduler control register 3 of Queue 0/Port 3 |
| 15021358 | <u>MMSCR2_Q1P3</u> | 32    | Max-Min scheduler control register 2 of Queue 1/Port 3 |
| 1502135C | <u>MMSCR3_Q1P3</u> | 32    | Max-Min scheduler control register 3 of Queue 1/Port 3 |
| 15021360 | <u>MMSCR2_Q2P3</u> | 32    | Max-Min scheduler control register 2 of Queue 2/Port 3 |
| 15021364 | <u>MMSCR3_Q2P3</u> | 32    | Max-Min scheduler control register 3 of Queue 2/Port 3 |
| 15021368 | <u>MMSCR2_Q3P3</u> | 32    | Max-Min scheduler control register 2 of Queue 3/Port 3 |
| 1502136C | <u>MMSCR3_Q3P3</u> | 32    | Max-Min scheduler control register 3 of Queue 3/Port 3 |
| 15021370 | <u>MMSCR2_Q4P3</u> | 32    | Max-Min scheduler control register 2 of Queue 4/Port 3 |
| 15021374 | <u>MMSCR3_Q4P3</u> | 32    | Max-Min scheduler control register 3 of Queue 4/Port 3 |
| 15021378 | <u>MMSCR2_Q5P3</u> | 32    | Max-Min scheduler control register 2 of Queue 5/Port 3 |
| 1502137C | <u>MMSCR3_Q5P3</u> | 32    | Max-Min scheduler control register 3 of Queue 5/Port 3 |
| 15021380 | <u>MMSCR2_Q6P3</u> | 32    | Max-Min scheduler control register 2 of Queue 6/Port 3 |

| Address  | Name               | Width | Register Function                                      |
|----------|--------------------|-------|--------------------------------------------------------|
| 15021384 | <u>MMSCR3_Q6P3</u> | 32    | Max-Min scheduler control register 3 of Queue 6/Port 3 |
| 15021388 | <u>MMSCR2_Q7P3</u> | 32    | Max-Min scheduler control register 2 of Queue 7/Port 3 |
| 1502138C | <u>MMSCR3_Q7P3</u> | 32    | Max-Min scheduler control register 3 of Queue 7/Port 3 |
| 15021390 | <u>MMSCR_P3</u>    | 32    | Max-Min scheduler control register of Port 3           |
| 15021600 | <u>MMSCR0_Q0P6</u> | 32    | Max-Min scheduler control register 0 of Queue 0/Port 6 |
| 15021604 | <u>MMSCR1_Q0P6</u> | 32    | Max-Min scheduler control register 1 of Queue 0/Port 6 |
| 15021608 | <u>MMSCR0_Q1P6</u> | 32    | Max-Min scheduler control register 0 of Queue 1/Port 6 |
| 1502160C | <u>MMSCR1_Q1P6</u> | 32    | Max-Min scheduler control register 1 of Queue 1/Port 6 |
| 15021610 | <u>MMSCR0_Q2P6</u> | 32    | Max-Min scheduler control register 0 of Queue 2/Port 6 |
| 15021614 | <u>MMSCR1_Q2P6</u> | 32    | Max-Min scheduler control register 1 of Queue 2/Port 6 |
| 15021618 | <u>MMSCR0_Q3P6</u> | 32    | Max-Min scheduler control register 0 of Queue 3/Port 6 |
| 1502161C | <u>MMSCR1_Q3P6</u> | 32    | Max-Min scheduler control register 1 of Queue 3/Port 6 |
| 15021620 | <u>MMSCR0_Q4P6</u> | 32    | Max-Min scheduler control register 0 of Queue 4/Port 6 |
| 15021624 | <u>MMSCR1_Q4P6</u> | 32    | Max-Min scheduler control register 1 of Queue 4/Port 6 |
| 15021628 | <u>MMSCR0_Q5P6</u> | 32    | Max-Min scheduler control register 0 of Queue 5/Port 6 |
| 1502162C | <u>MMSCR1_Q5P6</u> | 32    | Max-Min scheduler control register 1 of Queue 5/Port 6 |
| 15021630 | <u>MMSCR0_Q6P6</u> | 32    | Max-Min scheduler control register 0 of Queue 6/Port 6 |
| 15021634 | <u>MMSCR1_Q6P6</u> | 32    | Max-Min scheduler control register 1 of Queue 6/Port 6 |
| 15021638 | <u>MMSCR0_Q7P6</u> | 32    | Max-Min scheduler control register 0 of Queue 7/Port 6 |
| 1502163C | <u>MMSCR1_Q7P6</u> | 32    | Max-Min scheduler control register 1 of Queue 7/Port 6 |
| 15021640 | <u>ERLCR_P6</u>    | 32    | Egress rate limit control register of Port 6           |
| 15021650 | <u>MMSCR2_Q0P6</u> | 32    | Max-Min scheduler control register 2 of Queue 0/Port 6 |
| 15021654 | <u>MMSCR3_Q0P6</u> | 32    | Max-Min scheduler control register 3 of Queue 0/Port 6 |
| 15021658 | <u>MMSCR2_Q1P6</u> | 32    | Max-Min scheduler control register 2 of Queue 1/Port 6 |
| 1502165C | <u>MMSCR3_Q1P6</u> | 32    | Max-Min scheduler control register 3 of Queue 1/Port 6 |
| 15021660 | <u>MMSCR2_Q2P6</u> | 32    | Max-Min scheduler control register 2 of Queue 2/Port 6 |
| 15021664 | <u>MMSCR3_Q2P6</u> | 32    | Max-Min scheduler control register 3 of Queue 2/Port 6 |
| 15021668 | <u>MMSCR2_Q3P6</u> | 32    | Max-Min scheduler control register 2 of Queue 3/Port 6 |
| 1502166C | <u>MMSCR3_Q3P6</u> | 32    | Max-Min scheduler control register 3 of Queue 3/Port 6 |



| Address  | Name                 | Width | Register Function                                      |
|----------|----------------------|-------|--------------------------------------------------------|
| 15021670 | <u>MMSCR2_Q4P6</u>   | 32    | Max-Min scheduler control register 2 of Queue 4/Port 6 |
| 15021674 | <u>MMSCR3_Q4P6</u>   | 32    | Max-Min scheduler control register 3 of Queue 4/Port 6 |
| 15021678 | <u>MMSCR2_Q5P6</u>   | 32    | Max-Min scheduler control register 2 of Queue 5/Port 6 |
| 1502167C | <u>MMSCR3_Q5P6</u>   | 32    | Max-Min scheduler control register 3 of Queue 5/Port 6 |
| 15021680 | <u>MMSCR2_Q6P6</u>   | 32    | Max-Min scheduler control register 2 of Queue 6/Port 6 |
| 15021684 | <u>MMSCR3_Q6P6</u>   | 32    | Max-Min scheduler control register 3 of Queue 6/Port 6 |
| 15021688 | <u>MMSCR2_Q7P6</u>   | 32    | Max-Min scheduler control register 2 of Queue 7/Port 6 |
| 1502168C | <u>MMSCR3_Q7P6</u>   | 32    | Max-Min scheduler control register 3 of Queue 7/Port 6 |
| 15021690 | <u>MMSCR_P6</u>      | 32    | Max-Min scheduler control register of Port 6           |
| 15021800 | <u>IRLCR_P0</u>      | 32    | Ingress rate limit control register of Port 0          |
| 15021804 | <u>FPC_RXCTRL_P0</u> | 32    | Free page count at RX_CTRL of Port 0                   |
| 1502180C | <u>MMDPR_10_Q0P0</u> | 32    | Drop precedence control 10 of Q0 Port 0                |
| 15021810 | <u>MMDPR_10_Q1P0</u> | 32    | Drop precedence control 10 of Q1 Port 0                |
| 15021814 | <u>MMDPR_10_Q2P0</u> | 32    | Drop precedence control 10 of Q2 Port 0                |
| 15021818 | <u>MMDPR_10_Q3P0</u> | 32    | Drop precedence control 10 of Q3 Port 0                |
| 1502181C | <u>MMDPR_10_Q4P0</u> | 32    | Drop precedence control 10 of Q4 Port 0                |
| 15021820 | <u>MMDPR_10_Q5P0</u> | 32    | Drop precedence control 10 of Q5 Port 0                |
| 15021824 | <u>MMDPR_10_Q6P0</u> | 32    | Drop precedence control 10 of Q6 Port 0                |
| 15021828 | <u>MMDPR_10_Q7P0</u> | 32    | Drop precedence control 10 of Q7 Port 0                |
| 1502182C | <u>MMDPR_11_Q0P0</u> | 32    | Drop precedence control 11 of Q0 Port 0                |
| 15021830 | <u>MMDPR_11_Q1P0</u> | 32    | Drop precedence control 11 of Q1 Port 0                |
| 15021834 | <u>MMDPR_11_Q2P0</u> | 32    | Drop precedence control 11 of Q2 Port 0                |
| 15021838 | <u>MMDPR_11_Q3P0</u> | 32    | Drop precedence control 11 of Q3 Port 0                |
| 1502183C | <u>MMDPR_11_Q4P0</u> | 32    | Drop precedence control 11 of Q4 Port 0                |
| 15021840 | <u>MMDPR_11_Q5P0</u> | 32    | Drop precedence control 11 of Q5 Port 0                |
| 15021844 | <u>MMDPR_11_Q6P0</u> | 32    | Drop precedence control 11 of Q6 Port 0                |
| 15021848 | <u>MMDPR_11_Q7P0</u> | 32    | Drop precedence control 11 of Q7 Port 0                |
| 15021900 | <u>IRLCR_P1</u>      | 32    | Ingress rate limit control register of Port 1          |
| 15021904 | <u>FPC_RXCTRL_P1</u> | 32    | Free page count at RX_CTRL of Port 1                   |
| 1502190C | <u>MMDPR_10_Q0P1</u> | 32    | Drop precedence control 10 of Q0 Port 1                |
| 15021910 | <u>MMDPR_10_Q1P1</u> | 32    | Drop precedence control 10 of Q1 Port 1                |
| 15021914 | <u>MMDPR_10_Q2P1</u> | 32    | Drop precedence control 10 of Q2 Port 1                |
| 15021918 | <u>MMDPR_10_Q3P1</u> | 32    | Drop precedence control 10 of Q3 Port 1                |
| 1502191C | <u>MMDPR_10_Q4P1</u> | 32    | Drop precedence control 10 of Q4 Port 1                |
| 15021920 | <u>MMDPR_10_Q5P1</u> | 32    | Drop precedence control 10 of Q5 Port 1                |
| 15021924 | <u>MMDPR_10_Q6P1</u> | 32    | Drop precedence control 10 of Q6 Port 1                |
| 15021928 | <u>MMDPR_10_Q7P1</u> | 32    | Drop precedence control 10 of Q7 Port 1                |
| 1502192C | <u>MMDPR_11_Q0P1</u> | 32    | Drop precedence control 11 of Q0 Port 1                |
| 15021930 | <u>MMDPR_11_Q1P1</u> | 32    | Drop precedence control 11 of Q1 Port 1                |
| 15021934 | <u>MMDPR_11_Q2P1</u> | 32    | Drop precedence control 11 of Q2 Port 1                |
| 15021938 | <u>MMDPR_11_Q3P1</u> | 32    | Drop precedence control 11 of Q3 Port 1                |
| 1502193C | <u>MMDPR_11_Q4P1</u> | 32    | Drop precedence control 11 of Q4 Port 1                |
| 15021940 | <u>MMDPR_11_Q5P1</u> | 32    | Drop precedence control 11 of Q5 Port 1                |
| 15021944 | <u>MMDPR_11_Q6P1</u> | 32    | Drop precedence control 11 of Q6 Port 1                |



| Address  | Name                 | Width | Register Function                             |
|----------|----------------------|-------|-----------------------------------------------|
| 15021948 | <u>MMDPR 11 Q7P1</u> | 32    | Drop precedence control 11 of Q7 Port 1       |
| 15021A00 | <u>IRLCR P2</u>      | 32    | Ingress rate limit control register of Port 2 |
| 15021A04 | <u>FPC RXCTRL P2</u> | 32    | Free page count at RX_CTRL of Port 2          |
| 15021A0C | <u>MMDPR 10 Q0P2</u> | 32    | Drop precedence control 10 of Q0 Port 2       |
| 15021A10 | <u>MMDPR 10 Q1P2</u> | 32    | Drop precedence control 10 of Q1 Port 2       |
| 15021A14 | <u>MMDPR 10 Q2P2</u> | 32    | Drop precedence control 10 of Q2 Port 2       |
| 15021A18 | <u>MMDPR 10 Q3P2</u> | 32    | Drop precedence control 10 of Q3 Port 2       |
| 15021A1C | <u>MMDPR 10 Q4P2</u> | 32    | Drop precedence control 10 of Q4 Port 2       |
| 15021A20 | <u>MMDPR 10 Q5P2</u> | 32    | Drop precedence control 10 of Q5 Port 2       |
| 15021A24 | <u>MMDPR 10 Q6P2</u> | 32    | Drop precedence control 10 of Q6 Port 2       |
| 15021A28 | <u>MMDPR 10 Q7P2</u> | 32    | Drop precedence control 10 of Q7 Port 2       |
| 15021A2C | <u>MMDPR 11 Q0P2</u> | 32    | Drop precedence control 11 of Q0 Port 2       |
| 15021A30 | <u>MMDPR 11 Q1P2</u> | 32    | Drop precedence control 11 of Q1 Port 2       |
| 15021A34 | <u>MMDPR 11 Q2P2</u> | 32    | Drop precedence control 11 of Q2 Port 2       |
| 15021A38 | <u>MMDPR 11 Q3P2</u> | 32    | Drop precedence control 11 of Q3 Port 2       |
| 15021A3C | <u>MMDPR 11 Q4P2</u> | 32    | Drop precedence control 11 of Q4 Port 2       |
| 15021A40 | <u>MMDPR 11 Q5P2</u> | 32    | Drop precedence control 11 of Q5 Port 2       |
| 15021A44 | <u>MMDPR 11 Q6P2</u> | 32    | Drop precedence control 11 of Q6 Port 2       |
| 15021A48 | <u>MMDPR 11 Q7P2</u> | 32    | Drop precedence control 11 of Q7 Port 2       |
| 15021B00 | <u>IRLCR P3</u>      | 32    | Ingress rate limit control register of Port 3 |
| 15021B04 | <u>FPC RXCTRL P3</u> | 32    | Free page count at RX_CTRL of Port 3          |
| 15021B0C | <u>MMDPR 10 Q0P3</u> | 32    | Drop precedence control 10 of Q0 Port 3       |
| 15021B10 | <u>MMDPR 10 Q1P3</u> | 32    | Drop precedence control 10 of Q1 Port 3       |
| 15021B14 | <u>MMDPR 10 Q2P3</u> | 32    | Drop precedence control 10 of Q2 Port 3       |
| 15021B18 | <u>MMDPR 10 Q3P3</u> | 32    | Drop precedence control 10 of Q3 Port 3       |
| 15021B1C | <u>MMDPR 10 Q4P3</u> | 32    | Drop precedence control 10 of Q4 Port 3       |
| 15021B20 | <u>MMDPR 10 Q5P3</u> | 32    | Drop precedence control 10 of Q5 Port 3       |
| 15021B24 | <u>MMDPR 10 Q6P3</u> | 32    | Drop precedence control 10 of Q6 Port 3       |
| 15021B28 | <u>MMDPR 10 Q7P3</u> | 32    | Drop precedence control 10 of Q7 Port 3       |
| 15021B2C | <u>MMDPR 11 Q0P3</u> | 32    | Drop precedence control 11 of Q0 Port 3       |
| 15021B30 | <u>MMDPR 11 Q1P3</u> | 32    | Drop precedence control 11 of Q1 Port 3       |
| 15021B34 | <u>MMDPR 11 Q2P3</u> | 32    | Drop precedence control 11 of Q2 Port 3       |
| 15021B38 | <u>MMDPR 11 Q3P3</u> | 32    | Drop precedence control 11 of Q3 Port 3       |
| 15021B3C | <u>MMDPR 11 Q4P3</u> | 32    | Drop precedence control 11 of Q4 Port 3       |
| 15021B40 | <u>MMDPR 11 Q5P3</u> | 32    | Drop precedence control 11 of Q5 Port 3       |
| 15021B44 | <u>MMDPR 11 Q6P3</u> | 32    | Drop precedence control 11 of Q6 Port 3       |
| 15021B48 | <u>MMDPR 11 Q7P3</u> | 32    | Drop precedence control 11 of Q7 Port 3       |
| 15021C00 | <u>IRLCR P4</u>      | 32    | Ingress rate limit control register of Port 4 |
| 15021C04 | <u>FPC RXCTRL P4</u> | 32    | Free page count at RX_CTRL of Port 4          |
| 15021C0C | <u>MMDPR 10 Q0P4</u> | 32    | Drop precedence control 10 of Q0 Port 4       |
| 15021C10 | <u>MMDPR 10 Q1P4</u> | 32    | Drop precedence control 10 of Q1 Port 4       |
| 15021C14 | <u>MMDPR 10 Q2P4</u> | 32    | Drop precedence control 10 of Q2 Port 4       |
| 15021C18 | <u>MMDPR 10 Q3P4</u> | 32    | Drop precedence control 10 of Q3 Port 4       |
| 15021C1C | <u>MMDPR 10 Q4P4</u> | 32    | Drop precedence control 10 of Q4 Port 4       |
| 15021C20 | <u>MMDPR 10 Q5P4</u> | 32    | Drop precedence control 10 of Q5 Port 4       |
| 15021C24 | <u>MMDPR 10 Q6P4</u> | 32    | Drop precedence control 10 of Q6 Port 4       |
| 15021C28 | <u>MMDPR 10 Q7P4</u> | 32    | Drop precedence control 10 of Q7 Port 4       |
| 15021C2C | <u>MMDPR 11 Q0P4</u> | 32    | Drop precedence control 11 of Q0 Port 4       |
| 15021C30 | <u>MMDPR 11 Q1P4</u> | 32    | Drop precedence control 11 of Q1 Port 4       |
| 15021C34 | <u>MMDPR 11 Q2P4</u> | 32    | Drop precedence control 11 of Q2 Port 4       |

| Address  | Name                 | Width | Register Function                                           |
|----------|----------------------|-------|-------------------------------------------------------------|
| 15021C38 | <u>MMDPR 11 Q3P4</u> | 32    | Drop precedence control 11 of Q3 Port 4                     |
| 15021C3C | <u>MMDPR 11 Q4P4</u> | 32    | Drop precedence control 11 of Q4 Port 4                     |
| 15021C40 | <u>MMDPR 11 Q5P4</u> | 32    | Drop precedence control 11 of Q5 Port 4                     |
| 15021C44 | <u>MMDPR 11 Q6P4</u> | 32    | Drop precedence control 11 of Q6 Port 4                     |
| 15021C48 | <u>MMDPR 11 Q7P4</u> | 32    | Drop precedence control 11 of Q7 Port 4                     |
| 15021D00 | <u>IRLCR P5</u>      | 32    | Ingress rate limit control register of Port 5               |
| 15021D04 | <u>FPC RXCTRL P5</u> | 32    | Free page count at RX_CTRL of Port 5                        |
| 15021D0C | <u>MMDPR 10 Q0P5</u> | 32    | Drop precedence control 10 of Q0 Port 5                     |
| 15021D10 | <u>MMDPR 10 Q1P5</u> | 32    | Drop precedence control 10 of Q1 Port 5                     |
| 15021D14 | <u>MMDPR 10 Q2P5</u> | 32    | Drop precedence control 10 of Q2 Port 5                     |
| 15021D18 | <u>MMDPR 10 Q3P5</u> | 32    | Drop precedence control 10 of Q3 Port 5                     |
| 15021D1C | <u>MMDPR 10 Q4P5</u> | 32    | Drop precedence control 10 of Q4 Port 5                     |
| 15021D20 | <u>MMDPR 10 Q5P5</u> | 32    | Drop precedence control 10 of Q5 Port 5                     |
| 15021D24 | <u>MMDPR 10 Q6P5</u> | 32    | Drop precedence control 10 of Q6 Port 5                     |
| 15021D28 | <u>MMDPR 10 Q7P5</u> | 32    | Drop precedence control 10 of Q7 Port 5                     |
| 15021D2C | <u>MMDPR 11 Q0P5</u> | 32    | Drop precedence control 11 of Q0 Port 5                     |
| 15021D30 | <u>MMDPR 11 Q1P5</u> | 32    | Drop precedence control 11 of Q1 Port 5                     |
| 15021D34 | <u>MMDPR 11 Q2P5</u> | 32    | Drop precedence control 11 of Q2 Port 5                     |
| 15021D38 | <u>MMDPR 11 Q3P5</u> | 32    | Drop precedence control 11 of Q3 Port 5                     |
| 15021D3C | <u>MMDPR 11 Q4P5</u> | 32    | Drop precedence control 11 of Q4 Port 5                     |
| 15021D40 | <u>MMDPR 11 Q5P5</u> | 32    | Drop precedence control 11 of Q5 Port 5                     |
| 15021D44 | <u>MMDPR 11 Q6P5</u> | 32    | Drop precedence control 11 of Q6 Port 5                     |
| 15021D48 | <u>MMDPR 11 Q7P5</u> | 32    | Drop precedence control 11 of Q7 Port 5                     |
| 15021E00 | <u>IRLCR P6</u>      | 32    | Ingress rate limit control register of Port 6               |
| 15021E04 | <u>FPC RXCTRL P6</u> | 32    | Free page count at RX_CTRL of Port 6                        |
| 15021E0C | <u>MMDPR 10 Q0P6</u> | 32    | Drop precedence control 10 of Q0 Port 6                     |
| 15021E10 | <u>MMDPR 10 Q1P6</u> | 32    | Drop precedence control 10 of Q1 Port 6                     |
| 15021E14 | <u>MMDPR 10 Q2P6</u> | 32    | Drop precedence control 10 of Q2 Port 6                     |
| 15021E18 | <u>MMDPR 10 Q3P6</u> | 32    | Drop precedence control 10 of Q3 Port 6                     |
| 15021E1C | <u>MMDPR 10 Q4P6</u> | 32    | Drop precedence control 10 of Q4 Port 6                     |
| 15021E20 | <u>MMDPR 10 Q5P6</u> | 32    | Drop precedence control 10 of Q5 Port 6                     |
| 15021E24 | <u>MMDPR 10 Q6P6</u> | 32    | Drop precedence control 10 of Q6 Port 6                     |
| 15021E28 | <u>MMDPR 10 Q7P6</u> | 32    | Drop precedence control 10 of Q7 Port 6                     |
| 15021E2C | <u>MMDPR 11 Q0P6</u> | 32    | Drop precedence control 11 of Q0 Port 6                     |
| 15021E30 | <u>MMDPR 11 Q1P6</u> | 32    | Drop precedence control 11 of Q1 Port 6                     |
| 15021E34 | <u>MMDPR 11 Q2P6</u> | 32    | Drop precedence control 11 of Q2 Port 6                     |
| 15021E38 | <u>MMDPR 11 Q3P6</u> | 32    | Drop precedence control 11 of Q3 Port 6                     |
| 15021E3C | <u>MMDPR 11 Q4P6</u> | 32    | Drop precedence control 11 of Q4 Port 6                     |
| 15021E40 | <u>MMDPR 11 Q5P6</u> | 32    | Drop precedence control 11 of Q5 Port 6                     |
| 15021E44 | <u>MMDPR 11 Q6P6</u> | 32    | Drop precedence control 11 of Q6 Port 6                     |
| 15021E48 | <u>MMDPR 11 Q7P6</u> | 32    | Drop precedence control 11 of Q7 Port 6                     |
| 15021FC0 | <u>FPLC</u>          | 32    | Free page Link count register                               |
| 15021FE0 | <u>GFCCR0</u>        | 32    | Global Flow_Control control register 0                      |
| 15021FE4 | <u>GFCCR1</u>        | 32    | Global Flow_Control control register 1                      |
| 15021FE8 | <u>GFCCR2</u>        | 32    | Global Flow_Control control register 2                      |
| 15021FEC | <u>GFCCR3</u>        | 32    | Global Flow_Control control register 3                      |
| 15021FF0 | <u>GFCCR4</u>        | 32    | Global Flow_Control control register 4                      |
| 15021FF4 | <u>FCBRCR0</u>       | 32    | Flow control block reservation control register for group 0 |
| 15021FF8 | <u>FCBRCR1</u>       | 32    | Flow control block reservation control register for group 1 |

| Address  | Name               | Width | Register Function                          |
|----------|--------------------|-------|--------------------------------------------|
| 15021FFC | <u>GIRLCR</u>      | 32    | Global ingress rate limit control register |
| 15022000 | <u>P0_SSC</u>      | 32    | STP state control of P0                    |
| 15022004 | <u>P0_PCR</u>      | 32    | Port control of P0                         |
| 15022008 | <u>P0_PIC</u>      | 32    | Port IGMP control of P0                    |
| 1502200C | <u>P0_PSC</u>      | 32    | Port security control of P0                |
| 15022010 | <u>P0_PVC</u>      | 32    | Port VLAN control of P0                    |
| 15022014 | <u>P0_PPBV1</u>    | 32    | Port-and-Protocol based VLAN I of P0       |
| 15022018 | <u>P0_PPBV2</u>    | 32    | Port-and-Protocol based VLAN II of P0      |
| 1502201C | <u>P0_BSR</u>      | 32    | Broadcast storm rate control of P0         |
| 15022020 | <u>P0_STAG01</u>   | 32    | STAG index 0/1 of P0                       |
| 15022024 | <u>P0_STAG23</u>   | 32    | STAG index 2/3 of P0                       |
| 15022028 | <u>P0_STAG45</u>   | 32    | STAG index 4/5 of P0                       |
| 1502202C | <u>P0_STAG67</u>   | 32    | STAG index 6/7 of P0                       |
| 15022030 | <u>P0_BSR_EXT1</u> | 32    | Broadcast storm rate control I of P0       |
| 15022034 | <u>P0_BSR_EXT2</u> | 32    | Broadcast storm rate control II of P0      |
| 15022038 | <u>P0_BSR_EXT3</u> | 32    | Broadcast storm rate control III of P0     |
| 15022040 | <u>P0_UPW</u>      | 32    | User priority weight of P0                 |
| 15022044 | <u>P0_PEM1</u>     | 32    | User priority egress mapping I of P0       |
| 15022048 | <u>P0_PEM2</u>     | 32    | User priority egress mapping II of P0      |
| 1502204C | <u>P0_PEM3</u>     | 32    | User priority egress mapping III of P0     |
| 15022050 | <u>P0_PEM4</u>     | 32    | User priority egress mapping IV of P0      |
| 15022100 | <u>P1_SSC</u>      | 32    | STP state control of P1                    |
| 15022104 | <u>P1_PCR</u>      | 32    | Port control of P1                         |
| 15022108 | <u>P1_PIC</u>      | 32    | Port IGMP control of P1                    |
| 1502210C | <u>P1_PSC</u>      | 32    | Port security control of P1                |
| 15022110 | <u>P1_PVC</u>      | 32    | Port VLAN control of P1                    |
| 15022114 | <u>P1_PPBV1</u>    | 32    | Port-and-Protocol based VLAN I of P1       |
| 15022118 | <u>P1_PPBV2</u>    | 32    | Port-and-Protocol based VLAN II of P1      |
| 1502211C | <u>P1_BSR</u>      | 32    | Broadcast storm rate control of P1         |
| 15022120 | <u>P1_STAG01</u>   | 32    | STAG index 0/1 of P1                       |
| 15022124 | <u>P1_STAG23</u>   | 32    | STAG index 2/3 of P1                       |
| 15022128 | <u>P1_STAG45</u>   | 32    | STAG index 4/5 of P1                       |
| 1502212C | <u>P1_STAG67</u>   | 32    | STAG index 6/7 of P1                       |
| 15022130 | <u>P1_BSR_EXT1</u> | 32    | Broadcast storm rate control I of P1       |
| 15022134 | <u>P1_BSR_EXT2</u> | 32    | Broadcast storm rate control II of P1      |
| 15022138 | <u>P1_BSR_EXT3</u> | 32    | Broadcast storm rate control III of P1     |
| 15022140 | <u>P1_UPW</u>      | 32    | User priority weight of P1                 |
| 15022144 | <u>P1_PEM1</u>     | 32    | User priority egress mapping I of P1       |
| 15022148 | <u>P1_PEM2</u>     | 32    | User priority egress mapping II of P1      |
| 1502214C | <u>P1_PEM3</u>     | 32    | User priority egress mapping III of P1     |
| 15022150 | <u>P1_PEM4</u>     | 32    | User priority egress mapping IV of P1      |
| 15022200 | <u>P2_SSC</u>      | 32    | STP state control of P2                    |
| 15022204 | <u>P2_PCR</u>      | 32    | Port control of P2                         |
| 15022208 | <u>P2_PIC</u>      | 32    | Port IGMP control of P2                    |
| 1502220C | <u>P2_PSC</u>      | 32    | Port security control of P2                |
| 15022210 | <u>P2_PVC</u>      | 32    | Port VLAN control of P2                    |
| 15022214 | <u>P2_PPBV1</u>    | 32    | Port-and-Protocol based VLAN I of P2       |
| 15022218 | <u>P2_PPBV2</u>    | 32    | Port-and-Protocol based VLAN II of P2      |
| 1502221C | <u>P2_BSR</u>      | 32    | Broadcast storm rate control of P2         |
| 15022220 | <u>P2_STAG01</u>   | 32    | STAG index 0/1 of P2                       |

| Address  | Name               | Width | Register Function                      |
|----------|--------------------|-------|----------------------------------------|
| 15022224 | <b>P2_STAG23</b>   | 32    | STAG index 2/3 of P2                   |
| 15022228 | <b>P2_STAG45</b>   | 32    | STAG index 4/5 of P2                   |
| 1502222C | <b>P2_STAG67</b>   | 32    | STAG index 6/7 of P2                   |
| 15022230 | <b>P2_BSR_EXT1</b> | 32    | Broadcast storm rate control I of P2   |
| 15022234 | <b>P2_BSR_EXT2</b> | 32    | Broadcast storm rate control II of P2  |
| 15022238 | <b>P2_BSR_EXT3</b> | 32    | Broadcast storm rate control III of P2 |
| 15022240 | <b>P2_UPW</b>      | 32    | User priority weight of P2             |
| 15022244 | <b>P2_PEM1</b>     | 32    | User priority egress mapping I of P2   |
| 15022248 | <b>P2_PEM2</b>     | 32    | User priority egress mapping II of P2  |
| 1502224C | <b>P2_PEM3</b>     | 32    | User priority egress mapping III of P2 |
| 15022250 | <b>P2_PEM4</b>     | 32    | User priority egress mapping IV of P2  |
| 15022300 | <b>P3_SSC</b>      | 32    | STP state control of P3                |
| 15022304 | <b>P3_PCR</b>      | 32    | Port control of P3                     |
| 15022308 | <b>P3_PIC</b>      | 32    | Port IGMP control of P3                |
| 1502230C | <b>P3_PSC</b>      | 32    | Port security control of P3            |
| 15022310 | <b>P3_PVC</b>      | 32    | Port VLAN control of P3                |
| 15022314 | <b>P3_PPBV1</b>    | 32    | Port-and-Protocol based VLAN I of P3   |
| 15022318 | <b>P3_PPBV2</b>    | 32    | Port-and-Protocol based VLAN II of P3  |
| 1502231C | <b>P3_BSR</b>      | 32    | Broadcast storm rate control of P3     |
| 15022320 | <b>P3_STAG01</b>   | 32    | STAG index 0/1 of P3                   |
| 15022324 | <b>P3_STAG23</b>   | 32    | STAG index 2/3 of P3                   |
| 15022328 | <b>P3_STAG45</b>   | 32    | STAG index 4/5 of P3                   |
| 1502232C | <b>P3_STAG67</b>   | 32    | STAG index 6/7 of P3                   |
| 15022330 | <b>P3_BSR_EXT1</b> | 32    | Broadcast storm rate control I of P3   |
| 15022334 | <b>P3_BSR_EXT2</b> | 32    | Broadcast storm rate control II of P3  |
| 15022338 | <b>P3_BSR_EXT3</b> | 32    | Broadcast storm rate control III of P3 |
| 15022340 | <b>P3_UPW</b>      | 32    | User priority weight of P3             |
| 15022344 | <b>P3_PEM1</b>     | 32    | User priority egress mapping I of P3   |
| 15022348 | <b>P3_PEM2</b>     | 32    | User priority egress mapping II of P3  |
| 1502234C | <b>P3_PEM3</b>     | 32    | User priority egress mapping III of P3 |
| 15022350 | <b>P3_PEM4</b>     | 32    | User priority egress mapping IV of P3  |
| 15022600 | <b>P6_SSC</b>      | 32    | STP state control of P6                |
| 15022604 | <b>P6_PCR</b>      | 32    | Port control of P6                     |
| 15022608 | <b>P6_PIC</b>      | 32    | Port IGMP control of P6                |
| 1502260C | <b>P6_PSC</b>      | 32    | Port security control of P6            |
| 15022610 | <b>P6_PVC</b>      | 32    | Port VLAN control of P6                |
| 15022614 | <b>P6_PPBV1</b>    | 32    | Port-and-Protocol based VLAN I of P6   |
| 15022618 | <b>P6_PPBV2</b>    | 32    | Port-and-Protocol based VLAN II of P6  |
| 1502261C | <b>P6_BSR</b>      | 32    | Broadcast storm rate control of P6     |
| 15022620 | <b>P6_STAG01</b>   | 32    | STAG index 0/1 of P6                   |
| 15022624 | <b>P6_STAG23</b>   | 32    | STAG index 2/3 of P6                   |
| 15022628 | <b>P6_STAG45</b>   | 32    | STAG index 4/5 of P6                   |
| 1502262C | <b>P6_STAG67</b>   | 32    | STAG index 6/7 of P6                   |
| 15022630 | <b>P6_BSR_EXT1</b> | 32    | Broadcast storm rate control I of P6   |
| 15022634 | <b>P6_BSR_EXT2</b> | 32    | Broadcast storm rate control II of P6  |
| 15022638 | <b>P6_BSR_EXT3</b> | 32    | Broadcast storm rate control III of P6 |
| 15022640 | <b>P6_UPW</b>      | 32    | User priority weight of P6             |
| 15022644 | <b>P6_PEM1</b>     | 32    | User priority egress mapping I of P6   |
| 15022648 | <b>P6_PEM2</b>     | 32    | User priority egress mapping II of P6  |
| 1502264C | <b>P6_PEM3</b>     | 32    | User priority egress mapping III of P6 |

| Address  | Name                         | Width | Register Function                                 |
|----------|------------------------------|-------|---------------------------------------------------|
| 15022650 | <u>P6 PEM4</u>               | 32    | User priority egress mapping IV of P6             |
| 15022654 | <u>P6 BSR EXT4</u>           | 32    | Broadcast storm rate control IV of P6             |
| 15022658 | <u>P6 BSR EXT5</u>           | 32    | Broadcast storm rate control V of P6              |
| 15023000 | <u>PMCR P0</u>               | 32    | Port 0 MAC control register                       |
| 15023004 | <u>PMEEECR P0</u>            | 32    | Port 0 MAC EEE control register                   |
| 15023008 | <u>PMSR P0</u>               | 32    | Port 0 MAC status register                        |
| 15023010 | <u>PINT EN P0</u>            | 32    | Port 0 interrupt enable register                  |
| 15023014 | <u>PINT STS P0</u>           | 32    | Port 0 interrupt status register                  |
| 15023018 | <u>P0 DBG CNT</u>            | 32    | Port 0 debug count                                |
| 15023020 | <u>P0 WOL</u>                | 32    | Port 0 WOL                                        |
| 15023024 | <u>P0 PFC STS</u>            | 32    | Port 0 PFC status                                 |
| 15023030 | <u>P0 PFC RX PSON CNT L</u>  | 32    | Port 0 RX PFC pause on counter for low priority   |
| 15023034 | <u>P0 PFC RX PSON CNT H</u>  | 32    | Port 0 RX PFC pause on counter for high priority  |
| 15023038 | <u>P0 PFC RX PSOFF CNT L</u> | 32    | Port 0 RX PFC pause off counter for low priority  |
| 1502303C | <u>P0 PFC RX PSOFF CNT H</u> | 32    | Port 0 RX PFC pause off counter for high priority |
| 15023040 | <u>P0 PFC TX PSON CNT L</u>  | 32    | Port 0 TX PFC pause on counter for low priority   |
| 15023044 | <u>P0 PFC TX PSON CNT H</u>  | 32    | Port 0 TX PFC pause on counter for high priority  |
| 15023048 | <u>P0 PFC TX PSOFF CNT L</u> | 32    | Port 0 TX PFC pause off counter for low priority  |
| 1502304C | <u>P0 PFC TX PSOFF CNT H</u> | 32    | Port 0 TX PFC pause off counter for high priority |
| 150230B0 | <u>PFC CTRL</u>              | 32    | PFC control register                              |
| 150230B4 | <u>PFC AUTO SYNC DLY SEL</u> | 32    | PFC auto sync delay selection                     |
| 150230B8 | <u>SGMII 2P5G SPD CTRL</u>   | 32    | SGMII speed status control register               |
| 150230C0 | <u>LPDET CTRL</u>            | 32    | Loop detection control register                   |
| 150230C8 | <u>LPDET SA MSB</u>          | 32    | Loop detection SA MSB                             |
| 150230CC | <u>LPDET SA LSB</u>          | 32    | Loop detection SA LSB                             |
| 150230D0 | <u>LPDET RXSA MSB</u>        | 32    | Loop detection RX SA MSB                          |
| 150230E0 | <u>GMACCR</u>                | 32    | Global MAC control register                       |
| 150230E4 | <u>SMACCR0</u>               | 32    | System MAC control register 0                     |
| 150230E8 | <u>SMACCR1</u>               | 32    | System MAC control register 1                     |
| 150230F0 | <u>CKGCR</u>                 | 32    | Clock gating control register                     |
| 150230F4 | <u>GPINT EN</u>              | 32    | Global port interrupt enable register             |
| 150230F8 | <u>GPINT STS</u>             | 32    | Global port interrupt status register             |
| 15023100 | <u>PMCR P1</u>               | 32    | Port 1 MAC control register                       |
| 15023104 | <u>PMEEECR P1</u>            | 32    | Port 1 MAC EEE control register                   |
| 15023108 | <u>PMSR P1</u>               | 32    | Port 1 MAC status register                        |
| 15023110 | <u>PINT EN P1</u>            | 32    | Port 1 interrupt enable register                  |
| 15023114 | <u>PINT STS P1</u>           | 32    | Port 1 interrupt status register                  |
| 15023118 | <u>P1 DBG CNT</u>            | 32    | Port 1 debug count                                |
| 15023120 | <u>P1 WOL</u>                | 32    | Port 1 WOL                                        |
| 15023124 | <u>P1 PFC STS</u>            | 32    | Port 1 PFC status                                 |
| 15023130 | <u>P1 PFC RX PSON CNT L</u>  | 32    | Port 1 RX PFC pause on counter for low priority   |
| 15023134 | <u>P1 PFC RX PSON CNT H</u>  | 32    | Port 1 RX PFC pause on counter for high priority  |
| 15023138 | <u>P1 PFC RX PSOFF CNT L</u> | 32    | Port 1 RX PFC pause off counter for low priority  |
| 1502313C | <u>P1 PFC RX PSOFF CNT H</u> | 32    | Port 1 RX PFC pause off counter for high priority |
| 15023140 | <u>P1 PFC TX PSON CNT L</u>  | 32    | Port 1 TX PFC pause on counter for low priority   |
| 15023144 | <u>P1 PFC TX PSON CNT H</u>  | 32    | Port 1 TX PFC pause on counter for high priority  |
| 15023148 | <u>P1 PFC TX PSOFF CNT L</u> | 32    | Port 1 TX PFC pause off counter for low priority  |
| 1502314C | <u>P1 PFC TX PSOFF CNT H</u> | 32    | Port 1 TX PFC pause off counter for high priority |
| 15023200 | <u>PMCR P2</u>               | 32    | Port 2 MAC control register                       |
| 15023204 | <u>PMEEECR P2</u>            | 32    | PORT 2 MAC EEE control register                   |

| Address  | Name                         | Width | Register Function                                         |
|----------|------------------------------|-------|-----------------------------------------------------------|
| 15023208 | <u>PMSR_P2</u>               | 32    | Port 2 MAC status register                                |
| 15023210 | <u>PINT_EN_P2</u>            | 32    | Port 2 interrupt enable register                          |
| 15023214 | <u>PINT_STS_P2</u>           | 32    | Port 2 interrupt status register                          |
| 15023218 | <u>P2_DBG_CNT</u>            | 32    | Port 2 debug count                                        |
| 15023220 | <u>P2_WOL</u>                | 32    | Port 2 WOL                                                |
| 15023224 | <u>P2_PFC_STS</u>            | 32    | Port 2 PFC status                                         |
| 15023230 | <u>P2_PFC_RX_PSON_CNT_L</u>  | 32    | Port 2 RX PFC pause on counter for low priority           |
| 15023234 | <u>P2_PFC_RX_PSON_CNT_H</u>  | 32    | Port 2 RX PFC pause on counter for high priority          |
| 15023238 | <u>P2_PFC_RX_PSOFF_CNT_L</u> | 32    | Port 2 RX PFC pause off counter for low priority          |
| 1502323C | <u>P2_PFC_RX_PSOFF_CNT_H</u> | 32    | Port 2 RX PFC pause off counter for high priority         |
| 15023240 | <u>P2_PFC_TX_PSON_CNT_L</u>  | 32    | Port 2 TX PFC pause on counter for low priority           |
| 15023244 | <u>P2_PFC_TX_PSON_CNT_H</u>  | 32    | Port 2 TX PFC pause on counter for high priority          |
| 15023248 | <u>P2_PFC_TX_PSOFF_CNT_L</u> | 32    | Port 2 TX PFC pause off counter for low priority          |
| 1502324C | <u>P2_PFC_TX_PSOFF_CNT_H</u> | 32    | Port 2 TX PFC pause off counter for high priority         |
| 15023300 | <u>PMCR_P3</u>               | 32    | Port 3 MAC control register                               |
| 15023304 | <u>PMEEECR_P3</u>            | 32    | Port 3 MAC EEE control register                           |
| 15023308 | <u>PMSR_P3</u>               | 32    | Port 3 MAC status register                                |
| 15023310 | <u>PINT_EN_P3</u>            | 32    | Port 3 interrupt enable register                          |
| 15023314 | <u>PINT_STS_P3</u>           | 32    | Port 3 interrupt status register                          |
| 15023318 | <u>P3_DBG_CNT</u>            | 32    | Port 3 debug count                                        |
| 15023320 | <u>P3_WOL</u>                | 32    | Port 3 WOL                                                |
| 15023324 | <u>P3_PFC_STS</u>            | 32    | Port 3 PFC status                                         |
| 15023330 | <u>P3_PFC_RX_PSON_CNT_L</u>  | 32    | Port 3 RX PFC pause on counter for low priority           |
| 15023334 | <u>P3_PFC_RX_PSON_CNT_H</u>  | 32    | Port 3 RX PFC pause on counter for high priority          |
| 15023338 | <u>P3_PFC_RX_PSOFF_CNT_L</u> | 32    | Port 3 RX PFC pause off counter for low priority          |
| 1502333C | <u>P3_PFC_RX_PSOFF_CNT_H</u> | 32    | Port 3 RX PFC pause off counter for high priority         |
| 15023340 | <u>P3_PFC_TX_PSON_CNT_L</u>  | 32    | Port 3 TX PFC pause on counter for low priority           |
| 15023344 | <u>P3_PFC_TX_PSON_CNT_H</u>  | 32    | Port 3 TX PFC pause on counter for high priority          |
| 15023348 | <u>P3_PFC_TX_PSOFF_CNT_L</u> | 32    | Port 3 TX PFC pause off counter for low priority          |
| 1502334C | <u>P3_PFC_TX_PSOFF_CNT_H</u> | 32    | Port 3 TX PFC pause off counter for high priority         |
| 15023600 | <u>PMCR_P6</u>               | 32    | Port 6 MAC control register                               |
| 15023608 | <u>PMSR_P6</u>               | 32    | Port 6 MAC status register                                |
| 15023610 | <u>PINT_EN_P6</u>            | 32    | Port 6 interrupt enable register                          |
| 15023614 | <u>PINT_STS_P6</u>           | 32    | Port 6 interrupt status register                          |
| 15024000 | <u>TDPC_P0</u>               | 32    | TX drop packet counter of Port 0                          |
| 15024004 | <u>TCRC_P0</u>               | 32    | TX CRC packet counter of Port 0                           |
| 15024008 | <u>TUPC_P0</u>               | 32    | TX unicast packet counter of Port 0                       |
| 1502400C | <u>TMPC_P0</u>               | 32    | TX multicast packet counter of Port 0                     |
| 15024010 | <u>TBPC_P0</u>               | 32    | TX broadcast packet counter of Port 0                     |
| 15024014 | <u>TCEC_P0</u>               | 32    | TX collision event counter of Port 0                      |
| 15024018 | <u>TSCEC_P0</u>              | 32    | TX single collision event counter of Port 0               |
| 1502401C | <u>TMCEC_P0</u>              | 32    | TX multiple collision event counter of Port 0             |
| 15024020 | <u>TDEC_P0</u>               | 32    | TX deferred event counter of Port 0                       |
| 15024024 | <u>TLCEC_P0</u>              | 32    | TX late collision event counter of Port 0                 |
| 15024028 | <u>TXCEC_P0</u>              | 32    | TX excessive collision event counter of Port 0            |
| 1502402C | <u>TPPC_P0</u>               | 32    | TX pause packet counter of Port 0                         |
| 15024030 | <u>TL64PC_P0</u>             | 32    | TX packet length in 64-byte slot packet counter of Port 0 |
| 15024034 | <u>TL65PC_P0</u>             | 32    | TX packet length in 65-byte slot packet counter of Port 0 |



| Address  | Name                  | Width | Register Function                                           |
|----------|-----------------------|-------|-------------------------------------------------------------|
| 15024038 | <u>TL128PC_P0</u>     | 32    | TX packet length in 128-byte slot packet counter of Port 0  |
| 1502403C | <u>TL256PC_P0</u>     | 32    | TX packet length in 256-byte slot packet counter of Port 0  |
| 15024040 | <u>TL512PC_P0</u>     | 32    | TX packet length in 512-byte slot packet counter of Port 0  |
| 15024044 | <u>TL1024PC_P0</u>    | 32    | TX packet length in 1024-byte slot packet counter of Port 0 |
| 15024048 | <u>TOCL_P0</u>        | 32    | TX octet counter low double word of Port 0                  |
| 1502404C | <u>TOCH_P0</u>        | 32    | TX octet counter high double word of Port 0                 |
| 15024060 | <u>RDPC_P0</u>        | 32    | RX drop packet counter of Port 0                            |
| 15024064 | <u>RFPC_P0</u>        | 32    | RX filtering packet counter of Port 0                       |
| 15024068 | <u>RUPC_P0</u>        | 32    | RX unicast packet counter of Port 0                         |
| 1502406C | <u>RMPC_P0</u>        | 32    | RX multicast packet counter of Port 0                       |
| 15024070 | <u>RBPC_P0</u>        | 32    | RX broadcast packet counter of Port 0                       |
| 15024074 | <u>RAEPC_P0</u>       | 32    | RX alignment error packet counter of Port 0                 |
| 15024078 | <u>RCEPC_P0</u>       | 32    | RX CRC(FCS) error packet counter of Port 0                  |
| 1502407C | <u>RUSPC_P0</u>       | 32    | RX undersized packet counter of Port 0                      |
| 15024080 | <u>RFEP_C_P0</u>      | 32    | RX fragmented error packet counter of Port 0                |
| 15024084 | <u>ROSPC_P0</u>       | 32    | RX oversized packet counter of Port 0                       |
| 15024088 | <u>RJEP_C_P0</u>      | 32    | RX Jabber error packet counter of Port 0                    |
| 1502408C | <u>RPPC_P0</u>        | 32    | RX pause packet counter of Port 0                           |
| 15024090 | <u>RL64PC_P0</u>      | 32    | RX packet length in 64-byte slot packet counter of Port 0   |
| 15024094 | <u>RL65PC_P0</u>      | 32    | RX packet length in 65-byte slot packet counter of Port 0   |
| 15024098 | <u>RL128PC_P0</u>     | 32    | RX packet length in 128-byte slot packet counter of Port 0  |
| 1502409C | <u>RL256PC_P0</u>     | 32    | RX packet length in 256-byte slot packet counter of Port 0  |
| 150240A0 | <u>RL512PC_P0</u>     | 32    | RX packet length in 512-byte slot packet counter of Port 0  |
| 150240A4 | <u>RL1024PC_P0</u>    | 32    | RX packet length in 1024-byte slot packet counter of Port 0 |
| 150240A8 | <u>ROCL_P0</u>        | 32    | RX octet counter low double word of Port 0                  |
| 150240AC | <u>ROCH_P0</u>        | 32    | Rx octet counter high double word of Port 0                 |
| 150240B0 | <u>RDPC_CTRL_P0</u>   | 32    | RX CTRL drop packet counter of Port 0                       |
| 150240B4 | <u>RDPC_ING_P0</u>    | 32    | RX ingress drop packet counter of Port 0                    |
| 150240B8 | <u>RDPC_ARL_P0</u>    | 32    | RX ARL drop packet counter of Port 0                        |
| 150240D0 | <u>TMIB_HF_STS_P0</u> | 32    | TX port MIB counter half full status of Port 0              |
| 150240D4 | <u>RMIB_HF_STS_P0</u> | 32    | RX port MIB counter half full status of Port 0              |
| 15024100 | <u>TDPC_P1</u>        | 32    | TX drop packet counter of Port 1                            |
| 15024104 | <u>TCRC_P1</u>        | 32    | TX CRC packet counter of Port 1                             |
| 15024108 | <u>TUPC_P1</u>        | 32    | TX unicast packet counter of Port 1                         |
| 1502410C | <u>TMPC_P1</u>        | 32    | TX multicast packet counter of Port 1                       |
| 15024110 | <u>TBPC_P1</u>        | 32    | TX broadcast packet counter of Port 1                       |
| 15024114 | <u>TCEC_P1</u>        | 32    | TX collision event counter of Port 1                        |
| 15024118 | <u>TSCEC_P1</u>       | 32    | TX single collision event counter of Port 1                 |
| 1502411C | <u>TMCEC_P1</u>       | 32    | TX multiple collision event counter of Port 1               |
| 15024120 | <u>TDEC_P1</u>        | 32    | TX deferred event counter of Port 1                         |
| 15024124 | <u>TLCEC_P1</u>       | 32    | TX late collision event counter of Port 1                   |
| 15024128 | <u>TXCEC_P1</u>       | 32    | TX excessive collision event counter of Port 1              |

| Address  | Name                  | Width | Register Function                                           |
|----------|-----------------------|-------|-------------------------------------------------------------|
| 1502412C | <u>TPPC P1</u>        | 32    | TX pause packet counter of Port 1                           |
| 15024130 | <u>TL64PC P1</u>      | 32    | TX packet length in 64-byte slot packet counter of Port 1   |
| 15024134 | <u>TL65PC P1</u>      | 32    | TX packet length in 65-byte slot packet counter of Port 1   |
| 15024138 | <u>TL128PC P1</u>     | 32    | TX packet length in 128-byte slot packet counter of Port 1  |
| 1502413C | <u>TL256PC P1</u>     | 32    | TX packet length in 256-byte slot packet counter of Port 1  |
| 15024140 | <u>TL512PC P1</u>     | 32    | TX packet length in 512-byte slot packet counter of Port 1  |
| 15024144 | <u>TL1024PC P1</u>    | 32    | TX packet length in 1024-byte slot packet counter of Port 1 |
| 15024148 | <u>TOCL P1</u>        | 32    | TX octet counter low double word of Port 1                  |
| 1502414C | <u>TOCH P1</u>        | 32    | TX octet counter high double word of Port 1                 |
| 15024160 | <u>RDPC P1</u>        | 32    | RX drop packet counter of Port 1                            |
| 15024164 | <u>RFPC P1</u>        | 32    | RX filtering packet counter of Port 1                       |
| 15024168 | <u>RUPC P1</u>        | 32    | RX unicast packet counter of Port 1                         |
| 1502416C | <u>RMPC P1</u>        | 32    | RX multicast packet counter of Port 1                       |
| 15024170 | <u>RBPC P1</u>        | 32    | RX broadcast packet counter of Port 1                       |
| 15024174 | <u>RAEPC P1</u>       | 32    | RX alignment error packet counter of Port 1                 |
| 15024178 | <u>RCEPC P1</u>       | 32    | RX CRC(FCS) error packet counter of Port 1                  |
| 1502417C | <u>RUSPC P1</u>       | 32    | RX undersized packet counter of Port 1                      |
| 15024180 | <u>RFEP C1</u>        | 32    | RX fragmented error packet counter of Port 1                |
| 15024184 | <u>ROSPC P1</u>       | 32    | RX oversized packet counter of Port 1                       |
| 15024188 | <u>RJEP C1</u>        | 32    | RX Jabber error packet counter of Port 1                    |
| 1502418C | <u>RPPC P1</u>        | 32    | RX pause packet counter of Port 1                           |
| 15024190 | <u>RL64PC P1</u>      | 32    | RX packet length in 64-byte slot packet counter of Port 1   |
| 15024194 | <u>RL65PC P1</u>      | 32    | RX packet length in 65-byte slot packet counter of Port 1   |
| 15024198 | <u>RL128PC P1</u>     | 32    | RX packet length in 128-byte slot packet counter of Port 1  |
| 1502419C | <u>RL256PC P1</u>     | 32    | RX packet length in 256-byte slot packet counter of Port 1  |
| 150241A0 | <u>RL512PC P1</u>     | 32    | RX packet length in 512-byte slot packet counter of Port 1  |
| 150241A4 | <u>RL1024PC P1</u>    | 32    | RX packet length in 1024-byte slot packet counter of Port 1 |
| 150241A8 | <u>ROCL P1</u>        | 32    | RX octet counter low double word of Port 1                  |
| 150241AC | <u>ROCH P1</u>        | 32    | Rx octet counter high double word of Port 1                 |
| 150241B0 | <u>RDPC CTRL P1</u>   | 32    | RX CTRL drop packet counter of Port 1                       |
| 150241B4 | <u>RDPC ING P1</u>    | 32    | RX ingress drop packet counter of Port 1                    |
| 150241B8 | <u>RDPC ARL P1</u>    | 32    | RX ARL drop packet counter of Port 1                        |
| 150241D0 | <u>TMIB HF STS P1</u> | 32    | TX port MIB counter half full status of Port 1              |
| 150241D4 | <u>RMIB HF STS P1</u> | 32    | RX port MIB counter half full status of Port 1              |
| 15024200 | <u>TDPC P2</u>        | 32    | TX drop packet counter of Port 2                            |
| 15024204 | <u>TCRC P2</u>        | 32    | TX CRC packet counter of Port 2                             |
| 15024208 | <u>TUPC P2</u>        | 32    | TX unicast packet counter of Port 2                         |
| 1502420C | <u>TMPC P2</u>        | 32    | TX multicast packet counter of Port 2                       |
| 15024210 | <u>TBPC P2</u>        | 32    | TX broadcast packet counter of Port 2                       |
| 15024214 | <u>TCEC P2</u>        | 32    | TX collision event counter of Port 2                        |
| 15024218 | <u>TSCEC P2</u>       | 32    | TX single collision event counter of Port 2                 |



| Address  | Name                  | Width | Register Function                                           |
|----------|-----------------------|-------|-------------------------------------------------------------|
| 1502421C | <u>TMCEC_P2</u>       | 32    | TX multiple collision event counter of Port 2               |
| 15024220 | <u>TDEC_P2</u>        | 32    | TX deferred event counter of Port 2                         |
| 15024224 | <u>TLCEC_P2</u>       | 32    | TX late collision event counter of Port 2                   |
| 15024228 | <u>TXCEC_P2</u>       | 32    | TX excessive collision event counter of Port 2              |
| 1502422C | <u>TPPC_P2</u>        | 32    | TX pause packet counter of Port 2                           |
| 15024230 | <u>TL64PC_P2</u>      | 32    | TX packet length in 64-byte slot packet counter of Port 2   |
| 15024234 | <u>TL65PC_P2</u>      | 32    | TX packet length in 65-byte slot packet counter of Port 2   |
| 15024238 | <u>TL128PC_P2</u>     | 32    | TX packet length in 128-byte slot packet counter of Port 2  |
| 1502423C | <u>TL256PC_P2</u>     | 32    | TX packet length in 256-byte slot packet counter of Port 2  |
| 15024240 | <u>TL512PC_P2</u>     | 32    | TX packet length in 512-byte slot packet counter of Port 2  |
| 15024244 | <u>TL1024PC_P2</u>    | 32    | TX packet length in 1024-byte slot packet counter of Port 2 |
| 15024248 | <u>TOCL_P2</u>        | 32    | TX octet counter low double word of Port 2                  |
| 1502424C | <u>TOCH_P2</u>        | 32    | TX octet counter high double word of Port 2                 |
| 15024260 | <u>RDPC_P2</u>        | 32    | RX drop packet counter of Port 2                            |
| 15024264 | <u>RFPC_P2</u>        | 32    | RX filtering packet counter of Port 2                       |
| 15024268 | <u>RUPC_P2</u>        | 32    | RX unicast packet counter of Port 2                         |
| 1502426C | <u>RMPC_P2</u>        | 32    | RX multicast packet counter of Port 2                       |
| 15024270 | <u>RBPC_P2</u>        | 32    | RX broadcast packet counter of Port 2                       |
| 15024274 | <u>RAEPC_P2</u>       | 32    | RX alignment error packet counter of Port 2                 |
| 15024278 | <u>RCEPC_P2</u>       | 32    | RX CRC(FCS) error packet counter of Port 2                  |
| 1502427C | <u>RUSPC_P2</u>       | 32    | RX undersized packet counter of Port 2                      |
| 15024280 | <u>RFEP_C_P2</u>      | 32    | RX fragmented error packet counter of Port 2                |
| 15024284 | <u>ROSPC_P2</u>       | 32    | RX oversized packet counter of Port 2                       |
| 15024288 | <u>RJEP_C_P2</u>      | 32    | RX Jabber error packet counter of Port 2                    |
| 1502428C | <u>RPPC_P2</u>        | 32    | RX pause packet counter of Port 2                           |
| 15024290 | <u>RL64PC_P2</u>      | 32    | RX packet length in 64-byte slot packet counter of Port 2   |
| 15024294 | <u>RL65PC_P2</u>      | 32    | RX packet length in 65-byte slot packet counter of Port 2   |
| 15024298 | <u>RL128PC_P2</u>     | 32    | RX packet length in 128-byte slot packet counter of Port 2  |
| 1502429C | <u>RL256PC_P2</u>     | 32    | RX packet length in 256-byte slot packet counter of Port 2  |
| 150242A0 | <u>RL512PC_P2</u>     | 32    | RX packet length in 512-byte slot packet counter of Port 2  |
| 150242A4 | <u>RL1024PC_P2</u>    | 32    | RX packet length in 1024-byte slot packet counter of Port 2 |
| 150242A8 | <u>ROCL_P2</u>        | 32    | RX octet counter low double word of Port 2                  |
| 150242AC | <u>ROCH_P2</u>        | 32    | Rx octet counter high double word of Port 2                 |
| 150242B0 | <u>RDPC_CTRL_P2</u>   | 32    | RX CTRL drop packet counter of Port 2                       |
| 150242B4 | <u>RDPC_ING_P2</u>    | 32    | RX ingress drop packet counter of Port 2                    |
| 150242B8 | <u>RDPC_ARL_P2</u>    | 32    | RX ARL drop packet counter of Port 2                        |
| 150242D0 | <u>TMIB_HF_STS_P2</u> | 32    | TX port MIB counter half full status of Port 2              |
| 150242D4 | <u>RMIB_HF_STS_P2</u> | 32    | RX port MIB counter half full status of Port 2              |
| 15024300 | <u>TDPC_P3</u>        | 32    | TX drop packet counter of Port 3                            |
| 15024304 | <u>TCRC_P3</u>        | 32    | TX CRC packet counter of Port 3                             |
| 15024308 | <u>TUPC_P3</u>        | 32    | TX unicast packet counter of Port 3                         |

| Address  | Name                  | Width | Register Function                                           |
|----------|-----------------------|-------|-------------------------------------------------------------|
| 1502430C | <u>TMPC_P3</u>        | 32    | TX multicast packet counter of Port 3                       |
| 15024310 | <u>TBPC_P3</u>        | 32    | TX broadcast packet counter of Port 3                       |
| 15024314 | <u>TCEC_P3</u>        | 32    | TX collision event counter of Port 3                        |
| 15024318 | <u>TSCEC_P3</u>       | 32    | TX single collision event counter of Port 3                 |
| 1502431C | <u>TMCEC_P3</u>       | 32    | TX multiple collision event counter of Port 3               |
| 15024320 | <u>TDEC_P3</u>        | 32    | TX deferred event counter of Port 3                         |
| 15024324 | <u>TLCEC_P3</u>       | 32    | TX late collision event counter of Port 3                   |
| 15024328 | <u>TXCEC_P3</u>       | 32    | TX excessive collision event counter of Port 3              |
| 1502432C | <u>TPPC_P3</u>        | 32    | TX pause packet counter of Port 3                           |
| 15024330 | <u>TL64PC_P3</u>      | 32    | TX packet length in 64-byte slot packet counter of Port 3   |
| 15024334 | <u>TL65PC_P3</u>      | 32    | TX packet length in 65-byte slot packet counter of Port 3   |
| 15024338 | <u>TL128PC_P3</u>     | 32    | TX packet length in 128-byte slot packet counter of Port 3  |
| 1502433C | <u>TL256PC_P3</u>     | 32    | TX packet length in 256-byte slot packet counter of Port 3  |
| 15024340 | <u>TL512PC_P3</u>     | 32    | TX packet length in 512-byte slot packet counter of Port 3  |
| 15024344 | <u>TL1024PC_P3</u>    | 32    | TX packet length in 1024-byte slot packet counter of Port 3 |
| 15024348 | <u>TOCL_P3</u>        | 32    | TX octet counter low double word of Port 3                  |
| 1502434C | <u>TOCH_P3</u>        | 32    | TX octet counter high double word of Port 3                 |
| 15024360 | <u>RDPC_P3</u>        | 32    | RX drop packet counter of Port 3                            |
| 15024364 | <u>RFPC_P3</u>        | 32    | RX filtering packet counter of Port 3                       |
| 15024368 | <u>RUPC_P3</u>        | 32    | RX unicast packet counter of Port 3                         |
| 1502436C | <u>RMPC_P3</u>        | 32    | RX multicast packet counter of Port 3                       |
| 15024370 | <u>RBPC_P3</u>        | 32    | RX broadcast packet counter of Port 3                       |
| 15024374 | <u>RAEPC_P3</u>       | 32    | RX alignment error packet counter of Port 3                 |
| 15024378 | <u>RCEPC_P3</u>       | 32    | RX CRC(FCS) error packet counter of Port 3                  |
| 1502437C | <u>RUSPC_P3</u>       | 32    | RX undersized packet counter of Port 3                      |
| 15024380 | <u>RFEP_C_P3</u>      | 32    | RX fragmented error packet counter of Port 3                |
| 15024384 | <u>ROSPC_P3</u>       | 32    | RX oversized packet counter of Port 3                       |
| 15024388 | <u>RJEP_C_P3</u>      | 32    | RX Jabber error packet counter of Port 3                    |
| 1502438C | <u>RPPC_P3</u>        | 32    | RX pause packet counter of Port 3                           |
| 15024390 | <u>RL64PC_P3</u>      | 32    | RX packet length in 64-byte slot packet counter of Port 3   |
| 15024394 | <u>RL65PC_P3</u>      | 32    | RX packet length in 65-byte slot packet counter of Port 3   |
| 15024398 | <u>RL128PC_P3</u>     | 32    | RX packet length in 128-byte slot packet counter of Port 3  |
| 1502439C | <u>RL256PC_P3</u>     | 32    | RX packet length in 256-byte slot packet counter of Port 3  |
| 150243A0 | <u>RL512PC_P3</u>     | 32    | RX packet length in 512-byte slot packet counter of Port 3  |
| 150243A4 | <u>RL1024PC_P3</u>    | 32    | RX packet length in 1024-byte slot packet counter of Port 3 |
| 150243A8 | <u>ROCL_P3</u>        | 32    | RX octet counter low double word of Port 3                  |
| 150243AC | <u>ROCH_P3</u>        | 32    | Rx octet counter high double word of Port 3                 |
| 150243B0 | <u>RDPC_CTRL_P3</u>   | 32    | RX CTRL drop packet counter of Port 3                       |
| 150243B4 | <u>RDPC_ING_P3</u>    | 32    | RX ingress drop packet counter of Port 3                    |
| 150243B8 | <u>RDPC_ARL_P3</u>    | 32    | RX ARL drop packet counter of Port 3                        |
| 150243D0 | <u>TMIB_HF_STS_P3</u> | 32    | TX port MIB counter half full status of Port 3              |

| Address  | Name                         | Width | Register Function                                           |
|----------|------------------------------|-------|-------------------------------------------------------------|
| 150243D4 | <b><u>RMIB_HF_STS_P3</u></b> | 32    | RX port MIB counter half full status of Port 3              |
| 15024600 | <b><u>TDPC_P6</u></b>        | 32    | TX drop packet counter of Port 6                            |
| 15024604 | <b><u>TCRC_P6</u></b>        | 32    | TX CRC packet counter of Port 6                             |
| 15024608 | <b><u>TUPC_P6</u></b>        | 32    | TX unicast packet counter of Port 6                         |
| 1502460C | <b><u>TMPC_P6</u></b>        | 32    | TX multicast packet counter of Port 6                       |
| 15024610 | <b><u>TBPC_P6</u></b>        | 32    | TX broadcast packet counter of Port 6                       |
| 15024614 | <b><u>TCEC_P6</u></b>        | 32    | TX collision event counter of Port 6                        |
| 15024618 | <b><u>TSCEC_P6</u></b>       | 32    | TX single collision event counter of Port 6                 |
| 1502461C | <b><u>TMCEC_P6</u></b>       | 32    | TX multiple collision event counter of Port 6               |
| 15024620 | <b><u>TDEC_P6</u></b>        | 32    | TX deferred event counter of Port 6                         |
| 15024624 | <b><u>TLCEC_P6</u></b>       | 32    | TX late collision event counter of Port 6                   |
| 15024628 | <b><u>TXCEC_P6</u></b>       | 32    | TX excessive collision event counter of Port 6              |
| 1502462C | <b><u>TPPC_P6</u></b>        | 32    | TX pause packet counter of Port 6                           |
| 15024630 | <b><u>TL64PC_P6</u></b>      | 32    | TX packet length in 64-byte slot packet counter of Port 6   |
| 15024634 | <b><u>TL65PC_P6</u></b>      | 32    | TX packet length in 65-byte slot packet counter of Port 6   |
| 15024638 | <b><u>TL128PC_P6</u></b>     | 32    | TX packet length in 128-byte slot packet counter of Port 6  |
| 1502463C | <b><u>TL256PC_P6</u></b>     | 32    | TX packet length in 256-byte slot packet counter of Port 6  |
| 15024640 | <b><u>TL512PC_P6</u></b>     | 32    | TX packet length in 512-byte slot packet counter of Port 6  |
| 15024644 | <b><u>TL1024PC_P6</u></b>    | 32    | TX packet length in 1024-byte slot packet counter of Port 6 |
| 15024648 | <b><u>TOCL_P6</u></b>        | 32    | TX octet counter low double word of Port 6                  |
| 1502464C | <b><u>TOCH_P6</u></b>        | 32    | TX octet counter high double word of Port 6                 |
| 15024660 | <b><u>RDPC_P6</u></b>        | 32    | RX drop packet counter of Port 6                            |
| 15024664 | <b><u>RFPC_P6</u></b>        | 32    | RX filtering packet counter of Port 6                       |
| 15024668 | <b><u>RUPC_P6</u></b>        | 32    | RX unicast packet counter of Port 6                         |
| 1502466C | <b><u>RMPC_P6</u></b>        | 32    | RX multicast packet counter of Port 6                       |
| 15024670 | <b><u>RBPC_P6</u></b>        | 32    | RX broadcast packet counter of Port 6                       |
| 15024674 | <b><u>RAEPC_P6</u></b>       | 32    | RX alignment error packet counter of Port 6                 |
| 15024678 | <b><u>RCEPC_P6</u></b>       | 32    | RX CRC(FCS) error packet counter of Port 6                  |
| 1502467C | <b><u>RUSPC_P6</u></b>       | 32    | RX undersized packet counter of Port 6                      |
| 15024680 | <b><u>RFEPC_P6</u></b>       | 32    | RX fragmented error packet counter of Port 6                |
| 15024684 | <b><u>ROSPC_P6</u></b>       | 32    | RX oversized packet counter of Port 6                       |
| 15024688 | <b><u>RJEPC_P6</u></b>       | 32    | RX Jabber error packet counter of Port 6                    |
| 1502468C | <b><u>RPPC_P6</u></b>        | 32    | RX pause packet counter of Port 6                           |
| 15024690 | <b><u>RL64PC_P6</u></b>      | 32    | RX packet length in 64-byte slot packet counter of Port 6   |
| 15024694 | <b><u>RL65PC_P6</u></b>      | 32    | RX packet length in 65-byte slot packet counter of Port 6   |
| 15024698 | <b><u>RL128PC_P6</u></b>     | 32    | RX packet length in 128-byte slot packet counter of Port 6  |
| 1502469C | <b><u>RL256PC_P6</u></b>     | 32    | RX packet length in 256-byte slot packet counter of Port 6  |
| 150246A0 | <b><u>RL512PC_P6</u></b>     | 32    | RX packet length in 512-byte slot packet counter of Port 6  |
| 150246A4 | <b><u>RL1024PC_P6</u></b>    | 32    | RX packet length in 1024-byte slot packet counter of Port 6 |
| 150246A8 | <b><u>ROCL_P6</u></b>        | 32    | RX octet counter low double word of Port 6                  |
| 150246AC | <b><u>ROCH_P6</u></b>        | 32    | Rx octet counter high double word of Port 6                 |

| Address  | Name                   | Width | Register Function                                       |
|----------|------------------------|-------|---------------------------------------------------------|
| 150246B0 | <u>RDPC_CTRL_P6</u>    | 32    | RX CTRL drop packet counter of Port 6                   |
| 150246B4 | <u>RDPC_ING_P6</u>     | 32    | RX ingress drop packet counter of Port 6                |
| 150246B8 | <u>RDPC_ARL_P6</u>     | 32    | RX ARL drop packet counter of Port 6                    |
| 150246D0 | <u>TMIB_HF_STS_P6</u>  | 32    | TX port MIB counter half full status of Port 6          |
| 150246D4 | <u>RMIB_HF_STS_P6</u>  | 32    | RX port MIB counter half full status of Port 6          |
| 15024F00 | <u>AE0CNT</u>          | 32    | ACL event 0 counter                                     |
| 15024F04 | <u>AE1CNT</u>          | 32    | ACL event 1 counter                                     |
| 15024F08 | <u>AE2CNT</u>          | 32    | ACL event 2 counter                                     |
| 15024F0C | <u>AE3CNT</u>          | 32    | ACL event 3 counter                                     |
| 15024F10 | <u>AE4CNT</u>          | 32    | ACL event 4 counter                                     |
| 15024F14 | <u>AE5CNT</u>          | 32    | ACL event 5 counter                                     |
| 15024F18 | <u>AE6CNT</u>          | 32    | ACL event 6 counter                                     |
| 15024F1C | <u>AE7CNT</u>          | 32    | ACL event 7 counter                                     |
| 15024FE0 | <u>MIBCCR</u>          | 32    | MIB counter control                                     |
| 15024FE4 | <u>AECRR</u>           | 32    | ARL event counter control                               |
| 15024FE8 | <u>AEMIB_HF_STS</u>    | 32    | ARL event MIB counter half full status                  |
| 15024FF0 | <u>MIBHF_INT_EN</u>    | 32    | Port/ARL MIB counter half full interrupt enable         |
| 15024FF4 | <u>MIBHF_INT_STS</u>   | 32    | Port/ARL MIB counter half full interrupt status         |
| 15027000 | <u>SYS_CTRL</u>        | 32    | System control                                          |
| 15027008 | <u>SYS_INT_EN</u>      | 32    | System interrupt enable                                 |
| 1502700C | <u>SYS_INT_STS</u>     | 32    | System interrupt status                                 |
| 15027014 | <u>PMDC_CFG</u>        | 32    | PMDC control register                                   |
| 15027018 | <u>PHY_POLL</u>        | 32    | PHY polling and SMI master control register             |
| 1502701C | <u>PHY_IAC</u>         | 32    | PHY indirect access control                             |
| 15027020 | <u>PSR_P3_P0</u>       | 32    | PHY status register for Port 3 ~ Port 0                 |
| 15027024 | <u>PSR_P6_P4</u>       | 32    | PHY status register for Port 6 ~ Port 4                 |
| 15027028 | <u>PAUSE_CAP_P6_P0</u> | 32    | MAC pause TX/RX capability register for Port 6 ~ Port 0 |
| 15027124 | <u>EEPR_STS</u>        | 32    | EEPROM status register                                  |

15020004 CFC CPU forward control 00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23       | 22 | 21 | 20 | 19            | 18          | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----------|----|----|----|---------------|-------------|----|----|
| Name  | REV0 |    |    |    |    |    |    |    |          |    |    |    | MIRRO<br>R_EN | MIRROR_PORT |    |    |
| Type  | RW   |    |    |    |    |    |    |    |          |    |    |    | RW            | RW          |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0        | 0  | 0  | 0  | 0             | 0           | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7        | 6  | 5  | 4  | 3             | 2           | 1  | 0  |
| Name  | REV1 |    |    |    |    |    |    |    | CPU_PMAP |    |    |    |               |             |    |    |
| Type  | RW   |    |    |    |    |    |    |    | RW       |    |    |    |               |             |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0        | 0  | 0  | 0  | 0             | 0           | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                             |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 31:20  | REV0        | <b>Reserved</b>                                                                                                                         |
| 19     | MIRROR_EN   | <b>Mirror Port Enable</b><br><br>Enable the mirror port specified in MIRROR_PORT.<br><br>0: No mirror available<br><br>1: Enable mirror |
| 18:16  | MIRROR_PORT | <b>Mirror Port Number</b><br><br>Set the mirror port number.<br><br>3'h0: Port 0<br><br>...<br><br>3'h7: Port 7                         |
| 15:8   | REV1        | <b>Reserved</b>                                                                                                                         |
| 7:0    | CPU_PMAP    | <b>CPU Port Bit Map</b><br><br>Provide multiple CPU port selection.<br><br>[0]: Port 0<br><br>[1]: Port 1<br><br>...<br><br>[7]: Port 7 |

15020008      AISR      ACL interrupt status      00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | ACL_ISR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | ACL_ISR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                                     |
|--------|---------|---------------------------------------------------------------------------------|
| 31:0   | ACL_ISR | <b>ACL Interrupt Status for entry 0~31</b><br>(Refer to ACL Rule Control Table) |

1502000C AGC ARL global control 0007181D

| Bit   | 31           | 30        | 29        | 28        | 27   | 26 | 25 | 24            | 23       | 22          | 21           | 20        | 19        | 18        | 17            | 16        |
|-------|--------------|-----------|-----------|-----------|------|----|----|---------------|----------|-------------|--------------|-----------|-----------|-----------|---------------|-----------|
| Name  | MLDv2_int_en | TICK_SEL  | PCP_AWARE | SNOP_DROP | REV0 |    |    | MAC_SARLP_DIS | REV1     |             | MAC_HASH_SEL |           | REV2      | ACL_INT   | VLAN_INT      | ADDR_INT  |
| Type  | RW           | RW        | RW        | RW        | RO   |    |    | RW            | RO       |             | RW           |           | RO        | RO        | RO            | RO        |
| Reset | 0            | 0         | 0         | 0         | 0    | 0  | 0  | 0             | 0        | 0           | 0            | 0         | 0         | 1         | 1             | 1         |
| Bit   | 15           | 14        | 13        | 12        | 11   | 10 | 9  | 8             | 7        | 6           | 5            | 4         | 3         | 2         | 1             | 0         |
| Name  | RATE_COMP    | COMP_BNUM |           |           |      |    |    |               | LOCAL_EN | ARLP_ADDING | ACL_MULT     | L2LEN_CHK | CTRL_DROP | VLAN4_CPU | ARLP_PRIORITY | ALR_RST_N |
| Type  | RW           | RW        |           |           |      |    |    |               | RW       | RW          | RW           | RW        | RW        | RW        | RW            | RW        |
| Reset | 0            | 0         | 0         | 1         | 1    | 0  | 0  | 0             | 0        | 0           | 0            | 1         | 1         | 1         | 0             | 1         |

| Bit(s) | Name          | Description                                                                                                                                                                                                                                                                                                                                     |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MLDv2_int_en  | <b>MLDv2 interrupt enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                                                                                |
| 30     | TICK_SEL      | <b>Select 64Kbps or 1Mbps tick in ACL rate control for supporting 2.5G rate limit</b><br><br>0: 64Kbps tick<br><br>1: 1Mbps tick                                                                                                                                                                                                                |
| 29     | PCP_AWARE     | <b>Priority-tag aware for dump switch</b><br><br>0: Disable priority-tag<br><br>1: Enable priority-tag                                                                                                                                                                                                                                          |
| 28     | SNOP_DROP     | <b>IGMP snooping can learn the dropped frame</b><br><br>0: IGMP snoop will ignore the dropped frame<br><br>1: IGMP snoop will learn the dropped frame                                                                                                                                                                                           |
| 27:25  | REV0          | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                 |
| 24     | MAC_SARLP_DIS | <b>Disable oldest address replacement function for mac address learning.</b><br><br>In default, oldest mac address will be replaced by new address when there are no empty entry for mac address learning<br><br>Manual update address table won't be affected<br><br>0: Replace oldest mac address<br><br>1: Not to replace oldest mac address |
| 23:22  | REV1          | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                 |
| 21:20  | MAC_HASH_SEL  | <b>Select MAC Table Hash Function</b><br><br>2'b00: XOR<br><br>2'b01: CRC16                                                                                                                                                                                                                                                                     |

| Bit(s) | Name        | Description                                                                                                                                                                                                                         |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |             | 2'b10: CRC32                                                                                                                                                                                                                        |
| 19     | REV2        | <b>Reserved</b>                                                                                                                                                                                                                     |
| 18     | ACL_INT     | <b>Access Control List (ACL) Table Initialization Done</b><br><br>0: ACL Table is busy.<br><br>1: ACL Table is cleared.                                                                                                             |
| 17     | VLAN_INT    | <b>VLAN Table Initialization Done</b><br><br>0: VLAN Table is busy.<br><br>1: VLAN Table is cleaned.                                                                                                                                |
| 16     | ADDR_INT    | <b>ADDR Table Initialization Done</b><br><br>0: ADDR Table is busy.<br><br>1: ADDR Table is cleaned.                                                                                                                                |
| 15     | RATE_COMP   | <b>Rate Limit Compensation</b><br><br>Add or subtract the specific byte number while calculating the packet length.<br><br>0: Add<br><br>1: Minus                                                                                   |
| 14:8   | COMP_BNUM   | <b>Compensation Byte Number</b><br><br>The added/subtracted byte number for the rate limit or the meter table                                                                                                                       |
| 7      | LOCAL_EN    | <b>Local Port Forwarding Enable</b><br><br>0: Drop frames at the local port.<br><br>1: Allow frame forwarding to the local port.                                                                                                    |
| 6      | ARL_PADDING | <b>ARL Data Padding</b><br><br>Set ARL to add byte padding up to 46 bytes when the length of the data field of the incoming frame is less than 46 bytes.<br><br>0: Disable (default)<br><br>1: Enable                               |
| 5      | ACL_MULT    | <b>Enable Multiple ACL Hit</b><br><br>0: Only the first hit ACL entry<br><br>1: Allow multiple ACL hit entries on Rate, Interrupt, and MIB.                                                                                         |
| 4      | L2LEN_CHK   | <b>Layer 2 Frame Length Check</b><br><br>Enable a length check on length-encapsulated frame. Drop length error frames when the value of the ELEN field of this frame is bigger than the length of the data field.<br><br>0: Disable |



| Bit(s) | Name      | Description                                                                                                                                                       |
|--------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3      | CTRL_DROP | <p>1: Enable</p> <p><b>MAC Control Frame Drop</b></p> <p>Drop MAC frames with ETYPE=0x8808.</p> <p>0: Disable (default)</p>                                       |
| 2      | VLAN4CPU  | <p>1: Enable</p> <p><b>TO_CPU VLAN Member</b></p> <p>Set the TO_CPU frame to check VLAN members.</p> <p>0: Ignore VLAN members.</p> <p>1: Check VLAN members.</p> |
| 1      | ARL_PRI   | <p><b>ARL Resolution Priority</b></p> <p>0: P0 is the lowest priority.</p> <p>1: P0 is the highest priority.</p>                                                  |
| 0      | ALR_RST_N | <p><b>ARL Enable (Soft Reset)</b></p> <p>0: Reset the ARL engine.</p> <p>1: Enable ARL engine.</p>                                                                |

| 15020010 | MFC     |    |    |    |    |    |    |    | MAC forward control |    |    |    |    |    |    |    | FFFFFFF |
|----------|---------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|----|----|---------|
| Bit      | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |         |
| Name     | BC_FFP  |    |    |    |    |    |    |    | UNM_FFP             |    |    |    |    |    |    |    |         |
| Type     | RW      |    |    |    |    |    |    |    | RW                  |    |    |    |    |    |    |    |         |
| Reset    | 1       | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1                   | 1  | 1  | 1  | 1  | 1  | 1  | 1  |         |
| Bit      | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |         |
| Name     | UNU_FFP |    |    |    |    |    |    |    | QRY_FFP             |    |    |    |    |    |    |    |         |
| Type     | RW      |    |    |    |    |    |    |    | RW                  |    |    |    |    |    |    |    |         |
| Reset    | 1       | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1                   | 1  | 1  | 1  | 1  | 1  | 1  | 1  |         |

| Bit(s) | Name    | Description                                                                                                                                                                                                                                                                                          |
|--------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | BC_FFP  | <b>Broadcast Frame Flooding Ports</b><br><br>If MAC receives broadcast frames, this field indicates the flooding ports.<br><br>[NOTE]<br><br>1. The flooding ports exclude the received port on the switch.<br><br>2. Frame dropped though BC_FFP=7'b0                                               |
| 23:16  | UNM_FFP | <b>Unknown Multicast Frame Flooding Ports</b><br><br>If MAC receives multicast frames which can not be found on the ARL, this field indicates the flooding ports.<br><br>[NOTE]<br><br>1. The flooding ports exclude the received port by HW.<br><br>2. Frame dropped though UNM_FFP=7'b0.           |
| 15:8   | UNU_FFP | <b>Unknown Unicast Frame Flooding Ports</b><br><br>If MAC receives the unicast or multicast frames which can not be found on the ARL, the field indicates the flooding ports.<br><br>[NOTE]<br><br>1. The flooding ports exclude the received port by HW<br><br>2. Frame dropped though UNU_FFP=7'b0 |
| 7:0    | QRY_FFP | <b>IGMP/MLD Query Frame Flooding Ports</b><br><br>If MAC receives IGMP/MLD query frame, this field indicates the flooding ports.<br><br>[NOTE]<br><br>1. The flooding ports exclude the received port by HW.<br><br>2. Frame dropped though QRY_FFP=7'b0.                                            |

15020014 VTC VLAN TAG control 000000FF

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23        | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|-----------|----|----|----|------|----|----|----|
| Name  |      |    |    |    |    |    |    |    |           |    |    |    | REVO |    |    |    |
| Type  |      |    |    |    |    |    |    |    |           |    |    |    | RW   |    |    |    |
| Reset |      |    |    |    |    |    |    |    |           |    |    |    | 0    | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7         | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| Name  | REVO |    |    |    |    |    |    |    | GUEST_MEM |    |    |    |      |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    | RW        |    |    |    |      |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1         | 1  | 1  | 1  | 1    | 1  | 1  | 1  |

| Bit(s) | Name      | Description                                                                                                     |
|--------|-----------|-----------------------------------------------------------------------------------------------------------------|
| 19:8   | REVO      | Reserved                                                                                                        |
| 7:0    | GUEST_MEM | <b>Guest VLAN Member</b><br><br>The assigned VLAN member for the frames which cannot pass 802.1x authentication |

**15020018**      **ISC**      **IGMP snooping control**      **7F027DFF**

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23     | 22 | 21 | 20           | 19        | 18         | 17         | 16 |
|-------|----------|----|----|----|----|----|----|----|--------|----|----|--------------|-----------|------------|------------|----|
| Name  | LRN_RP   |    |    |    |    |    |    |    | REVO   |    |    | DWN_GRADE_EN | MLD_RP_EN | IGMP_RP_EN | ROBUST_VAR |    |
| Type  | RO       |    |    |    |    |    |    |    | RW     |    |    | RW           | RW        | RW         | RW         |    |
| Reset | 0        | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0      | 0  | 0  | 0            | 0         | 0          | 1          | 0  |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7      | 6  | 5  | 4            | 3         | 2          | 1          | 0  |
| Name  | QRY_INTL |    |    |    |    |    |    |    | DEF_RP |    |    |              |           |            |            |    |
| Type  | RW       |    |    |    |    |    |    |    | RW     |    |    |              |           |            |            |    |
| Reset | 0        | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1      | 1  | 1  | 1            | 1         | 1          | 1          | 1  |

| Bit(s) | Name         | Description                                                                                                                                                                                                        |
|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | LRN_RP       | <b>Learned Router Ports</b><br><br>Show the router ports for IGMP/MDL messages including the default and learned ports.                                                                                            |
| 23:21  | REVO         | <b>Reserved</b>                                                                                                                                                                                                    |
| 20     | DWN_GRADE_EN | <b>IGMP v2 to v1 Auto-Downgrade Enable</b><br><br>Enable an automatic downgrade from IGMPv2 to v1 due to a IGMPv1 report message.<br><br>0: Disable<br><br>1: Enable                                               |
| 19     | MLD_RP_EN    | <b>MLD Router Port Learning Enable</b><br><br>Enable automatic router port learning automatically based on MLD queries.<br><br>0: Disable<br><br>1: Enable                                                         |
| 18     | IGMP_RP_EN   | <b>IGMP Router Port Learning</b><br><br>Enable automatic router port learning based on IGMP queries.<br><br>0: Disable<br><br>1: Enable                                                                            |
| 17:16  | ROBUST_VAR   | <b>Robustness Variable</b><br><br>Define the maximum allowable number of IGMP Query messages that may be lost consecutively.<br><br>0: Reserved<br><br>1: One time<br><br>2: Twice (default)<br><br>3: Three times |
| 15:8   | QRY_INTL     | <b>Query Interval</b>                                                                                                                                                                                              |

| Bit(s) | Name   | Description                                                                                                                                                                                                     |
|--------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |        | Together with the Robustness Variable, the Query Interval sets the age-out time for router ports automatically learned from IGMP Query frames.<br><br>Age-out time = (QRY_INTL * ROBUST_VAR)<br><br>(Unit: sec) |
| 7:0    | DEF_RP | <b>Default Router Port</b><br><br>Set the default router port which will not be aged out when IGMP/MLD router port learning is enabled.                                                                         |

**1502001C IMC IGMP/MLD message control 08100810**

| Bit   | 31           | 30          | 29 | 28 | 27           | 26          | 25           | 24          | 23 | 22 | 21           | 20            | 19             | 18            | 17 | 16 |
|-------|--------------|-------------|----|----|--------------|-------------|--------------|-------------|----|----|--------------|---------------|----------------|---------------|----|----|
| Name  | MDL_RPT_MIR  | MLD_RPT_FW  |    |    | MLD_MANG_FR  | MLD_PAE_FR  | MLD_BPDU_FR  | MLD_EG_TAG  |    |    | MLD_LK_VLAN  | MLD_PRI_HIGH  | MLD_QUEUE_MIR  | MLD_QUEUE_FW  |    |    |
| Type  | RW           | RW          |    |    | RW           | RW          | RW           | RW          |    |    | RW           | RW            | RW             | RW            |    |    |
| Reset | 0            | 0           | 0  | 0  | 1            | 0           | 0            | 0           | 0  | 0  | 0            | 1             | 0              | 0             | 0  | 0  |
| Bit   | 15           | 14          | 13 | 12 | 11           | 10          | 9            | 8           | 7  | 6  | 5            | 4             | 3              | 2             | 1  | 0  |
| Name  | IGMP_RPT_MIR | IGMP_RPT_FW |    |    | IGMP_MANG_FR | IGMP_PAE_FR | IGMP_BPDU_FR | IGMP_EG_TAG |    |    | IGMP_LK_VLAN | IGMP_PRI_HIGH | IGMP_QUEUE_MIR | IGMP_QUEUE_FW |    |    |
| Type  | RW           | RW          |    |    | RW           | RW          | RW           | RW          |    |    | RW           | RW            | RW             | RW            |    |    |
| Reset | 0            | 0           | 0  | 0  | 1            | 0           | 0            | 0           | 0  | 0  | 0            | 1             | 0              | 0             | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                                                                                                                                           |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MDL_RPT_MIR | <b>MLD Report/Done Message to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                 |
| 30:28  | MLD_RPT_FW  | <b>MLD Report/Done Message TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame dropped |
| 27     | MLD_MANG_FR | <b>MLD Message as Management Frame</b><br><br>0: Disable<br><br>1: Regarded as management frame                                                                                                                                                                                                                                                                                                       |
| 26     | MLD_PAE_FR  | <b>MLD Message as PAE Frame</b><br><br>0: Disable<br><br>1: Regarded as PAE frame                                                                                                                                                                                                                                                                                                                     |
| 25     | MLD_BPDU_FR | <b>MLD Message as BPDU Frame</b><br><br>0: Non-BPDU Frame<br><br>1: Regarded as BPDU frame                                                                                                                                                                                                                                                                                                            |
| 24:22  | MLD_EG_TAG  | <b>MLD Message Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disable)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved                                                                                                                                                                                                                                                      |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                            |
|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 3'b100: Untagged                                                                                                                                                                                                                                                                                                                                                                                       |
|        |              | 3'b101: Swap                                                                                                                                                                                                                                                                                                                                                                                           |
|        |              | 3'b110: Tagged                                                                                                                                                                                                                                                                                                                                                                                         |
|        |              | 3'b111: Stack                                                                                                                                                                                                                                                                                                                                                                                          |
| 21     | MLD_LKY_VLAN | <b>MLD Leaky VLAN Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                                                                                                                                        |
| 20     | MLD_PRI_HIGH | <b>MLD Force the Highest Priority</b><br><br>0: System default<br><br>1: Assigned to the highest priority queue.                                                                                                                                                                                                                                                                                       |
| 19     | MLD_QUE_MIR  | <b>MLD Query Message to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                        |
| 18:16  | MLD_QUE_FW   | <b>MLD Query Message TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame Dropped        |
| 15     | IGMP_RPT_MIR | <b>IGMP Report/Done Message to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                 |
| 14:12  | IGMP_RPT_FW  | <b>IGMP Report/Done Message TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame dropped |
| 11     | IGMP_MANG_FR | <b>IGMP Message as Management Frame</b><br><br>0: Disable                                                                                                                                                                                                                                                                                                                                              |

| Bit(s) | Name          | Description                                                                                                                                                                                                                                                                                                                                                                                             |
|--------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10     | IGMP_PAE_FR   | <p>1: Regarded as management frame</p> <p><b>IGMP Message as PAE Frame</b></p> <p>0: Disable</p>                                                                                                                                                                                                                                                                                                        |
| 9      | IGMP_BPDU_FR  | <p>1: Regarded as PAE frame</p> <p><b>IGMP Message as BPDU Frame</b></p> <p>0: Non-BPDU Frame</p>                                                                                                                                                                                                                                                                                                       |
| 8:6    | IGMP_EG_TAG   | <p>1: Regarded as BPDU frame</p> <p><b>IGMP Message Egress VLAN Tag Attribution</b></p> <p>3'b000: System default (disable)</p> <p>3'b001: Consistent</p> <p>3'b010, 3'b011: Reserved</p> <p>3'b100: Untagged</p> <p>3'b101: Swap</p> <p>3'b110: Tagged</p> <p>3'b111: Stack</p>                                                                                                                        |
| 5      | IGMP_LKY_VLAN | <p><b>IGMP Leaky VLAN Enable</b></p> <p>0: Disable</p> <p>1: Enable</p>                                                                                                                                                                                                                                                                                                                                 |
| 4      | IGMP_PRI_HIGH | <p><b>IGMP Force the Highest Priority</b></p> <p>0: System default</p> <p>1: Assigned to the highest priority queue.</p>                                                                                                                                                                                                                                                                                |
| 3      | IGMP_QUE_MIR  | <p><b>IGMP Query Message to Mirror Port</b></p> <p>0: Disable</p> <p>1: Frame copied to Mirror port</p>                                                                                                                                                                                                                                                                                                 |
| 2:0    | IGMP_QUE_FW   | <p><b>IGMP Query Message TO_CPU Forwarding</b></p> <p>3'b0xx: System default (disable)</p> <p>3'b100: System default and CPU port excluded</p> <p>3'b101: System default and CPU port included</p> <p>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)</p> <p>3'b111: Frame Dropped</p> |



15020020 APC ARP and PPPoE control 08100810

| Bit   | 31   | 30 | 29 | 28 | 27          | 26         | 25          | 24         | 23 | 22 | 21           | 20           | 19      | 18          | 17 | 16 |
|-------|------|----|----|----|-------------|------------|-------------|------------|----|----|--------------|--------------|---------|-------------|----|----|
| Name  | REV0 |    |    |    | PPP_MANG_FR | PPP_PAE_FR | PPP_BPDU_FR | PPP_EG_TAG |    |    | PPP_LKY_VLAN | PPP_PRI_HIGH | PPP_MIR | PPP_PORT_FW |    |    |
| Type  | RO   |    |    |    | RW          | RW         | RW          | RW         |    |    | RW           | RW           | RW      | RW          |    |    |
| Reset | 0    | 0  | 0  | 0  | 1           | 0          | 0           | 0          | 0  | 0  | 0            | 1            | 0       | 0           | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11          | 10         | 9           | 8          | 7  | 6  | 5            | 4            | 3       | 2           | 1  | 0  |
| Name  | REV1 |    |    |    | ARP_MANG_FR | ARP_PAE_FR | ARP_BPDU_FR | ARP_EG_TAG |    |    | ARP_LKY_VLAN | ARP_PRI_HIGH | ARP_MIR | ARP_PORT_FW |    |    |
| Type  | RW   |    |    |    | RW          | RW         | RW          | RW         |    |    | RW           | RW           | RW      | RW          |    |    |
| Reset | 0    | 0  | 0  | 0  | 1           | 0          | 0           | 0          | 0  | 0  | 0            | 1            | 0       | 0           | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                     |
|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | REV0         | <b>Reserved</b>                                                                                                                                                                                                 |
| 27     | PPP_MANG_FR  | <b>PPPoE Discovery as Management Frame</b><br>0: Disable<br>1: Regarded as management frame                                                                                                                     |
| 26     | PPP_PAE_FR   | <b>PPPoE Discovery as PAE Frame</b><br>0: Disable<br>1: Regarded as PAE frame                                                                                                                                   |
| 25     | PPP_BPDU_FR  | <b>PPPoE Discovery as BPDU Frame</b><br>0: Non-BPDU Frame<br>1: Regarded as BPDU frame                                                                                                                          |
| 24:22  | PPP_EG_TAG   | <b>PPPoE Discovery Egress VLAN Tag Attribution</b><br>3'b000: System default (disable)<br>3'b001: Consistent<br>3'b010, 3'b011: Reserved<br>3'b100: Untagged<br>3'b101: Swap<br>3'b110: Tagged<br>3'b111: Stack |
| 21     | PPP_LKY_VLAN | <b>PPPoE Discovery Leaky VLAN Enable</b><br>0: Disable<br>1: Enable                                                                                                                                             |
| 20     | PPP_PRI_HIGH | <b>PPPoE Discovery Force the Highest Priority</b>                                                                                                                                                               |

| Bit(s) | Name         | Description                                                                                                                                                      |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 0: System default                                                                                                                                                |
|        |              | 1: Assigned to the highest priority queue.                                                                                                                       |
| 19     | PPP_MIR      | <b>PPPoE Discovery to Mirror Port</b>                                                                                                                            |
|        |              | 0: Disable                                                                                                                                                       |
|        |              | 1: Frame copied to Mirror port                                                                                                                                   |
| 18:16  | PPP_PORT_FW  | <b>PPPoE Discovery TO_CPU Forwarding</b>                                                                                                                         |
|        |              | 3'b0xx: System default (disable)                                                                                                                                 |
|        |              | 3'b100: System default and CPU port excluded                                                                                                                     |
|        |              | 3'b101: System default and CPU port included                                                                                                                     |
|        |              | 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) |
|        |              | 3'b111: Frame Dropped                                                                                                                                            |
| 15:12  | REV1         | <b>Reserved</b>                                                                                                                                                  |
| 11     | ARP_MANG_FR  | <b>ARP/RARP Discovery as Management Frame</b>                                                                                                                    |
|        |              | 0: Disable                                                                                                                                                       |
|        |              | 1: Regarded as management frame                                                                                                                                  |
| 10     | ARP_PAE_FR   | <b>ARP/RARP Discovery as PAE Frame</b>                                                                                                                           |
|        |              | 0: Disable                                                                                                                                                       |
|        |              | 1: Regarded as PAE frame                                                                                                                                         |
| 9      | ARP_BPDU_FR  | <b>ARP/RARP Discovery as BPDU Frame</b>                                                                                                                          |
|        |              | 0: Non-BPDU Frame                                                                                                                                                |
|        |              | 1: Regarded as BPDU frame                                                                                                                                        |
| 8:6    | ARP_EG_TAG   | <b>ARP/RARP Discovery Egress VLAN Tag Attribution</b>                                                                                                            |
|        |              | 3'b000: System default (disable)                                                                                                                                 |
|        |              | 3'b001: Consistent                                                                                                                                               |
|        |              | 3'b010, 3'b011: Reserved                                                                                                                                         |
|        |              | 3'b100: Untagged                                                                                                                                                 |
|        |              | 3'b101: Swap                                                                                                                                                     |
|        |              | 3'b110: Tagged                                                                                                                                                   |
|        |              | 3'b111: Stack                                                                                                                                                    |
| 5      | ARP_LKY_VLAN | <b>ARP/RARP Discovery Leaky VLAN Enable</b>                                                                                                                      |
|        |              | 0: Disable                                                                                                                                                       |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                      |
|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 1: Enable                                                                                                                                                                                                                                                                                                                                                                                        |
| 4      | ARP_PRI_HIGH | <b>ARP/RARP Discovery Force the Highest Priority</b><br><br>0: System default<br><br>1: Assigned to the highest priority queue.                                                                                                                                                                                                                                                                  |
| 3      | ARP_MIR      | <b>ARP/RARP Discovery to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                 |
| 2:0    | ARP_PORT_FW  | <b>ARP/RARP Discovery TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame Dropped |

**15020024      BPC      BPDU and PAE control      0C100A10**

| Bit   | 31   | 30 | 29 | 28 | 27           | 26          | 25           | 24          | 23 | 22 | 21            | 20            | 19       | 18           | 17 | 16 |
|-------|------|----|----|----|--------------|-------------|--------------|-------------|----|----|---------------|---------------|----------|--------------|----|----|
| Name  | REV0 |    |    |    | PAE_MANG_FR  | PAE_PAE_FR  | PAE_BPDU_FR  | PAE_EG_TAG  |    |    | PAE_LKY_VLAN  | PAE_PRI_HIGH  | PAE_MIR  | PAE_PORT_FW  |    |    |
| Type  | RO   |    |    |    | RW           | RW          | RW           | RW          |    |    | RW            | RW            | RW       | RW           |    |    |
| Reset | 0    | 0  | 0  | 0  | 1            | 1           | 0            | 0           | 0  | 0  | 0             | 1             | 0        | 0            | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11           | 10          | 9            | 8           | 7  | 6  | 5             | 4             | 3        | 2            | 1  | 0  |
| Name  | REV1 |    |    |    | BPDU_MANG_FR | BPDU_PAE_FR | BPDU_BPDU_FR | BPDU_EG_TAG |    |    | BPDU_LKY_VLAN | BPDU_PRI_HIGH | BPDU_MIR | BPDU_PORT_FW |    |    |
| Type  | RW   |    |    |    | RW           | RW          | RW           | RW          |    |    | RW            | RW            | RW       | RW           |    |    |
| Reset | 0    | 0  | 0  | 0  | 1            | 0           | 1            | 0           | 0  | 0  | 0             | 1             | 0        | 0            | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                     |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | REV0         | <b>Reserved</b>                                                                                                                                                                                                                 |
| 27     | PAE_MANG_FR  | <b>PAE as Management Frame</b><br><br>0: Disable<br><br>1: Regarded as management frame                                                                                                                                         |
| 26     | PAE_PAE_FR   | <b>PAE as PAE Frame</b><br><br>0: Disable<br><br>1: Regarded as PAE frame                                                                                                                                                       |
| 25     | PAE_BPDU_FR  | <b>PAE as BPDU Frame</b><br><br>0: Non-BPDU Frame<br><br>1: Regarded as BPDU frame                                                                                                                                              |
| 24:22  | PAE_EG_TAG   | <b>PAE Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disable)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged<br><br>3'b101: Swap<br><br>3'b110: Tagged<br><br>3'b111: Stack |
| 21     | PAE_LKY_VLAN | <b>PAE Leaky VLAN Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                 |
| 20     | PAE_PRI_HIGH | <b>PAE Force the Highest Priority</b><br><br>0: System default                                                                                                                                                                  |

| Bit(s) | Name          | Description                                                                                                                                                                                                                                                                                                                                                                       |
|--------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |               | 1: Assigned to the highest priority queue.                                                                                                                                                                                                                                                                                                                                        |
| 19     | PAE_MIR       | <b>PAE to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                 |
| 18:16  | PAE_PORT_FW   | <b>PAE TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame Dropped |
| 15:12  | REV1          | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                   |
| 11     | BPDU_MANG_FR  | <b>BPDU as Management Frame</b><br><br>0: Disable<br><br>1: Regarded as management frame                                                                                                                                                                                                                                                                                          |
| 10     | BPDU_PAE_FR   | <b>BPDU as PAE Frame</b><br><br>0: Disable<br><br>1: Regarded as PAE frame                                                                                                                                                                                                                                                                                                        |
| 9      | BPDU_BPDU_FR  | <b>BPDU as BPDU Frame</b><br><br>0: Non-BPDU Frame<br><br>1: Regarded as BPDU frame                                                                                                                                                                                                                                                                                               |
| 8:6    | BPDU_EG_TAG   | <b>BPDU Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disable)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged<br><br>3'b101: Swap<br><br>3'b110: Tagged<br><br>3'b111: Stack                                                                                                                                                  |
| 5      | BPDU_LKY_VLAN | <b>BPDU Leaky VLAN Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                                                                                                                  |

| Bit(s) | Name          | Description                                                                                                                                                                                                                                                                                                                                                                        |
|--------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4      | BPDU_PRI_HIGH | <b>BPDU Force the Highest Priority</b><br><br>0: System default<br><br>1: Assigned to the highest priority queue.                                                                                                                                                                                                                                                                  |
| 3      | BPDU_MIR      | <b>BPDU to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                 |
| 2:0    | BPDU_PORT_FW  | <b>BPDU TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame Dropped |

**15020028**      **RGAC1**      **REV\_01 and REV\_02 control**      **08100810**

| Bit   | 31   | 30 | 29 | 28 | 27          | 26         | 25          | 24         | 23 | 22 | 21           | 20           | 19      | 18          | 17 | 16 |
|-------|------|----|----|----|-------------|------------|-------------|------------|----|----|--------------|--------------|---------|-------------|----|----|
| Name  | REV0 |    |    |    | R02_MANG_FR | R02_PAE_FR | R02_BPDU_FR | R02_EG_TAG |    |    | R02_LKY_VLAN | R02_PRI_HIGH | R02_MIR | R02_PORT_FW |    |    |
| Type  | RO   |    |    |    | RW          | RW         | RW          | RW         |    |    | RW           | RW           | RW      | RW          |    |    |
| Reset | 0    | 0  | 0  | 0  | 1           | 0          | 0           | 0          | 0  | 0  | 0            | 1            | 0       | 0           | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11          | 10         | 9           | 8          | 7  | 6  | 5            | 4            | 3       | 2           | 1  | 0  |
| Name  | REV1 |    |    |    | R01_MANG_FR | R01_PAE_FR | R01_BPDU_FR | R01_EG_TAG |    |    | R01_LKY_VLAN | R01_PRI_HIGH | R01_MIR | R01_PORT_FW |    |    |
| Type  | RW   |    |    |    | RW          | RW         | RW          | RW         |    |    | RW           | RW           | RW      | RW          |    |    |
| Reset | 0    | 0  | 0  | 0  | 1           | 0          | 0           | 0          | 0  | 0  | 0            | 1            | 0       | 0           | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                        |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | REV0         | <b>Reserved</b>                                                                                                                                                                                                                    |
| 27     | R02_MANG_FR  | <b>REV_02 as Management Frame</b><br><br>0: Disable<br><br>1: Regarded as management frame                                                                                                                                         |
| 26     | R02_PAE_FR   | <b>REV_02 as PAE Frame</b><br><br>0: Disable<br><br>1: Regarded as PAE frame                                                                                                                                                       |
| 25     | R02_BPDU_FR  | <b>REV_02 as BPDU Frame</b><br><br>0: Non-BPDU Frame<br><br>1: Regarded as BPDU frame                                                                                                                                              |
| 24:22  | R02_EG_TAG   | <b>REV_02 Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disable)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged<br><br>3'b101: Swap<br><br>3'b110: Tagged<br><br>3'b111: Stack |
| 21     | R02_LKY_VLAN | <b>REV_02 Leaky VLAN Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                 |
| 20     | R02_PRI_HIGH | <b>REV_02 Force the Highest Priority</b><br><br>0: System default                                                                                                                                                                  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                          |
|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 1: Assigned to the highest priority queue.                                                                                                                                                                                                                                                                                                                                           |
| 19     | R02_MIR      | <b>REV_02 to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                 |
| 18:16  | R02_PORT_FW  | <b>REV_02 TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame Dropped |
| 15:12  | REV1         | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                      |
| 11     | R01_MANG_FR  | <b>REV_01 as Management Frame</b><br><br>0: Disable<br><br>1: Regarded as management frame                                                                                                                                                                                                                                                                                           |
| 10     | R01_PAE_FR   | <b>REV_01 as PAE Frame</b><br><br>0: Disable<br><br>1: Regarded as PAE frame                                                                                                                                                                                                                                                                                                         |
| 9      | R01_BPDU_FR  | <b>REV_01 as BPDU Frame</b><br><br>0: Non-BPDU Frame<br><br>1: Regarded as BPDU frame                                                                                                                                                                                                                                                                                                |
| 8:6    | R01_EG_TAG   | <b>REV_01 Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disable)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged<br><br>3'b101: Swap<br><br>3'b110: Tagged<br><br>3'b111: Stack                                                                                                                                                   |
| 5      | R01_LKY_VLAN | <b>REV_01 Leaky VLAN Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                                                                                                                   |



| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                          |
|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4      | R01_PRI_HIGH | <b>REV_01 Force the Highest Priority</b><br><br>0: System default<br><br>1: Assigned to the highest priority queue.                                                                                                                                                                                                                                                                  |
| 3      | R01_MIR      | <b>REV_01 to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                 |
| 2:0    | R01_PORT_FW  | <b>REV_01 TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame Dropped |

1502002C **RGAC2** **REV\_03 and REV\_OE control** **08100810**

| Bit   | 31   | 30 | 29 | 28 | 27          | 26         | 25          | 24         | 23 | 22 | 21           | 20           | 19      | 18          | 17 | 16 |
|-------|------|----|----|----|-------------|------------|-------------|------------|----|----|--------------|--------------|---------|-------------|----|----|
| Name  | REV0 |    |    |    | R0E_MANG_FR | R0E_PAE_FR | R0E_BPDU_FR | R0E_EG_TAG |    |    | R0E_LKY_VLAN | R0E_PRI_HIGH | R0E_MIR | R0E_PORT_FW |    |    |
| Type  | RO   |    |    |    | RW          | RW         | RW          | RW         |    |    | RW           | RW           | RW      | RW          |    |    |
| Reset | 0    | 0  | 0  | 0  | 1           | 0          | 0           | 0          | 0  | 0  | 0            | 1            | 0       | 0           | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11          | 10         | 9           | 8          | 7  | 6  | 5            | 4            | 3       | 2           | 1  | 0  |
| Name  | REV1 |    |    |    | R03_MANG_FR | R03_PAE_FR | R03_BPDU_FR | R03_EG_TAG |    |    | R03_LKY_VLAN | R03_PRI_HIGH | R03_MIR | R03_PORT_FW |    |    |
| Type  | RW   |    |    |    | RW          | RW         | RW          | RW         |    |    | RW           | RW           | RW      | RW          |    |    |
| Reset | 0    | 0  | 0  | 0  | 1           | 0          | 0           | 0          | 0  | 0  | 0            | 1            | 0       | 0           | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                        |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | REV0         | <b>Reserved</b>                                                                                                                                                                                                                    |
| 27     | R0E_MANG_FR  | <b>REV_OE as Management Frame</b><br><br>0: Disable<br><br>1: Regarded as management frame                                                                                                                                         |
| 26     | R0E_PAE_FR   | <b>REV_OE as PAE Frame</b><br><br>0: Disable<br><br>1: Regarded as PAE frame                                                                                                                                                       |
| 25     | R0E_BPDU_FR  | <b>REV_OE as BPDU Frame</b><br><br>0: Non-BPDU Frame<br><br>1: Regarded as BPDU frame                                                                                                                                              |
| 24:22  | R0E_EG_TAG   | <b>REV_OE Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disable)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged<br><br>3'b101: Swap<br><br>3'b110: Tagged<br><br>3'b111: Stack |
| 21     | R0E_LKY_VLAN | <b>REV_OE Leaky VLAN Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                 |
| 20     | R0E_PRI_HIGH | <b>REV_OE Force the Highest Priority</b><br><br>0: System default                                                                                                                                                                  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                          |
|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 1: Assigned to the highest priority queue.                                                                                                                                                                                                                                                                                                                                           |
| 19     | ROE_MIR      | <b>REV_OE to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                 |
| 18:16  | ROE_PORT_FW  | <b>REV_OE TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame Dropped |
| 15:12  | REV1         | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                      |
| 11     | R03_MANG_FR  | <b>REV_03 as Management Frame</b><br><br>0: Disable<br><br>1: Regarded as management frame                                                                                                                                                                                                                                                                                           |
| 10     | R03_PAE_FR   | <b>REV_03 as PAE Frame</b><br><br>0: Disable<br><br>1: Regarded as PAE frame                                                                                                                                                                                                                                                                                                         |
| 9      | R03_BPDU_FR  | <b>REV_03 as BPDU Frame</b><br><br>0: Non-BPDU Frame<br><br>1: Regarded as BPDU frame                                                                                                                                                                                                                                                                                                |
| 8:6    | R03_EG_TAG   | <b>REV_03 Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disable)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged<br><br>3'b101: Swap<br><br>3'b110: Tagged<br><br>3'b111: Stack                                                                                                                                                   |
| 5      | R03_LKY_VLAN | <b>REV_03 Leaky VLAN Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                                                                                                                   |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                          |
|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4      | R03_PRI_HIGH | <b>REV_03 Force the Highest Priority</b><br><br>0: System default<br><br>1: Assigned to the highest priority queue.                                                                                                                                                                                                                                                                  |
| 3      | R03_MIR      | <b>REV_03 to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                 |
| 2:0    | R03_PORT_FW  | <b>REV_03 TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame Dropped |

**15020030**      **RGAC3**      **REV\_10 and REV\_20 control**      **08100810**

| Bit   | 31   | 30 | 29 | 28 | 27          | 26         | 25          | 24         | 23 | 22 | 21 | 20           | 19           | 18      | 17          | 16 |
|-------|------|----|----|----|-------------|------------|-------------|------------|----|----|----|--------------|--------------|---------|-------------|----|
| Name  | REV0 |    |    |    | R20_MANG_FR | R20_PAE_FR | R20_BPDU_FR | R20_EG_TAG |    |    |    | R20_LKY_VLAN | R20_PRI_HIGH | R20_MIR | R20_PORT_FW |    |
| Type  | RO   |    |    |    | RW          | RW         | RW          | RW         |    |    |    | RW           | RW           | RW      | RW          |    |
| Reset | 0    | 0  | 0  | 0  | 1           | 0          | 0           | 0          | 0  | 0  | 0  | 1            | 0            | 0       | 0           | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11          | 10         | 9           | 8          | 7  | 6  | 5  | 4            | 3            | 2       | 1           | 0  |
| Name  | REV1 |    |    |    | R10_MANG_FR | R10_PAE_FR | R10_BPDU_FR | R10_EG_TAG |    |    |    | R10_LKY_VLAN | R10_PRI_HIGH | R10_MIR | R10_PORT_FW |    |
| Type  | RW   |    |    |    | RW          | RW         | RW          | RW         |    |    |    | RW           | RW           | RW      | RW          |    |
| Reset | 0    | 0  | 0  | 0  | 1           | 0          | 0           | 0          | 0  | 0  | 0  | 1            | 0            | 0       | 0           | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                        |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | REV0         | <b>Reserved</b>                                                                                                                                                                                                                    |
| 27     | R20_MANG_FR  | <b>REV_20 as Management Frame</b><br><br>0: Disable<br><br>1: Regarded as management frame                                                                                                                                         |
| 26     | R20_PAE_FR   | <b>REV_20 as PAE Frame</b><br><br>0: Disable<br><br>1: Regarded as PAE frame                                                                                                                                                       |
| 25     | R20_BPDU_FR  | <b>REV_20 as BPDU Frame</b><br><br>0: Non-BPDU Frame<br><br>1: Regarded as BPDU frame                                                                                                                                              |
| 24:22  | R20_EG_TAG   | <b>REV_20 Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disable)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged<br><br>3'b101: Swap<br><br>3'b110: Tagged<br><br>3'b111: Stack |
| 21     | R20_LKY_VLAN | <b>REV_20 Leaky VLAN Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                 |
| 20     | R20_PRI_HIGH | <b>REV_20 Force the Highest Priority</b><br><br>0: System default                                                                                                                                                                  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                          |
|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 1: Assigned to the highest priority queue.                                                                                                                                                                                                                                                                                                                                           |
| 19     | R20_MIR      | <b>REV_20 to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                 |
| 18:16  | R20_PORT_FW  | <b>REV_20 TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame Dropped |
| 15:12  | REV1         | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                      |
| 11     | R10_MANG_FR  | <b>REV_10 as Management Frame</b><br><br>0: Disable<br><br>1: Regarded as management frame                                                                                                                                                                                                                                                                                           |
| 10     | R10_PAE_FR   | <b>REV_10 as PAE Frame</b><br><br>0: Disable<br><br>1: Regarded as PAE frame                                                                                                                                                                                                                                                                                                         |
| 9      | R10_BPDU_FR  | <b>REV_10 as BPDU Frame</b><br><br>0: Non-BPDU Frame<br><br>1: Regarded as BPDU frame                                                                                                                                                                                                                                                                                                |
| 8:6    | R10_EG_TAG   | <b>REV_10 Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disable)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged<br><br>3'b101: Swap<br><br>3'b110: Tagged<br><br>3'b111: Stack                                                                                                                                                   |
| 5      | R10_LKY_VLAN | <b>REV_10 Leaky VLAN Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                                                                                                                   |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                          |
|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4      | R10_PRI_HIGH | <b>REV_10 Force the Highest Priority</b><br><br>0: System default<br><br>1: Assigned to the highest priority queue.                                                                                                                                                                                                                                                                  |
| 3      | R10_MIR      | <b>REV_10 to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                 |
| 2:0    | R10_PORT_FW  | <b>REV_10 TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame Dropped |

15020034 **RGAC4** **REV\_21 and REV\_UN control** 08100810

| Bit   | 31   | 30 | 29 | 28 | 27          | 26         | 25          | 24         | 23 | 22 | 21           | 20           | 19      | 18          | 17 | 16 |
|-------|------|----|----|----|-------------|------------|-------------|------------|----|----|--------------|--------------|---------|-------------|----|----|
| Name  | REV0 |    |    |    | RUN_MANG_FR | RUN_PAE_FR | RUN_BPDU_FR | RUN_EG_TAG |    |    | RUN_LKY_VLAN | RUN_PRI_HIGH | RUN_MIR | RUN_PORT_FW |    |    |
| Type  | RO   |    |    |    | RW          | RW         | RW          | RW         |    |    | RW           | RW           | RW      | RW          |    |    |
| Reset | 0    | 0  | 0  | 0  | 1           | 0          | 0           | 0          | 0  | 0  | 0            | 1            | 0       | 0           | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11          | 10         | 9           | 8          | 7  | 6  | 5            | 4            | 3       | 2           | 1  | 0  |
| Name  | REV1 |    |    |    | R21_MANG_FR | R21_PAE_FR | R21_BPDU_FR | R21_EG_TAG |    |    | R21_LKY_VLAN | R21_PRI_HIGH | R21_MIR | R21_PORT_FW |    |    |
| Type  | RW   |    |    |    | RW          | RW         | RW          | RW         |    |    | RW           | RW           | RW      | RW          |    |    |
| Reset | 0    | 0  | 0  | 0  | 1           | 0          | 0           | 0          | 0  | 0  | 0            | 1            | 0       | 0           | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                        |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | REV0         | <b>Reserved</b>                                                                                                                                                                                                                    |
| 27     | RUN_MANG_FR  | <b>REV_20 as Management Frame</b><br><br>0: Disable<br><br>1: Regarded as management frame                                                                                                                                         |
| 26     | RUN_PAE_FR   | <b>REV_20 as PAE Frame</b><br><br>0: Disable<br><br>1: Regarded as PAE frame                                                                                                                                                       |
| 25     | RUN_BPDU_FR  | <b>REV_20 as BPDU Frame</b><br><br>0: Non-BPDU Frame<br><br>1: Regarded as BPDU frame                                                                                                                                              |
| 24:22  | RUN_EG_TAG   | <b>REV_20 Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disable)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged<br><br>3'b101: Swap<br><br>3'b110: Tagged<br><br>3'b111: Stack |
| 21     | RUN_LKY_VLAN | <b>REV_20 Leaky VLAN Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                 |
| 20     | RUN_PRI_HIGH | <b>REV_20 Force the Highest Priority</b><br><br>0: System default                                                                                                                                                                  |



| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                          |
|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 1: Assigned to the highest priority queue.                                                                                                                                                                                                                                                                                                                                           |
| 19     | RUN_MIR      | <b>REV_20 to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                 |
| 18:16  | RUN_PORT_FW  | <b>REV_20 TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame Dropped |
| 15:12  | REV1         | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                      |
| 11     | R21_MANG_FR  | <b>REV_UN as Management Frame</b><br><br>0: Disable<br><br>1: Regarded as management frame                                                                                                                                                                                                                                                                                           |
| 10     | R21_PAE_FR   | <b>REV_UN as PAE Frame</b><br><br>0: Disable<br><br>1: Regarded as PAE frame                                                                                                                                                                                                                                                                                                         |
| 9      | R21_BPDU_FR  | <b>REV_UN as BPDU Frame</b><br><br>0: Non-BPDU Frame<br><br>1: Regarded as BPDU frame                                                                                                                                                                                                                                                                                                |
| 8:6    | R21_EG_TAG   | <b>REV_UN Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disable)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged<br><br>3'b101: Swap<br><br>3'b110: Tagged<br><br>3'b111: Stack                                                                                                                                                   |
| 5      | R21_LKY_VLAN | <b>REV_UN Leaky VLAN Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                                                                                                                   |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                          |
|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4      | R21_PRI_HIGH | <b>REV_UN Force the Highest Priority</b><br><br>0: System default<br><br>1: Assigned to the highest priority queue.                                                                                                                                                                                                                                                                  |
| 3      | R21_MIR      | <b>REV_UN to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                 |
| 2:0    | R21_PORT_FW  | <b>REV_UN TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame Dropped |

15020038 **PMC** Protocol match control 00000000

| Bit          | 31   | 30 | 29       | 28        | 27          | 26 | 25 | 24 | 23   | 22 | 21       | 20        | 19          | 18 | 17 | 16 |
|--------------|------|----|----------|-----------|-------------|----|----|----|------|----|----------|-----------|-------------|----|----|----|
| <b>Name</b>  | REV0 |    | TYPE3_EN | TYPE3_VLD | TYPE3_ENCAP |    |    |    | REV1 |    | TYPE2_EN | TYPE2_VLD | TYPE2_ENCAP |    |    |    |
| <b>Type</b>  | RW   |    | RW       | RW        | RW          |    |    |    | RW   |    | RW       | RW        | RW          |    |    |    |
| <b>Reset</b> | 0    | 0  | 0        | 0         | 0           | 0  | 0  | 0  | 0    | 0  | 0        | 0         | 0           | 0  | 0  | 0  |
| <b>Bit</b>   | 15   | 14 | 13       | 12        | 11          | 10 | 9  | 8  | 7    | 6  | 5        | 4         | 3           | 2  | 1  | 0  |
| <b>Name</b>  | REV2 |    | TYPE1_EN | TYPE1_VLD | TYPE1_ENCAP |    |    |    | REV3 |    |          |           |             |    |    |    |
| <b>Type</b>  | RW   |    | RW       | RW        | RW          |    |    |    | RW   |    |          |           |             |    |    |    |
| <b>Reset</b> | 0    | 0  | 0        | 0         | 0           | 0  | 0  | 0  | 0    | 0  | 0        | 0         | 0           | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                   |
|--------|-------------|-------------------------------------------------------------------------------|
| 31:30  | REV0        | Reserved                                                                      |
| 29     | TYPE3_EN    | TYPE 3 Match Enable                                                           |
| 28     | TYPE3_VLD   | TYPE 3 Value Valid                                                            |
| 27:24  | TYPE3_ENCAP | Encapsulated Frame Type Value                                                 |
| 23:22  | REV1        | Reserved                                                                      |
| 21     | TYPE2_EN    | TYPE 2 Match Enable                                                           |
| 20     | TYPE2_VLD   | TYPE 2 Value Valid                                                            |
| 19:16  | TYPE2_ENCAP | Encapsulated Frame Type Value                                                 |
| 15:14  | REV2        | Reserved                                                                      |
| 13     | TYPE1_EN    | TYPE 1 Match Enable                                                           |
| 12     | TYPE1_VLD   | TYPE 1 Value Valid                                                            |
|        |             | 0: TYPE 1 Value in register PBG.TYPE1 is "don't care", i.e. it has no effect. |
|        |             | 1: TYPE 1 Value in register PBG.TYPE1 is valid.                               |
| 11:8   | TYPE1_ENCAP | Encapsulated Frame Type Value                                                 |
|        |             | Bit0: Ethernet II                                                             |
|        |             | Bit1: RFC_1042                                                                |
|        |             | Bit2: IPX Raw 802.3                                                           |
|        |             | Bit3: 802.2/802.3 Length Encapsulated                                         |
| 7:0    | REV3        | Reserved                                                                      |

1502003C      PBG1      Protocol based group ID-1      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TYPE1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | REVO  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description                                                                                                                                                                                                  |
|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | TYPE1 | <b>TYPE 1 Value</b><br><br>Ethernet II: Matches EtherType<br><br>RFC_1042: Matches SNAP Type<br><br>IPX Raw 802.3: "Don't care"<br><br>802.2/802.3 Length Encapsulate: Matched with DSAP[15:8] and SSAP[7:0] |
| 15:0   | REVO  | <b>Reserved</b>                                                                                                                                                                                              |

15020040      **PBG2**      Protocol based group ID-2      00000000

| Bit          | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | TYPE3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | TYPE2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description  |
|--------|-------|--------------|
| 31:16  | TYPE3 | TYPE 3 Value |
| 15:0   | TYPE2 | TYPE 2 Value |

**15020058      PIM1      DSCP priority ingress mapping I      09000000**

| Bit          | 31              | 30          | 29          | 28 | 27          | 26          | 25 | 24          | 23          | 22 | 21          | 20          | 19 | 18          | 17          | 16 |
|--------------|-----------------|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|
| <b>Name</b>  | REV0            |             | PRI_DSCP_09 |    |             | PRI_DSCP_08 |    |             | PRI_DSCP_07 |    |             | PRI_DSCP_06 |    |             | PRI_DSCP_05 |    |
| <b>Type</b>  | RO              |             | RW          |    |             | RW          |    |             | RW          |    |             | RW          |    |             | RW          |    |
| <b>Reset</b> | 0               | 0           | 0           | 0  | 1           | 0           | 0  | 1           | 0           | 0  | 0           | 0           | 0  | 0           | 0           | 0  |
| Bit          | 15              | 14          | 13          | 12 | 11          | 10          | 9  | 8           | 7           | 6  | 5           | 4           | 3  | 2           | 1           | 0  |
| <b>Name</b>  | PRI_DS<br>CP_05 | PRI_DSCP_04 |             |    | PRI_DSCP_03 |             |    | PRI_DSCP_02 |             |    | PRI_DSCP_01 |             |    | PRI_DSCP_00 |             |    |
| <b>Type</b>  | RW              | RW          |             |    | RW          |             |    | RW          |             |    | RW          |             |    | RW          |             |    |
| <b>Reset</b> | 0               | 0           | 0           | 0  | 0           | 0           | 0  | 0           | 0           | 0  | 0           | 0           | 0  | 0           | 0           | 0  |

| Bit(s) | Name        | Description                                                           |
|--------|-------------|-----------------------------------------------------------------------|
| 31:30  | REV0        | Reserved                                                              |
| 29:27  | PRI_DSCP_09 | User Priority for Differentiated Services Code Point (DSCP) 0b001_001 |
| 26:24  | PRI_DSCP_08 | User Priority for DSCP 0b001_000                                      |
| 23:21  | PRI_DSCP_07 | User Priority for DSCP 0b000_111                                      |
| 20:18  | PRI_DSCP_06 | User Priority for DSCP 0b000_110                                      |
| 17:15  | PRI_DSCP_05 | User Priority for DSCP 0b000_101                                      |
| 14:12  | PRI_DSCP_04 | User Priority for DSCP 0b000_100                                      |
| 11:9   | PRI_DSCP_03 | User Priority for DSCP 0b000_011                                      |
| 8:6    | PRI_DSCP_02 | User Priority for DSCP 0b000_010                                      |
| 5:3    | PRI_DSCP_01 | User Priority for DSCP 0b000_001                                      |
| 2:0    | PRI_DSCP_00 | User Priority for DSCP 0b000_000                                      |

**1502005C**      **PIM2**      **DSCP priority ingress mapping II**      **12489249**

| Bit          | 31          | 30          | 29          | 28 | 27          | 26          | 25 | 24          | 23          | 22 | 21          | 20          | 19 | 18          | 17          | 16 |
|--------------|-------------|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|
| <b>Name</b>  | REV0        |             | PRI_DSCP_19 |    |             | PRI_DSCP_18 |    |             | PRI_DSCP_17 |    |             | PRI_DSCP_16 |    |             | PRI_DSCP_15 |    |
| <b>Type</b>  | RO          |             | RW          |    |             | RW          |    |             | RW          |    |             | RW          |    |             | RW          |    |
| <b>Reset</b> | 0           | 0           | 0           | 1  | 0           | 0           | 1  | 0           | 0           | 1  | 0           | 0           | 1  | 0           | 0           | 0  |
| Bit          | 15          | 14          | 13          | 12 | 11          | 10          | 9  | 8           | 7           | 6  | 5           | 4           | 3  | 2           | 1           | 0  |
| <b>Name</b>  | PRI_DSCP_15 | PRI_DSCP_14 |             |    | PRI_DSCP_13 |             |    | PRI_DSCP_12 |             |    | PRI_DSCP_11 |             |    | PRI_DSCP_10 |             |    |
| <b>Type</b>  | RW          | RW          |             |    | RW          |             |    | RW          |             |    | RW          |             |    | RW          |             |    |
| <b>Reset</b> | 1           | 0           | 0           | 1  | 0           | 0           | 1  | 0           | 0           | 1  | 0           | 0           | 1  | 0           | 0           | 1  |

| Bit(s) | Name        | Description                      |
|--------|-------------|----------------------------------|
| 31:30  | REV0        | Reserved                         |
| 29:27  | PRI_DSCP_19 | User Priority for DSCP 0b010_011 |
| 26:24  | PRI_DSCP_18 | User Priority for DSCP 0b010_010 |
| 23:21  | PRI_DSCP_17 | User Priority for DSCP 0b010_001 |
| 20:18  | PRI_DSCP_16 | User Priority for DSCP 0b010_000 |
| 17:15  | PRI_DSCP_15 | User Priority for DSCP 0b001_111 |
| 14:12  | PRI_DSCP_14 | User Priority for DSCP 0b001_110 |
| 11:9   | PRI_DSCP_13 | User Priority for DSCP 0b001_101 |
| 8:6    | PRI_DSCP_12 | User Priority for DSCP 0b001_100 |
| 5:3    | PRI_DSCP_11 | User Priority for DSCP 0b001_011 |
| 2:0    | PRI_DSCP_10 | User Priority for DSCP 0b001_010 |

**15020060 PIM3 DSCP priority ingress mapping III 1B6DB492**

| Bit   | 31          | 30          | 29          | 28 | 27          | 26          | 25 | 24          | 23          | 22 | 21          | 20          | 19 | 18          | 17          | 16 |
|-------|-------------|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|
| Name  | REV0        |             | PRI_DSCP_29 |    |             | PRI_DSCP_28 |    |             | PRI_DSCP_27 |    |             | PRI_DSCP_26 |    |             | PRI_DSCP_25 |    |
| Type  | RO          |             | RW          |    |             | RW          |    |             | RW          |    |             | RW          |    |             | RW          |    |
| Reset | 0           | 0           | 0           | 1  | 1           | 0           | 1  | 1           | 0           | 1  | 1           | 0           | 1  | 1           | 0           | 1  |
| Bit   | 15          | 14          | 13          | 12 | 11          | 10          | 9  | 8           | 7           | 6  | 5           | 4           | 3  | 2           | 1           | 0  |
| Name  | PRI_DSCP_25 | PRI_DSCP_24 |             |    | PRI_DSCP_23 |             |    | PRI_DSCP_22 |             |    | PRI_DSCP_21 |             |    | PRI_DSCP_20 |             |    |
| Type  | RW          | RW          |             |    | RW          |             |    | RW          |             |    | RW          |             |    | RW          |             |    |
| Reset | 1           | 0           | 1           | 1  | 0           | 1           | 0  | 0           | 1           | 0  | 0           | 1           | 0  | 0           | 1           | 0  |

| Bit(s) | Name        | Description                      |
|--------|-------------|----------------------------------|
| 31:30  | REV0        | Reserved                         |
| 29:27  | PRI_DSCP_29 | User Priority for DSCP 0b011_101 |
| 26:24  | PRI_DSCP_28 | User Priority for DSCP 0b011_100 |
| 23:21  | PRI_DSCP_27 | User Priority for DSCP 0b011_011 |
| 20:18  | PRI_DSCP_26 | User Priority for DSCP 0b011_010 |
| 17:15  | PRI_DSCP_25 | User Priority for DSCP 0b011_001 |
| 14:12  | PRI_DSCP_24 | User Priority for DSCP 0b011_000 |
| 11:9   | PRI_DSCP_23 | User Priority for DSCP 0b010_111 |
| 8:6    | PRI_DSCP_22 | User Priority for DSCP 0b010_110 |
| 5:3    | PRI_DSCP_21 | User Priority for DSCP 0b010_101 |
| 2:0    | PRI_DSCP_20 | User Priority for DSCP 0b010_100 |



**15020064 PIM4 DSCP priority ingress mapping IV 2492491B**

| Bit   | 31          | 30          | 29          | 28 | 27          | 26          | 25 | 24          | 23          | 22 | 21          | 20          | 19 | 18          | 17          | 16 |
|-------|-------------|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|
| Name  | REV0        |             | PRI_DSCP_39 |    |             | PRI_DSCP_38 |    |             | PRI_DSCP_37 |    |             | PRI_DSCP_36 |    |             | PRI_DSCP_35 |    |
| Type  | RO          |             | RW          |    |             | RW          |    |             | RW          |    |             | RW          |    |             | RW          |    |
| Reset | 0           | 0           | 1           | 0  | 0           | 1           | 0  | 0           | 1           | 0  | 0           | 1           | 0  | 0           | 1           | 0  |
| Bit   | 15          | 14          | 13          | 12 | 11          | 10          | 9  | 8           | 7           | 6  | 5           | 4           | 3  | 2           | 1           | 0  |
| Name  | PRI_DSCP_35 | PRI_DSCP_34 |             |    | PRI_DSCP_33 |             |    | PRI_DSCP_32 |             |    | PRI_DSCP_31 |             |    | PRI_DSCP_30 |             |    |
| Type  | RW          | RW          |             |    | RW          |             |    | RW          |             |    | RW          |             |    | RW          |             |    |
| Reset | 0           | 1           | 0           | 0  | 1           | 0           | 0  | 1           | 0           | 0  | 0           | 1           | 1  | 0           | 1           | 1  |

| Bit(s) | Name        | Description                      |
|--------|-------------|----------------------------------|
| 31:30  | REV0        | Reserved                         |
| 29:27  | PRI_DSCP_39 | User Priority for DSCP 0b100_111 |
| 26:24  | PRI_DSCP_38 | User Priority for DSCP 0b100_110 |
| 23:21  | PRI_DSCP_37 | User Priority for DSCP 0b100_101 |
| 20:18  | PRI_DSCP_36 | User Priority for DSCP 0b100_100 |
| 17:15  | PRI_DSCP_35 | User Priority for DSCP 0b100_011 |
| 14:12  | PRI_DSCP_34 | User Priority for DSCP 0b100_010 |
| 11:9   | PRI_DSCP_33 | User Priority for DSCP 0b100_001 |
| 8:6    | PRI_DSCP_32 | User Priority for DSCP 0b100_000 |
| 5:3    | PRI_DSCP_31 | User Priority for DSCP 0b011_111 |
| 2:0    | PRI_DSCP_30 | User Priority for DSCP 0b011_110 |

**15020068 PIM5 DSCP priority ingress mapping V 36B6DB6D**

| Bit   | 31          | 30          | 29          | 28 | 27          | 26          | 25 | 24          | 23          | 22 | 21          | 20          | 19 | 18          | 17          | 16 |
|-------|-------------|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|
| Name  | REV0        |             | PRI_DSCP_49 |    |             | PRI_DSCP_48 |    |             | PRI_DSCP_47 |    |             | PRI_DSCP_46 |    |             | PRI_DSCP_45 |    |
| Type  | RO          |             | RW          |    |             | RW          |    |             | RW          |    |             | RW          |    |             | RW          |    |
| Reset | 0           | 0           | 1           | 1  | 0           | 1           | 1  | 0           | 1           | 0  | 1           | 1           | 0  | 1           | 1           | 0  |
| Bit   | 15          | 14          | 13          | 12 | 11          | 10          | 9  | 8           | 7           | 6  | 5           | 4           | 3  | 2           | 1           | 0  |
| Name  | PRI_DSCP_45 | PRI_DSCP_44 |             |    | PRI_DSCP_43 |             |    | PRI_DSCP_42 |             |    | PRI_DSCP_41 |             |    | PRI_DSCP_40 |             |    |
| Type  | RW          | RW          |             |    | RW          |             |    | RW          |             |    | RW          |             |    | RW          |             |    |
| Reset | 1           | 1           | 0           | 1  | 1           | 0           | 1  | 1           | 0           | 1  | 1           | 0           | 1  | 1           | 0           | 1  |

| Bit(s) | Name        | Description                      |
|--------|-------------|----------------------------------|
| 31:30  | REV0        | Reserved                         |
| 29:27  | PRI_DSCP_49 | User Priority for DSCP 0b110_001 |
| 26:24  | PRI_DSCP_48 | User Priority for DSCP 0b110_000 |
| 23:21  | PRI_DSCP_47 | User Priority for DSCP 0b101_111 |
| 20:18  | PRI_DSCP_46 | User Priority for DSCP 0b101_110 |
| 17:15  | PRI_DSCP_45 | User Priority for DSCP 0b101_101 |
| 14:12  | PRI_DSCP_44 | User Priority for DSCP 0b101_100 |
| 11:9   | PRI_DSCP_43 | User Priority for DSCP 0b101_011 |
| 8:6    | PRI_DSCP_42 | User Priority for DSCP 0b101_010 |
| 5:3    | PRI_DSCP_41 | User Priority for DSCP 0b101_001 |
| 2:0    | PRI_DSCP_40 | User Priority for DSCP 0b101_000 |

**1502006C      PIM6      DSCP priority ingress mapping VI      3FFF6DB6**

| Bit          | 31          | 30          | 29          | 28 | 27          | 26          | 25 | 24          | 23          | 22 | 21          | 20          | 19 | 18          | 17          | 16 |
|--------------|-------------|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|-------------|-------------|----|
| <b>Name</b>  | REV0        |             | PRI_DSCP_59 |    |             | PRI_DSCP_58 |    |             | PRI_DSCP_57 |    |             | PRI_DSCP_56 |    |             | PRI_DSCP_55 |    |
| <b>Type</b>  | RO          |             | RW          |    |             | RW          |    |             | RW          |    |             | RW          |    |             | RW          |    |
| <b>Reset</b> | 0           | 0           | 1           | 1  | 1           | 1           | 1  | 1           | 1           | 1  | 1           | 1           | 1  | 1           | 1           | 1  |
| Bit          | 15          | 14          | 13          | 12 | 11          | 10          | 9  | 8           | 7           | 6  | 5           | 4           | 3  | 2           | 1           | 0  |
| <b>Name</b>  | PRI_DSCP_55 | PRI_DSCP_54 |             |    | PRI_DSCP_53 |             |    | PRI_DSCP_52 |             |    | PRI_DSCP_51 |             |    | PRI_DSCP_50 |             |    |
| <b>Type</b>  | RW          | RW          |             |    | RW          |             |    | RW          |             |    | RW          |             |    | RW          |             |    |
| <b>Reset</b> | 0           | 1           | 1           | 0  | 1           | 1           | 0  | 1           | 1           | 0  | 1           | 1           | 0  | 1           | 1           | 0  |

| Bit(s) | Name        | Description                      |
|--------|-------------|----------------------------------|
| 31:30  | REV0        | Reserved                         |
| 29:27  | PRI_DSCP_59 | User Priority for DSCP 0b111_011 |
| 26:24  | PRI_DSCP_58 | User Priority for DSCP 0b111_010 |
| 23:21  | PRI_DSCP_57 | User Priority for DSCP 0b111_001 |
| 20:18  | PRI_DSCP_56 | User Priority for DSCP 0b111_000 |
| 17:15  | PRI_DSCP_55 | User Priority for DSCP 0b110_111 |
| 14:12  | PRI_DSCP_54 | User Priority for DSCP 0b110_110 |
| 11:9   | PRI_DSCP_53 | User Priority for DSCP 0b110_101 |
| 8:6    | PRI_DSCP_52 | User Priority for DSCP 0b110_100 |
| 5:3    | PRI_DSCP_51 | User Priority for DSCP 0b110_011 |
| 2:0    | PRI_DSCP_50 | User Priority for DSCP 0b110_010 |

**15020070      PIM7      DSCP priority ingress mapping VII      00000FFF**

| Bit   | 31   | 30 | 29 | 28 | 27          | 26 | 25 | 24          | 23 | 22 | 21          | 20 | 19 | 18          | 17 | 16 |
|-------|------|----|----|----|-------------|----|----|-------------|----|----|-------------|----|----|-------------|----|----|
| Name  | REVO |    |    |    |             |    |    |             |    |    |             |    |    |             |    |    |
| Type  | RO   |    |    |    |             |    |    |             |    |    |             |    |    |             |    |    |
| Reset | 0    | 0  | 0  | 0  | 0           | 0  | 0  | 0           | 0  | 0  | 0           | 0  | 0  | 0           | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11          | 10 | 9  | 8           | 7  | 6  | 5           | 4  | 3  | 2           | 1  | 0  |
| Name  | REVO |    |    |    | PRI_DSCP_63 |    |    | PRI_DSCP_62 |    |    | PRI_DSCP_61 |    |    | PRI_DSCP_60 |    |    |
| Type  | RO   |    |    |    | RW          |    |    | RW          |    |    | RW          |    |    | RW          |    |    |
| Reset | 0    | 0  | 0  | 0  | 1           | 1  | 1  | 1           | 1  | 1  | 1           | 1  | 1  | 1           | 1  | 1  |

| Bit(s) | Name        | Description                      |
|--------|-------------|----------------------------------|
| 31:12  | REVO        | Reserved                         |
| 11:9   | PRI_DSCP_63 | User Priority for DSCP 0b111_111 |
| 8:6    | PRI_DSCP_62 | User Priority for DSCP 0b111_110 |
| 5:3    | PRI_DSCP_61 | User Priority for DSCP 0b111_101 |
| 2:0    | PRI_DSCP_60 | User Priority for DSCP 0b111_100 |

15020074      ATA1      Address table access I      00000000

| Bit   | 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|
| Name  | BYTE_0 |    |    |    |    |    |    |    | BYTE_1 |    |    |    |    |    |    |    |
| Type  | RW     |    |    |    |    |    |    |    | RW     |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | BYTE_2 |    |    |    |    |    |    |    | BYTE_3 |    |    |    |    |    |    |    |
| Type  | RW     |    |    |    |    |    |    |    | RW     |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name   | Description                                                |
|--------|--------|------------------------------------------------------------|
| 31:24  | BYTE_0 | MAC Address [47:40] / Destination IP (DIP) Address [31:24] |
| 23:16  | BYTE_1 | MAC Address [39:32] / Destination IP (DIP) Address [23:16] |
| 15:8   | BYTE_2 | MAC Address [31:24] / Destination IP (DIP) Address [15:8]  |
| 7:0    | BYTE_3 | MAC Address [23:16] / Destination IP (DIP) Address [7:0]   |

**15020078      ATA2      Address table access II      00000000**

| Bit          | 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|--------|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|
| <b>Name</b>  | BYTE_0 |    |    |    |    |    |    |    | BYTE_1 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW     |    |    |    |    |    |    |    | RW     |    |    |    |    |    |    |    |
| <b>Reset</b> | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | BYTE_2 |    |    |    |    |    |    |    | BYTE_3 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW     |    |    |    |    |    |    |    | RW     |    |    |    |    |    |    |    |
| <b>Reset</b> | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name   | Description                                                                                                                                                                                                                                                                                          |
|--------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | BYTE_0 | MAC Address [15:8] / Source IP(SIP) Address [31:24]                                                                                                                                                                                                                                                  |
| 23:16  | BYTE_1 | MAC Address [7:0] / Source IP(SIP) Address [23:16]                                                                                                                                                                                                                                                   |
| 15:8   | BYTE_2 | SIP Address [15: 8] or<br>bit [15]: IVL<br>bit [14:12]: Filter ID [2:0]<br>bit [11:8]: CVID [11: 8]<br><br>NOTE: When IVL is reset, MAC [47:0] and FID [2:0] will be used to read/write the address table. When IVL is set, MAC [47:0] and CVID [11:0] will be used to read/write the address table. |
| 7:0    | BYTE_3 | SIP Address [7:0] or CVID [7:0]                                                                                                                                                                                                                                                                      |

1502007C      ATWD      Address table write data      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description      |
|--------|-------|------------------|
| 31:0   | WDATA | Table Write Data |

**15020080      ATC      Address table control      00000000**

| Bit          | 31   | 30           | 29           | 28             | 27     | 26 | 25 | 24 | 23   | 22 | 21     | 20 | 19         | 18     | 17 | 16 |
|--------------|------|--------------|--------------|----------------|--------|----|----|----|------|----|--------|----|------------|--------|----|----|
| <b>Name</b>  | REVO |              |              | COL_A<br>CC    | ADDR   |    |    |    |      |    |        |    |            |        |    |    |
| <b>Type</b>  | RO   |              |              | RO             | RO     |    |    |    |      |    |        |    |            |        |    |    |
| <b>Reset</b> | 0    | 0            | 0            | 0              | 0      | 0  | 0  | 0  | 0    | 0  | 0      | 0  | 0          | 0      | 0  | 0  |
| Bit          | 15   | 14           | 13           | 12             | 11     | 10 | 9  | 8  | 7    | 6  | 5      | 4  | 3          | 2      | 1  | 0  |
| <b>Name</b>  | BUSY | SRCH_E<br>ND | SRCH_<br>HIT | ADDR_I<br>NVLD | AC_MAT |    |    |    | REV1 |    | AC_SAT |    | AC_CA<br>E | AC_CMD |    |    |
| <b>Type</b>  | W1S  | RO           | RO           | RO             | RW     |    |    |    | RW   |    | RW     |    | RW         | RW     |    |    |
| <b>Reset</b> | 0    | 0            | 0            | 0              | 0      | 0  | 0  | 0  | 0    | 0  | 0      | 0  | 0          | 0      | 0  | 0  |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                                   |
|--------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29  | REVO       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                               |
| 28     | COL_ACC    | <b>Access Target is Collision Pool</b><br><br>Read/Write command is applied to collision pool<br><br>0: Address Table<br><br>1: Collision Pool                                                                                                                                                                                                |
| 27:16  | ADDR       | <b>Address Table Access Index</b><br><br>The actual address table access index which is calculated from a 48-bit MAC address, a 32-bit DIP, and a SIP address. (for debugging purposes)                                                                                                                                                       |
| 15     | BUSY       | <b>Address Table Is Busy</b><br><br>SW can set this bit to 1 only if this bit is reset. After ATWD registers are written and this bit is set, this chip will perform the corresponding function according to AC_CMD, AC_SAT, and AC_MAT included in this register.                                                                            |
| 14     | SRCH_END   | <b>Linear Search End</b><br><br>The linear search has reached the index end of the address table.<br><br>For Search Command Only (AC_CMD=3'b100 or 3'b101)                                                                                                                                                                                    |
| 13     | SRCH_HIT   | <b>Linear Search Hit</b><br><br>The linear search finds the target based on AC_MAT and returns the data on TSRA1,2 and ATRD. If this register is not TRUE(1) after search command is complete, that means nothing found and data on TSRA1,2 and ATRD are invalid.<br><br>For Search Command Only (AC_CMD=3'b100 or 3'b101)                    |
| 12     | ADDR_INVLD | <b>Address Entry is not Valid</b><br><br>Read Operations: The specified entry is not valid for read or removal access. Read Data returned on TSRA1, TSRA2 and ATRD are invalid.<br><br>Write Operations: The specified entry cannot be modified or added for write access.<br><br>For Single Entry Read/Write Only (AC_CMD=3'b000 or 3'b001). |
| 11:8   | AC_MAT     | <b>Address Table Multiple Access Target</b>                                                                                                                                                                                                                                                                                                   |



| Bit(s) | Name   | Description                                                                                                                                                                                                                                                                                                            |
|--------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |        | Whenever MATC register is written and bit.15 is set, this chip will perform the corresponding function on the Address table based on AC_CMD bits.                                                                                                                                                                      |
|        |        | 4'b0000: All MAC address entries                                                                                                                                                                                                                                                                                       |
|        |        | 4'b0001: All DIP/GA address entries                                                                                                                                                                                                                                                                                    |
|        |        | 4'b0010: All SIP address entries                                                                                                                                                                                                                                                                                       |
|        |        | 4'b0011: All valid address entry                                                                                                                                                                                                                                                                                       |
|        |        | 4'b0100: All non-static MAC address entries.                                                                                                                                                                                                                                                                           |
|        |        | 4'b0101: All non-static DIP address entries.                                                                                                                                                                                                                                                                           |
|        |        | 4'b0110: All static MAC address entries                                                                                                                                                                                                                                                                                |
|        |        | 4'b0111: All static DIP address entries                                                                                                                                                                                                                                                                                |
|        |        | 4'b1000: All relative SIP address entries based on the specific DIP from ATA2 register.                                                                                                                                                                                                                                |
|        |        | 4'b1001: All relative SIP address entries based on the specific SIP from ATA2 register.                                                                                                                                                                                                                                |
|        |        | 4'b1010: All MAC Address entries with the customer VID specified in ATA2.CVID [11:0]                                                                                                                                                                                                                                   |
|        |        | 4'b1010: All MAC address entries with the Filter ID specified in ATA2.FID [2:0]                                                                                                                                                                                                                                        |
|        |        | 4'b1100: All MAC Address entries with the source ports specified in ATA1.PORT [7:0]                                                                                                                                                                                                                                    |
|        |        | 4'b1101 to 4'b1111: Reserved                                                                                                                                                                                                                                                                                           |
| 7:6    | REV1   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                        |
| 5:4    | AC_SAT | <b>Address Table Single Access Target</b><br><br>Whenever MATC register is written and bit.31 is set, this chip will perform the corresponding function on the Address table based on FUNC bits.                                                                                                                       |
|        |        | 2'b00: Specified MAC address entry                                                                                                                                                                                                                                                                                     |
|        |        | 2'b01: Specified DIP address entry                                                                                                                                                                                                                                                                                     |
|        |        | 2'b10: Specified SIP address entry                                                                                                                                                                                                                                                                                     |
|        |        | 2'b11: Specified address entry (read only)                                                                                                                                                                                                                                                                             |
| 3      | AC_CAE | <b>Collision Pool Access Enable</b><br><br>For Read and Write command (single entry), read/write collision pool while address table hash collision.<br><br>For Clean and Search command, access target is collision pool (not to access address table)<br><br>If Collision Pool is disabled, this register is invalid. |

| Bit(s) | Name   | Description                                       |
|--------|--------|---------------------------------------------------|
|        |        | 0: Disable                                        |
|        |        | 1: Enable                                         |
| 2:0    | AC_CMD | <b>Address Table Access Command</b>               |
|        |        | 3'b000: Read command (single entry)               |
|        |        | 3'b001: Write command (single entry)              |
|        |        | NOTE: Supports modify, add, and remove            |
|        |        | 3'b010: Clean command (multiple entries)          |
|        |        | 3'b011: Reserved                                  |
|        |        | 3'b100: Start Search command (reset to 1st entry) |
|        |        | 3'b101: Next Search command (next entry)          |
|        |        | 3'b110 to 3'b111: Reserved                        |

**15020084      TSRA1      Table Search read Address I      00000000**

| Bit          | 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|--------|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|
| <b>Name</b>  | BYTE_0 |    |    |    |    |    |    |    | BYTE_1 |    |    |    |    |    |    |    |
| <b>Type</b>  | RO     |    |    |    |    |    |    |    | RO     |    |    |    |    |    |    |    |
| <b>Reset</b> | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | BYTE_2 |    |    |    |    |    |    |    | BYTE_3 |    |    |    |    |    |    |    |
| <b>Type</b>  | RO     |    |    |    |    |    |    |    | RO     |    |    |    |    |    |    |    |
| <b>Reset</b> | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name   | Description                                                                                                                                                                                                                                                                     |
|--------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | BYTE_0 | <b>MAC Address [47:40] / Destination IP (DIP) Address [31:24]</b> <p>The data on this register is invalid if the following is true:</p> <p>Read/Write Operation: ADDR_INVLD=1 after the operation finished</p> <p>Search Operation: SRCH_HIT=0 after the operation finished</p> |
| 23:16  | BYTE_1 | <b>MAC Address [39:32] / Destination IP (DIP) Address [23:16]</b> <p>The data on this register is invalid if the following is true:</p> <p>Read/Write Operation: ADDR_INVLD=1 after the operation finished</p> <p>Search Operation: SRCH_HIT=0 after the operation finished</p> |
| 15:8   | BYTE_2 | <b>MAC Address [31:24] / Destination IP (DIP) Address [15:8]</b> <p>The data on this register is invalid if the following is true:</p> <p>Read/Write Operation: ADDR_INVLD=1 after the operation finished</p> <p>Search Operation: SRCH_HIT=0 after the operation finished</p>  |
| 7:0    | BYTE_3 | <b>MAC Address [23:16] / Destination IP (DIP) Address [7:0]</b> <p>The data on this register is invalid if the following is true:</p> <p>Read/Write Operation: ADDR_INVLD=1 after the operation finished</p> <p>Search Operation: SRCH_HIT=0 after the operation finished</p>   |

**15020088**      **TSRA2**      **Table Search read Address II**      **00000000**

| Bit          | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|---------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| <b>Name</b>  | <b>BYTE_0</b> |    |    |    |    |    |    |    | <b>BYTE_1</b> |    |    |    |    |    |    |    |
| <b>Type</b>  | RO            |    |    |    |    |    |    |    | RO            |    |    |    |    |    |    |    |
| <b>Reset</b> | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | <b>BYTE_2</b> |    |    |    |    |    |    |    | <b>BYTE_3</b> |    |    |    |    |    |    |    |
| <b>Type</b>  | RO            |    |    |    |    |    |    |    | RO            |    |    |    |    |    |    |    |
| <b>Reset</b> | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|--------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | BYTE_0 | <b>MAC Address [15:8] / Source IP(SIP) Address [31:24]</b> <p>The data on this register is invalid if the following is true:</p> <p>Read/Write Operation: ADDR_INVLD=1 after the operation finished</p> <p>Search Operation: SRCH_HIT=0 after the operation finished</p>                                                                                                                                                                                                                                                              |
| 23:16  | BYTE_1 | <b>MAC Address [7:0] / Source IP(SIP) Address [23:16]</b> <p>The data on this register is invalid if the following is true:</p> <p>Read/Write Operation: ADDR_INVLD=1 after the operation finished</p> <p>Search Operation: SRCH_HIT=0 after the operation finished</p>                                                                                                                                                                                                                                                               |
| 15:8   | BYTE_2 | <b>SIP Address [15: 8] or</b> <p>bit [15]: IVL</p> <p>bit [14:12]: Filter ID [2:0]</p> <p>bit [11:8]: CVID [11: 8]</p> <p>NOTE: When IVL is reset, MAC [47:0] and FID [2:0] will be used to read/write the address table. When IVL is set, MAC [47:0] and CVID [11:0] will be used to read/write the address table.</p> <p>The data on this register is invalid if the following is true:</p> <p>Read/Write Operation: ADDR_INVLD=1 after the operation finished</p> <p>Search Operation: SRCH_HIT=0 after the operation finished</p> |
| 7:0    | BYTE_3 | <b>SIP Address [7:0] or CVID [7:0]</b> <p>The data on this register is invalid if the following is true:</p> <p>Read/Write Operation: ADDR_INVLD=1 after the operation finished</p> <p>Search Operation: SRCH_HIT=0 after the operation finished</p>                                                                                                                                                                                                                                                                                  |

1502008C      ATRD      Address table read data      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description     |
|--------|-------|-----------------|
| 31:0   | RDATA | Table Read Data |

The data on this register is invalid if the following is true:

Read/Write Operation: ADDR\_INVLD=1 after the operation finished

Search Operation: SRCH\_HIT=0 after the operation finished

**15020090**      **VTCR**      **VLAN table control**      **00000000**

| Bit   | 31   | 30   | 29 | 28 | 27  | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
|-------|------|------|----|----|-----|----|----|----|----|----|----|----|----|----|----|------------|
| Name  | BUSY | REVO |    |    |     |    |    |    |    |    |    |    |    |    |    | IDX_IN VLD |
| Type  | W1S  | RO   |    |    |     |    |    |    |    |    |    |    |    |    |    | RO         |
| Reset | 0    | 0    | 0  | 0  | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          |
| Bit   | 15   | 14   | 13 | 12 | 11  | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| Name  | FUNC |      |    |    | VID |    |    |    |    |    |    |    |    |    |    |            |
| Type  | RW   |      |    |    | RW  |    |    |    |    |    |    |    |    |    |    |            |
| Reset | 0    | 0    | 0  | 0  | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          |

| Bit(s) | Name      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | BUSY      | <b>VLAN Table Is Busy</b><br><br>SW can set this bit to 1 only if this bit is reset. After the VTCR register is written and this bit is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 30:17  | REVO      | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 16     | IDX_INVLD | <b>Entry is not Valid</b><br><br>This index for the access control is out of the valid index.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 15:12  | FUNC      | <b>Access Control Function</b><br><br>Whenever VTCR register is written and bit.31 is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits.<br><br>4'b0000: Read the specified VID Entry from VAWD# register based on VID bits<br><br>4'b0001: Write the specified VID Entry though VAWD# register based on VID bits.<br><br>4'b0010: Make the specified VID entry invalid based on VID bits.<br><br>4'b0011: Make the specified VID entry valid based on VID bits.<br><br>4'b0100: Read the specified ACL Table entry.<br><br>4'b0101: Write the specified ACL Table entry.<br><br>4'b0110: Read the specified trTCM Meter Table.<br><br>4'b0111: Write the specified trTCM Meter Table.<br><br>4'b1000: Read the specified ACL Mask entry.<br><br>4'b1001: Write the specified ACL Mask entry.<br><br>4'b1010: Read the specified ACL Rule Control entry.<br><br>4'b1011: Write the specified ACL Rule Control entry.<br><br>4'b1100: Read the specified ACL Rate Control entry.<br><br>4'b1101: Write the specified ACL Rate Control entry.<br><br>4'b1110: Reserved |

| Bit(s) | Name | Description                                                                                                                                 |
|--------|------|---------------------------------------------------------------------------------------------------------------------------------------------|
|        |      | 4'b1111: Reserved                                                                                                                           |
| 11:0   | VID  | <b>1. VLAN ID Number: 0x0 to 0x1F (16)</b><br><b>2. ACL table index: 0x0 to 0xFF (256)</b><br><b>3. ACL mask control: 0x0 to 0x7F (128)</b> |

15020094      VAWD1      VLAN and ACL write data I      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description             |
|--------|-------|-------------------------|
| 31:0   | WDATA | VLAN Table Write Data I |



15020098      VAWD2      VLAN and ACL write data II      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description              |
|--------|-------|--------------------------|
| 31:0   | WDATA | VLAN Table Write Data II |

1502009C      TRTCM      Two rate three color mark      00000000

| Bit   | 31       | 30   | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TRTCM_EN | REVO |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0        | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15       | 14   | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | REVO     |      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0        | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name     | Description                                                                                                                                                                                                                                                                             |
|--------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | TRTCM_EN | <b>Two Rate Three Color Marker (trTCM) Enable</b><br><br>When this bit is enabled, the meter table will be updated based on Peak Information Rate (PIR) and Committed Information Rate (CIR). The color marker will also be enabled when ACL is hit.<br><br>0: Disable<br><br>1: Enable |
| 30:0   | REVO     | <b>Reserved</b>                                                                                                                                                                                                                                                                         |

150200A0 AAC Address age control 00095001

| Bit   | 31      | 30 | 29 | 28 | 27       | 26 | 25 | 24 | 23 | 22 | 21 | 20      | 19      | 18 | 17 | 16 |
|-------|---------|----|----|----|----------|----|----|----|----|----|----|---------|---------|----|----|----|
| Name  |         |    |    |    |          |    |    |    |    |    |    | AGE_DIS | AGE_CNT |    |    |    |
| Type  |         |    |    |    |          |    |    |    |    |    |    | RW      | RW      |    |    |    |
| Reset |         |    |    |    |          |    |    |    |    |    |    | 0       | 1       | 0  | 0  | 1  |
| Bit   | 15      | 14 | 13 | 12 | 11       | 10 | 9  | 8  | 7  | 6  | 5  | 4       | 3       | 2  | 1  | 0  |
| Name  | AGE_CNT |    |    |    | AGE_UNIT |    |    |    |    |    |    |         |         |    |    |    |
| Type  | RW      |    |    |    | RW       |    |    |    |    |    |    |         |         |    |    |    |
| Reset | 0       | 1  | 0  | 1  | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0       | 0       | 0  | 0  | 1  |

| Bit(s) | Name     | Description                                                                                                                                                                                                                                                                    |
|--------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20     | AGE_DIS  | <b>Address Table Aging Disable</b><br><br>Disable or pause MAC address aging.                                                                                                                                                                                                  |
| 19:12  | AGE_CNT  | <b>Address Table Age Count</b><br><br>This age count is recorded in the age timer field of the MAC address table when a new source address is received and the table entry is ready to refresh the timer. The applied age timer is equal to (AGE_CNT+1) *(AGE_UNIT+1) seconds. |
| 11:0   | AGE_UNIT | <b>Address Table Age Unit</b><br><br>The applied aging unit is equal to (AGE_UNIT+1) seconds.                                                                                                                                                                                  |

**150200A4 DHCP DHCP control 08100810**

| Bit   | 31   | 30 | 29 | 28 | 27              | 26            | 25              | 24            | 23 | 22 | 21              | 20              | 19         | 18             | 17 | 16 |
|-------|------|----|----|----|-----------------|---------------|-----------------|---------------|----|----|-----------------|-----------------|------------|----------------|----|----|
| Name  | REV0 |    |    |    | DHCPv6_MAN_G_FR | DHCPv6_PAE_FR | DHCPv6_BPD_U_FR | DHCPv6_EG_TAG |    |    | DHCPv6_LKY_VLAN | DHCPv6_PRI_HIGH | DHCPv6_MIR | DHCPv6_PORT_FW |    |    |
| Type  | RO   |    |    |    | RW              | RW            | RW              | RW            |    |    | RW              | RW              | RW         | RW             |    |    |
| Reset | 0    | 0  | 0  | 0  | 1               | 0             | 0               | 0             | 0  | 0  | 0               | 1               | 0          | 0              | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11              | 10            | 9               | 8             | 7  | 6  | 5               | 4               | 3          | 2              | 1  | 0  |
| Name  | REV1 |    |    |    | DHCPv4_MAN_G_FR | DHCPv4_PAE_FR | DHCPv4_BPD_U_FR | DHCPv4_EG_TAG |    |    | DHCPv4_LKY_VLAN | DHCPv4_PRI_HIGH | DHCPv4_MIR | DHCPv4_PORT_FW |    |    |
| Type  | RW   |    |    |    | RW              | RW            | RW              | RW            |    |    | RW              | RW              | RW         | RW             |    |    |
| Reset | 0    | 0  | 0  | 0  | 1               | 0             | 0               | 0             | 0  | 0  | 0               | 1               | 0          | 0              | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                                                              |
|--------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | REV0            | <b>Reserved</b>                                                                                                                                                                                                          |
| 27     | DHCPv6_MANG_FR  | <b>DHCPv6 Discovery/Request as Management Frame</b><br>0: Disable<br>1: Regarded as management frame                                                                                                                     |
| 26     | DHCPv6_PAE_FR   | <b>DHCPv6 Discovery/Request as PAE Frame</b><br>0: Disable<br>1: Regarded as PAE frame                                                                                                                                   |
| 25     | DHCPv6_BPDU_FR  | <b>DHCPv6 Discovery/Request as BPDU Frame</b><br>0: Non-BPDU Frame<br>1: Regarded as BPDU frame                                                                                                                          |
| 24:22  | DHCPv6_EG_TAG   | <b>DHCPv6 Discovery/Request Egress VLAN Tag Attribution</b><br>3'b000: System default (disable)<br>3'b001: Consistent<br>3'b010, 3'b011: Reserved<br>3'b100: Untagged<br>3'b101: Swap<br>3'b110: Tagged<br>3'b111: Stack |
| 21     | DHCPv6_LKY_VLAN | <b>DHCPv6 Discovery/Request Leaky VLAN Enable</b><br>0: Disable<br>1: Enable                                                                                                                                             |
| 20     | DHCPv6_PRI_HIGH | <b>DHCPv6 Discovery/Request Force the Highest Priority</b><br>0: System default                                                                                                                                          |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                                                                                                                            |
|--------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                 | 1: Assigned to the highest priority queue.                                                                                                                                                                                                                                                                                                                                                             |
| 19     | DHCPv6_MIR      | <b>DHCPv6 Discovery/Request to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                 |
| 18:16  | DHCPv6_PORT_FW  | <b>DHCPv6 Discovery/Request TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame Dropped |
| 15:12  | REV1            | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                        |
| 11     | DHCPv4_MANG_FR  | <b>DHCPv4 Discovery/Request as Management Frame</b><br><br>0: Disable<br><br>1: Regarded as management frame                                                                                                                                                                                                                                                                                           |
| 10     | DHCPv4_PAE_FR   | <b>DHCPv4 Discovery/Request as PAE Frame</b><br><br>0: Disable<br><br>1: Regarded as PAE frame                                                                                                                                                                                                                                                                                                         |
| 9      | DHCPv4_BPDU_FR  | <b>DHCPv4 Discovery/Request as BPDU Frame</b><br><br>0: Non-BPDU Frame<br><br>1: Regarded as BPDU frame                                                                                                                                                                                                                                                                                                |
| 8:6    | DHCPv4_EG_TAG   | <b>DHCPv4 Discovery/Request Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disable)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged<br><br>3'b101: Swap<br><br>3'b110: Tagged<br><br>3'b111: Stack                                                                                                                                                   |
| 5      | DHCPv4_LKY_VLAN | <b>DHCPv4 Discovery/Request Leaky VLAN Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                                                                                                                   |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                                                                                                                            |
|--------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4      | DHCPv4_PRI_HIGH | <b>DHCPv4 Discovery/Request Force the Highest Priority</b><br><br>0: System default<br><br>1: Assigned to the highest priority queue.                                                                                                                                                                                                                                                                  |
| 3      | DHCPv4_MIR      | <b>DHCPv4 Discovery/Request to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                 |
| 2:0    | DHCPv4_PORT_FW  | <b>DHCPv4 Discovery/Request TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame Dropped |

**150200A8      LCP      PPPoE LCP control      08100000**

| Bit   | 31   | 30 | 29 | 28 | 27              | 26             | 25              | 24             | 23 | 22 | 21 | 20               | 19               | 18            | 17              | 16 |
|-------|------|----|----|----|-----------------|----------------|-----------------|----------------|----|----|----|------------------|------------------|---------------|-----------------|----|
| Name  | REV0 |    |    |    | PPP_LCP_MANG_FR | PPP_LCP_PAE_FR | PPP_LCP_BPDU_FR | PPP_LCP_EG_TAG |    |    |    | PPP_LCP_LKY_VLAN | PPP_LCP_PRI_HIGH | PPP_LCP_P_MIR | PPP_LCP_PORT_FW |    |
| Type  | RW   |    |    |    | RW              | RW             | RW              | RW             |    |    |    | RW               | RW               | RW            | RW              |    |
| Reset | 0    | 0  | 0  | 0  | 1               | 0              | 0               | 0              | 0  | 0  | 0  | 1                | 0                | 0             | 0               | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11              | 10             | 9               | 8              | 7  | 6  | 5  | 4                | 3                | 2             | 1               | 0  |
| Name  | REV1 |    |    |    |                 |                |                 |                |    |    |    |                  |                  |               |                 |    |
| Type  | RW   |    |    |    |                 |                |                 |                |    |    |    |                  |                  |               |                 |    |
| Reset | 0    | 0  | 0  | 0  | 0               | 0              | 0               | 0              | 0  | 0  | 0  | 0                | 0                | 0             | 0               | 0  |

| Bit(s) | Name             | Description                                                                                                                                                                                                                                   |
|--------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | REV0             | <b>Reserved</b>                                                                                                                                                                                                                               |
| 27     | PPP_LCP_MANG_FR  | <b>PPPoE Session LCP as Management Frame</b><br><br>0: Disable<br><br>1: Regarded as management frame                                                                                                                                         |
| 26     | PPP_LCP_PAE_FR   | <b>PPPoE Session LCP as PAE Frame</b><br><br>0: Disable<br><br>1: Regarded as PAE frame                                                                                                                                                       |
| 25     | PPP_LCP_BPDU_FR  | <b>PPPoE Session LCP as BPDU Frame</b><br><br>0: Non-BPDU Frame<br><br>1: Regarded as BPDU frame                                                                                                                                              |
| 24:22  | PPP_LCP_EG_TAG   | <b>PPPoE Session LCP Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disable)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged<br><br>3'b101: Swap<br><br>3'b110: Tagged<br><br>3'b111: Stack |
| 21     | PPP_LCP_LKY_VLAN | <b>PPPoE Session LCP Leaky VLAN Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                 |
| 20     | PPP_LCP_PRI_HIGH | <b>PPPoE Session LCP Force the Highest Priority</b><br><br>0: System default<br><br>1: Assigned to the highest priority queue.                                                                                                                |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                                                                                                                     |
|--------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19     | PPP_LCP_MIR     | <b>PPPoE Session LCP to Mirror Port</b><br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                                 |
| 18:16  | PPP_LCP_PORT_FW | <b>PPPoE Session LCP TO_CPU Forwarding</b><br><br>3'b0xx: System default (disable)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)<br><br>3'b111: Frame Dropped |
| 15:0   | REV1            | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                 |



150200AC      MHS      MAC table hash seed      FFFFFFFF

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CRC_SEED |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1        | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CRC_SEED |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1        | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name     | Description                     |
|--------|----------|---------------------------------|
| 31:0   | CRC_SEED | MAC Table Hash CRC16/CRC32 Seed |
|        |          | CRC32: bit [31:0]               |
|        |          | CRC16: bit [15:0]               |

150200B0 CPGC Collision pool global control 00000017

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19           | 18            | 17             | 16         |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|--------------|---------------|----------------|------------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |              |               |                |            |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |              |               |                |            |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |              |               |                |            |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3            | 2             | 1              | 0          |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    | COL_B<br>USY | COL_RS<br>T_N | COL_CL<br>K_EN | COL_E<br>N |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    | RO           | RW            | RW             | RW         |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    | 0            | 1             | 1              | 1          |

| Bit(s) | Name       | Description                                                                                                                                                              |
|--------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3      | COL_BUSY   | <b>Collision Pool is Busy</b><br><br>0: IDLE<br><br>1: BUSY                                                                                                              |
| 2      | COL_RST_N  | <b>Collision Pool Soft Reset</b><br><br>Active Low. Before reset collision pool, it must be disabled and is not busy<br><br>0: Reset activated<br><br>1: Not activated   |
| 1      | COL_CLK_EN | <b>Collision Pool Clock Enable</b><br><br>Before enable/disable collision pool clock, collision pool must be disabled and is not busy<br><br>0: Disable<br><br>1: Enable |
| 0      | COL_EN     | <b>Collision Pool Enable</b><br><br>Do NOT enable collision pool while collision pool soft reset activated<br><br>0: Disable<br><br>1: Enable                            |

**150200B4 CPMONC Collision pool monitor control 00070020**

| Bit   | 31 | 30           | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21            | 20                       | 19                      | 18             | 17          | 16 |
|-------|----|--------------|----|----|----|----|----|----|----|----|---------------|--------------------------|-------------------------|----------------|-------------|----|
| Name  |    |              |    |    |    |    |    |    |    |    |               | COL_F<br>ULL_CN<br>T_CLR | COL_C<br>NT_CLR         | COL_CNT_CTRL   |             |    |
| Type  |    |              |    |    |    |    |    |    |    |    |               | W1S                      | W1S                     | RW             |             |    |
| Reset |    |              |    |    |    |    |    |    |    |    |               | 0                        | 0                       | 1              | 1           | 1  |
| Bit   | 15 | 14           | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5             | 4                        | 3                       | 2              | 1           | 0  |
| Name  |    | COL_USED_CNT |    |    |    |    |    |    |    |    | COL_E<br>MPTY | COL_F<br>ULL             | COL_F<br>ULL_CN<br>T_EN | COL_C<br>NT_EN | COL_MON_SEL |    |
| Type  |    | RO           |    |    |    |    |    |    |    |    | RO            | RO                       | RW                      | RW             | RW          |    |
| Reset |    | 0            | 0  | 0  | 0  | 0  | 0  | 0  |    |    | 1             | 0                        | 0                       | 0              | 0           | 0  |

| Bit(s) | Name             | Description                                                                                                                                                                                                                                                                   |
|--------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20     | COL_FULL_CNT_CLR | <b>Full and Collision Counter Reset</b><br><br>Return to 0 automatically after reset done<br><br>0: Reset released<br><br>1: Reset activated                                                                                                                                  |
| 19     | COL_CNT_CLR      | <b>Address Table Collision Counter Reset</b><br><br>Return to 0 automatically after reset done<br><br>0: Reset released<br><br>1: Reset activated                                                                                                                             |
| 18:16  | COL_CNT_CTRL     | <b>Collision Type Bit Map for Collision Counters</b><br><br>The type of collision for counters. To enable the specific type, set corresponding bits to 1.<br><br>BIT 0: DIP Table Collision<br><br>BIT 1: SA Learning Collision<br><br>BIT 2: CSR Path Write Access Collision |
| 14:8   | COL_USED_CNT     | <b>Collision Pool used entry counter</b>                                                                                                                                                                                                                                      |
| 5      | COL_EMPTY        | <b>Collision Pool is empty</b><br><br>0: Not empty<br><br>1: Empty                                                                                                                                                                                                            |
| 4      | COL_FULL         | <b>Collision Pool is full</b><br><br>0: Not full<br><br>1: Full                                                                                                                                                                                                               |
| 3      | COL_FULL_CNT_EN  | <b>Full and Collision Counter Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                   |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                  |
|--------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2      | COL_CNT_EN  | <b>Address Table Collision Counter Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                             |
| 1:0    | COL_MON_SEL | <b>Collision Pool Entry Status Monitor Selection</b><br><br>Select which type of entries are shown in Entry Status Monitor CPMOND1 and CPMOND2<br><br>2'b00: Empty entry<br><br>2'b01: Dynamic entry<br><br>2'b10: Reserved entry<br><br>2'b11: Static entry |

150200B8      CPMOND1      Collision pool entry status monitor 1      FFFFFFFF

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | ENTRY |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1     | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | ENTRY |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1     | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name  | Description                                                                                                                             |
|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | ENTRY | <b>Collision Pool Entry Status Monitor</b><br><br>Bit map of entry 31~0<br><br>0: Not hit selected status<br><br>1: Hit selected status |

**150200BC      CPMOND2      Collision pool entry status monitor 2      FFFFFFFF**

| Bit          | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | ENTRY |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 1     | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit          | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | ENTRY |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 1     | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name  | Description                                                                                                                              |
|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | ENTRY | <b>Collision Pool Entry Status Monitor</b><br><br>Bit map of entry 63~32<br><br>0: Not hit selected status<br><br>1: Hit selected status |

150200C0 CPSTSC Collision pool status counter 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | COL_FULL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | COL_CNT      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                             |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | COL_FULL_CNT | <b>Full and Collision Counter</b><br>Address Table Collision when Collision Pool is Full<br>Counter disabled automatically when Collision Pool disabled |
| 15:0   | COL_CNT      | <b>Address Table Collision Counter</b>                                                                                                                  |

150200C4      AISR\_EXT1      ACL extension interrupt status I      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | ACL_ISR_EXT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | ACL_ISR_EXT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                          |
|--------|-------------|--------------------------------------|
| 31:0   | ACL_ISR_EXT | ACL Interrupt Status for entry 32~63 |



150200C8      AISR\_EXT2      ACL extension interrupt status II      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | ACL_ISR_EXT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | ACL_ISR_EXT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                          |
|--------|-------------|--------------------------------------|
| 31:0   | ACL_ISR_EXT | ACL Interrupt Status for entry 64~95 |

150200CC      AISR\_EXT3      ACL extension interrupt status III      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | ACL_ISR_EXT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | ACL_ISR_EXT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | ACL_ISR_EXT | ACL Interrupt Status for entry 96~127 |

150200D0 MISR MLDv2 interrupt status 00000000

| Bit   | 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | MLDv2_ISR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MLDv2_ISR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name      | Description                                                                  |
|--------|-----------|------------------------------------------------------------------------------|
| 31:0   | MLDv2_ISR | <b>MLDv2 Interrupt Status for entry 0~31</b><br><br>0: Not hit<br><br>1: Hit |

150200D4 MISR\_EXT1 MLDv2 extension interrupt status I 00000000

| Bit   | 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | MLDv2_ISR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MLDv2_ISR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name      | Description                                                                   |
|--------|-----------|-------------------------------------------------------------------------------|
| 31:0   | MLDv2_ISR | <b>MLDv2 Interrupt Status for entry 32~63</b><br><br>0: Not hit<br><br>1: Hit |

150200E0      VAWD3      ACL write data III      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description                   |
|--------|-------|-------------------------------|
| 31:0   | WDATA | ACL Mask Table Write Data III |

150200E4      VAWD4      ACL write data IV      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description                  |
|--------|-------|------------------------------|
| 31:0   | WDATA | ACL Mask Table Write Data IV |

150200E8      VAWD5      ACL write data V      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description                 |
|--------|-------|-----------------------------|
| 31:0   | WDATA | ACL Mask Table Write Data V |

150200EC      VAWD6      ACL write data VI      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description                  |
|--------|-------|------------------------------|
| 31:0   | WDATA | ACL Mask Table Write Data VI |



150200F0      VAWD7      ACL write data VII      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description                   |
|--------|-------|-------------------------------|
| 31:0   | WDATA | ACL Mask Table Write Data VII |

150200F4      VAWD8      ACL write data VIII      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | WDATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name  | Description                    |
|--------|-------|--------------------------------|
| 31:0   | WDATA | ACL Mask Table Write Data VIII |

**15020100      PTC      Port trunking control      0000FE00**

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17   | 16 |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|------|----|
| Name  |          |    |    |    |    |    |    |    |    |    |    |    |    |    |      |    |
| Type  |          |    |    |    |    |    |    |    |    |    |    |    |    |    |      |    |
| Reset |          |    |    |    |    |    |    |    |    |    |    |    |    |    |      |    |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1    | 0  |
| Name  | INFO_SEL |    |    |    |    |    |    |    |    |    |    |    |    |    | BUSY |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    | RO   |    |
| Reset | 1        | 1  | 1  | 1  | 1  | 1  | 1  |    |    |    |    |    |    |    | 0    |    |

| Bit(s) | Name     | Description                                                                                                                                                                                                                                                                                                                                 |
|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:9   | INFO_SEL | <b>Information Control Bit Map</b><br><br>The information used to assign conversations to ports. To apply the information, set corresponding bits to 1.<br><br>BIT 0: Source Port<br><br>BIT 1: MAC SA<br><br>BIT 2: MAC DA<br><br>BIT 3: IPv4/IPv6 SIP<br><br>BIT 4: IPv4/IPv6 DIP<br><br>BIT 5: TCP/UDP SPORT<br><br>BIT 6: TCP/UDP DPORT |
| 1      | BUSY     | <b>Busy</b><br><br>0: IDLE<br><br>1: BUSY                                                                                                                                                                                                                                                                                                   |

15020104      PTHS      Port trunking algorithm seed      0000FFFF

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | SEED |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name | Description |
|--------|------|-------------|
| 15:0   | SEED | Seed        |

**15020108 PTGC0 Port trunking group control 0 00001012**

| Bit   | 31 | 30        | 29 | 28 | 27 | 26        | 25 | 24 | 23 | 22      | 21          | 20 | 19 | 18 | 17       | 16 |
|-------|----|-----------|----|----|----|-----------|----|----|----|---------|-------------|----|----|----|----------|----|
| Name  |    |           |    |    |    |           |    |    |    |         |             |    |    |    |          |    |
| Type  |    |           |    |    |    |           |    |    |    |         |             |    |    |    |          |    |
| Reset |    |           |    |    |    |           |    |    |    |         |             |    |    |    |          |    |
| Bit   | 15 | 14        | 13 | 12 | 11 | 10        | 9  | 8  | 7  | 6       | 5           | 4  | 3  | 2  | 1        | 0  |
| Name  |    | GRP_PORT1 |    |    |    | GRP_PORT0 |    |    |    | ACL_TNK | SA_LRN_PORT |    |    |    | LINK_DWN | EN |
| Type  |    | RW        |    |    |    | RW        |    |    |    | RW      | RW          |    |    |    | RO       | RW |
| Reset |    | 0         | 0  | 1  |    | 0         | 0  | 0  |    | 0       | 0           | 1  |    |    | 1        | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                              |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14:12  | GRP_PORT1   | <b>Trunking Port 1</b><br><br>Set the trunking port of this group                                                                                                                                                                        |
| 10:8   | GRP_PORT0   | <b>Trunking Port 0</b><br><br>Set the trunking port of this group                                                                                                                                                                        |
| 6      | ACL_TNK     | <b>ACL Destination Port Trunking</b><br><br>Enable Port Trunking for ACL forced destination port if the destination port is trunking port.<br><br>0: Disable<br><br>1: Enable                                                            |
| 5:4    | SA_LRN_PORT | <b>Port Trunking Source MAC Address Learning Port</b><br><br>Select the source port for MAC SA Learning if ingress port is in this trunking group.<br><br>2'b00: Ingress Port<br>2'b01: GRP_PORT0<br>2'b10: GRP_PORT1<br>2'b11: Reserved |
| 1      | LINK_DWN    | <b>Port Trunking Group Link Down</b><br><br>Link down when all trunking ports link down<br><br>Link up when one or more trunking ports link up<br><br>0: Link Up<br><br>1: Link Down                                                     |
| 0      | EN          | <b>Port Trunking Group Enable</b><br><br>Enable/Disable this group<br><br>0: Disable<br><br>1: Enable                                                                                                                                    |

| Bit(s) | Name | Description |
|--------|------|-------------|
|--------|------|-------------|

**1502010C      PTC1      Port trunking group control 1      00004312**

| Bit   | 31 | 30        | 29 | 28 | 27 | 26        | 25 | 24 | 23 | 22      | 21          | 20 | 19 | 18 | 17       | 16 |
|-------|----|-----------|----|----|----|-----------|----|----|----|---------|-------------|----|----|----|----------|----|
| Name  |    |           |    |    |    |           |    |    |    |         |             |    |    |    |          |    |
| Type  |    |           |    |    |    |           |    |    |    |         |             |    |    |    |          |    |
| Reset |    |           |    |    |    |           |    |    |    |         |             |    |    |    |          |    |
| Bit   | 15 | 14        | 13 | 12 | 11 | 10        | 9  | 8  | 7  | 6       | 5           | 4  | 3  | 2  | 1        | 0  |
| Name  |    | GRP_PORT1 |    |    |    | GRP_PORT0 |    |    |    | ACL_TNK | SA_LRN_PORT |    |    |    | LINK_DWN | EN |
| Type  |    | RW        |    |    |    | RW        |    |    |    | RW      | RW          |    |    |    | RO       | RW |
| Reset |    | 1         | 0  | 0  |    | 0         | 1  | 1  |    | 0       | 0           | 1  |    |    | 1        | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                              |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14:12  | GRP_PORT1   | <b>Trunking Port 1</b><br><br>Set the trunking port of this group                                                                                                                                                                        |
| 10:8   | GRP_PORT0   | <b>Trunking Port 0</b><br><br>Set the trunking port of this group                                                                                                                                                                        |
| 6      | ACL_TNK     | <b>ACL Destination Port Trunking</b><br><br>Enable Port Trunking for ACL forced destination port if the destination port is trunking port.<br><br>0: Disable<br><br>1: Enable                                                            |
| 5:4    | SA_LRN_PORT | <b>Port Trunking Source MAC Address Learning Port</b><br><br>Select the source port for MAC SA Learning if ingress port is in this trunking group.<br><br>2'b00: Ingress Port<br>2'b01: GRP_PORT0<br>2'b10: GRP_PORT1<br>2'b11: Reserved |
| 1      | LINK_DWN    | <b>Port Trunking Group Link Down</b><br><br>Link down when all trunking ports link down<br><br>Link up when one or more trunking ports link up<br><br>0: Link Up<br><br>1: Link Down                                                     |
| 0      | EN          | <b>Port Trunking Group Enable</b><br><br>Enable/Disable this group<br><br>0: Disable<br><br>1: Enable                                                                                                                                    |

| Bit(s) | Name | Description |
|--------|------|-------------|
|--------|------|-------------|



**15020110      PTC2      Port trunking group control 2      00006512**

| Bit   | 31 | 30        | 29 | 28 | 27 | 26        | 25 | 24 | 23 | 22      | 21          | 20 | 19 | 18 | 17       | 16 |
|-------|----|-----------|----|----|----|-----------|----|----|----|---------|-------------|----|----|----|----------|----|
| Name  |    |           |    |    |    |           |    |    |    |         |             |    |    |    |          |    |
| Type  |    |           |    |    |    |           |    |    |    |         |             |    |    |    |          |    |
| Reset |    |           |    |    |    |           |    |    |    |         |             |    |    |    |          |    |
| Bit   | 15 | 14        | 13 | 12 | 11 | 10        | 9  | 8  | 7  | 6       | 5           | 4  | 3  | 2  | 1        | 0  |
| Name  |    | GRP_PORT1 |    |    |    | GRP_PORT0 |    |    |    | ACL_TNK | SA_LRN_PORT |    |    |    | LINK_DWN | EN |
| Type  |    | RW        |    |    |    | RW        |    |    |    | RW      | RW          |    |    |    | RO       | RW |
| Reset |    | 1         | 1  | 0  |    | 1         | 0  | 1  |    | 0       | 0           | 1  |    |    | 1        | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                              |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14:12  | GRP_PORT1   | <b>Trunking Port 1</b><br><br>Set the trunking port of this group                                                                                                                                                                        |
| 10:8   | GRP_PORT0   | <b>Trunking Port 0</b><br><br>Set the trunking port of this group                                                                                                                                                                        |
| 6      | ACL_TNK     | <b>ACL Destination Port Trunking</b><br><br>Enable Port Trunking for ACL forced destination port if the destination port is trunking port.<br><br>0: Disable<br><br>1: Enable                                                            |
| 5:4    | SA_LRN_PORT | <b>Port Trunking Source MAC Address Learning Port</b><br><br>Select the source port for MAC SA Learning if ingress port is in this trunking group.<br><br>2'b00: Ingress Port<br>2'b01: GRP_PORT0<br>2'b10: GRP_PORT1<br>2'b11: Reserved |
| 1      | LINK_DWN    | <b>Port Trunking Group Link Down</b><br><br>Link down when all trunking ports link down<br><br>Link up when one or more trunking ports link up<br><br>0: Link Up<br><br>1: Link Down                                                     |
| 0      | EN          | <b>Port Trunking Group Enable</b><br><br>Enable/Disable this group<br><br>0: Disable<br><br>1: Enable                                                                                                                                    |

| Bit(s) | Name | Description |
|--------|------|-------------|
|--------|------|-------------|

15020114      **PTGSC0**      Port trunking group security control 0      0000FFF8

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16            |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|
| Name  |            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |
| Type  |            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |
| Reset |            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0             |
| Name  | MAX_SA_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SA_CN<br>T_EN |
| Type  | RW         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW            |
| Reset | 1          | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |    |    | 0             |

| Bit(s) | Name       | Description                                                                                                                      |
|--------|------------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:3   | MAX_SA_CNT | <b>SA Allowable Learning Number</b><br><br>Maximum number of SA learned addresses for this trunking group when SA_CNT_EN is set. |
| 0      | SA_CNT_EN  | <b>Enables the learned source MAC Address counter of this group</b><br><br>0: Disable<br><br>1: Enable                           |

**15020118**      **PTGSC1**      **Port trunking group security control 1**      **0000FFF8**

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16            |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|
| Name  |            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |
| Type  |            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |
| Reset |            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0             |
| Name  | MAX_SA_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SA_CN<br>T_EN |
| Type  | RW         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW            |
| Reset | 1          | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |    |    | 0             |

| Bit(s) | Name       | Description                                                                                                                      |
|--------|------------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:3   | MAX_SA_CNT | <b>SA Allowable Learning Number</b><br><br>Maximum number of SA learned addresses for this trunking group when SA_CNT_EN is set. |
| 0      | SA_CNT_EN  | <b>Enables the learned source MAC Address counter of this group</b><br><br>0: Disable<br><br>1: Enable                           |

**1502011C      PTGSC2      Port trunking group security control 2      0000FFF8**

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16            |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|
| Name  |            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |
| Type  |            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |
| Reset |            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0             |
| Name  | MAX_SA_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SA_CN<br>T_EN |
| Type  | RW         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW            |
| Reset | 1          | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |    |    | 0             |

| Bit(s) | Name       | Description                                                                                                                      |
|--------|------------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:3   | MAX_SA_CNT | <b>SA Allowable Learning Number</b><br><br>Maximum number of SA learned addresses for this trunking group when SA_CNT_EN is set. |
| 0      | SA_CNT_EN  | <b>Enables the learned source MAC Address counter of this group</b><br><br>0: Disable<br><br>1: Enable                           |

**15020120 SPTC0 Port trunking table control 84F0012C**

| Bit          | 31       | 30 | 29 | 28      | 27       | 26 | 25 | 24      | 23       | 22 | 21 | 20 | 19      | 18 | 17 | 16 |
|--------------|----------|----|----|---------|----------|----|----|---------|----------|----|----|----|---------|----|----|----|
| <b>Name</b>  | TBL1_GRP |    |    | TBL1_EN | TBLO_GRP |    |    | TBLO_EN | INFO_SEL |    |    |    | AGE_CNT |    |    |    |
| <b>Type</b>  | RW       |    |    | RW      | RW       |    |    | RW      | RW       |    |    |    | RW      |    |    |    |
| <b>Reset</b> | 1        | 0  |    | 0       | 0        | 1  |    | 0       | 1        | 1  | 1  | 1  | 0       | 0  | 0  | 0  |
| <b>Bit</b>   | 15       | 14 | 13 | 12      | 11       | 10 | 9  | 8       | 7        | 6  | 5  | 4  | 3       | 2  | 1  | 0  |
| <b>Name</b>  | AGE_CNT  |    |    |         |          |    |    |         |          |    |    |    |         |    |    |    |
| <b>Type</b>  | RW       |    |    |         |          |    |    |         |          |    |    |    |         |    |    |    |
| <b>Reset</b> | 0        | 0  | 0  | 0       | 0        | 0  | 0  | 1       | 0        | 0  | 1  | 0  | 1       | 1  | 0  | 0  |

| Bit(s) | Name     | Description                                                                                                                                                                                                                                                                                |
|--------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30  | TBL1_GRP | <b>Trunking Table 1 Group Selection</b><br>Select trunking group to be serviced<br>2'b00: Group 0<br>2'b01: Group 1<br>2'b10: Group 2<br>2'b11: Reserved                                                                                                                                   |
| 28     | TBL1_EN  | <b>Trunking Table 1 Enable</b><br>0: Disable<br>1: Enable                                                                                                                                                                                                                                  |
| 27:26  | TBLO_GRP | <b>Trunking Table 0 Group Selection</b><br>Select trunking group to be serviced<br>2'b00: Group 0<br>2'b01: Group 1<br>2'b10: Group 2<br>2'b11: Reserved                                                                                                                                   |
| 24     | TBLO_EN  | <b>Trunking Table 0 Enable</b><br>0: Disable<br>1: Enable                                                                                                                                                                                                                                  |
| 23:20  | INFO_SEL | <b>Trunking Table Information Control Bit Map</b><br>The information used by table to assign conversations to ports. To apply the information, set corresponding bits in the bit map to 1.<br>BIT 0: IPv4/IPv6 SIP<br>BIT 1: IPv4/IPv6 DIP<br>BIT 2: TCP/UDP SPORT<br>BIT 3: TCP/UDP DPORT |

| Bit(s) | Name    | Description                                                                                                                                                                        |
|--------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:0   | AGE_CNT | <b>Trunking Table Age Count</b><br><br>This age count is recorded in the age timer field of the Trunking table for a new entry. The applied age timer is equal to AGE_CNT seconds. |

15021000

MMSCRO\_Q0P0

Max-Min scheduler control register 0 of Queue  
0/Port 0

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q0_P0  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q0_P0 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q0_P0 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q0_P0 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q0_P0             | <b>Port 0 Queue 0 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                                                                                                                                                                                  |
| 15     | MIN_RATE_EN_Q0_P0            | <b>Port 0 Queue 0 min. shaper rate limit control is enabled</b><br><br>0: Queue 0 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 0 min. shaper rate limit control is enabled                                                                                                                                                                                                                                |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q0_P0 | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 0 min. shaper rate limit control, value range: 0 to 5<br><br>0: 1Kbps<br>1: 10Kbps<br>2: 100Kbps<br>3: 1Mbps<br>4: 10Mbps<br>5: 100Mbps<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14<br><br>0: 1/128ms<br>1: 1/64ms<br>2: 1/32ms<br>3: 1/16ms<br>4: 1/8ms |



| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--------|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                                | 5: 1/4ms                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                                | 6: 1/2ms                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                                | 7: 1ms                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|        |                                | 8: 2ms                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|        |                                | 9: 4ms                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|        |                                | 10: 8ms                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                                | 11: 16ms                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                                | 12: 32ms                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                                | 13: 64ms                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                                | 14: 128ms                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q0_P0 | <p><b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b></p> <p>When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 0 min. shaper rate limit control, value range: 1 to 255</p> <p>Final Rate Limit = <math>MAN * 10^{(EXP)} * 1Kbps</math></p> <p>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping, and</p> <p>Token Bucket = Max ( MIN_RATE_CIR*TB_T, TB_CBS*512 )</p> |

15021004

MMSCR1\_Q0P0

Max-Min scheduler control register 1 of Queue  
0/Port 0

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q0_P0  |    |    |    | MAX_WEIGHT_Q0_P0             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q0_P0 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q0_P0 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q0_P0 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|--------|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q0_P0             | <b>Port 0 Queue 0 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                                                                                                                                      |
| 27:24  | MAX_WEIGHT_Q0_P0             | <b>Port 0 Queue 0 weighted value for max. WFQ weighted value is (q0_max_weight+1'b1)</b>                                                                                                                                                                                                                                                                                                                                                        |
| 15     | MAX_RATE_EN_Q0_P0            | <b>Port 0 Queue 0 max. shaper rate limit control is enabled</b><br><br>0: Queue 0 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 0 max. shaper rate limit control is enabled                                                                                                                                                                                               |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q0_P0 | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 0 max. shaper rate limit control, value range: 0 to 5<br><br>0: 1Kbps<br>1: 10Kbps<br>2: 100Kbps<br>3: 1Mbps<br>4: 10Mbps<br>5: 100Mbps<br><br>When MIN_MAX_TB_EN = 1, TB_T period for rate measurement, value range: 0 to 14<br><br>0: 1/128ms<br>1: 1/64ms<br>2: 1/32ms |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--------|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                                | 3: 1/16ms                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                                | 4: 1/8ms                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                                | 5: 1/4ms                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                                | 6: 1/2ms                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                                | 7: 1ms                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|        |                                | 8: 2ms                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|        |                                | 9: 4ms                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|        |                                | 10: 8ms                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                                | 11: 16ms                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                                | 12: 32ms                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                                | 13: 64ms                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                                | 14: 128ms                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q0_P0 | <p><b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b></p> <p>When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 0 max. shaper rate limit control, value range: 1 to 255</p> <p>Final Rate Limit = <math>MAN * 10^{(EXP)} * 1Kbps</math></p> <p>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping, and</p> <p>Token Bucket = Max ( MAX_RATE_CIR*TB_T, TB_CBS*512 )</p> |

15021008

MMSCRO\_Q1P0

Max-Min scheduler control register 0 of Queue  
1/Port 0

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q1_P0  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q1_P0 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q1_P0 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q1_P0 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q1_P0               | <b>Port 0 Queue 1 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q1_P0              | <b>Port 0 Queue 1 min. shaper rate limit control is enabled</b><br><br>0: Queue 1 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 1 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q1_P0   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 1 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q1_P0 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 1 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

1502100C

MMSCR1\_Q1P0

Max-Min scheduler control register 1 of Queue  
1/Port 0

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q1_P0  |    |    |    | MAX_WEIGHT_Q1_P0             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q1_P0 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q1_P0 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q1_P0 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q1_P0               | <b>Port 0 Queue 1 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q1_P0               | <b>Port 0 Queue 1 weighted value for max. WFQ weighted value is (q1_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q1_P0              | <b>Port 0 Queue 1 max. shaper rate limit control is enabled</b><br><br>0: Queue 1 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 1 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q1_P0   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 1 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q1_P0 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 1 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021010

MMSCRO\_Q2P0

Max-Min scheduler control register 0 of Queue  
2/Port 0

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q2_P0  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q2_P0 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q2_P0 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q2_P0 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q2_P0               | <b>Port 0 Queue 2 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q2_P0              | <b>Port 0 Queue 2 min. shaper rate limit control is enabled</b><br><br>0: Queue 2 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 2 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q2_P0   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 2 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q2_P0 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 2 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021014

MMSCR1\_Q2P0

Max-Min scheduler control register 1 of Queue  
2/Port 0

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q2_P0  |    |    |    | MAX_WEIGHT_Q2_P0             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q2_P0 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q2_P0 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q2_P0 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q2_P0               | <b>Port 0 Queue 2 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q2_P0               | <b>Port 0 Queue 2 weighted value for max. WFQ weighted value is (q1_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q2_P0              | <b>Port 0 Queue 2 max. shaper rate limit control is enabled</b><br><br>0: Queue 2 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 2 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q2_P0   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 2 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q2_P0 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 2 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021018

MMSCRO\_Q3P0

Max-Min scheduler control register 0 of Queue  
3/Port 0

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q3_P0  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q3_P0 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q3_P0 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q3_P0 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q3_P0               | <b>Port 0 Queue 3 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q3_P0              | <b>Port 0 Queue 3 min. shaper rate limit control is enabled</b><br><br>0: Queue 3 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 3 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q3_P0   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 3 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q3_P0 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 3 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |



1502101C

MMSCR1\_Q3P0

Max-Min scheduler control register 1 of Queue  
3/Port 0

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q3_P0  |    |    |    | MAX_WEIGHT_Q3_P0             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q3_P0 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q3_P0 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q3_P0 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q3_P0               | <b>Port 0 Queue 3 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q3_P0               | <b>Port 0 Queue 3 weighted value for max. WFQ weighted value is (q3_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q3_P0              | <b>Port 0 Queue 3 max. shaper rate limit control is enabled</b><br><br>0: Queue 3 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 3 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q3_P0   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 3 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q3_P0 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 3 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021020

MMSCRO\_Q4P0

Max-Min scheduler control register 0 of Queue  
4/Port 0

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q4_P0  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q4_P0 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q4_P0 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q4_P0 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q4_P0               | <b>Port 0 Queue 4 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q4_P0              | <b>Port 0 Queue 4 min. shaper rate limit control is enabled</b><br><br>0: Queue 4 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 4 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q4_P0   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 4 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q4_P0 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 4 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021024

MMSCR1\_Q4P0

Max-Min scheduler control register 1 of Queue  
4/Port 0

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q4_P0  |    |    |    | MAX_WEIGHT_Q4_P0             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q4_P0 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q4_P0 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q4_P0 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q4_P0               | <b>Port 0 Queue 4 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q4_P0               | <b>Port 0 Queue 4 weighted value for max. WFQ weighted value is (q4_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q4_P0              | <b>Port 0 Queue 4 max. shaper rate limit control is enabled</b><br><br>0: Queue 4 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 4 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q4_P0   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 4 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q4_P0 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 4 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021028

MMSCRO\_Q5P0

Max-Min scheduler control register 0 of Queue  
5/Port 0

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q5_P0  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q5_P0 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q5_P0 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q5_P0 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q5_P0               | <b>Port 0 Queue 5 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q5_P0              | <b>Port 0 Queue 5 min. shaper rate limit control is enabled</b><br><br>0: Queue 5 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 5 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q5_P0   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 5 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q5_P0 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 5 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

1502102C

MMSCR1\_Q5P0

Max-Min scheduler control register 1 of Queue  
5/Port 0

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q5_P0  |    |    |    | MAX_WEIGHT_Q5_P0             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q5_P0 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q5_P0 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q5_P0 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q5_P0               | <b>Port 0 Queue 5 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q5_P0               | <b>Port 0 Queue 5 weighted value for max. WFQ weighted value is (q5_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q5_P0              | <b>Port 0 Queue 5 max. shaper rate limit control is enabled</b><br><br>0: Queue 5 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 5 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q5_P0   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 5 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q5_P0 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 5 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021030

MMSCRO\_Q6P0

Max-Min scheduler control register 0 of Queue  
6/Port 0

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q6_P0  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q6_P0 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q6_P0 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q6_P0 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q6_P0               | <b>Port 0 Queue 6 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q6_P0              | <b>Port 0 Queue 6 min. shaper rate limit control is enabled</b><br><br>0: Queue 6 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 6 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q6_P0   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 6 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q6_P0 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 6 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021034

MMSCR1\_Q6P0

Max-Min scheduler control register 1 of Queue  
6/Port 0

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q6_P0  |    |    |    | MAX_WEIGHT_Q6_P0             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q6_P0 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q6_P0 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q6_P0 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q6_P0               | <b>Port 0 Queue 6 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q6_P0               | <b>Port 0 Queue 6 weighted value for max. WFQ weighted value is (q6_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q6_P0              | <b>Port 0 Queue 6 max. shaper rate limit control is enabled</b><br><br>0: Queue 6 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 6 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q6_P0   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 6 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q6_P0 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 6 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021038

MMSCRO\_Q7P0

Max-Min scheduler control register 0 of Queue  
7/Port 0

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q7_P0  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q7_P0 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q7_P0 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q7_P0 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                         |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q7_P0               | <b>Port 0 Queue 7 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                     |
| 15     | MIN_RATE_EN_Q7_P0              | <b>Port 0 Queue 7 min. shaper rate limit control is enabled</b><br><br>0: Queue 7 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 7 min. shaper rate limit control is enabled                                                                   |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q7_P0   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 7 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, TB_T period for rate measurement, value range: 0 to 14   |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q7_P0 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 7 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping |



1502103C

MMSCR1\_Q7P0

Max-Min scheduler control register 1 of Queue  
7/Port 0

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q7_P0  |    |    |    | MAX_WEIGHT_Q7_P0             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q7_P0 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q7_P0 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q7_P0 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q7_P0               | <b>Port 0 Queue 7 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q7_P0               | <b>Port 0 Queue 7 weighted value for max. WFQ weighted value is (q7_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q7_P0              | <b>Port 0 Queue 7 max. shaper rate limit control is enabled</b><br><br>0: Queue 7 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 7 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q7_P0   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 7 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q7_P0 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 7 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

**15021040 ERLCR\_P0 Egress rate limit control register of Port 0 00000000**

| Bit          | 31                   | 30           | 29 | 28                 | 27                               | 26 | 25 | 24 | 23                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------------|--------------|----|--------------------|----------------------------------|----|----|----|------------------------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | EGC_RATE_CIR_15_0_P0 |              |    |                    |                                  |    |    |    |                                    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                   |              |    |                    |                                  |    |    |    |                                    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0            | 0  | 0                  | 0                                | 0  | 0  | 0  | 0                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                   | 14           | 13 | 12                 | 11                               | 10 | 9  | 8  | 7                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | EG_RATE_LIMIT_EN_P0  | EGC_TB_EN_P0 |    | EGC_RATE_CIR_16_P0 | EG_RATE_LIMIT_EXP_P0_EGC_TB_T_P0 |    |    |    | EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                   | RW           |    | RW                 | RW                               |    |    |    | RW                                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0            |    | 0                  | 0                                | 0  | 0  | 0  | 0                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                             | Description                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | EGC_RATE_CIR_15_0_P0             | <p>When EGC_TB_EN = 1, total 17 bits EGC_RATE_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps</p> <p><math>EGC\_RATE\_CIR = [Egress\ Rate\ Limit(bps) / 32Kbps]</math></p>                                                                                                                                                                                                          |
| 15     | EG_RATE_LIMIT_EN_P0              | <p><b>Port 0 Egress rate limit control is enabled</b></p> <p>0: Egress rate limit control disable</p> <p>1: Enable</p>                                                                                                                                                                                                                                                                                                              |
| 14     | EGC_TB_EN_P0                     | <p><b>When this bit is disabled, the Egress rate control acts like a leaky bucket principle.</b></p> <p>Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p>                                                                                                      |
| 12     | EGC_RATE_CIR_16_P0               | <b>Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value</b>                                                                                                                                                                                                                                                                                                                                                                  |
| 11:8   | EG_RATE_LIMIT_EXP_P0_EGC_TB_T_P0 | <p><b>Depend on EGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b></p> <p>When EGC_TB_EN = 0, exponent part of Port 0 Egress rate limit control, value range: 0 to 5</p> <p>0: 1Kbps</p> <p>1: 10Kbps</p> <p>2: 100Kbps</p> <p>3: 1Mbps</p> <p>4: 10Mbps</p> <p>5: 100Mbps</p> <p>When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, value range: 0 to 14</p> <p>0: 1/128ms</p> |

| Bit(s) | Name                               | Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
|--------|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                                    | 1: 1/64ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        |                                    | 2: 1/32ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        |                                    | 3: 1/16ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        |                                    | 4: 1/8ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 5: 1/4ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 6: 1/2ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 7: 1ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                                    | 8: 2ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                                    | 9: 4ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                                    | 10: 8ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                                    | 11: 16ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 12: 32ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 13: 64ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 14: 128ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7:0    | EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0 | <p><b>Depend on EGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b></p> <p>When EGC_TB_EN = 0, mantissa part of Port 0 Egress rate limit control, value range: 1 to 255</p> <p>Egress Rate Limit = <math>MAN * 10^{(EXP)} * 1Kbps</math></p> <p>When EGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and</p> <p>Token Bucket = Max ( EGC_RATE_CIR*EGC_TB_T, EGC_TB_CBS*512 )</p> |

15021050

MMSCR2\_Q0P0

Max-Min scheduler control register 2 of Queue  
0/Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_RATE_CIR_Q0_P0 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MIN_RATE_CIR_Q0_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                                                                                                                                          |
|--------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q0_P0 | <p>When MIN_MAX_TB_EN = 1, total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps</p> <p><math>MIN\_RATE\_CIR = \lceil MIN\ Shaper\ Rate\ Limit(bps) / 32Kbps \rceil</math></p> |

15021054

MMSCR3\_Q0P0

Max-Min scheduler control register 3 of Queue  
0/Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q0_P0 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q0_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                                                                                                                                               |
|--------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q0_P0 | <p>When MIN_MAX_TB_EN = 1, total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps</p> <p><math>MAX\_RATE\_CIR = \lceil MAX \text{ Shaper Rate Limit(bps)} / 32Kbps \rceil</math></p> |

15021058

MMSCR2\_Q1P0Max-Min scheduler control register 2 of Queue  
1/Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                            |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_C<br>R_Q1_<br>P0 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                            |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                             |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                             |
| Name  | MIN_RATE_CIR_Q1_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                             |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q1_P0 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502105C

MMSCR3\_Q1P0Max-Min scheduler control register 3 of Queue  
1/Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q1_P0 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q1_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q1_P0 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021060

MMSCR2\_Q2P0Max-Min scheduler control register 2 of Queue  
2/Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                            |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_C<br>R_Q2_<br>P0 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                            |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                             |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                             |
| Name  | MIN_RATE_CIR_Q2_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                             |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q2_P0 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |



15021064

MMSCR3\_Q2P0Max-Min scheduler control register 3 of Queue  
2/Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q2_P0 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q2_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q2_P0 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021068

MMSCR2\_Q3P0Max-Min scheduler control register 2 of Queue  
3/Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                            |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_C<br>R_Q3_<br>P0 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                            |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                             |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                             |
| Name  | MIN_RATE_CIR_Q3_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                             |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q3_P0 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502106C

MMSCR3\_Q3P0Max-Min scheduler control register 3 of Queue  
3/Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q3_P0 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q3_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q3_P0 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021070

MMSCR2\_Q4P0Max-Min scheduler control register 2 of Queue  
4/Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                            |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_C<br>R_Q4_<br>P0 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                            |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                             |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                             |
| Name  | MIN_RATE_CIR_Q4_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                             |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q4_P0 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021074

MMSCR3\_Q4P0Max-Min scheduler control register 3 of Queue  
4/Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                            |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_R<br>ATE_C<br>R_Q4_<br>P0 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                            |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                             |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                             |
| Name  | MAX_RATE_CIR_Q4_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                             |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q4_P0 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021078

MMSCR2\_Q5P0

Max-Min scheduler control register 2 of Queue  
5/Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                     |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_CIR_Q5_P0 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                     |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                      |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                      |
| Name  | MIN_RATE_CIR_Q5_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                      |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q5_P0 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502107C

MMSCR3\_Q5P0

Max-Min scheduler control register 3 of Queue  
5/Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q5_P0 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q5_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q5_P0 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021080

MMSCR2\_Q6P0

Max-Min scheduler control register 2 of Queue  
6/Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                     |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_CIR_Q6_P0 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                     |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                      |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                      |
| Name  | MIN_RATE_CIR_Q6_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                      |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q6_P0 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |



15021084

MMSCR3\_Q6P0Max-Min scheduler control register 3 of Queue  
6/Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q6_P0 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q6_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q6_P0 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021088

MMSCR2\_Q7P0

Max-Min scheduler control register 2 of Queue  
7/Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_RATE_CIR_Q7_P0 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MIN_RATE_CIR_Q7_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q7_P0 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502108C

MMSCR3\_Q7P0

Max-Min scheduler control register 3 of Queue  
7/Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q7_P0 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q7_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q7_P0 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

**15021090**      **MMSCR\_P0**      **Max-Min scheduler control register of Port 0**      **00000001**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_MAX_TB_EN_P0 |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW               |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 1                |

| Bit(s) | Name             | Description                                                                                                                                                                                                                                                                                                  |
|--------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0      | MIN_MAX_TB_EN_P0 | <p><b>When this bit is disabled, the rate limit acts like a leaky bucket principle.</b></p> <p>Otherwise, the rate limit uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p> |

**150210E0 GERLCR Global egress rate limit control register 00000118**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25          | 24         | 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|-------------|------------|--------------|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    |    |             |            |              |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    |    |             |            |              |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    |    |             |            |              |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9           | 8          | 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    |    | EGC_MFRM_EX | EGC_IPG_OP | EGC_IPG_BYTE |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    |    | RW          | RW         | RW           |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    |    | 0           | 1          | 0            | 0  | 0  | 1  | 1  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9      | EGC_MFRM_EX  | <p><b>When this bit is enabled, management frames are excluded in the egress rate limit control mechanism; otherwise, management frames are included.</b></p> <p>(Management frame type is set by ARL registers)</p> <p>0: Include management frames</p> <p>1: Exclude management frames</p> |
| 8      | EGC_IPG_OP   | <p><b>Egress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted for the rate calculation.</b></p> <p>0: IPG byte is excluded</p> <p>1: IPG byte is included</p>                                                                                                  |
| 7:0    | EGC_IPG_BYTE | <p><b>Egress Rate IPG Byte Count</b></p> <p>Byte count should be added while calculating the rate limit.</p> <p>0x04: 4-byte CRC</p> <p>0x18: 4-byte CRC + 12 byte IPG + 8 byte Preamble (default)</p>                                                                                       |

15021100

MMSCRO\_Q0P1

Max-Min scheduler control register 0 of Queue  
0/Port 1

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q0_P1  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q0_P1 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q0_P1 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q0_P1 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q0_P1               | <b>Port 1 Queue 0 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q0_P1              | <b>Port 1 Queue 0 min. shaper rate limit control is enabled</b><br><br>0: Queue 0 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 0 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q0_P1   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 0 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q0_P1 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 0 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021104

MMSCR1\_Q0P1

Max-Min scheduler control register 1 of Queue  
0/Port 1

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q0_P1  |    |    |    | MAX_WEIGHT_Q0_P1             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q0_P1 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q0_P1 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q0_P1 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q0_P1               | <b>Port 1 Queue 0 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q0_P1               | <b>Port 1 Queue 0 weighted value for max. WFQ weighted value is (q0_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q0_P1              | <b>Port 1 Queue 0 max. shaper rate limit control is enabled</b><br><br>0: Queue 0 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 0 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q0_P1   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 0 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q0_P1 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 0 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021108

MMSCRO\_Q1P1

Max-Min scheduler control register 0 of Queue  
1/Port 1

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q1_P1  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q1_P1 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q1_P1 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q1_P1 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q1_P1               | <b>Port 1 Queue 1 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q1_P1              | <b>Port 1 Queue 1 min. shaper rate limit control is enabled</b><br><br>0: Queue 1 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 1 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q1_P1   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 1 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q1_P1 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 1 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |



1502110C

MMSCR1\_Q1P1

Max-Min scheduler control register 1 of Queue  
1/Port 1

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q1_P1  |    |    |    | MAX_WEIGHT_Q1_P1             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q1_P1 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q1_P1 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q1_P1 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q1_P1               | <b>Port 1 Queue 1 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q1_P1               | <b>Port 1 Queue 1 weighted value for max. WFQ weighted value is (q1_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q1_P1              | <b>Port 1 Queue 1 max. shaper rate limit control is enabled</b><br><br>0: Queue 1 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 1 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q1_P1   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 1 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q1_P1 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 1 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021110

MMSCRO\_Q2P1

Max-Min scheduler control register 0 of Queue  
2/Port 1

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q2_P1  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q2_P1 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q2_P1 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q2_P1 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q2_P1               | <b>Port 1 Queue 2 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q2_P1              | <b>Port 1 Queue 2 min. shaper rate limit control is enabled</b><br><br>0: Queue 2 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 2 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q2_P1   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 2 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q2_P1 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 2 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021114

MMSCR1\_Q2P1

Max-Min scheduler control register 1 of Queue  
2/Port 1

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q2_P1  |    |    |    | MAX_WEIGHT_Q2_P1             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q2_P1 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q2_P1 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q2_P1 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q2_P1               | <b>Port 1 Queue 2 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q2_P1               | <b>Port 1 Queue 2 weighted value for max. WFQ weighted value is (q2_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q2_P1              | <b>Port 1 Queue 2 max. shaper rate limit control is enabled</b><br><br>0: Queue 2 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 2 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q2_P1   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 2 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q2_P1 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 2 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021118

MMSCRO\_Q3P1

Max-Min scheduler control register 0 of Queue  
3/Port 1

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q3_P1  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q3_P1 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q3_P1 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q3_P1 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q3_P1               | <b>Port 1 Queue 3 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q3_P1              | <b>Port 1 Queue 3 min. shaper rate limit control is enabled</b><br><br>0: Queue 3 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 3 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q3_P1   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 3 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q3_P1 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 3 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

1502111C

MMSCR1\_Q3P1

Max-Min scheduler control register 1 of Queue  
3/Port 1

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q3_P1  |    |    |    | MAX_WEIGHT_Q3_P1             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q3_P1 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q3_P1 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q3_P1 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q3_P1               | <b>Port 1 Queue 3 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q3_P1               | <b>Port 1 Queue 3 weighted value for max. WFQ weighted value is (q3_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q3_P1              | <b>Port 1 Queue 3 max. shaper rate limit control is enabled</b><br><br>0: Queue 3 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 3 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q3_P1   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 3 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q3_P1 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 3 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021120

MMSCRO\_Q4P1

Max-Min scheduler control register 0 of Queue  
4/Port 1

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q4_P1  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q4_P1 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q4_P1 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q4_P1 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q4_P1               | <b>Port 1 Queue 4 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q4_P1              | <b>Port 1 Queue 4 min. shaper rate limit control is enabled</b><br><br>0: Queue 4 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 4 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q4_P1   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 4 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q4_P1 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 4 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021124

MMSCR1\_Q4P1

Max-Min scheduler control register 1 of Queue  
4/Port 1

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q4_P1  |    |    |    | MAX_WEIGHT_Q4_P1             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q4_P1 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q4_P1 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q4_P1 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q4_P1               | <b>Port 1 Queue 4 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q4_P1               | <b>Port 1 Queue 4 weighted value for max. WFQ weighted value is (q4_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q4_P1              | <b>Port 1 Queue 4 max. shaper rate limit control is enabled</b><br><br>0: Queue 4 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 4 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q4_P1   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 4 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q4_P1 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 4 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021128

MMSCRO\_Q5P1

Max-Min scheduler control register 0 of Queue  
5/Port 1

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q5_P1  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q5_P1 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q5_P1 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q5_P1 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q5_P1               | <b>Port 1 Queue 5 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q5_P1              | <b>Port 1 Queue 5 min. shaper rate limit control is enabled</b><br><br>0: Queue 5 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 5 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q5_P1   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 5 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q5_P1 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 5 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |



1502112C

MMSCR1\_Q5P1

Max-Min scheduler control register 1 of Queue  
5/Port 1

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q5_P1  |    |    |    | MAX_WEIGHT_Q5_P1             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q5_P1 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q5_P1 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q5_P1 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q5_P1               | <b>Port 1 Queue 5 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q5_P1               | <b>Port 1 Queue 5 weighted value for max. WFQ weighted value is (q5_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q5_P1              | <b>Port 1 Queue 5 max. shaper rate limit control is enabled</b><br><br>0: Queue 5 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 5 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q5_P1   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 5 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q5_P1 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 5 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021130

MMSCRO\_Q6P1

Max-Min scheduler control register 0 of Queue  
6/Port 1

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q6_P1  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q6_P1 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q6_P1 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q6_P1 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q6_P1               | <b>Port 1 Queue 6 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q6_P1              | <b>Port 1 Queue 6 min. shaper rate limit control is enabled</b><br><br>0: Queue 6 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 6 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q6_P1   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 6 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q6_P1 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 6 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021134

MMSCR1\_Q6P1

Max-Min scheduler control register 1 of Queue  
6/Port 1

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q6_P1  |    |    |    | MAX_WEIGHT_Q6_P1             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q6_P1 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q6_P1 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q6_P1 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q6_P1               | <b>Port 1 Queue 6 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q6_P1               | <b>Port 1 Queue 6 weighted value for max. WFQ weighted value is (q6_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q6_P1              | <b>Port 1 Queue 6 max. shaper rate limit control is enabled</b><br><br>0: Queue 6 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 6 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q6_P1   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 6 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q6_P1 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 6 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021138

MMSCRO\_Q7P1

Max-Min scheduler control register 0 of Queue  
7/Port 1

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q7_P1  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q7_P1 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q7_P1 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q7_P1 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q7_P1               | <b>Port 1 Queue 7 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q7_P1              | <b>Port 1 Queue 7 min. shaper rate limit control is enabled</b><br><br>0: Queue 7 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 7 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q7_P1   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 7 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q7_P1 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 7 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

1502113C

MMSCR1\_Q7P1

Max-Min scheduler control register 1 of Queue  
7/Port 1

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q7_P1  |    |    |    | MAX_WEIGHT_Q7_P1             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q7_P1 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q7_P1 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q7_P1 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q7_P1               | <b>Port 1 Queue 7 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q7_P1               | <b>Port 1 Queue 7 weighted value for max. WFQ weighted value is (q7_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q7_P1              | <b>Port 1 Queue 7 max. shaper rate limit control is enabled</b><br><br>0: Queue 7 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 7 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q7_P1   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 7 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q7_P1 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 7 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

**15021140 ERLCR\_P1 Egress rate limit control register of Port 1 00000000**

| Bit   | 31                   | 30           | 29 | 28                 | 27                               | 26 | 25 | 24 | 23                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|--------------|----|--------------------|----------------------------------|----|----|----|------------------------------------|----|----|----|----|----|----|----|
| Name  | EGC_RATE_CIR_15_0_P1 |              |    |                    |                                  |    |    |    |                                    |    |    |    |    |    |    |    |
| Type  | RW                   |              |    |                    |                                  |    |    |    |                                    |    |    |    |    |    |    |    |
| Reset | 0                    | 0            | 0  | 0                  | 0                                | 0  | 0  | 0  | 0                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14           | 13 | 12                 | 11                               | 10 | 9  | 8  | 7                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | EG_RATE_LIMIT_EN_P1  | EGC_TB_EN_P1 |    | EGC_RATE_CIR_16_P1 | EG_RATE_LIMIT_EXP_P1_EGC_TB_T_P1 |    |    |    | EG_RATE_LIMIT_MAN_P1_EGC_TB_CBS_P1 |    |    |    |    |    |    |    |
| Type  | RW                   | RW           |    | RW                 | RW                               |    |    |    | RW                                 |    |    |    |    |    |    |    |
| Reset | 0                    | 0            |    | 0                  | 0                                | 0  | 0  | 0  | 0                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                             | Description                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | EGC_RATE_CIR_15_0_P1             | <p>When EGC_TB_EN = 1, total 17 bits EGC_RATE_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps</p> <p><math>EGC\_RATE\_CIR = [Egress\ Rate\ Limit(bps) / 32Kbps]</math></p>                                                                                                                                                                                                          |
| 15     | EG_RATE_LIMIT_EN_P1              | <p><b>Port 1 Egress rate limit control is enabled</b></p> <p>0: Egress rate limit control disable</p> <p>1: Enable</p>                                                                                                                                                                                                                                                                                                              |
| 14     | EGC_TB_EN_P1                     | <p><b>When this bit is disabled, the Egress rate control acts like a leaky bucket principle.</b></p> <p>Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p>                                                                                                      |
| 12     | EGC_RATE_CIR_16_P1               | <b>Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value</b>                                                                                                                                                                                                                                                                                                                                                                  |
| 11:8   | EG_RATE_LIMIT_EXP_P1_EGC_TB_T_P1 | <p><b>Depend on EGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b></p> <p>When EGC_TB_EN = 0, exponent part of Port 1 Egress rate limit control, value range: 0 to 5</p> <p>0: 1Kbps</p> <p>1: 10Kbps</p> <p>2: 100Kbps</p> <p>3: 1Mbps</p> <p>4: 10Mbps</p> <p>5: 100Mbps</p> <p>When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, value range: 0 to 14</p> <p>0: 1/128ms</p> |

| Bit(s) | Name                               | Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
|--------|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                                    | 1: 1/64ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        |                                    | 2: 1/32ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        |                                    | 3: 1/16ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        |                                    | 4: 1/8ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 5: 1/4ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 6: 1/2ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 7: 1ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                                    | 8: 2ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                                    | 9: 4ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                                    | 10: 8ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                                    | 11: 16ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 12: 32ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 13: 64ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 14: 128ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7:0    | EG_RATE_LIMIT_MAN_P1_EGC_TB_CBS_P1 | <p><b>Depend on EGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b></p> <p>When EGC_TB_EN = 0, mantissa part of Port 1 Egress rate limit control, value range: 1 to 255</p> <p>Egress Rate Limit = <math>MAN * 10^{(EXP)} * 1Kbps</math></p> <p>When EGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and</p> <p>Token Bucket = Max ( EGC_RATE_CIR*EGC_TB_T, EGC_TB_CBS*512 )</p> |

15021150

MMSCR2\_Q0P1Max-Min scheduler control register 2 of Queue  
0/Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                            |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_C<br>R_Q0_<br>P1 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                            |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                             |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                             |
| Name  | MIN_RATE_CIR_Q0_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                             |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q0_P1 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |



15021154

MMSCR3\_Q0P1Max-Min scheduler control register 3 of Queue  
0/Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                             |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_R<br>ATE_CI<br>R_Q0_<br>P1 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                             |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                              |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                              |
| Name  | MAX_RATE_CIR_Q0_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                                |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                                |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                              |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q0_P1 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021158

MMSCR2\_Q1P1Max-Min scheduler control register 2 of Queue  
1/Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                            |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_C<br>R_Q1_<br>P1 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                            |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                             |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                             |
| Name  | MIN_RATE_CIR_Q1_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                             |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q1_P1 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502115C

MMSCR3\_Q1P1Max-Min scheduler control register 3 of Queue  
1/Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q1_P1 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q1_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q1_P1 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021160

MMSCR2\_Q2P1Max-Min scheduler control register 2 of Queue  
2/Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_RATE_CIR_Q2_P1 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MIN_RATE_CIR_Q2_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q2_P1 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021164

MMSCR3\_Q2P1Max-Min scheduler control register 3 of Queue  
2/Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q2_P1 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q2_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q2_P1 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021168

MMSCR2\_Q3P1Max-Min scheduler control register 2 of Queue  
3/Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                     |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_CIR_Q3_P1 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                     |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                      |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                      |
| Name  | MIN_RATE_CIR_Q3_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                      |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q3_P1 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502116C

MMSCR3\_Q3P1Max-Min scheduler control register 3 of Queue  
3/Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q3_P1 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q3_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q3_P1 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021170

MMSCR2\_Q4P1Max-Min scheduler control register 2 of Queue  
4/Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                            |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_C<br>R_Q4_<br>P1 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                            |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                             |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                             |
| Name  | MIN_RATE_CIR_Q4_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                             |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q4_P1 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |



15021174

MMSCR3\_Q4P1Max-Min scheduler control register 3 of Queue  
4/Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q4_P1 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q4_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q4_P1 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021178      MMSCR2\_Q5P1      Max-Min scheduler control register 2 of Queue 5/Port 1      00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_RATE_CIR_Q5_P1 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MIN_RATE_CIR_Q5_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q5_P1 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502117C

MMSCR3\_Q5P1Max-Min scheduler control register 3 of Queue  
5/Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q5_P1 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q5_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q5_P1 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021180

MMSCR2\_Q6P1Max-Min scheduler control register 2 of Queue  
6/Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_RATE_CIR_Q6_P1 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MIN_RATE_CIR_Q6_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q6_P1 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021184

MMSCR3\_Q6P1Max-Min scheduler control register 3 of Queue  
6/Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q6_P1 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q6_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q6_P1 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021188

MMSCR2\_Q7P1Max-Min scheduler control register 2 of Queue  
7/Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_RATE_CIR_Q7_P1 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MIN_RATE_CIR_Q7_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q7_P1 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502118C

MMSCR3\_Q7P1

Max-Min scheduler control register 3 of Queue  
7/Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q7_P1 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q7_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q7_P1 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021190 **MMSCR\_P1** Max-Min scheduler control register of Port 1 00000001

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_MAX_TB_EN_P1 |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW               |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 1                |

| Bit(s) | Name             | Description                                                                                                                                                                                                                                                                                                  |
|--------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0      | MIN_MAX_TB_EN_P1 | <p><b>When this bit is disabled, the rate limit acts like a leaky bucket principle.</b></p> <p>Otherwise, the rate limit uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p> |



15021200

MMSCRO\_Q0P2

Max-Min scheduler control register 0 of Queue  
0/Port 2

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q0_P2  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q0_P2 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q0_P2 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q0_P2 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q0_P2               | <b>Port 2 Queue 0 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q0_P2              | <b>Port 2 Queue 0 min. shaper rate limit control is enabled</b><br><br>0: Queue 0 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 0 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q0_P2   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 0 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q0_P2 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 0 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021204

MMSCR1\_Q0P2

Max-Min scheduler control register 1 of Queue  
0/Port 2

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q0_P2  |    |    |    | MAX_WEIGHT_Q0_P2             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q0_P2 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q0_P2 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q0_P2 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q0_P2               | <b>Port 2 Queue 0 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q0_P2               | <b>Port 2 Queue 0 weighted value for max. WFQ weighted value is (q0_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q0_P2              | <b>Port 2 Queue 0 max. shaper rate limit control is enabled</b><br><br>0: Queue 0 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 0 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q0_P2   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 0 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q0_P2 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 0 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021208

MMSCRO\_Q1P2

Max-Min scheduler control register 0 of Queue  
1/Port 2

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q1_P2  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q1_P2 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q1_P2 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q1_P2 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q1_P2               | <b>Port 2 Queue 1 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q1_P2              | <b>Port 2 Queue 1 min. shaper rate limit control is enabled</b><br><br>0: Queue 1 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 1 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q1_P2   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 1 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q1_P2 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 1 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

1502120C

MMSCR1\_Q1P2

Max-Min scheduler control register 1 of Queue  
1/Port 2

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q1_P2  |    |    |    | MAX_WEIGHT_Q1_P2             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q1_P2 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q1_P2 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q1_P2 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q1_P2               | <b>Port 2 Queue 1 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q1_P2               | <b>Port 2 Queue 1 weighted value for max. WFQ weighted value is (q1_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q1_P2              | <b>Port 2 Queue 1 max. shaper rate limit control is enabled</b><br><br>0: Queue 1 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 1 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q1_P2   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 1 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q1_P2 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 1 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021210

MMSCRO\_Q2P2

Max-Min scheduler control register 0 of Queue  
2/Port 2

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q2_P2  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q2_P2 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q2_P2 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q2_P2 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q2_P2               | <b>Port 2 Queue 2 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q2_P2              | <b>Port 2 Queue 2 min. shaper rate limit control is enabled</b><br><br>0: Queue 2 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 2 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q2_P2   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 2 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q2_P2 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 2 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021214

MMSCR1\_Q2P2

Max-Min scheduler control register 1 of Queue  
2/Port 2

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q2_P2  |    |    |    | MAX_WEIGHT_Q2_P2             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q2_P2 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q2_P2 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q2_P2 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q2_P2               | <b>Port 2 Queue 2 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q2_P2               | <b>Port 2 Queue 2 weighted value for max. WFQ weighted value is (q2_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q2_P2              | <b>Port 2 Queue 2 max. shaper rate limit control is enabled</b><br><br>0: Queue 2 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 2 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q2_P2   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 2 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q2_P2 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 2 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021218

MMSCRO\_Q3P2

Max-Min scheduler control register 0 of Queue  
3/Port 2

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q3_P2  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q3_P2 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q3_P2 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q3_P2 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q3_P2               | <b>Port 2 Queue 3 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q3_P2              | <b>Port 2 Queue 3 min. shaper rate limit control is enabled</b><br><br>0: Queue 3 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 3 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q3_P2   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 3 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q3_P2 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 3 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

1502121C

MMSCR1\_Q3P2

Max-Min scheduler control register 1 of Queue  
3/Port 2

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q3_P2  |    |    |    | MAX_WEIGHT_Q3_P2             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q3_P2 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q3_P2 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q3_P2 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q3_P2               | <b>Port 2 Queue 3 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q3_P2               | <b>Port 2 Queue 3 weighted value for max. WFQ weighted value is (q3_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q3_P2              | <b>Port 2 Queue 3 max. shaper rate limit control is enabled</b><br><br>0: Queue 3 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 3 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q3_P2   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 3 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q3_P2 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 3 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |



15021220

MMSCRO\_Q4P2

Max-Min scheduler control register 0 of Queue  
4/Port 2

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q4_P2  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q4_P2 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q4_P2 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q4_P2 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q4_P2               | <b>Port 2 Queue 4 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q4_P2              | <b>Port 2 Queue 4 min. shaper rate limit control is enabled</b><br><br>0: Queue 4 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 4 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q4_P2   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 4 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q4_P2 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 4 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021224

MMSCR1\_Q4P2

Max-Min scheduler control register 1 of Queue  
4/Port 2

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q4_P2  |    |    |    | MAX_WEIGHT_Q4_P2             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q4_P2 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q4_P2 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q4_P2 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q4_P2               | <b>Port 2 Queue 4 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q4_P2               | <b>Port 2 Queue 4 weighted value for max. WFQ weighted value is (q4_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q4_P2              | <b>Port 2 Queue 4 max. shaper rate limit control is enabled</b><br><br>0: Queue 4 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 4 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q4_P2   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 4 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q4_P2 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 4 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021228

MMSCRO\_Q5P2

Max-Min scheduler control register 0 of Queue  
5/Port 2

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q5_P2  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q5_P2 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q5_P2 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q5_P2 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q5_P2               | <b>Port 2 Queue 5 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q5_P2              | <b>Port 2 Queue 5 min. shaper rate limit control is enabled</b><br><br>0: Queue 5 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 5 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q5_P2   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 5 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q5_P2 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 5 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

1502122C

MMSCR1\_Q5P2

Max-Min scheduler control register 1 of Queue  
5/Port 2

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q5_P2  |    |    |    | MAX_WEIGHT_Q5_P2             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q5_P2 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q5_P2 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q5_P2 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q5_P2               | <b>Port 2 Queue 5 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q5_P2               | <b>Port 2 Queue 5 weighted value for max. WFQ weighted value is (q5_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q5_P2              | <b>Port 2 Queue 5 max. shaper rate limit control is enabled</b><br><br>0: Queue 5 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 5 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q5_P2   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 5 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q5_P2 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 5 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021230

MMSCRO\_Q6P2

Max-Min scheduler control register 0 of Queue  
6/Port 2

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q6_P2  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q6_P2 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q6_P2 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q6_P2 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q6_P2               | <b>Port 2 Queue 6 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q6_P2              | <b>Port 2 Queue 6 min. shaper rate limit control is enabled</b><br><br>0: Queue 6 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 6 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q6_P2   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 6 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q6_P2 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 6 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021234

MMSCR1\_Q6P2

Max-Min scheduler control register 1 of Queue  
6/Port 2

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q6_P2  |    |    |    | MAX_WEIGHT_Q6_P2             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q6_P2 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q6_P2 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q6_P2 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q6_P2               | <b>Port 2 Queue 6 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q6_P2               | <b>Port 2 Queue 6 weighted value for max. WFQ weighted value is (q6_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q6_P2              | <b>Port 2 Queue 6 max. shaper rate limit control is enabled</b><br><br>0: Queue 6 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 6 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q6_P2   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 6 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q6_P2 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 6 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021238

MMSCRO\_Q7P2

Max-Min scheduler control register 0 of Queue  
7/Port 2

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q7_P2  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q7_P2 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q7_P2 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q7_P2 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q7_P2               | <b>Port 2 Queue 7 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q7_P2              | <b>Port 2 Queue 7 min. shaper rate limit control is enabled</b><br><br>0: Queue 7 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 7 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q7_P2   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 7 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q7_P2 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 7 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

1502123C

MMSCR1\_Q7P2

Max-Min scheduler control register 1 of Queue  
7/Port 2

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q7_P2  |    |    |    | MAX_WEIGHT_Q7_P2             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q7_P2 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q7_P2 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q7_P2 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q7_P2               | <b>Port 2 Queue 7 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q7_P2               | <b>Port 2 Queue 7 weighted value for max. WFQ weighted value is (q7_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q7_P2              | <b>Port 2 Queue 7 max. shaper rate limit control is enabled</b><br><br>0: Queue 7 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 7 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q7_P2   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 7 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q7_P2 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 7 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |



**15021240 ERLCR\_P2 Egress rate limit control register of Port 2 00000000**

| Bit   | 31                   | 30           | 29 | 28                 | 27                               | 26 | 25 | 24 | 23                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|--------------|----|--------------------|----------------------------------|----|----|----|------------------------------------|----|----|----|----|----|----|----|
| Name  | EGC_RATE_CIR_15_0_P2 |              |    |                    |                                  |    |    |    |                                    |    |    |    |    |    |    |    |
| Type  | RW                   |              |    |                    |                                  |    |    |    |                                    |    |    |    |    |    |    |    |
| Reset | 0                    | 0            | 0  | 0                  | 0                                | 0  | 0  | 0  | 0                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14           | 13 | 12                 | 11                               | 10 | 9  | 8  | 7                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | EG_RATE_LIMIT_EN_P2  | EGC_TB_EN_P2 |    | EGC_RATE_CIR_16_P2 | EG_RATE_LIMIT_EXP_P2_EGC_TB_T_P2 |    |    |    | EG_RATE_LIMIT_MAN_P2_EGC_TB_CBS_P2 |    |    |    |    |    |    |    |
| Type  | RW                   | RW           |    | RW                 | RW                               |    |    |    | RW                                 |    |    |    |    |    |    |    |
| Reset | 0                    | 0            |    | 0                  | 0                                | 0  | 0  | 0  | 0                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                             | Description                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | EGC_RATE_CIR_15_0_P2             | <p>When EGC_TB_EN = 1, total 17 bits EGC_RATE_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps</p> <p><math>EGC\_RATE\_CIR = [Egress\ Rate\ Limit(bps) / 32Kbps]</math></p>                                                                                                                                                                                                          |
| 15     | EG_RATE_LIMIT_EN_P2              | <p><b>Port 2 Egress rate limit control is enabled</b></p> <p>0: Egress rate limit control disable</p> <p>1: Enable</p>                                                                                                                                                                                                                                                                                                              |
| 14     | EGC_TB_EN_P2                     | <p><b>When this bit is disabled, the Egress rate control acts like a leaky bucket principle.</b></p> <p>Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p>                                                                                                      |
| 12     | EGC_RATE_CIR_16_P2               | <b>Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value</b>                                                                                                                                                                                                                                                                                                                                                                  |
| 11:8   | EG_RATE_LIMIT_EXP_P2_EGC_TB_T_P2 | <p><b>Depend on EGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b></p> <p>When EGC_TB_EN = 0, exponent part of Port 2 Egress rate limit control, value range: 0 to 5</p> <p>0: 1Kbps</p> <p>1: 10Kbps</p> <p>2: 100Kbps</p> <p>3: 1Mbps</p> <p>4: 10Mbps</p> <p>5: 100Mbps</p> <p>When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, value range: 0 to 14</p> <p>0: 1/128ms</p> |

| Bit(s) | Name                               | Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
|--------|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                                    | 1: 1/64ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        |                                    | 2: 1/32ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        |                                    | 3: 1/16ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        |                                    | 4: 1/8ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 5: 1/4ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 6: 1/2ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 7: 1ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                                    | 8: 2ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                                    | 9: 4ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                                    | 10: 8ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                                    | 11: 16ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 12: 32ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 13: 64ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 14: 128ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7:0    | EG_RATE_LIMIT_MAN_P2_EGC_TB_CBS_P2 | <p><b>Depend on EGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b></p> <p>When EGC_TB_EN = 0, mantissa part of Port 2 Egress rate limit control, value range: 1 to 255</p> <p>Egress Rate Limit = <math>MAN * 10^{(EXP)} * 1Kbps</math></p> <p>When EGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and</p> <p>Token Bucket = Max ( EGC_RATE_CIR*EGC_TB_T, EGC_TB_CBS*512 )</p> |

15021250

MMSCR2\_Q0P2Max-Min scheduler control register 2 of Queue  
0/Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                            |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_C<br>R_Q0_<br>P2 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                            |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                             |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                             |
| Name  | MIN_RATE_CIR_Q0_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                             |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q0_P2 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021254      MMSCR3\_Q0P2      Max-Min scheduler control register 3 of Queue 0/Port 2      00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q0_P2 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q0_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q0_P2 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021258

MMSCR2\_Q1P2Max-Min scheduler control register 2 of Queue  
1/Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_RATE_CIR_Q1_P2 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MIN_RATE_CIR_Q1_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q1_P2 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502125C

MMSCR3\_Q1P2

Max-Min scheduler control register 3 of Queue  
1/Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q1_P2 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q1_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q1_P2 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021260

MMSCR2\_Q2P2Max-Min scheduler control register 2 of Queue  
2/Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                     |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_CIR_Q2_P2 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                     |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                      |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                      |
| Name  | MIN_RATE_CIR_Q2_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                      |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q2_P2 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021264

MMSCR3\_Q2P2Max-Min scheduler control register 3 of Queue  
2/Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q2_P2 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q2_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q2_P2 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |



15021268

MMSCR2\_Q3P2Max-Min scheduler control register 2 of Queue  
3/Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                     |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_CIR_Q3_P2 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                     |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                      |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                      |
| Name  | MIN_RATE_CIR_Q3_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                      |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q3_P2 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502126C

MMSCR3\_Q3P2

Max-Min scheduler control register 3 of Queue  
3/Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q3_P2 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q3_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q3_P2 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021270

MMSCR2\_Q4P2Max-Min scheduler control register 2 of Queue  
4/Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                            |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_C<br>R_Q4_<br>P2 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                            |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                             |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                             |
| Name  | MIN_RATE_CIR_Q4_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                             |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q4_P2 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021274

MMSCR3\_Q4P2Max-Min scheduler control register 3 of Queue  
4/Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q4_P2 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q4_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q4_P2 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021278

MMSCR2\_Q5P2Max-Min scheduler control register 2 of Queue  
5/Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_RATE_CIR_Q5_P2 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MIN_RATE_CIR_Q5_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q5_P2 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502127C

MMSCR3\_Q5P2

Max-Min scheduler control register 3 of Queue  
5/Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q5_P2 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q5_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q5_P2 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021280

MMSCR2\_Q6P2Max-Min scheduler control register 2 of Queue  
6/Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_RATE_CIR_Q6_P2 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MIN_RATE_CIR_Q6_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q6_P2 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021284

MMSCR3\_Q6P2Max-Min scheduler control register 3 of Queue  
6/Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q6_P2 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q6_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q6_P2 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |



15021288

MMSCR2\_Q7P2Max-Min scheduler control register 2 of Queue  
7/Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_RATE_CIR_Q7_P2 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MIN_RATE_CIR_Q7_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q7_P2 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502128C

MMSCR3\_Q7P2

Max-Min scheduler control register 3 of Queue  
7/Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q7_P2 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q7_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q7_P2 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021290      **MMSCR\_P2**      Max-Min scheduler control register of Port 2      00000001

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                   |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------------------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                      |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                      |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                      |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                    |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_<br>MAX_TB_EN_P2 |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                   |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 1                    |

| Bit(s) | Name             | Description                                                                                                                                                                                                                                                                                                  |
|--------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0      | MIN_MAX_TB_EN_P2 | <p><b>When this bit is disabled, the rate limit acts like a leaky bucket principle.</b></p> <p>Otherwise, the rate limit uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p> |

15021300

MMSCRO\_Q0P3

Max-Min scheduler control register 0 of Queue  
0/Port 3

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q0_P3  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q0_P3 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q0_P3 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q0_P3 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q0_P3               | <b>Port 3 Queue 0 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q0_P3              | <b>Port 3 Queue 0 min. shaper rate limit control is enabled</b><br><br>0: Queue 0 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 0 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q0_P3   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 0 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q0_P3 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 0 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021304

MMSCR1\_Q0P3

Max-Min scheduler control register 1 of Queue  
0/Port 3

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q0_P3  |    |    |    | MAX_WEIGHT_Q0_P3             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q0_P3 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q0_P3 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q0_P3 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q0_P3               | <b>Port 3 Queue 0 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q0_P3               | <b>Port 3 Queue 0 weighted value for max. WFQ weighted value is (q0_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q0_P3              | <b>Port 3 Queue 0 max. shaper rate limit control is enabled</b><br><br>0: Queue 0 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 0 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q0_P3   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 0 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q0_P3 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 0 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021308

MMSCRO\_Q1P3

Max-Min scheduler control register 0 of Queue  
1/Port 3

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q1_P3  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q1_P3 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q1_P3 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q1_P3 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q1_P3               | <b>Port 3 Queue 1 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q1_P3              | <b>Port 3 Queue 1 min. shaper rate limit control is enabled</b><br><br>0: Queue 1 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 1 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q1_P3   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 1 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q1_P3 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 1 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

1502130C

MMSCR1\_Q1P3

Max-Min scheduler control register 1 of Queue  
1/Port 3

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q1_P3  |    |    |    | MAX_WEIGHT_Q1_P3             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q1_P3 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q1_P3 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q1_P3 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q1_P3               | <b>Port 3 Queue 1 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q1_P3               | <b>Port 3 Queue 1 weighted value for max. WFQ weighted value is (q1_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q1_P3              | <b>Port 3 Queue 1 max. shaper rate limit control is enabled</b><br><br>0: Queue 1 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 1 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q1_P3   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 1 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q1_P3 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 1 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021310

MMSCRO\_Q2P3

Max-Min scheduler control register 0 of Queue  
2/Port 3

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q2_P3  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q2_P3 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q2_P3 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q2_P3 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q2_P3               | <b>Port 3 Queue 2 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q2_P3              | <b>Port 3 Queue 2 min. shaper rate limit control is enabled</b><br><br>0: Queue 2 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 2 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q2_P3   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 2 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q2_P3 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 2 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |



15021314

MMSCR1\_Q2P3

Max-Min scheduler control register 1 of Queue  
2/Port 3

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q2_P3  |    |    |    | MAX_WEIGHT_Q2_P3             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q2_P3 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q2_P3 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q2_P3 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q2_P3               | <b>Port 3 Queue 2 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q2_P3               | <b>Port 3 Queue 2 weighted value for max. WFQ weighted value is (q2_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q2_P3              | <b>Port 3 Queue 2 max. shaper rate limit control is enabled</b><br><br>0: Queue 2 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 2 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q2_P3   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 2 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q2_P3 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 2 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021318

MMSCRO\_Q3P3

Max-Min scheduler control register 0 of Queue  
3/Port 3

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q3_P3  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q3_P3 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q3_P3 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q3_P3 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q3_P3               | <b>Port 3 Queue 3 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q3_P3              | <b>Port 3 Queue 3 min. shaper rate limit control is enabled</b><br><br>0: Queue 3 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 3 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q3_P3   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 3 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q3_P3 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 3 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

1502131C

MMSCR1\_Q3P3

Max-Min scheduler control register 1 of Queue  
3/Port 3

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q3_P3  |    |    |    | MAX_WEIGHT_Q3_P3             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q3_P3 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q3_P3 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q3_P3 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q3_P3               | <b>Port 3 Queue 3 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q3_P3               | <b>Port 3 Queue 3 weighted value for max. WFQ weighted value is (q3_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q3_P3              | <b>Port 3 Queue 3 max. shaper rate limit control is enabled</b><br><br>0: Queue 3 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 3 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q3_P3   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 3 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q3_P3 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 3 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021320

MMSCRO\_Q4P3

Max-Min scheduler control register 0 of Queue  
4/Port 3

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q4_P3  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q4_P3 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q4_P3 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q4_P3 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q4_P3               | <b>Port 3 Queue 4 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q4_P3              | <b>Port 3 Queue 4 min. shaper rate limit control is enabled</b><br><br>0: Queue 4 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 4 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q4_P3   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 4 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q4_P3 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 4 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021324

MMSCR1\_Q4P3

Max-Min scheduler control register 1 of Queue  
4/Port 3

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q4_P3  |    |    |    | MAX_WEIGHT_Q4_P3             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q4_P3 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q4_P3 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q4_P3 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q4_P3               | <b>Port 3 Queue 4 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q4_P3               | <b>Port 3 Queue 4 weighted value for max. WFQ weighted value is (q4_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q4_P3              | <b>Port 3 Queue 4 max. shaper rate limit control is enabled</b><br><br>0: Queue 4 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 4 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q4_P3   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 4 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q4_P3 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 4 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021328

MMSCRO\_Q5P3

Max-Min scheduler control register 0 of Queue  
5/Port 3

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q5_P3  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q5_P3 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q5_P3 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q5_P3 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q5_P3               | <b>Port 3 Queue 5 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q5_P3              | <b>Port 3 Queue 5 min. shaper rate limit control is enabled</b><br><br>0: Queue 5 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 5 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q5_P3   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 5 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q5_P3 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 5 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

1502132C

MMSCR1\_Q5P3

Max-Min scheduler control register 1 of Queue  
5/Port 3

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q5_P3  |    |    |    | MAX_WEIGHT_Q5_P3             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q5_P3 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q5_P3 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q5_P3 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q5_P3               | <b>Port 3 Queue 5 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q5_P3               | <b>Port 3 Queue 5 weighted value for max. WFQ weighted value is (q5_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q5_P3              | <b>Port 3 Queue 5 max. shaper rate limit control is enabled</b><br><br>0: Queue 5 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 5 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q5_P3   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 5 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q5_P3 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 5 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021330

MMSCRO\_Q6P3

Max-Min scheduler control register 0 of Queue  
6/Port 3

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q6_P3  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q6_P3 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q6_P3 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q6_P3 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q6_P3               | <b>Port 3 Queue 6 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q6_P3              | <b>Port 3 Queue 6 min. shaper rate limit control is enabled</b><br><br>0: Queue 6 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 6 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q6_P3   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 6 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q6_P3 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 6 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |



15021334

MMSCR1\_Q6P3

Max-Min scheduler control register 1 of Queue  
6/Port 3

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q6_P3  |    |    |    | MAX_WEIGHT_Q6_P3             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q6_P3 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q6_P3 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q6_P3 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q6_P3               | <b>Port 3 Queue 6 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q6_P3               | <b>Port 3 Queue 6 weighted value for max. WFQ weighted value is (q6_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q6_P3              | <b>Port 3 Queue 6 max. shaper rate limit control is enabled</b><br><br>0: Queue 6 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 6 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q6_P3   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 6 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q6_P3 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 6 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021338

MMSCRO\_Q7P3

Max-Min scheduler control register 0 of Queue  
7/Port 3

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q7_P3  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q7_P3 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q7_P3 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q7_P3 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q7_P3               | <b>Port 3 Queue 7 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q7_P3              | <b>Port 3 Queue 7 min. shaper rate limit control is enabled</b><br><br>0: Queue 7 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 7 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q7_P3   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 7 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q7_P3 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 7 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

1502133C

MMSCR1\_Q7P3

Max-Min scheduler control register 1 of Queue  
7/Port 3

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q7_P3  |    |    |    | MAX_WEIGHT_Q7_P3             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q7_P3 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q7_P3 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q7_P3 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q7_P3               | <b>Port 3 Queue 7 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q7_P3               | <b>Port 3 Queue 7 weighted value for max. WFQ weighted value is (q7_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q7_P3              | <b>Port 3 Queue 7 max. shaper rate limit control is enabled</b><br><br>0: Queue 7 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 7 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q7_P3   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 7 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q7_P3 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 7 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

**15021340 ERLCR\_P3 Egress rate limit control register of Port 3 00000000**

| Bit          | 31                   | 30           | 29 | 28                 | 27                               | 26 | 25 | 24 | 23                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------------|--------------|----|--------------------|----------------------------------|----|----|----|------------------------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | EGC_RATE_CIR_15_0_P3 |              |    |                    |                                  |    |    |    |                                    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                   |              |    |                    |                                  |    |    |    |                                    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0            | 0  | 0                  | 0                                | 0  | 0  | 0  | 0                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                   | 14           | 13 | 12                 | 11                               | 10 | 9  | 8  | 7                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | EG_RATE_LIMIT_EN_P3  | EGC_TB_EN_P3 |    | EGC_RATE_CIR_16_P3 | EG_RATE_LIMIT_EXP_P3_EGC_TB_T_P3 |    |    |    | EG_RATE_LIMIT_MAN_P3_EGC_TB_CBS_P3 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                   | RW           |    | RW                 | RW                               |    |    |    | RW                                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0            |    | 0                  | 0                                | 0  | 0  | 0  | 0                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                             | Description                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | EGC_RATE_CIR_15_0_P3             | <p>When EGC_TB_EN = 1, total 17 bits EGC_RATE_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps</p> <p><math>EGC\_RATE\_CIR = [Egress\ Rate\ Limit(bps) / 32Kbps]</math></p>                                                                                                                                                                                                          |
| 15     | EG_RATE_LIMIT_EN_P3              | <p><b>Port 3 Egress rate limit control is enabled</b></p> <p>0: Egress rate limit control disable</p> <p>1: Enable</p>                                                                                                                                                                                                                                                                                                              |
| 14     | EGC_TB_EN_P3                     | <p><b>When this bit is disabled, the Egress rate control acts like a leaky bucket principle.</b></p> <p>Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p>                                                                                                      |
| 12     | EGC_RATE_CIR_16_P3               | <b>Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value</b>                                                                                                                                                                                                                                                                                                                                                                  |
| 11:8   | EG_RATE_LIMIT_EXP_P3_EGC_TB_T_P3 | <p><b>Depend on EGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b></p> <p>When EGC_TB_EN = 0, exponent part of Port 3 Egress rate limit control, value range: 0 to 5</p> <p>0: 1Kbps</p> <p>1: 10Kbps</p> <p>2: 100Kbps</p> <p>3: 1Mbps</p> <p>4: 10Mbps</p> <p>5: 100Mbps</p> <p>When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, value range: 0 to 14</p> <p>0: 1/128ms</p> |

| Bit(s) | Name                               | Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
|--------|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                                    | 1: 1/64ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        |                                    | 2: 1/32ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        |                                    | 3: 1/16ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        |                                    | 4: 1/8ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 5: 1/4ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 6: 1/2ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 7: 1ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                                    | 8: 2ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                                    | 9: 4ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                                    | 10: 8ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                                    | 11: 16ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 12: 32ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 13: 64ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 14: 128ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7:0    | EG_RATE_LIMIT_MAN_P3_EGC_TB_CBS_P3 | <p><b>Depend on EGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b></p> <p>When EGC_TB_EN = 0, mantissa part of Port 3 Egress rate limit control, value range: 1 to 255</p> <p>Egress Rate Limit = <math>MAN * 10^{(EXP)} * 1Kbps</math></p> <p>When EGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and</p> <p>Token Bucket = Max ( EGC_RATE_CIR*EGC_TB_T, EGC_TB_CBS*512 )</p> |

15021350

MMSCR2\_Q0P3Max-Min scheduler control register 2 of Queue  
0/Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                            |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_C<br>R_Q0_<br>P3 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                            |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                             |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                             |
| Name  | MIN_RATE_CIR_Q0_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                             |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q0_P3 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021354

MMSCR3\_Q0P3Max-Min scheduler control register 3 of Queue  
0/Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q0_P3 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q0_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q0_P3 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021358

MMSCR2\_Q1P3Max-Min scheduler control register 2 of Queue  
1/Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                     |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_CIR_Q1_P3 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                     |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                      |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                      |
| Name  | MIN_RATE_CIR_Q1_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                      |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q1_P3 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |



1502135C

MMSCR3\_Q1P3Max-Min scheduler control register 3 of Queue  
1/Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q1_P3 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q1_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q1_P3 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021360

MMSCR2\_Q2P3Max-Min scheduler control register 2 of Queue  
2/Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                     |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_CIR_Q2_P3 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                     |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                      |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                      |
| Name  | MIN_RATE_CIR_Q2_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                      |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q2_P3 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021364

MMSCR3\_Q2P3Max-Min scheduler control register 3 of Queue  
2/Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q2_P3 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q2_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q2_P3 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021368

MMSCR2\_Q3P3Max-Min scheduler control register 2 of Queue  
3/Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                     |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_CIR_Q3_P3 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                     |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                      |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                      |
| Name  | MIN_RATE_CIR_Q3_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                      |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q3_P3 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502136C

MMSCR3\_Q3P3Max-Min scheduler control register 3 of Queue  
3/Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q3_P3 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q3_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q3_P3 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021370

MMSCR2\_Q4P3Max-Min scheduler control register 2 of Queue  
4/Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                     |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_CIR_Q4_P3 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                     |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                      |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                      |
| Name  | MIN_RATE_CIR_Q4_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                      |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q4_P3 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021374

MMSCR3\_Q4P3Max-Min scheduler control register 3 of Queue  
4/Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q4_P3 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q4_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q4_P3 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021378

MMSCR2\_Q5P3Max-Min scheduler control register 2 of Queue  
5/Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                     |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_CIR_Q5_P3 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                     |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                      |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                      |
| Name  | MIN_RATE_CIR_Q5_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                      |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q5_P3 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |



1502137C

MMSCR3\_Q5P3Max-Min scheduler control register 3 of Queue  
5/Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q5_P3 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q5_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q5_P3 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021380

MMSCR2\_Q6P3Max-Min scheduler control register 2 of Queue  
6/Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                     |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_CIR_Q6_P3 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                     |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                      |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                      |
| Name  | MIN_RATE_CIR_Q6_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                      |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q6_P3 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021384

MMSCR3\_Q6P3Max-Min scheduler control register 3 of Queue  
6/Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q6_P3 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q6_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q6_P3 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021388

MMSCR2\_Q7P3Max-Min scheduler control register 2 of Queue  
7/Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                            |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_C<br>R_Q7_<br>P3 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                            |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                             |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                             |
| Name  | MIN_RATE_CIR_Q7_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                             |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q7_P3 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502138C

MMSCR3\_Q7P3

Max-Min scheduler control register 3 of Queue  
7/Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q7_P3 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q7_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q7_P3 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021390 **MMSCR\_P3** Max-Min scheduler control register of Port 3 00000001

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_MAX_TB_EN_P3 |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW               |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 1                |

| Bit(s) | Name             | Description                                                                                                                                                                                                                                                                                                  |
|--------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0      | MIN_MAX_TB_EN_P3 | <p><b>When this bit is disabled, the rate limit acts like a leaky bucket principle.</b></p> <p>Otherwise, the rate limit uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p> |

15021600

MMSCRO\_Q0P6

Max-Min scheduler control register 0 of Queue  
0/Port 6

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q0_P6  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q0_P6 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q0_P6 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q0_P6 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q0_P6               | <b>Port 6 Queue 0 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q0_P6              | <b>Port 6 Queue 0 min. shaper rate limit control is enabled</b><br><br>0: Queue 0 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 0 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q0_P6   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 0 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q0_P6 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 0 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021604

MMSCR1\_Q0P6

Max-Min scheduler control register 1 of Queue  
0/Port 6

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q0_P6  |    |    |    | MAX_WEIGHT_Q0_P6             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q0_P6 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q0_P6 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q0_P6 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q0_P6               | <b>Port 6 Queue 0 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q0_P6               | <b>Port 6 Queue 0 weighted value for max. WFQ weighted value is (q0_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q0_P6              | <b>Port 6 Queue 0 max. shaper rate limit control is enabled</b><br><br>0: Queue 0 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 0 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q0_P6   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 0 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q0_P6 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 0 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |



15021608

MMSCRO\_Q1P6

Max-Min scheduler control register 0 of Queue  
1/Port 6

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q1_P6  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q1_P6 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q1_P6 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q1_P6 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q1_P6               | <b>Port 6 Queue 1 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q1_P6              | <b>Port 6 Queue 1 min. shaper rate limit control is enabled</b><br><br>0: Queue 1 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 1 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q1_P6   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 1 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q1_P6 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 1 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

1502160C

MMSCR1\_Q1P6

Max-Min scheduler control register 1 of Queue  
1/Port 6

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q1_P6  |    |    |    | MAX_WEIGHT_Q1_P6             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q1_P6 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q1_P6 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q1_P6 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q1_P6               | <b>Port 6 Queue 1 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q1_P6               | <b>Port 6 Queue 1 weighted value for max. WFQ weighted value is (q1_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q1_P6              | <b>Port 6 Queue 1 max. shaper rate limit control is enabled</b><br><br>0: Queue 1 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 1 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q1_P6   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 1 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q1_P6 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 1 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021610

MMSCRO\_Q2P6

Max-Min scheduler control register 0 of Queue  
2/Port 6

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q2_P6  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q2_P6 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q2_P6 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q2_P6 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q2_P6               | <b>Port 6 Queue 2 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q2_P6              | <b>Port 6 Queue 2 min. shaper rate limit control is enabled</b><br><br>0: Queue 2 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 2 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q2_P6   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 2 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q2_P6 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 2 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021614

MMSCR1\_Q2P6

Max-Min scheduler control register 1 of Queue  
2/Port 6

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q2_P6  |    |    |    | MAX_WEIGHT_Q2_P6             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q2_P6 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q2_P6 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q2_P6 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q2_P6               | <b>Port 6 Queue 2 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q2_P6               | <b>Port 6 Queue 2 weighted value for max. WFQ weighted value is (q2_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q2_P6              | <b>Port 6 Queue 2 max. shaper rate limit control is enabled</b><br><br>0: Queue 2 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 2 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q2_P6   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 2 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q2_P6 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 2 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021618

MMSCRO\_Q3P6

Max-Min scheduler control register 0 of Queue  
3/Port 6

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q3_P6  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q3_P6 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q3_P6 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q3_P6 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q3_P6               | <b>Port 6 Queue 3 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q3_P6              | <b>Port 6 Queue 3 min. shaper rate limit control is enabled</b><br><br>0: Queue 3 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 3 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q3_P6   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 3 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q3_P6 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 3 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

1502161C

MMSCR1\_Q3P6

Max-Min scheduler control register 1 of Queue  
3/Port 6

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q3_P6  |    |    |    | MAX_WEIGHT_Q3_P6             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q3_P6 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q3_P6 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q3_P6 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q3_P6               | <b>Port 6 Queue 3 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q3_P6               | <b>Port 6 Queue 3 weighted value for max. WFQ weighted value is (q3_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q3_P6              | <b>Port 6 Queue 3 max. shaper rate limit control is enabled</b><br><br>0: Queue 3 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 3 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q3_P6   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 3 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q3_P6 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 3 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021620

MMSCRO\_Q4P6

Max-Min scheduler control register 0 of Queue  
4/Port 6

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q4_P6  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q4_P6 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q4_P6 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q4_P6 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q4_P6               | <b>Port 6 Queue 4 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q4_P6              | <b>Port 6 Queue 4 min. shaper rate limit control is enabled</b><br><br>0: Queue 4 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 4 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q4_P6   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 4 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q4_P6 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 4 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021624

MMSCR1\_Q4P6

Max-Min scheduler control register 1 of Queue  
4/Port 6

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q4_P6  |    |    |    | MAX_WEIGHT_Q4_P6             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q4_P6 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q4_P6 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q4_P6 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q4_P6               | <b>Port 6 Queue 4 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q4_P6               | <b>Port 6 Queue 4 weighted value for max. WFQ weighted value is (q4_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q4_P6              | <b>Port 6 Queue 4 max. shaper rate limit control is enabled</b><br><br>0: Queue 4 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 4 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q4_P6   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 4 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q4_P6 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 4 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |



15021628

MMSCRO\_Q5P6

Max-Min scheduler control register 0 of Queue  
5/Port 6

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q5_P6  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q5_P6 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q5_P6 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q5_P6 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q5_P6               | <b>Port 6 Queue 5 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q5_P6              | <b>Port 6 Queue 5 min. shaper rate limit control is enabled</b><br><br>0: Queue 5 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 5 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q5_P6   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 5 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q5_P6 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 5 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

1502162C

MMSCR1\_Q5P6

Max-Min scheduler control register 1 of Queue  
5/Port 6

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q5_P6  |    |    |    | MAX_WEIGHT_Q5_P6             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q5_P6 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q5_P6 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q5_P6 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q5_P6               | <b>Port 6 Queue 5 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q5_P6               | <b>Port 6 Queue 5 weighted value for max. WFQ weighted value is (q5_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q5_P6              | <b>Port 6 Queue 5 max. shaper rate limit control is enabled</b><br><br>0: Queue 5 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 5 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q5_P6   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 5 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q5_P6 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 5 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021630

MMSCRO\_Q6P6

Max-Min scheduler control register 0 of Queue  
6/Port 6

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q6_P6  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q6_P6 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q6_P6 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q6_P6 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q6_P6               | <b>Port 6 Queue 6 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q6_P6              | <b>Port 6 Queue 6 min. shaper rate limit control is enabled</b><br><br>0: Queue 6 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 6 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q6_P6   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 6 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q6_P6 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 6 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021634

MMSCR1\_Q6P6

Max-Min scheduler control register 1 of Queue  
6/Port 6

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q6_P6  |    |    |    | MAX_WEIGHT_Q6_P6             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q6_P6 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q6_P6 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q6_P6 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q6_P6               | <b>Port 6 Queue 6 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q6_P6               | <b>Port 6 Queue 6 weighted value for max. WFQ weighted value is (q6_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q6_P6              | <b>Port 6 Queue 6 max. shaper rate limit control is enabled</b><br><br>0: Queue 6 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 6 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q6_P6   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 6 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q6_P6 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 6 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

15021638

MMSCRO\_Q7P6

Max-Min scheduler control register 0 of Queue  
7/Port 6

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MIN_SP_WRR_Q7_P6  |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    |                              |    |    |    |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MIN_RATE_EN_Q7_P6 |    |    |    | MIN_RATE_CTRL_EXP_TB_T_Q7_P6 |    |    |    | MIN_RATE_CTRL_MAN_TB_CBS_Q7_P6 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIN_SP_WRR_Q7_P6               | <b>Port 6 Queue 7 min. traffic arbitration scheme</b><br><br>0: Round-Robin (RR)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                           |
| 15     | MIN_RATE_EN_Q7_P6              | <b>Port 6 Queue 7 min. shaper rate limit control is enabled</b><br><br>0: Queue 7 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 7 min. shaper rate limit control is enabled                                                                         |
| 11:8   | MIN_RATE_CTRL_EXP_TB_T_Q7_P6   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 7 min. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MIN_RATE_CTRL_MAN_TB_CBS_Q7_P6 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 7 min. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

1502163C

MMSCR1\_Q7P6

Max-Min scheduler control register 1 of Queue  
7/Port 6

00000000

| Bit   | 31                | 30 | 29 | 28 | 27                           | 26 | 25 | 24 | 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|------------------------------|----|----|----|--------------------------------|----|----|----|----|----|----|----|
| Name  | MAX_SP_WFQ_Q7_P6  |    |    |    | MAX_WEIGHT_Q7_P6             |    |    |    |                                |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    |                                |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  |                                |    |    |    |    |    |    |    |
| Bit   | 15                | 14 | 13 | 12 | 11                           | 10 | 9  | 8  | 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_RATE_EN_Q7_P6 |    |    |    | MAX_RATE_CTRL_EXP_TB_T_Q7_P6 |    |    |    | MAX_RATE_CTRL_MAN_TB_CBS_Q7_P6 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    | RW                           |    |    |    | RW                             |    |    |    |    |    |    |    |
| Reset | 0                 |    |    |    | 0                            | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                           | Description                                                                                                                                                                                                                                                                                                               |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MAX_SP_WFQ_Q7_P6               | <b>Port 6 Queue 7 max. traffic arbitration scheme</b><br><br>0: Weighted Fair Queuing (WFQ)<br><br>1: Strict Priority (SP)                                                                                                                                                                                                |
| 27:24  | MAX_WEIGHT_Q7_P6               | <b>Port 6 Queue 7 weighted value for max. WFQ weighted value is (q7_max_weight+1'b1)</b>                                                                                                                                                                                                                                  |
| 15     | MAX_RATE_EN_Q7_P6              | <b>Port 6 Queue 7 max. shaper rate limit control is enabled</b><br><br>0: Queue 7 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)<br><br>1: Queue 7 max. shaper rate limit control is enabled                                                                         |
| 11:8   | MAX_RATE_CTRL_EXP_TB_T_Q7_P6   | <b>Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 7 max. shaper rate limit control, value range: 0 to 5<br><br>When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0 to 14 |
| 7:0    | MAX_RATE_CTRL_MAN_TB_CBS_Q7_P6 | <b>Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b><br><br>When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 7 max. shaper rate limit control, value range: 1 to 255<br><br>When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping       |

**15021640 ERLCR\_P6 Egress rate limit control register of Port 6 00000000**

| Bit          | 31                   | 30           | 29 | 28                 | 27                               | 26 | 25 | 24 | 23                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------------|--------------|----|--------------------|----------------------------------|----|----|----|------------------------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | EGC_RATE_CIR_15_0_P6 |              |    |                    |                                  |    |    |    |                                    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                   |              |    |                    |                                  |    |    |    |                                    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0            | 0  | 0                  | 0                                | 0  | 0  | 0  | 0                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                   | 14           | 13 | 12                 | 11                               | 10 | 9  | 8  | 7                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | EG_RATE_LIMIT_EN_P6  | EGC_TB_EN_P6 |    | EGC_RATE_CIR_16_P6 | EG_RATE_LIMIT_EXP_P6_EGC_TB_T_P6 |    |    |    | EG_RATE_LIMIT_MAN_P6_EGC_TB_CBS_P6 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                   | RW           |    | RW                 | RW                               |    |    |    | RW                                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0            |    | 0                  | 0                                | 0  | 0  | 0  | 0                                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                             | Description                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | EGC_RATE_CIR_15_0_P6             | <p>When EGC_TB_EN = 1, total 17 bits EGC_RATE_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps</p> <p><math>EGC\_RATE\_CIR = [Egress\ Rate\ Limit(bps) / 32Kbps]</math></p>                                                                                                                                                                                                          |
| 15     | EG_RATE_LIMIT_EN_P6              | <p><b>Port 6 Egress rate limit control is enabled</b></p> <p>0: Egress rate limit control disable</p> <p>1: Enable</p>                                                                                                                                                                                                                                                                                                              |
| 14     | EGC_TB_EN_P6                     | <p><b>When this bit is disabled, the Egress rate control acts like a leaky bucket principle.</b></p> <p>Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p>                                                                                                      |
| 12     | EGC_RATE_CIR_16_P6               | <b>Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value</b>                                                                                                                                                                                                                                                                                                                                                                  |
| 11:8   | EG_RATE_LIMIT_EXP_P6_EGC_TB_T_P6 | <p><b>Depend on EGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b></p> <p>When EGC_TB_EN = 0, exponent part of Port 6 Egress rate limit control, value range: 0 to 5</p> <p>0: 1Kbps</p> <p>1: 10Kbps</p> <p>2: 100Kbps</p> <p>3: 1Mbps</p> <p>4: 10Mbps</p> <p>5: 100Mbps</p> <p>When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, value range: 0 to 14</p> <p>0: 1/128ms</p> |

| Bit(s) | Name                               | Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
|--------|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                                    | 1: 1/64ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        |                                    | 2: 1/32ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        |                                    | 3: 1/16ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        |                                    | 4: 1/8ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 5: 1/4ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 6: 1/2ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 7: 1ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                                    | 8: 2ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                                    | 9: 4ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                                    | 10: 8ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                                    | 11: 16ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 12: 32ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 13: 64ms                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|        |                                    | 14: 128ms                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7:0    | EG_RATE_LIMIT_MAN_P6_EGC_TB_CBS_P6 | <p><b>Depend on EGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b></p> <p>When EGC_TB_EN = 0, mantissa part of Port 6 Egress rate limit control, value range: 1 to 255</p> <p>Egress Rate Limit = <math>MAN * 10^{(EXP)} * 1Kbps</math></p> <p>When EGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and</p> <p>Token Bucket = Max ( EGC_RATE_CIR*EGC_TB_T, EGC_TB_CBS*512 )</p> |



15021650

MMSCR2\_Q0P6Max-Min scheduler control register 2 of Queue  
0/Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                     |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_CIR_Q0_P6 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                     |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                      |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                      |
| Name  | MIN_RATE_CIR_Q0_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                      |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q0_P6 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021654

MMSCR3\_Q0P6Max-Min scheduler control register 3 of Queue  
0/Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q0_P6 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q0_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q0_P6 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021658

MMSCR2\_Q1P6Max-Min scheduler control register 2 of Queue  
1/Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                            |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_C<br>R_Q1_<br>P6 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                            |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                             |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                             |
| Name  | MIN_RATE_CIR_Q1_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                             |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q1_P6 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502165C

MMSCR3\_Q1P6Max-Min scheduler control register 3 of Queue  
1/Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q1_P6 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q1_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q1_P6 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021660

MMSCR2\_Q2P6

Max-Min scheduler control register 2 of Queue  
2/Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                     |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_CIR_Q2_P6 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                     |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                      |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                      |
| Name  | MIN_RATE_CIR_Q2_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                      |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q2_P6 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021664

MMSCR3\_Q2P6Max-Min scheduler control register 3 of Queue  
2/Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q2_P6 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q2_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q2_P6 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021668

MMSCR2\_Q3P6

Max-Min scheduler control register 2 of Queue  
3/Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_RATE_CIR_Q3_P6 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MIN_RATE_CIR_Q3_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q3_P6 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502166C

MMSCR3\_Q3P6Max-Min scheduler control register 3 of Queue  
3/Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q3_P6 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q3_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q3_P6 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |



15021670

MMSCR2\_Q4P6Max-Min scheduler control register 2 of Queue  
4/Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                            |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_C<br>R_Q4_<br>P6 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                            |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                             |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                             |
| Name  | MIN_RATE_CIR_Q4_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                             |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q4_P6 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021674

MMSCR3\_Q4P6Max-Min scheduler control register 3 of Queue  
4/Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q4_P6 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q4_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q4_P6 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021678

MMSCR2\_Q5P6

Max-Min scheduler control register 2 of Queue  
5/Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_RATE_CIR_Q5_P6 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MIN_RATE_CIR_Q5_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q5_P6 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502167C

MMSCR3\_Q5P6

Max-Min scheduler control register 3 of Queue  
5/Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q5_P6 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q5_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q5_P6 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021680

MMSCR2\_Q6P6

Max-Min scheduler control register 2 of Queue  
6/Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_RATE_CIR_Q6_P6 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MIN_RATE_CIR_Q6_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q6_P6 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021684

MMSCR3\_Q6P6Max-Min scheduler control register 3 of Queue  
6/Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q6_P6 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q6_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q6_P6 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

15021688

MMSCR2\_Q7P6

Max-Min scheduler control register 2 of Queue  
7/Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                            |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_R<br>ATE_C<br>R_Q7_<br>P6 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                            |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                             |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                             |
| Name  | MIN_RATE_CIR_Q7_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                               |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                             |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MIN_RATE_CIR_Q7_P6 | Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |

1502168C

MMSCR3\_Q7P6

Max-Min scheduler control register 3 of Queue  
7/Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|
| Name  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_RATE_CIR_Q7_P6 |
| Type  |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |
| Reset |                    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| Name  | MAX_RATE_CIR_Q7_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  |

| Bit(s) | Name               | Description                                                                 |
|--------|--------------------|-----------------------------------------------------------------------------|
| 16:0   | MAX_RATE_CIR_Q7_P6 | Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps |



15021690      **MMSCR\_P6**      Max-Min scheduler control register of Port 6      00000001

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                           |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------------------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                              |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                              |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                              |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                            |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MIN_<br>MAX_T<br>B_EN_<br>P6 |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                           |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 1                            |

| Bit(s) | Name             | Description                                                                                                                                                                                                                                                                                                  |
|--------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0      | MIN_MAX_TB_EN_P6 | <p><b>When this bit is disabled, the rate limit acts like a leaky bucket principle.</b></p> <p>Otherwise, the rate limit uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p> |

**15021800 IRLCR\_P0 Ingress rate limit control register of Port 0 00000000**

| Bit   | 31                   | 30           | 29 | 28                 | 27                          | 26 | 25 | 24 | 23                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|--------------|----|--------------------|-----------------------------|----|----|----|-------------------------------|----|----|----|----|----|----|----|
| Name  | IGC_RATE_CIR_15_0_P0 |              |    |                    |                             |    |    |    |                               |    |    |    |    |    |    |    |
| Type  | RW                   |              |    |                    |                             |    |    |    |                               |    |    |    |    |    |    |    |
| Reset | 0                    | 0            | 0  | 0                  | 0                           | 0  | 0  | 0  | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14           | 13 | 12                 | 11                          | 10 | 9  | 8  | 7                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | IGC_RATE_EN_P0       | IGC_TB_EN_P0 |    | IGC_RATE_CIR_16_P0 | IGC_RATE_EXP_P0_IGC_TB_T_P0 |    |    |    | IGC_RATE_MAN_P0_IGC_TB_CBS_P0 |    |    |    |    |    |    |    |
| Type  | RW                   | RW           |    | RW                 | RW                          |    |    |    | RW                            |    |    |    |    |    |    |    |
| Reset | 0                    | 0            |    | 0                  | 0                           | 0  | 0  | 0  | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|--------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | IGC_RATE_CIR_15_0_P0        | <p>When IGC_TB_EN = 1, total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps</p> <p><math>IGC\_RATE\_CIR = [Ingress\ Rate\ Limit(bps) / 32Kbps]</math></p>                                                                                                                                                                                                                                |
| 15     | IGC_RATE_EN_P0              | <p><b>Port 0 Ingress rate limit control is enabled</b></p> <p>0: Ingress rate limit control is disabled</p> <p>1: Ingress rate limit control is enabled</p>                                                                                                                                                                                                                                                                                           |
| 14     | IGC_TB_EN_P0                | <p><b>When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.</b></p> <p>Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p>                                                                                                                      |
| 12     | IGC_RATE_CIR_16_P0          | <b>Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value</b>                                                                                                                                                                                                                                                                                                                                                                                    |
| 11:8   | IGC_RATE_EXP_P0_IGC_TB_T_P0 | <p><b>Depend on IGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b></p> <p>When IGC_TB_EN = 0, exponent part of Port 0 Ingress rate limit control, value range: 0 to 5</p> <p>0: 1Kbps</p> <p>1: 10Kbps</p> <p>2: 100Kbps</p> <p>3: 1Mbps</p> <p>4: 10Mbps</p> <p>5: 100Mbps</p> <p>When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, value range: 0 to 14</p> <p>0: 1/128ms</p> <p>1: 1/64ms</p> |

| Bit(s) | Name                          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|--------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                               | 2: 1/32ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                               | 3: 1/16ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                               | 4: 1/8ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 5: 1/4ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 6: 1/2ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 7: 1ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 8: 2ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 9: 4ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 10: 8ms                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                               | 11: 16ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 12: 32ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 13: 64ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 14: 128ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 7:0    | IGC_RATE_MAN_P0_IGC_TB_CBS_P0 | <p><b>Depend on IGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b></p> <p>When IGC_TB_EN = 0, mantissa part of Port 0 Ingress rate limit control, value range: 1 to 255</p> <p>Ingress Rate Limit = <math>MAN * 10^{(EXP)} * 1Kbps</math></p> <p>When IGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and</p> <p>Token Bucket = Max ( IGC_RATE_CIR*IGC_TB_T, IGC_TB_CBS*512 )</p> |

15021804      **FPC\_RXCTRL\_P0**      Free page count at RX\_CTRL of Port 0      00000003

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18            | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2             | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    | FPC_RXCTRL_P0 |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    | RO            |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    | 0             | 1  | 1  |

| Bit(s) | Name          | Description                                         |
|--------|---------------|-----------------------------------------------------|
| 2:0    | FPC_RXCTRL_P0 | It indicates the free page count at RX_CTRL module. |

**1502180C MMDPR\_10\_Q0P0 Drop precedence control 10 of Q0 Port 0 00000000**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  | P0_DP_en     |    |    |    |    | P0Q0_pr_dp10 |    |    |              |    |    | P0Q0_ht_dp10 |    |    |    |    |
| Type  | RW           |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset | 0            |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P0Q0_ht_dp10 |    |    |    |    |              |    |    | P0Q0_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | P0_DP_en     | <b>Enable Drop Precedence function of P0. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)</b> <p>(1) When queue depth <math>\geq</math> P0Q0_ht_dp10, the drop probability of the incoming packet is 100%.</p> <p>(2) When queue depth <math>&lt;</math> P0Q0_lt_dp10, the drop probability of the incoming packet is 0%.</p> <p>(3) When P0Q0_lt_dp10 <math>\leq</math> queue depth <math>&lt;</math> P0Q0_ht_dp10, the drop probability of incoming packet is based on the setting P0Q0_pr_dp10.</p> <p>0: Disable</p> <p>1: Enable</p> |
| 26:24  | P0Q0_pr_dp10 | <b>Drop probability of P0 Q0 for drop precedence = 2'b10.</b> <p>0x0: 0%</p> <p>0x1: 12.5%</p> <p>0xn: <math>n \times 12.5\%</math></p> <p>0x7: 87.5% (<math>n=2 \sim 6</math>)</p>                                                                                                                                                                                                                                                                                                                                                                                                          |
| 20:12  | P0Q0_ht_dp10 | <b>High threshold of P0 Q0 depth for drop precedence = 2'b10. Unit: page size</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 8:0    | P0Q0_lt_dp10 | <b>Low threshold of P0 Q0 depth for drop precedence = 2'b10. Unit: page size</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

15021810      **MMDPR\_10\_Q1P0**      Drop precedence control 10 of Q1 Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P0Q1_pr_dp10 |    |              |    |    |    | P0Q1_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P0Q1_ht_dp10 |    |    |    |    |              |    | P0Q1_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P0Q1_pr_dp10 | <b>Drop probability of P0 Q1 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P0Q1_ht_dp10 | <b>High threshold of P0 Q1 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P0Q1_lt_dp10 | <b>Low threshold of P0 Q1 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021814      **MMDPR\_10\_Q2P0**      Drop precedence control 10 of Q2 Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P0Q2_pr_dp10 |    |    |              |    |    | P0Q2_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P0Q2_ht_dp10 |    |    |    |    |              |    |    | P0Q2_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P0Q2_pr_dp10 | <b>Drop probability of P0 Q2 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P0Q2_ht_dp10 | <b>High threshold of P0 Q2 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P0Q2_lt_dp10 | <b>Low threshold of P0 Q2 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021818      **MMDPR\_10\_Q3P0**      Drop precedence control 10 of Q3 Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P0Q3_pr_dp10 |    |              |    |    |    | P0Q3_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P0Q3_ht_dp10 |    |    |    |    |              |    | P0Q3_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P0Q3_pr_dp10 | <b>Drop probability of P0 Q3 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P0Q3_ht_dp10 | <b>High threshold of P0 Q3 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P0Q3_lt_dp10 | <b>Low threshold of P0 Q3 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |



1502181C      **MMDPR 10 Q4P0**      Drop precedence control 10 of Q4 Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P0Q4_pr_dp10 |    |              |    |    |    | P0Q4_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P0Q4_ht_dp10 |    |    |    |    |              |    | P0Q4_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P0Q4_pr_dp10 | <b>Drop probability of P0 Q4 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P0Q4_ht_dp10 | <b>High threshold of P0 Q4 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P0Q4_lt_dp10 | <b>Low threshold of P0 Q4 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021820      **MMDPR\_10\_Q5P0**      Drop precedence control 10 of Q5 Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P0Q5_pr_dp10 |    |              |    |    |    | P0Q5_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P0Q5_ht_dp10 |    |    |    |    |              |    | P0Q5_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P0Q5_pr_dp10 | <b>Drop probability of P0 Q5 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P0Q5_ht_dp10 | <b>High threshold of P0 Q5 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P0Q5_lt_dp10 | <b>Low threshold of P0 Q5 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021824      **MMDPR\_10\_Q6P0**      Drop precedence control 10 of Q6 Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P0Q6_pr_dp10 |    |              |    |    |    | P0Q6_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P0Q6_ht_dp10 |    |    |    |    |              |    | P0Q6_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P0Q6_pr_dp10 | <b>Drop probability of P0 Q6 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P0Q6_ht_dp10 | <b>High threshold of P0 Q6 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P0Q6_lt_dp10 | <b>Low threshold of P0 Q6 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021828      **MMDPR\_10\_Q7P0**      Drop precedence control 10 of Q7 Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P0Q7_pr_dp10 |    |              |    |    |    | P0Q7_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P0Q7_ht_dp10 |    |    |    |    |              |    | P0Q7_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P0Q7_pr_dp10 | <b>Drop probability of P0 Q7 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P0Q7_ht_dp10 | <b>High threshold of P0 Q7 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P0Q7_lt_dp10 | <b>Low threshold of P0 Q7 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

1502182C      **MMDPR\_11\_Q0P0**      Drop precedence control 11 of Q0 Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P0Q0_pr_dp11 |    |              |    |    |    | P0Q0_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P0Q0_ht_dp11 |    |    |    |    |              |    | P0Q0_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P0Q0_pr_dp11 | <b>Drop probability of P0 Q0 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P0Q0_ht_dp11 | <b>High threshold of P0 Q0 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P0Q0_lt_dp11 | <b>Low threshold of P0 Q0 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021830      **MMDPR\_11\_Q1P0**      Drop precedence control 11 of Q1 Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P0Q1_pr_dp11 |    |              |    |    |    | P0Q1_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P0Q1_ht_dp11 |    |    |    |    |              |    | P0Q1_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P0Q1_pr_dp11 | <b>Drop probability of P0 Q1 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P0Q1_ht_dp11 | <b>High threshold of P0 Q1 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P0Q1_lt_dp11 | <b>Low threshold of P0 Q1 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021834      **MMDPR\_11\_Q2P0**      Drop precedence control 11 of Q2 Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P0Q2_pr_dp11 |    |              |    |    |    | P0Q2_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P0Q2_ht_dp11 |    |    |    |    |              |    | P0Q2_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P0Q2_pr_dp11 | <b>Drop probability of P0 Q2 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P0Q2_ht_dp11 | <b>High threshold of P0 Q2 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P0Q2_lt_dp11 | <b>Low threshold of P0 Q2 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021838      **MMDPR\_11\_Q3P0**      Drop precedence control 11 of Q3 Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P0Q3_pr_dp11 |    |              |    |    |    | P0Q3_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P0Q3_ht_dp11 |    |    |    |    |              |    | P0Q3_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P0Q3_pr_dp11 | <b>Drop probability of P0 Q3 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P0Q3_ht_dp11 | <b>High threshold of P0 Q3 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P0Q3_lt_dp11 | <b>Low threshold of P0 Q3 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |



1502183C      **MMDPR\_11\_Q4P0**      Drop precedence control 11 of Q4 Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P0Q4_pr_dp11 |    |              |    |    |    | P0Q4_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P0Q4_ht_dp11 |    |    |    |    |              |    | P0Q4_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P0Q4_pr_dp11 | <b>Drop probability of P0 Q4 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P0Q4_ht_dp11 | <b>High threshold of P0 Q4 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P0Q4_lt_dp11 | <b>Low threshold of P0 Q4 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021840      **MMDPR\_11\_Q5P0**      Drop precedence control 11 of Q5 Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P0Q5_pr_dp11 |    |              |    |    |    | P0Q5_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P0Q5_ht_dp11 |    |    |    |    |              |    | P0Q5_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P0Q5_pr_dp11 | <b>Drop probability of P0 Q5 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P0Q5_ht_dp11 | <b>High threshold of P0 Q5 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P0Q5_lt_dp11 | <b>Low threshold of P0 Q5 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021844      **MMDPR\_11\_Q6P0**      Drop precedence control 11 of Q6 Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P0Q6_pr_dp11 |    |              |    |    |    | P0Q6_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P0Q6_ht_dp11 |    |    |    |    |              |    | P0Q6_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P0Q6_pr_dp11 | <b>Drop probability of P0 Q6 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P0Q6_ht_dp11 | <b>High threshold of P0 Q6 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P0Q6_lt_dp11 | <b>Low threshold of P0 Q6 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021848      **MMDPR\_11\_Q7P0**      Drop precedence control 11 of Q7 Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P0Q7_pr_dp11 |    |              |    |    |    | P0Q7_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P0Q7_ht_dp11 |    |    |    |    |              |    | P0Q7_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P0Q7_pr_dp11 | <b>Drop probability of P0 Q7 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P0Q7_ht_dp11 | <b>High threshold of P0 Q7 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P0Q7_lt_dp11 | <b>Low threshold of P0 Q7 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021900 IRLCR\_P1 Ingress rate limit control register of Port 1 00000000

| Bit   | 31                   | 30           | 29 | 28                 | 27                          | 26 | 25 | 24 | 23                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|--------------|----|--------------------|-----------------------------|----|----|----|-------------------------------|----|----|----|----|----|----|----|
| Name  | IGC_RATE_CIR_15_0_P1 |              |    |                    |                             |    |    |    |                               |    |    |    |    |    |    |    |
| Type  | RW                   |              |    |                    |                             |    |    |    |                               |    |    |    |    |    |    |    |
| Reset | 0                    | 0            | 0  | 0                  | 0                           | 0  | 0  | 0  | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14           | 13 | 12                 | 11                          | 10 | 9  | 8  | 7                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | IGC_RATE_EN_P1       | IGC_TB_EN_P1 |    | IGC_RATE_CIR_16_P1 | IGC_RATE_EXP_P1_IGC_TB_T_P1 |    |    |    | IGC_RATE_MAN_P1_IGC_TB_CBS_P1 |    |    |    |    |    |    |    |
| Type  | RW                   | RW           |    | RW                 | RW                          |    |    |    | RW                            |    |    |    |    |    |    |    |
| Reset | 0                    | 0            |    | 0                  | 0                           | 0  | 0  | 0  | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|--------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | IGC_RATE_CIR_15_0_P1        | <p>When IGC_TB_EN = 1, total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps</p> <p><math>IGC\_RATE\_CIR = [Ingress\ Rate\ Limit(bps) / 32Kbps]</math></p>                                                                                                                                                                                                                                |
| 15     | IGC_RATE_EN_P1              | <p><b>Port 1 Ingress rate limit control is enabled</b></p> <p>0: Ingress rate limit control is disabled</p> <p>1: Ingress rate limit control is enabled</p>                                                                                                                                                                                                                                                                                           |
| 14     | IGC_TB_EN_P1                | <p><b>When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.</b></p> <p>Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p>                                                                                                                      |
| 12     | IGC_RATE_CIR_16_P1          | <b>Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value</b>                                                                                                                                                                                                                                                                                                                                                                                    |
| 11:8   | IGC_RATE_EXP_P1_IGC_TB_T_P1 | <p><b>Depend on IGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b></p> <p>When IGC_TB_EN = 0, exponent part of Port 1 Ingress rate limit control, value range: 0 to 5</p> <p>0: 1Kbps</p> <p>1: 10Kbps</p> <p>2: 100Kbps</p> <p>3: 1Mbps</p> <p>4: 10Mbps</p> <p>5: 100Mbps</p> <p>When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, value range: 0 to 14</p> <p>0: 1/128ms</p> <p>1: 1/64ms</p> |

| Bit(s) | Name                          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|--------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                               | 2: 1/32ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                               | 3: 1/16ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                               | 4: 1/8ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 5: 1/4ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 6: 1/2ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 7: 1ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 8: 2ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 9: 4ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 10: 8ms                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                               | 11: 16ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 12: 32ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 13: 64ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 14: 128ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 7:0    | IGC_RATE_MAN_P1_IGC_TB_CBS_P1 | <p><b>Depend on IGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b></p> <p>When IGC_TB_EN = 0, mantissa part of Port 1 Ingress rate limit control, value range: 1 to 255</p> <p>Ingress Rate Limit = <math>MAN * 10^{(EXP)} * 1Kbps</math></p> <p>When IGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and</p> <p>Token Bucket = Max ( IGC_RATE_CIR*IGC_TB_T, IGC_TB_CBS*512 )</p> |

15021904      **FPC\_RXCTRL\_P1**      Free page count at RX\_CTRL of Port 1      00000003

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18            | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2             | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    | FPC_RXCTRL_P1 |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    | RO            |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    | 0             | 1  | 1  |

| Bit(s) | Name          | Description                                         |
|--------|---------------|-----------------------------------------------------|
| 2:0    | FPC_RXCTRL_P1 | It indicates the free page count at RX_CTRL module. |

1502190C MMDPR\_10\_Q0P1 Drop precedence control 10 of Q0 Port 1 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  | P1_DP_en     |    |    |    |    | P1Q0_pr_dp10 |    |    |              |    |    | P1Q0_ht_dp10 |    |    |    |    |
| Type  | RW           |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset | 0            |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P1Q0_ht_dp10 |    |    |    |    |              |    |    | P1Q0_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | P1_DP_en     | <p><b>Enable Drop Precedence function of P1. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)</b></p> <p>(1) When queue depth <math>\geq</math> P1Q0_ht_dp10, the drop probability of the incoming packet is 100%.</p> <p>(2) When queue depth <math>&lt;</math> P1Q0_lt_dp10, the drop probability of the incoming packet is 0%.</p> <p>(3) When P1Q0_lt_dp10 <math>\leq</math> queue depth <math>&lt;</math> P1Q0_ht_dp10, the drop probability of incoming packet is based on the setting P1Q0_pr_dp10.</p> <p>0: Disable</p> <p>1: Enable</p> |
| 26:24  | P1Q0_pr_dp10 | <p><b>Drop probability of P1 Q0 for drop precedence = 2'b10.</b></p> <p>0x0: 0%</p> <p>0x1: 12.5%</p> <p>0xn: <math>n \times 12.5\%</math></p> <p>0x7: 87.5% (<math>n=2 \sim 6</math>)</p>                                                                                                                                                                                                                                                                                                                                                                                                          |
| 20:12  | P1Q0_ht_dp10 | <p><b>High threshold of P1 Q0 depth for drop precedence = 2'b10. Unit: page size</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 8:0    | P1Q0_lt_dp10 | <p><b>Low threshold of P1 Q0 depth for drop precedence = 2'b10. Unit: page size</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |



15021910      MMDPR 10 Q1P1      Drop precedence control 10 of Q1 Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P1Q1_pr_dp10 |    |    |              |    |    | P1Q1_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P1Q1_ht_dp10 |    |    |    |    |              |    |    | P1Q1_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P1Q1_pr_dp10 | <b>Drop probability of P1 Q1 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P1Q1_ht_dp10 | <b>High threshold of P1 Q1 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P1Q1_lt_dp10 | <b>Low threshold of P1 Q1 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021914 MMDPR\_10\_Q2P1 Drop precedence control 10 of Q2 Port 1 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P1Q2_pr_dp10 |    |    |              |    |    | P1Q2_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P1Q2_ht_dp10 |    |    |    |    |              |    |    | P1Q2_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P1Q2_pr_dp10 | <b>Drop probability of P1 Q2 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P1Q2_ht_dp10 | <b>High threshold of P1 Q2 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P1Q2_lt_dp10 | <b>Low threshold of P1 Q2 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021918      MMDPR\_10\_Q3P1      Drop precedence control 10 of Q3 Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P1Q3_pr_dp10 |    |    |              |    |    | P1Q3_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P1Q3_ht_dp10 |    |    |    |    |              |    |    | P1Q3_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P1Q3_pr_dp10 | <b>Drop probability of P1 Q3 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P1Q3_ht_dp10 | <b>High threshold of P1 Q3 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P1Q3_lt_dp10 | <b>Low threshold of P1 Q3 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

1502191C      MMDPR 10 Q4P1      Drop precedence control 10 of Q4 Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P1Q4_pr_dp10 |    |    |              |    |    | P1Q4_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P1Q4_ht_dp10 |    |    |    |    |              |    |    | P1Q4_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P1Q4_pr_dp10 | <b>Drop probability of P1 Q4 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P1Q4_ht_dp10 | <b>High threshold of P1 Q4 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P1Q4_lt_dp10 | <b>Low threshold of P1 Q4 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021920      MMDPR\_10\_Q5P1      Drop precedence control 10 of Q5 Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P1Q5_pr_dp10 |    |              |    |    |    | P1Q5_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P1Q5_ht_dp10 |    |    |    |    |              |    | P1Q5_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P1Q5_pr_dp10 | <b>Drop probability of P1 Q5 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P1Q5_ht_dp10 | <b>High threshold of P1 Q5 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P1Q5_lt_dp10 | <b>Low threshold of P1 Q5 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021924 MMDPR\_10\_Q6P1 Drop precedence control 10 of Q6 Port 1 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P1Q6_pr_dp10 |    |    |              |    |    | P1Q6_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P1Q6_ht_dp10 |    |    |    |    |              |    |    | P1Q6_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P1Q6_pr_dp10 | <b>Drop probability of P1 Q6 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P1Q6_ht_dp10 | <b>High threshold of P1 Q6 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P1Q6_lt_dp10 | <b>Low threshold of P1 Q6 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021928      MMDPR\_10\_Q7P1      Drop precedence control 10 of Q7 Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P1Q7_pr_dp10 |    |              |    |    |    | P1Q7_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P1Q7_ht_dp10 |    |    |    |    |              |    | P1Q7_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P1Q7_pr_dp10 | <b>Drop probability of P1 Q7 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P1Q7_ht_dp10 | <b>High threshold of P1 Q7 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P1Q7_lt_dp10 | <b>Low threshold of P1 Q7 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

1502192C      MMDPR\_11\_Q0P1      Drop precedence control 11 of Q0 Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P1Q0_pr_dp11 |    |              |    |    |    | P1Q0_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P1Q0_ht_dp11 |    |    |    |    |              |    | P1Q0_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P1Q0_pr_dp11 | <b>Drop probability of P1 Q0 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P1Q0_ht_dp11 | <b>High threshold of P1 Q0 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P1Q0_lt_dp11 | <b>Low threshold of P1 Q0 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |



15021930 MMDPR\_11\_Q1P1 Drop precedence control 11 of Q1 Port 1 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P1Q1_pr_dp11 |    |              |    |    |    | P1Q1_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P1Q1_ht_dp11 |    |    |    |    |              |    | P1Q1_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P1Q1_pr_dp11 | <b>Drop probability of P1 Q1 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P1Q1_ht_dp11 | <b>High threshold of P1 Q1 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P1Q1_lt_dp11 | <b>Low threshold of P1 Q1 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021934 MMDPR\_11\_Q2P1 Drop precedence control 11 of Q2 Port 1 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P1Q2_pr_dp11 |    |              |    |    |    | P1Q2_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P1Q2_ht_dp11 |    |    |    |    |              |    | P1Q2_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P1Q2_pr_dp11 | <b>Drop probability of P1 Q2 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P1Q2_ht_dp11 | <b>High threshold of P1 Q2 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P1Q2_lt_dp11 | <b>Low threshold of P1 Q2 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021938      MMDPR\_11\_Q3P1      Drop precedence control 11 of Q3 Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P1Q3_pr_dp11 |    |              |    |    |    | P1Q3_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P1Q3_ht_dp11 |    |    |    |    |              |    | P1Q3_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P1Q3_pr_dp11 | <b>Drop probability of P1 Q3 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P1Q3_ht_dp11 | <b>High threshold of P1 Q3 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P1Q3_lt_dp11 | <b>Low threshold of P1 Q3 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

1502193C      MMDPR\_11\_Q4P1      Drop precedence control 11 of Q4 Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P1Q4_pr_dp11 |    |              |    |    |    | P1Q4_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P1Q4_ht_dp11 |    |    |    |    |              |    | P1Q4_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P1Q4_pr_dp11 | <b>Drop probability of P1 Q4 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P1Q4_ht_dp11 | <b>High threshold of P1 Q4 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P1Q4_lt_dp11 | <b>Low threshold of P1 Q4 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021940      MMDPR\_11\_Q5P1      Drop precedence control 11 of Q5 Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P1Q5_pr_dp11 |    |              |    |    |    | P1Q5_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P1Q5_ht_dp11 |    |    |    |    |              |    | P1Q5_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P1Q5_pr_dp11 | <b>Drop probability of P1 Q5 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P1Q5_ht_dp11 | <b>High threshold of P1 Q5 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P1Q5_lt_dp11 | <b>Low threshold of P1 Q5 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021944 MMDPR\_11\_Q6P1 Drop precedence control 11 of Q6 Port 1 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P1Q6_pr_dp11 |    |              |    |    |    | P1Q6_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P1Q6_ht_dp11 |    |    |    |    |              |    | P1Q6_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P1Q6_pr_dp11 | <b>Drop probability of P1 Q6 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P1Q6_ht_dp11 | <b>High threshold of P1 Q6 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P1Q6_lt_dp11 | <b>Low threshold of P1 Q6 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021948      MMDPR\_11\_Q7P1      Drop precedence control 11 of Q7 Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P1Q7_pr_dp11 |    |              |    |    |    | P1Q7_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P1Q7_ht_dp11 |    |    |    |    |              |    | P1Q7_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P1Q7_pr_dp11 | <b>Drop probability of P1 Q7 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P1Q7_ht_dp11 | <b>High threshold of P1 Q7 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P1Q7_lt_dp11 | <b>Low threshold of P1 Q7 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021A00 IRLCR\_P2 Ingress rate limit control register of Port 2 00000000

| Bit   | 31                   | 30           | 29 | 28                 | 27                          | 26 | 25 | 24 | 23                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|--------------|----|--------------------|-----------------------------|----|----|----|-------------------------------|----|----|----|----|----|----|----|
| Name  | IGC_RATE_CIR_15_0_P2 |              |    |                    |                             |    |    |    |                               |    |    |    |    |    |    |    |
| Type  | RW                   |              |    |                    |                             |    |    |    |                               |    |    |    |    |    |    |    |
| Reset | 0                    | 0            | 0  | 0                  | 0                           | 0  | 0  | 0  | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14           | 13 | 12                 | 11                          | 10 | 9  | 8  | 7                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | IGC_RATE_EN_P2       | IGC_TB_EN_P2 |    | IGC_RATE_CIR_16_P2 | IGC_RATE_EXP_P2_IGC_TB_T_P2 |    |    |    | IGC_RATE_MAN_P2_IGC_TB_CBS_P2 |    |    |    |    |    |    |    |
| Type  | RW                   | RW           |    | RW                 | RW                          |    |    |    | RW                            |    |    |    |    |    |    |    |
| Reset | 0                    | 0            |    | 0                  | 0                           | 0  | 0  | 0  | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|--------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | IGC_RATE_CIR_15_0_P2        | <p>When IGC_TB_EN = 1, total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps</p> <p><math>IGC\_RATE\_CIR = [Ingress\ Rate\ Limit(bps) / 32Kbps]</math></p>                                                                                                                                                                                                                                |
| 15     | IGC_RATE_EN_P2              | <p><b>Port 2 Ingress rate limit control is enabled</b></p> <p>0: Ingress rate limit control is disabled</p> <p>1: Ingress rate limit control is enabled</p>                                                                                                                                                                                                                                                                                           |
| 14     | IGC_TB_EN_P2                | <p><b>When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.</b></p> <p>Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p>                                                                                                                      |
| 12     | IGC_RATE_CIR_16_P2          | <b>Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value</b>                                                                                                                                                                                                                                                                                                                                                                                    |
| 11:8   | IGC_RATE_EXP_P2_IGC_TB_T_P2 | <p><b>Depend on IGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b></p> <p>When IGC_TB_EN = 0, exponent part of Port 2 Ingress rate limit control, value range: 0 to 5</p> <p>0: 1Kbps</p> <p>1: 10Kbps</p> <p>2: 100Kbps</p> <p>3: 1Mbps</p> <p>4: 10Mbps</p> <p>5: 100Mbps</p> <p>When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, value range: 0 to 14</p> <p>0: 1/128ms</p> <p>1: 1/64ms</p> |



| Bit(s) | Name                          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|--------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                               | 2: 1/32ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                               | 3: 1/16ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                               | 4: 1/8ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 5: 1/4ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 6: 1/2ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 7: 1ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 8: 2ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 9: 4ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 10: 8ms                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                               | 11: 16ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 12: 32ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 13: 64ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 14: 128ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 7:0    | IGC_RATE_MAN_P2_IGC_TB_CBS_P2 | <p><b>Depend on IGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b></p> <p>When IGC_TB_EN = 0, mantissa part of Port 2 Ingress rate limit control, value range: 1 to 255</p> <p>Ingress Rate Limit = <math>MAN * 10^{(EXP)} * 1Kbps</math></p> <p>When IGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and</p> <p>Token Bucket = Max ( IGC_RATE_CIR*IGC_TB_T, IGC_TB_CBS*512 )</p> |

15021A04      FPC\_RXCTRL\_P2      Free page count at RX\_CTRL of Port 2      00000003

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18            | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2             | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    | FPC_RXCTRL_P2 |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    | RO            |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    | 0             | 1  | 1  |

| Bit(s) | Name          | Description                                         |
|--------|---------------|-----------------------------------------------------|
| 2:0    | FPC_RXCTRL_P2 | It indicates the free page count at RX_CTRL module. |

15021A0C MMDPR\_10\_Q0P2 Drop precedence control 10 of Q0 Port 2 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  | P2_DP_en     |    |    |    |    | P2Q0_pr_dp10 |    |    |              |    |    | P2Q0_ht_dp10 |    |    |    |    |
| Type  | RW           |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset | 0            |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P2Q0_ht_dp10 |    |    |    |    |              |    |    | P2Q0_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | P2_DP_en     | <p><b>Enable Drop Precedence function of P2. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)</b></p> <p>(1) When queue depth <math>\geq</math> P2Q0_ht_dp10, the drop probability of the incoming packet is 100%.</p> <p>(2) When queue depth <math>&lt;</math> P2Q0_lt_dp10, the drop probability of the incoming packet is 0%.</p> <p>(3) When <math>P2Q0\_lt\_dp10 \leq \text{queue depth} &lt; P2Q0\_ht\_dp10</math>, the drop probability of incoming packet is based on the setting P2Q0_pr_dp10.</p> <p>0: Disable</p> <p>1: Enable</p> |
| 26:24  | P2Q0_pr_dp10 | <p><b>Drop probability of P2 Q0 for drop precedence = 2'b10.</b></p> <p>0x0: 0%</p> <p>0x1: 12.5%</p> <p>0xn: <math>n \times 12.5\%</math></p> <p>0x7: 87.5% (<math>n=2 \sim 6</math>)</p>                                                                                                                                                                                                                                                                                                                                                                                                        |
| 20:12  | P2Q0_ht_dp10 | <p><b>High threshold of P2 Q0 depth for drop precedence = 2'b10. Unit: page size</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 8:0    | P2Q0_lt_dp10 | <p><b>Low threshold of P2 Q0 depth for drop precedence = 2'b10. Unit: page size</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

15021A10      **MMDPR\_10\_Q1P2**      Drop precedence control 10 of Q1 Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P2Q1_pr_dp10 |    |    |              |    |    | P2Q1_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P2Q1_ht_dp10 |    |    |    |    |              |    |    | P2Q1_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P2Q1_pr_dp10 | <b>Drop probability of P2 Q1 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P2Q1_ht_dp10 | <b>High threshold of P2 Q1 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P2Q1_lt_dp10 | <b>Low threshold of P2 Q1 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021A14      **MMDPR\_10\_Q2P2**      Drop precedence control 10 of Q2 Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P2Q2_pr_dp10 |    |    |              |    |    | P2Q2_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P2Q2_ht_dp10 |    |    |    |    |              |    |    | P2Q2_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P2Q2_pr_dp10 | <b>Drop probability of P2 Q2 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P2Q2_ht_dp10 | <b>High threshold of P2 Q2 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P2Q2_lt_dp10 | <b>Low threshold of P2 Q2 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021A18      MMDPR 10 Q3P2      Drop precedence control 10 of Q3 Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P2Q3_pr_dp10 |    |    |              |    |    | P2Q3_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P2Q3_ht_dp10 |    |    |    |    |              |    |    | P2Q3_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P2Q3_pr_dp10 | <b>Drop probability of P2 Q3 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P2Q3_ht_dp10 | <b>High threshold of P2 Q3 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P2Q3_lt_dp10 | <b>Low threshold of P2 Q3 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021A1C      **MMDPR\_10\_Q4P2**      Drop precedence control 10 of Q4 Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P2Q4_pr_dp10 |    |    |              |    |    | P2Q4_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P2Q4_ht_dp10 |    |    |    |    |              |    |    | P2Q4_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P2Q4_pr_dp10 | <b>Drop probability of P2 Q4 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P2Q4_ht_dp10 | <b>High threshold of P2 Q4 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P2Q4_lt_dp10 | <b>Low threshold of P2 Q4 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021A20      MMDPR\_10\_Q5P2      Drop precedence control 10 of Q5 Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P2Q5_pr_dp10 |    |    |              |    |    | P2Q5_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P2Q5_ht_dp10 |    |    |    |    |              |    |    | P2Q5_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P2Q5_pr_dp10 | <b>Drop probability of P2 Q5 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P2Q5_ht_dp10 | <b>High threshold of P2 Q5 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P2Q5_lt_dp10 | <b>Low threshold of P2 Q5 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |



15021A24      **MMDPR\_10\_Q6P2**      Drop precedence control 10 of Q6 Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P2Q6_pr_dp10 |    |    |              |    |    | P2Q6_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P2Q6_ht_dp10 |    |    |    |    |              |    |    | P2Q6_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P2Q6_pr_dp10 | <b>Drop probability of P2 Q6 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P2Q6_ht_dp10 | <b>High threshold of P2 Q6 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P2Q6_lt_dp10 | <b>Low threshold of P2 Q6 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021A28      MMDPR\_10\_Q7P2      Drop precedence control 10 of Q7 Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P2Q7_pr_dp10 |    |              |    |    |    | P2Q7_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P2Q7_ht_dp10 |    |    |    |    |              |    | P2Q7_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P2Q7_pr_dp10 | <b>Drop probability of P2 Q7 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P2Q7_ht_dp10 | <b>High threshold of P2 Q7 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P2Q7_lt_dp10 | <b>Low threshold of P2 Q7 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021A2C      MMDPR\_11\_Q0P2      Drop precedence control 11 of Q0 Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P2Q0_pr_dp11 |    |              |    |    |    | P2Q0_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P2Q0_ht_dp11 |    |    |    |    |              |    | P2Q0_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P2Q0_pr_dp11 | <b>Drop probability of P2 Q0 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P2Q0_ht_dp11 | <b>High threshold of P2 Q0 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P2Q0_lt_dp11 | <b>Low threshold of P2 Q0 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021A30      **MMDPR\_11\_Q1P2**      Drop precedence control 11 of Q1 Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P2Q1_pr_dp11 |    |              |    |    |    | P2Q1_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P2Q1_ht_dp11 |    |    |    |    |              |    | P2Q1_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P2Q1_pr_dp11 | <b>Drop probability of P2 Q1 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P2Q1_ht_dp11 | <b>High threshold of P2 Q1 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P2Q1_lt_dp11 | <b>Low threshold of P2 Q1 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021A34      **MMDPR\_11\_Q2P2**      Drop precedence control 11 of Q2 Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P2Q2_pr_dp11 |    |              |    |    |    | P2Q2_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P2Q2_ht_dp11 |    |    |    |    |              |    | P2Q2_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P2Q2_pr_dp11 | <b>Drop probability of P2 Q2 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P2Q2_ht_dp11 | <b>High threshold of P2 Q2 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P2Q2_lt_dp11 | <b>Low threshold of P2 Q2 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021A38      MMDPR\_11\_Q3P2      Drop precedence control 11 of Q3 Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P2Q3_pr_dp11 |    |              |    |    |    | P2Q3_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P2Q3_ht_dp11 |    |    |    |    |              |    | P2Q3_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P2Q3_pr_dp11 | <b>Drop probability of P2 Q3 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P2Q3_ht_dp11 | <b>High threshold of P2 Q3 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P2Q3_lt_dp11 | <b>Low threshold of P2 Q3 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021A3C      **MMDPR\_11\_Q4P2**      Drop precedence control 11 of Q4 Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P2Q4_pr_dp11 |    |              |    |    |    | P2Q4_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P2Q4_ht_dp11 |    |    |    |    |              |    | P2Q4_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P2Q4_pr_dp11 | <b>Drop probability of P2 Q4 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P2Q4_ht_dp11 | <b>High threshold of P2 Q4 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P2Q4_lt_dp11 | <b>Low threshold of P2 Q4 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021A40      MMDPR\_11\_Q5P2      Drop precedence control 11 of Q5 Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P2Q5_pr_dp11 |    |              |    |    |    | P2Q5_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P2Q5_ht_dp11 |    |    |    |    |              |    | P2Q5_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P2Q5_pr_dp11 | <b>Drop probability of P2 Q5 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P2Q5_ht_dp11 | <b>High threshold of P2 Q5 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P2Q5_lt_dp11 | <b>Low threshold of P2 Q5 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |



15021A44      **MMDPR\_11\_Q6P2**      Drop precedence control 11 of Q6 Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P2Q6_pr_dp11 |    |              |    |    |    | P2Q6_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P2Q6_ht_dp11 |    |    |    |    |              |    | P2Q6_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P2Q6_pr_dp11 | <b>Drop probability of P2 Q6 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P2Q6_ht_dp11 | <b>High threshold of P2 Q6 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P2Q6_lt_dp11 | <b>Low threshold of P2 Q6 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021A48      **MMDPR\_11\_Q7P2**      Drop precedence control 11 of Q7 Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P2Q7_pr_dp11 |    |              |    |    |    | P2Q7_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P2Q7_ht_dp11 |    |    |    |    |              |    | P2Q7_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P2Q7_pr_dp11 | <b>Drop probability of P2 Q7 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P2Q7_ht_dp11 | <b>High threshold of P2 Q7 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P2Q7_lt_dp11 | <b>Low threshold of P2 Q7 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

**15021B00 IRLCR\_P3 Ingress rate limit control register of Port 3 00000000**

| Bit   | 31                   | 30           | 29 | 28                 | 27                          | 26 | 25 | 24 | 23                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|--------------|----|--------------------|-----------------------------|----|----|----|-------------------------------|----|----|----|----|----|----|----|
| Name  | IGC_RATE_CIR_15_0_P3 |              |    |                    |                             |    |    |    |                               |    |    |    |    |    |    |    |
| Type  | RW                   |              |    |                    |                             |    |    |    |                               |    |    |    |    |    |    |    |
| Reset | 0                    | 0            | 0  | 0                  | 0                           | 0  | 0  | 0  | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14           | 13 | 12                 | 11                          | 10 | 9  | 8  | 7                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | IGC_RATE_EN_P3       | IGC_TB_EN_P3 |    | IGC_RATE_CIR_16_P3 | IGC_RATE_EXP_P3_IGC_TB_T_P3 |    |    |    | IGC_RATE_MAN_P3_IGC_TB_CBS_P3 |    |    |    |    |    |    |    |
| Type  | RW                   | RW           |    | RW                 | RW                          |    |    |    | RW                            |    |    |    |    |    |    |    |
| Reset | 0                    | 0            |    | 0                  | 0                           | 0  | 0  | 0  | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|--------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | IGC_RATE_CIR_15_0_P3        | <p>When IGC_TB_EN = 1, total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps</p> <p><math>IGC\_RATE\_CIR = [Ingress\ Rate\ Limit(bps) / 32Kbps]</math></p>                                                                                                                                                                                                                                |
| 15     | IGC_RATE_EN_P3              | <p><b>Port 3 Ingress rate limit control is enabled</b></p> <p>0: Ingress rate limit control is disabled</p> <p>1: Ingress rate limit control is enabled</p>                                                                                                                                                                                                                                                                                           |
| 14     | IGC_TB_EN_P3                | <p><b>When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.</b></p> <p>Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p>                                                                                                                      |
| 12     | IGC_RATE_CIR_16_P3          | <b>Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value</b>                                                                                                                                                                                                                                                                                                                                                                                    |
| 11:8   | IGC_RATE_EXP_P3_IGC_TB_T_P3 | <p><b>Depend on IGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b></p> <p>When IGC_TB_EN = 0, exponent part of Port 3 Ingress rate limit control, value range: 0 to 5</p> <p>0: 1Kbps</p> <p>1: 10Kbps</p> <p>2: 100Kbps</p> <p>3: 1Mbps</p> <p>4: 10Mbps</p> <p>5: 100Mbps</p> <p>When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, value range: 0 to 14</p> <p>0: 1/128ms</p> <p>1: 1/64ms</p> |

| Bit(s) | Name                          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|--------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                               | 2: 1/32ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                               | 3: 1/16ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                               | 4: 1/8ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 5: 1/4ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 6: 1/2ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 7: 1ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 8: 2ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 9: 4ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 10: 8ms                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                               | 11: 16ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 12: 32ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 13: 64ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 14: 128ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 7:0    | IGC_RATE_MAN_P3_IGC_TB_CBS_P3 | <p><b>Depend on IGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b></p> <p>When IGC_TB_EN = 0, mantissa part of Port 3 Ingress rate limit control, value range: 1 to 255</p> <p>Ingress Rate Limit = <math>MAN * 10^{(EXP)} * 1Kbps</math></p> <p>When IGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and</p> <p>Token Bucket = Max ( IGC_RATE_CIR*IGC_TB_T, IGC_TB_CBS*512 )</p> |

15021B04      **FPC\_RXCTRL\_P3**      Free page count at RX\_CTRL of Port 3      00000003

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18            | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2             | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    | FPC_RXCTRL_P3 |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    | RO            |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    | 0             | 1  | 1  |

| Bit(s) | Name          | Description                                         |
|--------|---------------|-----------------------------------------------------|
| 2:0    | FPC_RXCTRL_P3 | It indicates the free page count at RX_CTRL module. |

**15021B0C MMDPR\_10\_Q0P3 Drop precedence control 10 of Q0 Port 3 00000000**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  | P3_DP_en     |    |    |    |    | P3Q0_pr_dp10 |    |    |              |    |    | P3Q0_ht_dp10 |    |    |    |    |
| Type  | RW           |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset | 0            |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P3Q0_ht_dp10 |    |    |    |    |              |    |    | P3Q0_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | P3_DP_en     | <p><b>Enable Drop Precedence function of P3. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)</b></p> <p>(1) When queue depth <math>\geq</math> P3Q0_ht_dp10, the drop probability of the incoming packet is 100%.</p> <p>(2) When queue depth <math>&lt;</math> P3Q0_lt_dp10, the drop probability of the incoming packet is 0%.</p> <p>(3) When P3Q0_lt_dp10 <math>\leq</math> queue depth <math>&lt;</math> P3Q0_ht_dp10, the drop probability of incoming packet is based on the setting P3Q0_pr_dp10.</p> <p>0: Disable</p> <p>1: Enable</p> |
| 26:24  | P3Q0_pr_dp10 | <p><b>Drop probability of P3 Q0 for drop precedence = 2'b10.</b></p> <p>0x0: 0%</p> <p>0x1: 12.5%</p> <p>0xn: <math>n \times 12.5\%</math></p> <p>0x7: 87.5% (<math>n=2 \sim 6</math>)</p>                                                                                                                                                                                                                                                                                                                                                                                                          |
| 20:12  | P3Q0_ht_dp10 | <p><b>High threshold of P3 Q0 depth for drop precedence = 2'b10. Unit: page size</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 8:0    | P3Q0_lt_dp10 | <p><b>Low threshold of P3 Q0 depth for drop precedence = 2'b10. Unit: page size</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

15021B10      **MMDPR\_10\_Q1P3**      Drop precedence control 10 of Q1 Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P3Q1_pr_dp10 |    |              |    |    |    | P3Q1_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P3Q1_ht_dp10 |    |    |    |    |              |    | P3Q1_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P3Q1_pr_dp10 | <b>Drop probability of P3 Q1 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P3Q1_ht_dp10 | <b>High threshold of P3 Q1 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P3Q1_lt_dp10 | <b>Low threshold of P3 Q1 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021B14      **MMDPR\_10\_Q2P3**      Drop precedence control 10 of Q2 Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P3Q2_pr_dp10 |    |              |    |    |    | P3Q2_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P3Q2_ht_dp10 |    |    |    |    |              |    | P3Q2_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P3Q2_pr_dp10 | <b>Drop probability of P3 Q2 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P3Q2_ht_dp10 | <b>High threshold of P3 Q2 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P3Q2_lt_dp10 | <b>Low threshold of P3 Q2 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |



15021B18      **MMDPR\_10\_Q3P3**      Drop precedence control 10 of Q3 Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P3Q3_pr_dp10 |    |    |              |    |    | P3Q3_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P3Q3_ht_dp10 |    |    |    |    |              |    |    | P3Q3_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P3Q3_pr_dp10 | <b>Drop probability of P3 Q3 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P3Q3_ht_dp10 | <b>High threshold of P3 Q3 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P3Q3_lt_dp10 | <b>Low threshold of P3 Q3 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021B1C      **MMDPR\_10\_Q4P3**      Drop precedence control 10 of Q4 Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P3Q4_pr_dp10 |    |    |              |    |    | P3Q4_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P3Q4_ht_dp10 |    |    |    |    |              |    |    | P3Q4_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P3Q4_pr_dp10 | <b>Drop probability of P3 Q4 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P3Q4_ht_dp10 | <b>High threshold of P3 Q4 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P3Q4_lt_dp10 | <b>Low threshold of P3 Q4 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021B20      **MMDPR\_10\_Q5P3**      Drop precedence control 10 of Q5 Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P3Q5_pr_dp10 |    |              |    |    |    | P3Q5_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P3Q5_ht_dp10 |    |    |    |    |              |    | P3Q5_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P3Q5_pr_dp10 | <b>Drop probability of P3 Q5 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P3Q5_ht_dp10 | <b>High threshold of P3 Q5 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P3Q5_lt_dp10 | <b>Low threshold of P3 Q5 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021B24      **MMDPR\_10\_Q6P3**      Drop precedence control 10 of Q6 Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P3Q6_pr_dp10 |    |              |    |    |    | P3Q6_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P3Q6_ht_dp10 |    |    |    |    |              |    | P3Q6_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P3Q6_pr_dp10 | <b>Drop probability of P3 Q6 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P3Q6_ht_dp10 | <b>High threshold of P3 Q6 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P3Q6_lt_dp10 | <b>Low threshold of P3 Q6 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021B28      **MMDPR\_10\_Q7P3**      Drop precedence control 10 of Q7 Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P3Q7_pr_dp10 |    |              |    |    |    | P3Q7_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P3Q7_ht_dp10 |    |    |    |    |              |    | P3Q7_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P3Q7_pr_dp10 | <b>Drop probability of P3 Q7 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P3Q7_ht_dp10 | <b>High threshold of P3 Q7 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P3Q7_lt_dp10 | <b>Low threshold of P3 Q7 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

**15021B2C      MMDPR\_11\_Q0P3      Drop precedence control 11 of Q0 Port 3      00000000**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P3Q0_pr_dp11 |    |              |    |    |    | P3Q0_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P3Q0_ht_dp11 |    |    |    |    |              |    | P3Q0_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P3Q0_pr_dp11 | <b>Drop probability of P3 Q0 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P3Q0_ht_dp11 | <b>High threshold of P3 Q0 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P3Q0_lt_dp11 | <b>Low threshold of P3 Q0 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021B30      **MMDPR\_11\_Q1P3**      Drop precedence control 11 of Q1 Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P3Q1_pr_dp11 |    |              |    |    |    | P3Q1_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P3Q1_ht_dp11 |    |    |    |    |              |    | P3Q1_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P3Q1_pr_dp11 | <b>Drop probability of P3 Q1 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P3Q1_ht_dp11 | <b>High threshold of P3 Q1 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P3Q1_lt_dp11 | <b>Low threshold of P3 Q1 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021B34      **MMDPR\_11\_Q2P3**      Drop precedence control 11 of Q2 Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P3Q2_pr_dp11 |    |              |    |    |    | P3Q2_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P3Q2_ht_dp11 |    |    |    |    |              |    | P3Q2_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P3Q2_pr_dp11 | <b>Drop probability of P3 Q2 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P3Q2_ht_dp11 | <b>High threshold of P3 Q2 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P3Q2_lt_dp11 | <b>Low threshold of P3 Q2 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |



15021B38      **MMDPR\_11\_Q3P3**      Drop precedence control 11 of Q3 Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P3Q3_pr_dp11 |    |              |    |    |    | P3Q3_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P3Q3_ht_dp11 |    |    |    |    |              |    | P3Q3_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P3Q3_pr_dp11 | <b>Drop probability of P3 Q3 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P3Q3_ht_dp11 | <b>High threshold of P3 Q3 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P3Q3_lt_dp11 | <b>Low threshold of P3 Q3 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021B3C      **MMDPR\_11\_Q4P3**      Drop precedence control 11 of Q4 Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P3Q4_pr_dp11 |    |              |    |    |    | P3Q4_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P3Q4_ht_dp11 |    |    |    |    |              |    | P3Q4_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P3Q4_pr_dp11 | <b>Drop probability of P3 Q4 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P3Q4_ht_dp11 | <b>High threshold of P3 Q4 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P3Q4_lt_dp11 | <b>Low threshold of P3 Q4 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021B40      **MMDPR\_11\_Q5P3**      Drop precedence control 11 of Q5 Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P3Q5_pr_dp11 |    |              |    |    |    | P3Q5_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P3Q5_ht_dp11 |    |    |    |    |              |    | P3Q5_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P3Q5_pr_dp11 | <b>Drop probability of P3 Q5 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P3Q5_ht_dp11 | <b>High threshold of P3 Q5 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P3Q5_lt_dp11 | <b>Low threshold of P3 Q5 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021B44      **MMDPR\_11\_Q6P3**      Drop precedence control 11 of Q6 Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P3Q6_pr_dp11 |    |              |    |    |    | P3Q6_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P3Q6_ht_dp11 |    |    |    |    |              |    | P3Q6_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P3Q6_pr_dp11 | <b>Drop probability of P3 Q6 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P3Q6_ht_dp11 | <b>High threshold of P3 Q6 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P3Q6_lt_dp11 | <b>Low threshold of P3 Q6 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021B48      **MMDPR\_11\_Q7P3**      Drop precedence control 11 of Q7 Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P3Q7_pr_dp11 |    |              |    |    |    | P3Q7_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P3Q7_ht_dp11 |    |    |    |    |              |    | P3Q7_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P3Q7_pr_dp11 | <b>Drop probability of P3 Q7 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P3Q7_ht_dp11 | <b>High threshold of P3 Q7 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P3Q7_lt_dp11 | <b>Low threshold of P3 Q7 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021C00 IRLCR\_P4 Ingress rate limit control register of Port 4 00000000

| Bit   | 31                   | 30           | 29 | 28                 | 27                          | 26 | 25 | 24 | 23                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|--------------|----|--------------------|-----------------------------|----|----|----|-------------------------------|----|----|----|----|----|----|----|
| Name  | IGC_RATE_CIR_15_0_P4 |              |    |                    |                             |    |    |    |                               |    |    |    |    |    |    |    |
| Type  | RW                   |              |    |                    |                             |    |    |    |                               |    |    |    |    |    |    |    |
| Reset | 0                    | 0            | 0  | 0                  | 0                           | 0  | 0  | 0  | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14           | 13 | 12                 | 11                          | 10 | 9  | 8  | 7                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | IGC_RATE_EN_P4       | IGC_TB_EN_P4 |    | IGC_RATE_CIR_16_P4 | IGC_RATE_EXP_P4_IGC_TB_T_P4 |    |    |    | IGC_RATE_MAN_P4_IGC_TB_CBS_P4 |    |    |    |    |    |    |    |
| Type  | RW                   | RW           |    | RW                 | RW                          |    |    |    | RW                            |    |    |    |    |    |    |    |
| Reset | 0                    | 0            |    | 0                  | 0                           | 0  | 0  | 0  | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|--------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | IGC_RATE_CIR_15_0_P4        | <p>When IGC_TB_EN = 1, total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps</p> <p><math>IGC\_RATE\_CIR = [Ingress\ Rate\ Limit(bps) / 32Kbps]</math></p>                                                                                                                                                                                                                                |
| 15     | IGC_RATE_EN_P4              | <p><b>Port 4 Ingress rate limit control is enabled</b></p> <p>0: Ingress rate limit control is disabled</p> <p>1: Ingress rate limit control is enabled</p>                                                                                                                                                                                                                                                                                           |
| 14     | IGC_TB_EN_P4                | <p><b>When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.</b></p> <p>Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p>                                                                                                                      |
| 12     | IGC_RATE_CIR_16_P4          | <b>Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value</b>                                                                                                                                                                                                                                                                                                                                                                                    |
| 11:8   | IGC_RATE_EXP_P4_IGC_TB_T_P4 | <p><b>Depend on IGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b></p> <p>When IGC_TB_EN = 0, exponent part of Port 4 Ingress rate limit control, value range: 0 to 5</p> <p>0: 1Kbps</p> <p>1: 10Kbps</p> <p>2: 100Kbps</p> <p>3: 1Mbps</p> <p>4: 10Mbps</p> <p>5: 100Mbps</p> <p>When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, value range: 0 to 14</p> <p>0: 1/128ms</p> <p>1: 1/64ms</p> |

| Bit(s) | Name                          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|--------|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                               | 2: 1/32ms                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|        |                               | 3: 1/16ms                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|        |                               | 4: 1/8ms                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|        |                               | 5: 1/4ms                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|        |                               | 6: 1/2ms                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|        |                               | 7: 1ms                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|        |                               | 8: 2ms                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|        |                               | 9: 4ms                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|        |                               | 10: 8ms                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|        |                               | 11: 16ms                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|        |                               | 12: 32ms                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|        |                               | 13: 64ms                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|        |                               | 14: 128ms                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 7:0    | IGC_RATE_MAN_P4_IGC_TB_CBS_P4 | <p><b>Depend on IGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b></p> <p>When IGC_TB_EN = 0, mantissa part of Port 4 Ingress rate limit control, value range: 1 to 255</p> <p>Ingress Rate Limit = <math>MAN * 10^{(EXP)} * 1Kbps</math></p> <p>When IGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and</p> <p>Token Bucket = <math>Max ( IGC\_RATE\_CIR * IGC\_TB\_T, IGC\_TB\_CBS * 512 )</math></p> |

15021C04      **FPC\_RXCTRL\_P4**      Free page count at RX\_CTRL of Port 4      00000003

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18            | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2             | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    | FPC_RXCTRL_P4 |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    | RO            |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    | 0             | 1  | 1  |

| Bit(s) | Name          | Description                                         |
|--------|---------------|-----------------------------------------------------|
| 2:0    | FPC_RXCTRL_P4 | It indicates the free page count at RX_CTRL module. |



15021C0C MMDPR 10 Q0P4 Drop precedence control 10 of Q0 Port 4 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  | P4_DP_en     |    |    |    |    | P4Q0_pr_dp10 |    |    |              |    |    | P4Q0_ht_dp10 |    |    |    |    |
| Type  | RW           |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset | 0            |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P4Q0_ht_dp10 |    |    |    |    |              |    |    | P4Q0_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | P4_DP_en     | <p><b>Enable Drop Precedence function of P4. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)</b></p> <p>(1) When queue depth <math>\geq</math> P4Q0_ht_dp10, the drop probability of the incoming packet is 100%.</p> <p>(2) When queue depth <math>&lt;</math> P4Q0_lt_dp10, the drop probability of the incoming packet is 0%.</p> <p>(3) When P4Q0_lt_dp10 <math>\leq</math> queue depth <math>&lt;</math> P4Q0_ht_dp10, the drop probability of incoming packet is based on the setting P4Q0_pr_dp10.</p> <p>0: Disable</p> <p>1: Enable</p> |
| 26:24  | P4Q0_pr_dp10 | <p><b>Drop probability of P4 Q0 for drop precedence = 2'b10.</b></p> <p>0x0: 0%</p> <p>0x1: 12.5%</p> <p>0xn: <math>n \times 12.5\%</math></p> <p>0x7: 87.5% (<math>n=2 \sim 6</math>)</p>                                                                                                                                                                                                                                                                                                                                                                                                          |
| 20:12  | P4Q0_ht_dp10 | <p><b>High threshold of P4 Q0 depth for drop precedence = 2'b10. Unit: page size</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 8:0    | P4Q0_lt_dp10 | <p><b>Low threshold of P4 Q0 depth for drop precedence = 2'b10. Unit: page size</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

15021C10      MMDPR 10 Q1P4      Drop precedence control 10 of Q1 Port 4      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P4Q1_pr_dp10 |    |              |    |    |    | P4Q1_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P4Q1_ht_dp10 |    |    |    |    |              |    | P4Q1_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P4Q1_pr_dp10 | <b>Drop probability of P4 Q1 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P4Q1_ht_dp10 | <b>High threshold of P4 Q1 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P4Q1_lt_dp10 | <b>Low threshold of P4 Q1 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021C14      **MMDPR\_10\_Q2P4**      Drop precedence control 10 of Q2 Port 4      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P4Q2_pr_dp10 |    |    |              |    |    | P4Q2_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P4Q2_ht_dp10 |    |    |    |    |              |    |    | P4Q2_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P4Q2_pr_dp10 | <b>Drop probability of P4 Q2 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P4Q2_ht_dp10 | <b>High threshold of P4 Q2 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P4Q2_lt_dp10 | <b>Low threshold of P4 Q2 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021C18      MMDPR 10 Q3P4      Drop precedence control 10 of Q3 Port 4      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P4Q3_pr_dp10 |    |              |    |    |    | P4Q3_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P4Q3_ht_dp10 |    |    |    |    |              |    | P4Q3_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P4Q3_pr_dp10 | <b>Drop probability of P4 Q3 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P4Q3_ht_dp10 | <b>High threshold of P4 Q3 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P4Q3_lt_dp10 | <b>Low threshold of P4 Q3 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021C1C      MMDPR\_10\_Q4P4      Drop precedence control 10 of Q4 Port 4      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P4Q4_pr_dp10 |    |    |              |    |    | P4Q4_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P4Q4_ht_dp10 |    |    |    |    |              |    |    | P4Q4_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P4Q4_pr_dp10 | <b>Drop probability of P4 Q4 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P4Q4_ht_dp10 | <b>High threshold of P4 Q4 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P4Q4_lt_dp10 | <b>Low threshold of P4 Q4 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021C20      MMDPR 10 Q5P4      Drop precedence control 10 of Q5 Port 4      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P4Q5_pr_dp10 |    |    |              |    |    | P4Q5_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P4Q5_ht_dp10 |    |    |    |    |              |    |    | P4Q5_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P4Q5_pr_dp10 | <b>Drop probability of P4 Q5 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P4Q5_ht_dp10 | <b>High threshold of P4 Q5 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P4Q5_lt_dp10 | <b>Low threshold of P4 Q5 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021C24      MMDPR 10 Q6P4      Drop precedence control 10 of Q6 Port 4      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P4Q6_pr_dp10 |    |              |    |    |    | P4Q6_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P4Q6_ht_dp10 |    |    |    |    |              |    | P4Q6_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P4Q6_pr_dp10 | <b>Drop probability of P4 Q6 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P4Q6_ht_dp10 | <b>High threshold of P4 Q6 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P4Q6_lt_dp10 | <b>Low threshold of P4 Q6 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021C28      **MMDPR\_10\_Q7P4**      Drop precedence control 10 of Q7 Port 4      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P4Q7_pr_dp10 |    |    |              |    |    | P4Q7_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P4Q7_ht_dp10 |    |    |    |    |              |    |    | P4Q7_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P4Q7_pr_dp10 | <b>Drop probability of P4 Q7 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P4Q7_ht_dp10 | <b>High threshold of P4 Q7 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P4Q7_lt_dp10 | <b>Low threshold of P4 Q7 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |



15021C2C      MMDPR\_11\_Q0P4      Drop precedence control 11 of Q0 Port 4      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P4Q0_pr_dp11 |    |              |    |    |    | P4Q0_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P4Q0_ht_dp11 |    |    |    |    |              |    | P4Q0_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P4Q0_pr_dp11 | <b>Drop probability of P4 Q0 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P4Q0_ht_dp11 | <b>High threshold of P4 Q0 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P4Q0_lt_dp11 | <b>Low threshold of P4 Q0 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021C30      **MMDPR\_11\_Q1P4**      Drop precedence control 11 of Q1 Port 4      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P4Q1_pr_dp11 |    |              |    |    |    | P4Q1_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P4Q1_ht_dp11 |    |    |    |    |              |    | P4Q1_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P4Q1_pr_dp11 | <b>Drop probability of P4 Q1 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P4Q1_ht_dp11 | <b>High threshold of P4 Q1 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P4Q1_lt_dp11 | <b>Low threshold of P4 Q1 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021C34      **MMDPR\_11\_Q2P4**      Drop precedence control 11 of Q2 Port 4      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P4Q2_pr_dp11 |    |              |    |    |    | P4Q2_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P4Q2_ht_dp11 |    |    |    |    |              |    | P4Q2_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P4Q2_pr_dp11 | <b>Drop probability of P4 Q2 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P4Q2_ht_dp11 | <b>High threshold of P4 Q2 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P4Q2_lt_dp11 | <b>Low threshold of P4 Q2 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021C38      **MMDPR\_11\_Q3P4**      Drop precedence control 11 of Q3 Port 4      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P4Q3_pr_dp11 |    |              |    |    |    | P4Q3_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P4Q3_ht_dp11 |    |    |    |    |              |    | P4Q3_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P4Q3_pr_dp11 | <b>Drop probability of P4 Q3 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P4Q3_ht_dp11 | <b>High threshold of P4 Q3 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P4Q3_lt_dp11 | <b>Low threshold of P4 Q3 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021C3C      MMDPR 11 Q4P4      Drop precedence control 11 of Q4 Port 4      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P4Q4_pr_dp11 |    |              |    |    |    | P4Q4_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P4Q4_ht_dp11 |    |    |    |    |              |    | P4Q4_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P4Q4_pr_dp11 | <b>Drop probability of P4 Q4 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P4Q4_ht_dp11 | <b>High threshold of P4 Q4 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P4Q4_lt_dp11 | <b>Low threshold of P4 Q4 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021C40      **MMDPR\_11\_Q5P4**      Drop precedence control 11 of Q5 Port 4      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P4Q5_pr_dp11 |    |              |    |    |    | P4Q5_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P4Q5_ht_dp11 |    |    |    |    |              |    | P4Q5_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P4Q5_pr_dp11 | <b>Drop probability of P4 Q5 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P4Q5_ht_dp11 | <b>High threshold of P4 Q5 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P4Q5_lt_dp11 | <b>Low threshold of P4 Q5 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021C44      MMDPR\_11\_Q6P4      Drop precedence control 11 of Q6 Port 4      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P4Q6_pr_dp11 |    |              |    |    |    | P4Q6_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P4Q6_ht_dp11 |    |    |    |    |              |    | P4Q6_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                           |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P4Q6_pr_dp11 | Drop probability of P4 Q6 for drop precedence = 2'b11.<br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P4Q6_ht_dp11 | High threshold of P4 Q6 depth for drop precedence = 2'b11. Unit: page size                                                            |
| 8:0    | P4Q6_lt_dp11 | Low threshold of P4 Q6 depth for drop precedence = 2'b11. Unit: page size                                                             |

15021C48      **MMDPR\_11\_Q7P4**      Drop precedence control 11 of Q7 Port 4      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P4Q7_pr_dp11 |    |              |    |    |    | P4Q7_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P4Q7_ht_dp11 |    |    |    |    |              |    | P4Q7_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P4Q7_pr_dp11 | <b>Drop probability of P4 Q7 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P4Q7_ht_dp11 | <b>High threshold of P4 Q7 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P4Q7_lt_dp11 | <b>Low threshold of P4 Q7 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |



**15021D00 IRLCR\_P5 Ingress rate limit control register of Port 5 00000000**

| Bit          | 31                   | 30           | 29 | 28                 | 27                          | 26 | 25 | 24 | 23                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------------|--------------|----|--------------------|-----------------------------|----|----|----|-------------------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | IGC_RATE_CIR_15_0_P5 |              |    |                    |                             |    |    |    |                               |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                   |              |    |                    |                             |    |    |    |                               |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0            | 0  | 0                  | 0                           | 0  | 0  | 0  | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                   | 14           | 13 | 12                 | 11                          | 10 | 9  | 8  | 7                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | IGC_RATE_EN_P5       | IGC_TB_EN_P5 |    | IGC_RATE_CIR_16_P5 | IGC_RATE_EXP_P5_IGC_TB_T_P5 |    |    |    | IGC_RATE_MAN_P5_IGC_TB_CBS_P5 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                   | RW           |    | RW                 | RW                          |    |    |    | RW                            |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0            |    | 0                  | 0                           | 0  | 0  | 0  | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|--------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | IGC_RATE_CIR_15_0_P5        | <p>When IGC_TB_EN = 1, total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps</p> <p><math>IGC\_RATE\_CIR = [Ingress\ Rate\ Limit(bps) / 32Kbps]</math></p>                                                                                                                                                                                                                                |
| 15     | IGC_RATE_EN_P5              | <p><b>Port 5 Ingress rate limit control is enabled</b></p> <p>0: Ingress rate limit control is disabled</p> <p>1: Ingress rate limit control is enabled</p>                                                                                                                                                                                                                                                                                           |
| 14     | IGC_TB_EN_P5                | <p><b>When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.</b></p> <p>Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p>                                                                                                                      |
| 12     | IGC_RATE_CIR_16_P5          | <b>Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value</b>                                                                                                                                                                                                                                                                                                                                                                                    |
| 11:8   | IGC_RATE_EXP_P5_IGC_TB_T_P5 | <p><b>Depend on IGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b></p> <p>When IGC_TB_EN = 0, exponent part of Port 5 Ingress rate limit control, value range: 0 to 5</p> <p>0: 1Kbps</p> <p>1: 10Kbps</p> <p>2: 100Kbps</p> <p>3: 1Mbps</p> <p>4: 10Mbps</p> <p>5: 100Mbps</p> <p>When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, value range: 0 to 14</p> <p>0: 1/128ms</p> <p>1: 1/64ms</p> |

| Bit(s) | Name                          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|--------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                               | 2: 1/32ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                               | 3: 1/16ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                               | 4: 1/8ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 5: 1/4ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 6: 1/2ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 7: 1ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 8: 2ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 9: 4ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 10: 8ms                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                               | 11: 16ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 12: 32ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 13: 64ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 14: 128ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 7:0    | IGC_RATE_MAN_P5_IGC_TB_CBS_P5 | <p><b>Depend on IGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b></p> <p>When IGC_TB_EN = 0, mantissa part of Port 5 Ingress rate limit control, value range: 1 to 255</p> <p>Ingress Rate Limit = <math>MAN * 10^{(EXP)} * 1Kbps</math></p> <p>When IGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and</p> <p>Token Bucket = Max ( IGC_RATE_CIR*IGC_TB_T, IGC_TB_CBS*512 )</p> |

15021D04      **FPC\_RXCTRL\_P5**      Free page count at RX\_CTRL of Port 5      00000003

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18            | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2             | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    | FPC_RXCTRL_P5 |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    | RO            |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    | 0             | 1  | 1  |

| Bit(s) | Name          | Description                                         |
|--------|---------------|-----------------------------------------------------|
| 2:0    | FPC_RXCTRL_P5 | It indicates the free page count at RX_CTRL module. |

**15021D0C MMDPR\_10\_Q0P5 Drop precedence control 10 of Q0 Port 5 00000000**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  | P5_DP_en     |    |    |    |    | P5Q0_pr_dp10 |    |    |              |    |    | P5Q0_ht_dp10 |    |    |    |    |
| Type  | RW           |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset | 0            |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P5Q0_ht_dp10 |    |    |    |    |              |    |    | P5Q0_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | P5_DP_en     | <p><b>Enable Drop Precedence function of P5. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)</b></p> <p>(1) When queue depth <math>\geq</math> P5Q0_ht_dp10, the drop probability of the incoming packet is 100%.</p> <p>(2) When queue depth <math>&lt;</math> P5Q0_lt_dp10, the drop probability of the incoming packet is 0%.</p> <p>(3) When P5Q0_lt_dp10 <math>\leq</math> queue depth <math>&lt;</math> P5Q0_ht_dp10, the drop probability of incoming packet is based on the setting P5Q0_pr_dp10.</p> <p>0: Disable</p> <p>1: Enable</p> |
| 26:24  | P5Q0_pr_dp10 | <p><b>Drop probability of P5 Q0 for drop precedence = 2'b10.</b></p> <p>0x0: 0%</p> <p>0x1: 12.5%</p> <p>0xn: <math>n \times 12.5\%</math></p> <p>0x7: 87.5% (<math>n=2 \sim 6</math>)</p>                                                                                                                                                                                                                                                                                                                                                                                                          |
| 20:12  | P5Q0_ht_dp10 | <p><b>High threshold of P5 Q0 depth for drop precedence = 2'b10. Unit: page size</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 8:0    | P5Q0_lt_dp10 | <p><b>Low threshold of P5 Q0 depth for drop precedence = 2'b10. Unit: page size</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

15021D10      MMDPR 10 Q1P5      Drop precedence control 10 of Q1 Port 5      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P5Q1_pr_dp10 |    |              |    |    |    | P5Q1_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P5Q1_ht_dp10 |    |    |    |    |              |    | P5Q1_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P5Q1_pr_dp10 | <b>Drop probability of P5 Q1 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P5Q1_ht_dp10 | <b>High threshold of P5 Q1 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P5Q1_lt_dp10 | <b>Low threshold of P5 Q1 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021D14      MMDPR\_10\_Q2P5      Drop precedence control 10 of Q2 Port 5      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P5Q2_pr_dp10 |    |              |    |    |    | P5Q2_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P5Q2_ht_dp10 |    |    |    |    |              |    | P5Q2_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P5Q2_pr_dp10 | <b>Drop probability of P5 Q2 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P5Q2_ht_dp10 | <b>High threshold of P5 Q2 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P5Q2_lt_dp10 | <b>Low threshold of P5 Q2 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021D18      MMDPR 10 Q3P5      Drop precedence control 10 of Q3 Port 5      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P5Q3_pr_dp10 |    |    |              |    |    | P5Q3_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P5Q3_ht_dp10 |    |    |    |    |              |    |    | P5Q3_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P5Q3_pr_dp10 | <b>Drop probability of P5 Q3 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P5Q3_ht_dp10 | <b>High threshold of P5 Q3 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P5Q3_lt_dp10 | <b>Low threshold of P5 Q3 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021D1C      MMDPR 10 Q4P5      Drop precedence control 10 of Q4 Port 5      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P5Q4_pr_dp10 |    |    |              |    |    | P5Q4_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P5Q4_ht_dp10 |    |    |    |    |              |    |    | P5Q4_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P5Q4_pr_dp10 | <b>Drop probability of P5 Q4 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P5Q4_ht_dp10 | <b>High threshold of P5 Q4 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P5Q4_lt_dp10 | <b>Low threshold of P5 Q4 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |



15021D20      MMDPR\_10\_Q5P5      Drop precedence control 10 of Q5 Port 5      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P5Q5_pr_dp10 |    |    |              |    |    | P5Q5_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P5Q5_ht_dp10 |    |    |    |    |              |    |    | P5Q5_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P5Q5_pr_dp10 | <b>Drop probability of P5 Q5 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P5Q5_ht_dp10 | <b>High threshold of P5 Q5 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P5Q5_lt_dp10 | <b>Low threshold of P5 Q5 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021D24      MMDPR\_10\_Q6P5      Drop precedence control 10 of Q6 Port 5      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P5Q6_pr_dp10 |    |    |              |    |    | P5Q6_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P5Q6_ht_dp10 |    |    |    |    |              |    |    | P5Q6_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P5Q6_pr_dp10 | <b>Drop probability of P5 Q6 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P5Q6_ht_dp10 | <b>High threshold of P5 Q6 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P5Q6_lt_dp10 | <b>Low threshold of P5 Q6 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021D28      MMDPR\_10\_Q7P5      Drop precedence control 10 of Q7 Port 5      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P5Q7_pr_dp10 |    |              |    |    |    | P5Q7_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P5Q7_ht_dp10 |    |    |    |    |              |    | P5Q7_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P5Q7_pr_dp10 | <b>Drop probability of P5 Q7 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P5Q7_ht_dp10 | <b>High threshold of P5 Q7 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P5Q7_lt_dp10 | <b>Low threshold of P5 Q7 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021D2C      MMDPR\_11\_Q0P5      Drop precedence control 11 of Q0 Port 5      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P5Q0_pr_dp11 |    |              |    |    |    | P5Q0_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P5Q0_ht_dp11 |    |    |    |    |              |    | P5Q0_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P5Q0_pr_dp11 | <b>Drop probability of P5 Q0 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P5Q0_ht_dp11 | <b>High threshold of P5 Q0 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P5Q0_lt_dp11 | <b>Low threshold of P5 Q0 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021D30      **MMDPR\_11\_Q1P5**      Drop precedence control 11 of Q1 Port 5      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P5Q1_pr_dp11 |    |              |    |    |    | P5Q1_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P5Q1_ht_dp11 |    |    |    |    |              |    | P5Q1_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P5Q1_pr_dp11 | <b>Drop probability of P5 Q1 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P5Q1_ht_dp11 | <b>High threshold of P5 Q1 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P5Q1_lt_dp11 | <b>Low threshold of P5 Q1 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021D34      **MMDPR\_11\_Q2P5**      Drop precedence control 11 of Q2 Port 5      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P5Q2_pr_dp11 |    |              |    |    |    | P5Q2_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P5Q2_ht_dp11 |    |    |    |    |              |    | P5Q2_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P5Q2_pr_dp11 | <b>Drop probability of P5 Q2 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P5Q2_ht_dp11 | <b>High threshold of P5 Q2 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P5Q2_lt_dp11 | <b>Low threshold of P5 Q2 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021D38      MMDPR\_11\_Q3P5      Drop precedence control 11 of Q3 Port 5      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P5Q3_pr_dp11 |    |              |    |    |    | P5Q3_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P5Q3_ht_dp11 |    |    |    |    |              |    | P5Q3_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P5Q3_pr_dp11 | <b>Drop probability of P5 Q3 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P5Q3_ht_dp11 | <b>High threshold of P5 Q3 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P5Q3_lt_dp11 | <b>Low threshold of P5 Q3 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021D3C MMDPR\_11\_Q4P5 Drop precedence control 11 of Q4 Port 5 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P5Q4_pr_dp11 |    |              |    |    |    | P5Q4_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P5Q4_ht_dp11 |    |    |    |    |              |    | P5Q4_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                           |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P5Q4_pr_dp11 | Drop probability of P5 Q4 for drop precedence = 2'b11.<br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P5Q4_ht_dp11 | High threshold of P5 Q4 depth for drop precedence = 2'b11. Unit: page size                                                            |
| 8:0    | P5Q4_lt_dp11 | Low threshold of P5 Q4 depth for drop precedence = 2'b11. Unit: page size                                                             |



15021D40      MMDPR\_11\_Q5P5      Drop precedence control 11 of Q5 Port 5      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P5Q5_pr_dp11 |    |              |    |    |    | P5Q5_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P5Q5_ht_dp11 |    |    |    |    |              |    | P5Q5_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P5Q5_pr_dp11 | <b>Drop probability of P5 Q5 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P5Q5_ht_dp11 | <b>High threshold of P5 Q5 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P5Q5_lt_dp11 | <b>Low threshold of P5 Q5 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021D44      **MMDPR\_11\_Q6P5**      Drop precedence control 11 of Q6 Port 5      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P5Q6_pr_dp11 |    |              |    |    |    | P5Q6_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P5Q6_ht_dp11 |    |    |    |    |              |    | P5Q6_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                           |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P5Q6_pr_dp11 | Drop probability of P5 Q6 for drop precedence = 2'b11.<br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P5Q6_ht_dp11 | High threshold of P5 Q6 depth for drop precedence = 2'b11. Unit: page size                                                            |
| 8:0    | P5Q6_lt_dp11 | Low threshold of P5 Q6 depth for drop precedence = 2'b11. Unit: page size                                                             |

15021D48      **MMDPR\_11\_Q7P5**      Drop precedence control 11 of Q7 Port 5      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P5Q7_pr_dp11 |    |              |    |    |    | P5Q7_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P5Q7_ht_dp11 |    |    |    |    |              |    | P5Q7_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P5Q7_pr_dp11 | <b>Drop probability of P5 Q7 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P5Q7_ht_dp11 | <b>High threshold of P5 Q7 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P5Q7_lt_dp11 | <b>Low threshold of P5 Q7 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

**15021E00 IRLCR\_P6 Ingress rate limit control register of Port 6 00000000**

| Bit          | 31                   | 30           | 29 | 28                 | 27                          | 26 | 25 | 24 | 23                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------------|--------------|----|--------------------|-----------------------------|----|----|----|-------------------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | IGC_RATE_CIR_15_0_P6 |              |    |                    |                             |    |    |    |                               |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                   |              |    |                    |                             |    |    |    |                               |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0            | 0  | 0                  | 0                           | 0  | 0  | 0  | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                   | 14           | 13 | 12                 | 11                          | 10 | 9  | 8  | 7                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | IGC_RATE_EN_P6       | IGC_TB_EN_P6 |    | IGC_RATE_CIR_16_P6 | IGC_RATE_EXP_P6_IGC_TB_T_P6 |    |    |    | IGC_RATE_MAN_P6_IGC_TB_CBS_P6 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                   | RW           |    | RW                 | RW                          |    |    |    | RW                            |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0            |    | 0                  | 0                           | 0  | 0  | 0  | 0                             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|--------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | IGC_RATE_CIR_15_0_P6        | <p>When IGC_TB_EN = 1, total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps</p> <p><math>IGC\_RATE\_CIR = [Ingress\ Rate\ Limit(bps) / 32Kbps]</math></p>                                                                                                                                                                                                                                |
| 15     | IGC_RATE_EN_P6              | <p><b>Port 6 Ingress rate limit control is enabled</b></p> <p>0: Ingress rate limit control is disabled</p> <p>1: Ingress rate limit control is enabled</p>                                                                                                                                                                                                                                                                                           |
| 14     | IGC_TB_EN_P6                | <p><b>When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.</b></p> <p>Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction.</p> <p>0: CIR/CBS mode token bucket disable</p> <p>1: Token bucket mode enable</p>                                                                                                                      |
| 12     | IGC_RATE_CIR_16_P6          | <b>Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value</b>                                                                                                                                                                                                                                                                                                                                                                                    |
| 11:8   | IGC_RATE_EXP_P6_IGC_TB_T_P6 | <p><b>Depend on IGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket</b></p> <p>When IGC_TB_EN = 0, exponent part of Port 6 Ingress rate limit control, value range: 0 to 5</p> <p>0: 1Kbps</p> <p>1: 10Kbps</p> <p>2: 100Kbps</p> <p>3: 1Mbps</p> <p>4: 10Mbps</p> <p>5: 100Mbps</p> <p>When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, value range: 0 to 14</p> <p>0: 1/128ms</p> <p>1: 1/64ms</p> |

| Bit(s) | Name                          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|--------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                               | 2: 1/32ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                               | 3: 1/16ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |                               | 4: 1/8ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 5: 1/4ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 6: 1/2ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 7: 1ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 8: 2ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 9: 4ms                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |                               | 10: 8ms                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|        |                               | 11: 16ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 12: 32ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 13: 64ms                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|        |                               | 14: 128ms                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 7:0    | IGC_RATE_MAN_P6_IGC_TB_CBS_P6 | <p><b>Depend on IGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket</b></p> <p>When IGC_TB_EN = 0, mantissa part of Port 6 Ingress rate limit control, value range: 1 to 255</p> <p>Ingress Rate Limit = <math>MAN * 10^{(EXP)} * 1Kbps</math></p> <p>When IGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and</p> <p>Token Bucket = Max ( IGC_RATE_CIR*IGC_TB_T, IGC_TB_CBS*512 )</p> |

15021E04      FPC\_RXCTRL\_P6      Free page count at RX\_CTRL of Port 6      00000003

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18            | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2             | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    | FPC_RXCTRL_P6 |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    | RO            |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    | 0             | 1  | 1  |

| Bit(s) | Name          | Description                                         |
|--------|---------------|-----------------------------------------------------|
| 2:0    | FPC_RXCTRL_P6 | It indicates the free page count at RX_CTRL module. |

15021E0C MMDPR\_10\_Q0P6 Drop precedence control 10 of Q0 Port 6 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  | P6_DP_en     |    |    |    |    | P6Q0_pr_dp10 |    |    |              |    |    | P6Q0_ht_dp10 |    |    |    |    |
| Type  | RW           |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset | 0            |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P6Q0_ht_dp10 |    |    |    |    |              |    |    | P6Q0_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | P6_DP_en     | <p><b>Enable Drop Precedence function of P6. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)</b></p> <p>(1) When queue depth <math>\geq</math> P6Q0_ht_dp10, the drop probability of the incoming packet is 100%.</p> <p>(2) When queue depth <math>&lt;</math> P6Q0_lt_dp10, the drop probability of the incoming packet is 0%.</p> <p>(3) When P6Q0_lt_dp10 <math>\leq</math> queue depth <math>&lt;</math> P6Q0_ht_dp10, the drop probability of incoming packet is based on the setting P6Q0_pr_dp10.</p> <p>0: Disable</p> <p>1: Enable</p> |
| 26:24  | P6Q0_pr_dp10 | <p><b>Drop probability of P6 Q0 for drop precedence = 2'b10.</b></p> <p>0x0: 0%</p> <p>0x1: 12.5%</p> <p>0xn: <math>n \times 12.5\%</math></p> <p>0x7: 87.5% (<math>n=2 \sim 6</math>)</p>                                                                                                                                                                                                                                                                                                                                                                                                          |
| 20:12  | P6Q0_ht_dp10 | <p><b>High threshold of P6 Q0 depth for drop precedence = 2'b10. Unit: page size</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 8:0    | P6Q0_lt_dp10 | <p><b>Low threshold of P6 Q0 depth for drop precedence = 2'b10. Unit: page size</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

15021E10      MMDPR 10 Q1P6      Drop precedence control 10 of Q1 Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P6Q1_pr_dp10 |    |              |    |    |    | P6Q1_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P6Q1_ht_dp10 |    |    |    |    |              |    | P6Q1_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P6Q1_pr_dp10 | <b>Drop probability of P6 Q1 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P6Q1_ht_dp10 | <b>High threshold of P6 Q1 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P6Q1_lt_dp10 | <b>Low threshold of P6 Q1 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |



15021E14      **MMDPR\_10\_Q2P6**      Drop precedence control 10 of Q2 Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P6Q2_pr_dp10 |    |              |    |    |    | P6Q2_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P6Q2_ht_dp10 |    |    |    |    |              |    | P6Q2_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P6Q2_pr_dp10 | <b>Drop probability of P6 Q2 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P6Q2_ht_dp10 | <b>High threshold of P6 Q2 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P6Q2_lt_dp10 | <b>Low threshold of P6 Q2 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021E18      **MMDPR\_10\_Q3P6**      Drop precedence control 10 of Q3 Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P6Q3_pr_dp10 |    |              |    |    |    | P6Q3_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P6Q3_ht_dp10 |    |    |    |    |              |    | P6Q3_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P6Q3_pr_dp10 | <b>Drop probability of P6 Q3 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P6Q3_ht_dp10 | <b>High threshold of P6 Q3 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P6Q3_lt_dp10 | <b>Low threshold of P6 Q3 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021E1C      **MMDPR 10 Q4P6**      Drop precedence control 10 of Q4 Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P6Q4_pr_dp10 |    |              |    |    |    | P6Q4_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P6Q4_ht_dp10 |    |    |    |    |              |    | P6Q4_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P6Q4_pr_dp10 | <b>Drop probability of P6 Q4 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P6Q4_ht_dp10 | <b>High threshold of P6 Q4 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P6Q4_lt_dp10 | <b>Low threshold of P6 Q4 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021E20      MMDPR\_10\_Q5P6      Drop precedence control 10 of Q5 Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P6Q5_pr_dp10 |    |              |    |    |    | P6Q5_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P6Q5_ht_dp10 |    |    |    |    |              |    | P6Q5_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P6Q5_pr_dp10 | <b>Drop probability of P6 Q5 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P6Q5_ht_dp10 | <b>High threshold of P6 Q5 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P6Q5_lt_dp10 | <b>Low threshold of P6 Q5 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021E24      **MMDPR\_10\_Q6P6**      Drop precedence control 10 of Q6 Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P6Q6_pr_dp10 |    |              |    |    |    | P6Q6_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P6Q6_ht_dp10 |    |    |    |    |              |    | P6Q6_lt_dp10 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P6Q6_pr_dp10 | <b>Drop probability of P6 Q6 for drop precedence = 2'b10.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P6Q6_ht_dp10 | <b>High threshold of P6 Q6 depth for drop precedence = 2'b10. Unit: page size</b>                                                            |
| 8:0    | P6Q6_lt_dp10 | <b>Low threshold of P6 Q6 depth for drop precedence = 2'b10. Unit: page size</b>                                                             |

15021E28      MMDPR\_10\_Q7P6      Drop precedence control 10 of Q7 Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24 | 23           | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|----|--------------|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P6Q7_pr_dp10 |    |    |              |    |    | P6Q7_ht_dp10 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |    |              |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0  |              |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8  | 7            | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P6Q7_ht_dp10 |    |    |    |    |              |    |    | P6Q7_lt_dp10 |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    |    | RW           |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0  | 0            | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                           |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P6Q7_pr_dp10 | Drop probability of P6 Q7 for drop precedence = 2'b10.<br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P6Q7_ht_dp10 | High threshold of P6 Q7 depth for drop precedence = 2'b10. Unit: page size                                                            |
| 8:0    | P6Q7_lt_dp10 | Low threshold of P6 Q7 depth for drop precedence = 2'b10. Unit: page size                                                             |

15021E2C      MMDPR\_11\_Q0P6      Drop precedence control 11 of Q0 Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P6Q0_pr_dp11 |    |              |    |    |    | P6Q0_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P6Q0_ht_dp11 |    |    |    |    |              |    | P6Q0_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P6Q0_pr_dp11 | <b>Drop probability of P6 Q0 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P6Q0_ht_dp11 | <b>High threshold of P6 Q0 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P6Q0_lt_dp11 | <b>Low threshold of P6 Q0 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021E30      MMDPR\_11\_Q1P6      Drop precedence control 11 of Q1 Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P6Q1_pr_dp11 |    |              |    |    |    | P6Q1_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P6Q1_ht_dp11 |    |    |    |    |              |    | P6Q1_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P6Q1_pr_dp11 | <b>Drop probability of P6 Q1 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P6Q1_ht_dp11 | <b>High threshold of P6 Q1 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P6Q1_lt_dp11 | <b>Low threshold of P6 Q1 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |



15021E34      **MMDPR\_11\_Q2P6**      Drop precedence control 11 of Q2 Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P6Q2_pr_dp11 |    |              |    |    |    | P6Q2_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P6Q2_ht_dp11 |    |    |    |    |              |    | P6Q2_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P6Q2_pr_dp11 | <b>Drop probability of P6 Q2 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P6Q2_ht_dp11 | <b>High threshold of P6 Q2 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P6Q2_lt_dp11 | <b>Low threshold of P6 Q2 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021E38      **MMDPR\_11\_Q3P6**      Drop precedence control 11 of Q3 Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P6Q3_pr_dp11 |    |              |    |    |    | P6Q3_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P6Q3_ht_dp11 |    |    |    |    |              |    | P6Q3_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P6Q3_pr_dp11 | <b>Drop probability of P6 Q3 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P6Q3_ht_dp11 | <b>High threshold of P6 Q3 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P6Q3_lt_dp11 | <b>Low threshold of P6 Q3 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021E3C      **MMDPR\_11\_Q4P6**      Drop precedence control 11 of Q4 Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P6Q4_pr_dp11 |    |              |    |    |    | P6Q4_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P6Q4_ht_dp11 |    |    |    |    |              |    | P6Q4_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P6Q4_pr_dp11 | <b>Drop probability of P6 Q4 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P6Q4_ht_dp11 | <b>High threshold of P6 Q4 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P6Q4_lt_dp11 | <b>Low threshold of P6 Q4 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021E40      MMDPR\_11\_Q5P6      Drop precedence control 11 of Q5 Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P6Q5_pr_dp11 |    |              |    |    |    | P6Q5_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P6Q5_ht_dp11 |    |    |    |    |              |    | P6Q5_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                           |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P6Q5_pr_dp11 | Drop probability of P6 Q5 for drop precedence = 2'b11.<br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P6Q5_ht_dp11 | High threshold of P6 Q5 depth for drop precedence = 2'b11. Unit: page size                                                            |
| 8:0    | P6Q5_lt_dp11 | Low threshold of P6 Q5 depth for drop precedence = 2'b11. Unit: page size                                                             |

15021E44      **MMDPR\_11\_Q6P6**      Drop precedence control 11 of Q6 Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P6Q6_pr_dp11 |    |              |    |    |    | P6Q6_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P6Q6_ht_dp11 |    |    |    |    |              |    | P6Q6_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P6Q6_pr_dp11 | <b>Drop probability of P6 Q6 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P6Q6_ht_dp11 | <b>High threshold of P6 Q6 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P6Q6_lt_dp11 | <b>Low threshold of P6 Q6 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

15021E48      **MMDPR\_11\_Q7P6**      Drop precedence control 11 of Q7 Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26           | 25 | 24           | 23 | 22 | 21 | 20           | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|--------------|----|--------------|----|----|----|--------------|----|----|----|----|
| Name  |              |    |    |    |    | P6Q7_pr_dp11 |    |              |    |    |    | P6Q7_ht_dp11 |    |    |    |    |
| Type  |              |    |    |    |    | RW           |    |              |    |    |    | RW           |    |    |    |    |
| Reset |              |    |    |    |    | 0            | 0  | 0            |    |    |    | 0            | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10           | 9  | 8            | 7  | 6  | 5  | 4            | 3  | 2  | 1  | 0  |
| Name  | P6Q7_ht_dp11 |    |    |    |    |              |    | P6Q7_lt_dp11 |    |    |    |              |    |    |    |    |
| Type  | RW           |    |    |    |    |              |    | RW           |    |    |    |              |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  |    |              |    | 0            | 0  | 0  | 0  | 0            | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 26:24  | P6Q7_pr_dp11 | <b>Drop probability of P6 Q7 for drop precedence = 2'b11.</b><br><br>0x0: 0%<br><br>0x1: 12.5%<br><br>0xn: n* 12.5%<br><br>0x7: 87.5%(n=2~6) |
| 20:12  | P6Q7_ht_dp11 | <b>High threshold of P6 Q7 depth for drop precedence = 2'b11. Unit: page size</b>                                                            |
| 8:0    | P6Q7_lt_dp11 | <b>Low threshold of P6 Q7 depth for drop precedence = 2'b11. Unit: page size</b>                                                             |

**15021FC0      FPLC      Free page Link count register      OFFF0600**

| Bit          | 31 | 30 | 29 | 28 | 27                     | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----|----|----|----|------------------------|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  |    |    |    |    | <b>MIN_FREE_PL_CNT</b> |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  |    |    |    |    | RO                     |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> |    |    |    |    | 1                      | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit          | 15 | 14 | 13 | 12 | 11                     | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  |    |    |    |    | <b>FREE_PL_CNT</b>     |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  |    |    |    |    | RO                     |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> |    |    |    |    | 0                      | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                               |
|--------|-----------------|-----------------------------------------------------------|
| 27:16  | MIN_FREE_PL_CNT | Minimal Free Page Link Count in LMU from last read access |
| 11:0   | FREE_PL_CNT     | Free Page Link Count in LMU                               |

**15021FE0      GFCCRO      Global Flow\_Control control register 0      20F000B0**

| Bit   | 31 | 30 | 29            | 28            | 27 | 26 | 25                | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|---------------|---------------|----|----|-------------------|----|----|----|----|----|----|----|----|----|
| Name  |    |    | FC_OFF2ON_OPT | FC_ON2OFF_OPT |    |    | FC_FREE_BLK_HITHD |    |    |    |    |    |    |    |    |    |
| Type  |    |    | RW            | RW            |    |    | RW                |    |    |    |    |    |    |    |    |    |
| Reset |    |    | 1             | 0             |    |    | 0                 | 0  | 1  | 1  | 1  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13            | 12            | 11 | 10 | 9                 | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |               |               |    |    | FC_FREE_BLK_LOTHD |    |    |    |    |    |    |    |    |    |
| Type  |    |    |               |               |    |    | RW                |    |    |    |    |    |    |    |    |    |
| Reset |    |    |               |               |    |    | 0                 | 0  | 1  | 0  | 1  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                                                                                                                          |
|--------|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29     | FC_OFF2ON_OPT     | <b>Flow control assertion option</b><br><br>0: Disable<br><br>1: Enable aggressive frame discard option in flow control transition from OFF to ON    |
| 28     | FC_ON2OFF_OPT     | <b>Flow control de-assertion option</b><br><br>0: Disable<br><br>1: Enable aggressive frame discard option in flow control transition from ON to OFF |
| 25:16  | FC_FREE_BLK_HITHD | <b>High water mark of memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block)</b> |
| 9:0    | FC_FREE_BLK_LOTHD | <b>Low water mark of memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block)</b>  |



**15021FE4      GFCCR1      Global Flow\_Control control register 1      00120008**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25                 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    |    | FC_PORT_BLK_HI_THD |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    |    | 0                  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9                  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    |    | FC_PORT_BLK_THD    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    |    | 0                  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                         |
|--------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 25:16  | FC_PORT_BLK_HI_THD | Number of port block high threshold (unit: 2 blocks) associated with packet discard mechanism                                       |
| 9:0    | FC_PORT_BLK_THD    | Per port memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block) |

**15021FE8      GFCCR2      Global Flow\_Control control register 2      04040404**

| Bit   | 31 | 30 | 29            | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21            | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|---------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|
| Name  |    |    | FC_BLK_THD_Q3 |    |    |    |    |    |    |    | FC_BLK_THD_Q2 |    |    |    |    |    |
| Type  |    |    | RW            |    |    |    |    |    |    |    | RW            |    |    |    |    |    |
| Reset |    |    | 0             | 0  | 0  | 1  | 0  | 0  |    |    | 0             | 0  | 0  | 1  | 0  | 0  |
| Bit   | 15 | 14 | 13            | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5             | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    | FC_BLK_THD_Q1 |    |    |    |    |    |    |    | FC_BLK_THD_Q0 |    |    |    |    |    |
| Type  |    |    | RW            |    |    |    |    |    |    |    | RW            |    |    |    |    |    |
| Reset |    |    | 0             | 0  | 0  | 1  | 0  | 0  |    |    | 0             | 0  | 0  | 1  | 0  | 0  |

| Bit(s) | Name          | Description                                 |
|--------|---------------|---------------------------------------------|
| 29:24  | FC_BLK_THD_Q3 | TX Queue 3 block threshold for flow control |
| 21:16  | FC_BLK_THD_Q2 | TX Queue 2 block threshold for flow control |
| 13:8   | FC_BLK_THD_Q1 | TX Queue 1 block threshold for flow control |
| 5:0    | FC_BLK_THD_Q0 | TX Queue 0 block threshold for flow control |

**15021FEC      GFCCR3      Global Flow\_Control control register 3      04040404**

| Bit   | 31 | 30 | 29            | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20            | 19 | 18 | 17 | 16 |
|-------|----|----|---------------|----|----|----|----|----|----|----|----|---------------|----|----|----|----|
| Name  |    |    | FC_BLK_THD_Q7 |    |    |    |    |    |    |    |    | FC_BLK_THD_Q6 |    |    |    |    |
| Type  |    |    | RW            |    |    |    |    |    |    |    |    | RW            |    |    |    |    |
| Reset |    |    | 0             | 0  | 0  | 1  | 0  | 0  |    |    | 0  | 0             | 0  | 1  | 0  | 0  |
| Bit   | 15 | 14 | 13            | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4             | 3  | 2  | 1  | 0  |
| Name  |    |    | FC_BLK_THD_Q5 |    |    |    |    |    |    |    |    | FC_BLK_THD_Q4 |    |    |    |    |
| Type  |    |    | RW            |    |    |    |    |    |    |    |    | RW            |    |    |    |    |
| Reset |    |    | 0             | 0  | 0  | 1  | 0  | 0  |    |    | 0  | 0             | 0  | 1  | 0  | 0  |

| Bit(s) | Name          | Description                                 |
|--------|---------------|---------------------------------------------|
| 29:24  | FC_BLK_THD_Q7 | TX Queue 7 block threshold for flow control |
| 21:16  | FC_BLK_THD_Q6 | TX Queue 6 block threshold for flow control |
| 13:8   | FC_BLK_THD_Q5 | TX Queue 5 block threshold for flow control |
| 5:0    | FC_BLK_THD_Q4 | TX Queue 4 block threshold for flow control |

**15021FF0      GFCCR4      Global Flow\_Control control register 4      0000000C**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25                | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    |    |                   |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    |    |                   |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    |    |                   |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9                 | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    |    | FC_QUE_BLK_HI_THD |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    |    | 0                 | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  |

| Bit(s) | Name              | Description                                                                                    |
|--------|-------------------|------------------------------------------------------------------------------------------------|
| 9:0    | FC_QUE_BLK_HI_THD | Number of queue block high threshold (unit: 2 blocks) associated with packet discard mechanism |

15021FF4

FCBRCR0

Flow control block reservation control register  
for group 0

00000000

| Bit   | 31             | 30 | 29 | 28 | 27                  | 26 | 25 | 24 | 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|---------------------|----|----|----|------------------|----|----|----|----|----|----|----|
| Name  | FC_RSV_GRP0_EN |    |    |    |                     |    |    |    | FC_RSV_GRP0_PMAP |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |                     |    |    |    | RW               |    |    |    |    |    |    |    |
| Reset | 0              |    |    |    |                     |    |    |    | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11                  | 10 | 9  | 8  | 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |                |    |    |    | FC_RSV_GRP0_BLK_NUM |    |    |    | FC_RSV_GRP0_QMAP |    |    |    |    |    |    |    |
| Type  |                |    |    |    | RW                  |    |    |    | RW               |    |    |    |    |    |    |    |
| Reset |                |    |    |    | 0                   | 0  | 0  | 0  | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                             |
|--------|---------------------|-------------------------------------------------------------------------------------------------------------------------|
| 31     | FC_RSV_GRP0_EN      | <p><b>Enable queue block reservation group 0</b></p> <p>0: Disable</p> <p>1: Enable queue block reservation group 0</p> |
| 23:16  | FC_RSV_GRP0_PMAP    | <p><b>When FC_RSV_GRP0_EN=1,</b></p> <p>Port map for queue block reservation group 0</p> <p>Note: assume 8 port</p>     |
| 11:8   | FC_RSV_GRP0_BLK_NUM | <p><b>When FC_RSV_GRP0_EN=1,</b></p> <p>Block size for queue block reservation group 0</p>                              |
| 7:0    | FC_RSV_GRP0_QMAP    | <p><b>When FC_RSV_GRP0_EN=1,</b></p> <p>Queue map for queue block reservation group 0</p>                               |

15021FF8

FCBRCR1Flow control block reservation control register  
for group 1

00000000

| Bit   | 31             | 30 | 29 | 28 | 27                  | 26 | 25 | 24 | 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|---------------------|----|----|----|------------------|----|----|----|----|----|----|----|
| Name  | FC_RSV_GRP1_EN |    |    |    |                     |    |    |    | FC_RSV_GRP1_PMAP |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |                     |    |    |    | RW               |    |    |    |    |    |    |    |
| Reset | 0              |    |    |    |                     |    |    |    | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11                  | 10 | 9  | 8  | 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |                |    |    |    | FC_RSV_GRP1_BLK_NUM |    |    |    | FC_RSV_GRP1_QMAP |    |    |    |    |    |    |    |
| Type  |                |    |    |    | RW                  |    |    |    | RW               |    |    |    |    |    |    |    |
| Reset |                |    |    |    | 0                   | 0  | 0  | 0  | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                      |
|--------|---------------------|------------------------------------------------------------------------------------------------------------------|
| 31     | FC_RSV_GRP1_EN      | <b>Enable queue block reservation group 0</b><br><br>0: Disable<br><br>1: Enable queue block reservation group 0 |
| 23:16  | FC_RSV_GRP1_PMAP    | <b>When FC_RSV_GRP1_EN=1,</b><br><br>Port map for queue block reservation group 1<br><br>Note: assume 8 port     |
| 11:8   | FC_RSV_GRP1_BLK_NUM | <b>When FC_RSV_GRP1_EN=1,</b><br><br>Block size for queue block reservation group 1                              |
| 7:0    | FC_RSV_GRP1_QMAP    | <b>When FC_RSV_GRP1_EN=1,</b><br><br>Queue map for queue block reservation group 1                               |

**15021FFC**      **GIRLCR**      **Global ingress rate limit control register**      **00110118**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25          | 24         | 23             | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|-------------|------------|----------------|----|----|----|-----------------|----|----|----|
| Name  |    |    |    |    |    |    |             |            | IGC_FC_OFF_THD |    |    |    | IGC_FC_DROP_THD |    |    |    |
| Type  |    |    |    |    |    |    |             |            | RW             |    |    |    | RW              |    |    |    |
| Reset |    |    |    |    |    |    |             |            | 0              | 0  | 0  | 1  | 0               | 0  | 0  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9           | 8          | 7              | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| Name  |    |    |    |    |    |    | IGC_MFRM_EX | IGC_IPG_OP | IGC_IPG_BYTE   |    |    |    |                 |    |    |    |
| Type  |    |    |    |    |    |    | RW          | RW         | RW             |    |    |    |                 |    |    |    |
| Reset |    |    |    |    |    |    | 0           | 1          | 0              | 0  | 0  | 1  | 1               | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                    |
|--------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:20  | IGC_FC_OFF_THD  | <b>Ingress Rate Limit Pause-Off Threshold</b><br><br>Pause-off frame is sent when the ingress token bucket is higher than pause-off threshold.<br><br>Threshold = max_bucket_size >> igc_fc_off_thd                                            |
| 19:16  | IGC_FC_DROP_THD | <b>Ingress Rate Limit Drop Threshold</b><br><br>If Port Flow Control and rate limit control is enabled, frame is drop when the ingress token bucket is less than drop threshold.<br><br>Threshold = -(max_bucket_size >> igc_fc_drop_thd)      |
| 9      | IGC_MFRM_EX     | <b>Ingress Rate Excludes Management Frames</b><br><br>Management frames will be ignored by rate limit.<br>(management frame type is set by ARL registers)<br><br>0: Include management frames<br><br>1: Exclude management frames              |
| 8      | IGC_IPG_OP      | <b>Ingress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted on the rate calculation.</b><br><br>0: IPG byte is excluded<br><br>1: IPG byte is included                                                           |
| 7:0    | IGC_IPG_BYTE    | <b>Ingress Rate IPG Byte Count</b><br><br>Byte count should be added while calculating the rate limit<br><br>8'h4: add 4-byte CRC (byte rate calculation)<br><br>8'h18: add 4-byte CRC + 8 byte Preamble + 12 byte IPG (line rate calculation) |

15022000      P0\_SSC      STP state control of P0      0000FFFF

| Bit   | 31       | 30 | 29       | 28 | 27       | 26 | 25       | 24 | 23       | 22 | 21       | 20 | 19       | 18 | 17       | 16 |
|-------|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|
| Name  | REVO     |    |          |    |          |    |          |    |          |    |          |    |          |    |          |    |
| Type  | RO       |    |          |    |          |    |          |    |          |    |          |    |          |    |          |    |
| Reset | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  |
| Bit   | 15       | 14 | 13       | 12 | 11       | 10 | 9        | 8  | 7        | 6  | 5        | 4  | 3        | 2  | 1        | 0  |
| Name  | FID7_PST |    | FID6_PST |    | FID5_PST |    | FID4_PST |    | FID3_PST |    | FID2_PST |    | FID1_PST |    | FID0_PST |    |
| Type  | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    |
| Reset | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  |

| Bit(s) | Name     | Description                                                                                                                                                                                                                    |
|--------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | REVO     | <b>Reserved</b>                                                                                                                                                                                                                |
| 15:14  | FID7_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 13:12  | FID6_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 11:10  | FID5_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 9:8    | FID4_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 7:6    | FID3_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)                                                |



| Bit(s) | Name     | Description                                      |
|--------|----------|--------------------------------------------------|
| 5:4    | FID2_PST | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |
|        |          | <b>(Rapid) Spanning Tree Protocol Port State</b> |
|        |          | 2'b00: Disable (STP) / Discard (RSTP)            |
|        |          | 2'b01: Listening (STP) / Discard (RSTP)          |
|        |          | 2'b10: Learning (STP) / Learning (RSTP)          |
| 3:2    | FID1_PST | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |
|        |          | <b>(Rapid) Spanning Tree Protocol Port State</b> |
|        |          | 2'b00: Disable (STP) / Discard (RSTP)            |
|        |          | 2'b01: Listening (STP) / Discard (RSTP)          |
|        |          | 2'b10: Learning (STP) / Learning (RSTP)          |
| 1:0    | FID0_PST | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |
|        |          | <b>(Rapid) Spanning Tree Protocol Port State</b> |
|        |          | 2'b00: Disable (STP) / Discard (RSTP)            |
|        |          | 2'b01: Listening (STP) / Discard (RSTP)          |
|        |          | 2'b10: Learning (STP) / Learning (RSTP)          |
|        |          | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |

15022004      **P0\_PCR**      Port control of P0      00FF2000

| Bit   | 31   | 30       | 29     | 28         | 27        | 26       | 25         | 24         | 23          | 22          | 21 | 20 | 19   | 18       | 17        | 16 |
|-------|------|----------|--------|------------|-----------|----------|------------|------------|-------------|-------------|----|----|------|----------|-----------|----|
| Name  | REV0 | MLDv2_EN | EG_TAG |            | REV1      | PORT_PRI |            |            | PORT_MATRIX |             |    |    |      |          |           |    |
| Type  | RW   | RW       | RW     |            | RW        | RW       |            |            | RW          |             |    |    |      |          |           |    |
| Reset | 0    | 0        | 0      | 0          | 0         | 0        | 0          | 0          | 1           | 1           | 1  | 1  | 1    | 1        | 1         | 1  |
| Bit   | 15   | 14       | 13     | 12         | 11        | 10       | 9          | 8          | 7           | 6           | 5  | 4  | 3    | 2        | 1         | 0  |
| Name  | REV2 |          |        | UP2DSCP_EN | UP2TAG_EN | ACL_EN   | PORT_TX_MR | PORT_RX_MR | ACL_MR      | MIS_PORT_FW |    |    | REV3 | VLAN_MIS | PORT_VLAN |    |
| Type  | RW   |          |        | RW         | RW        | RW       | RW         | RW         | RW          | RW          |    |    | RW   | RW       | RW        |    |
| Reset | 0    | 0        | 1      | 0          | 0         | 0        | 0          | 0          | 0           | 0           | 0  | 0  | 0    | 0        | 0         | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                     |
|--------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | REV0        | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 30     | MLDv2_EN    | <b>IPv6 MLDv2 source address multicast forwarding enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                 |
| 29:28  | EG_TAG      | <b>Port-Based Egress VLAN Tag Attribution</b><br><br>2'b00: Untagged<br><br>2'b01: Swap<br><br>2'b10: Tagged<br><br>2'b11: Stack                                                                                                                                                |
| 27     | REV1        | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 26:24  | PORT_PRI    | <b>Port-based User Priority</b><br><br>User priority for the ingress port                                                                                                                                                                                                       |
| 23:16  | PORT_MATRIX | <b>Port Matrix Member</b><br><br>The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member.<br><br>NOTE: The final and effective port member should exclude the received port. |
| 15:13  | REV2        | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 12     | UP2DSCP_EN  | <b>User Priority to DSCP Enable</b><br><br>Replace DSCP according to user priority.<br><br>0: Disable<br><br>1: Enable                                                                                                                                                          |
| 11     | UP2TAG_EN   | <b>User Priority to Tag Enable</b><br><br>Replace 802.Q priority by user priority.                                                                                                                                                                                              |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |             | 0: Disable                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |             | 1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 10     | ACL_EN      | <b>Port-based ACL Enable</b><br>0: Bypass the ACL Table.<br>1: Look up the ACL Table and take corresponding actions.                                                                                                                                                                                                                                                                                                                           |
| 9      | PORT_TX_MIR | <b>Port Tx Mirror Enable</b><br>All frames transmitted from this port are copied to the mirror port.<br>[NOTE] Multi-port support is possible.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                      |
| 8      | PORT_RX_MIR | <b>Port Rx Mirror Enable</b><br>All frames received from this port are copied to the mirror port.<br>[NOTE] Multi-port support is possible.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                         |
| 7      | ACL_MIR     | <b>ACL Mismatch to Mirror Port</b><br>Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                     |
| 6:4    | MIS_PORT_FW | <b>ACL Mismatch TO_CPU Forward</b><br>Frame port forwarding when ACL table is enabled and the frame is mismatched<br>3'b0xx: System default (disabled)<br>3'b100: System default and CPU port excluded<br>3'b101: System default and CPU port included<br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.)<br>3'b111: Frame dropped |
| 3      | REV3        | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 2      | VLAN_MIS    | <b>VLAN Mismatch to Mirror Port</b><br>1'b0: Frame is processed according to PORT_VLAN.<br>1'b1: VLAN mismatched frame is copied to MIRROR port.                                                                                                                                                                                                                                                                                               |

| Bit(s) | Name      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0    | PORT_VLAN | <b>Port-based VLAN Mechanism Select</b><br><br>2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member.<br><br>2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member.<br><br>2'b10: Check Mode. Forward received frames whose ingress port do not belong to the VLAN member. Discard frames if VID is missed on the VLAN table.<br><br>2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table. |

15022008      P0\_PIC      Port IGMP control of P0      00008000

| Bit   | 31         | 30 | 29           | 28            | 27   | 26       | 25    | 24    | 23          | 22            | 21         | 20          | 19         | 18           | 17         | 16           |
|-------|------------|----|--------------|---------------|------|----------|-------|-------|-------------|---------------|------------|-------------|------------|--------------|------------|--------------|
| Name  | REVO       |    |              |               |      |          |       |       |             |               |            |             | IGMP_MIR   | IGMP_MIS     |            |              |
| Type  | RO         |    |              |               |      |          |       |       |             |               |            |             | RW         | RW           |            |              |
| Reset | 0          | 0  | 0            | 0             | 0    | 0        | 0     | 0     | 0           | 0             | 0          | 0           | 0          | 0            | 0          | 0            |
| Bit   | 15         | 14 | 13           | 12            | 11   | 10       | 9     | 8     | 7           | 6             | 5          | 4           | 3          | 2            | 1          | 0            |
| Name  | ROBUST_VAR |    | MLD_HW_LEAVE | IGMP_HW_LEAVE | REV1 | IPM22_44 | IPM33 | IPM01 | MLD2_JOIN_N | IGMP3_JOIN_EN | MLD_JOIN_N | IGMP_JOIN_N | MLD_SQRY_N | IGMP_SQRY_EN | MLD_GQRY_N | IGMP_GQRY_EN |
| Type  | RW         |    | RW           | RW            | RW   | RW       | RW    | RW    | RW          | RW            | RW         | RW          | RW         | RW           | RW         | RW           |
| Reset | 1          | 0  | 0            | 0             | 0    | 0        | 0     | 0     | 0           | 0             | 0          | 0           | 0          | 0            | 0          | 0            |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20  | REVO       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 19     | IGMP_MIR   | <b>IP Multicast IGMP Table Mismatch to Mirror Port</b><br><br>Copy IP multicast frames with an IGMP table mismatch to the mirror port.<br><br>[NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis.<br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                     |
| 18:16  | IGMP_MIS   | <b>IP Multicast "TO_CPU" Forwarding</b><br><br>Select how to forward IP multicast frames when the IGMP table is mismatched.<br><br>[NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis.<br><br>3'b0xx: System default (By MFC.UNM_FFP)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.)<br><br>3'b111: Frame dropped |
| 15:14  | ROBUST_VAR | <b>Robustness Variable</b><br><br>Define the number of times an IGMP report message may be lost consecutively.<br><br>0: Unlimited (No Age out)<br><br>1: One time<br><br>2: Twice (default)<br><br>3: Three times                                                                                                                                                                                                                                                                                                                                                                        |

| Bit(s) | Name          | Description                                                                                                                                                                                                                         |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13     | MLD_HW_LEAVE  | <b>MLD HW Leave Enable</b><br><br>Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed from the specific group address without a group-specific query.<br><br>0: Disable<br><br>1: Enable    |
| 12     | IGMP_HW_LEAVE | <b>IGMP HW Leave Enable</b><br><br>Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed from the specific group address without a group-specific query.<br><br>0: Disable<br><br>1: Enable |
| 11     | REV1          | <b>Reserved</b>                                                                                                                                                                                                                     |
| 10     | IPM_2244      | <b>IP Multicast frame for DIP is Class D: 224.x.x.x to 239.x.x.x</b><br><br>0: This frame is regarded as a normal multicast and search ADDR Table.<br><br>1: This frame is regarded as an IP multicast frame and search IGMP table. |
| 9      | IPM_33        | <b>IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx</b><br><br>0: This frame is regarded as normal multicast and search ADDR table.<br><br>1: This frame is regarded as IP multicast frame and search IGMP table.                 |
| 8      | IPM_01        | <b>IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx</b><br><br>0: This frame is regarded as normal multicast and search ADDR Table.<br><br>1: This frame is regarded as IP multicast frame and search IGMP table.                 |
| 7      | MLD2_JOIN_EN  | <b>MLD v2 HW Join Enable</b><br><br>Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX().<br><br>0: Disable<br><br>1: Enable             |
| 6      | IGMP3_JOIN_EN | <b>IGMP v3 HW Join Enable</b><br><br>Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX().<br><br>0: Disable<br><br>1: Enable            |
| 5      | MLD_JOIN_EN   | <b>MLD Snooping HW Join Enable</b>                                                                                                                                                                                                  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                 |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame.                                                                                                                                                           |
|        |              | 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).                                                                                                                                                 |
| 4      | IGMP_JOIN_EN | <b>IGMP Snooping HW Join Enable</b><br><br>Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically.<br><br>0: Disable<br><br>1: Enable                                                             |
| 3      | MLD_SQRY_EN  | <b>MLD HW Specific Query Enable</b><br><br>0: MLD-specific query message does not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the MLD-specific query message to refresh the specific multicast member.    |
| 2      | IGMP_SQRY_EN | <b>IGMP HW Specific Query Enable</b><br><br>0: IGMP-specific query message does not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the IGMP-specific query message to refresh the specific multicast member. |
| 1      | MLD_GQRY_EN  | <b>MLD HW General Query Enable</b><br><br>0: MLD general query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the MLD general query message to refresh the multicast member.                |
| 0      | IGMP_GQRY_EN | <b>IGMP HW General Query Enable</b><br><br>0: IGMP general Query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.             |

**1502200C      P0\_PSC      Port security control of P0      000FFF00**

| Bit          | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23   | 22 | 21        | 20     | 19         | 18 | 17           | 16           |
|--------------|------------|----|----|----|----|----|----|----|------|----|-----------|--------|------------|----|--------------|--------------|
| <b>Name</b>  | SA_LRN_CNT |    |    |    |    |    |    |    |      |    |           |        | MAC_SA_LRN |    |              |              |
| <b>Type</b>  | RO         |    |    |    |    |    |    |    |      |    |           |        | RW         |    |              |              |
| <b>Reset</b> | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0    | 0  | 0         | 0      | 1          | 1  | 1            | 1            |
| Bit          | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7    | 6  | 5         | 4      | 3          | 2  | 1            | 0            |
| <b>Name</b>  | MAC_SA_LRN |    |    |    |    |    |    |    | REVO |    | SA_CNT_EN | SA_DIS | SA_LOCK    |    | TX_PORT_LOCK | RX_PORT_LOCK |
| <b>Type</b>  | RW         |    |    |    |    |    |    |    | RW   |    | RW        | RW     | RW         |    | RW           | RW           |
| <b>Reset</b> | 1          | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0    | 0  | 0         | 0      | 0          | 0  | 0            | 0            |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20  | SA_LRN_CNT | <b>Learned Source Address Number</b>                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 19:8   | MAC_SA_LRN | <b>Rx SA Allowable Learning Number</b><br><br>Set the maximum number of SA learned addresses when SA_CNT_EN is set.<br><br>12'h0: Disable SA learning<br><br>12'h1:<br><br>12'hFFE: 1 to 4094 address table<br><br>12'hFFF: SA Learning without limitation                                                                                                                                                                                               |
| 7:6    | REVO       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5      | SA_CNT_EN  | <b>SA Counter Enable</b><br><br>Enable the learned source MAC Address counter.<br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                                                                                                                                        |
| 4      | SA_DIS     | <b>SA Disable</b><br><br>Disable source MAC address learning.<br><br>0: Enable<br><br>1: Disable                                                                                                                                                                                                                                                                                                                                                         |
| 3:2    | SA_LOCK    | <b>SA Lock Select</b><br><br>[NOTE] PAE frames should be passed and is not affected by SA Lock.<br><br>2'b00: Receive without SA authorization.<br><br>2'b01: All received frames whose SA look-up is missing or the received frames that are not port members in the ARL will be dropped.<br><br>2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). |



| Bit(s) | Name         | Description                                                                                                                                                                  |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)                         |
| 1      | TX_PORT_LOCK | <b>Tx Port Lock Enable</b><br><br>[NOTE] PAE Frames should be passed and are not affected by Port Lock.<br><br>0: Transmit authorized.<br><br>1: Disable frame transmission. |
| 0      | RX_PORT_LOCK | <b>Rx Port Lock Enable</b><br><br>[NOTE] PAE frames should be passed and are not affected by Port Lock.<br><br>0: Receive authorized.<br><br>1: Disable frame receiving.     |

**15022010 P0\_PVC Port VLAN control of P0 810000C0**

| Bit          | 31           | 30             | 29             | 28   | 27            | 26     | 25 | 24 | 23        | 22 | 21            | 20              | 19             | 18             | 17      | 16 |
|--------------|--------------|----------------|----------------|------|---------------|--------|----|----|-----------|----|---------------|-----------------|----------------|----------------|---------|----|
| <b>Name</b>  | STAG_VPID    |                |                |      |               |        |    |    |           |    |               |                 |                |                |         |    |
| <b>Type</b>  | RW           |                |                |      |               |        |    |    |           |    |               |                 |                |                |         |    |
| <b>Reset</b> | 1            | 0              | 0              | 0    | 0             | 0      | 0  | 1  | 0         | 0  | 0             | 0               | 0              | 0              | 0       | 0  |
| Bit          | 15           | 14             | 13             | 12   | 11            | 10     | 9  | 8  | 7         | 6  | 5             | 4               | 3              | 2              | 1       | 0  |
| <b>Name</b>  | DIS_PV<br>ID | FORCE<br>_PVID | BC_LKY<br>V_EN | REVO | PT_OP<br>TION | EG_TAG |    |    | VLAN_ATTR |    | PORT_<br>STAG | IPM_LK<br>YV_EN | MC_LK<br>YV_EN | UC_LKY<br>V_EN | ACC_FRM |    |
| <b>Type</b>  | RW           | RW             | RW             | RW   | RW            | RW     |    |    | RW        |    | RW            | RW              | RW             | RW             | RW      |    |
| <b>Reset</b> | 0            | 0              | 0              | 0    | 0             | 0      | 0  | 0  | 1         | 1  | 0             | 0               | 0              | 0              | 0       | 0  |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                            |
|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | STAG_VPID  | <b>Stack Tag VPID (VLAN Protocol ID) Value</b><br><br>The received frame will be regarded as a legal stack tag frame if the following conditions are matched:<br><br>Outer VPID == STAG_VPID<br><br>Inner VPID == 16'h8100<br><br>The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID. |
| 15     | DIS_PVID   | <b>PVID Disable</b><br><br>Disable PVID insertion in priority-tagged frames.<br><br>0: Use PVID for priority-tagged frames.<br><br>1: Keep VID=0 for priority-tagged frames.                                                                                                                                                           |
| 14     | FORCE_PVID | <b>Force PVID on VLAN-tagged frames</b><br><br>0: Use VID in VLAN-tagged frame.<br><br>1: Force the replacement of VID with PVID.                                                                                                                                                                                                      |
| 13     | BC_LKYV_EN | <b>Broadcast Leaky VLAN Enable</b><br><br>0: Broadcast frames received by this port will be blocked by VLAN.<br><br>1: Broadcast frames received by this port can pass through VLAN.                                                                                                                                                   |
| 12     | REVO       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                        |
| 11     | PT_OPTION  | <b>Pass-through capability on TX special tag</b><br><br>0: Disable pass-through on TX special tag<br><br>1: Enable pass-through on TX special tag                                                                                                                                                                                      |
| 10:8   | EG_TAG     | <b>Incoming Port Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disabled)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged                                                                                                                                                            |

| Bit(s) | Name        | Description                                                                                                                                       |
|--------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6    | VLAN_ATTR   | 3'b101: Swap                                                                                                                                      |
|        |             | 3'b110: Tagged                                                                                                                                    |
|        |             | 3'b111: Stack                                                                                                                                     |
|        |             | <b>VLAN Port Attribute</b>                                                                                                                        |
|        |             | 2'b00: User port                                                                                                                                  |
|        |             | 2'b01: Stack port                                                                                                                                 |
|        |             | 2'b10: Translation port                                                                                                                           |
| 5      | PORT_STAG   | 2'b11: Transparent port                                                                                                                           |
|        |             | <b>Special Tag Enable</b>                                                                                                                         |
|        |             | Enable a proprietary VLAN tag format to carry additional information to the remote port.                                                          |
| 4      | IPM_LKYV_EN | 0: No special tag format for Tx/Rx                                                                                                                |
|        |             | 1: Enable                                                                                                                                         |
|        |             | <b>IP Multicast Leaky VLAN Enable</b>                                                                                                             |
|        |             | (note*) If MC_LKYV_EN is set, this field will become "don't care" bit. All multicast frames including IP_Multi will be leaky between VLAN groups. |
| 3      | MC_LKYV_EN  | 0: IP_Multi frames received by this port will be blocked by VLAN.                                                                                 |
|        |             | 1: IP_Multi frames received by this port can pass through VLAN.                                                                                   |
|        |             | <b>Multicast Leaky VLAN Enable</b>                                                                                                                |
| 2      | UC_LKYV_EN  | 0: Multicast frames received by this port will be blocked by VLAN.                                                                                |
|        |             | 1: Multicast frames received by this port can pass through VLAN.                                                                                  |
|        |             | <b>Unicast Leaky VLAN Enable</b>                                                                                                                  |
| 1:0    | ACC_FRM     | 0: Unicast frame received by this port will be blocked by VLAN.                                                                                   |
|        |             | 1: Unicast frame received by this port can pass through VLAN.                                                                                     |
|        |             | <b>Acceptable Frame Type</b>                                                                                                                      |
|        |             | 2'b00: Admit All frames                                                                                                                           |
|        |             | 2'b01: Admit Only VLAN-tagged frames                                                                                                              |
|        |             | 2'b10: Admit only untagged or priority-tagged frames.                                                                                             |
|        |             | 2'b11: Reserved                                                                                                                                   |

15022014 P0\_PPBV1 Port-and-Protocol based VLAN I of P0 00010001

| Bit   | 31          | 30 | 29 | 28   | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|------|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  | G1_PORT_PRI |    |    | REV0 | G1_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| Bit   | 15          | 14 | 13 | 12   | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | G0_PORT_PRI |    |    | REV1 | G0_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name        | Description                                                                                                                                    |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29  | G1_PORT_PRI | <b>Group 1 Port Priority (optional)</b><br><br>The Group 1 Priority for each port according to IEEE 802.1Q definition                          |
| 28     | REV0        | <b>Reserved</b>                                                                                                                                |
| 27:16  | G1_PORT_VID | <b>Group 1 Port VLAN ID (optional)</b><br><br>The Group 1 VID for each port according to IEEE 802.1Q definition                                |
| 15:13  | G0_PORT_PRI | <b>Group 0 Port Priority (Default Port Priority)</b><br><br>The Group 0 and default Priority for each port according to IEEE 802.1Q definition |
| 12     | REV1        | <b>Reserved</b>                                                                                                                                |
| 11:0   | G0_PORT_VID | <b>Group 0 Port VLAN ID (Default Port VID)</b><br><br>The Group 0 and default VID for each port according to IEEE 802.1Q definition            |

15022018      P0\_PPBV2      Port-and-Protocol based VLAN II of P0      00010001

| Bit   | 31          | 30 | 29 | 28   | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|------|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |             |    |    | REV0 | G3_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| Bit   | 15          | 14 | 13 | 12   | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | G2_PORT_PRI |    |    | REV1 | G2_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name        | Description                                                                                                           |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------|
| 28     | REV0        | Reserved                                                                                                              |
| 27:16  | G3_PORT_VID | <b>Group 3 Port VLAN ID (optional)</b><br><br>The Group 3 VID for each port according to IEEE 802.1Q definition       |
| 15:13  | G2_PORT_PRI | <b>Group 2 Port Priority (optional)</b><br><br>The Group 2 Priority for each port according to IEEE 802.1Q definition |
| 12     | REV1        | Reserved                                                                                                              |
| 11:0   | G2_PORT_VID | <b>Group 2 Port VLAN ID (optional)</b><br><br>The Group 2 VID for each port according to IEEE 802.1Q definition       |

1502201C      **P0\_BSR**      Broadcast storm rate control of P0      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
|        |            | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
| 7:0    | STORM_10M  | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |

15022020      P0\_STAG01      STAG index 0/1 of P0      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REVO |    |    |    |      |    |    |    | VID1 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID1 |    |    |    | VID0 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID1 | VLAN Identifier for STAG index 1 |
| 11:0   | VID0 | VLAN Identifier for STAG index 0 |



15022024      P0\_STAG23      STAG index 2/3 of P0      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REVO |    |    |    |      |    |    |    | VID3 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID3 |    |    |    | VID2 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID3 | VLAN Identifier for STAG index 3 |
| 11:0   | VID2 | VLAN Identifier for STAG index 2 |

15022028      P0\_STAG45      STAG index 4/5 of P0      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REVO |    |    |    |      |    |    |    | VID5 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID5 |    |    |    | VID4 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID5 | VLAN Identifier for STAG index 5 |
| 11:0   | VID4 | VLAN Identifier for STAG index 4 |

1502202C      P0\_STAG67      STAG index 6/7 of P0      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REVO |    |    |    |      |    |    |    | VID7 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID7 |    |    |    | VID6 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID7 | VLAN Identifier for STAG index 7 |
| 11:0   | VID6 | VLAN Identifier for STAG index 6 |

15022030 P0\_BSR\_EXT1 Broadcast storm rate control I of P0 00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
| 7:0    | STORM_10M  | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
|        |            | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |

15022034      **P0\_BSR\_EXT2**      Broadcast storm rate control II of P0      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
| 7:0    | STORM_10M  | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            |                                                         |

15022038      **P0\_BSR\_EXT3**      Broadcast storm rate control III of P0      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |



| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
| 7:0    | STORM_10M  | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            |                                                         |

**15022040 P0\_UPW User priority weight of P0 00234567**

| Bit   | 31   | 30       | 29 | 28 | 27   | 26      | 25 | 24 | 23   | 22       | 21 | 20 | 19   | 18       | 17 | 16 |
|-------|------|----------|----|----|------|---------|----|----|------|----------|----|----|------|----------|----|----|
| Name  |      |          |    |    |      |         |    |    | REV0 | ARL_UPW  |    |    | REV1 | PORT_UPW |    |    |
| Type  |      |          |    |    |      |         |    |    | RW   | RW       |    |    | RW   | RW       |    |    |
| Reset |      |          |    |    |      |         |    |    | 0    | 0        | 1  | 0  | 0    | 0        | 1  | 1  |
| Bit   | 15   | 14       | 13 | 12 | 11   | 10      | 9  | 8  | 7    | 6        | 5  | 4  | 3    | 2        | 1  | 0  |
| Name  | REV2 | DSCP_UPW |    |    | REV3 | TAG_UPW |    |    | REV4 | STAG_UPW |    |    | REV5 | ACL_UPW  |    |    |
| Type  | RW   | RW       |    |    | RW   | RW      |    |    | RW   | RW       |    |    | RW   | RW       |    |    |
| Reset | 0    | 1        | 0  | 0  | 0    | 1       | 0  | 1  | 0    | 1        | 1  | 0  | 0    | 1        | 1  | 1  |

| Bit(s) | Name     | Description                                                             |
|--------|----------|-------------------------------------------------------------------------|
| 23     | REV0     | Reserved                                                                |
| 22:20  | ARL_UPW  | ARL User Priority Weight (MAC/DIP Hit)                                  |
| 19     | REV1     | Reserved                                                                |
| 18:16  | PORT_UPW | Port-Based User Priority Weight Value<br>Weights range from 0x0 to 0x7. |
| 15     | REV2     | Reserved                                                                |
| 14:12  | DSCP_UPW | DSCP Priority Weight (IPv4)                                             |
| 11     | REV3     | Reserved                                                                |
| 10:8   | TAG_UPW  | Priority Tag User Priority Weight                                       |
| 7      | REV4     | Reserved                                                                |
| 6:4    | STAG_UPW | Special Tag User Priority Weight                                        |
| 3      | REV5     | Reserved                                                                |
| 2:0    | ACL_UPW  | ACL User Priority Weight (ACL Hit)                                      |

**15022044**      **P0\_PEM1**      **User priority egress mapping I of P0**      **10080480**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_1 |    |    | QUE_PFCR_1 |    |    | QUE_PFCT_1 |    |    | DSCP_PRI_1 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 0  | 1  | 0          | 0  | 0  | 0          | 0  | 0  | 0          | 0  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_0 |    |    | QUE_PFCR_0 |    |    | QUE_PFCT_0 |    |    | DSCP_PRI_0 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 0  | 0  | 0          | 1  | 0  | 0          | 1  | 0  | 0          | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_1  | User Priority 1 Priority Tag Value                       |
| 27:25  | QUE_PFCR_1 | User Priority 1 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_1 | User Priority 1 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_1 | User Priority 1 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_0  | User Priority 0 Priority Tag Value                       |
| 11:9   | QUE_PFCR_0 | User Priority 0 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_0 | User Priority 0 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_0 | User Priority 0 DSCP Value                               |

**15022048      P0\_PEM2      User priority egress mapping II of P0      36D82250**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_3 |    |    | QUE_PFCR_3 |    |    | QUE_PFCT_3 |    |    | DSCP_PRI_3 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 1  | 1  | 0          | 1  | 1  | 0          | 1  | 1  | 0          | 1  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_2 |    |    | QUE_PFCR_2 |    |    | QUE_PFCT_2 |    |    | DSCP_PRI_2 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 1  | 0  | 0          | 0  | 1  | 0          | 0  | 1  | 0          | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_3  | User Priority 3 Priority Tag Value                       |
| 27:25  | QUE_PFCR_3 | User Priority 3 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_3 | User Priority 3 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_3 | User Priority 3 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_2  | User Priority 2 Priority Tag Value                       |
| 11:9   | QUE_PFCR_2 | User Priority 2 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_2 | User Priority 2 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_2 | User Priority 2 DSCP Value                               |

**1502204C      P0\_PEM3      User priority egress mapping III of P0      5B684920**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_5 |    |    | QUE_PFCR_5 |    |    | QUE_PFCT_5 |    |    | DSCP_PRI_5 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 0  | 1  | 1          | 0  | 1  | 1          | 0  | 1  | 1          | 0  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_4 |    |    | QUE_PFCR_4 |    |    | QUE_PFCT_4 |    |    | DSCP_PRI_4 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 0  | 0  | 1          | 0  | 0  | 1          | 0  | 0  | 1          | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_5  | User Priority 5 Priority Tag Value                       |
| 27:25  | QUE_PFCR_5 | User Priority 5 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_5 | User Priority 5 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_5 | User Priority 5 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_4  | User Priority 4 Priority Tag Value                       |
| 11:9   | QUE_PFCR_4 | User Priority 4 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_4 | User Priority 4 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_4 | User Priority 4 DSCP Value                               |

**15022050      P0\_PEM4      User priority egress mapping IV of P0      7FF86DB0**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_7 |    |    | QUE_PFCR_7 |    |    | QUE_PFCT_7 |    |    | DSCP_PRI_7 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 1  | 1  | 1          | 1  | 1  | 1          | 1  | 1  | 1          | 1  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_6 |    |    | QUE_PFCR_6 |    |    | QUE_PFCT_6 |    |    | DSCP_PRI_6 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 1  | 0  | 1          | 1  | 0  | 1          | 1  | 0  | 1          | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_7  | User Priority 7 Priority Tag Value                       |
| 27:25  | QUE_PFCR_7 | User Priority 7 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_7 | User Priority 7 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_7 | User Priority 7 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_6  | User Priority 6 Priority Tag Value                       |
| 11:9   | QUE_PFCR_6 | User Priority 6 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_6 | User Priority 6 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_6 | User Priority 6 DSCP Value                               |

15022100      P1\_SSC      STP state control of P1      0000FFFF

| Bit   | 31       | 30 | 29       | 28 | 27       | 26 | 25       | 24 | 23       | 22 | 21       | 20 | 19       | 18 | 17       | 16 |
|-------|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|
| Name  | REVO     |    |          |    |          |    |          |    |          |    |          |    |          |    |          |    |
| Type  | RO       |    |          |    |          |    |          |    |          |    |          |    |          |    |          |    |
| Reset | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  |
| Bit   | 15       | 14 | 13       | 12 | 11       | 10 | 9        | 8  | 7        | 6  | 5        | 4  | 3        | 2  | 1        | 0  |
| Name  | FID7_PST |    | FID6_PST |    | FID5_PST |    | FID4_PST |    | FID3_PST |    | FID2_PST |    | FID1_PST |    | FID0_PST |    |
| Type  | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    |
| Reset | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  |

| Bit(s) | Name     | Description                                                                                                                                                                                                                    |
|--------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | REVO     | <b>Reserved</b>                                                                                                                                                                                                                |
| 15:14  | FID7_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 13:12  | FID6_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 11:10  | FID5_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 9:8    | FID4_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 7:6    | FID3_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)                                                |

| Bit(s) | Name     | Description                                      |
|--------|----------|--------------------------------------------------|
| 5:4    | FID2_PST | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |
|        |          | <b>(Rapid) Spanning Tree Protocol Port State</b> |
|        |          | 2'b00: Disable (STP) / Discard (RSTP)            |
|        |          | 2'b01: Listening (STP) / Discard (RSTP)          |
|        |          | 2'b10: Learning (STP) / Learning (RSTP)          |
| 3:2    | FID1_PST | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |
|        |          | <b>(Rapid) Spanning Tree Protocol Port State</b> |
|        |          | 2'b00: Disable (STP) / Discard (RSTP)            |
|        |          | 2'b01: Listening (STP) / Discard (RSTP)          |
|        |          | 2'b10: Learning (STP) / Learning (RSTP)          |
| 1:0    | FID0_PST | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |
|        |          | <b>(Rapid) Spanning Tree Protocol Port State</b> |
|        |          | 2'b00: Disable (STP) / Discard (RSTP)            |
|        |          | 2'b01: Listening (STP) / Discard (RSTP)          |
|        |          | 2'b10: Learning (STP) / Learning (RSTP)          |
|        |          | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |



**15022104 P1\_PCR Port control of P1 00FF2000**

| Bit   | 31   | 30       | 29     | 28         | 27        | 26       | 25         | 24         | 23          | 22          | 21 | 20 | 19   | 18       | 17        | 16 |
|-------|------|----------|--------|------------|-----------|----------|------------|------------|-------------|-------------|----|----|------|----------|-----------|----|
| Name  | REV0 | MLDv2_EN | EG_TAG |            | REV1      | PORT_PRI |            |            | PORT_MATRIX |             |    |    |      |          |           |    |
| Type  | RW   | RW       | RW     |            | RW        | RW       |            |            | RW          |             |    |    |      |          |           |    |
| Reset | 0    | 0        | 0      | 0          | 0         | 0        | 0          | 0          | 1           | 1           | 1  | 1  | 1    | 1        | 1         | 1  |
| Bit   | 15   | 14       | 13     | 12         | 11        | 10       | 9          | 8          | 7           | 6           | 5  | 4  | 3    | 2        | 1         | 0  |
| Name  | REV2 |          |        | UP2DSCP_EN | UP2TAG_EN | ACL_EN   | PORT_TX_MR | PORT_RX_MR | ACL_MR      | MIS_PORT_FW |    |    | REV3 | VLAN_MIS | PORT_VLAN |    |
| Type  | RW   |          |        | RW         | RW        | RW       | RW         | RW         | RW          | RW          |    |    | RW   | RW       | RW        |    |
| Reset | 0    | 0        | 1      | 0          | 0         | 0        | 0          | 0          | 0           | 0           | 0  | 0  | 0    | 0        | 0         | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                     |
|--------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | REV0        | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 30     | MLDv2_EN    | <b>IPv6 MLDv2 source address multicast forwarding enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                 |
| 29:28  | EG_TAG      | <b>Port-Based Egress VLAN Tag Attribution</b><br><br>2'b00: Untagged<br><br>2'b01: Swap<br><br>2'b10: Tagged<br><br>2'b11: Stack                                                                                                                                                |
| 27     | REV1        | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 26:24  | PORT_PRI    | <b>Port-based User Priority</b><br><br>User priority for the ingress port                                                                                                                                                                                                       |
| 23:16  | PORT_MATRIX | <b>Port Matrix Member</b><br><br>The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member.<br><br>NOTE: The final and effective port member should exclude the received port. |
| 15:13  | REV2        | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 12     | UP2DSCP_EN  | <b>User Priority to DSCP Enable</b><br><br>Replace DSCP according to user priority.<br><br>0: Disable<br><br>1: Enable                                                                                                                                                          |
| 11     | UP2TAG_EN   | <b>User Priority to Tag Enable</b><br><br>Replace 802.Q priority by user priority.                                                                                                                                                                                              |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |             | 0: Disable                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |             | 1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 10     | ACL_EN      | <b>Port-based ACL Enable</b><br>0: Bypass the ACL Table.<br>1: Lookup the ACL Table and take the corresponding actions.                                                                                                                                                                                                                                                                                                                        |
| 9      | PORT_TX_MIR | <b>Port Tx Mirror Enable</b><br>All frames transmitted from this port are copied to the mirror port.<br>[NOTE] Multi-port support is possible.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                      |
| 8      | PORT_RX_MIR | <b>Port Rx Mirror Enable</b><br>All frames received from this port are copied to the mirror port.<br>[NOTE] Multi-port support is possible.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                         |
| 7      | ACL_MIR     | <b>ACL Mismatch to Mirror Port</b><br>Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                     |
| 6:4    | MIS_PORT_FW | <b>ACL Mismatch TO_CPU Forward</b><br>Frame port forwarding when ACL table is enabled and the frame is mismatched<br>3'b0xx: System default (disabled)<br>3'b100: System default and CPU port excluded<br>3'b101: System default and CPU port included<br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.)<br>3'b111: Frame dropped |
| 3      | REV3        | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 2      | VLAN_MIS    | <b>VLAN Mismatch to Mirror Port</b><br>1'b0: Frame is processed according to PORT_VLAN.<br>1'b1: VLAN mismatched frame is copied to MIRROR port.                                                                                                                                                                                                                                                                                               |

| Bit(s) | Name      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|--------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0    | PORT_VLAN | <b>Port-based VLAN Mechanism Select</b><br><br>2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member.<br><br>2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member.<br><br>2'b10: Check Mode. Forward received frames whose ingress port does not belong to the VLAN member. Discard frames if VID is missed on the VLAN table.<br><br>2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table. |

15022108      P1\_PIC      Port IGMP control of P1      00008000

| Bit   | 31         | 30 | 29           | 28            | 27   | 26       | 25    | 24    | 23          | 22            | 21         | 20          | 19         | 18           | 17         | 16           |
|-------|------------|----|--------------|---------------|------|----------|-------|-------|-------------|---------------|------------|-------------|------------|--------------|------------|--------------|
| Name  | REVO       |    |              |               |      |          |       |       |             |               |            |             | IGMP_MIR   | IGMP_MIS     |            |              |
| Type  | RO         |    |              |               |      |          |       |       |             |               |            |             | RW         | RW           |            |              |
| Reset | 0          | 0  | 0            | 0             | 0    | 0        | 0     | 0     | 0           | 0             | 0          | 0           | 0          | 0            | 0          | 0            |
| Bit   | 15         | 14 | 13           | 12            | 11   | 10       | 9     | 8     | 7           | 6             | 5          | 4           | 3          | 2            | 1          | 0            |
| Name  | ROBUST_VAR |    | MLD_HW_LEAVE | IGMP_HW_LEAVE | REV1 | IPM22_44 | IPM33 | IPM01 | MLD2_JOIN_N | IGMP3_JOIN_EN | MLD_JOIN_N | IGMP_JOIN_N | MLD_SQRY_N | IGMP_SQRY_EN | MLD_GQRY_N | IGMP_GQRY_EN |
| Type  | RW         |    | RW           | RW            | RW   | RW       | RW    | RW    | RW          | RW            | RW         | RW          | RW         | RW           | RW         | RW           |
| Reset | 1          | 0  | 0            | 0             | 0    | 0        | 0     | 0     | 0           | 0             | 0          | 0           | 0          | 0            | 0          | 0            |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20  | REVO       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 19     | IGMP_MIR   | <b>IP Multicast IGMP Table Mismatch to Mirror Port</b><br><br>Copy IP multicast frames with an IGMP table mismatch to the mirror port.<br><br>[NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis.<br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                     |
| 18:16  | IGMP_MIS   | <b>IP Multicast "TO_CPU" Forwarding</b><br><br>Select how to forward IP multicast frames when the IGMP table is mismatched.<br><br>[NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis.<br><br>3'b0xx: System default (By MFC.UNM_FFP)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.)<br><br>3'b111: Frame dropped |
| 15:14  | ROBUST_VAR | <b>Robustness Variable</b><br><br>Define the number of times an IGMP report message may be lost consecutively.<br><br>0: Unlimited (No Age out)<br><br>1: One time<br><br>2: Twice (default)<br><br>3: Three times                                                                                                                                                                                                                                                                                                                                                                        |

| Bit(s) | Name          | Description                                                                                                                                                                                                                         |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13     | MLD_HW_LEAVE  | <b>MLD HW Leave Enable</b><br><br>Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query.<br><br>0: Disable<br><br>1: Enable      |
| 12     | IGMP_HW_LEAVE | <b>IGMP HW Leave Enable</b><br><br>Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query.<br><br>0: Disable<br><br>1: Enable   |
| 11     | REV1          | <b>Reserved</b>                                                                                                                                                                                                                     |
| 10     | IPM_2244      | <b>IP Multicast frame for DIP is Class D: 224.x.x.x to 239.x.x.x</b><br><br>0: This frame is regarded as a normal multicast and search ADDR Table.<br><br>1: This frame is regarded as an IP multicast frame and search IGMP table. |
| 9      | IPM_33        | <b>IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx</b><br><br>0: This frame is regarded as normal multicast and search ADDR table.<br><br>1: This frame is regarded as IP multicast frame and search IGMP table.                 |
| 8      | IPM_01        | <b>IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx</b><br><br>0: This frame is regarded as normal multicast and search ADDR Table.<br><br>1: This frame is regarded as IP multicast frame and search IGMP table.                 |
| 7      | MLD2_JOIN_EN  | <b>MLD v2 HW Join Enable</b><br><br>Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX().<br><br>0: Disable<br><br>1: Enable             |
| 6      | IGMP3_JOIN_EN | <b>IGMP v3 HW Join Enable</b><br><br>Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX().<br><br>0: Disable<br><br>1: Enable            |
| 5      | MLD_JOIN_EN   | <b>MLD Snooping HW Join Enable</b>                                                                                                                                                                                                  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                 |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame.                                                                                                                                                           |
|        |              | 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).                                                                                                                                                 |
| 4      | IGMP_JOIN_EN | <b>IGMP Snooping HW Join Enable</b><br><br>Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically.<br><br>0: Disable<br><br>1: Enable                                                             |
| 3      | MLD_SQRY_EN  | <b>MLD HW Specific Query Enable</b><br><br>0: MLD specific query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the MLD specific query message to refresh the specific multicast member.    |
| 2      | IGMP_SQRY_EN | <b>IGMP HW Specific Query Enable</b><br><br>0: IGMP specific query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member. |
| 1      | MLD_GQRY_EN  | <b>MLD HW General Query Enable</b><br><br>0: MLD general query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the MLD general query message to refresh the multicast member.                |
| 0      | IGMP_GQRY_EN | <b>IGMP HW General Query Enable</b><br><br>0: IGMP general Query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.             |

**1502210C      P1\_PSC      Port security control of P1      000FFF00**

| Bit          | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23   | 22 | 21        | 20     | 19         | 18 | 17           | 16           |
|--------------|------------|----|----|----|----|----|----|----|------|----|-----------|--------|------------|----|--------------|--------------|
| <b>Name</b>  | SA_LRN_CNT |    |    |    |    |    |    |    |      |    |           |        | MAC_SA_LRN |    |              |              |
| <b>Type</b>  | RO         |    |    |    |    |    |    |    |      |    |           |        | RW         |    |              |              |
| <b>Reset</b> | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0    | 0  | 0         | 0      | 1          | 1  | 1            | 1            |
| Bit          | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7    | 6  | 5         | 4      | 3          | 2  | 1            | 0            |
| <b>Name</b>  | MAC_SA_LRN |    |    |    |    |    |    |    | REVO |    | SA_CNT_EN | SA_DIS | SA_LOCK    |    | TX_PORT_LOCK | RX_PORT_LOCK |
| <b>Type</b>  | RW         |    |    |    |    |    |    |    | RW   |    | RW        | RW     | RW         |    | RW           | RW           |
| <b>Reset</b> | 1          | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0    | 0  | 0         | 0      | 0          | 0  | 0            | 0            |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20  | SA_LRN_CNT | <b>Learned Source Address Number</b>                                                                                                                                                                                                                                                                                                                                                                                             |
| 19:8   | MAC_SA_LRN | <b>Rx SA Allowable Learning Number</b><br><br>Sets the maximum number of SA learned addresses when SA_CNT_EN is set.<br><br>12'h0: Disable SA learning<br><br>12'h1:<br><br>12'hFFE: 1 to 4094 address table<br><br>12'hFFF: SA Learning without limitation                                                                                                                                                                      |
| 7:6    | REVO       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 5      | SA_CNT_EN  | <b>SA Counter Enable</b><br><br>Enable the learned source MAC Address counter.<br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                                                                                                                |
| 4      | SA_DIS     | <b>SA Disable</b><br><br>Disable source MAC address learning.<br><br>0: Enable<br><br>1: Disable                                                                                                                                                                                                                                                                                                                                 |
| 3:2    | SA_LOCK    | <b>SA Lock Select</b><br><br>[NOTE] PAE frames should be passed and are not affected by SA Lock.<br><br>2'b00: Receive without SA authorization.<br><br>2'b01: All received frames whose SA look-up is missing or are not port members in the ARL will be dropped.<br><br>2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). |

| Bit(s) | Name         | Description                                                                                                                                                                  |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)                         |
| 1      | TX_PORT_LOCK | <b>Tx Port Lock Enable</b><br><br>[NOTE] PAE Frames should be passed and are not affected by Port Lock.<br><br>0: Transmit authorized.<br><br>1: Disable frame transmission. |
| 0      | RX_PORT_LOCK | <b>Rx Port Lock Enable</b><br><br>[NOTE] PAE frames should be passed and are not affected by Port Lock.<br><br>0: Receive authorized.<br><br>1: Disable frame receiving.     |



**15022110 P1\_PVC Port VLAN control of P1 810000C0**

| Bit          | 31           | 30             | 29             | 28   | 27            | 26     | 25 | 24 | 23        | 22 | 21            | 20              | 19             | 18             | 17      | 16 |
|--------------|--------------|----------------|----------------|------|---------------|--------|----|----|-----------|----|---------------|-----------------|----------------|----------------|---------|----|
| <b>Name</b>  | STAG_VPID    |                |                |      |               |        |    |    |           |    |               |                 |                |                |         |    |
| <b>Type</b>  | RW           |                |                |      |               |        |    |    |           |    |               |                 |                |                |         |    |
| <b>Reset</b> | 1            | 0              | 0              | 0    | 0             | 0      | 0  | 1  | 0         | 0  | 0             | 0               | 0              | 0              | 0       | 0  |
| Bit          | 15           | 14             | 13             | 12   | 11            | 10     | 9  | 8  | 7         | 6  | 5             | 4               | 3              | 2              | 1       | 0  |
| <b>Name</b>  | DIS_PV<br>ID | FORCE<br>_PVID | BC_LKY<br>V_EN | REVO | PT_OP<br>TION | EG_TAG |    |    | VLAN_ATTR |    | PORT_<br>STAG | IPM_LK<br>YV_EN | MC_LK<br>YV_EN | UC_LKY<br>V_EN | ACC_FRM |    |
| <b>Type</b>  | RW           | RW             | RW             | RW   | RW            | RW     |    |    | RW        |    | RW            | RW              | RW             | RW             | RW      |    |
| <b>Reset</b> | 0            | 0              | 0              | 0    | 0             | 0      | 0  | 0  | 1         | 1  | 0             | 0               | 0              | 0              | 0       | 0  |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                            |
|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | STAG_VPID  | <b>Stack Tag VPID (VLAN Protocol ID) Value</b><br><br>The received frame will be regarded as a legal stack tag frame if the following conditions are matched:<br><br>Outer VPID == STAG_VPID<br><br>Inner VPID == 16'h8100<br><br>The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID. |
| 15     | DIS_PVID   | <b>PVID Disable</b><br><br>Disable PVID insertion in priority-tagged frames.<br><br>0: Use PVID for priority-tagged frames.<br><br>1: Keep VID=0 for priority-tagged frames.                                                                                                                                                           |
| 14     | FORCE_PVID | <b>Force PVID on VLAN-tagged frames</b><br><br>0: Use VID in VLAN-tagged frame.<br><br>1: Force the replacement of VID with PVID.                                                                                                                                                                                                      |
| 13     | BC_LKYV_EN | <b>Broadcast Leaky VLAN Enable</b><br><br>0: Broadcast frames received by this port will be blocked by VLAN.<br><br>1: Broadcast frames received by this port can pass through VLAN.                                                                                                                                                   |
| 12     | REVO       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                        |
| 11     | PT_OPTION  | <b>Pass-through capability on TX special tag</b><br><br>0: Disable pass-through on TX special tag<br><br>1: Enable pass-through on TX special tag                                                                                                                                                                                      |
| 10:8   | EG_TAG     | <b>Incoming Port Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disabled)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged                                                                                                                                                            |

| Bit(s) | Name        | Description                                                                                                                                       |
|--------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
|        |             | 3'b101: Swap                                                                                                                                      |
|        |             | 3'b110: Tagged                                                                                                                                    |
|        |             | 3'b111: Stack                                                                                                                                     |
| 7:6    | VLAN_ATTR   | <b>VLAN Port Attribute</b>                                                                                                                        |
|        |             | 2'b00: User port                                                                                                                                  |
|        |             | 2'b01: Stack port                                                                                                                                 |
|        |             | 2'b10: Translation port                                                                                                                           |
|        |             | 2'b11: Transparent port                                                                                                                           |
| 5      | PORT_STAG   | <b>Special Tag Enable</b>                                                                                                                         |
|        |             | Enable a proprietary VLAN tag format to carry additional information to the remote port.                                                          |
|        |             | 0: No special tag format for Tx/Rx                                                                                                                |
|        |             | 1: Enable                                                                                                                                         |
| 4      | IPM_LKYV_EN | <b>IP Multicast Leaky VLAN Enable</b>                                                                                                             |
|        |             | (note*) If MC_LKYV_EN is set, this field will become "don't care" bit. All multicast frames including IP_Multi will be leaky between VLAN groups. |
|        |             | 0: IP_Multi frames received by this port will be blocked by VLAN.                                                                                 |
|        |             | 1: IP_Multi frames received by this port can pass through VLAN.                                                                                   |
| 3      | MC_LKYV_EN  | <b>Multicast Leaky VLAN Enable</b>                                                                                                                |
|        |             | 0: Multicast frames received by this port will be blocked by VLAN.                                                                                |
|        |             | 1: Multicast frames received by this port can pass through VLAN.                                                                                  |
| 2      | UC_LKYV_EN  | <b>Unicast Leaky VLAN Enable</b>                                                                                                                  |
|        |             | 0: Unicast frame received by this port will be blocked by VLAN.                                                                                   |
|        |             | 1: Unicast frame received by this port can pass through VLAN.                                                                                     |
| 1:0    | ACC_FRM     | <b>Acceptable Frame Type</b>                                                                                                                      |
|        |             | 2'b00: Admit All frames                                                                                                                           |
|        |             | 2'b01: Admit Only VLAN-tagged frames                                                                                                              |
|        |             | 2'b10: Admit only untagged or priority-tagged frames.                                                                                             |
|        |             | 2'b11: Reserved                                                                                                                                   |

15022114      P1\_PPBV1      Port-and-Protocol based VLAN I of P1      00010001

| Bit   | 31          | 30 | 29 | 28   | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|------|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  | G1_PORT_PRI |    |    | REV0 | G1_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| Bit   | 15          | 14 | 13 | 12   | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | G0_PORT_PRI |    |    | REV1 | G0_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name        | Description                                                                                                                                    |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29  | G1_PORT_PRI | <b>Group 1 Port Priority (optional)</b><br><br>The Group 1 Priority for each port according to IEEE 802.1Q definition                          |
| 28     | REV0        | <b>Reserved</b>                                                                                                                                |
| 27:16  | G1_PORT_VID | <b>Group 1 Port VLAN ID (optional)</b><br><br>The Group 1 VID for each port according to IEEE 802.1Q definition                                |
| 15:13  | G0_PORT_PRI | <b>Group 0 Port Priority (Default Port Priority)</b><br><br>The Group 0 and default Priority for each port according to IEEE 802.1Q definition |
| 12     | REV1        | <b>Reserved</b>                                                                                                                                |
| 11:0   | G0_PORT_VID | <b>Group 0 Port VLAN ID (Default Port VID)</b><br><br>The Group 0 and default VID for each port according to IEEE 802.1Q definition            |

15022118      P1\_PPBV2      Port-and-Protocol based VLAN II of P1      00010001

| Bit   | 31          | 30 | 29 | 28   | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|------|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |             |    |    | REV0 | G3_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| Bit   | 15          | 14 | 13 | 12   | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | G2_PORT_PRI |    |    | REV1 | G2_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name        | Description                                                                                                           |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------|
| 28     | REV0        | Reserved                                                                                                              |
| 27:16  | G3_PORT_VID | <b>Group 3 Port VLAN ID (optional)</b><br><br>The Group 3 VID for each port according to IEEE 802.1Q definition       |
| 15:13  | G2_PORT_PRI | <b>Group 2 Port Priority (optional)</b><br><br>The Group 2 Priority for each port according to IEEE 802.1Q definition |
| 12     | REV1        | Reserved                                                                                                              |
| 11:0   | G2_PORT_VID | <b>Group 2 Port VLAN ID (optional)</b><br><br>The Group 2 VID for each port according to IEEE 802.1Q definition       |

1502211C      **P1\_BSR**      Broadcast storm rate control of P1      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
| 7:0    | STORM_10M  | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
|        |            | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |

15022120      P1\_STAG01      STAG index 0/1 of P1      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REVO |    |    |    |      |    |    |    | VID1 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID1 |    |    |    | VID0 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID1 | VLAN Identifier for STAG index 1 |
| 11:0   | VID0 | VLAN Identifier for STAG index 0 |

15022124      P1\_STAG23      STAG index 2/3 of P1      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REVO |    |    |    |      |    |    |    | VID3 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID3 |    |    |    | VID2 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID3 | VLAN Identifier for STAG index 3 |
| 11:0   | VID2 | VLAN Identifier for STAG index 2 |



15022128      P1\_STAG45      STAG index 4/5 of P1      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REV0 |    |    |    |      |    |    |    | VID5 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID5 |    |    |    | VID4 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REV0 | Reserved                         |
| 23:12  | VID5 | VLAN Identifier for STAG index 5 |
| 11:0   | VID4 | VLAN Identifier for STAG index 4 |

1502212C      P1\_STAG67      STAG index 6/7 of P1      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REVO |    |    |    |      |    |    |    | VID7 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID7 |    |    |    | VID6 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID7 | VLAN Identifier for STAG index 7 |
| 11:0   | VID6 | VLAN Identifier for STAG index 6 |

15022130      **P1\_BSR\_EXT1**      Broadcast storm rate control I of P1      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
| 7:0    | STORM_10M  | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
|        |            | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |

15022134      P1\_BSR\_EXT2      Broadcast storm rate control II of P1      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
|        |            | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
| 7:0    | STORM_10M  | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |

15022138      P1\_BSR\_EXT3      Broadcast storm rate control III of P1      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
| 7:0    | STORM_10M  | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
|        |            | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |



**15022140 P1\_UPW User priority weight of P1 00234567**

| Bit   | 31   | 30       | 29 | 28 | 27   | 26      | 25 | 24 | 23   | 22       | 21 | 20 | 19   | 18       | 17 | 16 |
|-------|------|----------|----|----|------|---------|----|----|------|----------|----|----|------|----------|----|----|
| Name  |      |          |    |    |      |         |    |    | REV0 | ARL_UPW  |    |    | REV1 | PORT_UPW |    |    |
| Type  |      |          |    |    |      |         |    |    | RW   | RW       |    |    | RW   | RW       |    |    |
| Reset |      |          |    |    |      |         |    |    | 0    | 0        | 1  | 0  | 0    | 0        | 1  | 1  |
| Bit   | 15   | 14       | 13 | 12 | 11   | 10      | 9  | 8  | 7    | 6        | 5  | 4  | 3    | 2        | 1  | 0  |
| Name  | REV2 | DSCP_UPW |    |    | REV3 | TAG_UPW |    |    | REV4 | STAG_UPW |    |    | REV5 | ACL_UPW  |    |    |
| Type  | RW   | RW       |    |    | RW   | RW      |    |    | RW   | RW       |    |    | RW   | RW       |    |    |
| Reset | 0    | 1        | 0  | 0  | 0    | 1       | 0  | 1  | 0    | 1        | 1  | 0  | 0    | 1        | 1  | 1  |

| Bit(s) | Name     | Description                                                             |
|--------|----------|-------------------------------------------------------------------------|
| 23     | REV0     | Reserved                                                                |
| 22:20  | ARL_UPW  | ARL User Priority Weight (MAC/DIP Hit)                                  |
| 19     | REV1     | Reserved                                                                |
| 18:16  | PORT_UPW | Port-Based User Priority Weight Value<br>Weights range from 0x0 to 0x7. |
| 15     | REV2     | Reserved                                                                |
| 14:12  | DSCP_UPW | DSCP Priority Weight (IPv4)                                             |
| 11     | REV3     | Reserved                                                                |
| 10:8   | TAG_UPW  | Priority Tag User Priority Weight                                       |
| 7      | REV4     | Reserved                                                                |
| 6:4    | STAG_UPW | Special Tag User Priority Weight                                        |
| 3      | REV5     | Reserved                                                                |
| 2:0    | ACL_UPW  | ACL User Priority Weight (ACL Hit)                                      |

**15022144      P1\_PEM1      User priority egress mapping I of P1      10080480**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_1 |    |    | QUE_PFCR_1 |    |    | QUE_PFCT_1 |    |    | DSCP_PRI_1 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 0  | 1  | 0          | 0  | 0  | 0          | 0  | 0  | 0          | 0  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_0 |    |    | QUE_PFCR_0 |    |    | QUE_PFCT_0 |    |    | DSCP_PRI_0 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 0  | 0  | 0          | 1  | 0  | 0          | 1  | 0  | 0          | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_1  | User Priority 1 Priority Tag Value                       |
| 27:25  | QUE_PFCR_1 | User Priority 1 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_1 | User Priority 1 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_1 | User Priority 1 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_0  | User Priority 0 Priority Tag Value                       |
| 11:9   | QUE_PFCR_0 | User Priority 0 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_0 | User Priority 0 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_0 | User Priority 0 DSCP Value                               |

**15022148      P1\_PEM2      User priority egress mapping II of P1      36D82250**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_3 |    |    | QUE_PFCR_3 |    |    | QUE_PFCT_3 |    |    | DSCP_PRI_3 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 1  | 1  | 0          | 1  | 1  | 0          | 1  | 1  | 0          | 1  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_2 |    |    | QUE_PFCR_2 |    |    | QUE_PFCT_2 |    |    | DSCP_PRI_2 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 1  | 0  | 0          | 0  | 1  | 0          | 0  | 1  | 0          | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_3  | User Priority 3 Priority Tag Value                       |
| 27:25  | QUE_PFCR_3 | User Priority 3 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_3 | User Priority 3 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_3 | User Priority 3 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_2  | User Priority 2 Priority Tag Value                       |
| 11:9   | QUE_PFCR_2 | User Priority 2 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_2 | User Priority 2 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_2 | User Priority 2 DSCP Value                               |

**1502214C**      **P1\_PEM3**      **User priority egress mapping III of P1**      **5B684920**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_5 |    |    | QUE_PFCR_5 |    |    | QUE_PFCT_5 |    |    | DSCP_PRI_5 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 0  | 1  | 1          | 0  | 1  | 1          | 0  | 1  | 1          | 0  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_4 |    |    | QUE_PFCR_4 |    |    | QUE_PFCT_4 |    |    | DSCP_PRI_4 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 0  | 0  | 1          | 0  | 0  | 1          | 0  | 0  | 1          | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_5  | User Priority 5 Priority Tag Value                       |
| 27:25  | QUE_PFCR_5 | User Priority 5 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_5 | User Priority 5 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_5 | User Priority 5 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_4  | User Priority 4 Priority Tag Value                       |
| 11:9   | QUE_PFCR_4 | User Priority 4 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_4 | User Priority 4 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_4 | User Priority 4 DSCP Value                               |

**15022150 P1\_PEM4 User priority egress mapping IV of P1 7FF86DB0**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_7 |    |    | QUE_PFCR_7 |    |    | QUE_PFCT_7 |    |    | DSCP_PRI_7 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 1  | 1  | 1          | 1  | 1  | 1          | 1  | 1  | 1          | 1  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_6 |    |    | QUE_PFCR_6 |    |    | QUE_PFCT_6 |    |    | DSCP_PRI_6 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 1  | 0  | 1          | 1  | 0  | 1          | 1  | 0  | 1          | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_7  | User Priority 7 Priority Tag Value                       |
| 27:25  | QUE_PFCR_7 | User Priority 7 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_7 | User Priority 7 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_7 | User Priority 7 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_6  | User Priority 6 Priority Tag Value                       |
| 11:9   | QUE_PFCR_6 | User Priority 6 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_6 | User Priority 6 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_6 | User Priority 6 DSCP Value                               |

15022200      P2\_SSC      STP state control of P2      0000FFFF

| Bit   | 31       | 30 | 29       | 28 | 27       | 26 | 25       | 24 | 23       | 22 | 21       | 20 | 19       | 18 | 17       | 16 |
|-------|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|
| Name  | REVO     |    |          |    |          |    |          |    |          |    |          |    |          |    |          |    |
| Type  | RO       |    |          |    |          |    |          |    |          |    |          |    |          |    |          |    |
| Reset | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  |
| Bit   | 15       | 14 | 13       | 12 | 11       | 10 | 9        | 8  | 7        | 6  | 5        | 4  | 3        | 2  | 1        | 0  |
| Name  | FID7_PST |    | FID6_PST |    | FID5_PST |    | FID4_PST |    | FID3_PST |    | FID2_PST |    | FID1_PST |    | FID0_PST |    |
| Type  | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    |
| Reset | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  |

| Bit(s) | Name     | Description                                                                                                                                                                                                                    |
|--------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | REVO     | <b>Reserved</b>                                                                                                                                                                                                                |
| 15:14  | FID7_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 13:12  | FID6_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 11:10  | FID5_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 9:8    | FID4_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 7:6    | FID3_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)                                                |

| Bit(s) | Name     | Description                                      |
|--------|----------|--------------------------------------------------|
| 5:4    | FID2_PST | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |
|        |          | <b>(Rapid) Spanning Tree Protocol Port State</b> |
|        |          | 2'b00: Disable (STP) / Discard (RSTP)            |
|        |          | 2'b01: Listening (STP) / Discard (RSTP)          |
|        |          | 2'b10: Learning (STP) / Learning (RSTP)          |
| 3:2    | FID1_PST | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |
|        |          | <b>(Rapid) Spanning Tree Protocol Port State</b> |
|        |          | 2'b00: Disable (STP) / Discard (RSTP)            |
|        |          | 2'b01: Listening (STP) / Discard (RSTP)          |
|        |          | 2'b10: Learning (STP) / Learning (RSTP)          |
| 1:0    | FID0_PST | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |
|        |          | <b>(Rapid) Spanning Tree Protocol Port State</b> |
|        |          | 2'b00: Disable (STP) / Discard (RSTP)            |
|        |          | 2'b01: Listening (STP) / Discard (RSTP)          |
|        |          | 2'b10: Learning (STP) / Learning (RSTP)          |
|        |          | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |

**15022204      P2\_PCR      Port control of P2      00FF2000**

| Bit   | 31   | 30       | 29     | 28         | 27        | 26       | 25         | 24         | 23          | 22          | 21 | 20 | 19   | 18       | 17        | 16 |
|-------|------|----------|--------|------------|-----------|----------|------------|------------|-------------|-------------|----|----|------|----------|-----------|----|
| Name  | REV0 | MLDv2_EN | EG_TAG |            | REV1      | PORT_PRI |            |            | PORT_MATRIX |             |    |    |      |          |           |    |
| Type  | RW   | RW       | RW     |            | RW        | RW       |            |            | RW          |             |    |    |      |          |           |    |
| Reset | 0    | 0        | 0      | 0          | 0         | 0        | 0          | 0          | 1           | 1           | 1  | 1  | 1    | 1        | 1         | 1  |
| Bit   | 15   | 14       | 13     | 12         | 11        | 10       | 9          | 8          | 7           | 6           | 5  | 4  | 3    | 2        | 1         | 0  |
| Name  | REV2 |          |        | UP2DSCP_EN | UP2TAG_EN | ACL_EN   | PORT_TX_MR | PORT_RX_MR | ACL_MR      | MIS_PORT_FW |    |    | REV3 | VLAN_MIS | PORT_VLAN |    |
| Type  | RW   |          |        | RW         | RW        | RW       | RW         | RW         | RW          | RW          |    |    | RW   | RW       | RW        |    |
| Reset | 0    | 0        | 1      | 0          | 0         | 0        | 0          | 0          | 0           | 0           | 0  | 0  | 0    | 0        | 0         | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                     |
|--------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | REV0        | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 30     | MLDv2_EN    | <b>IPv6 MLDv2 source address multicast forwarding enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                 |
| 29:28  | EG_TAG      | <b>Port-Based Egress VLAN Tag Attribution</b><br><br>2'b00: Untagged<br><br>2'b01: Swap<br><br>2'b10: Tagged<br><br>2'b11: Stack                                                                                                                                                |
| 27     | REV1        | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 26:24  | PORT_PRI    | <b>Port-based User Priority</b><br><br>User priority for the ingress port                                                                                                                                                                                                       |
| 23:16  | PORT_MATRIX | <b>Port Matrix Member</b><br><br>The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member.<br><br>NOTE: The final and effective port member should exclude the received port. |
| 15:13  | REV2        | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 12     | UP2DSCP_EN  | <b>User Priority to DSCP Enable</b><br><br>Replace DSCP according to user priority.<br><br>0: Disable<br><br>1: Enable                                                                                                                                                          |
| 11     | UP2TAG_EN   | <b>User Priority to Tag Enable</b><br><br>Replace 802.Q priority by user priority                                                                                                                                                                                               |



| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |             | 0: Disable                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |             | 1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 10     | ACL_EN      | <b>Port-based ACL Enable</b><br>0: Bypass the ACL Table.<br>1: Lookup the ACL Table and take the corresponding actions.                                                                                                                                                                                                                                                                                                                        |
| 9      | PORT_TX_MIR | <b>Port Tx Mirror Enable</b><br>All frames transmitted from this port are copied to the mirror port.<br>[NOTE] Multi-port support is possible.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                      |
| 8      | PORT_RX_MIR | <b>Port Rx Mirror Enable</b><br>All frames received from this port are copied to the mirror port.<br>[NOTE] Multi-port support is possible.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                         |
| 7      | ACL_MIR     | <b>ACL Mismatch to Mirror Port</b><br>Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                     |
| 6:4    | MIS_PORT_FW | <b>ACL Mismatch TO_CPU Forward</b><br>Frame port forwarding when ACL table is enabled and the frame is mismatched<br>3'b0xx: System default (disabled)<br>3'b100: System default and CPU port excluded<br>3'b101: System default and CPU port included<br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.)<br>3'b111: Frame dropped |
| 3      | REV3        | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 2      | VLAN_MIS    | <b>VLAN Mismatch to Mirror Port</b><br>1'b0: Frame processed according to PORT_VLAN.<br>1'b1: VLAN mismatched frame copied to MIRROR port.                                                                                                                                                                                                                                                                                                     |

| Bit(s) | Name      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|--------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0    | PORT_VLAN | <b>Port-based VLAN Mechanism Select</b><br><br>2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member.<br><br>2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member.<br><br>2'b10: Check Mode. Forward received frames whose ingress port does not belong to the VLAN member. But, discard frames if VID is missed on the VLAN table.<br><br>2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table. |

15022208      P2\_PIC      Port IGMP control of P2      00008000

| Bit   | 31         | 30 | 29           | 28            | 27   | 26       | 25    | 24    | 23           | 22            | 21          | 20           | 19          | 18           | 17          | 16           |
|-------|------------|----|--------------|---------------|------|----------|-------|-------|--------------|---------------|-------------|--------------|-------------|--------------|-------------|--------------|
| Name  | REVO       |    |              |               |      |          |       |       |              |               |             |              | IGMP_MIR    | IGMP_MIS     |             |              |
| Type  | RO         |    |              |               |      |          |       |       |              |               |             |              | RW          | RW           |             |              |
| Reset | 0          | 0  | 0            | 0             | 0    | 0        | 0     | 0     | 0            | 0             | 0           | 0            | 0           | 0            | 0           | 0            |
| Bit   | 15         | 14 | 13           | 12            | 11   | 10       | 9     | 8     | 7            | 6             | 5           | 4            | 3           | 2            | 1           | 0            |
| Name  | ROBUST_VAR |    | MLD_HW_LEAVE | IGMP_HW_LEAVE | REV1 | IPM22_44 | IPM33 | IPM01 | MLD2_JOIN_EN | IGMP3_JOIN_EN | MLD_JOIN_EN | IGMP_JOIN_EN | MLD_SQRY_EN | IGMP_SQRY_EN | MLD_GQRY_EN | IGMP_GQRY_EN |
| Type  | RW         |    | RW           | RW            | RW   | RW       | RW    | RW    | RW           | RW            | RW          | RW           | RW          | RW           | RW          | RW           |
| Reset | 1          | 0  | 0            | 0             | 0    | 0        | 0     | 0     | 0            | 0             | 0           | 0            | 0           | 0            | 0           | 0            |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20  | REVO       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 19     | IGMP_MIR   | <b>IP Multicast IGMP Table Mismatch to Mirror Port</b><br><br>Copy IP multicast frames with an IGMP table mismatch to the mirror port.<br><br>[NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis.<br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                     |
| 18:16  | IGMP_MIS   | <b>IP Multicast "TO_CPU" Forwarding</b><br><br>Select how to forward IP multicast frames when the IGMP table is mismatched.<br><br>[NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis.<br><br>3'b0xx: System default (By MFC.UNM_FFP)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.)<br><br>3'b111: Frame dropped |
| 15:14  | ROBUST_VAR | <b>Robustness Variable</b><br><br>Define the number of times an IGMP report message may be lost consecutively.<br><br>0: Unlimited (No Age out)<br><br>1: One time<br><br>2: Twice (default)<br><br>3: Three times                                                                                                                                                                                                                                                                                                                                                                        |

| Bit(s) | Name          | Description                                                                                                                                                                                                                         |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13     | MLD_HW_LEAVE  | <b>MLD HW Leave Enable</b><br><br>Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query.<br><br>0: Disable<br><br>1: Enable      |
| 12     | IGMP_HW_LEAVE | <b>IGMP HW Leave Enable</b><br><br>Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query.<br><br>0: Disable<br><br>1: Enable   |
| 11     | REV1          | <b>Reserved</b>                                                                                                                                                                                                                     |
| 10     | IPM_2244      | <b>IP Multicast frame for DIP is Class D: 224.x.x.x to 239.x.x.x</b><br><br>0: This frame is regarded as a normal multicast and search ADDR Table.<br><br>1: This frame is regarded as an IP multicast frame and search IGMP table. |
| 9      | IPM_33        | <b>IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx</b><br><br>0: This frame is regarded as normal multicast and search ADDR table.<br><br>1: This frame is regarded as IP multicast frame and search IGMP table.                 |
| 8      | IPM_01        | <b>IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx</b><br><br>0: This frame is regarded as normal multicast and search ADDR Table.<br><br>1: This frame is regarded as IP multicast frame and search IGMP table.                 |
| 7      | MLD2_JOIN_EN  | <b>MLD v2 HW Join Enable</b><br><br>Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX().<br><br>0: Disable<br><br>1: Enable             |
| 6      | IGMP3_JOIN_EN | <b>IGMP v3 HW Join Enable</b><br><br>Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX().<br><br>0: Disable<br><br>1: Enable            |
| 5      | MLD_JOIN_EN   | <b>MLD Snooping HW Join Enable</b>                                                                                                                                                                                                  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                 |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame.                                                                                                                                                           |
|        |              | 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).                                                                                                                                                 |
| 4      | IGMP_JOIN_EN | <b>IGMP Snooping HW Join Enable</b><br><br>Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically.<br><br>0: Disable<br><br>1: Enable                                                             |
| 3      | MLD_SQRY_EN  | <b>MLD HW Specific Query Enable</b><br><br>0: MLD specific query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the MLD specific query message to refresh the specific multicast member.    |
| 2      | IGMP_SQRY_EN | <b>IGMP HW Specific Query Enable</b><br><br>0: IGMP specific query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member. |
| 1      | MLD_GQRY_EN  | <b>MLD HW General Query Enable</b><br><br>0: MLD general query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the MLD general query message to refresh the multicast member.                |
| 0      | IGMP_GQRY_EN | <b>IGMP HW General Query Enable</b><br><br>0: IGMP general Query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.             |

**1502220C      P2\_PSC      Port security control of P2      000FFF00**

| Bit          | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23   | 22 | 21        | 20     | 19         | 18 | 17           | 16           |
|--------------|------------|----|----|----|----|----|----|----|------|----|-----------|--------|------------|----|--------------|--------------|
| <b>Name</b>  | SA_LRN_CNT |    |    |    |    |    |    |    |      |    |           |        | MAC_SA_LRN |    |              |              |
| <b>Type</b>  | RO         |    |    |    |    |    |    |    |      |    |           |        | RW         |    |              |              |
| <b>Reset</b> | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0    | 0  | 0         | 0      | 1          | 1  | 1            | 1            |
| Bit          | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7    | 6  | 5         | 4      | 3          | 2  | 1            | 0            |
| <b>Name</b>  | MAC_SA_LRN |    |    |    |    |    |    |    | REVO |    | SA_CNT_EN | SA_DIS | SA_LOCK    |    | TX_PORT_LOCK | RX_PORT_LOCK |
| <b>Type</b>  | RW         |    |    |    |    |    |    |    | RW   |    | RW        | RW     | RW         |    | RW           | RW           |
| <b>Reset</b> | 1          | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0    | 0  | 0         | 0      | 0          | 0  | 0            | 0            |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20  | SA_LRN_CNT | <b>Learned Source Address Number</b>                                                                                                                                                                                                                                                                                                                                                                                             |
| 19:8   | MAC_SA_LRN | <b>Rx SA Allowable Learning Number</b><br><br>Sets the maximum number of SA learned addresses when SA_CNT_EN is set.<br><br>12'h0: Disable SA learning<br><br>12'h1:<br><br>12'hFFE: 1 to 4094 address table<br><br>12'hFFF: SA Learning without limitation                                                                                                                                                                      |
| 7:6    | REVO       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 5      | SA_CNT_EN  | <b>SA Counter Enable</b><br><br>Enable the learned source MAC Address counter.<br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                                                                                                                |
| 4      | SA_DIS     | <b>SA Disable</b><br><br>Disable source MAC address learning.<br><br>0: Enable<br><br>1: Disable                                                                                                                                                                                                                                                                                                                                 |
| 3:2    | SA_LOCK    | <b>SA Lock Select</b><br><br>[NOTE] PAE frames should be passed and are not affected by SA Lock.<br><br>2'b00: Receive without SA authorization.<br><br>2'b01: All received frames whose SA look-up is missing or are not port members in the ARL will be dropped.<br><br>2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). |

| Bit(s) | Name         | Description                                                                                                                                                                  |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)                         |
| 1      | TX_PORT_LOCK | <b>Tx Port Lock Enable</b><br><br>[NOTE] PAE Frames should be passed and are not affected by Port Lock.<br><br>0: Transmit authorized.<br><br>1: Disable frame transmission. |
| 0      | RX_PORT_LOCK | <b>Rx Port Lock Enable</b><br><br>[NOTE] PAE frames should be passed and are not affected by Port Lock.<br><br>0: Receive authorized.<br><br>1: Disable frame receiving.     |

**15022210 P2\_PVC Port VLAN control of P2 810000C0**

| Bit          | 31           | 30             | 29             | 28   | 27            | 26     | 25 | 24 | 23        | 22 | 21            | 20              | 19             | 18             | 17      | 16 |
|--------------|--------------|----------------|----------------|------|---------------|--------|----|----|-----------|----|---------------|-----------------|----------------|----------------|---------|----|
| <b>Name</b>  | STAG_VPID    |                |                |      |               |        |    |    |           |    |               |                 |                |                |         |    |
| <b>Type</b>  | RW           |                |                |      |               |        |    |    |           |    |               |                 |                |                |         |    |
| <b>Reset</b> | 1            | 0              | 0              | 0    | 0             | 0      | 0  | 1  | 0         | 0  | 0             | 0               | 0              | 0              | 0       | 0  |
| Bit          | 15           | 14             | 13             | 12   | 11            | 10     | 9  | 8  | 7         | 6  | 5             | 4               | 3              | 2              | 1       | 0  |
| <b>Name</b>  | DIS_PV<br>ID | FORCE<br>_PVID | BC_LKY<br>V_EN | REVO | PT_OP<br>TION | EG_TAG |    |    | VLAN_ATTR |    | PORT_<br>STAG | IPM_LK<br>YV_EN | MC_LK<br>YV_EN | UC_LKY<br>V_EN | ACC_FRM |    |
| <b>Type</b>  | RW           | RW             | RW             | RW   | RW            | RW     |    |    | RW        |    | RW            | RW              | RW             | RW             | RW      |    |
| <b>Reset</b> | 0            | 0              | 0              | 0    | 0             | 0      | 0  | 0  | 1         | 1  | 0             | 0               | 0              | 0              | 0       | 0  |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                            |
|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | STAG_VPID  | <b>Stack Tag VPID (VLAN Protocol ID) Value</b><br><br>The received frame will be regarded as a legal stack tag frame if the following conditions are matched:<br><br>Outer VPID == STAG_VPID<br><br>Inner VPID == 16'h8100<br><br>The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID. |
| 15     | DIS_PVID   | <b>PVID Disable</b><br><br>Disable PVID insertion in priority-tagged frames.<br><br>0: Use PVID for priority-tagged frames.<br><br>1: Keep VID=0 for priority-tagged frames.                                                                                                                                                           |
| 14     | FORCE_PVID | <b>Force PVID on VLAN-tagged frames</b><br><br>0: Use VID in VLAN-tagged frame.<br><br>1: Force the replacement of VID with PVID.                                                                                                                                                                                                      |
| 13     | BC_LKYV_EN | <b>Broadcast Leaky VLAN Enable</b><br><br>0: Broadcast frames received by this port will be blocked by VLAN.<br><br>1: Broadcast frames received by this port can pass through VLAN.                                                                                                                                                   |
| 12     | REVO       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                        |
| 11     | PT_OPTION  | <b>Pass-through capability on TX special tag</b><br><br>0: Disable pass-through on TX special tag<br><br>1: Enable pass-through on TX special tag                                                                                                                                                                                      |
| 10:8   | EG_TAG     | <b>Incoming Port Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disabled)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged                                                                                                                                                            |



| Bit(s) | Name        | Description                                                                                                                                       |
|--------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
|        |             | 3'b101: Swap                                                                                                                                      |
|        |             | 3'b110: Tagged                                                                                                                                    |
|        |             | 3'b111: Stack                                                                                                                                     |
| 7:6    | VLAN_ATTR   | <b>VLAN Port Attribute</b>                                                                                                                        |
|        |             | 2'b00: User port                                                                                                                                  |
|        |             | 2'b01: Stack port                                                                                                                                 |
|        |             | 2'b10: Translation port                                                                                                                           |
|        |             | 2'b11: Transparent port                                                                                                                           |
| 5      | PORT_STAG   | <b>Special Tag Enable</b>                                                                                                                         |
|        |             | Enable a proprietary VLAN tag format to carry additional information to the remote port.                                                          |
|        |             | 0: No special tag format for Tx/Rx                                                                                                                |
|        |             | 1: Enable                                                                                                                                         |
| 4      | IPM_LKYV_EN | <b>IP Multicast Leaky VLAN Enable</b>                                                                                                             |
|        |             | (note*) If MC_LKYV_EN is set, this field will become "don't care" bit. All multicast frames including IP_Multi will be leaky between VLAN groups. |
|        |             | 0: IP_Multi frames received by this port will be blocked by VLAN.                                                                                 |
|        |             | 1: IP_Multi frames received by this port can pass through VLAN.                                                                                   |
| 3      | MC_LKYV_EN  | <b>Multicast Leaky VLAN Enable</b>                                                                                                                |
|        |             | 0: Multicast frames received by this port will be blocked by VLAN.                                                                                |
|        |             | 1: Multicast frames received by this port can pass through VLAN.                                                                                  |
| 2      | UC_LKYV_EN  | <b>Unicast Leaky VLAN Enable</b>                                                                                                                  |
|        |             | 0: Unicast frame received by this port will be blocked by VLAN.                                                                                   |
|        |             | 1: Unicast frame received by this port can pass through VLAN.                                                                                     |
| 1:0    | ACC_FRM     | <b>Acceptable Frame Type</b>                                                                                                                      |
|        |             | 2'b00: Admit All frames                                                                                                                           |
|        |             | 2'b01: Admit Only VLAN-tagged frames                                                                                                              |
|        |             | 2'b10: Admit only untagged or priority-tagged frames.                                                                                             |
|        |             | 2'b11: Reserved                                                                                                                                   |

15022214      P2\_PPBV1      Port-and-Protocol based VLAN I of P2      00010001

| Bit          | 31          | 30 | 29 | 28   | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------|----|----|------|-------------|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | G1_PORT_PRI |    |    | REV0 | G1_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW          |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0           | 0  | 0  | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| Bit          | 15          | 14 | 13 | 12   | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | G0_PORT_PRI |    |    | REV1 | G0_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW          |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0           | 0  | 0  | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name        | Description                                                                                                                                    |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29  | G1_PORT_PRI | <b>Group 1 Port Priority (optional)</b><br><br>The Group 1 Priority for each port according to IEEE 802.1Q definition                          |
| 28     | REV0        | <b>Reserved</b>                                                                                                                                |
| 27:16  | G1_PORT_VID | <b>Group 1 Port VLAN ID (optional)</b><br><br>The Group 1 VID for each port according to IEEE 802.1Q definition                                |
| 15:13  | G0_PORT_PRI | <b>Group 0 Port Priority (Default Port Priority)</b><br><br>The Group 0 and default Priority for each port according to IEEE 802.1Q definition |
| 12     | REV1        | <b>Reserved</b>                                                                                                                                |
| 11:0   | G0_PORT_VID | <b>Group 0 Port VLAN ID (Default Port VID)</b><br><br>The Group 0 and default VID for each port according to IEEE 802.1Q definition            |

15022218      P2\_PPBV2      Port-and-Protocol based VLAN II of P2      00010001

| Bit   | 31          | 30 | 29 | 28   | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|------|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |             |    |    | REV0 | G3_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| Bit   | 15          | 14 | 13 | 12   | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | G2_PORT_PRI |    |    | REV1 | G2_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name        | Description                                                                                                           |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------|
| 28     | REV0        | Reserved                                                                                                              |
| 27:16  | G3_PORT_VID | <b>Group 3 Port VLAN ID (optional)</b><br><br>The Group 3 VID for each port according to IEEE 802.1Q definition       |
| 15:13  | G2_PORT_PRI | <b>Group 2 Port Priority (optional)</b><br><br>The Group 2 Priority for each port according to IEEE 802.1Q definition |
| 12     | REV1        | Reserved                                                                                                              |
| 11:0   | G2_PORT_VID | <b>Group 2 Port VLAN ID (optional)</b><br><br>The Group 2 VID for each port according to IEEE 802.1Q definition       |

1502221C      P2\_BSR      Broadcast storm rate control of P2      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
| 7:0    | STORM_10M  | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
|        |            | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
| 7:0    | STORM_10M  | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
| 7:0    | STORM_10M  | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |

15022220      P2\_STAG01      STAG index 0/1 of P2      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REVO |    |    |    |      |    |    |    | VID1 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID1 |    |    |    | VID0 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID1 | VLAN Identifier for STAG index 1 |
| 11:0   | VID0 | VLAN Identifier for STAG index 0 |

15022224      P2\_STAG23      STAG index 2/3 of P2      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REVO |    |    |    |      |    |    |    | VID3 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID3 |    |    |    | VID2 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID3 | VLAN Identifier for STAG index 3 |
| 11:0   | VID2 | VLAN Identifier for STAG index 2 |

15022228      P2\_STAG45      STAG index 4/5 of P2      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REV0 |    |    |    |      |    |    |    | VID5 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID5 |    |    |    | VID4 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REV0 | Reserved                         |
| 23:12  | VID5 | VLAN Identifier for STAG index 5 |
| 11:0   | VID4 | VLAN Identifier for STAG index 4 |



1502222C      P2\_STAG67      STAG index 6/7 of P2      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REVO |    |    |    |      |    |    |    | VID7 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID7 |    |    |    | VID6 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID7 | VLAN Identifier for STAG index 7 |
| 11:0   | VID6 | VLAN Identifier for STAG index 6 |

15022230      P2\_BSR\_EXT1      Broadcast storm rate control I of P2      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
| 7:0    | STORM_10M  | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
|        |            | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |

15022234      **P2\_BSR\_EXT2**      Broadcast storm rate control II of P2      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
| 7:0    | STORM_10M  | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            |                                                         |

15022238      P2\_BSR\_EXT3      Broadcast storm rate control III of P2      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
| 7:0    | STORM_10M  | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
|        |            | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |

**15022240      P2\_UPW      User priority weight of P2      00234567**

| Bit   | 31   | 30       | 29 | 28 | 27   | 26      | 25 | 24 | 23   | 22       | 21 | 20 | 19   | 18       | 17 | 16 |
|-------|------|----------|----|----|------|---------|----|----|------|----------|----|----|------|----------|----|----|
| Name  |      |          |    |    |      |         |    |    | REV0 | ARL_UPW  |    |    | REV1 | PORT_UPW |    |    |
| Type  |      |          |    |    |      |         |    |    | RW   | RW       |    |    | RW   | RW       |    |    |
| Reset |      |          |    |    |      |         |    |    | 0    | 0        | 1  | 0  | 0    | 0        | 1  | 1  |
| Bit   | 15   | 14       | 13 | 12 | 11   | 10      | 9  | 8  | 7    | 6        | 5  | 4  | 3    | 2        | 1  | 0  |
| Name  | REV2 | DSCP_UPW |    |    | REV3 | TAG_UPW |    |    | REV4 | STAG_UPW |    |    | REV5 | ACL_UPW  |    |    |
| Type  | RW   | RW       |    |    | RW   | RW      |    |    | RW   | RW       |    |    | RW   | RW       |    |    |
| Reset | 0    | 1        | 0  | 0  | 0    | 1       | 0  | 1  | 0    | 1        | 1  | 0  | 0    | 1        | 1  | 1  |

| Bit(s) | Name     | Description                                                             |
|--------|----------|-------------------------------------------------------------------------|
| 23     | REV0     | Reserved                                                                |
| 22:20  | ARL_UPW  | ARL User Priority Weight (MAC/DIP Hit)                                  |
| 19     | REV1     | Reserved                                                                |
| 18:16  | PORT_UPW | Port-Based User Priority Weight Value<br>Weights range from 0x0 to 0x7. |
| 15     | REV2     | Reserved                                                                |
| 14:12  | DSCP_UPW | DSCP Priority Weight (IPv4)                                             |
| 11     | REV3     | Reserved                                                                |
| 10:8   | TAG_UPW  | Priority Tag User Priority Weight                                       |
| 7      | REV4     | Reserved                                                                |
| 6:4    | STAG_UPW | Special Tag User Priority Weight                                        |
| 3      | REV5     | Reserved                                                                |
| 2:0    | ACL_UPW  | ACL User Priority Weight (ACL Hit)                                      |



**1502244 P2\_PEM1 User priority egress mapping I of P2 10080480**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_1 |    |    | QUE_PFCR_1 |    |    | QUE_PFCT_1 |    |    | DSCP_PRI_1 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 0  | 1  | 0          | 0  | 0  | 0          | 0  | 0  | 0          | 0  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_0 |    |    | QUE_PFCR_0 |    |    | QUE_PFCT_0 |    |    | DSCP_PRI_0 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 0  | 0  | 0          | 1  | 0  | 0          | 1  | 0  | 0          | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_1  | User Priority 1 Priority Tag Value                       |
| 27:25  | QUE_PFCR_1 | User Priority 1 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_1 | User Priority 1 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_1 | User Priority 1 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_0  | User Priority 0 Priority Tag Value                       |
| 11:9   | QUE_PFCR_0 | User Priority 0 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_0 | User Priority 0 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_0 | User Priority 0 DSCP Value                               |

**15022248      P2\_PEM2      User priority egress mapping II of P2      36D82250**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_3 |    |    | QUE_PFCR_3 |    |    | QUE_PFCT_3 |    |    | DSCP_PRI_3 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 1  | 1  | 0          | 1  | 1  | 0          | 1  | 1  | 0          | 1  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_2 |    |    | QUE_PFCR_2 |    |    | QUE_PFCT_2 |    |    | DSCP_PRI_2 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 1  | 0  | 0          | 0  | 1  | 0          | 0  | 1  | 0          | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_3  | User Priority 3 Priority Tag Value                       |
| 27:25  | QUE_PFCR_3 | User Priority 3 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_3 | User Priority 3 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_3 | User Priority 3 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_2  | User Priority 2 Priority Tag Value                       |
| 11:9   | QUE_PFCR_2 | User Priority 2 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_2 | User Priority 2 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_2 | User Priority 2 DSCP Value                               |

**1502224C      P2\_PEM3      User priority egress mapping III of P2      5B684920**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_5 |    |    | QUE_PFCR_5 |    |    | QUE_PFCT_5 |    |    | DSCP_PRI_5 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 0  | 1  | 1          | 0  | 1  | 1          | 0  | 1  | 1          | 0  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_4 |    |    | QUE_PFCR_4 |    |    | QUE_PFCT_4 |    |    | DSCP_PRI_4 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 0  | 0  | 1          | 0  | 0  | 1          | 0  | 0  | 1          | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_5  | User Priority 5 Priority Tag Value                       |
| 27:25  | QUE_PFCR_5 | User Priority 5 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_5 | User Priority 5 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_5 | User Priority 5 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_4  | User Priority 4 Priority Tag Value                       |
| 11:9   | QUE_PFCR_4 | User Priority 4 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_4 | User Priority 4 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_4 | User Priority 4 DSCP Value                               |

**15022250      P2\_PEM4      User priority egress mapping IV of P2      7FF86DB0**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_7 |    |    | QUE_PFCR_7 |    |    | QUE_PFCT_7 |    |    | DSCP_PRI_7 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 1  | 1  | 1          | 1  | 1  | 1          | 1  | 1  | 1          | 1  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_6 |    |    | QUE_PFCR_6 |    |    | QUE_PFCT_6 |    |    | DSCP_PRI_6 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 1  | 0  | 1          | 1  | 0  | 1          | 1  | 0  | 1          | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_7  | User Priority 7 Priority Tag Value                       |
| 27:25  | QUE_PFCR_7 | User Priority 7 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_7 | User Priority 7 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_7 | User Priority 7 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_6  | User Priority 6 Priority Tag Value                       |
| 11:9   | QUE_PFCR_6 | User Priority 6 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_6 | User Priority 6 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_6 | User Priority 6 DSCP Value                               |

15022300      P3\_SSC      STP state control of P3      0000FFFF

| Bit   | 31       | 30 | 29       | 28 | 27       | 26 | 25       | 24 | 23       | 22 | 21       | 20 | 19       | 18 | 17       | 16 |
|-------|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|
| Name  | REVO     |    |          |    |          |    |          |    |          |    |          |    |          |    |          |    |
| Type  | RO       |    |          |    |          |    |          |    |          |    |          |    |          |    |          |    |
| Reset | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  |
| Bit   | 15       | 14 | 13       | 12 | 11       | 10 | 9        | 8  | 7        | 6  | 5        | 4  | 3        | 2  | 1        | 0  |
| Name  | FID7_PST |    | FID6_PST |    | FID5_PST |    | FID4_PST |    | FID3_PST |    | FID2_PST |    | FID1_PST |    | FID0_PST |    |
| Type  | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    |
| Reset | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  |

| Bit(s) | Name     | Description                                                                                                                                                                                                                    |
|--------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | REVO     | <b>Reserved</b>                                                                                                                                                                                                                |
| 15:14  | FID7_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 13:12  | FID6_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 11:10  | FID5_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 9:8    | FID4_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 7:6    | FID3_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)                                                |

| Bit(s) | Name     | Description                                      |
|--------|----------|--------------------------------------------------|
| 5:4    | FID2_PST | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |
|        |          | <b>(Rapid) Spanning Tree Protocol Port State</b> |
|        |          | 2'b00: Disable (STP) / Discard (RSTP)            |
|        |          | 2'b01: Listening (STP) / Discard (RSTP)          |
|        |          | 2'b10: Learning (STP) / Learning (RSTP)          |
| 3:2    | FID1_PST | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |
|        |          | <b>(Rapid) Spanning Tree Protocol Port State</b> |
|        |          | 2'b00: Disable (STP) / Discard (RSTP)            |
|        |          | 2'b01: Listening (STP) / Discard (RSTP)          |
|        |          | 2'b10: Learning (STP) / Learning (RSTP)          |
| 1:0    | FID0_PST | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |
|        |          | <b>(Rapid) Spanning Tree Protocol Port State</b> |
|        |          | 2'b00: Disable (STP) / Discard (RSTP)            |
|        |          | 2'b01: Listening (STP) / Discard (RSTP)          |
|        |          | 2'b10: Learning (STP) / Learning (RSTP)          |
|        |          | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |

15022304      **P3\_PCR**      Port control of P3      00FF2000

| Bit   | 31   | 30       | 29     | 28         | 27        | 26       | 25         | 24         | 23          | 22          | 21 | 20 | 19   | 18       | 17        | 16 |
|-------|------|----------|--------|------------|-----------|----------|------------|------------|-------------|-------------|----|----|------|----------|-----------|----|
| Name  | REV0 | MLDv2_EN | EG_TAG |            | REV1      | PORT_PRI |            |            | PORT_MATRIX |             |    |    |      |          |           |    |
| Type  | RW   | RW       | RW     |            | RW        | RW       |            |            | RW          |             |    |    |      |          |           |    |
| Reset | 0    | 0        | 0      | 0          | 0         | 0        | 0          | 0          | 1           | 1           | 1  | 1  | 1    | 1        | 1         | 1  |
| Bit   | 15   | 14       | 13     | 12         | 11        | 10       | 9          | 8          | 7           | 6           | 5  | 4  | 3    | 2        | 1         | 0  |
| Name  | REV2 |          |        | UP2DSCP_EN | UP2TAG_EN | ACL_EN   | PORT_TX_MR | PORT_RX_MR | ACL_MR      | MIS_PORT_FW |    |    | REV3 | VLAN_MIS | PORT_VLAN |    |
| Type  | RW   |          |        | RW         | RW        | RW       | RW         | RW         | RW          | RW          |    |    | RW   | RW       | RW        |    |
| Reset | 0    | 0        | 1      | 0          | 0         | 0        | 0          | 0          | 0           | 0           | 0  | 0  | 0    | 0        | 0         | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                     |
|--------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | REV0        | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 30     | MLDv2_EN    | <b>IPv6 MLDv2 source address multicast forwarding Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                 |
| 29:28  | EG_TAG      | <b>Port-Based Egress VLAN Tag Attribution</b><br><br>2'b00: Untagged<br><br>2'b01: Swap<br><br>2'b10: Tagged<br><br>2'b11: Stack                                                                                                                                                |
| 27     | REV1        | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 26:24  | PORT_PRI    | <b>Port-based User Priority</b><br><br>User priority for the ingress port                                                                                                                                                                                                       |
| 23:16  | PORT_MATRIX | <b>Port Matrix Member</b><br><br>The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member.<br><br>NOTE: The final and effective port member should exclude the received port. |
| 15:13  | REV2        | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 12     | UP2DSCP_EN  | <b>User Priority to DSCP Enable</b><br><br>Replace DSCP according to user priority.<br><br>0: Disable<br><br>1: Enable                                                                                                                                                          |
| 11     | UP2TAG_EN   | <b>User Priority to Tag Enable</b><br><br>Replace 802.Q priority by user priority.                                                                                                                                                                                              |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |             | 0: Disable                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |             | 1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 10     | ACL_EN      | <b>Port-based ACL Enable</b><br>0: Bypass the ACL Table.<br>1: Lookup the ACL Table and take the corresponding actions.                                                                                                                                                                                                                                                                                                                        |
| 9      | PORT_TX_MIR | <b>Port Tx Mirror Enable</b><br>All frames transmitted from this port are copied to the mirror port.<br>[NOTE] Multi-port support is possible.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                      |
| 8      | PORT_RX_MIR | <b>Port Rx Mirror Enable</b><br>All frames received from this port are copied to the mirror port.<br>[NOTE] Multi-port support is possible.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                         |
| 7      | ACL_MIR     | <b>ACL Mismatch to Mirror Port</b><br>Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                     |
| 6:4    | MIS_PORT_FW | <b>ACL Mismatch TO_CPU Forward</b><br>Frame port forwarding when ACL table is enabled and the frame is mismatched<br>3'b0xx: System default (disabled)<br>3'b100: System default and CPU port excluded<br>3'b101: System default and CPU port included<br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.)<br>3'b111: Frame dropped |
| 3      | REV3        | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 2      | VLAN_MIS    | <b>VLAN Mismatch to Mirror Port</b><br>1'b0: Frame processed according to PORT_VLAN.<br>1'b1: VLAN mismatched frame copied to MIRROR port.                                                                                                                                                                                                                                                                                                     |



| Bit(s) | Name      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|--------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0    | PORT_VLAN | <b>Port-based VLAN Mechanism Select</b><br><br>2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member.<br><br>2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member.<br><br>2'b10: Check Mode. Forward received frames whose ingress port does not belong to the VLAN member. But, discard frames if VID is missed on the VLAN table.<br><br>2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table. |

15022308      P3\_PIC      Port IGMP control of P3      00008000

| Bit   | 31         | 30 | 29           | 28            | 27   | 26       | 25    | 24    | 23          | 22            | 21         | 20          | 19         | 18           | 17         | 16           |
|-------|------------|----|--------------|---------------|------|----------|-------|-------|-------------|---------------|------------|-------------|------------|--------------|------------|--------------|
| Name  | REVO       |    |              |               |      |          |       |       |             |               |            |             | IGMP_MIR   | IGMP_MIS     |            |              |
| Type  | RO         |    |              |               |      |          |       |       |             |               |            |             | RW         | RW           |            |              |
| Reset | 0          | 0  | 0            | 0             | 0    | 0        | 0     | 0     | 0           | 0             | 0          | 0           | 0          | 0            | 0          | 0            |
| Bit   | 15         | 14 | 13           | 12            | 11   | 10       | 9     | 8     | 7           | 6             | 5          | 4           | 3          | 2            | 1          | 0            |
| Name  | ROBUST_VAR |    | MLD_HW_LEAVE | IGMP_HW_LEAVE | REV1 | IPM22_44 | IPM33 | IPM01 | MLD2_JOIN_N | IGMP3_JOIN_EN | MLD_JOIN_N | IGMP_JOIN_N | MLD_SQRY_N | IGMP_SQRY_EN | MLD_GQRY_N | IGMP_GQRY_EN |
| Type  | RW         |    | RW           | RW            | RW   | RW       | RW    | RW    | RW          | RW            | RW         | RW          | RW         | RW           | RW         | RW           |
| Reset | 1          | 0  | 0            | 0             | 0    | 0        | 0     | 0     | 0           | 0             | 0          | 0           | 0          | 0            | 0          | 0            |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20  | REVO       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 19     | IGMP_MIR   | <b>IP Multicast IGMP Table Mismatch to Mirror Port</b><br><br>Copy IP multicast frames with an IGMP table mismatch to the mirror port.<br><br>[NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis.<br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                     |
| 18:16  | IGMP_MIS   | <b>IP Multicast "TO_CPU" Forwarding</b><br><br>Select how to forward IP multicast frames when the IGMP table is mismatched.<br><br>[NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis.<br><br>3'b0xx: System default (By MFC.UNM_FFP)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.)<br><br>3'b111: Frame dropped |
| 15:14  | ROBUST_VAR | <b>Robustness Variable</b><br><br>Define the number of times an IGMP report message may be lost consecutively.<br><br>0: Unlimited (No Age out)<br><br>1: One time<br><br>2: Twice (default)<br><br>3: Three times                                                                                                                                                                                                                                                                                                                                                                        |

| Bit(s) | Name          | Description                                                                                                                                                                                                                         |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13     | MLD_HW_LEAVE  | <b>MLD HW Leave Enable</b><br><br>Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query.<br><br>0: Disable<br><br>1: Enable      |
| 12     | IGMP_HW_LEAVE | <b>IGMP HW Leave Enable</b><br><br>Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query.<br><br>0: Disable<br><br>1: Enable   |
| 11     | REV1          | <b>Reserved</b>                                                                                                                                                                                                                     |
| 10     | IPM_2244      | <b>IP Multicast frame for DIP is Class D: 224.x.x.x to 239.x.x.x</b><br><br>0: This frame is regarded as a normal multicast and search ADDR Table.<br><br>1: This frame is regarded as an IP multicast frame and search IGMP table. |
| 9      | IPM_33        | <b>IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx</b><br><br>0: This frame is regarded as normal multicast and search ADDR table.<br><br>1: This frame is regarded as IP multicast frame and search IGMP table.                 |
| 8      | IPM_01        | <b>IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx</b><br><br>0: This frame is regarded as normal multicast and search ADDR Table.<br><br>1: This frame is regarded as IP multicast frame and search IGMP table.                 |
| 7      | MLD2_JOIN_EN  | <b>MLD v2 HW Join Enable</b><br><br>Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX().<br><br>0: Disable<br><br>1: Enable             |
| 6      | IGMP3_JOIN_EN | <b>IGMP v3 HW Join Enable</b><br><br>Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX().<br><br>0: Disable<br><br>1: Enable            |
| 5      | MLD_JOIN_EN   | <b>MLD Snooping HW Join Enable</b>                                                                                                                                                                                                  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                 |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame.                                                                                                                                                           |
|        |              | 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).                                                                                                                                                 |
| 4      | IGMP_JOIN_EN | <b>IGMP Snooping HW Join Enable</b><br><br>Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically.<br><br>0: Disable<br><br>1: Enable                                                             |
| 3      | MLD_SQRY_EN  | <b>MLD HW Specific Query Enable</b><br><br>0: MLD specific query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the MLD specific query message to refresh the specific multicast member.    |
| 2      | IGMP_SQRY_EN | <b>IGMP HW Specific Query Enable</b><br><br>0: IGMP specific query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member. |
| 1      | MLD_GQRY_EN  | <b>MLD HW General Query Enable</b><br><br>0: MLD general query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the MLD general query message to refresh the multicast member.                |
| 0      | IGMP_GQRY_EN | <b>IGMP HW General Query Enable</b><br><br>0: IGMP general Query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.             |

**1502230C      P3\_PSC      Port security control of P3      000FFF00**

| Bit          | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23   | 22 | 21        | 20     | 19         | 18 | 17           | 16           |
|--------------|------------|----|----|----|----|----|----|----|------|----|-----------|--------|------------|----|--------------|--------------|
| <b>Name</b>  | SA_LRN_CNT |    |    |    |    |    |    |    |      |    |           |        | MAC_SA_LRN |    |              |              |
| <b>Type</b>  | RO         |    |    |    |    |    |    |    |      |    |           |        | RW         |    |              |              |
| <b>Reset</b> | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0    | 0  | 0         | 0      | 1          | 1  | 1            | 1            |
| Bit          | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7    | 6  | 5         | 4      | 3          | 2  | 1            | 0            |
| <b>Name</b>  | MAC_SA_LRN |    |    |    |    |    |    |    | REVO |    | SA_CNT_EN | SA_DIS | SA_LOCK    |    | TX_PORT_LOCK | RX_PORT_LOCK |
| <b>Type</b>  | RW         |    |    |    |    |    |    |    | RW   |    | RW        | RW     | RW         |    | RW           | RW           |
| <b>Reset</b> | 1          | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0    | 0  | 0         | 0      | 0          | 0  | 0            | 0            |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20  | SA_LRN_CNT | <b>Learned Source Address Number</b>                                                                                                                                                                                                                                                                                                                                                                                             |
| 19:8   | MAC_SA_LRN | <b>Rx SA Allowable Learning Number</b><br><br>Sets the maximum number of SA learned addresses when SA_CNT_EN is set.<br><br>12'h0: Disable SA learning<br><br>12'h1:<br><br>12'hFFE: 1 to 4094 address table<br><br>12'hFFF: SA Learning without limitation                                                                                                                                                                      |
| 7:6    | REVO       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 5      | SA_CNT_EN  | <b>SA Counter Enable</b><br><br>Enable the learned source MAC Address counter.<br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                                                                                                                |
| 4      | SA_DIS     | <b>SA Disable</b><br><br>Disable source MAC address learning.<br><br>0: Enable<br><br>1: Disable                                                                                                                                                                                                                                                                                                                                 |
| 3:2    | SA_LOCK    | <b>SA Lock Select</b><br><br>[NOTE] PAE frames should be passed and are not affected by SA Lock.<br><br>2'b00: Receive without SA authorization.<br><br>2'b01: All received frames whose SA look-up is missing or are not port members in the ARL will be dropped.<br><br>2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). |

| Bit(s) | Name         | Description                                                                                                                                                                  |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)                         |
| 1      | TX_PORT_LOCK | <b>Tx Port Lock Enable</b><br><br>[NOTE] PAE Frames should be passed and are not affected by Port Lock.<br><br>0: Transmit authorized.<br><br>1: Disable frame transmission. |
| 0      | RX_PORT_LOCK | <b>Rx Port Lock Enable</b><br><br>[NOTE] PAE frames should be passed and are not affected by Port Lock.<br><br>0: Receive authorized.<br><br>1: Disable frame receiving.     |

**15022310 P3\_PVC Port VLAN control of P3 810000C0**

| Bit   | 31           | 30             | 29             | 28   | 27            | 26     | 25 | 24 | 23        | 22 | 21            | 20              | 19             | 18             | 17      | 16 |
|-------|--------------|----------------|----------------|------|---------------|--------|----|----|-----------|----|---------------|-----------------|----------------|----------------|---------|----|
| Name  | STAG_VPID    |                |                |      |               |        |    |    |           |    |               |                 |                |                |         |    |
| Type  | RW           |                |                |      |               |        |    |    |           |    |               |                 |                |                |         |    |
| Reset | 1            | 0              | 0              | 0    | 0             | 0      | 0  | 1  | 0         | 0  | 0             | 0               | 0              | 0              | 0       | 0  |
| Bit   | 15           | 14             | 13             | 12   | 11            | 10     | 9  | 8  | 7         | 6  | 5             | 4               | 3              | 2              | 1       | 0  |
| Name  | DIS_PV<br>ID | FORCE<br>_PVID | BC_LKY<br>V_EN | REVO | PT_OP<br>TION | EG_TAG |    |    | VLAN_ATTR |    | PORT_<br>STAG | IPM_LK<br>YV_EN | MC_LK<br>YV_EN | UC_LKY<br>V_EN | ACC_FRM |    |
| Type  | RW           | RW             | RW             | RW   | RW            | RW     |    |    | RW        |    | RW            | RW              | RW             | RW             | RW      |    |
| Reset | 0            | 0              | 0              | 0    | 0             | 0      | 0  | 0  | 1         | 1  | 0             | 0               | 0              | 0              | 0       | 0  |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                            |
|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | STAG_VPID  | <b>Stack Tag VPID (VLAN Protocol ID) Value</b><br><br>The received frame will be regarded as a legal stack tag frame if the following conditions are matched:<br><br>Outer VPID == STAG_VPID<br><br>Inner VPID == 16'h8100<br><br>The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID. |
| 15     | DIS_PVID   | <b>PVID Disable</b><br><br>Disable PVID insertion in priority-tagged frames.<br><br>0: Use PVID for priority-tagged frames.<br><br>1: Keep VID=0 for priority-tagged frames.                                                                                                                                                           |
| 14     | FORCE_PVID | <b>Force PVID on VLAN-tagged frames</b><br><br>0: Use VID in VLAN-tagged frame.<br><br>1: Force the replacement of VID with PVID.                                                                                                                                                                                                      |
| 13     | BC_LKYV_EN | <b>Broadcast Leaky VLAN Enable</b><br><br>0: Broadcast frames received by this port will be blocked by VLAN.<br><br>1: Broadcast frames received by this port can pass through VLAN.                                                                                                                                                   |
| 12     | REVO       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                        |
| 11     | PT_OPTION  | <b>Pass-through capability on TX special tag</b><br><br>0: Disable pass-through on TX special tag<br><br>1: Enable pass-through on TX special tag                                                                                                                                                                                      |
| 10:8   | EG_TAG     | <b>Incoming Port Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disabled)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged                                                                                                                                                            |

| Bit(s) | Name        | Description                                                                                                                                       |
|--------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6    | VLAN_ATTR   | 3'b101: Swap                                                                                                                                      |
|        |             | 3'b110: Tagged                                                                                                                                    |
|        |             | 3'b111: Stack                                                                                                                                     |
|        |             | <b>VLAN Port Attribute</b>                                                                                                                        |
|        |             | 2'b00: User port                                                                                                                                  |
|        |             | 2'b01: Stack port                                                                                                                                 |
|        |             | 2'b10: Translation port                                                                                                                           |
| 5      | PORT_STAG   | 2'b11: Transparent port                                                                                                                           |
|        |             | <b>Special Tag Enable</b>                                                                                                                         |
|        |             | Enable a proprietary VLAN tag format to carry additional information to the remote port.                                                          |
| 4      | IPM_LKYV_EN | 0: No special tag format for Tx/Rx                                                                                                                |
|        |             | 1: Enable                                                                                                                                         |
|        |             | <b>IP Multicast Leaky VLAN Enable</b>                                                                                                             |
| 3      | MC_LKYV_EN  | (note*) If MC_LKYV_EN is set, this field will become "don't care" bit. All multicast frames including IP_Multi will be leaky between VLAN groups. |
|        |             | 0: IP_Multi frames received by this port will be blocked by VLAN.                                                                                 |
|        |             | 1: IP_Multi frames received by this port can pass through VLAN.                                                                                   |
| 2      | UC_LKYV_EN  | <b>Multicast Leaky VLAN Enable</b>                                                                                                                |
|        |             | 0: Multicast frames received by this port will be blocked by VLAN.                                                                                |
|        |             | 1: Multicast frames received by this port can pass through VLAN.                                                                                  |
| 1:0    | ACC_FRM     | <b>Unicast Leaky VLAN Enable</b>                                                                                                                  |
|        |             | 0: Unicast frame received by this port will be blocked by VLAN.                                                                                   |
|        |             | 1: Unicast frame received by this port can pass through VLAN.                                                                                     |
|        |             | <b>Acceptable Frame Type</b>                                                                                                                      |
|        |             | 2'b00: Admit All frames                                                                                                                           |
|        |             | 2'b01: Admit Only VLAN-tagged frames                                                                                                              |
|        |             | 2'b10: Admit only untagged or priority-tagged frames.                                                                                             |
|        |             | 2'b11: Reserved                                                                                                                                   |



15022314      P3\_PPBV1      Port-and-Protocol based VLAN I of P3      00010001

| Bit   | 31          | 30 | 29 | 28   | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|------|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  | G1_PORT_PRI |    |    | REV0 | G1_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| Bit   | 15          | 14 | 13 | 12   | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | G0_PORT_PRI |    |    | REV1 | G0_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name        | Description                                                                                                                                |
|--------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29  | G1_PORT_PRI | <b>Group 1 Port Priority (optional)</b><br>The Group 1 Priority for each port according to IEEE 802.1Q definition                          |
| 28     | REV0        | <b>Reserved</b>                                                                                                                            |
| 27:16  | G1_PORT_VID | <b>Group 1 Port VLAN ID (optional)</b><br>The Group 1 VID for each port according to IEEE 802.1Q definition                                |
| 15:13  | G0_PORT_PRI | <b>Group 0 Port Priority (Default Port Priority)</b><br>The Group 0 and default Priority for each port according to IEEE 802.1Q definition |
| 12     | REV1        | <b>Reserved</b>                                                                                                                            |
| 11:0   | G0_PORT_VID | <b>Group 0 Port VLAN ID (Default Port VID)</b><br>The Group 0 and default VID for each port according to IEEE 802.1Q definition            |

15022318      P3\_PPBV2      Port-and-Protocol based VLAN II of P3      00010001

| Bit   | 31          | 30 | 29 | 28   | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|------|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |             |    |    | REV0 | G3_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| Bit   | 15          | 14 | 13 | 12   | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | G2_PORT_PRI |    |    | REV1 | G2_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name        | Description                                                                                                           |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------|
| 28     | REV0        | Reserved                                                                                                              |
| 27:16  | G3_PORT_VID | <b>Group 3 Port VLAN ID (optional)</b><br><br>The Group 3 VID for each port according to IEEE 802.1Q definition       |
| 15:13  | G2_PORT_PRI | <b>Group 2 Port Priority (optional)</b><br><br>The Group 2 Priority for each port according to IEEE 802.1Q definition |
| 12     | REV1        | Reserved                                                                                                              |
| 11:0   | G2_PORT_VID | <b>Group 2 Port VLAN ID (optional)</b><br><br>The Group 2 VID for each port according to IEEE 802.1Q definition       |

1502231C      P3\_BSR      Broadcast storm rate control of P3      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
|        |            | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
| 7:0    | STORM_10M  | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |

15022320      P3\_STAG01      STAG index 0/1 of P3      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REVO |    |    |    |      |    |    |    | VID1 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID1 |    |    |    | VID0 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID1 | VLAN Identifier for STAG index 1 |
| 11:0   | VID0 | VLAN Identifier for STAG index 0 |

15022324      **P3 STAG23**      **STAG index 2/3 of P3**      00000000

| Bit          | 31          | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------|----|----|----|-------------|----|----|----|-------------|----|----|----|----|----|----|----|
| <b>Name</b>  | <b>REVO</b> |    |    |    |             |    |    |    | <b>VID3</b> |    |    |    |    |    |    |    |
| <b>Type</b>  | RO          |    |    |    |             |    |    |    | RW          |    |    |    |    |    |    |    |
| <b>Reset</b> | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15          | 14 | 13 | 12 | 11          | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | <b>VID3</b> |    |    |    | <b>VID2</b> |    |    |    |             |    |    |    |    |    |    |    |
| <b>Type</b>  | RW          |    |    |    | RW          |    |    |    |             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID3 | VLAN Identifier for STAG index 3 |
| 11:0   | VID2 | VLAN Identifier for STAG index 2 |

15022328      P3 STAG45      STAG index 4/5 of P3      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REVO |    |    |    |      |    |    |    | VID5 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID5 |    |    |    | VID4 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID5 | VLAN Identifier for STAG index 5 |
| 11:0   | VID4 | VLAN Identifier for STAG index 4 |

1502232C      P3\_STAG67      STAG index 6/7 of P3      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REVO |    |    |    |      |    |    |    | VID7 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID7 |    |    |    | VID6 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID7 | VLAN Identifier for STAG index 7 |
| 11:0   | VID6 | VLAN Identifier for STAG index 6 |



15022330      **P3\_BSR\_EXT1**      Broadcast storm rate control I of P3      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
| 7:0    | STORM_10M  | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            |                                                         |

15022334      P3\_BSR\_EXT2      Broadcast storm rate control II of P3      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
|        |            | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
| 7:0    | STORM_10M  | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |

15022338      **P3 BSR\_EXT3**      Broadcast storm rate control III of P3      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
| 7:0    | STORM_10M  | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
|        |            | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |

**15022340      P3\_UPW      User priority weight of P3      00234567**

| Bit   | 31   | 30       | 29 | 28 | 27   | 26      | 25 | 24 | 23   | 22       | 21 | 20 | 19   | 18       | 17 | 16 |
|-------|------|----------|----|----|------|---------|----|----|------|----------|----|----|------|----------|----|----|
| Name  |      |          |    |    |      |         |    |    | REV0 | ARL_UPW  |    |    | REV1 | PORT_UPW |    |    |
| Type  |      |          |    |    |      |         |    |    | RW   | RW       |    |    | RW   | RW       |    |    |
| Reset |      |          |    |    |      |         |    |    | 0    | 0        | 1  | 0  | 0    | 0        | 1  | 1  |
| Bit   | 15   | 14       | 13 | 12 | 11   | 10      | 9  | 8  | 7    | 6        | 5  | 4  | 3    | 2        | 1  | 0  |
| Name  | REV2 | DSCP_UPW |    |    | REV3 | TAG_UPW |    |    | REV4 | STAG_UPW |    |    | REV5 | ACL_UPW  |    |    |
| Type  | RW   | RW       |    |    | RW   | RW      |    |    | RW   | RW       |    |    | RW   | RW       |    |    |
| Reset | 0    | 1        | 0  | 0  | 0    | 1       | 0  | 1  | 0    | 1        | 1  | 0  | 0    | 1        | 1  | 1  |

| Bit(s) | Name     | Description                                                             |
|--------|----------|-------------------------------------------------------------------------|
| 23     | REV0     | Reserved                                                                |
| 22:20  | ARL_UPW  | ARL User Priority Weight (MAC/DIP Hit)                                  |
| 19     | REV1     | Reserved                                                                |
| 18:16  | PORT_UPW | Port-Based User Priority Weight Value<br>Weights range from 0x0 to 0x7. |
| 15     | REV2     | Reserved                                                                |
| 14:12  | DSCP_UPW | DSCP Priority Weight (IPv4)                                             |
| 11     | REV3     | Reserved                                                                |
| 10:8   | TAG_UPW  | Priority Tag User Priority Weight                                       |
| 7      | REV4     | Reserved                                                                |
| 6:4    | STAG_UPW | Special Tag User Priority Weight                                        |
| 3      | REV5     | Reserved                                                                |
| 2:0    | ACL_UPW  | ACL User Priority Weight (ACL Hit)                                      |

**15022344      P3\_PEM1      User priority egress mapping I of P3      10080480**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_1 |    |    | QUE_PFCR_1 |    |    | QUE_PFCT_1 |    |    | DSCP_PRI_1 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 0  | 1  | 0          | 0  | 0  | 0          | 0  | 0  | 0          | 0  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_0 |    |    | QUE_PFCR_0 |    |    | QUE_PFCT_0 |    |    | DSCP_PRI_0 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 0  | 0  | 0          | 1  | 0  | 0          | 1  | 0  | 0          | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_1  | User Priority 1 Priority Tag Value                       |
| 27:25  | QUE_PFCR_1 | User Priority 1 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_1 | User Priority 1 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_1 | User Priority 1 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_0  | User Priority 0 Priority Tag Value                       |
| 11:9   | QUE_PFCR_0 | User Priority 0 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_0 | User Priority 0 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_0 | User Priority 0 DSCP Value                               |



**15022348      P3\_PEM2      User priority egress mapping II of P3      36D82250**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_3 |    |    | QUE_PFCR_3 |    |    | QUE_PFCT_3 |    |    | DSCP_PRI_3 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 1  | 1  | 0          | 1  | 1  | 0          | 1  | 1  | 0          | 1  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_2 |    |    | QUE_PFCR_2 |    |    | QUE_PFCT_2 |    |    | DSCP_PRI_2 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 1  | 0  | 0          | 0  | 1  | 0          | 0  | 1  | 0          | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_3  | User Priority 3 Priority Tag Value                       |
| 27:25  | QUE_PFCR_3 | User Priority 3 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_3 | User Priority 3 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_3 | User Priority 3 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_2  | User Priority 2 Priority Tag Value                       |
| 11:9   | QUE_PFCR_2 | User Priority 2 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_2 | User Priority 2 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_2 | User Priority 2 DSCP Value                               |

**1502234C      P3\_PEM3      User priority egress mapping III of P3      5B684920**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_5 |    |    | QUE_PFCR_5 |    |    | QUE_PFCT_5 |    |    | DSCP_PRI_5 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 0  | 1  | 1          | 0  | 1  | 1          | 0  | 1  | 1          | 0  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_4 |    |    | QUE_PFCR_4 |    |    | QUE_PFCT_4 |    |    | DSCP_PRI_4 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 0  | 0  | 1          | 0  | 0  | 1          | 0  | 0  | 1          | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_5  | User Priority 5 Priority Tag Value                       |
| 27:25  | QUE_PFCR_5 | User Priority 5 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_5 | User Priority 5 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_5 | User Priority 5 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_4  | User Priority 4 Priority Tag Value                       |
| 11:9   | QUE_PFCR_4 | User Priority 4 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_4 | User Priority 4 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_4 | User Priority 4 DSCP Value                               |

**15022350      P3\_PEM4      User priority egress mapping IV of P3      7FF86DB0**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_7 |    |    | QUE_PFCR_7 |    |    | QUE_PFCT_7 |    |    | DSCP_PRI_7 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 1  | 1  | 1          | 1  | 1  | 1          | 1  | 1  | 1          | 1  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_6 |    |    | QUE_PFCR_6 |    |    | QUE_PFCT_6 |    |    | DSCP_PRI_6 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 1  | 0  | 1          | 1  | 0  | 1          | 1  | 0  | 1          | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_7  | User Priority 7 Priority Tag Value                       |
| 27:25  | QUE_PFCR_7 | User Priority 7 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_7 | User Priority 7 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_7 | User Priority 7 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_6  | User Priority 6 Priority Tag Value                       |
| 11:9   | QUE_PFCR_6 | User Priority 6 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_6 | User Priority 6 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_6 | User Priority 6 DSCP Value                               |

15022600      P6\_SSC      STP state control of P6      0000FFFF

| Bit   | 31       | 30 | 29       | 28 | 27       | 26 | 25       | 24 | 23       | 22 | 21       | 20 | 19       | 18 | 17       | 16 |
|-------|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|
| Name  | REVO     |    |          |    |          |    |          |    |          |    |          |    |          |    |          |    |
| Type  | RO       |    |          |    |          |    |          |    |          |    |          |    |          |    |          |    |
| Reset | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  | 0        | 0  |
| Bit   | 15       | 14 | 13       | 12 | 11       | 10 | 9        | 8  | 7        | 6  | 5        | 4  | 3        | 2  | 1        | 0  |
| Name  | FID7_PST |    | FID6_PST |    | FID5_PST |    | FID4_PST |    | FID3_PST |    | FID2_PST |    | FID1_PST |    | FID0_PST |    |
| Type  | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    | RW       |    |
| Reset | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  | 1        | 1  |

| Bit(s) | Name     | Description                                                                                                                                                                                                                    |
|--------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | REVO     | <b>Reserved</b>                                                                                                                                                                                                                |
| 15:14  | FID7_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 13:12  | FID6_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 11:10  | FID5_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 9:8    | FID4_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)<br>2'b11: Forwarding (STP) / Forwarding (RSTP) |
| 7:6    | FID3_PST | <b>(Rapid) Spanning Tree Protocol Port State</b><br>2'b00: Disable (STP) / Discard (RSTP)<br>2'b01: Listening (STP) / Discard (RSTP)<br>2'b10: Learning (STP) / Learning (RSTP)                                                |

| Bit(s) | Name     | Description                                      |
|--------|----------|--------------------------------------------------|
| 5:4    | FID2_PST | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |
|        |          | <b>(Rapid) Spanning Tree Protocol Port State</b> |
|        |          | 2'b00: Disable (STP) / Discard (RSTP)            |
|        |          | 2'b01: Listening (STP) / Discard (RSTP)          |
|        |          | 2'b10: Learning (STP) / Learning (RSTP)          |
| 3:2    | FID1_PST | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |
|        |          | <b>(Rapid) Spanning Tree Protocol Port State</b> |
|        |          | 2'b00: Disable (STP) / Discard (RSTP)            |
|        |          | 2'b01: Listening (STP) / Discard (RSTP)          |
|        |          | 2'b10: Learning (STP) / Learning (RSTP)          |
| 1:0    | FID0_PST | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |
|        |          | <b>(Rapid) Spanning Tree Protocol Port State</b> |
|        |          | 2'b00: Disable (STP) / Discard (RSTP)            |
|        |          | 2'b01: Listening (STP) / Discard (RSTP)          |
|        |          | 2'b10: Learning (STP) / Learning (RSTP)          |
|        |          | 2'b11: Forwarding (STP) / Forwarding (RSTP)      |

**15022604      P6\_PCR      Port control of P6      00FF2000**

| Bit   | 31   | 30       | 29     | 28         | 27        | 26       | 25         | 24         | 23          | 22          | 21 | 20 | 19   | 18       | 17        | 16 |
|-------|------|----------|--------|------------|-----------|----------|------------|------------|-------------|-------------|----|----|------|----------|-----------|----|
| Name  | REV0 | MLDv2_EN | EG_TAG |            | REV1      | PORT_PRI |            |            | PORT_MATRIX |             |    |    |      |          |           |    |
| Type  | RW   | RW       | RW     |            | RW        | RW       |            |            | RW          |             |    |    |      |          |           |    |
| Reset | 0    | 0        | 0      | 0          | 0         | 0        | 0          | 0          | 1           | 1           | 1  | 1  | 1    | 1        | 1         | 1  |
| Bit   | 15   | 14       | 13     | 12         | 11        | 10       | 9          | 8          | 7           | 6           | 5  | 4  | 3    | 2        | 1         | 0  |
| Name  | REV2 |          |        | UP2DSCP_EN | UP2TAG_EN | ACL_EN   | PORT_TX_MR | PORT_RX_MR | ACL_MR      | MIS_PORT_FW |    |    | REV3 | VLAN_MIS | PORT_VLAN |    |
| Type  | RW   |          |        | RW         | RW        | RW       | RW         | RW         | RW          | RW          |    |    | RW   | RW       | RW        |    |
| Reset | 0    | 0        | 1      | 0          | 0         | 0        | 0          | 0          | 0           | 0           | 0  | 0  | 0    | 0        | 0         | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                     |
|--------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | REV0        | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 30     | MLDv2_EN    | <b>IPv6 MLDv2 source address multicast forwarding enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                 |
| 29:28  | EG_TAG      | <b>Port-Based Egress VLAN Tag Attribution</b><br><br>2'b00: Untagged<br><br>2'b01: Swap<br><br>2'b10: Tagged<br><br>2'b11: Stack                                                                                                                                                |
| 27     | REV1        | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 26:24  | PORT_PRI    | <b>Port-based User Priority</b><br><br>User priority for the ingress port                                                                                                                                                                                                       |
| 23:16  | PORT_MATRIX | <b>Port Matrix Member</b><br><br>The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member.<br><br>NOTE: The final and effective port member should exclude the received port. |
| 15:13  | REV2        | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 12     | UP2DSCP_EN  | <b>User Priority to DSCP Enable</b><br><br>Replace DSCP according to user priority.<br><br>0: Disable<br><br>1: Enable                                                                                                                                                          |
| 11     | UP2TAG_EN   | <b>User Priority to Tag Enable</b><br><br>Replace 802.Q priority by user priority.                                                                                                                                                                                              |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |             | 0: Disable                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|        |             | 1: Enable                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 10     | ACL_EN      | <b>Port-based ACL Enable</b><br>0: Bypass the ACL Table.<br>1: Lookup the ACL Table and take the corresponding actions.                                                                                                                                                                                                                                                                                                                        |
| 9      | PORT_TX_MIR | <b>Port Tx Mirror Enable</b><br>All frames transmitted from this port are copied to the mirror port.<br>[NOTE] Multi-port support is possible.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                      |
| 8      | PORT_RX_MIR | <b>Port Rx Mirror Enable</b><br>All frames received from this port are copied to the mirror port.<br>[NOTE] Multi-port support is possible.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                         |
| 7      | ACL_MIR     | <b>ACL Mismatch to Mirror Port</b><br>Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule.<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                     |
| 6:4    | MIS_PORT_FW | <b>ACL Mismatch TO_CPU Forward</b><br>Frame port forwarding when ACL table is enabled and the frame is mismatched<br>3'b0xx: System default (disabled)<br>3'b100: System default and CPU port excluded<br>3'b101: System default and CPU port included<br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.)<br>3'b111: Frame dropped |
| 3      | REV3        | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 2      | VLAN_MIS    | <b>VLAN Mismatch to Mirror Port</b><br>1'b0: Frame processed according to PORT_VLAN.<br>1'b1: VLAN mismatched frame copied to MIRROR port.                                                                                                                                                                                                                                                                                                     |

| Bit(s) | Name      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|--------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0    | PORT_VLAN | <b>Port-based VLAN Mechanism Select</b><br><br>2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member.<br><br>2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member.<br><br>2'b10: Check Mode. Forward received frames whose ingress port does not belong to the VLAN member. But, discard frames if VID is missed on the VLAN table.<br><br>2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table. |



15022608      P6\_PIC      Port IGMP control of P6      00008000

| Bit   | 31         | 30 | 29           | 28            | 27   | 26       | 25    | 24    | 23           | 22            | 21          | 20           | 19          | 18           | 17          | 16           |
|-------|------------|----|--------------|---------------|------|----------|-------|-------|--------------|---------------|-------------|--------------|-------------|--------------|-------------|--------------|
| Name  | REVO       |    |              |               |      |          |       |       |              |               |             |              | IGMP_MIR    | IGMP_MIS     |             |              |
| Type  | RO         |    |              |               |      |          |       |       |              |               |             |              | RW          | RW           |             |              |
| Reset | 0          | 0  | 0            | 0             | 0    | 0        | 0     | 0     | 0            | 0             | 0           | 0            | 0           | 0            | 0           | 0            |
| Bit   | 15         | 14 | 13           | 12            | 11   | 10       | 9     | 8     | 7            | 6             | 5           | 4            | 3           | 2            | 1           | 0            |
| Name  | ROBUST_VAR |    | MLD_HW_LEAVE | IGMP_HW_LEAVE | REV1 | IPM22_44 | IPM33 | IPM01 | MLD2_JOIN_EN | IGMP3_JOIN_EN | MLD_JOIN_EN | IGMP_JOIN_EN | MLD_SQRY_EN | IGMP_SQRY_EN | MLD_GQRY_EN | IGMP_GQRY_EN |
| Type  | RW         |    | RW           | RW            | RW   | RW       | RW    | RW    | RW           | RW            | RW          | RW           | RW          | RW           | RW          | RW           |
| Reset | 1          | 0  | 0            | 0             | 0    | 0        | 0     | 0     | 0            | 0             | 0           | 0            | 0           | 0            | 0           | 0            |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20  | REVO       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 19     | IGMP_MIR   | <b>IP Multicast IGMP Table Mismatch to Mirror Port</b><br><br>Copy IP multicast frames with an IGMP table mismatch to the mirror port.<br><br>[NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis.<br><br>0: Disable<br><br>1: Frame copied to Mirror port                                                                                                                                                                                                                                                                                     |
| 18:16  | IGMP_MIS   | <b>IP Multicast "TO_CPU" Forwarding</b><br><br>Select how to forward IP multicast frames when the IGMP table is mismatched.<br><br>[NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis.<br><br>3'b0xx: System default (By MFC.UNM_FFP)<br><br>3'b100: System default and CPU port excluded<br><br>3'b101: System default and CPU port included<br><br>3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.)<br><br>3'b111: Frame dropped |
| 15:14  | ROBUST_VAR | <b>Robustness Variable</b><br><br>Define the number of times an IGMP report message may be lost consecutively.<br><br>0: Unlimited (No Age out)<br><br>1: One time<br><br>2: Twice (default)<br><br>3: Three times                                                                                                                                                                                                                                                                                                                                                                        |

| Bit(s) | Name          | Description                                                                                                                                                                                                                         |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13     | MLD_HW_LEAVE  | <b>MLD HW Leave Enable</b><br><br>Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query.<br><br>0: Disable<br><br>1: Enable      |
| 12     | IGMP_HW_LEAVE | <b>IGMP HW Leave Enable</b><br><br>Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query.<br><br>0: Disable<br><br>1: Enable   |
| 11     | REV1          | <b>Reserved</b>                                                                                                                                                                                                                     |
| 10     | IPM_2244      | <b>IP Multicast frame for DIP is Class D: 224.x.x.x to 239.x.x.x</b><br><br>0: This frame is regarded as a normal multicast and search ADDR Table.<br><br>1: This frame is regarded as an IP multicast frame and search IGMP table. |
| 9      | IPM_33        | <b>IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx</b><br><br>0: This frame is regarded as normal multicast and search ADDR table.<br><br>1: This frame is regarded as IP multicast frame and search IGMP table.                 |
| 8      | IPM_01        | <b>IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx</b><br><br>0: This frame is regarded as normal multicast and search ADDR Table.<br><br>1: This frame is regarded as IP multicast frame and search IGMP table.                 |
| 7      | MLD2_JOIN_EN  | <b>MLD v2 HW Join Enable</b><br><br>Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX().<br><br>0: Disable<br><br>1: Enable             |
| 6      | IGMP3_JOIN_EN | <b>IGMP v3 HW Join Enable</b><br><br>Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX().<br><br>0: Disable<br><br>1: Enable            |
| 5      | MLD_JOIN_EN   | <b>MLD Snooping HW Join Enable</b>                                                                                                                                                                                                  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                 |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame.                                                                                                                                                           |
|        |              | 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).                                                                                                                                                 |
| 4      | IGMP_JOIN_EN | <b>IGMP Snooping HW Join Enable</b><br><br>Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically.<br><br>0: Disable<br><br>1: Enable                                                             |
| 3      | MLD_SQRY_EN  | <b>MLD HW Specific Query Enable</b><br><br>0: MLD specific query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the MLD specific query message to refresh the specific multicast member.    |
| 2      | IGMP_SQRY_EN | <b>IGMP HW Specific Query Enable</b><br><br>0: IGMP specific query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member. |
| 1      | MLD_GQRY_EN  | <b>MLD HW General Query Enable</b><br><br>0: MLD general query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the MLD general query message to refresh the multicast member.                |
| 0      | IGMP_GQRY_EN | <b>IGMP HW General Query Enable</b><br><br>0: IGMP general Query message will not refresh the IP multicast table.<br><br>1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.             |

**1502260C      P6\_PSC      Port security control of P6      000FFF00**

| Bit          | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23   | 22 | 21        | 20     | 19         | 18 | 17           | 16           |
|--------------|------------|----|----|----|----|----|----|----|------|----|-----------|--------|------------|----|--------------|--------------|
| <b>Name</b>  | SA_LRN_CNT |    |    |    |    |    |    |    |      |    |           |        | MAC_SA_LRN |    |              |              |
| <b>Type</b>  | RO         |    |    |    |    |    |    |    |      |    |           |        | RW         |    |              |              |
| <b>Reset</b> | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0    | 0  | 0         | 0      | 1          | 1  | 1            | 1            |
| Bit          | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7    | 6  | 5         | 4      | 3          | 2  | 1            | 0            |
| <b>Name</b>  | MAC_SA_LRN |    |    |    |    |    |    |    | REVO |    | SA_CNT_EN | SA_DIS | SA_LOCK    |    | TX_PORT_LOCK | RX_PORT_LOCK |
| <b>Type</b>  | RW         |    |    |    |    |    |    |    | RW   |    | RW        | RW     | RW         |    | RW           | RW           |
| <b>Reset</b> | 1          | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0    | 0  | 0         | 0      | 0          | 0  | 0            | 0            |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                                     |
|--------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20  | SA_LRN_CNT | <b>Learned Source Address Number</b>                                                                                                                                                                                                                                                                                                                                                                                            |
| 19:8   | MAC_SA_LRN | <b>Rx SA Allowable Learning Number</b><br><br>Sets the maximum number of SA learned addresses when SA_CNT_EN is set.<br><br>12'h0: Disable SA learning<br><br>12'h1:<br><br>12'hFFE: 1 to 4094 address table<br><br>12'hFFF: SA Learning without limitation                                                                                                                                                                     |
| 7:6    | REVO       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 5      | SA_CNT_EN  | <b>SA Counter Enable</b><br><br>Enable the learned source MAC Address counter.<br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                                                                                                               |
| 4      | SA_DIS     | <b>SA Disable</b><br><br>Disable source MAC address learning.<br><br>0: Enable<br><br>1: Disable                                                                                                                                                                                                                                                                                                                                |
| 3:2    | SA_LOCK    | <b>SA Lock Select</b><br><br>[NOTE] PAE frames should be passed and are not affected by SA Lock.<br><br>2'b00: Receive without SA authorization.<br><br>2'b01: All received frame whose SA look-up is missing or are not port members in the ARL will be dropped.<br><br>2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). |

| Bit(s) | Name         | Description                                                                                                                                                                  |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)                         |
| 1      | TX_PORT_LOCK | <b>Tx Port Lock Enable</b><br><br>[NOTE] PAE Frames should be passed and are not affected by Port Lock.<br><br>0: Transmit authorized.<br><br>1: Disable frame transmission. |
| 0      | RX_PORT_LOCK | <b>Rx Port Lock Enable</b><br><br>[NOTE] PAE frames should be passed and are not affected by Port Lock.<br><br>0: Receive authorized.<br><br>1: Disable frame receiving.     |

**15022610 P6\_PVC Port VLAN control of P6 810000C0**

| Bit          | 31           | 30             | 29             | 28   | 27            | 26     | 25 | 24 | 23        | 22 | 21            | 20              | 19             | 18             | 17      | 16 |
|--------------|--------------|----------------|----------------|------|---------------|--------|----|----|-----------|----|---------------|-----------------|----------------|----------------|---------|----|
| <b>Name</b>  | STAG_VPID    |                |                |      |               |        |    |    |           |    |               |                 |                |                |         |    |
| <b>Type</b>  | RW           |                |                |      |               |        |    |    |           |    |               |                 |                |                |         |    |
| <b>Reset</b> | 1            | 0              | 0              | 0    | 0             | 0      | 0  | 1  | 0         | 0  | 0             | 0               | 0              | 0              | 0       | 0  |
| Bit          | 15           | 14             | 13             | 12   | 11            | 10     | 9  | 8  | 7         | 6  | 5             | 4               | 3              | 2              | 1       | 0  |
| <b>Name</b>  | DIS_PV<br>ID | FORCE<br>_PVID | BC_LKY<br>V_EN | REVO | PT_OP<br>TION | EG_TAG |    |    | VLAN_ATTR |    | PORT_<br>STAG | IPM_LK<br>YV_EN | MC_LK<br>YV_EN | UC_LKY<br>V_EN | ACC_FRM |    |
| <b>Type</b>  | RW           | RW             | RW             | RW   | RW            | RW     |    |    | RW        |    | RW            | RW              | RW             | RW             | RW      |    |
| <b>Reset</b> | 0            | 0              | 0              | 0    | 0             | 0      | 0  | 0  | 1         | 1  | 0             | 0               | 0              | 0              | 0       | 0  |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                            |
|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | STAG_VPID  | <b>Stack Tag VPID (VLAN Protocol ID) Value</b><br><br>The received frame will be regarded as a legal stack tag frame if the following conditions are matched:<br><br>Outer VPID == STAG_VPID<br><br>Inner VPID == 16'h8100<br><br>The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID. |
| 15     | DIS_PVID   | <b>PVID Disable</b><br><br>Disable PVID insertion in priority-tagged frames.<br><br>0: Use PVID for priority-tagged frames.<br><br>1: Keep VID=0 for priority-tagged frames.                                                                                                                                                           |
| 14     | FORCE_PVID | <b>Force PVID on VLAN-tagged frames</b><br><br>0: Use VID in VLAN-tagged frame.<br><br>1: Force the replacement of VID with PVID.                                                                                                                                                                                                      |
| 13     | BC_LKYV_EN | <b>Broadcast Leaky VLAN Enable</b><br><br>0: Broadcast frames received by this port will be blocked by VLAN.<br><br>1: Broadcast frames received by this port can pass through VLAN.                                                                                                                                                   |
| 12     | REVO       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                        |
| 11     | PT_OPTION  | <b>Pass-through capability on TX special tag</b><br><br>0: Disable pass-through on TX special tag<br><br>1: Enable pass-through on TX special tag                                                                                                                                                                                      |
| 10:8   | EG_TAG     | <b>Incoming Port Egress VLAN Tag Attribution</b><br><br>3'b000: System default (disabled)<br><br>3'b001: Consistent<br><br>3'b010, 3'b011: Reserved<br><br>3'b100: Untagged                                                                                                                                                            |

| Bit(s) | Name        | Description                                                                                                                                       |
|--------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
|        |             | 3'b101: Swap                                                                                                                                      |
|        |             | 3'b110: Tagged                                                                                                                                    |
|        |             | 3'b111: Stack                                                                                                                                     |
| 7:6    | VLAN_ATTR   | <b>VLAN Port Attribute</b>                                                                                                                        |
|        |             | 2'b00: User port                                                                                                                                  |
|        |             | 2'b01: Stack port                                                                                                                                 |
|        |             | 2'b10: Translation port                                                                                                                           |
|        |             | 2'b11: Transparent port                                                                                                                           |
| 5      | PORT_STAG   | <b>Special Tag Enable</b>                                                                                                                         |
|        |             | Enable a proprietary VLAN tag format to carry additional information to the remote port.                                                          |
|        |             | 0: No special tag format for Tx/Rx                                                                                                                |
|        |             | 1: Enable                                                                                                                                         |
| 4      | IPM_LKYV_EN | <b>IP Multicast Leaky VLAN Enable</b>                                                                                                             |
|        |             | (note*) If MC_LKYV_EN is set, this field will become "don't care" bit. All multicast frames including IP_Multi will be leaky between VLAN groups. |
|        |             | 0: IP_Multi frames received by this port will be blocked by VLAN.                                                                                 |
|        |             | 1: IP_Multi frames received by this port can pass through VLAN.                                                                                   |
| 3      | MC_LKYV_EN  | <b>Multicast Leaky VLAN Enable</b>                                                                                                                |
|        |             | 0: Multicast frames received by this port will be blocked by VLAN.                                                                                |
|        |             | 1: Multicast frames received by this port can pass through VLAN.                                                                                  |
| 2      | UC_LKYV_EN  | <b>Unicast Leaky VLAN Enable</b>                                                                                                                  |
|        |             | 0: Unicast frame received by this port will be blocked by VLAN.                                                                                   |
|        |             | 1: Unicast frame received by this port can pass through VLAN.                                                                                     |
| 1:0    | ACC_FRM     | <b>Acceptable Frame Type</b>                                                                                                                      |
|        |             | 2'b00: Admit All frames                                                                                                                           |
|        |             | 2'b01: Admit Only VLAN-tagged frames                                                                                                              |
|        |             | 2'b10: Admit only untagged or priority-tagged frames.                                                                                             |
|        |             | 2'b11: Reserved                                                                                                                                   |

15022614      P6\_PPBV1      Port-and-Protocol based VLAN I of P6      00010001

| Bit   | 31          | 30 | 29 | 28   | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|------|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  | G1_PORT_PRI |    |    | REV0 | G1_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| Bit   | 15          | 14 | 13 | 12   | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | G0_PORT_PRI |    |    | REV1 | G0_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name        | Description                                                                                                                                    |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29  | G1_PORT_PRI | <b>Group 1 Port Priority (optional)</b><br><br>The Group 1 Priority for each port according to IEEE 802.1Q definition                          |
| 28     | REV0        | <b>Reserved</b>                                                                                                                                |
| 27:16  | G1_PORT_VID | <b>Group 1 Port VLAN ID (optional)</b><br><br>The Group 1 VID for each port according to IEEE 802.1Q definition                                |
| 15:13  | G0_PORT_PRI | <b>Group 0 Port Priority (Default Port Priority)</b><br><br>The Group 0 and default Priority for each port according to IEEE 802.1Q definition |
| 12     | REV1        | <b>Reserved</b>                                                                                                                                |
| 11:0   | G0_PORT_VID | <b>Group 0 Port VLAN ID (Default Port VID)</b><br><br>The Group 0 and default VID for each port according to IEEE 802.1Q definition            |



15022618      P6\_PPBV2      Port-and-Protocol based VLAN II of P6      00010001

| Bit   | 31          | 30 | 29 | 28   | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|------|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |             |    |    | REV0 | G3_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| Bit   | 15          | 14 | 13 | 12   | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | G2_PORT_PRI |    |    | REV1 | G2_PORT_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    | RW   | RW          |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name        | Description                                                                                                           |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------|
| 28     | REV0        | Reserved                                                                                                              |
| 27:16  | G3_PORT_VID | <b>Group 3 Port VLAN ID (optional)</b><br><br>The Group 3 VID for each port according to IEEE 802.1Q definition       |
| 15:13  | G2_PORT_PRI | <b>Group 2 Port Priority (optional)</b><br><br>The Group 2 Priority for each port according to IEEE 802.1Q definition |
| 12     | REV1        | Reserved                                                                                                              |
| 11:0   | G2_PORT_VID | <b>Group 2 Port VLAN ID (optional)</b><br><br>The Group 2 VID for each port according to IEEE 802.1Q definition       |

1502261C      P6\_BSR      Broadcast storm rate control of P6      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
| 7:0    | STORM_10M  | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
|        |            | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |

15022620      P6\_STAG01      STAG index 0/1 of P6      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REVO |    |    |    |      |    |    |    | VID1 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID1 |    |    |    | VID0 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID1 | VLAN Identifier for STAG index 1 |
| 11:0   | VID0 | VLAN Identifier for STAG index 0 |

15022624      P6\_STAG23      STAG index 2/3 of P6      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REVO |    |    |    |      |    |    |    | VID3 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID3 |    |    |    | VID2 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID3 | VLAN Identifier for STAG index 3 |
| 11:0   | VID2 | VLAN Identifier for STAG index 2 |

15022628      P6\_STAG45      STAG index 4/5 of P6      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REV0 |    |    |    |      |    |    |    | VID5 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID5 |    |    |    | VID4 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REV0 | Reserved                         |
| 23:12  | VID5 | VLAN Identifier for STAG index 5 |
| 11:0   | VID4 | VLAN Identifier for STAG index 4 |

1502262C      P6\_STAG67      STAG index 6/7 of P6      00000000

| Bit   | 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|------|----|----|----|------|----|----|----|----|----|----|----|
| Name  | REVO |    |    |    |      |    |    |    | VID7 |    |    |    |    |    |    |    |
| Type  | RO   |    |    |    |      |    |    |    | RW   |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  | 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VID7 |    |    |    | VID6 |    |    |    |      |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    | RW   |    |    |    |      |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                      |
|--------|------|----------------------------------|
| 31:24  | REVO | Reserved                         |
| 23:12  | VID7 | VLAN Identifier for STAG index 7 |
| 11:0   | VID6 | VLAN Identifier for STAG index 6 |

15022630      **P6\_BSR\_EXT1**      Broadcast storm rate control I of P6      00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |



| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
| 7:0    | STORM_10M  | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            |                                                         |

15022634 P6\_BSR\_EXT2 Broadcast storm rate control II of P6 00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
| 7:0    | STORM_10M  | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
|        |            | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |

15022638 P6\_BSR\_EXT3 Broadcast storm rate control III of P6 00000000

| Bit   | 31         | 30          | 29          | 28          | 27        | 26        | 25        | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|-------------|-------------|-------------|-----------|-----------|-----------|----|-----------|----|----|----|----|----|----|----|
| Name  | STRM_MODE  | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT |    | STORM_1G  |    |    |    |    |    |    |    |
| Type  | RW         | RW          | RW          | RW          | RW        | RW        | RW        |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14          | 13          | 12          | 11        | 10        | 9         | 8  | 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_100M |             |             |             |           |           |           |    | STORM_10M |    |    |    |    |    |    |    |
| Type  | RW         |             |             |             |           |           |           |    | RW        |    |    |    |    |    |    |    |
| Reset | 0          | 0           | 0           | 0           | 0         | 0         | 0         | 0  | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                          |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | STRM_MODE   | <b>Broadcast Storm Suppression</b><br>0: Packet-based (1 second period)<br>1: Rate-based                                                                             |
| 30     | STRM_BC_INC | <b>Broadcast Storm Included</b><br>0: Exclude BC frame<br>1: Include BC frame                                                                                        |
| 29     | STRM_MC_INC | <b>Unknown Multicast Storm Included</b><br>0: Exclude MC frame<br>1: Include MC frame                                                                                |
| 28     | STRM_UC_INC | <b>Unknown Unicast Storm Included</b><br>0: Exclude UC frame<br>1: Include UC frame                                                                                  |
| 27     | STRM_DROP   | <b>Broadcast Storm Suppression enabled</b><br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected                                          |
| 26     | STRM_PERD   | <b>Broadcast Storm Detection Signal Period</b><br>0: One second<br>1: 125us                                                                                          |
| 25:24  | STRM_UNIT   | <b>Broadcast Storm Suppression</b><br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16  | STORM_1G    | <b>1000 Mbps Broadcast Storm Rate Limit Control</b>                                                                                                                  |

| Bit(s) | Name       | Description                                             |
|--------|------------|---------------------------------------------------------|
| 15:8   | STORM_100M | The broadcast storm rate limit for 1000 Mbps link speed |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>100 Mbps Broadcast Storm Rate Limit Control</b>      |
|        |            | The broadcast storm rate limit for 100 Mbps link speed  |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
| 7:0    | STORM_10M  | 8'h1: (1* STORM_UNIT) packets or bps                    |
|        |            | <b>10 Mbps Broadcast Storm Rate Limit Control</b>       |
|        |            | The broadcast storm rate limit for 10 Mbps link speed   |
|        |            | 8'h0: (0* STORM_UNIT) packets or bps                    |
|        |            | 8'h1: (1* STORM_UNIT) packets or bps                    |

**15022640**      **P6\_UPW**      **User priority weight of P6**      **00234567**

| Bit   | 31   | 30       | 29 | 28 | 27   | 26      | 25 | 24 | 23   | 22       | 21 | 20 | 19   | 18       | 17 | 16 |
|-------|------|----------|----|----|------|---------|----|----|------|----------|----|----|------|----------|----|----|
| Name  |      |          |    |    |      |         |    |    | REV0 | ARL_UPW  |    |    | REV1 | PORT_UPW |    |    |
| Type  |      |          |    |    |      |         |    |    | RW   | RW       |    |    | RW   | RW       |    |    |
| Reset |      |          |    |    |      |         |    |    | 0    | 0        | 1  | 0  | 0    | 0        | 1  | 1  |
| Bit   | 15   | 14       | 13 | 12 | 11   | 10      | 9  | 8  | 7    | 6        | 5  | 4  | 3    | 2        | 1  | 0  |
| Name  | REV2 | DSCP_UPW |    |    | REV3 | TAG_UPW |    |    | REV4 | STAG_UPW |    |    | REV5 | ACL_UPW  |    |    |
| Type  | RW   | RW       |    |    | RW   | RW      |    |    | RW   | RW       |    |    | RW   | RW       |    |    |
| Reset | 0    | 1        | 0  | 0  | 0    | 1       | 0  | 1  | 0    | 1        | 1  | 0  | 0    | 1        | 1  | 1  |

| Bit(s) | Name     | Description                                                             |
|--------|----------|-------------------------------------------------------------------------|
| 23     | REV0     | Reserved                                                                |
| 22:20  | ARL_UPW  | ARL User Priority Weight (MAC/DIP Hit)                                  |
| 19     | REV1     | Reserved                                                                |
| 18:16  | PORT_UPW | Port-Based User Priority Weight Value<br>Weights range from 0x0 to 0x7. |
| 15     | REV2     | Reserved                                                                |
| 14:12  | DSCP_UPW | DSCP Priority Weight (IPv4)                                             |
| 11     | REV3     | Reserved                                                                |
| 10:8   | TAG_UPW  | Priority Tag User Priority Weight                                       |
| 7      | REV4     | Reserved                                                                |
| 6:4    | STAG_UPW | Special Tag User Priority Weight                                        |
| 3      | REV5     | Reserved                                                                |
| 2:0    | ACL_UPW  | ACL User Priority Weight (ACL Hit)                                      |

**15022644**      **P6\_PEM1**      **User priority egress mapping I of P6**      **10080480**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_1 |    |    | QUE_PFCR_1 |    |    | QUE_PFCT_1 |    |    | DSCP_PRI_1 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 0  | 1  | 0          | 0  | 0  | 0          | 0  | 0  | 0          | 0  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_0 |    |    | QUE_PFCR_0 |    |    | QUE_PFCT_0 |    |    | DSCP_PRI_0 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 0  | 0  | 0          | 1  | 0  | 0          | 1  | 0  | 0          | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_1  | User Priority 1 Priority Tag Value                       |
| 27:25  | QUE_PFCR_1 | User Priority 1 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_1 | User Priority 1 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_1 | User Priority 1 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_0  | User Priority 0 Priority Tag Value                       |
| 11:9   | QUE_PFCR_0 | User Priority 0 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_0 | User Priority 0 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_0 | User Priority 0 DSCP Value                               |

**15022648      P6\_PEM2      User priority egress mapping II of P6      36D82250**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_3 |    |    | QUE_PFCR_3 |    |    | QUE_PFCT_3 |    |    | DSCP_PRI_3 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 1  | 1  | 0          | 1  | 1  | 0          | 1  | 1  | 0          | 1  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_2 |    |    | QUE_PFCR_2 |    |    | QUE_PFCT_2 |    |    | DSCP_PRI_2 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 0         | 1  | 0  | 0          | 0  | 1  | 0          | 0  | 1  | 0          | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_3  | User Priority 3 Priority Tag Value                       |
| 27:25  | QUE_PFCR_3 | User Priority 3 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_3 | User Priority 3 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_3 | User Priority 3 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_2  | User Priority 2 Priority Tag Value                       |
| 11:9   | QUE_PFCR_2 | User Priority 2 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_2 | User Priority 2 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_2 | User Priority 2 DSCP Value                               |



**1502264C      P6\_PEM3      User priority egress mapping III of P6      5B684920**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_5 |    |    | QUE_PFCR_5 |    |    | QUE_PFCT_5 |    |    | DSCP_PRI_5 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 0  | 1  | 1          | 0  | 1  | 1          | 0  | 1  | 1          | 0  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_4 |    |    | QUE_PFCR_4 |    |    | QUE_PFCT_4 |    |    | DSCP_PRI_4 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 0  | 0  | 1          | 0  | 0  | 1          | 0  | 0  | 1          | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_5  | User Priority 5 Priority Tag Value                       |
| 27:25  | QUE_PFCR_5 | User Priority 5 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_5 | User Priority 5 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_5 | User Priority 5 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_4  | User Priority 4 Priority Tag Value                       |
| 11:9   | QUE_PFCR_4 | User Priority 4 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_4 | User Priority 4 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_4 | User Priority 4 DSCP Value                               |

**15022650      P6\_PEM4      User priority egress mapping IV of P6      7FF86DB0**

| Bit          | 31   | 30        | 29 | 28 | 27         | 26 | 25 | 24         | 23 | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
|--------------|------|-----------|----|----|------------|----|----|------------|----|----|------------|----|----|----|----|----|
| <b>Name</b>  | REV0 | TAG_PRI_7 |    |    | QUE_PFCR_7 |    |    | QUE_PFCT_7 |    |    | DSCP_PRI_7 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 1  | 1  | 1          | 1  | 1  | 1          | 1  | 1  | 1          | 1  | 1  | 0  | 0  | 0  |
| Bit          | 15   | 14        | 13 | 12 | 11         | 10 | 9  | 8          | 7  | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | REV1 | TAG_PRI_6 |    |    | QUE_PFCR_6 |    |    | QUE_PFCT_6 |    |    | DSCP_PRI_6 |    |    |    |    |    |
| <b>Type</b>  | RW   | RW        |    |    | RW         |    |    | RW         |    |    | RW         |    |    |    |    |    |
| <b>Reset</b> | 0    | 1         | 1  | 0  | 1          | 1  | 0  | 1          | 1  | 0  | 1          | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                              |
|--------|------------|----------------------------------------------------------|
| 31     | REV0       | Reserved                                                 |
| 30:28  | TAG_PRI_7  | User Priority 7 Priority Tag Value                       |
| 27:25  | QUE_PFCR_7 | User Priority 7 Egress Queue Selection or PFC RX Mapping |
| 24:22  | QUE_PFCT_7 | User Priority 7 PFC TX Mapping                           |
| 21:16  | DSCP_PRI_7 | User Priority 7 DSCP Value                               |
| 15     | REV1       | Reserved                                                 |
| 14:12  | TAG_PRI_6  | User Priority 6 Priority Tag Value                       |
| 11:9   | QUE_PFCR_6 | User Priority 6 Egress Queue Selection or PFC RX Mapping |
| 8:6    | QUE_PFCT_6 | User Priority 6 PFC TX Mapping                           |
| 5:0    | DSCP_PRI_6 | User Priority 6 DSCP Value                               |

15022654      P6\_BSR\_EXT4      Broadcast storm rate control IV of P6      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | STORM_2P5G_EXT3 |    |    |    |    |    |    |    | STORM_2P5G_EXT2 |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    | RW              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | STORM_2P5G_EXT1 |    |    |    |    |    |    |    | STORM_2P5G      |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    | RW              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                |
|--------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | STORM_2P5G_EXT3 | <b>2500 Mbps Broadcast Storm Rate Limit Control</b><br>The broadcast storm rate limit for 2500 Mbps link speed<br>Limitation: Max. rate limit is 1000 Mbps<br>8'h0: (0* STORM_UNIT) packets or bps<br>8'h1: (1* STORM_UNIT) packets or bps |
| 23:16  | STORM_2P5G_EXT2 | <b>2500 Mbps Broadcast Storm Rate Limit Control</b><br>The broadcast storm rate limit for 2500 Mbps link speed<br>Limitation: Max. rate limit is 1000 Mbps<br>8'h0: (0* STORM_UNIT) packets or bps<br>8'h1: (1* STORM_UNIT) packets or bps |
| 15:8   | STORM_2P5G_EXT1 | <b>2500 Mbps Broadcast Storm Rate Limit Control</b><br>The broadcast storm rate limit for 2500 Mbps link speed<br>Limitation: Max. rate limit is 1000 Mbps<br>8'h0: (0* STORM_UNIT) packets or bps<br>8'h1: (1* STORM_UNIT) packets or bps |
| 7:0    | STORM_2P5G      | <b>2500 Mbps Broadcast Storm Rate Limit Control</b><br>The broadcast storm rate limit for 2500 Mbps link speed<br>Limitation: Max. rate limit is 1000 Mbps<br>8'h0: (0* STORM_UNIT) packets or bps<br>8'h1: (1* STORM_UNIT) packets or bps |

15022658      **P6\_BSR\_EXT5**      Broadcast storm rate control V of P6      00000000

| Bit          | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19               | 18               | 17               | 16          |
|--------------|------|----|----|----|----|----|----|----|----|----|----|----|------------------|------------------|------------------|-------------|
| <b>Name</b>  | REVO |    |    |    |    |    |    |    |    |    |    |    |                  |                  |                  |             |
| <b>Type</b>  | RW   |    |    |    |    |    |    |    |    |    |    |    |                  |                  |                  |             |
| <b>Reset</b> | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                | 0                | 0                | 0           |
| Bit          | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3                | 2                | 1                | 0           |
| <b>Name</b>  | REVO |    |    |    |    |    |    |    |    |    |    |    | STRM_UNIT_1_EXT3 | STRM_UNIT_1_EXT2 | STRM_UNIT_1_EXT1 | STRM_UNIT_1 |
| <b>Type</b>  | RW   |    |    |    |    |    |    |    |    |    |    |    | RW               | RW               | RW               | RW          |
| <b>Reset</b> | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                | 0                | 0                | 0           |

| Bit(s) | Name             | Description                                                         |
|--------|------------------|---------------------------------------------------------------------|
| 31:4   | REVO             | <b>Reserved</b>                                                     |
| 3      | STRM_UNIT_1_EXT3 | <b>Broadcast Storm Suppression</b><br>1'b1: 16 K packets or 16 Mbps |
| 2      | STRM_UNIT_1_EXT2 | <b>Broadcast Storm Suppression</b><br>1'b1: 16 K packets or 16 Mbps |
| 1      | STRM_UNIT_1_EXT1 | <b>Broadcast Storm Suppression</b><br>1'b1: 16 K packets or 16 Mbps |
| 0      | STRM_UNIT_1      | <b>Broadcast Storm Suppression</b><br>1'b1: 16 K packets or 16 Mbps |

**15023000 PMCR\_P0 Port 0 MAC control register 00056330**

| Bit   | 31                | 30                | 29                | 28                  | 27                  | 26                  | 25                  | 24           | 23             | 22             | 21             | 20             | 19           | 18 | 17           | 16           |
|-------|-------------------|-------------------|-------------------|---------------------|---------------------|---------------------|---------------------|--------------|----------------|----------------|----------------|----------------|--------------|----|--------------|--------------|
| Name  | FORCE_MODE_LNK_P0 | FORCE_MODE_SPD_P0 | FORCE_MODE_DPX_P0 | FORCE_MODE_RX_FC_P0 | FORCE_MODE_TX_FC_P0 | FORCE_MODE_EEE10_P0 | FORCE_MODE_EEE1G_P0 |              |                |                |                |                | IPG_CFG_P0   |    | EXT_PHY_P0   | MAC_MODE_P0  |
| Type  | RW                | RW                | RW                | RW                  | RW                  | RW                  | RW                  |              |                |                |                |                | RW           |    | RW           | RW           |
| Reset | 0                 | 0                 | 0                 | 0                   | 0                   | 0                   | 0                   |              |                |                |                |                | 0            | 1  | 0            | 1            |
| Bit   | 15                | 14                | 13                | 12                  | 11                  | 10                  | 9                   | 8            | 7              | 6              | 5              | 4              | 3            | 2  | 1            | 0            |
| Name  |                   | MAC_TX_EN_P0      | MAC_RX_EN_P0      |                     | MAC_PRE_P0          |                     | BKOFF_EN_P0         | BACKPR_EN_P0 | FORCE_EEE1G_P0 | FORCE_EEE10_P0 | FORCE_RX_FC_P0 | FORCE_TX_FC_P0 | FORCE_SPD_P0 |    | FORCE_DPX_P0 | FORCE_LNK_P0 |
| Type  |                   | RW                | RW                |                     | RW                  |                     | RW                  | RW           | RW             | RW             | RW             | RW             | RW           |    | RW           | RW           |
| Reset |                   | 1                 | 1                 |                     | 0                   |                     | 1                   | 1            | 0              | 0              | 1              | 1              | 0            | 0  | 0            | 0            |

| Bit(s) | Name                 | Description                                                                                                                                                                                                         |
|--------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | FORCE_MODE_LNK_P0    | <b>PORT 0 link status force Mode.</b><br><br>0: Force mode is off. (MAC link status is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC link status is determined by force_link_P0 register) |
| 30     | FORCE_MODE_SPD_P0    | <b>PORT 0 speed force Mode.</b><br><br>0: Force mode is off. (MAC speed is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC speed is determined by force_spd_P0 register)                    |
| 29     | FORCE_MODE_DPX_P0    | <b>PORT 0 duplex force Mode.</b><br><br>0: Force mode is off. (MAC duplex mode is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC duplex mode is determined by force_dpx_P0 register)       |
| 28     | FORCE_MODE_RX_FC_P0  | <b>PORT 0 RX FC force Mode.</b><br><br>0: Force mode is off. (MAC RX FC ability is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC RX FC ability is determined by force_rx_fc_P0 register)  |
| 27     | FORCE_MODE_TX_FC_P0  | <b>PORT 0 TX FC force Mode.</b><br><br>0: Force mode is off. (MAC TX FC ability is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC TX FC ability is determined by force_tx_fc_P0 register)  |
| 26     | FORCE_MODE_EEE100_P0 | <b>PORT 0 100M EEE force Mode.</b><br><br>0: Force mode is off. (MAC 100M EEE ability is determined by PHY auto-polling module)                                                                                     |

| Bit(s) | Name                | Description                                                                                                                                                                                                                                                       |
|--------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25     | FORCE_MODE_EEE1G_P0 | <p>1: Force mode is on. (MAC 100M EEE ability is determined by force_eee100_P0 register)</p> <p><b>PORT 0 1G EEE force Mode.</b></p> <p>0: Force mode is off. (MAC 1G EEE ability is determined by PHY auto-polling module)</p>                                   |
| 19:18  | IPG_CFG_P0          | <p>1: Force mode is on. (MAC 1G EEE ability is determined by force_eee1g_P0 register)</p> <p><b>PORT 0 Inter-Frame+ Gap Shrink</b></p> <p>00: Normal 96-bit IFG</p> <p>01: Transmit 96-bit IFG with short IFG in random behavior</p> <p>10: Shrink 64-bit IFG</p> |
| 17     | EXT_PHY_P0          | <p><b>PORT 0 External PHY. Port 0 connects with external PHY.</b></p> <p>0: PORT 0 DOES NOT connect with external PHY</p> <p>1: PORT 0 connects with external PHY</p>                                                                                             |
| 16     | MAC_MODE_P0         | <p><b>PORT 0 MAC Mode. PORT 0 operates in MAC mode</b></p> <p>0: PORT 0 operates in PHY mode.</p> <p>1: PORT 0 operates in MAC mode.</p>                                                                                                                          |
| 14     | MAC_TX_EN_P0        | <p><b>Port 0 TX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)</b></p> <p>0: TX MAC function is disabled</p> <p>1: TX MAC function is enabled</p>                                         |
| 13     | MAC_RX_EN_P0        | <p><b>PORT 0 RX MAC Enable. (Note: This bit only has impact on MAC function, it has no impact on the link status or Queue manager.)</b></p> <p>0: RX MAC function is disabled</p> <p>1: RX MAC function is enabled</p>                                            |
| 11     | MAC_PRE_P0          | <p><b>TX short preamble mode</b></p> <p>0: TX short preamble length is disabled</p> <p>1: TX short preamble is enabled.</p>                                                                                                                                       |
| 9      | BKOFF_EN_P0         | <p><b>PORT 0 Backoff Enable</b></p> <p>0: Disabled</p> <p>1: Let the MAC of PORT 0 follow the back-off mechanism when collision happens.</p>                                                                                                                      |
| 8      | BACKPR_EN_P0        | <p><b>PORT 0 Backpressure Enable</b></p> <p>0: Disabled</p>                                                                                                                                                                                                       |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7      | FORCE_EEE1G_P0  | <p>1: Enable back pressure mechanism when operating in half-duplex mode with low internal free memory page count.</p> <p><b>PORT 0 Force LPI Mode For 1000Mbps. When (force_mode_P0 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 0.</b></p> <p>0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps.</p> <p>1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps.</p> |
| 6      | FORCE_EEE100_P0 | <p><b>PORT 0 Force LPI Mode For 100Mbps. When (force_mode_P0 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 0.</b></p> <p>0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps.</p> <p>1: Have the ability of entering EEE Low Power Idle mode for 100Mbps.</p>                                                                                                                          |
| 5      | FORCE_RX_FC_P0  | <p><b>PORT 0 Force RX FC. When (force_mode_P0 = 1), this bit is used to control the RX FC ability of PORT 0.</b></p> <p>0: Disabled</p> <p>1: Let the MAC of PORT 0 accept a pause frame when operating in full-duplex mode.</p>                                                                                                                                                                                                     |
| 4      | FORCE_TX_FC_P0  | <p><b>PORT 0 Force TX FC. When (force_mode_P0 = 1), this bit is used to control the TX FC ability of PORT 0.</b></p> <p>0: Disabled</p> <p>1: Let the MAC of PORT 0 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.</p>                                                                                                                                                          |
| 3:2    | FORCE_SPD_P0    | <p><b>PORT 0 Force Speed [1:0]. When (force_mode_P0 = 1), these bits are used to control MAC speed of PORT 0.</b></p> <p>00: 10Mbps</p> <p>01: 100Mbps</p> <p>10: 1000Mbps</p> <p>11: Reserved</p>                                                                                                                                                                                                                                   |
| 1      | FORCE_DPX_P0    | <p><b>PORT 0 Force duplex. When (force_mode_P0 = 1), this bit is used to control MAC duplex of PORT 0.</b></p> <p>0: Half Duplex</p> <p>1: Full Duplex</p>                                                                                                                                                                                                                                                                           |
| 0      | FORCE_LNK_P0    | <p><b>PORT 0 Force MAC Link Up. When (force_mode_P0 = 1), this bit is used to control link status of PORT 0.</b></p> <p>0: Link Down</p> <p>1: Link Up</p>                                                                                                                                                                                                                                                                           |

| 15023004 | PMEEECR_P0          |    |    |    |    |    |    |    | Port 0 MAC EEE control register |    |    |    |    |    |    |                | 111E01E0 |  |
|----------|---------------------|----|----|----|----|----|----|----|---------------------------------|----|----|----|----|----|----|----------------|----------|--|
| Bit      | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16             |          |  |
| Name     | WAKEUP_TIME_1000_P0 |    |    |    |    |    |    |    | WAKEUP_TIME_100_P0              |    |    |    |    |    |    |                |          |  |
| Type     | RW                  |    |    |    |    |    |    |    | RW                              |    |    |    |    |    |    |                |          |  |
| Reset    | 0                   | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0                               | 0  | 0  | 1  | 1  | 1  | 1  | 0              |          |  |
| Bit      | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0              |          |  |
| Name     | LPI_THRESH_P0       |    |    |    |    |    |    |    |                                 |    |    |    |    |    |    | LPI_MODE_EN_P0 |          |  |
| Type     | RW                  |    |    |    |    |    |    |    |                                 |    |    |    |    |    |    | RW             |          |  |
| Reset    | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1                               | 1  | 1  | 0  |    |    |    | 0              |          |  |

| Bit(s) | Name                | Description                                                                                                                                                                                                                                                                                                                                                                                      |
|--------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | WAKEUP_TIME_1000_P0 | <b>PORT 0 Wake Up Time for 1000Mbps LPI Mode.</b><br><br>The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup.<br><br>Time unit: 1 microsecond                                                                                                                                                                                     |
| 23:16  | WAKEUP_TIME_100_P0  | <b>PORT 0 Wake Up Time for 100Mbps LPI Mode.</b><br><br>The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup.<br><br>Time unit: 1 microsecond                                                                                                                                                                                      |
| 15:4   | LPI_THRESH_P0       | <b>PORT 0 LPI Threshold.</b><br><br>When there is no packet to be transmitted, and the idle time is greater than P0_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.                                                                                                                                                      |
| 0      | LPI_MODE_EN_P0      | <b>PORT 0 Enter LPI Mode.</b><br><br>When there is no packet to be transmitted, and the idle time is greater than P0_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.<br><br>0: LPI mode depends on the P0_LPI_THRESHOLD.<br><br>1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner. |



| 15023008 | PMSR_P0 |    |    | Port 0 MAC status register |    |    |    |    |              |               |              |              |                |    |                | 00000000       |  |
|----------|---------|----|----|----------------------------|----|----|----|----|--------------|---------------|--------------|--------------|----------------|----|----------------|----------------|--|
| Bit      | 31      | 30 | 29 | 28                         | 27 | 26 | 25 | 24 | 23           | 22            | 21           | 20           | 19             | 18 | 17             | 16             |  |
| Name     |         |    |    |                            |    |    |    |    |              |               |              |              |                |    |                |                |  |
| Type     |         |    |    |                            |    |    |    |    |              |               |              |              |                |    |                |                |  |
| Reset    |         |    |    |                            |    |    |    |    |              |               |              |              |                |    |                |                |  |
| Bit      | 15      | 14 | 13 | 12                         | 11 | 10 | 9  | 8  | 7            | 6             | 5            | 4            | 3              | 2  | 1              | 0              |  |
| Name     |         |    |    |                            |    |    |    |    | EEE1G_STS_P0 | EEE100_STS_P0 | RX_FC_STS_P0 | TX_FC_STS_P0 | MAC_SPD_STS_P0 |    | MAC_DPX_STS_P0 | MAC_LNK_STS_P0 |  |
| Type     |         |    |    |                            |    |    |    |    | RO           | RO            | RO           | RO           | RO             |    | RO             | RO             |  |
| Reset    |         |    |    |                            |    |    |    |    | 0            | 0             | 0            | 0            | 0              | 0  | 0              | 0              |  |

| Bit(s) | Name           | Description                                                                                                                                                                                                        |
|--------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7      | EEE1G_STS_P0   | <b>PORT 0 LPI Mode Status For 1000Mbps</b><br><br>0: Not capable of entering EEE Low Power Idle mode for 1000Mbps.<br><br>1: Capable of entering EEE Low Power Idle mode for 1000Mbps.                             |
| 6      | EEE100_STS_P0  | <b>PORT 0 LPI Status Mode For 100Mbps</b><br><br>0: Not capable of entering EEE Low Power Idle mode for 100Mbps.<br><br>1: Capable of entering EEE Low Power Idle mode for 100Mbps.                                |
| 5      | RX_FC_STS_P0   | <b>PORT 0 RX XFC Status. Port 0 Rx flow control status.</b><br><br>0: Disabled<br><br>1: Let the MAC of PORT 0 accept a pause frame when operating in full-duplex mode.                                            |
| 4      | TX_FC_STS_P0   | <b>PORT 0 TX XFC Status. PORT 0 TX flow control status.</b><br><br>0: Disabled<br><br>1: Let the MAC of PORT 0 transmit a pause frame when operating in full-duplex mode with low internal free memory page count. |
| 3:2    | MAC_SPD_STS_P0 | <b>PORT 0 Speed [1:0] Status. Current speed of PORT 0 after PHY links up.</b><br><br>00: 10 Mbps<br><br>01: 100 Mbps<br><br>10: 1000 Mbps<br><br>11: Reserved                                                      |
| 1      | MAC_DPX_STS_P0 | <b>PORT 0 duplex Status. Current duplex mode of PORT 0 after PHY links up.</b><br><br>0: Half Duplex<br><br>1: Full Duplex                                                                                         |
| 0      | MAC_LNK_STS_P0 | <b>Port 6 Link Up Status. Link up status of PORT 0.</b><br><br>0: Link Down                                                                                                                                        |

| Bit(s) | Name | Description |
|--------|------|-------------|
|        |      | 1: Link Up  |

**15023010 PINT\_EN\_P0 Port 0 interrupt enable register 00000000**

| Bit   | 31                 | 30                    | 29                    | 28                  | 27                   | 26                   | 25                  | 24                 | 23 | 22 | 21 | 20 | 19                  | 18                 | 17                  | 16                   |
|-------|--------------------|-----------------------|-----------------------|---------------------|----------------------|----------------------|---------------------|--------------------|----|----|----|----|---------------------|--------------------|---------------------|----------------------|
| Name  |                    |                       |                       |                     |                      |                      |                     |                    |    |    |    |    |                     |                    |                     |                      |
| Type  |                    |                       |                       |                     |                      |                      |                     |                    |    |    |    |    |                     |                    |                     |                      |
| Reset |                    |                       |                       |                     |                      |                      |                     |                    |    |    |    |    |                     |                    |                     |                      |
| Bit   | 15                 | 14                    | 13                    | 12                  | 11                   | 10                   | 9                   | 8                  | 7  | 6  | 5  | 4  | 3                   | 2                  | 1                   | 0                    |
| Name  | TX_TFF_UNDR_INT_EN | TX_MISVLAN_ERR_INT_EN | TX_MISPAGE_ERR_INT_EN | TX_RPAGE_ERR_INT_EN | TX_RPAGE_TOUT_INT_EN | TX_GPAGE_TOUT_INT_EN | TX_RDPB_TOUT_INT_EN | TX_DEQ_TOUT_INT_EN |    |    |    |    | RX_AFFL_TOUT_INT_EN | RX_ARL_TOUT_INT_EN | RX_WRPB_TOUT_INT_EN | RX_GPAGE_TOUT_INT_EN |
| Type  | RW                 | RW                    | RW                    | RW                  | RW                   | RW                   | RW                  | RW                 |    |    |    |    | RW                  | RW                 | RW                  | RW                   |
| Reset | 0                  | 0                     | 0                     | 0                   | 0                    | 0                    | 0                   | 0                  |    |    |    |    | 0                   | 0                  | 0                   | 0                    |

| Bit(s) | Name                  | Description                                                                               |
|--------|-----------------------|-------------------------------------------------------------------------------------------|
| 15     | TX_TFF_UNDR_INT_EN    | <b>TXMAC TXFIFO Under run Interrupt Enable</b><br>0: Disabled<br>1: Enabled               |
| 14     | TX_MISVLAN_ERR_INT_EN | <b>TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable</b><br>0: Disabled<br>1: Enabled |
| 13     | TX_MISPAGE_ERR_INT_EN | <b>TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable</b><br>0: Disabled<br>1: Enabled |
| 12     | TX_RPAGE_ERR_INT_EN   | <b>TX_CTRL Release Page Count Error Interrupt Enable</b><br>0: Disabled<br>1: Enabled     |
| 11     | TX_RPAGE_TOUT_INT_EN  | <b>TX_CTRL Release Page Timeout Interrupt Enable</b><br>0: Disabled<br>1: Enabled         |
| 10     | TX_GPAGE_TOUT_INT_EN  | <b>TX_CTRL Get Page Timeout Interrupt Enable</b><br>0: Disabled<br>1: Enabled             |
| 9      | TX_RDPB_TOUT_INT_EN   | <b>TX_CTRL RD_PB Timeout Interrupt Enable</b><br>0: Disabled<br>1: Enabled                |
| 8      | TX_DEQ_TOUT_INT_EN    | <b>TX_CTRL DEQ Timeout Interrupt Enable</b><br>0: Disabled                                |

| Bit(s) | Name                 | Description                                      |
|--------|----------------------|--------------------------------------------------|
|        |                      | 1: Enabled                                       |
| 3      | RX_AFF_FULL_INT_EN   | <b>RX_CTRL Agent FIFO Full Interrupt Enable</b>  |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |
| 2      | RX_ARL_TOUT_INT_EN   | <b>RX_CTRL ARL Timeout Interrupt Enable</b>      |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |
| 1      | RX_WRPB_TOUT_INT_EN  | <b>RX_CTRL WR_PB Timeout Interrupt Enable</b>    |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |
| 0      | RX_GPAGE_TOUT_INT_EN | <b>RX_CTRL Get Page Timeout Interrupt Enable</b> |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |

**15023014      PINT\_STS\_PO      Port 0 interrupt status register      00000000**

| Bit   | 31              | 30                 | 29                 | 28               | 27                | 26                | 25               | 24              | 23 | 22 | 21 | 20 | 19              | 18              | 17               | 16                |
|-------|-----------------|--------------------|--------------------|------------------|-------------------|-------------------|------------------|-----------------|----|----|----|----|-----------------|-----------------|------------------|-------------------|
| Name  |                 |                    |                    |                  |                   |                   |                  |                 |    |    |    |    |                 |                 |                  |                   |
| Type  |                 |                    |                    |                  |                   |                   |                  |                 |    |    |    |    |                 |                 |                  |                   |
| Reset |                 |                    |                    |                  |                   |                   |                  |                 |    |    |    |    |                 |                 |                  |                   |
| Bit   | 15              | 14                 | 13                 | 12               | 11                | 10                | 9                | 8               | 7  | 6  | 5  | 4  | 3               | 2               | 1                | 0                 |
| Name  | TX_TFF_UNDR_INT | TX_MISVLAN_ERR_INT | TX_MISPAGE_ERR_INT | TX_RPAGE_ERR_INT | TX_RPAGE_TOUT_INT | TX_GPAGE_TOUT_INT | TX_RDPB_TOUT_INT | TX_DEQ_TOUT_INT |    |    |    |    | RX_AFF_FULL_INT | RX_ARL_TOUT_INT | RX_WRPB_TOUT_INT | RX_GPAGE_TOUT_INT |
| Type  | RC              | RC                 | RC                 | RC               | RC                | RC                | RC               | RC              |    |    |    |    | RC              | RC              | RC               | RC                |
| Reset | 0               | 0                  | 0                  | 0                | 0                 | 0                 | 0                | 0               |    |    |    |    | 0               | 0               | 0                | 0                 |

| Bit(s) | Name               | Description                                                                          |
|--------|--------------------|--------------------------------------------------------------------------------------|
| 15     | TX_TFF_UNDR_INT    | <b>TXMAC TXFIFO Under run Interrupt</b><br><br>0: False<br><br>1: True               |
| 14     | TX_MISVLAN_ERR_INT | <b>TX_CTRL PKT INFO VLAN Mismatch Error Interrupt</b><br><br>0: False<br><br>1: True |
| 13     | TX_MISPAGE_ERR_INT | <b>TX_CTRL PKT INFO Page Mismatch Error Interrupt</b><br><br>0: False<br><br>1: True |
| 12     | TX_RPAGE_ERR_INT   | <b>TX_CTRL Release Page Count Error Interrupt</b><br><br>0: False<br><br>1: True     |
| 11     | TX_RPAGE_TOUT_INT  | <b>TX_CTRL Release Page Timeout Interrupt</b><br><br>0: False<br><br>1: True         |
| 10     | TX_GPAGE_TOUT_INT  | <b>TX_CTRL Get Page Timeout Interrupt</b><br><br>0: False<br><br>1: True             |
| 9      | TX_RDPB_TOUT_INT   | <b>TX_CTRL RD_PB Timeout Interrupt</b><br><br>0: False<br><br>1: True                |
| 8      | TX_DEQ_TOUT_INT    | <b>TX_CTRL DEQ Timeout Interrupt</b><br><br>0: False                                 |

| Bit(s) | Name              | Description                               |
|--------|-------------------|-------------------------------------------|
|        |                   | 1: True                                   |
| 3      | RX_AFF_FULL_INT   | <b>RX_CTRL Agent FIFO Full Interrupt</b>  |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |
| 2      | RX_ARL_TOUT_INT   | <b>RX_CTRL ARL Timeout Interrupt</b>      |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |
| 1      | RX_WRPB_TOUT_INT  | <b>RX_CTRL WR_PB Timeout Interrupt</b>    |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |
| 0      | RX_GPAGE_TOUT_INT | <b>RX_CTRL Get Page Timeout Interrupt</b> |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |

15023018      P0\_DBG\_CNT      Port 0 debug count      00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22           | 21 | 20 | 19 | 18         | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|--------------|----|----|----|------------|----|----|
| Name  |    |    |    |    |    |    |    |    |    |              |    |    |    |            |    |    |
| Type  |    |    |    |    |    |    |    |    |    |              |    |    |    |            |    |    |
| Reset |    |    |    |    |    |    |    |    |    |              |    |    |    |            |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6            | 5  | 4  | 3  | 2          | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    | TX_FIFO_URUN |    |    |    | RX_FIFO_OV |    |    |
| Type  |    |    |    |    |    |    |    |    |    | RO           |    |    |    | RO         |    |    |
| Reset |    |    |    |    |    |    |    |    |    | 0            | 0  | 0  |    | 0          | 0  | 0  |

| Bit(s) | Name         | Description                                                                     |
|--------|--------------|---------------------------------------------------------------------------------|
| 6:4    | TX_FIFO_URUN | Underrun count of TX FIFO. The field is increased when TX FIFO underrun occurs. |
| 2:0    | RX_FIFO_OV   | Overflow count of RX FIFO. The field is increased when RX FIFO overflow occurs. |

15023020      P0\_WOL      Port 0 WOL      00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19      | 18      | 17          | 16      |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|---------|---------|-------------|---------|
| Name  | WOL_DBG |    |    |    |    |    |    |    |    |    |    |    |         |         | WOL_INT_STS | WOL_STS |
| Type  | RO      |    |    |    |    |    |    |    |    |    |    |    |         |         | W1C         | RO      |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       | 0       | 0           | 0       |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3       | 2       | 1           | 0       |
| Name  |         |    |    |    |    |    |    |    |    |    |    |    | SNP_PKT | CRC_DIS | WOL_INT_EN  | WOL_EN  |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    | RW      | RW      | RW          | RW      |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    | 0       | 0       | 0           | 0       |

| Bit(s) | Name        | Description                                                                                                                                                                                                |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:18  | WOL_DBG     | <b>Port0 Wake-up On Lan Debug Signals</b>                                                                                                                                                                  |
| 17     | WOL_INT_STS | <b>Port0 Wake-up On Lan Interrupt Status</b>                                                                                                                                                               |
| 16     | WOL_STS     | <b>Port0 Wake-up On Lan Status</b><br><br>If enable WOL_EN, this bit will change from 0 to 1 when GMAC RX state machine enter IDLE state. It indicates GMAC will drop all packets and detect magic packet. |
| 3      | SNP_PKT     | <b>Port0 Wake-up On Lan with snoopy packet</b><br><br>0: Disable<br><br>1: Enable                                                                                                                          |
| 2      | CRC_DIS     | <b>Port0 Wake-up On Lan with CRC Check Disable</b><br><br>0: CRC check enable<br><br>1: CRC check disable                                                                                                  |
| 1      | WOL_INT_EN  | <b>Port0 Wake-up On Lan Interrupt Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                            |
| 0      | WOL_EN      | <b>Port0 Wake-up On Lan Function Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                             |



15023024      P0\_PFC\_STS      Port 0 PFC status      00000000

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|
| Name  |            |    |    |    |    |    |    |    |            |    |    |    |    |    |    |    |
| Type  |            |    |    |    |    |    |    |    |            |    |    |    |    |    |    |    |
| Reset |            |    |    |    |    |    |    |    |            |    |    |    |    |    |    |    |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PFC_STS |    |    |    |    |    |    |    | RX_PFC_STS |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    | RO         |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                           |
|--------|------------|-----------------------------------------------------------------------|
| 15:8   | TX_PFC_STS | Port0 PFC TX pause on status of 8 priorities 1: pause on 0: pause off |
| 7:0    | RX_PFC_STS | Port0 PFC RX pause on status of 8 priorities 1: pause on 0: pause off |

15023030      **P0\_PFC\_RX\_PSON\_CNT\_L**      Port 0 RX PFC pause on counter for low priority      00000000

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q3_RX_PSON_CNT |    |    |    |    |    |    |    | Q2_RX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q1_RX_PSON_CNT |    |    |    |    |    |    |    | Q0_RX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                |
|--------|----------------|--------------------------------------------|
| 31:24  | Q3_RX_PSON_CNT | PFC RX pause on count for port0 priority 3 |
| 23:16  | Q2_RX_PSON_CNT | PFC RX pause on count for port0 priority 2 |
| 15:8   | Q1_RX_PSON_CNT | PFC RX pause on count for port0 priority 1 |
| 7:0    | Q0_RX_PSON_CNT | PFC RX pause on count for port0 priority 0 |

15023034      **P0\_PFC\_RX\_PSON\_CNT\_H**      Port 0 RX PFC pause on counter for high priority      00000000

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q7_RX_PSON_CNT |    |    |    |    |    |    |    | Q6_RX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q5_RX_PSON_CNT |    |    |    |    |    |    |    | Q4_RX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                |
|--------|----------------|--------------------------------------------|
| 31:24  | Q7_RX_PSON_CNT | PFC RX pause on count for port0 priority 7 |
| 23:16  | Q6_RX_PSON_CNT | PFC RX pause on count for port0 priority 6 |
| 15:8   | Q5_RX_PSON_CNT | PFC RX pause on count for port0 priority 5 |
| 7:0    | Q4_RX_PSON_CNT | PFC RX pause on count for port0 priority 4 |

15023038      **P0\_PFC\_RX\_PSOFF\_CNT\_L**      Port 0 RX PFC pause off counter for low priority      00000000

| Bit          | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q3_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q2_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q1_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q0_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                 |
|--------|-----------------|---------------------------------------------|
| 31:24  | Q3_RX_PSOFF_CNT | PFC RX pause off count for port0 priority 3 |
| 23:16  | Q2_RX_PSOFF_CNT | PFC RX pause off count for port0 priority 2 |
| 15:8   | Q1_RX_PSOFF_CNT | PFC RX pause off count for port0 priority 1 |
| 7:0    | Q0_RX_PSOFF_CNT | PFC RX pause off count for port0 priority 0 |

1502303C      P0\_PFC\_RX\_PSOFF\_CNT\_H      Port 0 RX PFC pause off counter for high priority      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | Q7_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q6_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q4_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                 |
|--------|-----------------|---------------------------------------------|
| 31:24  | Q7_RX_PSOFF_CNT | PFC RX pause off count for port0 priority 7 |
| 23:16  | Q6_RX_PSOFF_CNT | PFC RX pause off count for port0 priority 6 |
| 15:8   | Q5_RX_PSOFF_CNT | PFC RX pause off count for port0 priority 5 |
| 7:0    | Q4_RX_PSOFF_CNT | PFC RX pause off count for port0 priority 4 |

15023040      **P0\_PFC\_TX\_PSON\_CNT\_L**      Port 0 TX PFC pause on counter for low priority      00000000

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q3_TX_PSON_CNT |    |    |    |    |    |    |    | Q2_TX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q1_TX_PSON_CNT |    |    |    |    |    |    |    | Q0_TX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                |
|--------|----------------|--------------------------------------------|
| 31:24  | Q3_TX_PSON_CNT | PFC TX pause on count for port0 priority 3 |
| 23:16  | Q2_TX_PSON_CNT | PFC TX pause on count for port0 priority 2 |
| 15:8   | Q1_TX_PSON_CNT | PFC TX pause on count for port0 priority 1 |
| 7:0    | Q0_TX_PSON_CNT | PFC TX pause on count for port0 priority 0 |

15023044      **P0\_PFC\_TX\_PSON\_CNT\_H**      Port 0 TX PFC pause on counter for high priority      00000000

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q7_TX_PSON_CNT |    |    |    |    |    |    |    | Q6_TX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q5_TX_PSON_CNT |    |    |    |    |    |    |    | Q4_TX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                |
|--------|----------------|--------------------------------------------|
| 31:24  | Q7_TX_PSON_CNT | PFC TX pause on count for port0 priority 7 |
| 23:16  | Q6_TX_PSON_CNT | PFC TX pause on count for port0 priority 6 |
| 15:8   | Q5_TX_PSON_CNT | PFC TX pause on count for port0 priority 5 |
| 7:0    | Q4_TX_PSON_CNT | PFC TX pause on count for port0 priority 4 |

15023048      **P0\_PFC\_TX\_PSOFF\_CNT\_L**      Port 0 TX PFC pause off counter for low priority      00000000

| Bit          | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q3_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q2_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q1_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q0_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                 |
|--------|-----------------|---------------------------------------------|
| 31:24  | Q3_TX_PSOFF_CNT | PFC TX pause off count for port0 priority 3 |
| 23:16  | Q2_TX_PSOFF_CNT | PFC TX pause off count for port0 priority 2 |
| 15:8   | Q1_TX_PSOFF_CNT | PFC TX pause off count for port0 priority 1 |
| 7:0    | Q0_TX_PSOFF_CNT | PFC TX pause off count for port0 priority 0 |



1502304C      P0\_PFC\_TX\_PSOFF\_CNT\_H      Port 0 TX PFC pause off counter for high priority      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | Q7_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q6_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q4_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                 |
|--------|-----------------|---------------------------------------------|
| 31:24  | Q7_TX_PSOFF_CNT | PFC TX pause off count for port0 priority 7 |
| 23:16  | Q6_TX_PSOFF_CNT | PFC TX pause off count for port0 priority 6 |
| 15:8   | Q5_TX_PSOFF_CNT | PFC TX pause off count for port0 priority 5 |
| 7:0    | Q4_TX_PSOFF_CNT | PFC TX pause off count for port0 priority 4 |

**150230B0      PFC\_CTRL      PFC control register      00000000**

| Bit   | 31               | 30               | 29               | 28 | 27 | 26               | 25               | 24               | 23               | 22      | 21 | 20               | 19      | 18      | 17               | 16               |
|-------|------------------|------------------|------------------|----|----|------------------|------------------|------------------|------------------|---------|----|------------------|---------|---------|------------------|------------------|
| Name  |                  |                  |                  |    |    |                  |                  |                  |                  |         |    | PFC_A<br>UTO_EN6 |         |         | PFC_A<br>UTO_EN3 | PFC_A<br>UTO_EN2 |
| Type  |                  |                  |                  |    |    |                  |                  |                  |                  |         |    | RO               |         |         | RO               | RO               |
| Reset |                  |                  |                  |    |    |                  |                  |                  |                  |         |    | 0                |         |         | 0                | 0                |
| Bit   | 15               | 14               | 13               | 12 | 11 | 10               | 9                | 8                | 7                | 6       | 5  | 4                | 3       | 2       | 1                | 0                |
| Name  | PFC_A<br>UTO_EN1 | PFC_A<br>UTO_EN0 | PFC_SY<br>NC_EN6 |    |    | PFC_SY<br>NC_EN3 | PFC_SY<br>NC_EN2 | PFC_SY<br>NC_EN1 | PFC_SY<br>NC_EN0 | PFC_EN6 |    |                  | PFC_EN3 | PFC_EN2 | PFC_EN1          | PFC_EN0          |
| Type  | RO               | RO               | RW               |    |    | RW               | RW               | RW               | RW               | RW      |    |                  | RW      | RW      | RW               | RW               |
| Reset | 0                | 0                | 0                |    |    | 0                | 0                | 0                | 0                | 0       |    |                  | 0       | 0       | 0                | 0                |

| Bit(s) | Name         | Description                                                                                |
|--------|--------------|--------------------------------------------------------------------------------------------|
| 20     | PFC_AUTO_EN6 | <b>PFC auto enable status of user port 6.</b><br><br>0: Disabled<br><br>1: Enabled         |
| 17     | PFC_AUTO_EN3 | <b>PFC auto enable status of user port 3.</b><br><br>0: Disabled<br><br>1: Enabled         |
| 16     | PFC_AUTO_EN2 | <b>PFC auto enable status of user port 2.</b><br><br>0: Disabled<br><br>1: Enabled         |
| 15     | PFC_AUTO_EN1 | <b>PFC auto enable status of user port 1.</b><br><br>0: Disabled<br><br>1: Enabled         |
| 14     | PFC_AUTO_EN0 | <b>PFC auto enable status of user port 0.</b><br><br>0: Disabled<br><br>1: Enabled         |
| 13     | PFC_SYNC_EN6 | <b>Enable the PFC auto-sync ability of user port 6.</b><br><br>0: Disable<br><br>1: Enable |
| 10     | PFC_SYNC_EN3 | <b>Enable the PFC auto-sync ability of user port 3.</b><br><br>0: Disable<br><br>1: Enable |
| 9      | PFC_SYNC_EN2 | <b>Enable the PFC auto-sync ability of user port 2.</b><br><br>0: Disable                  |

| Bit(s) | Name         | Description                                             |
|--------|--------------|---------------------------------------------------------|
|        |              | 1: Enable                                               |
| 8      | PFC_SYNC_EN1 | <b>Enable the PFC auto-sync ability of user port 1.</b> |
|        |              | 0: Disable                                              |
|        |              | 1: Enable                                               |
| 7      | PFC_SYNC_EN0 | <b>Enable the PFC auto-sync ability of user port 0.</b> |
|        |              | 0: Disable                                              |
|        |              | 1: Enable                                               |
| 6      | PFC_EN6      | <b>Enable the PFC ability of user port 6.</b>           |
|        |              | 0: Disable                                              |
|        |              | 1: Enable                                               |
| 3      | PFC_EN3      | <b>Enable the PFC ability of user port 3.</b>           |
|        |              | 0: Disable                                              |
|        |              | 1: Enable                                               |
| 2      | PFC_EN2      | <b>Enable the PFC ability of user port 2.</b>           |
|        |              | 0: Disable                                              |
|        |              | 1: Enable                                               |
| 1      | PFC_EN1      | <b>Enable the PFC ability of user port 1.</b>           |
|        |              | 0: Disable                                              |
|        |              | 1: Enable                                               |
| 0      | PFC_EN0      | <b>Enable the PFC ability of user port 0.</b>           |
|        |              | 0: Disable                                              |
|        |              | 1: Enable                                               |

150230B4      **PFC\_AUTO\_SYNC\_DLY\_SEL**      PFC auto sync delay selection      00000000

| Bit   | 31 | 30 | 29                     | 28 | 27 | 26 | 25 | 24 | 23                     | 22 | 21                     | 20 | 19                     | 18 | 17                     | 16 |
|-------|----|----|------------------------|----|----|----|----|----|------------------------|----|------------------------|----|------------------------|----|------------------------|----|
| Name  |    |    |                        |    |    |    |    |    |                        |    |                        |    |                        |    |                        |    |
| Type  |    |    |                        |    |    |    |    |    |                        |    |                        |    |                        |    |                        |    |
| Reset |    |    |                        |    |    |    |    |    |                        |    |                        |    |                        |    |                        |    |
| Bit   | 15 | 14 | 13                     | 12 | 11 | 10 | 9  | 8  | 7                      | 6  | 5                      | 4  | 3                      | 2  | 1                      | 0  |
| Name  |    |    | PFC_AUTO_SYNC_DLY_SEL6 |    |    |    |    |    | PFC_AUTO_SYNC_DLY_SEL3 |    | PFC_AUTO_SYNC_DLY_SEL2 |    | PFC_AUTO_SYNC_DLY_SEL1 |    | PFC_AUTO_SYNC_DLY_SEL0 |    |
| Type  |    |    | RW                     |    |    |    |    |    | RW                     |    | RW                     |    | RW                     |    | RW                     |    |
| Reset |    |    | 0                      | 0  |    |    |    |    | 0                      | 0  | 0                      | 0  | 0                      | 0  | 0                      | 0  |

| Bit(s) | Name                   | Description                                                                                                                                          |
|--------|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13:12  | PFC_AUTO_SYNC_DLY_SEL6 | <b>Select the delay of sending PFC auto sync packet of user port 6</b><br><br>0: Delay 0s<br><br>1: Delay 0.5s<br><br>2: Delay 1s<br><br>3: Delay 2s |
| 7:6    | PFC_AUTO_SYNC_DLY_SEL3 | <b>Select the delay of sending PFC auto sync packet of user port 3</b><br><br>0: Delay 0s<br><br>1: Delay 0.5s<br><br>2: Delay 1s<br><br>3: Delay 2s |
| 5:4    | PFC_AUTO_SYNC_DLY_SEL2 | <b>Select the delay of sending PFC auto sync packet of user port 2</b><br><br>0: Delay 0s<br><br>1: Delay 0.5s<br><br>2: Delay 1s<br><br>3: Delay 2s |
| 3:2    | PFC_AUTO_SYNC_DLY_SEL1 | <b>Select the delay of sending PFC auto sync packet of user port 1</b><br><br>0: Delay 0s<br><br>1: Delay 0.5s<br><br>2: Delay 1s<br><br>3: Delay 2s |
| 1:0    | PFC_AUTO_SYNC_DLY_SEL0 | <b>Select the delay of sending PFC auto sync packet of user port 0</b><br><br>0: Delay 0s<br><br>1: Delay 0.5s<br><br>2: Delay 1s                    |

| Bit(s) | Name | Description |
|--------|------|-------------|
|        |      | 3: Delay 2s |

**150230B8 SGMII\_2P5G\_SPD\_CTRL SGMII speed status control register 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21                                | 20 | 19                                      | 18 | 17                                               | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|-----------------------------------|----|-----------------------------------------|----|--------------------------------------------------|----|
| Name  |    |    |    |    |    |    |    |    |    |    |                                   |    |                                         |    |                                                  |    |
| Type  |    |    |    |    |    |    |    |    |    |    |                                   |    |                                         |    |                                                  |    |
| Reset |    |    |    |    |    |    |    |    |    |    |                                   |    |                                         |    |                                                  |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5                                 | 4  | 3                                       | 2  | 1                                                | 0  |
| Name  |    |    |    |    |    |    |    |    |    |    | P6_SG<br>MII_2P<br>5G_SP<br>D_STS |    | FORCE<br>_P6_SG<br>MII_2P<br>5G_SP<br>D |    | FORCE<br>_MODE<br>_P6_SG<br>MII_2P<br>5G_SP<br>D |    |
| Type  |    |    |    |    |    |    |    |    |    |    | RO                                |    | RW                                      |    | RW                                               |    |
| Reset |    |    |    |    |    |    |    |    |    |    | 0                                 |    | 0                                       |    | 0                                                |    |

| Bit(s) | Name                         | Description                                                                                                       |
|--------|------------------------------|-------------------------------------------------------------------------------------------------------------------|
| 5      | P6_SGMII_2P5G_SPD_STS        | <b>Port 6 SGMII speed status.</b><br><br>0: SGMII is not running at 2.5G<br><br>1: SGMII is running at 2.5G       |
| 3      | FORCE_P6_SGMII_2P5G_SPD      | <b>Force port 6 SGMII speed status.</b><br><br>0: SGMII is not running at 2.5G<br><br>1: SGMII is running at 2.5G |
| 1      | FORCE_MODE_P6_SGMII_2P5G_SPD | <b>Port 6 SGMII speed force Mode.</b><br><br>0: Force mode is off<br><br>1: Force mode is on                      |

**150230C0**      **LPDET\_CTRL**      **Loop detection control register**      **00132000**

| Bit   | 31           | 30           | 29 | 28 | 27        | 26        | 25        | 24        | 23              | 22             | 21         | 20           | 19             | 18              | 17            | 16            |
|-------|--------------|--------------|----|----|-----------|-----------|-----------|-----------|-----------------|----------------|------------|--------------|----------------|-----------------|---------------|---------------|
| Name  |              | LPDET_EN6    |    |    | LPDET_EN3 | LPDET_EN2 | LPDET_EN1 | LPDET_EN0 | LPDET_PERIOD_EN | LPDET_ALARM_EN | LPDET_PASS | LPDET_PERIOD | LPDET_LED_RATE | LPDET_THRESHOLD |               |               |
| Type  |              | RW           |    |    | RW        | RW        | RW        | RW        | RW              | RW             | RW         | RW           | RW             | RW              |               |               |
| Reset |              | 0            |    |    | 0         | 0         | 0         | 0         | 0               | 0              | 0          | 1            | 0              | 0               | 1             | 1             |
| Bit   | 15           | 14           | 13 | 12 | 11        | 10        | 9         | 8         | 7               | 6              | 5          | 4            | 3              | 2               | 1             | 0             |
| Name  | LPDET_ST_LOP | LPDET_ST_BCS |    |    |           |           |           |           |                 | LPDET_ALARM_6  |            |              | LPDET_ALARM_3  | LPDET_ALARM_2   | LPDET_ALARM_1 | LPDET_ALARM_0 |
| Type  | RO           | RO           |    |    |           |           |           |           |                 | RO             |            |              | RO             | RO              | RO            | W1C           |
| Reset | 0            | 0            |    |    |           |           |           |           |                 | 0              |            |              | 0              | 0               | 0             | 0             |

| Bit(s) | Name            | Description                                                                                                                                  |
|--------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 30     | LPDET_EN6       | <b>Enable the loop detection ability of user port 6.</b><br><br>0: Disable<br><br>1: Enable                                                  |
| 27     | LPDET_EN3       | <b>Enable the loop detection ability of user port 3.</b><br><br>0: Disable<br><br>1: Enable                                                  |
| 26     | LPDET_EN2       | <b>Enable the loop detection ability of user port 2.</b><br><br>0: Disable<br><br>1: Enable                                                  |
| 25     | LPDET_EN1       | <b>Enable the loop detection ability of user port 1.</b><br><br>0: Disable<br><br>1: Enable                                                  |
| 24     | LPDET_EN0       | <b>Enable the loop detection ability of user port 0.</b><br><br>0: Disable<br><br>1: Enable                                                  |
| 23     | LPDET_PERIOD_EN | <b>The loop detection frame is triggered by a periodical timer or by broadcast storm.</b><br><br>0: Broadcast mode<br><br>1: Periodical mode |
| 22     | LPDET_ALARM_EN  | <b>Enable 2 kHz alarm output and per-port LED when loop is detected.</b><br><br>0: Disable<br><br>1: Enable                                  |
| 21     | LPDET_PASS      | <b>Loop detection frame is blocked or passed to packet memory.</b>                                                                           |

| Bit(s) | Name            | Description                                                                                                                              |
|--------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------|
|        |                 | 0: Blocked                                                                                                                               |
|        |                 | 1: Pass                                                                                                                                  |
| 20     | LPDET_PERIOD    | <b>Interval of transmitting loop detection frame in Periodical mode.</b>                                                                 |
|        |                 | 0: 125 us                                                                                                                                |
|        |                 | 1: 1000 ms                                                                                                                               |
| 19     | LPDET_LED_RATE  | <b>LED blinking rate of per port when loop is detected.</b>                                                                              |
|        |                 | 0: LED blinking at 2 Hz                                                                                                                  |
|        |                 | 1: LED blinking at 4 Hz                                                                                                                  |
| 18:16  | LPDET_THRESHOLD | <b>Number of missed loop detection frame before 2 kHz alarm is reset</b>                                                                 |
| 15     | LPDET_ST_LOOP   | <b>The status of loop detection. In LOOP state, the loop detection frame is transmitted, and the loop detection frames are received.</b> |
|        |                 | 0: Not in Loop state                                                                                                                     |
|        |                 | 1: Loop state                                                                                                                            |
| 14     | LPDET_ST_BCST   | <b>The status of loop detection. In BCST state, the loop detection frame is transmitted, but no loop detection frame is received.</b>    |
|        |                 | 0: Not in BCST state                                                                                                                     |
|        |                 | 1: BCST state                                                                                                                            |
| 6      | LPDET_ALARM6    | <b>The status of loop detected on port 6. This bit is cleared when LPDET_ALARM0 is written as 1.</b>                                     |
|        |                 | 0: Not detected                                                                                                                          |
|        |                 | 1: Detected                                                                                                                              |
| 3      | LPDET_ALARM3    | <b>The status of loop detected on port 3. This bit is cleared when LPDET_ALARM0 is written as 1.</b>                                     |
|        |                 | 0: Not detected                                                                                                                          |
|        |                 | 1: Detected                                                                                                                              |
| 2      | LPDET_ALARM2    | <b>The status of loop detected on port 2. This bit is cleared when LPDET_ALARM0 is written as 1.</b>                                     |
|        |                 | 0: Not detected                                                                                                                          |
|        |                 | 1: Detected                                                                                                                              |
| 1      | LPDET_ALARM1    | <b>The status of loop detected on port 1. This bit is cleared when LPDET_ALARM0 is written as 1.</b>                                     |
|        |                 | 0: Not detected                                                                                                                          |
|        |                 | 1: Detected                                                                                                                              |
| 0      | LPDET_ALARM0    | <b>The status of loop detected on port 0. This bit is cleared when it is written as 1.</b>                                               |



| Bit(s) | Name | Description     |
|--------|------|-----------------|
|        |      | 0: Not detected |
|        |      | 1: Detected     |

150230C8      LPDET\_SA\_MSB      Loop detection SA MSB      88740180

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | LPDET_TYPE   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1            | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 1  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | LPDET_SA_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                             |
|--------|--------------|-----------------------------------------|
| 31:16  | LPDET_TYPE   | Loop detection frame type               |
| 15:0   | LPDET_SA_MSB | Bits [47:32] of loop detection frame SA |

150230CC      LPDET\_SA\_LSB      Loop detection SA LSB      C2000001

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | LPDET_SA_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1            | 1  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | LPDET_SA_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name         | Description                             |
|--------|--------------|-----------------------------------------|
| 31:0   | LPDET_SA_LSB | Bits [31:00] of loop detection frame SA |

150230D0      LPDET\_RXSA\_MSB      Loop detection RX SA\_MSB      00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23           | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|--------------|----|----|----|---------------|----|----|----|
| Name  |    |    |    |    |    |    |    |    | LPDET_RXPORT |    |    |    | LPDET_SRCPORT |    |    |    |
| Type  |    |    |    |    |    |    |    |    | RO           |    |    |    | RO            |    |    |    |
| Reset |    |    |    |    |    |    |    |    | 0            | 0  | 0  | 0  | 0             | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7            | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |              |    |    |    |               |    |    |    |
| Type  |    |    |    |    |    |    |    |    |              |    |    |    |               |    |    |    |
| Reset |    |    |    |    |    |    |    |    |              |    |    |    |               |    |    |    |

| Bit(s) | Name          | Description                                                                     |
|--------|---------------|---------------------------------------------------------------------------------|
| 23:20  | LPDET_RXPORT  | This is the 4-bit port number from which the loop detection frame was received. |
| 19:16  | LPDET_SRCPORT | This is the 4-bit source port number in the received loop detection frame.      |

**150230E0      GMACCR      Global MAC control register      00001E3F**

| Bit   | 31 | 30 | 29 | 28       | 27 | 26 | 25 | 24 | 23 | 22 | 21           | 20 | 19       | 18       | 17             | 16 |
|-------|----|----|----|----------|----|----|----|----|----|----|--------------|----|----------|----------|----------------|----|
| Name  |    |    |    |          |    |    |    |    |    |    |              |    | TXCRC_EN | RXCRC_EN | PRMBL_LMT_EN   |    |
| Type  |    |    |    |          |    |    |    |    |    |    |              |    | RW       | RW       | RW             |    |
| Reset |    |    |    |          |    |    |    |    |    |    |              |    | 0        | 0        | 0              |    |
| Bit   | 15 | 14 | 13 | 12       | 11 | 10 | 9  | 8  | 7  | 6  | 5            | 4  | 3        | 2        | 1              | 0  |
| Name  |    |    |    | MTCC_LMT |    |    |    |    |    |    | MAX_RX_JUMBO |    |          |          | MAX_RX_PKT_LEN |    |
| Type  |    |    |    | RW       |    |    |    |    |    |    | RW           |    |          |          | RW             |    |
| Reset |    |    |    | 1        | 1  | 1  | 1  |    |    |    | 1            | 1  | 1        | 1        | 1              | 1  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                               |
|--------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19     | TXCRC_EN     | <b>TX CRC Enable</b><br><br>0: TX CRC insertion is enabled.<br><br>1: TX CRC insertion is disabled.                                                                                                                                       |
| 18     | RXCRC_EN     | <b>RX CRC Enable</b><br><br>0: RX CRC removal is enabled.<br><br>1: RX CRC removal is disabled.                                                                                                                                           |
| 17     | PRMBL_LMT_EN | <b>Preamble Limit Enable</b><br><br>0: RXMAC can recognize SFD anytime.<br><br>1: RXMAC will recognize SFD within 7 Preamble bits, if SFD (0xd5) shows up after 7 bits preamble; RXMAC will not recognize it and treat it as no SFD case. |
| 12:9   | MTCC_LMT     | <b>MTCC Limit.</b><br><br>Maximum transmitted collision count limitation<br><br>0: Disable TX collision abort function, send packet until the packet is sent successfully.<br><br>15: Maximum transmitted collision count is up to 15.    |
| 5:2    | MAX_RX_JUMBO | <b>Maximum length of ingress jumbo frames</b><br><br>0: Reserved.<br><br>1: Reserved.<br><br>2: 2K Bytes.<br><br>3: 3K Bytes.<br><br>4: 4K Bytes.<br><br>5: 5K Bytes.<br><br>6: 6K Bytes.<br><br>7: 7K Bytes.                             |

| Bit(s) | Name           | Description                                                                                                                                                                                                                                                  |
|--------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                | 8: 8K Bytes.                                                                                                                                                                                                                                                 |
|        |                | 9: 9K Bytes.                                                                                                                                                                                                                                                 |
|        |                | 10: 10K Bytes.                                                                                                                                                                                                                                               |
|        |                | 11: 11K Bytes.                                                                                                                                                                                                                                               |
|        |                | 12: 12K Bytes.                                                                                                                                                                                                                                               |
|        |                | 13: 13K Bytes.                                                                                                                                                                                                                                               |
|        |                | 14: 14K Bytes.                                                                                                                                                                                                                                               |
|        |                | 15: 15K Bytes.                                                                                                                                                                                                                                               |
| 1:0    | MAX_RX_PKT_LEN | <b>Max Receive Packet Length.</b><br><br>Maximum length of ingress packet including CRC which can be received by MAC<br><br>0: 1518 bytes for untagged frames; 1522 bytes for tagged frames.<br><br>1: 1536bytes<br><br>2: 1552 bytes<br><br>3: MAX_RX_JUMBO |

**150230E4      SMACCR0      System MAC control register 0      0017A501**

| Bit          | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | SMACCR0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 1  | 1  |
| Bit          | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | SMACCR0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 1       | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name    | Description                                                                                                                |
|--------|---------|----------------------------------------------------------------------------------------------------------------------------|
| 31:0   | SMACCR0 | System MAC Address, sys_mac [31:0]. The first 32-bit of system MAC address. It is unique and is specified for pause frame. |

**150230E8      SMACCR1      System MAC control register 1      00000000**

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | SMACCR1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                                                                                  |
|--------|---------|------------------------------------------------------------------------------------------------------------------------------|
| 15:0   | SMACCR1 | System MAC Address, sys_mac [47:32]. The second 16-bit of system MAC address. It is unique and is specified for pause frame. |



**150230F0**      **CKGCR**      **Clock gating control register**      **00001E03**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21             | 20            | 19 | 18 | 17                     | 16                    |
|-------|----------------|----|----|----|----|----|----|----|----|----|----------------|---------------|----|----|------------------------|-----------------------|
| Name  |                |    |    |    |    |    |    |    |    |    |                |               |    |    |                        |                       |
| Type  |                |    |    |    |    |    |    |    |    |    |                |               |    |    |                        |                       |
| Reset |                |    |    |    |    |    |    |    |    |    |                |               |    |    |                        |                       |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5              | 4             | 3  | 2  | 1                      | 0                     |
| Name  | LPI_TXIDLE_THD |    |    |    |    |    |    |    |    |    | CKG_T<br>XIDLE | CKG_R<br>XLPI |    |    | CKG_L<br>NKDN_<br>PORT | CKG_L<br>NKDN_<br>GLB |
| Type  | RW             |    |    |    |    |    |    |    |    |    | RW             | RW            |    |    | RW                     | RW                    |
| Reset | 0              | 0  | 0  | 1  | 1  | 1  | 1  | 0  |    |    | 0              | 0             |    |    | 1                      | 1                     |

| Bit(s) | Name           | Description                                                                                                                                                                                                                                                                                                                                                       |
|--------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8   | LPI_TXIDLE_THD | <p><b>When there is no packet to be transmitted, and the idle time is greater than LPI_TXIDLE_THD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.</b></p> <p>Default: 30ms (Unit: 1ms)</p>                                                                                                              |
| 5      | CKG_TXIDLE     | <p><b>Stop the TX port clock ticking when the corresponding port has no traffic to send, and the idle time is greater than &lt;LPI_TXIDLE_THD&gt; ms.</b></p> <p>0: Keep the TX port clock ticking.</p> <p>1: Stop the TX port clock ticking when the corresponding port has no traffic to send, and the idle time is greater than &lt;LPI_TXIDLE_THD&gt; ms.</p> |
| 4      | CKG_RXLPI      | <p><b>Stop the RX port clock ticking when the corresponding port enters the LPI mode, and the RX FIFO is empty.</b></p> <p>0: Keep RX port clock ticking.</p> <p>1: Stop the RX port clock ticking when the corresponding port enters the LPI mode, and the RX FIFO is empty.</p>                                                                                 |
| 1      | CKG_LNKDN_PORT | <p><b>Port clock gating: Clock of gmac, port_ctrl, sch</b></p> <p>0: Keep the RX and TX port clock ticking.</p> <p>1: Stop both RX and TX port clock ticking when the corresponding port enters the link-down status for 2 seconds.</p>                                                                                                                           |
| 0      | CKG_LNKDN_GLB  | <p><b>Global clock gating: Clock of bmu, pb_ctrl, arl</b></p> <p>0: Keep the global clock ticking.</p> <p>1: Stop the global clock ticking when port0~port5 enter the link-down status for 2 seconds.</p>                                                                                                                                                         |

**150230F4      GPINT\_EN      Global port interrupt enable register      00000000**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25             | 24               | 23 | 22             | 21 | 20 | 19             | 18             | 17             | 16             |
|-------|----|----|----|----|----|----|----------------|------------------|----|----------------|----|----|----------------|----------------|----------------|----------------|
| Name  |    |    |    |    |    |    |                |                  |    |                |    |    |                |                |                |                |
| Type  |    |    |    |    |    |    |                |                  |    |                |    |    |                |                |                |                |
| Reset |    |    |    |    |    |    |                |                  |    |                |    |    |                |                |                |                |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9              | 8                | 7  | 6              | 5  | 4  | 3              | 2              | 1              | 0              |
| Name  |    |    |    |    |    |    | WOL_I<br>NT_EN | LPDET_<br>INT_EN |    | PC6_IN<br>T_EN |    |    | PC3_IN<br>T_EN | PC2_IN<br>T_EN | PC1_IN<br>T_EN | PC0_IN<br>T_EN |
| Type  |    |    |    |    |    |    | RW             | RW               |    | RW             |    |    | RW             | RW             | RW             | RW             |
| Reset |    |    |    |    |    |    | 0              | 0                |    | 0              |    |    | 0              | 0              | 0              | 0              |

| Bit(s) | Name         | Description                                                                           |
|--------|--------------|---------------------------------------------------------------------------------------|
| 9      | WOL_INT_EN   | <b>Enable interrupt of Wake-On-LAN.</b><br><br>0: Disable<br><br>1: Enable            |
| 8      | LPDET_INT_EN | <b>Enable interrupt when the loop is detected.</b><br><br>0: Disable<br><br>1: Enable |
| 6      | PC6_INT_EN   | <b>Port Controller 6 Interrupt Enable</b><br><br>0: Disable<br><br>1: Enable          |
| 3      | PC3_INT_EN   | <b>Port Controller 3 Interrupt Enable</b><br><br>0: Disable<br><br>1: Enable          |
| 2      | PC2_INT_EN   | <b>Port Controller 2 Interrupt Enable</b><br><br>0: Disable<br><br>1: Enable          |
| 1      | PC1_INT_EN   | <b>Port Controller 1 Interrupt Enable</b><br><br>0: Disable<br><br>1: Enable          |
| 0      | PC0_INT_EN   | <b>Port Controller 0 Interrupt Enable</b><br><br>0: Disable<br><br>1: Enable          |

**150230F8      GPINT\_STS      Global port interrupt status register      00000000**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25          | 24            | 23 | 22          | 21 | 20 | 19          | 18          | 17          | 16          |
|-------|----|----|----|----|----|----|-------------|---------------|----|-------------|----|----|-------------|-------------|-------------|-------------|
| Name  |    |    |    |    |    |    |             |               |    |             |    |    |             |             |             |             |
| Type  |    |    |    |    |    |    |             |               |    |             |    |    |             |             |             |             |
| Reset |    |    |    |    |    |    |             |               |    |             |    |    |             |             |             |             |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9           | 8             | 7  | 6           | 5  | 4  | 3           | 2           | 1           | 0           |
| Name  |    |    |    |    |    |    | WOL_I<br>NT | LPDET_<br>INT |    | PC6_IN<br>T |    |    | PC3_IN<br>T | PC2_IN<br>T | PC1_IN<br>T | PC0_IN<br>T |
| Type  |    |    |    |    |    |    | W1C         | W1C           |    | W1C         |    |    | W1C         | W1C         | W1C         | W1C         |
| Reset |    |    |    |    |    |    | 0           | 0             |    | 0           |    |    | 0           | 0           | 0           | 0           |

| Bit(s) | Name      | Description                                                                                                         |
|--------|-----------|---------------------------------------------------------------------------------------------------------------------|
| 9      | WOL_INT   | <b>Wake-On-LAN interrupt status. This bit is cleared when it is written as 1.</b><br><br>0: False<br><br>1: True    |
| 8      | LPDET_INT | <b>Loop detection interrupt status. This bit is cleared when it is written as 1.</b><br><br>0: False<br><br>1: True |
| 6      | PC6_INT   | <b>Port Controller 6 Interrupt. This bit is cleared when it is written as 1.</b><br><br>0: False<br><br>1: True     |
| 3      | PC3_INT   | <b>Port Controller 3 Interrupt. This bit is cleared when it is written as 1.</b><br><br>0: False<br><br>1: True     |
| 2      | PC2_INT   | <b>Port Controller 2 Interrupt. This bit is cleared when it is written as 1.</b><br><br>0: False<br><br>1: True     |
| 1      | PC1_INT   | <b>Port Controller 1 Interrupt. This bit is cleared when it is written as 1.</b><br><br>0: False<br><br>1: True     |
| 0      | PC0_INT   | <b>Port Controller 0 Interrupt. This bit is cleared when it is written as 1.</b><br><br>0: False<br><br>1: True     |

**15023100 PMCR\_P1 Port 1 MAC control register 00056330**

| Bit   | 31                | 30                | 29                | 28                  | 27                  | 26                   | 25                  | 24           | 23             | 22              | 21             | 20             | 19           | 18 | 17           | 16           |
|-------|-------------------|-------------------|-------------------|---------------------|---------------------|----------------------|---------------------|--------------|----------------|-----------------|----------------|----------------|--------------|----|--------------|--------------|
| Name  | FORCE_MODE_LNK_P1 | FORCE_MODE_SPD_P1 | FORCE_MODE_DPX_P1 | FORCE_MODE_RX_FC_P1 | FORCE_MODE_TX_FC_P1 | FORCE_MODE_EEE100_P1 | FORCE_MODE_EEE1G_P1 |              |                |                 |                |                | IPG_CFG_P1   |    | EXT_PHY_P1   | MAC_MODE_P1  |
| Type  | RW                | RW                | RW                | RW                  | RW                  | RW                   | RW                  |              |                |                 |                |                | RW           |    | RW           | RW           |
| Reset | 0                 | 0                 | 0                 | 0                   | 0                   | 0                    | 0                   |              |                |                 |                |                | 0            | 1  | 0            | 1            |
| Bit   | 15                | 14                | 13                | 12                  | 11                  | 10                   | 9                   | 8            | 7              | 6               | 5              | 4              | 3            | 2  | 1            | 0            |
| Name  |                   | MAC_TX_EN_P1      | MAC_RX_EN_P1      |                     | MAC_PRE_P1          |                      | BKOFF_EN_P1         | BACKPR_EN_P1 | FORCE_EEE1G_P1 | FORCE_EEE100_P1 | FORCE_RX_FC_P1 | FORCE_TX_FC_P1 | FORCE_SPD_P1 |    | FORCE_DPX_P1 | FORCE_LNK_P1 |
| Type  |                   | RW                | RW                |                     | RW                  |                      | RW                  | RW           | RW             | RW              | RW             | RW             | RW           |    | RW           | RW           |
| Reset |                   | 1                 | 1                 |                     | 0                   |                      | 1                   | 1            | 0              | 0               | 1              | 1              | 0            | 0  | 0            | 0            |

| Bit(s) | Name                 | Description                                                                                                                                                                                                         |
|--------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | FORCE_MODE_LNK_P1    | <b>PORT 1 link status force Mode.</b><br><br>0: Force mode is off. (MAC link status is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC link status is determined by force_link_P1 register) |
| 30     | FORCE_MODE_SPD_P1    | <b>PORT 1 speed force Mode.</b><br><br>0: Force mode is off. (MAC speed is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC speed is determined by force_spd_P1 register)                    |
| 29     | FORCE_MODE_DPX_P1    | <b>PORT 1 duplex force Mode.</b><br><br>0: Force mode is off. (MAC duplex mode is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC duplex mode is determined by force_dpx_P1 register)       |
| 28     | FORCE_MODE_RX_FC_P1  | <b>PORT 1 RX FC force Mode.</b><br><br>0: Force mode is off. (MAC RX FC ability is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC RX FC ability is determined by force_rx_fc_P1 register)  |
| 27     | FORCE_MODE_TX_FC_P1  | <b>PORT 1 TX FC force Mode.</b><br><br>0: Force mode is off. (MAC TX FC ability is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC TX FC ability is determined by force_tx_fc_P1 register)  |
| 26     | FORCE_MODE_EEE100_P1 | <b>PORT 1 100M EEE force Mode.</b><br><br>0: Force mode is off. (MAC 100M EEE ability is determined by PHY auto-polling module)                                                                                     |

| Bit(s) | Name                | Description                                                                                                                                                                                                                                                                                                               |
|--------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25     | FORCE_MODE_EEE1G_P1 | <p>1: Force mode is on. (MAC 100M EEE ability is determined by force_eee100_P1 register)</p> <p><b>PORT 1 1G EEE force Mode.</b></p> <p>0: Force mode is off. (MAC 1G EEE ability is determined by PHY auto-polling module)</p> <p>1: Force mode is on. (MAC 1G EEE ability is determined by force_eee1g_P1 register)</p> |
| 19:18  | IPG_CFG_P1          | <p><b>PORT 1 Inter-Frame+ Gap Shrink.</b></p> <p>00: Normal 96-bit IFG</p> <p>01: Transmit 96-bit IFG with short IFG in random behavior</p> <p>10: Shrink 64-bit IFG</p>                                                                                                                                                  |
| 17     | EXT_PHY_P1          | <p><b>PORT 1 External PHY. Port 1 connects with external PHY.</b></p> <p>0: PORT 1 DOES NOT connect with external PHY</p> <p>1: PORT 1 connects with external PHY</p>                                                                                                                                                     |
| 16     | MAC_MODE_P1         | <p><b>PORT 1 MAC Mode. PORT 1 operates in MAC mode</b></p> <p>0: PORT 1 operates in PHY mode</p> <p>1: PORT 1 operates in MAC mode</p>                                                                                                                                                                                    |
| 14     | MAC_TX_EN_P1        | <p><b>Port 1 TX MAC Enable (Note: This bit only has impacts on the MAC function, it has no impact on the link status or Queue manager.)</b></p> <p>0: TX MAC function is disabled</p> <p>1: TX MAC function is enabled</p>                                                                                                |
| 13     | MAC_RX_EN_P1        | <p><b>PORT 1 RX MAC Enable (Note: This bit only has impacts on MAC function, it has no impact on the link status or Queue manager.)</b></p> <p>0: RX MAC function is disabled</p> <p>1: RX MAC function is enabled</p>                                                                                                    |
| 11     | MAC_PRE_P1          | <p><b>TX short preamble mode</b></p> <p>0: The TX short preamble length is disabled.</p> <p>1: The TX short preamble is enabled.</p>                                                                                                                                                                                      |
| 9      | BKOFF_EN_P1         | <p><b>PORT 1 Backoff Enable</b></p> <p>0: Disabled</p> <p>1: Let the MAC of PORT 1 follow the back-off mechanism when collision happens.</p>                                                                                                                                                                              |
| 8      | BACKPR_EN_P1        | <p><b>PORT 1 Backpressure Enable</b></p> <p>0: Disabled</p>                                                                                                                                                                                                                                                               |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7      | FORCE_EEE1G_P1  | <p>1: Enable back pressure mechanism when operating in half-duplex mode with low internal free memory page count.</p> <p><b>PORT 1 Force LPI Mode For 1000Mbps. When (force_mode_P1 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 1.</b></p> <p>0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps.</p> <p>1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps.</p> |
| 6      | FORCE_EEE100_P1 | <p><b>PORT 1 Force LPI Mode For 100Mbps. When (force_mode_P1 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 1.</b></p> <p>0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps.</p> <p>1: Have the ability of entering EEE Low Power Idle mode for 100Mbps.</p>                                                                                                                          |
| 5      | FORCE_RX_FC_P1  | <p><b>PORT 1 Force RX FC. When (force_mode_P1 = 1), this bit is used to control the RX FC ability of PORT 1.</b></p> <p>0: Disabled</p> <p>1: Let the MAC of PORT 1 accept a pause frame when operating in full-duplex mode.</p>                                                                                                                                                                                                     |
| 4      | FORCE_TX_FC_P1  | <p><b>PORT 1 Force TX FC. When (force_mode_P1 = 1), this bit is used to control the TX FC ability of PORT 1.</b></p> <p>0: Disabled</p> <p>1: Let the MAC of PORT 1 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.</p>                                                                                                                                                          |
| 3:2    | FORCE_SPD_P1    | <p><b>PORT 1 Force Speed [1:0]. When (force_mode_P1 = 1), these bits are used to control MAC speed of PORT 1.</b></p> <p>00: 10Mbps</p> <p>01: 100Mbps</p> <p>10: 1000Mbps</p> <p>11: reserved</p>                                                                                                                                                                                                                                   |
| 1      | FORCE_DPX_P1    | <p><b>PORT 1 Force duplex. When (force_mode_P1 = 1), this bit is used to control MAC duplex of PORT 1.</b></p> <p>0: Half Duplex</p> <p>1: Full Duplex</p>                                                                                                                                                                                                                                                                           |
| 0      | FORCE_LNK_P1    | <p><b>PORT 1 Force MAC Link Up. When (force_mode_P1 = 1), this bit is used to control link status of PORT 1.</b></p> <p>0: Link Down</p> <p>1: Link Up</p>                                                                                                                                                                                                                                                                           |

| 15023104 |                     | PMEEECR_P1 |    |    |    |    |    |    |                    | Port 1 MAC EEE control register |    |    |    |    |    |                        |  | 111E01E0 |  |
|----------|---------------------|------------|----|----|----|----|----|----|--------------------|---------------------------------|----|----|----|----|----|------------------------|--|----------|--|
| Bit      | 31                  | 30         | 29 | 28 | 27 | 26 | 25 | 24 | 23                 | 22                              | 21 | 20 | 19 | 18 | 17 | 16                     |  |          |  |
| Name     | WAKEUP_TIME_1000_P1 |            |    |    |    |    |    |    | WAKEUP_TIME_100_P1 |                                 |    |    |    |    |    |                        |  |          |  |
| Type     | RW                  |            |    |    |    |    |    |    | RW                 |                                 |    |    |    |    |    |                        |  |          |  |
| Reset    | 0                   | 0          | 0  | 1  | 0  | 0  | 0  | 1  | 0                  | 0                               | 0  | 1  | 1  | 1  | 1  | 0                      |  |          |  |
| Bit      | 15                  | 14         | 13 | 12 | 11 | 10 | 9  | 8  | 7                  | 6                               | 5  | 4  | 3  | 2  | 1  | 0                      |  |          |  |
| Name     | LPI_THRESH_P1       |            |    |    |    |    |    |    |                    |                                 |    |    |    |    |    | LPI_M<br>ODE_E<br>N_P1 |  |          |  |
| Type     | RW                  |            |    |    |    |    |    |    |                    |                                 |    |    |    |    |    | RW                     |  |          |  |
| Reset    | 0                   | 0          | 0  | 0  | 0  | 0  | 0  | 1  | 1                  | 1                               | 1  | 0  |    |    |    | 0                      |  |          |  |

| Bit(s) | Name                | Description                                                                                                                                                                                                                                                                                                                                                                                                 |
|--------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | WAKEUP_TIME_1000_P1 | <p><b>PORT 1 Wake Up Time for 1000Mbps LPI Mode.</b></p> <p>The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup.</p> <p>Time unit: 1 microsecond</p>                                                                                                                                                                                         |
| 23:16  | WAKEUP_TIME_100_P1  | <p><b>PORT 1 Wake Up Time for 100Mbps LPI Mode.</b></p> <p>The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup.</p> <p>Time unit: 1 microsecond</p>                                                                                                                                                                                          |
| 15:4   | LPI_THRESH_P1       | <p><b>PORT 1 LPI Threshold.</b></p> <p>When there is no packet to be transmitted, and the idle time is greater than P1_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.</p>                                                                                                                                                          |
| 0      | LPI_MODE_EN_P1      | <p><b>PORT 1 Enter LPI Mode.</b></p> <p>When there is no packet to be transmitted, and the idle time is greater than P1_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.</p> <p>0: LPI mode depends on the P1_LPI_THRESHOLD.</p> <p>1: Let the system enter the LPI mode immediately and send EEE LPI frame to the link partner.</p> |

**15023108 PMSR\_P1 Port 1 MAC status register 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23           | 22            | 21           | 20           | 19             | 18             | 17             | 16 |
|-------|----|----|----|----|----|----|----|----|--------------|---------------|--------------|--------------|----------------|----------------|----------------|----|
| Name  |    |    |    |    |    |    |    |    |              |               |              |              |                |                |                |    |
| Type  |    |    |    |    |    |    |    |    |              |               |              |              |                |                |                |    |
| Reset |    |    |    |    |    |    |    |    |              |               |              |              |                |                |                |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7            | 6             | 5            | 4            | 3              | 2              | 1              | 0  |
| Name  |    |    |    |    |    |    |    |    | EEE1G_STS_P1 | EEE100_STS_P1 | RX_FC_STS_P1 | TX_FC_STS_P1 | MAC_SPD_STS_P1 | MAC_DPX_STS_P1 | MAC_LNK_STS_P1 |    |
| Type  |    |    |    |    |    |    |    |    | RO           | RO            | RO           | RO           | RO             | RO             | RO             | RO |
| Reset |    |    |    |    |    |    |    |    | 0            | 0             | 0            | 0            | 0              | 0              | 0              | 0  |

| Bit(s) | Name           | Description                                                                                                                                                                                                        |
|--------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7      | EEE1G_STS_P1   | <b>PORT 1 LPI Mode Status For 1000Mbps</b><br><br>0: Not capable of entering EEE Low Power Idle mode for 1000Mbps.<br><br>1: Capable of entering EEE Low Power Idle mode for 1000Mbps.                             |
| 6      | EEE100_STS_P1  | <b>PORT 1 LPI Status Mode For 100Mbps</b><br><br>0: Not capable of entering EEE Low Power Idle mode for 100Mbps.<br><br>1: Capable of entering EEE Low Power Idle mode for 100Mbps.                                |
| 5      | RX_FC_STS_P1   | <b>PORT 1 RX XFC Status. Port 1 Rx flow control status.</b><br><br>0: Disabled<br><br>1: Let the MAC of PORT 1 accept a pause frame when operating in full-duplex mode.                                            |
| 4      | TX_FC_STS_P1   | <b>PORT 1 TX XFC Status. PORT 1 TX flow control status.</b><br><br>0: Disabled<br><br>1: Let the MAC of PORT 1 transmit a pause frame when operating in full-duplex mode with low internal free memory page count. |
| 3:2    | MAC_SPD_STS_P1 | <b>PORT 1 Speed [1:0] Status. Current speed of PORT 1 after PHY links up.</b><br><br>00: 10 Mbps<br><br>01: 100 Mbps<br><br>10: 1000 Mbps<br><br>11: Reserved                                                      |
| 1      | MAC_DPX_STS_P1 | <b>PORT 1 duplex Status. Current duplex mode of PORT 1 after PHY links up.</b><br><br>0: Half Duplex<br><br>1: Full Duplex                                                                                         |
| 0      | MAC_LNK_STS_P1 | <b>Port 1 Link Up Status. Link up status of PORT 1.</b><br><br>0: Link Down                                                                                                                                        |



| Bit(s) | Name | Description |
|--------|------|-------------|
|        |      | 1: Link Up  |

**15023110 PINT\_EN\_P1 Port 1 interrupt enable register 00000000**

| Bit   | 31                 | 30                    | 29                    | 28                  | 27                   | 26                   | 25                  | 24                 | 23 | 22 | 21 | 20 | 19                  | 18                 | 17                  | 16                   |
|-------|--------------------|-----------------------|-----------------------|---------------------|----------------------|----------------------|---------------------|--------------------|----|----|----|----|---------------------|--------------------|---------------------|----------------------|
| Name  |                    |                       |                       |                     |                      |                      |                     |                    |    |    |    |    |                     |                    |                     |                      |
| Type  |                    |                       |                       |                     |                      |                      |                     |                    |    |    |    |    |                     |                    |                     |                      |
| Reset |                    |                       |                       |                     |                      |                      |                     |                    |    |    |    |    |                     |                    |                     |                      |
| Bit   | 15                 | 14                    | 13                    | 12                  | 11                   | 10                   | 9                   | 8                  | 7  | 6  | 5  | 4  | 3                   | 2                  | 1                   | 0                    |
| Name  | TX_TFF_UNDR_INT_EN | TX_MISVLAN_ERR_INT_EN | TX_MISPAGE_ERR_INT_EN | TX_RPAGE_ERR_INT_EN | TX_RPAGE_TOUT_INT_EN | TX_GPAGE_TOUT_INT_EN | TX_RDPB_TOUT_INT_EN | TX_DEQ_TOUT_INT_EN |    |    |    |    | RX_AFFL_TOUT_INT_EN | RX_ARL_TOUT_INT_EN | RX_WRPB_TOUT_INT_EN | RX_GPAGE_TOUT_INT_EN |
| Type  | RW                 | RW                    | RW                    | RW                  | RW                   | RW                   | RW                  | RW                 |    |    |    |    | RW                  | RW                 | RW                  | RW                   |
| Reset | 0                  | 0                     | 0                     | 0                   | 0                    | 0                    | 0                   | 0                  |    |    |    |    | 0                   | 0                  | 0                   | 0                    |

| Bit(s) | Name                  | Description                                                                               |
|--------|-----------------------|-------------------------------------------------------------------------------------------|
| 15     | TX_TFF_UNDR_INT_EN    | <b>TXMAC TXFIFO Under run Interrupt Enable</b><br>0: Disabled<br>1: Enabled               |
| 14     | TX_MISVLAN_ERR_INT_EN | <b>TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable</b><br>0: Disabled<br>1: Enabled |
| 13     | TX_MISPAGE_ERR_INT_EN | <b>TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable</b><br>0: Disabled<br>1: Enabled |
| 12     | TX_RPAGE_ERR_INT_EN   | <b>TX_CTRL Release Page Count Error Interrupt Enable</b><br>0: Disabled<br>1: Enabled     |
| 11     | TX_RPAGE_TOUT_INT_EN  | <b>TX_CTRL Release Page Timeout Interrupt Enable</b><br>0: Disabled<br>1: Enabled         |
| 10     | TX_GPAGE_TOUT_INT_EN  | <b>TX_CTRL Get Page Timeout Interrupt Enable</b><br>0: Disabled<br>1: Enabled             |
| 9      | TX_RDPB_TOUT_INT_EN   | <b>TX_CTRL RD_PB Timeout Interrupt Enable</b><br>0: Disabled<br>1: Enabled                |
| 8      | TX_DEQ_TOUT_INT_EN    | <b>TX_CTRL DEQ Timeout Interrupt Enable</b><br>0: Disabled                                |

| Bit(s) | Name                 | Description                                      |
|--------|----------------------|--------------------------------------------------|
|        |                      | 1: Enabled                                       |
| 3      | RX_AFF_FULL_INT_EN   | <b>RX_CTRL Agent FIFO Full Interrupt Enable</b>  |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |
| 2      | RX_ARL_TOUT_INT_EN   | <b>RX_CTRL ARL Timeout Interrupt Enable</b>      |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |
| 1      | RX_WRPB_TOUT_INT_EN  | <b>RX_CTRL WR_PB Timeout Interrupt Enable</b>    |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |
| 0      | RX_GPAGE_TOUT_INT_EN | <b>RX_CTRL Get Page Timeout Interrupt Enable</b> |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |

**15023114 PINT\_STS\_P1 Port 1 interrupt status register 00000000**

| Bit   | 31              | 30                 | 29                 | 28               | 27                | 26                | 25               | 24              | 23 | 22 | 21 | 20 | 19              | 18              | 17               | 16                |
|-------|-----------------|--------------------|--------------------|------------------|-------------------|-------------------|------------------|-----------------|----|----|----|----|-----------------|-----------------|------------------|-------------------|
| Name  |                 |                    |                    |                  |                   |                   |                  |                 |    |    |    |    |                 |                 |                  |                   |
| Type  |                 |                    |                    |                  |                   |                   |                  |                 |    |    |    |    |                 |                 |                  |                   |
| Reset |                 |                    |                    |                  |                   |                   |                  |                 |    |    |    |    |                 |                 |                  |                   |
| Bit   | 15              | 14                 | 13                 | 12               | 11                | 10                | 9                | 8               | 7  | 6  | 5  | 4  | 3               | 2               | 1                | 0                 |
| Name  | TX_TFF_UNDR_INT | TX_MISVLAN_ERR_INT | TX_MISPAGE_ERR_INT | TX_RPAGE_ERR_INT | TX_RPAGE_TOUT_INT | TX_GPAGE_TOUT_INT | TX_RDPB_TOUT_INT | TX_DEQ_TOUT_INT |    |    |    |    | RX_AFF_FULL_INT | RX_ARL_TOUT_INT | RX_WRPB_TOUT_INT | RX_GPAGE_TOUT_INT |
| Type  | RO              | RO                 | RO                 | RO               | RO                | RO                | RO               | RO              |    |    |    |    | RO              | RO              | RO               | RO                |
| Reset | 0               | 0                  | 0                  | 0                | 0                 | 0                 | 0                | 0               |    |    |    |    | 0               | 0               | 0                | 0                 |

| Bit(s) | Name               | Description                                                                          |
|--------|--------------------|--------------------------------------------------------------------------------------|
| 15     | TX_TFF_UNDR_INT    | <b>TXMAC TXFIFO Under run Interrupt</b><br><br>0: False<br><br>1: True               |
| 14     | TX_MISVLAN_ERR_INT | <b>TX_CTRL PKT INFO VLAN Mismatch Error Interrupt</b><br><br>0: False<br><br>1: True |
| 13     | TX_MISPAGE_ERR_INT | <b>TX_CTRL PKT INFO Page Mismatch Error Interrupt</b><br><br>0: False<br><br>1: True |
| 12     | TX_RPAGE_ERR_INT   | <b>TX_CTRL Release Page Count Error Interrupt</b><br><br>0: False<br><br>1: True     |
| 11     | TX_RPAGE_TOUT_INT  | <b>TX_CTRL Release Page Timeout Interrupt</b><br><br>0: False<br><br>1: True         |
| 10     | TX_GPAGE_TOUT_INT  | <b>TX_CTRL Get Page Timeout Interrupt</b><br><br>0: False<br><br>1: True             |
| 9      | TX_RDPB_TOUT_INT   | <b>TX_CTRL RD_PB Timeout Interrupt</b><br><br>0: False<br><br>1: True                |
| 8      | TX_DEQ_TOUT_INT    | <b>TX_CTRL DEQ Timeout Interrupt</b><br><br>0: False                                 |

| Bit(s) | Name              | Description                               |
|--------|-------------------|-------------------------------------------|
|        |                   | 1: True                                   |
| 3      | RX_AFF_FULL_INT   | <b>RX_CTRL Agent FIFO Full Interrupt</b>  |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |
| 2      | RX_ARL_TOUT_INT   | <b>RX_CTRL ARL Timeout Interrupt</b>      |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |
| 1      | RX_WRPB_TOUT_INT  | <b>RX_CTRL WR_PB Timeout Interrupt</b>    |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |
| 0      | RX_GPAGE_TOUT_INT | <b>RX_CTRL Get Page Timeout Interrupt</b> |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |

15023118      P1\_DBG\_CNT      Port 1 debug count      00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22           | 21 | 20 | 19 | 18         | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|--------------|----|----|----|------------|----|----|
| Name  |    |    |    |    |    |    |    |    |    |              |    |    |    |            |    |    |
| Type  |    |    |    |    |    |    |    |    |    |              |    |    |    |            |    |    |
| Reset |    |    |    |    |    |    |    |    |    |              |    |    |    |            |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6            | 5  | 4  | 3  | 2          | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    | TX_FIFO_URUN |    |    |    | RX_FIFO_OV |    |    |
| Type  |    |    |    |    |    |    |    |    |    | RO           |    |    |    | RO         |    |    |
| Reset |    |    |    |    |    |    |    |    |    | 0            | 0  | 0  |    | 0          | 0  | 0  |

| Bit(s) | Name         | Description                                                                     |
|--------|--------------|---------------------------------------------------------------------------------|
| 6:4    | TX_FIFO_URUN | Underrun count of TX FIFO. The field is increased when TX FIFO underrun occurs. |
| 2:0    | RX_FIFO_OV   | Overflow count of RX FIFO. The field is increased when RX FIFO overflow occurs. |

15023120      P1\_WOL      Port 1 WOL      00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19      | 18      | 17          | 16      |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|---------|---------|-------------|---------|
| Name  | WOL_DBG |    |    |    |    |    |    |    |    |    |    |    |         |         | WOL_INT_STS | WOL_STS |
| Type  | RO      |    |    |    |    |    |    |    |    |    |    |    |         |         | W1C         | RO      |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       | 0       | 0           | 0       |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3       | 2       | 1           | 0       |
| Name  |         |    |    |    |    |    |    |    |    |    |    |    | SNP_PKT | CRC_DIS | WOL_INT_EN  | WOL_EN  |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    | RW      | RW      | RW          | RW      |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    | 0       | 0       | 0           | 0       |

| Bit(s) | Name        | Description                                                                                                                                                                                                |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:18  | WOL_DBG     | <b>Port1 Wake-up On Lan Debug Signals</b>                                                                                                                                                                  |
| 17     | WOL_INT_STS | <b>Port1 Wake-up On Lan Interrupt Status</b>                                                                                                                                                               |
| 16     | WOL_STS     | <b>Port1 Wake-up On Lan Status</b><br><br>If enable WOL_EN, this bit will change from 0 to 1 when GMAC RX state machine enter IDLE state. It indicates GMAC will drop all packets and detect magic packet. |
| 3      | SNP_PKT     | <b>Port1 Wake-up On Lan with snoopy packet</b><br><br>0: Disable<br><br>1: Enable                                                                                                                          |
| 2      | CRC_DIS     | <b>Port1 Wake-up On Lan with CRC Check Disable</b><br><br>0: CRC check enable<br><br>1: CRC check disable                                                                                                  |
| 1      | WOL_INT_EN  | <b>Port1 Wake-up On Lan Interrupt Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                            |
| 0      | WOL_EN      | <b>Port1 Wake-up On Lan Function Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                             |

15023124      P1\_PFC\_STS      Port 1 PFC status      00000000

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|
| Name  |            |    |    |    |    |    |    |    |            |    |    |    |    |    |    |    |
| Type  |            |    |    |    |    |    |    |    |            |    |    |    |    |    |    |    |
| Reset |            |    |    |    |    |    |    |    |            |    |    |    |    |    |    |    |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PFC_STS |    |    |    |    |    |    |    | RX_PFC_STS |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    | RO         |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                           |
|--------|------------|-----------------------------------------------------------------------|
| 15:8   | TX_PFC_STS | Port1 PFC TX pause on status of 8 priorities 1: pause on 0: pause off |
| 7:0    | RX_PFC_STS | Port1 PFC RX pause on status of 8 priorities 1: pause on 0: pause off |



15023130      **P1\_PFC\_RX\_PSON\_CNT\_L**      Port 1 RX PFC pause on counter for low priority      00000000

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q3_RX_PSON_CNT |    |    |    |    |    |    |    | Q2_RX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q1_RX_PSON_CNT |    |    |    |    |    |    |    | Q0_RX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                |
|--------|----------------|--------------------------------------------|
| 31:24  | Q3_RX_PSON_CNT | PFC RX pause on count for port1 priority 3 |
| 23:16  | Q2_RX_PSON_CNT | PFC RX pause on count for port1 priority 2 |
| 15:8   | Q1_RX_PSON_CNT | PFC RX pause on count for port1 priority 1 |
| 7:0    | Q0_RX_PSON_CNT | PFC RX pause on count for port1 priority 0 |

15023134      **P1\_PFC\_RX\_PSON\_CNT\_H**      Port 1 RX PFC pause on counter for high priority      00000000

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q7_RX_PSON_CNT |    |    |    |    |    |    |    | Q6_RX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q5_RX_PSON_CNT |    |    |    |    |    |    |    | Q4_RX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                |
|--------|----------------|--------------------------------------------|
| 31:24  | Q7_RX_PSON_CNT | PFC RX pause on count for port1 priority 7 |
| 23:16  | Q6_RX_PSON_CNT | PFC RX pause on count for port1 priority 6 |
| 15:8   | Q5_RX_PSON_CNT | PFC RX pause on count for port1 priority 5 |
| 7:0    | Q4_RX_PSON_CNT | PFC RX pause on count for port1 priority 4 |

15023138      **P1\_PFC\_RX\_PSOFF\_CNT\_L**      Port 1 RX PFC pause off counter for low priority      00000000

| Bit          | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q3_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q2_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q1_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q0_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                 |
|--------|-----------------|---------------------------------------------|
| 31:24  | Q3_RX_PSOFF_CNT | PFC RX pause off count for port1 priority 3 |
| 23:16  | Q2_RX_PSOFF_CNT | PFC RX pause off count for port1 priority 2 |
| 15:8   | Q1_RX_PSOFF_CNT | PFC RX pause off count for port1 priority 1 |
| 7:0    | Q0_RX_PSOFF_CNT | PFC RX pause off count for port1 priority 0 |

1502313C      **P1\_PFC\_RX\_PSOFF\_CNT\_H**      Port 1 RX PFC pause off counter for high priority      00000000

| Bit          | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q7_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q6_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q5_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q4_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                 |
|--------|-----------------|---------------------------------------------|
| 31:24  | Q7_RX_PSOFF_CNT | PFC RX pause off count for port1 priority 7 |
| 23:16  | Q6_RX_PSOFF_CNT | PFC RX pause off count for port1 priority 6 |
| 15:8   | Q5_RX_PSOFF_CNT | PFC RX pause off count for port1 priority 5 |
| 7:0    | Q4_RX_PSOFF_CNT | PFC RX pause off count for port1 priority 4 |

15023140      **P1\_PFC\_TX\_PSON\_CNT\_L**      Port 1 TX PFC pause on counter for low priority      00000000

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q3_TX_PSON_CNT |    |    |    |    |    |    |    | Q2_TX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q1_TX_PSON_CNT |    |    |    |    |    |    |    | Q0_TX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                |
|--------|----------------|--------------------------------------------|
| 31:24  | Q3_TX_PSON_CNT | PFC TX pause on count for port1 priority 3 |
| 23:16  | Q2_TX_PSON_CNT | PFC TX pause on count for port1 priority 2 |
| 15:8   | Q1_TX_PSON_CNT | PFC TX pause on count for port1 priority 1 |
| 7:0    | Q0_TX_PSON_CNT | PFC TX pause on count for port1 priority 0 |

15023144      **P1\_PFC\_TX\_PSON\_CNT\_H**      Port 1 TX PFC pause on counter for high priority      00000000

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q7_TX_PSON_CNT |    |    |    |    |    |    |    | Q6_TX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q5_TX_PSON_CNT |    |    |    |    |    |    |    | Q4_TX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                |
|--------|----------------|--------------------------------------------|
| 31:24  | Q7_TX_PSON_CNT | PFC TX pause on count for port1 priority 7 |
| 23:16  | Q6_TX_PSON_CNT | PFC TX pause on count for port1 priority 6 |
| 15:8   | Q5_TX_PSON_CNT | PFC TX pause on count for port1 priority 5 |
| 7:0    | Q4_TX_PSON_CNT | PFC TX pause on count for port1 priority 4 |

15023148      **P1\_PFC\_TX\_PSOFF\_CNT\_L**      Port 1 TX PFC pause off counter for low priority      00000000

| Bit          | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q3_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q2_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q1_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q0_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                 |
|--------|-----------------|---------------------------------------------|
| 31:24  | Q3_TX_PSOFF_CNT | PFC TX pause off count for port1 priority 3 |
| 23:16  | Q2_TX_PSOFF_CNT | PFC TX pause off count for port1 priority 2 |
| 15:8   | Q1_TX_PSOFF_CNT | PFC TX pause off count for port1 priority 1 |
| 7:0    | Q0_TX_PSOFF_CNT | PFC TX pause off count for port1 priority 0 |

1502314C      **P1\_PFC\_TX\_PSOFF\_CNT\_H**      Port 1 TX PFC pause off counter for high priority      00000000

| Bit          | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q7_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q6_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q5_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q4_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                 |
|--------|-----------------|---------------------------------------------|
| 31:24  | Q7_TX_PSOFF_CNT | PFC TX pause off count for port1 priority 7 |
| 23:16  | Q6_TX_PSOFF_CNT | PFC TX pause off count for port1 priority 6 |
| 15:8   | Q5_TX_PSOFF_CNT | PFC TX pause off count for port1 priority 5 |
| 7:0    | Q4_TX_PSOFF_CNT | PFC TX pause off count for port1 priority 4 |



**15023200 PMCR\_P2 Port 2 MAC control register 00056130**

| Bit   | 31                | 30                | 29                | 28                  | 27                  | 26                  | 25                  | 24           | 23             | 22             | 21             | 20             | 19           | 18 | 17           | 16           |
|-------|-------------------|-------------------|-------------------|---------------------|---------------------|---------------------|---------------------|--------------|----------------|----------------|----------------|----------------|--------------|----|--------------|--------------|
| Name  | FORCE_MODE_LNK_P2 | FORCE_MODE_SPD_P2 | FORCE_MODE_DPX_P2 | FORCE_MODE_RX_FC_P2 | FORCE_MODE_TX_FC_P2 | FORCE_MODE_EEE10_P2 | FORCE_MODE_EEE1G_P2 |              |                |                |                |                | IPG_CFG_P2   |    | EXT_PHY_P2   | MAC_MODE_P2  |
| Type  | RW                | RW                | RW                | RW                  | RW                  | RW                  | RW                  |              |                |                |                |                | RW           |    | RW           | RW           |
| Reset | 0                 | 0                 | 0                 | 0                   | 0                   | 0                   | 0                   |              |                |                |                |                | 0            | 1  | 0            | 1            |
| Bit   | 15                | 14                | 13                | 12                  | 11                  | 10                  | 9                   | 8            | 7              | 6              | 5              | 4              | 3            | 2  | 1            | 0            |
| Name  |                   | MAC_TX_EN_P2      | MAC_RX_EN_P2      |                     | MAC_PRE_P2          |                     |                     | BACKPR_EN_P2 | FORCE_EEE1G_P2 | FORCE_EEE10_P2 | FORCE_RX_FC_P2 | FORCE_TX_FC_P2 | FORCE_SPD_P2 |    | FORCE_DPX_P2 | FORCE_LNK_P2 |
| Type  |                   | RW                | RW                |                     | RW                  |                     |                     | RW           | RW             | RW             | RW             | RW             | RW           |    | RW           | RW           |
| Reset |                   | 1                 | 1                 |                     | 0                   |                     |                     | 1            | 0              | 0              | 1              | 1              | 0            | 0  | 0            | 0            |

| Bit(s) | Name                 | Description                                                                                                                                                                                                         |
|--------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | FORCE_MODE_LNK_P2    | <b>PORT 2 link status force Mode.</b><br><br>0: Force mode is off. (MAC link status is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC link status is determined by force_link_P2 register) |
| 30     | FORCE_MODE_SPD_P2    | <b>PORT 2 speed force Mode.</b><br><br>0: Force mode is off. (MAC speed is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC speed is determined by force_spd_P2 register)                    |
| 29     | FORCE_MODE_DPX_P2    | <b>PORT 2 duplex force Mode.</b><br><br>0: Force mode is off. (MAC duplex mode is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC duplex mode is determined by force_dpx_P2 register)       |
| 28     | FORCE_MODE_RX_FC_P2  | <b>PORT 2 RX FC force Mode.</b><br><br>0: Force mode is off. (MAC RX FC ability is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC RX FC ability is determined by force_rx_fc_P2 register)  |
| 27     | FORCE_MODE_TX_FC_P2  | <b>PORT 2 TX FC force Mode.</b><br><br>0: Force mode is off. (MAC TX FC ability is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC TX FC ability is determined by force_tx_fc_P2 register)  |
| 26     | FORCE_MODE_EEE100_P2 | <b>PORT 2 100M EEE force Mode.</b><br><br>0: Force mode is off. (MAC 100M EEE ability is determined by PHY auto-polling module)                                                                                     |

| Bit(s) | Name                | Description                                                                                                                                                                                                                                                       |
|--------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25     | FORCE_MODE_EEE1G_P2 | <p>1: Force mode is on. (MAC 100M EEE ability is determined by force_eee100_P2 register)</p> <p><b>PORT 2 1G EEE force Mode.</b></p> <p>0: Force mode is off. (MAC 1G EEE ability is determined by PHY auto-polling module)</p>                                   |
| 19:18  | IPG_CFG_P2          | <p>1: Force mode is on. (MAC 1G EEE ability is determined by force_eee1g_P2 register)</p> <p><b>PORT 2 Inter-Frame+ Gap Shrink</b></p> <p>00: Normal 96-bit IFG</p> <p>01: Transmit 96-bit IFG with short IFG in random behavior</p> <p>10: Shrink 64-bit IFG</p> |
| 17     | EXT_PHY_P2          | <p><b>PORT 2 External PHY. Port 2 connects with external PHY.</b></p> <p>0: PORT 2 DOES NOT connect with external PHY</p> <p>1: PORT 2 connects with external PHY</p>                                                                                             |
| 16     | MAC_MODE_P2         | <p><b>PORT 2 MAC Mode. PORT 2 operates in MAC mode</b></p> <p>0: PORT 2 operates in PHY mode</p> <p>1: PORT 2 operates in MAC mode</p>                                                                                                                            |
| 14     | MAC_TX_EN_P2        | <p><b>Port 2 TX MAC Enable (Note: This bit only has impacts on MAC function, it has no impact on the link status or Queue manager.)</b></p> <p>0: TX MAC function is disabled</p> <p>1: TX MAC function is enabled</p>                                            |
| 13     | MAC_RX_EN_P2        | <p><b>PORT 2 RX MAC Enable (Note: This bit only has impacts on MAC function, it has no impact on the link status or Queue manager.)</b></p> <p>0: RX MAC function is disabled</p> <p>1: RX MAC function is enabled</p>                                            |
| 11     | MAC_PRE_P2          | <p><b>TX short preamble mode</b></p> <p>0: TX short preamble length is disabled</p> <p>1: TX short preamble is enabled.</p>                                                                                                                                       |
| 8      | BACKPR_EN_P2        | <p><b>PORT 2 Backpressure Enable</b></p> <p>0: Disabled</p> <p>1: Enable back pressure mechanism when operating in half-duplex mode with low internal free memory page count.</p>                                                                                 |
| 7      | FORCE_EEE1G_P2      | <p><b>PORT 2 Force LPI Mode For 1000Mbps. When (force_mode_pn = 1), this bit is used to control the 1000Base-T EEE ability of PORT 2.</b></p> <p>0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps.</p>                                 |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                                                            |
|--------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6      | FORCE_EEE100_P2 | <p>1: Have the ability of entering EEE Low Power Idle mode for 100Mbps.</p> <p><b>PORT 2 Force LPI Mode For 100Mbps. When (force_mode_pn = 1), this bit is used to control the 100Base-TX EEE ability of PORT 2.</b></p> <p>0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps.</p>                            |
| 5      | FORCE_RX_FC_P2  | <p>1: Have the ability of entering EEE Low Power Idle mode for 100Mbps.</p> <p><b>PORT 2 Force RX FC. When (force_mode_P2 = 1), this bit is used to control the RX FC ability of PORT 2.</b></p> <p>0: Disabled.</p>                                                                                                                   |
| 4      | FORCE_TX_FC_P2  | <p>1: Let the MAC of PORT 2 accept a pause frame when operating in full-duplex mode.</p> <p><b>PORT 2 Force TX FC. When (force_mode_P2 = 1), this bit is used to control the TX FC ability of PORT 2.</b></p> <p>0: Disabled.</p>                                                                                                      |
| 3:2    | FORCE_SPD_P2    | <p>1: Let the MAC of PORT 2 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.</p> <p><b>PORT 2 Force Speed [1:0]. When (force_mode_P2 = 1), these bits are used to control MAC speed of PORT 2.</b></p> <p>00: 10Mbps</p> <p>01: 100Mbps</p> <p>10: 1000Mbps</p> <p>11: Reserved</p> |
| 1      | FORCE_DPX_P2    | <p><b>PORT 2 Force duplex. When (force_mode_P2 = 1), this bit is used to control the MAC duplex of PORT 2.</b></p> <p>0: Half Duplex</p> <p>1: Full Duplex</p>                                                                                                                                                                         |
| 0      | FORCE_LNK_P2    | <p><b>PORT 2 Force MAC Link Up. When (force_mode_P2 = 1), this bit is used to control the link status of PORT 2.</b></p> <p>0: Link Down</p> <p>1: Link Up</p>                                                                                                                                                                         |

**15023204 PMEEECR\_P2 PORT 2 MAC EEE control register 111E01E0**

| Bit          | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16             |
|--------------|---------------------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|----------------|
| <b>Name</b>  | WAKEUP_TIME_1000_P2 |    |    |    |    |    |    |    | WAKEUP_TIME_100_P2 |    |    |    |    |    |    |                |
| <b>Type</b>  | RW                  |    |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |                |
| <b>Reset</b> | 0                   | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0                  | 0  | 0  | 1  | 1  | 1  | 1  | 0              |
| Bit          | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0              |
| <b>Name</b>  | LPI_THRESH_P2       |    |    |    |    |    |    |    |                    |    |    |    |    |    |    | LPI_MODE_EN_P2 |
| <b>Type</b>  | RW                  |    |    |    |    |    |    |    |                    |    |    |    |    |    |    | RW             |
| <b>Reset</b> | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1                  | 1  | 1  | 0  |    |    |    | 0              |

| Bit(s) | Name                | Description                                                                                                                                                                                                                                                                                                                                                                                          |
|--------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | WAKEUP_TIME_1000_P2 | <b>PORT 2 Wake Up Time for 1000Mbps LPI Mode</b><br><br>The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup.<br><br>Time unit: 1 microsecond                                                                                                                                                                                          |
| 23:16  | WAKEUP_TIME_100_P2  | <b>PORT 2 Wake Up Time for 100Mbps LPI Mode</b><br><br>The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup.<br><br>Time unit: 1 microsecond                                                                                                                                                                                           |
| 15:4   | LPI_THRESH_P2       | <b>PORT 2 LPI Threshold.</b><br><br>When there is no packet to be transmitted, and the idle time is greater than P2_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.                                                                                                                                                          |
| 0      | LPI_MODE_EN_P2      | <b>PORT 2 Enter LPI Mode.</b><br><br>When there is no packet to be transmitted, and the idle time is greater than P2_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.<br><br>0: LPI mode depends on the P2_LPI_THRESHOLD.<br><br>1: Let the system enter the LPI mode immediately and send EEE LPI frame to the link partner. |

|          |         |    |    |                            |    |    |    |    |              |               |              |              |                |    |                |                |  |
|----------|---------|----|----|----------------------------|----|----|----|----|--------------|---------------|--------------|--------------|----------------|----|----------------|----------------|--|
| 15023208 | PMSR_P2 |    |    | Port 2 MAC status register |    |    |    |    |              |               |              |              |                |    |                | 00000000       |  |
| Bit      | 31      | 30 | 29 | 28                         | 27 | 26 | 25 | 24 | 23           | 22            | 21           | 20           | 19             | 18 | 17             | 16             |  |
| Name     |         |    |    |                            |    |    |    |    |              |               |              |              |                |    |                |                |  |
| Type     |         |    |    |                            |    |    |    |    |              |               |              |              |                |    |                |                |  |
| Reset    |         |    |    |                            |    |    |    |    |              |               |              |              |                |    |                |                |  |
| Bit      | 15      | 14 | 13 | 12                         | 11 | 10 | 9  | 8  | 7            | 6             | 5            | 4            | 3              | 2  | 1              | 0              |  |
| Name     |         |    |    |                            |    |    |    |    | EEE1G_STS_P2 | EEE100_STS_P2 | RX_FC_STS_P2 | TX_FC_STS_P2 | MAC_SPD_STS_P2 |    | MAC_DPX_STS_P2 | MAC_LNK_STS_P2 |  |
| Type     |         |    |    |                            |    |    |    |    | RO           | RO            | RO           | RO           | RO             |    | RO             | RO             |  |
| Reset    |         |    |    |                            |    |    |    |    | 0            | 0             | 0            | 0            | 0              | 0  | 0              | 0              |  |

| Bit(s) | Name           | Description                                                                                                                                                                                                              |
|--------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7      | EEE1G_STS_P2   | <b>PORT 2 LPI Mode Status For 1000Mbps</b><br><br>0: Not capable of entering EEE Low Power Idle mode for 1000Mbps<br><br>1: Capable of entering EEE Low Power Idle mode for 1000Mbps                                     |
| 6      | EEE100_STS_P2  | <b>PORT 2 LPI Status Mode For 100Mbps</b><br><br>0: Not capable of entering EEE Low Power Idle mode for 100Mbps<br><br>1: Capable of entering EEE Low Power Idle mode for 100Mbps                                        |
| 5      | RX_FC_STS_P2   | <b>PORT 2 RX XFC Status. Port 2 Rx flow control status</b><br><br>0: Disabled.<br><br>1: Let the MAC of PORT 2 accept a pause frame when operating in full-duplex mode.                                                  |
| 4      | TX_FC_STS_P2   | <b>PORT 2 TX XFC Status</b><br><br>PORT 2 TX flow control status<br><br>0: Disabled.<br><br>1: Let the MAC of PORT 2 transmit a pause frame when operating in full-duplex mode with low internal free memory page count. |
| 3:2    | MAC_SPD_STS_P2 | <b>PORT 2 Speed [1:0] Status</b><br><br>Current speed of PORT 2 after PHY links up<br><br>00: 10 Mbps<br><br>01: 100 Mbps<br><br>10: 1000 Mbps<br><br>11: Reserved                                                       |
| 1      | MAC_DPX_STS_P2 | <b>PORT 2 duplex Status</b><br><br>Current duplex mode of PORT 2 after PHY links up<br><br>0: Half Duplex<br><br>1: Full Duplex                                                                                          |

| Bit(s) | Name           | Description                                                                                        |
|--------|----------------|----------------------------------------------------------------------------------------------------|
| 0      | MAC_LNK_STS_P2 | <b>Port 2 Link Up Status</b><br><br>Link up status of PORT 2<br><br>0: Link Down<br><br>1: Link Up |

**15023210 PINT\_EN\_P2 Port 2 interrupt enable register 00000000**

| Bit   | 31                 | 30                    | 29                    | 28                  | 27                   | 26                   | 25                  | 24                 | 23 | 22 | 21 | 20 | 19                  | 18                 | 17                  | 16                   |
|-------|--------------------|-----------------------|-----------------------|---------------------|----------------------|----------------------|---------------------|--------------------|----|----|----|----|---------------------|--------------------|---------------------|----------------------|
| Name  |                    |                       |                       |                     |                      |                      |                     |                    |    |    |    |    |                     |                    |                     |                      |
| Type  |                    |                       |                       |                     |                      |                      |                     |                    |    |    |    |    |                     |                    |                     |                      |
| Reset |                    |                       |                       |                     |                      |                      |                     |                    |    |    |    |    |                     |                    |                     |                      |
| Bit   | 15                 | 14                    | 13                    | 12                  | 11                   | 10                   | 9                   | 8                  | 7  | 6  | 5  | 4  | 3                   | 2                  | 1                   | 0                    |
| Name  | TX_TFF_UNDR_INT_EN | TX_MISVLAN_ERR_INT_EN | TX_MISPAGE_ERR_INT_EN | TX_RPAGE_ERR_INT_EN | TX_RPAGE_TOUT_INT_EN | TX_GPAGE_TOUT_INT_EN | TX_RDPB_TOUT_INT_EN | TX_DEQ_TOUT_INT_EN |    |    |    |    | RX_AFFL_TOUT_INT_EN | RX_ARL_TOUT_INT_EN | RX_WRPB_TOUT_INT_EN | RX_GPAGE_TOUT_INT_EN |
| Type  | RW                 | RW                    | RW                    | RW                  | RW                   | RW                   | RW                  | RW                 |    |    |    |    | RW                  | RW                 | RW                  | RW                   |
| Reset | 0                  | 0                     | 0                     | 0                   | 0                    | 0                    | 0                   | 0                  |    |    |    |    | 0                   | 0                  | 0                   | 0                    |

| Bit(s) | Name                  | Description                                                                               |
|--------|-----------------------|-------------------------------------------------------------------------------------------|
| 15     | TX_TFF_UNDR_INT_EN    | <b>TXMAC TXFIFO Under run Interrupt Enable</b><br>0: Disabled<br>1: Enabled               |
| 14     | TX_MISVLAN_ERR_INT_EN | <b>TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable</b><br>0: Disabled<br>1: Enabled |
| 13     | TX_MISPAGE_ERR_INT_EN | <b>TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable</b><br>0: Disabled<br>1: Enabled |
| 12     | TX_RPAGE_ERR_INT_EN   | <b>TX_CTRL Release Page Count Error Interrupt Enable</b><br>0: Disabled<br>1: Enabled     |
| 11     | TX_RPAGE_TOUT_INT_EN  | <b>TX_CTRL Release Page Timeout Interrupt Enable</b><br>0: Disabled<br>1: Enabled         |
| 10     | TX_GPAGE_TOUT_INT_EN  | <b>TX_CTRL Get Page Timeout Interrupt Enable</b><br>0: Disabled<br>1: Enabled             |
| 9      | TX_RDPB_TOUT_INT_EN   | <b>TX_CTRL RD_PB Timeout Interrupt Enable</b><br>0: Disabled<br>1: Enabled                |
| 8      | TX_DEQ_TOUT_INT_EN    | <b>TX_CTRL DEQ Timeout Interrupt Enable</b><br>0: Disabled                                |

| Bit(s) | Name                 | Description                                      |
|--------|----------------------|--------------------------------------------------|
|        |                      | 1: Enabled                                       |
| 3      | RX_AFF_FULL_INT_EN   | <b>RX_CTRL Agent FIFO Full Interrupt Enable</b>  |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |
| 2      | RX_ARL_TOUT_INT_EN   | <b>RX_CTRL ARL Timeout Interrupt Enable</b>      |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |
| 1      | RX_WRPB_TOUT_INT_EN  | <b>RX_CTRL WR_PB Timeout Interrupt Enable</b>    |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |
| 0      | RX_GPAGE_TOUT_INT_EN | <b>RX_CTRL Get Page Timeout Interrupt Enable</b> |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |



**15023214 PINT\_STS\_P2 Port 2 interrupt status register 00000000**

| Bit   | 31              | 30                 | 29                 | 28               | 27                | 26                | 25               | 24              | 23 | 22 | 21 | 20 | 19              | 18              | 17               | 16                |
|-------|-----------------|--------------------|--------------------|------------------|-------------------|-------------------|------------------|-----------------|----|----|----|----|-----------------|-----------------|------------------|-------------------|
| Name  |                 |                    |                    |                  |                   |                   |                  |                 |    |    |    |    |                 |                 |                  |                   |
| Type  |                 |                    |                    |                  |                   |                   |                  |                 |    |    |    |    |                 |                 |                  |                   |
| Reset |                 |                    |                    |                  |                   |                   |                  |                 |    |    |    |    |                 |                 |                  |                   |
| Bit   | 15              | 14                 | 13                 | 12               | 11                | 10                | 9                | 8               | 7  | 6  | 5  | 4  | 3               | 2               | 1                | 0                 |
| Name  | TX_TFF_UNDR_INT | TX_MISVLAN_ERR_INT | TX_MISPAGE_ERR_INT | TX_RPAGE_ERR_INT | TX_RPAGE_TOUT_INT | TX_GPAGE_TOUT_INT | TX_RDPB_TOUT_INT | TX_DEQ_TOUT_INT |    |    |    |    | RX_AFF_FULL_INT | RX_ARL_TOUT_INT | RX_WRPB_TOUT_INT | RX_GPAGE_TOUT_INT |
| Type  | RO              | RO                 | RO                 | RO               | RO                | RO                | RO               | RO              |    |    |    |    | RO              | RO              | RO               | RO                |
| Reset | 0               | 0                  | 0                  | 0                | 0                 | 0                 | 0                | 0               |    |    |    |    | 0               | 0               | 0                | 0                 |

| Bit(s) | Name               | Description                                                                          |
|--------|--------------------|--------------------------------------------------------------------------------------|
| 15     | TX_TFF_UNDR_INT    | <b>TXMAC TXFIFO Under run Interrupt</b><br><br>0: False<br><br>1: True               |
| 14     | TX_MISVLAN_ERR_INT | <b>TX_CTRL PKT INFO VLAN Mismatch Error Interrupt</b><br><br>0: False<br><br>1: True |
| 13     | TX_MISPAGE_ERR_INT | <b>TX_CTRL PKT INFO Page Mismatch Error Interrupt</b><br><br>0: False<br><br>1: True |
| 12     | TX_RPAGE_ERR_INT   | <b>TX_CTRL Release Page Count Error Interrupt</b><br><br>0: False<br><br>1: True     |
| 11     | TX_RPAGE_TOUT_INT  | <b>TX_CTRL Release Page Timeout Interrupt</b><br><br>0: False<br><br>1: True         |
| 10     | TX_GPAGE_TOUT_INT  | <b>TX_CTRL Get Page Timeout Interrupt</b><br><br>0: False<br><br>1: True             |
| 9      | TX_RDPB_TOUT_INT   | <b>TX_CTRL RD_PB Timeout Interrupt</b><br><br>0: False<br><br>1: True                |
| 8      | TX_DEQ_TOUT_INT    | <b>TX_CTRL DEQ Timeout Interrupt</b><br><br>0: False                                 |

| Bit(s) | Name              | Description                               |
|--------|-------------------|-------------------------------------------|
|        |                   | 1: True                                   |
| 3      | RX_AFF_FULL_INT   | <b>RX_CTRL Agent FIFO Full Interrupt</b>  |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |
| 2      | RX_ARL_TOUT_INT   | <b>RX_CTRL ARL Timeout Interrupt</b>      |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |
| 1      | RX_WRPB_TOUT_INT  | <b>RX_CTRL WR_PB Timeout Interrupt</b>    |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |
| 0      | RX_GPAGE_TOUT_INT | <b>RX_CTRL Get Page Timeout Interrupt</b> |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |

15023218      P2\_DBG\_CNT      Port 2 debug count      00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22           | 21 | 20 | 19 | 18         | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|--------------|----|----|----|------------|----|----|
| Name  |    |    |    |    |    |    |    |    |    |              |    |    |    |            |    |    |
| Type  |    |    |    |    |    |    |    |    |    |              |    |    |    |            |    |    |
| Reset |    |    |    |    |    |    |    |    |    |              |    |    |    |            |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6            | 5  | 4  | 3  | 2          | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    | TX_FIFO_URUN |    |    |    | RX_FIFO_OV |    |    |
| Type  |    |    |    |    |    |    |    |    |    | RO           |    |    |    | RO         |    |    |
| Reset |    |    |    |    |    |    |    |    |    | 0            | 0  | 0  |    | 0          | 0  | 0  |

| Bit(s) | Name         | Description                                                                     |
|--------|--------------|---------------------------------------------------------------------------------|
| 6:4    | TX_FIFO_URUN | Underrun count of TX FIFO. The field is increased when TX FIFO underrun occurs. |
| 2:0    | RX_FIFO_OV   | Overflow count of RX FIFO. The field is increased when RX FIFO overflow occurs. |

15023220      P2\_WOL      Port 2 WOL      00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19      | 18      | 17          | 16      |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|---------|---------|-------------|---------|
| Name  | WOL_DBG |    |    |    |    |    |    |    |    |    |    |    |         |         | WOL_INT_STS | WOL_STS |
| Type  | RO      |    |    |    |    |    |    |    |    |    |    |    |         |         | W1C         | RO      |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       | 0       | 0           | 0       |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3       | 2       | 1           | 0       |
| Name  |         |    |    |    |    |    |    |    |    |    |    |    | SNP_PKT | CRC_DIS | WOL_INT_EN  | WOL_EN  |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    | RW      | RW      | RW          | RW      |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    | 0       | 0       | 0           | 0       |

| Bit(s) | Name        | Description                                                                                                                                                                                                |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:18  | WOL_DBG     | <b>Port2 Wake-up On Lan Debug Signals</b>                                                                                                                                                                  |
| 17     | WOL_INT_STS | <b>Port2 Wake-up On Lan Interrupt Status</b>                                                                                                                                                               |
| 16     | WOL_STS     | <b>Port2 Wake-up On Lan Status</b><br><br>If enable WOL_EN, this bit will change from 0 to 1 when GMAC RX state machine enter IDLE state. It indicates GMAC will drop all packets and detect magic packet. |
| 3      | SNP_PKT     | <b>Port2 Wake-up On Lan with snoopy packet</b><br><br>0: Disable<br><br>1: Enable                                                                                                                          |
| 2      | CRC_DIS     | <b>Port2 Wake-up On Lan with CRC Check Disable</b><br><br>0: CRC check enable<br><br>1: CRC check disable                                                                                                  |
| 1      | WOL_INT_EN  | <b>Port2 Wake-up On Lan Interrupt Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                            |
| 0      | WOL_EN      | <b>Port2 Wake-up On Lan Function Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                             |

15023224      P2\_PFC\_STS      Port 2 PFC status      00000000

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|
| Name  |            |    |    |    |    |    |    |    |            |    |    |    |    |    |    |    |
| Type  |            |    |    |    |    |    |    |    |            |    |    |    |    |    |    |    |
| Reset |            |    |    |    |    |    |    |    |            |    |    |    |    |    |    |    |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PFC_STS |    |    |    |    |    |    |    | RX_PFC_STS |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    | RO         |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                           |
|--------|------------|-----------------------------------------------------------------------|
| 15:8   | TX_PFC_STS | Port2 PFC TX pause on status of 8 priorities 1: pause on 0: pause off |
| 7:0    | RX_PFC_STS | Port2 PFC RX pause on status of 8 priorities 1: pause on 0: pause off |

15023230      **P2\_PFC\_RX\_PSON\_CNT\_L**      Port 2 RX PFC pause on counter for low priority      00000000

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q3_RX_PSON_CNT |    |    |    |    |    |    |    | Q2_RX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q1_RX_PSON_CNT |    |    |    |    |    |    |    | Q0_RX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                |
|--------|----------------|--------------------------------------------|
| 31:24  | Q3_RX_PSON_CNT | PFC RX pause on count for port2 priority 3 |
| 23:16  | Q2_RX_PSON_CNT | PFC RX pause on count for port2 priority 2 |
| 15:8   | Q1_RX_PSON_CNT | PFC RX pause on count for port2 priority 1 |
| 7:0    | Q0_RX_PSON_CNT | PFC RX pause on count for port2 priority 0 |

15023234      **P2\_PFC\_RX\_PSON\_CNT\_H**      Port 2 RX PFC pause on counter for high priority      00000000

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q7_RX_PSON_CNT |    |    |    |    |    |    |    | Q6_RX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q5_RX_PSON_CNT |    |    |    |    |    |    |    | Q4_RX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                |
|--------|----------------|--------------------------------------------|
| 31:24  | Q7_RX_PSON_CNT | PFC RX pause on count for port2 priority 7 |
| 23:16  | Q6_RX_PSON_CNT | PFC RX pause on count for port2 priority 6 |
| 15:8   | Q5_RX_PSON_CNT | PFC RX pause on count for port2 priority 5 |
| 7:0    | Q4_RX_PSON_CNT | PFC RX pause on count for port2 priority 4 |

15023238      **P2\_PFC\_RX\_PSOFF\_CNT\_L**      Port 2 RX PFC pause off counter for low priority      00000000

| Bit          | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q3_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q2_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q1_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q0_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                 |
|--------|-----------------|---------------------------------------------|
| 31:24  | Q3_RX_PSOFF_CNT | PFC RX pause off count for port2 priority 3 |
| 23:16  | Q2_RX_PSOFF_CNT | PFC RX pause off count for port2 priority 2 |
| 15:8   | Q1_RX_PSOFF_CNT | PFC RX pause off count for port2 priority 1 |
| 7:0    | Q0_RX_PSOFF_CNT | PFC RX pause off count for port2 priority 0 |



1502323C      P2\_PFC\_RX\_PSOFF\_CNT\_H      Port 2 RX PFC pause off counter for high priority      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | Q7_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q6_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q4_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                 |
|--------|-----------------|---------------------------------------------|
| 31:24  | Q7_RX_PSOFF_CNT | PFC RX pause off count for port2 priority 7 |
| 23:16  | Q6_RX_PSOFF_CNT | PFC RX pause off count for port2 priority 6 |
| 15:8   | Q5_RX_PSOFF_CNT | PFC RX pause off count for port2 priority 5 |
| 7:0    | Q4_RX_PSOFF_CNT | PFC RX pause off count for port2 priority 4 |

15023240      **P2\_PFC\_TX\_PSON\_CNT\_L**      Port 2 TX PFC pause on counter for low priority      00000000

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  | Q3_TX_PSON_CNT |    |    |    |    |    |    |    | Q2_TX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q1_TX_PSON_CNT |    |    |    |    |    |    |    | Q0_TX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                |
|--------|----------------|--------------------------------------------|
| 31:24  | Q3_TX_PSON_CNT | PFC TX pause on count for port2 priority 3 |
| 23:16  | Q2_TX_PSON_CNT | PFC TX pause on count for port2 priority 2 |
| 15:8   | Q1_TX_PSON_CNT | PFC TX pause on count for port2 priority 1 |
| 7:0    | Q0_TX_PSON_CNT | PFC TX pause on count for port2 priority 0 |

15023244      **P2\_PFC\_TX\_PSON\_CNT\_H**      Port 2 TX PFC pause on counter for high priority      00000000

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  | Q7_TX_PSON_CNT |    |    |    |    |    |    |    | Q6_TX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_TX_PSON_CNT |    |    |    |    |    |    |    | Q4_TX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                |
|--------|----------------|--------------------------------------------|
| 31:24  | Q7_TX_PSON_CNT | PFC TX pause on count for port2 priority 7 |
| 23:16  | Q6_TX_PSON_CNT | PFC TX pause on count for port2 priority 6 |
| 15:8   | Q5_TX_PSON_CNT | PFC TX pause on count for port2 priority 5 |
| 7:0    | Q4_TX_PSON_CNT | PFC TX pause on count for port2 priority 4 |

15023248      **P2\_PFC\_TX\_PSOFF\_CNT\_L**      Port 2 TX PFC pause off counter for low priority      00000000

| Bit          | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q3_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q2_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q1_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q0_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                 |
|--------|-----------------|---------------------------------------------|
| 31:24  | Q3_TX_PSOFF_CNT | PFC TX pause off count for port2 priority 3 |
| 23:16  | Q2_TX_PSOFF_CNT | PFC TX pause off count for port2 priority 2 |
| 15:8   | Q1_TX_PSOFF_CNT | PFC TX pause off count for port2 priority 1 |
| 7:0    | Q0_TX_PSOFF_CNT | PFC TX pause off count for port2 priority 0 |

1502324C      **P2\_PFC\_TX\_PSOFF\_CNT\_H**      Port 2 TX PFC pause off counter for high priority      00000000

| Bit          | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q7_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q6_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q5_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q4_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                 |
|--------|-----------------|---------------------------------------------|
| 31:24  | Q7_TX_PSOFF_CNT | PFC TX pause off count for port2 priority 7 |
| 23:16  | Q6_TX_PSOFF_CNT | PFC TX pause off count for port2 priority 6 |
| 15:8   | Q5_TX_PSOFF_CNT | PFC TX pause off count for port2 priority 5 |
| 7:0    | Q4_TX_PSOFF_CNT | PFC TX pause off count for port2 priority 4 |

**15023300 PMCR\_P3 Port 3 MAC control register 00056330**

| Bit   | 31                | 30                | 29                | 28                  | 27                  | 26                  | 25                  | 24           | 23             | 22             | 21             | 20             | 19           | 18 | 17           | 16           |
|-------|-------------------|-------------------|-------------------|---------------------|---------------------|---------------------|---------------------|--------------|----------------|----------------|----------------|----------------|--------------|----|--------------|--------------|
| Name  | FORCE_MODE_LNK_P3 | FORCE_MODE_SPD_P3 | FORCE_MODE_DPX_P3 | FORCE_MODE_RX_FC_P3 | FORCE_MODE_TX_FC_P3 | FORCE_MODE_EEE10_P3 | FORCE_MODE_EEE1G_P3 |              |                |                |                |                | IPG_CFG_P3   |    | EXT_PHY_P3   | MAC_MODE_P3  |
| Type  | RW                | RW                | RW                | RW                  | RW                  | RW                  | RW                  |              |                |                |                |                | RW           |    | RW           | RW           |
| Reset | 0                 | 0                 | 0                 | 0                   | 0                   | 0                   | 0                   |              |                |                |                |                | 0            | 1  | 0            | 1            |
| Bit   | 15                | 14                | 13                | 12                  | 11                  | 10                  | 9                   | 8            | 7              | 6              | 5              | 4              | 3            | 2  | 1            | 0            |
| Name  |                   | MAC_TX_EN_P3      | MAC_RX_EN_P3      |                     | MAC_PRE_P3          |                     | BKOFF_EN_P3         | BACKPR_EN_P3 | FORCE_EEE1G_P3 | FORCE_EEE10_P3 | FORCE_RX_FC_P3 | FORCE_TX_FC_P3 | FORCE_SPD_P3 |    | FORCE_DPX_P3 | FORCE_LNK_P3 |
| Type  |                   | RW                | RW                |                     | RW                  |                     | RW                  | RW           | RW             | RW             | RW             | RW             | RW           |    | RW           | RW           |
| Reset |                   | 1                 | 1                 |                     | 0                   |                     | 1                   | 1            | 0              | 0              | 1              | 1              | 0            | 0  | 0            | 0            |

| Bit(s) | Name                 | Description                                                                                                                                                                                                         |
|--------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | FORCE_MODE_LNK_P3    | <b>PORT 3 link status force Mode.</b><br><br>0: Force mode is off. (MAC link status is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC link status is determined by force_link_P3 register) |
| 30     | FORCE_MODE_SPD_P3    | <b>PORT 3 speed force Mode.</b><br><br>0: Force mode is off. (MAC speed is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC speed is determined by force_spd_P3 register)                    |
| 29     | FORCE_MODE_DPX_P3    | <b>PORT 3 duplex force Mode.</b><br><br>0: Force mode is off. (MAC duplex mode is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC duplex mode is determined by force_dpx_P3 register)       |
| 28     | FORCE_MODE_RX_FC_P3  | <b>PORT 3 RX FC force Mode.</b><br><br>0: Force mode is off. (MAC RX FC ability is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC RX FC ability is determined by force_rx_fc_P3 register)  |
| 27     | FORCE_MODE_TX_FC_P3  | <b>PORT 3 TX FC force Mode.</b><br><br>0: Force mode is off. (MAC TX FC ability is determined by PHY auto-polling module)<br><br>1: Force mode is on. (MAC TX FC ability is determined by force_tx_fc_P3 register)  |
| 26     | FORCE_MODE_EEE100_P3 | <b>PORT 3 100M EEE force Mode.</b><br><br>0: Force mode is off. (MAC 100M EEE ability is determined by PHY auto-polling module)                                                                                     |

| Bit(s) | Name                | Description                                                                                                                                                                                                                                                                                                               |
|--------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25     | FORCE_MODE_EEE1G_P3 | <p>1: Force mode is on. (MAC 100M EEE ability is determined by force_eee100_P3 register)</p> <p><b>PORT 3 1G EEE force Mode.</b></p> <p>0: Force mode is off. (MAC 1G EEE ability is determined by PHY auto-polling module)</p> <p>1: Force mode is on. (MAC 1G EEE ability is determined by force_eee1g_P3 register)</p> |
| 19:18  | IPG_CFG_P3          | <p><b>PORT 3 Inter-Frame+ Gap Shrink</b></p> <p>00: Normal 96-bit IFG</p> <p>01: Transmit 96-bit IFG with short IFG in random behavior</p> <p>10: Shrink 64-bit IFG</p>                                                                                                                                                   |
| 17     | EXT_PHY_P3          | <p><b>PORT 3 External PHY</b></p> <p>Port 3 connects with external PHY.</p> <p>0: PORT 3 DOES NOT connect with external PHY</p> <p>1: PORT 3 connects with external PHY</p>                                                                                                                                               |
| 16     | MAC_MODE_P3         | <p><b>PORT 3 MAC Mode</b></p> <p>PORT 3 operates in MAC mode.</p> <p>0: PORT 3 operates in PHY mode</p> <p>1: PORT 3 operates in MAC mode</p>                                                                                                                                                                             |
| 14     | MAC_TX_EN_P3        | <p><b>Port 3 TX MAC Enable (Note: This bit only has impact on MAC function, it has no impact on the link status or Queue manager.)</b></p> <p>0: TX MAC function is disabled</p> <p>1: TX MAC function is enabled</p>                                                                                                     |
| 13     | MAC_RX_EN_P3        | <p><b>PORT 3 RX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)</b></p> <p>0: RX MAC function is disabled</p> <p>1: RX MAC function is enabled</p>                                                                                                 |
| 11     | MAC_PRE_P3          | <p><b>TX short preamble mode</b></p> <p>0: TX short preamble length is disabled</p> <p>1: TX short preamble is enabled.</p>                                                                                                                                                                                               |
| 9      | BKOFF_EN_P3         | <p><b>PORT 3 Backoff Enable</b></p> <p>0: Disabled</p> <p>1: Let the MAC of PORT 3 to follow the back-off mechanism when collision happens.</p>                                                                                                                                                                           |
| 8      | BACKPR_EN_P3        | <p><b>PORT 3 Backpressure Enable</b></p>                                                                                                                                                                                                                                                                                  |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                                   |
|--------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                 | 0: Disabled                                                                                                                                                                                                                                                                                                   |
|        |                 | 1: Enable the back pressure mechanism when operating in half-duplex mode with low internal free memory page count .                                                                                                                                                                                           |
| 7      | FORCE_EEE1G_P3  | <b>PORT 3 Force LPI Mode For 1000Mbps</b><br><br>When (force_mode_P3 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 3.<br><br>0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps.<br><br>1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps. |
| 6      | FORCE_EEE100_P3 | <b>PORT 3 Force LPI Mode For 100Mbps</b><br><br>When (force_mode_P3 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 3.<br><br>0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps.<br><br>1: Have the ability of entering EEE Low Power Idle mode for 100Mbps.    |
| 5      | FORCE_RX_FC_P3  | <b>PORT 3 Force RX FC</b><br><br>When (force_mode_P3 = 1), this bit is used to control the RX FC ability of PORT 3.<br><br>0: Disabled.<br><br>1: Let the MAC of PORT 3 accept a pause frame when operating in full-duplex mode.                                                                              |
| 4      | FORCE_TX_FC_P3  | <b>PORT 3 Force TX FC</b><br><br>When (force_mode_P3 = 1), this bit is used to control the TX FC ability of PORT 3.<br><br>0: Disabled.<br><br>1: Let the MAC of PORT 3 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.                                   |
| 3:2    | FORCE_SPD_P3    | <b>PORT 3 Force Speed [1:0]</b><br><br>When (force_mode_P3 = 1), these bits are used to control the MAC speed of PORT 3.<br><br>00: 10Mbps<br><br>01: 100Mbps<br><br>10: 1000Mbps<br><br>11: Reserved                                                                                                         |
| 1      | FORCE_DPX_P3    | <b>PORT 3 Force duplex.</b><br><br>When (force_mode_P3 = 1), this bit is used to control the MAC duplex of PORT 3.                                                                                                                                                                                            |



| Bit(s) | Name         | Description                                                                                                                                                   |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 0: Half Duplex                                                                                                                                                |
|        |              | 1: Full Duplex                                                                                                                                                |
| 0      | FORCE_LNK_P3 | <b>PORT 3 Force MAC Link Up</b><br><br>When (force_mode_P3 = 1), this bit is used to control the link status of PORT 3.<br><br>0: Link Down<br><br>1: Link Up |

**15023304 PMEEECR\_P3 Port 3 MAC EEE control register 111E01E0**

| Bit          | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16                     |
|--------------|---------------------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|------------------------|
| <b>Name</b>  | WAKEUP_TIME_1000_P3 |    |    |    |    |    |    |    | WAKEUP_TIME_100_P3 |    |    |    |    |    |    |                        |
| <b>Type</b>  | RW                  |    |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |                        |
| <b>Reset</b> | 0                   | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0                  | 0  | 0  | 1  | 1  | 1  | 1  | 0                      |
| Bit          | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0                      |
| <b>Name</b>  | LPI_THRESH_P3       |    |    |    |    |    |    |    |                    |    |    |    |    |    |    | LPI_M<br>ODE_E<br>N_P3 |
| <b>Type</b>  | RW                  |    |    |    |    |    |    |    |                    |    |    |    |    |    |    | RW                     |
| <b>Reset</b> | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1                  | 1  | 1  | 0  |    |    |    | 0                      |

| Bit(s) | Name                | Description                                                                                                                                                                                                                                                                                                                                                                                      |
|--------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | WAKEUP_TIME_1000_P3 | <b>PORT 3 Wake Up Time for 1000Mbps LPI Mode</b><br><br>The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup.<br><br>Time unit: 1 microsecond                                                                                                                                                                                      |
| 23:16  | WAKEUP_TIME_100_P3  | <b>PORT 3 Wake Up Time for 100Mbps LPI Mode.</b><br><br>The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup.<br><br>Time unit: 1 microsecond                                                                                                                                                                                      |
| 15:4   | LPI_THRESH_P3       | <b>PORT 3 LPI Threshold</b><br><br>When there is no packet to be transmitted, and the idle time is greater than P3_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.                                                                                                                                                       |
| 0      | LPI_MODE_EN_P3      | <b>PORT 3 Enter LPI Mode.</b><br><br>When there is no packet to be transmitted, and the idle time is greater than P3_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.<br><br>0: LPI mode depends on the P3_LPI_THRESHOLD.<br><br>1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner. |

**15023308 PMSR\_P3 Port 3 MAC status register 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23           | 22            | 21           | 20           | 19             | 18             | 17             | 16 |
|-------|----|----|----|----|----|----|----|----|--------------|---------------|--------------|--------------|----------------|----------------|----------------|----|
| Name  |    |    |    |    |    |    |    |    |              |               |              |              |                |                |                |    |
| Type  |    |    |    |    |    |    |    |    |              |               |              |              |                |                |                |    |
| Reset |    |    |    |    |    |    |    |    |              |               |              |              |                |                |                |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7            | 6             | 5            | 4            | 3              | 2              | 1              | 0  |
| Name  |    |    |    |    |    |    |    |    | EEE1G_STS_P3 | EEE100_STS_P3 | RX_FC_STS_P3 | TX_FC_STS_P3 | MAC_SPD_STS_P3 | MAC_DPX_STS_P3 | MAC_LNK_STS_P3 |    |
| Type  |    |    |    |    |    |    |    |    | RO           | RO            | RO           | RO           | RO             | RO             | RO             | RO |
| Reset |    |    |    |    |    |    |    |    | 0            | 0             | 0            | 0            | 0              | 0              | 0              | 0  |

| Bit(s) | Name           | Description                                                                                                                                                                                                              |
|--------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7      | EEE1G_STS_P3   | <b>PORT 3 LPI Mode Status For 1000Mbps</b><br><br>0: Not capable of entering EEE Low Power Idle mode for 1000Mbps<br><br>1: Capable of entering EEE Low Power Idle mode for 1000Mbps                                     |
| 6      | EEE100_STS_P3  | <b>PORT 3 LPI Status Mode For 100Mbps</b><br><br>0: Not capable of entering EEE Low Power Idle mode for 100Mbps<br><br>1: Capable of entering EEE Low Power Idle mode for 100Mbps                                        |
| 5      | RX_FC_STS_P3   | <b>PORT 3 RX XFC Status</b><br><br>Port 3 Rx flow control status<br><br>0: Disabled.<br><br>1: Let the MAC of PORT 3 accept a pause frame when operating in full-duplex mode.                                            |
| 4      | TX_FC_STS_P3   | <b>PORT 3 TX XFC Status</b><br><br>PORT 3 TX flow control status<br><br>0: Disabled.<br><br>1: Let the MAC of PORT 3 transmit a pause frame when operating in full-duplex mode with low internal free memory page count. |
| 3:2    | MAC_SPD_STS_P3 | <b>PORT 3 Speed [1:0] Status</b><br><br>Current speed of PORT 3 after PHY links up<br><br>00: 10 Mbps<br><br>01: 100 Mbps<br><br>10: 1000 Mbps<br><br>11: Reserved                                                       |
| 1      | MAC_DPX_STS_P3 | <b>PORT 3 duplex Status</b><br><br>Current duplex mode of port 3 after PHY links up<br><br>0: Half Duplex                                                                                                                |

| Bit(s) | Name           | Description                                                                            |
|--------|----------------|----------------------------------------------------------------------------------------|
|        |                | 1: Full Duplex                                                                         |
| 0      | MAC_LNK_STS_P3 | <b>Port 3 Link Up Status</b><br>Link up status of PORT 3<br>0: Link Down<br>1: Link Up |

**15023310 PINT\_EN\_P3 Port 3 interrupt enable register 00000000**

| Bit   | 31                 | 30                    | 29                    | 28                  | 27                   | 26                   | 25                  | 24                 | 23 | 22 | 21 | 20 | 19                  | 18                  | 17                   | 16 |
|-------|--------------------|-----------------------|-----------------------|---------------------|----------------------|----------------------|---------------------|--------------------|----|----|----|----|---------------------|---------------------|----------------------|----|
| Name  |                    |                       |                       |                     |                      |                      |                     |                    |    |    |    |    |                     |                     |                      |    |
| Type  |                    |                       |                       |                     |                      |                      |                     |                    |    |    |    |    |                     |                     |                      |    |
| Reset |                    |                       |                       |                     |                      |                      |                     |                    |    |    |    |    |                     |                     |                      |    |
| Bit   | 15                 | 14                    | 13                    | 12                  | 11                   | 10                   | 9                   | 8                  | 7  | 6  | 5  | 4  | 3                   | 2                   | 1                    | 0  |
| Name  | TX_TFF_UNDR_INT_EN | TX_MISVLAN_ERR_INT_EN | TX_MISPAGE_ERR_INT_EN | TX_RPAGE_ERR_INT_EN | TX_RPAGE_TOUT_INT_EN | TX_GPAGE_TOUT_INT_EN | TX_RDPB_TOUT_INT_EN | TX_DEQ_TOUT_INT_EN |    |    |    |    | RX_AFFL_TOUT_INT_EN | RX_WRPB_TOUT_INT_EN | RX_GPAGE_TOUT_INT_EN |    |
| Type  | RW                 | RW                    | RW                    | RW                  | RW                   | RW                   | RW                  | RW                 |    |    |    |    | RW                  | RW                  | RW                   | RW |
| Reset | 0                  | 0                     | 0                     | 0                   | 0                    | 0                    | 0                   | 0                  |    |    |    |    | 0                   | 0                   | 0                    | 0  |

| Bit(s) | Name                  | Description                                                                               |
|--------|-----------------------|-------------------------------------------------------------------------------------------|
| 15     | TX_TFF_UNDR_INT_EN    | <b>TXMAC TXFIFO Under run Interrupt Enable</b><br>0: Disabled<br>1: Enabled               |
| 14     | TX_MISVLAN_ERR_INT_EN | <b>TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable</b><br>0: Disabled<br>1: Enabled |
| 13     | TX_MISPAGE_ERR_INT_EN | <b>TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable</b><br>0: Disabled<br>1: Enabled |
| 12     | TX_RPAGE_ERR_INT_EN   | <b>TX_CTRL Release Page Count Error Interrupt Enable</b><br>0: Disabled<br>1: Enabled     |
| 11     | TX_RPAGE_TOUT_INT_EN  | <b>TX_CTRL Release Page Timeout Interrupt Enable</b><br>0: Disabled<br>1: Enabled         |
| 10     | TX_GPAGE_TOUT_INT_EN  | <b>TX_CTRL Get Page Timeout Interrupt Enable</b><br>0: Disabled<br>1: Enabled             |
| 9      | TX_RDPB_TOUT_INT_EN   | <b>TX_CTRL RD_PB Timeout Interrupt Enable</b><br>0: Disabled<br>1: Enabled                |
| 8      | TX_DEQ_TOUT_INT_EN    | <b>TX_CTRL DEQ Timeout Interrupt Enable</b><br>0: Disabled                                |

| Bit(s) | Name                 | Description                                      |
|--------|----------------------|--------------------------------------------------|
|        |                      | 1: Enabled                                       |
| 3      | RX_AFF_FULL_INT_EN   | <b>RX_CTRL Agent FIFO Full Interrupt Enable</b>  |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |
| 2      | RX_ARL_TOUT_INT_EN   | <b>RX_CTRL ARL Timeout Interrupt Enable</b>      |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |
| 1      | RX_WRPB_TOUT_INT_EN  | <b>RX_CTRL WR_PB Timeout Interrupt Enable</b>    |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |
| 0      | RX_GPAGE_TOUT_INT_EN | <b>RX_CTRL Get Page Timeout Interrupt Enable</b> |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |

**15023314 PINT\_STS\_P3 Port 3 interrupt status register 00000000**

| Bit   | 31              | 30                 | 29                 | 28               | 27                | 26                | 25               | 24              | 23 | 22 | 21 | 20 | 19              | 18              | 17               | 16                |
|-------|-----------------|--------------------|--------------------|------------------|-------------------|-------------------|------------------|-----------------|----|----|----|----|-----------------|-----------------|------------------|-------------------|
| Name  |                 |                    |                    |                  |                   |                   |                  |                 |    |    |    |    |                 |                 |                  |                   |
| Type  |                 |                    |                    |                  |                   |                   |                  |                 |    |    |    |    |                 |                 |                  |                   |
| Reset |                 |                    |                    |                  |                   |                   |                  |                 |    |    |    |    |                 |                 |                  |                   |
| Bit   | 15              | 14                 | 13                 | 12               | 11                | 10                | 9                | 8               | 7  | 6  | 5  | 4  | 3               | 2               | 1                | 0                 |
| Name  | TX_TFF_UNDR_INT | TX_MISVLAN_ERR_INT | TX_MISPAGE_ERR_INT | TX_RPAGE_ERR_INT | TX_RPAGE_TOUT_INT | TX_GPAGE_TOUT_INT | TX_RDPB_TOUT_INT | TX_DEQ_TOUT_INT |    |    |    |    | RX_AFF_FULL_INT | RX_ARL_TOUT_INT | RX_WRPB_TOUT_INT | RX_GPAGE_TOUT_INT |
| Type  | RO              | RO                 | RO                 | RO               | RO                | RO                | RO               | RO              |    |    |    |    | RO              | RO              | RO               | RO                |
| Reset | 0               | 0                  | 0                  | 0                | 0                 | 0                 | 0                | 0               |    |    |    |    | 0               | 0               | 0                | 0                 |

| Bit(s) | Name               | Description                                                                          |
|--------|--------------------|--------------------------------------------------------------------------------------|
| 15     | TX_TFF_UNDR_INT    | <b>TXMAC TXFIFO Under run Interrupt</b><br><br>0: False<br><br>1: True               |
| 14     | TX_MISVLAN_ERR_INT | <b>TX_CTRL PKT INFO VLAN Mismatch Error Interrupt</b><br><br>0: False<br><br>1: True |
| 13     | TX_MISPAGE_ERR_INT | <b>TX_CTRL PKT INFO Page Mismatch Error Interrupt</b><br><br>0: False<br><br>1: True |
| 12     | TX_RPAGE_ERR_INT   | <b>TX_CTRL Release Page Count Error Interrupt</b><br><br>0: False<br><br>1: True     |
| 11     | TX_RPAGE_TOUT_INT  | <b>TX_CTRL Release Page Timeout Interrupt</b><br><br>0: False<br><br>1: True         |
| 10     | TX_GPAGE_TOUT_INT  | <b>TX_CTRL Get Page Timeout Interrupt</b><br><br>0: False<br><br>1: True             |
| 9      | TX_RDPB_TOUT_INT   | <b>TX_CTRL RD_PB Timeout Interrupt</b><br><br>0: False<br><br>1: True                |
| 8      | TX_DEQ_TOUT_INT    | <b>TX_CTRL DEQ Timeout Interrupt</b><br><br>0: False                                 |

| Bit(s) | Name              | Description                               |
|--------|-------------------|-------------------------------------------|
|        |                   | 1: True                                   |
| 3      | RX_AFF_FULL_INT   | <b>RX_CTRL Agent FIFO Full Interrupt</b>  |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |
| 2      | RX_ARL_TOUT_INT   | <b>RX_CTRL ARL Timeout Interrupt</b>      |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |
| 1      | RX_WRPB_TOUT_INT  | <b>RX_CTRL WR_PB Timeout Interrupt</b>    |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |
| 0      | RX_GPAGE_TOUT_INT | <b>RX_CTRL Get Page Timeout Interrupt</b> |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |



15023318      P3\_DBG\_CNT      Port 3 debug count      00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22           | 21 | 20 | 19 | 18         | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|--------------|----|----|----|------------|----|----|
| Name  |    |    |    |    |    |    |    |    |    |              |    |    |    |            |    |    |
| Type  |    |    |    |    |    |    |    |    |    |              |    |    |    |            |    |    |
| Reset |    |    |    |    |    |    |    |    |    |              |    |    |    |            |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6            | 5  | 4  | 3  | 2          | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    | TX_FIFO_URUN |    |    |    | RX_FIFO_OV |    |    |
| Type  |    |    |    |    |    |    |    |    |    | RO           |    |    |    | RO         |    |    |
| Reset |    |    |    |    |    |    |    |    |    | 0            | 0  | 0  |    | 0          | 0  | 0  |

| Bit(s) | Name         | Description                                                                                  |
|--------|--------------|----------------------------------------------------------------------------------------------|
| 6:4    | TX_FIFO_URUN | <b>Underrun count of TX FIFO</b><br><br>The field is increased when TX FIFO underrun occurs. |
| 2:0    | RX_FIFO_OV   | <b>Overflow count of RX FIFO</b><br><br>The field is increased when RX FIFO overflow occurs. |

15023320      P3\_WOL      Port 3 WOL      00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19      | 18      | 17          | 16      |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|---------|---------|-------------|---------|
| Name  | WOL_DBG |    |    |    |    |    |    |    |    |    |    |    |         |         | WOL_INT_STS | WOL_STS |
| Type  | RO      |    |    |    |    |    |    |    |    |    |    |    |         |         | W1C         | RO      |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       | 0       | 0           | 0       |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3       | 2       | 1           | 0       |
| Name  |         |    |    |    |    |    |    |    |    |    |    |    | SNP_PKT | CRC_DIS | WOL_INT_EN  | WOL_EN  |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    | RW      | RW      | RW          | RW      |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    | 0       | 0       | 0           | 0       |

| Bit(s) | Name        | Description                                                                                                                                                                                                |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:18  | WOL_DBG     | <b>Port3 Wake-up On Lan Debug Signals</b>                                                                                                                                                                  |
| 17     | WOL_INT_STS | <b>Port3 Wake-up On Lan Interrupt Status</b>                                                                                                                                                               |
| 16     | WOL_STS     | <b>Port3 Wake-up On Lan Status</b><br><br>If enable WOL_EN, this bit will change from 0 to 1 when GMAC RX state machine enter IDLE state. It indicates GMAC will drop all packets and detect magic packet. |
| 3      | SNP_PKT     | <b>Port3 Wake-up On Lan with snoopy packet</b><br><br>0: Disable<br><br>1: Enable                                                                                                                          |
| 2      | CRC_DIS     | <b>Port3 Wake-up On Lan with CRC Check Disable</b><br><br>0: CRC check enable<br><br>1: CRC check disable                                                                                                  |
| 1      | WOL_INT_EN  | <b>Port3 Wake-up On Lan Interrupt Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                            |
| 0      | WOL_EN      | <b>Port3 Wake-up On Lan Function Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                             |

15023324      **P3\_PFC\_STS**      Port 3 PFC status      00000000

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|
| Name  |            |    |    |    |    |    |    |    |            |    |    |    |    |    |    |    |
| Type  |            |    |    |    |    |    |    |    |            |    |    |    |    |    |    |    |
| Reset |            |    |    |    |    |    |    |    |            |    |    |    |    |    |    |    |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PFC_STS |    |    |    |    |    |    |    | RX_PFC_STS |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    | RO         |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                           |
|--------|------------|-----------------------------------------------------------------------|
| 15:8   | TX_PFC_STS | Port3 PFC TX pause on status of 8 priorities 1: pause on 0: pause off |
| 7:0    | RX_PFC_STS | Port3 PFC RX pause on status of 8 priorities 1: pause on 0: pause off |

15023330      **P3\_PFC\_RX\_PSON\_CNT\_L**      Port 3 RX PFC pause on counter for low priority      00000000

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  | Q3_RX_PSON_CNT |    |    |    |    |    |    |    | Q2_RX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q1_RX_PSON_CNT |    |    |    |    |    |    |    | Q0_RX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                |
|--------|----------------|--------------------------------------------|
| 31:24  | Q3_RX_PSON_CNT | PFC RX pause on count for port3 priority 3 |
| 23:16  | Q2_RX_PSON_CNT | PFC RX pause on count for port3 priority 2 |
| 15:8   | Q1_RX_PSON_CNT | PFC RX pause on count for port3 priority 1 |
| 7:0    | Q0_RX_PSON_CNT | PFC RX pause on count for port3 priority 0 |

15023334      **P3\_PFC\_RX\_PSON\_CNT\_H**      Port 3 RX PFC pause on counter for high priority      00000000

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  | Q7_RX_PSON_CNT |    |    |    |    |    |    |    | Q6_RX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_RX_PSON_CNT |    |    |    |    |    |    |    | Q4_RX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                |
|--------|----------------|--------------------------------------------|
| 31:24  | Q7_RX_PSON_CNT | PFC RX pause on count for port3 priority 7 |
| 23:16  | Q6_RX_PSON_CNT | PFC RX pause on count for port3 priority 6 |
| 15:8   | Q5_RX_PSON_CNT | PFC RX pause on count for port3 priority 5 |
| 7:0    | Q4_RX_PSON_CNT | PFC RX pause on count for port3 priority 4 |

15023338      **P3\_PFC\_RX\_PSOFF\_CNT\_L**      Port 3 RX PFC pause off counter for low priority      00000000

| Bit          | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q3_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q2_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q1_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q0_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                 |
|--------|-----------------|---------------------------------------------|
| 31:24  | Q3_RX_PSOFF_CNT | PFC RX pause off count for port3 priority 3 |
| 23:16  | Q2_RX_PSOFF_CNT | PFC RX pause off count for port3 priority 2 |
| 15:8   | Q1_RX_PSOFF_CNT | PFC RX pause off count for port3 priority 1 |
| 7:0    | Q0_RX_PSOFF_CNT | PFC RX pause off count for port3 priority 0 |

1502333C      **P3\_PFC\_RX\_PSOFF\_CNT\_H**      Port 3 RX PFC pause off counter for high priority      00000000

| Bit          | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q7_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q6_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q5_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q4_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                 |
|--------|-----------------|---------------------------------------------|
| 31:24  | Q7_RX_PSOFF_CNT | PFC RX pause off count for port3 priority 7 |
| 23:16  | Q6_RX_PSOFF_CNT | PFC RX pause off count for port3 priority 6 |
| 15:8   | Q5_RX_PSOFF_CNT | PFC RX pause off count for port3 priority 5 |
| 7:0    | Q4_RX_PSOFF_CNT | PFC RX pause off count for port3 priority 4 |

15023340      **P3\_PFC\_TX\_PSON\_CNT\_L**      Port 3 TX PFC pause on counter for low priority      00000000

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q3_TX_PSON_CNT |    |    |    |    |    |    |    | Q2_TX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q1_TX_PSON_CNT |    |    |    |    |    |    |    | Q0_TX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                |
|--------|----------------|--------------------------------------------|
| 31:24  | Q3_TX_PSON_CNT | PFC TX pause on count for port3 priority 3 |
| 23:16  | Q2_TX_PSON_CNT | PFC TX pause on count for port3 priority 2 |
| 15:8   | Q1_TX_PSON_CNT | PFC TX pause on count for port3 priority 1 |
| 7:0    | Q0_TX_PSON_CNT | PFC TX pause on count for port3 priority 0 |



15023344      **P3\_PFC\_TX\_PSON\_CNT\_H**      Port 3 TX PFC pause on counter for high priority      00000000

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q7_TX_PSON_CNT |    |    |    |    |    |    |    | Q6_TX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q5_TX_PSON_CNT |    |    |    |    |    |    |    | Q4_TX_PSON_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                |
|--------|----------------|--------------------------------------------|
| 31:24  | Q7_TX_PSON_CNT | PFC TX pause on count for port3 priority 7 |
| 23:16  | Q6_TX_PSON_CNT | PFC TX pause on count for port3 priority 6 |
| 15:8   | Q5_TX_PSON_CNT | PFC TX pause on count for port3 priority 5 |
| 7:0    | Q4_TX_PSON_CNT | PFC TX pause on count for port3 priority 4 |

15023348      **P3\_PFC\_TX\_PSOFF\_CNT\_L**      Port 3 TX PFC pause off counter for low priority      00000000

| Bit          | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | Q3_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q2_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | Q1_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q0_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| <b>Type</b>  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                 |
|--------|-----------------|---------------------------------------------|
| 31:24  | Q3_TX_PSOFF_CNT | PFC TX pause off count for port3 priority 3 |
| 23:16  | Q2_TX_PSOFF_CNT | PFC TX pause off count for port3 priority 2 |
| 15:8   | Q1_TX_PSOFF_CNT | PFC TX pause off count for port3 priority 1 |
| 7:0    | Q0_TX_PSOFF_CNT | PFC TX pause off count for port3 priority 0 |

1502334C      **P3\_PFC\_TX\_PSOFF\_CNT\_H**      Port 3 TX PFC pause off counter for high priority      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | Q7_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q6_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q4_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                 |
|--------|-----------------|---------------------------------------------|
| 31:24  | Q7_TX_PSOFF_CNT | PFC TX pause off count for port3 priority 7 |
| 23:16  | Q6_TX_PSOFF_CNT | PFC TX pause off count for port3 priority 6 |
| 15:8   | Q5_TX_PSOFF_CNT | PFC TX pause off count for port3 priority 5 |
| 7:0    | Q4_TX_PSOFF_CNT | PFC TX pause off count for port3 priority 4 |

| 15023600 PMCR_P6 |                   |                   |                   |                     | Port 6 MAC control register |    |    |    |    |    |                |                |              |    | 00056330     |              |
|------------------|-------------------|-------------------|-------------------|---------------------|-----------------------------|----|----|----|----|----|----------------|----------------|--------------|----|--------------|--------------|
| Bit              | 31                | 30                | 29                | 28                  | 27                          | 26 | 25 | 24 | 23 | 22 | 21             | 20             | 19           | 18 | 17           | 16           |
| Name             | FORCE_MODE_LNK_P6 | FORCE_MODE_SPD_P6 | FORCE_MODE_DPX_P6 | FORCE_MODE_RX_FC_P6 | FORCE_MODE_TX_FC_P6         |    |    |    |    |    |                |                |              |    |              |              |
| Type             | RW                | RW                | RW                | RW                  | RW                          |    |    |    |    |    |                |                |              |    |              |              |
| Reset            | 0                 | 0                 | 0                 | 0                   | 0                           |    |    |    |    |    |                |                |              |    |              |              |
| Bit              | 15                | 14                | 13                | 12                  | 11                          | 10 | 9  | 8  | 7  | 6  | 5              | 4              | 3            | 2  | 1            | 0            |
| Name             |                   | MAC_TX_EN_P6      | MAC_RX_EN_P6      |                     |                             |    |    |    |    |    | FORCE_RX_FC_P6 | FORCE_TX_FC_P6 | FORCE_SPD_P6 |    | FORCE_DPX_P6 | FORCE_LNK_P6 |
| Type             |                   | RW                | RW                |                     |                             |    |    |    |    |    | RW             | RW             | RW           |    | RW           | RW           |
| Reset            |                   | 1                 | 1                 |                     |                             |    |    |    |    |    | 1              | 1              | 0            | 0  | 0            | 0            |

| Bit(s) | Name                | Description                                                                                                                                                                                                          |
|--------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | FORCE_MODE_LNK_P6   | <b>PORT 6 link status force Mode.</b><br><br>0: Reserved.<br><br>1: Force mode is on. (MAC link status is determined by force_link_P6 register)                                                                      |
| 30     | FORCE_MODE_SPD_P6   | <b>PORT 6 speed force Mode.</b><br><br>0: Reserved.<br><br>1: Force mode is on. (MAC speed is determined by force_spd_P6 register)                                                                                   |
| 29     | FORCE_MODE_DPX_P6   | <b>PORT 6 duplex force Mode.</b><br><br>0: Reserved.<br><br>1: Force mode is on. (MAC duplex mode is determined by force_dpx_P6 register)                                                                            |
| 28     | FORCE_MODE_RX_FC_P6 | <b>PORT 6 RX FC force Mode.</b><br><br>0: Reserved.<br><br>1: Force mode is on. (MAC RX FC ability is determined by force_rx_fc_P6 register)                                                                         |
| 27     | FORCE_MODE_TX_FC_P6 | <b>PORT 6 TX FC force Mode.</b><br><br>0: Reserved.<br><br>1: Force mode is on. (MAC TX FC ability is determined by force_tx_fc_P6 register)                                                                         |
| 14     | MAC_TX_EN_P6        | <b>Port 6 TX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)</b><br><br>0: TX MAC function is disabled.<br><br>1: TX MAC function is enabled. |
| 13     | MAC_RX_EN_P6        | <b>PORT 6 RX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)</b>                                                                              |

| Bit(s) | Name           | Description                                                                                                                  |
|--------|----------------|------------------------------------------------------------------------------------------------------------------------------|
|        |                | 0: RX MAC function is disabled.                                                                                              |
|        |                | 1: RX MAC function is enabled.                                                                                               |
| 5      | FORCE_RX_FC_P6 | <b>PORT 6 Force RX FC. When (force_mode_P6 = 1), this bit is used to control the RX FC ability of PORT 6.</b>                |
|        |                | 0: Reserved.                                                                                                                 |
|        |                | 1: Let the MAC of PORT 6 accept a pause event when operating in full-duplex mode.                                            |
| 4      | FORCE_TX_FC_P6 | <b>PORT 6 Force TX FC</b>                                                                                                    |
|        |                | When (force_mode_P6 = 1), this bit is used to control the TX FC ability of PORT 6.                                           |
|        |                | 0: Reserved.                                                                                                                 |
|        |                | 1: Let the MAC of PORT 6 transmit a pause event when operating in full-duplex mode with low internal free memory page count. |
| 3:2    | FORCE_SPD_P6   | <b>PORT 6 Force Speed [1:0]</b>                                                                                              |
|        |                | When (force_mode_P6 = 1), these bits are used to control MAC speed of PORT 6.                                                |
|        |                | 00: Reserved                                                                                                                 |
|        |                | 01: Reserved                                                                                                                 |
|        |                | 10: 1000Mbps                                                                                                                 |
|        |                | 11: Reserved                                                                                                                 |
| 1      | FORCE_DPX_P6   | <b>PORT 6 Force duplex</b>                                                                                                   |
|        |                | When (force_mode_P6 = 1), this bit is used to control MAC duplex of PORT 6.                                                  |
|        |                | 0: Reserved                                                                                                                  |
|        |                | 1: Full Duplex                                                                                                               |
| 0      | FORCE_LNK_P6   | <b>PORT 6 Force MAC Link Up</b>                                                                                              |
|        |                | When (force_mode_P6 = 1), this bit is used to control link status of PORT 6.                                                 |
|        |                | 0: Link Down                                                                                                                 |
|        |                | 1: Link Up                                                                                                                   |

**15023608 PMSR\_P6 Port 6 MAC status register 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21           | 20           | 19             | 18 | 17             | 16             |
|-------|----|----|----|----|----|----|----|----|----|----|--------------|--------------|----------------|----|----------------|----------------|
| Name  |    |    |    |    |    |    |    |    |    |    |              |              |                |    |                |                |
| Type  |    |    |    |    |    |    |    |    |    |    |              |              |                |    |                |                |
| Reset |    |    |    |    |    |    |    |    |    |    |              |              |                |    |                |                |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5            | 4            | 3              | 2  | 1              | 0              |
| Name  |    |    |    |    |    |    |    |    |    |    | RX_FC_STS_P6 | TX_FC_STS_P6 | MAC_SPD_STS_P6 |    | MAC_DPX_STS_P6 | MAC_LNK_STS_P6 |
| Type  |    |    |    |    |    |    |    |    |    |    | RO           | RO           | RO             |    | RO             | RO             |
| Reset |    |    |    |    |    |    |    |    |    |    | 0            | 0            | 0              | 0  | 0              | 0              |

| Bit(s) | Name           | Description                                                                                                                                                                                                              |
|--------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5      | RX_FC_STS_P6   | <b>PORT 6 RX XFC Status</b><br><br>Port 6 Rx flow control status<br><br>0: Disabled.<br><br>1: Let the MAC of PORT 6 accept a pause event when operating in full-duplex mode                                             |
| 4      | TX_FC_STS_P6   | <b>PORT 6 TX XFC Status</b><br><br>PORT 6 TX flow control status<br><br>0: Disabled.<br><br>1: Let the MAC of PORT 6 transmit a pause event when operating in full-duplex mode with low internal free memory page count. |
| 3:2    | MAC_SPD_STS_P6 | <b>PORT 6 Speed [1:0] Status</b><br><br>Current speed of PORT 6 after PHY links up<br><br>00: Reserved<br><br>01: Reserved<br><br>10: 1000 Mbps<br><br>11: Reserved                                                      |
| 1      | MAC_DPX_STS_P6 | <b>PORT 6 duplex Status</b><br><br>Current duplex mode of PORT 6 after PHY links up<br><br>0: Reserved<br><br>1: Full Duplex                                                                                             |
| 0      | MAC_LNK_STS_P6 | <b>Port 6 Link Up Status</b><br><br>Link up status of PORT 6<br><br>0: Link Down<br><br>1: Link Up                                                                                                                       |

| 15023610 | PINT_EN_P6         |                        |                        |                     | Port 6 interrupt enable register |                      |                     |                    |    |    |    |    | 00000000            |                    |                     |                      |
|----------|--------------------|------------------------|------------------------|---------------------|----------------------------------|----------------------|---------------------|--------------------|----|----|----|----|---------------------|--------------------|---------------------|----------------------|
| Bit      | 31                 | 30                     | 29                     | 28                  | 27                               | 26                   | 25                  | 24                 | 23 | 22 | 21 | 20 | 19                  | 18                 | 17                  | 16                   |
| Name     |                    |                        |                        |                     |                                  |                      |                     |                    |    |    |    |    |                     |                    |                     |                      |
| Type     |                    |                        |                        |                     |                                  |                      |                     |                    |    |    |    |    |                     |                    |                     |                      |
| Reset    |                    |                        |                        |                     |                                  |                      |                     |                    |    |    |    |    |                     |                    |                     |                      |
| Bit      | 15                 | 14                     | 13                     | 12                  | 11                               | 10                   | 9                   | 8                  | 7  | 6  | 5  | 4  | 3                   | 2                  | 1                   | 0                    |
| Name     | TX_TFF_UNDR_INT_EN | TX_MIS_VLAN_ERR_INT_EN | TX_MIS_PAGE_ERR_INT_EN | TX_RPAGE_ERR_INT_EN | TX_RPAGE_TOUT_INT_EN             | TX_GPAGE_TOUT_INT_EN | TX_RDPB_TOUT_INT_EN | TX_DEQ_TOUT_INT_EN |    |    |    |    | RX_AFFL_TOUT_INT_EN | RX_ARL_TOUT_INT_EN | RX_WRPB_TOUT_INT_EN | RX_GPAGE_TOUT_INT_EN |
| Type     | RW                 | RW                     | RW                     | RW                  | RW                               | RW                   | RW                  | RW                 |    |    |    |    | RW                  | RW                 | RW                  | RW                   |
| Reset    | 0                  | 0                      | 0                      | 0                   | 0                                | 0                    | 0                   | 0                  |    |    |    |    | 0                   | 0                  | 0                   | 0                    |

| Bit(s) | Name                  | Description                                                                               |
|--------|-----------------------|-------------------------------------------------------------------------------------------|
| 15     | TX_TFF_UNDR_INT_EN    | <b>TXMAC TXFIFO Under run Interrupt Enable</b><br>0: Disabled<br>1: Enabled               |
| 14     | TX_MISVLAN_ERR_INT_EN | <b>TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable</b><br>0: Disabled<br>1: Enabled |
| 13     | TX_MISPAGE_ERR_INT_EN | <b>TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable</b><br>0: Disabled<br>1: Enabled |
| 12     | TX_RPAGE_ERR_INT_EN   | <b>TX_CTRL Release Page Count Error Interrupt Enable</b><br>0: Disabled<br>1: Enabled     |
| 11     | TX_RPAGE_TOUT_INT_EN  | <b>TX_CTRL Release Page Timeout Interrupt Enable</b><br>0: Disabled<br>1: Enabled         |
| 10     | TX_GPAGE_TOUT_INT_EN  | <b>TX_CTRL Get Page Timeout Interrupt Enable</b><br>0: Disabled<br>1: Enabled             |
| 9      | TX_RDPB_TOUT_INT_EN   | <b>TX_CTRL RD_PB Timeout Interrupt Enable</b><br>0: Disabled<br>1: Enabled                |
| 8      | TX_DEQ_TOUT_INT_EN    | <b>TX_CTRL DEQ Timeout Interrupt Enable</b><br>0: Disabled                                |

| Bit(s) | Name                 | Description                                      |
|--------|----------------------|--------------------------------------------------|
|        |                      | 1: Enabled                                       |
| 3      | RX_AFF_FULL_INT_EN   | <b>RX_CTRL Agent FIFO Full Interrupt Enable</b>  |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |
| 2      | RX_ARL_TOUT_INT_EN   | <b>RX_CTRL ARL Timeout Interrupt Enable</b>      |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |
| 1      | RX_WRPB_TOUT_INT_EN  | <b>RX_CTRL WR_PB Timeout Interrupt Enable</b>    |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |
| 0      | RX_GPAGE_TOUT_INT_EN | <b>RX_CTRL Get Page Timeout Interrupt Enable</b> |
|        |                      | 0: Disabled                                      |
|        |                      | 1: Enabled                                       |



**15023614**      **PINT\_STS\_P6**      **Port 6 interrupt status register**      **00000000**

| Bit   | 31              | 30                 | 29                 | 28               | 27                | 26                | 25               | 24              | 23 | 22 | 21 | 20 | 19              | 18              | 17               | 16                |
|-------|-----------------|--------------------|--------------------|------------------|-------------------|-------------------|------------------|-----------------|----|----|----|----|-----------------|-----------------|------------------|-------------------|
| Name  |                 |                    |                    |                  |                   |                   |                  |                 |    |    |    |    |                 |                 |                  |                   |
| Type  |                 |                    |                    |                  |                   |                   |                  |                 |    |    |    |    |                 |                 |                  |                   |
| Reset |                 |                    |                    |                  |                   |                   |                  |                 |    |    |    |    |                 |                 |                  |                   |
| Bit   | 15              | 14                 | 13                 | 12               | 11                | 10                | 9                | 8               | 7  | 6  | 5  | 4  | 3               | 2               | 1                | 0                 |
| Name  | TX_TFF_UNDR_INT | TX_MISVLAN_ERR_INT | TX_MISPAGE_ERR_INT | TX_RPAGE_ERR_INT | TX_RPAGE_TOUT_INT | TX_GPAGE_TOUT_INT | TX_RDPB_TOUT_INT | TX_DEQ_TOUT_INT |    |    |    |    | RX_AFF_FULL_INT | RX_ARL_TOUT_INT | RX_WRPB_TOUT_INT | RX_GPAGE_TOUT_INT |
| Type  | RO              | RO                 | RO                 | RO               | RO                | RO                | RO               | RO              |    |    |    |    | RO              | RO              | RO               | RO                |
| Reset | 0               | 0                  | 0                  | 0                | 0                 | 0                 | 0                | 0               |    |    |    |    | 0               | 0               | 0                | 0                 |

| Bit(s) | Name               | Description                                                                          |
|--------|--------------------|--------------------------------------------------------------------------------------|
| 15     | TX_TFF_UNDR_INT    | <b>TXMAC TXFIFO Under run Interrupt</b><br><br>0: False<br><br>1: True               |
| 14     | TX_MISVLAN_ERR_INT | <b>TX_CTRL PKT INFO VLAN Mismatch Error Interrupt</b><br><br>0: False<br><br>1: True |
| 13     | TX_MISPAGE_ERR_INT | <b>TX_CTRL PKT INFO Page Mismatch Error Interrupt</b><br><br>0: False<br><br>1: True |
| 12     | TX_RPAGE_ERR_INT   | <b>TX_CTRL Release Page Count Error Interrupt</b><br><br>0: False<br><br>1: True     |
| 11     | TX_RPAGE_TOUT_INT  | <b>TX_CTRL Release Page Timeout Interrupt</b><br><br>0: False<br><br>1: True         |
| 10     | TX_GPAGE_TOUT_INT  | <b>TX_CTRL Get Page Timeout Interrupt</b><br><br>0: False<br><br>1: True             |
| 9      | TX_RDPB_TOUT_INT   | <b>TX_CTRL RD_PB Timeout Interrupt</b><br><br>0: False<br><br>1: True                |
| 8      | TX_DEQ_TOUT_INT    | <b>TX_CTRL DEQ Timeout Interrupt</b><br><br>0: False                                 |

| Bit(s) | Name              | Description                               |
|--------|-------------------|-------------------------------------------|
|        |                   | 1: True                                   |
| 3      | RX_AFF_FULL_INT   | <b>RX_CTRL Agent FIFO Full Interrupt</b>  |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |
| 2      | RX_ARL_TOUT_INT   | <b>RX_CTRL ARL Timeout Interrupt</b>      |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |
| 1      | RX_WRPB_TOUT_INT  | <b>RX_CTRL WR_PB Timeout Interrupt</b>    |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |
| 0      | RX_GPAGE_TOUT_INT | <b>RX_CTRL Get Page Timeout Interrupt</b> |
|        |                   | 0: False                                  |
|        |                   | 1: True                                   |

15024000 TDPC\_P0 TX drop packet counter of Port 0 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                   |
|--------|-------------|---------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_DROP_CNT | The number of events when the frame output should be dropped due to the late collision or excessive collision |

15024004      TCRC\_P0      TX CRC packet counter of Port 0      00000000

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_CRC_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_CRC_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                                          |
|--------|------------|--------------------------------------------------------------------------------------|
| 31:0   | TX_CRC_CNT | The number of events when the frame will output a CRC packet due to TX FIFO underrun |

15024008      TUPC\_P0      TX unicast packet counter of Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                         |
|--------|--------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_UCAST_CNT | The number of unicast frames transmitted without any error. It excludes Pause frame but includes MAC and successful retransmission. |

1502400C      TMPC\_P0      TX multicast packet counter of Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                  |
|--------|--------------|--------------------------------------------------------------|
| 31:0   | TX_MCAST_CNT | The number of multicast frames transmitted without any error |

15024010      TBPC\_P0      TX broadcast packet counter of Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                  |
|--------|--------------|--------------------------------------------------------------|
| 31:0   | TX_BCAST_CNT | The number of broadcast frames transmitted without any error |

15024014      TCEC\_P0      TX collision event counter of Port 0      00000000

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_COL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_COL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                               |
|--------|------------|---------------------------------------------------------------------------|
| 31:0   | TX_COL_CNT | The total number of collision events occurrence during frame transmission |



15024018      TSCEC\_P0      TX single collision event counter of Port 0      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_SCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_SCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                     |
|--------|-------------|---------------------------------------------------------------------------------|
| 31:0   | TX_SCOL_CNT | The number of frames transmitted without any error following a single collision |

1502401C      TMCEC\_P0      TX multiple collision event counter of Port 0      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_MCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_MCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                      |
|--------|-------------|----------------------------------------------------------------------------------|
| 31:0   | TX_MCOL_CNT | The number of frames transmitted without any error following multiple collisions |

15024020      TDEC\_P0      TX deferred event counter of Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DEFER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DEFER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                      |
|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_DEFER_CNT | The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode. Frame involved in collision is not counted |

15024024 TLCEC\_P0 TX late collision event counter of Port 0 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_LCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_LCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                   |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_LCOL_CNT | The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet |

15024028      TXCEC\_P0      TX excessive collision event counter of Port 0      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_XCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_XCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                       |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_XCOL_CNT | The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions |

1502402C      TPPC\_P0      TX pause packet counter of Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                              |
|--------|--------------|----------------------------------------------------------|
| 31:0   | TX_PAUSE_CNT | The number of correct transmitted MAC flow-control frame |

15024030

TL64PC\_P0

TX packet length in 64-byte slot packet counter  
of Port 0

00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                |
|--------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_64_CNT | It indicates the total number of packets, including bad packets transmitted equal to 64 octets in length, excluding framing bits but including FCS octets. |

15024034

TL65PC\_P0

TX packet length in 65-byte slot packet counter  
of Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                       |
|--------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_65TO127_CNT | It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, excluding framing bits but including FCS octets. |



15024038

TL128PC\_P0

TX packet length in 128-byte slot packet counter  
of Port 0

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                        |
|--------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_128TO255_CNT | It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets. |

1502403C

TL256PC\_P0

TX packet length in 256-byte slot packet counter  
of Port 0

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                        |
|--------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_256TO511_CNT | It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, excluding framing bits but including FCS octets. |

15024040

TL512PC\_P0TX packet length in 512-byte slot packet counter  
of Port 0

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                         |
|--------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_512TO1023_CNT | It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, excluding framing bits but including FCS octets. |

15024044

TL1024PC\_P0

TX packet length in 1024-byte slot packet  
counter of Port 0

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                    |
|--------|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_1024TOMAX_CNT | It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets. |

15024048      TOCL\_P0      TX octet counter low double word of Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_OCT_CNT_L | <p><b>{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets.</b></p> <p>TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.</p> <p>TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted.</p> <p>TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted.</p> <p>TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.</p> |

1502404C      TOCH\_P0      TX octet counter high double word of Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                    |
|--------|--------------|--------------------------------|
| 31:0   | TX_OCT_CNT_H | Refer to TX_OCT_CNT_L (above). |

15024060      RDPC\_P0      RX drop packet counter of Port 0      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                                 |
|--------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_DROP_CNT | <p><b>The number of events when the frame should be dropped due to</b></p> <ol style="list-style-type: none"> <li>1. an internal buffer shortage by RX_CTRL</li> <li>2. ingress rate limit by Ingress rate limiter</li> <li>3. broadcast Storm Control, trTCM or ACL Rate Limit.</li> </ol> |

15024064      RFPC\_P0      RX filtering packet counter of Port 0      00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_FILTER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_FILTER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                          |
|--------|---------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_FILTER_CNT | The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or port map is equal to zero. |



15024068      RUPC\_P0      RX unicast packet counter of Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                            |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_UCAST_CNT | The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC frames |

1502406C      RMPC\_P0      RX multicast packet counter of Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                              |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_MCAST_CNT | The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC frames |

15024070      RBPC\_P0      RX broadcast packet counter of Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                              |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_BCAST_CNT | The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC frames |

15024074      RAEPC\_P0      RX alignment error packet counter of Port 0      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_ALIGN_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_ALIGN_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                                                                                                                                   |
|--------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_ALIGN_ERR_CNT | The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted. |

15024078      RCEPC\_P0      RX CRC(FCS) error packet counter of Port 0      00000000

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_FCS_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_FCS_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                                                                                |
|--------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_FCS_ERR_CNT | The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted. |

1502407C      RUSPC\_P0      RX undersized packet counter of Port 0      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_UNDERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_UNDERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                                                                                                                              |
|--------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_UNDERSIZE_CNT | The total number of packets received that are less than 64 octets long excluding framing bits, but including FCS octets which are otherwise well formed. |

15024080      RFEPC\_P0      RX fragmented error packet counter of Port 0      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_FRAG_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_FRAG_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                     |
|--------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_FRAG_ERR_CNT | The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error). |

15024084      ROSPC\_P0      RX oversized packet counter of Port 0      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_OVERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_OVERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                      |
|--------|-----------------|--------------------------------------------------------------------------------------------------|
| 31:0   | RX_OVERSIZE_CNT | The number of frames with length larger than the maximum frame size, received without any error. |



15024088      RJEPD\_P0      RX Jabber error packet counter of Port 0      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_JABB_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_JABB_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                |
|--------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_JABB_ERR_CNT | The total number of packets received that are longer than 1518 octets excluding framing bits, but including FCS octets, and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error). |

1502408C      RPPC\_P0      RX pause packet counter of Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                              |
|--------|--------------|----------------------------------------------------------|
| 31:0   | RX_PAUSE_CNT | The number of correctly received MAC flow-control frame. |

15024090

RL64PC\_P0RX packet length in 64-byte slot packet counter  
of Port 0

00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                             |
|--------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_64_CNT | It indicates the total number of packets, including bad packets received equal to 64 octets in length, excluding framing bits but including FCS octets. |

15024094

RL65PC\_P0RX packet length in 65-byte slot packet counter  
of Port 0

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                    |
|--------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_65TO127_CNT | It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets. |

15024098

RL128PC\_P0RX packet length in 128-byte slot packet counter  
of Port 0

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                                 |
|--------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_128TO255_CNT | It indicates the total number of packets, including bad packets received transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets. |

1502409C

RL256PC\_P0RX packet length in 256-byte slot packet counter  
of Port 0

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                     |
|--------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_256TO511_CNT | It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets. |

150240A0

RL512PC\_P0RX packet length in 512-byte slot packet counter  
of Port 0

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                      |
|--------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_512TO1023_CNT | It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets. |

150240A4

RL1024PC\_P0RX packet length in 1024-byte slot packet  
counter of Port 0

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                 |
|--------|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_1024TOMAX_CNT | It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets. |



150240A8      ROCL\_P0      RX octet counter low double word of Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|--------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_OCT_CNT_L | <p><b>{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets.</b></p> <p>RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.</p> <p>RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted.</p> <p>RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted.</p> <p>RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.</p> |

150240AC      ROCH\_P0      Rx octet counter high double word of Port 0      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                   |
|--------|--------------|-------------------------------|
| 31:0   | RX_OCT_CNT_H | Refer to RX_OCT_CNT_L (above) |

150240B0 RDPC\_CTRL\_P0 RX CTRL drop packet counter of Port 0 00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_CTRL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_CTRL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                                                                    |
|--------|------------------|------------------------------------------------------------------------------------------------|
| 31:0   | RX_CTRL_DROP_CNT | The number of events when the frame should be dropped due to error interrupt issued by RX_CTRL |

150240B4      RDPC\_ING\_P0      RX ingress drop packet counter of Port 0      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_ING_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_ING_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                               |
|--------|-----------------|---------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_ING_DROP_CNT | The number of events when the frame should be dropped according to the ingress rate limit set by the Ingress rate limiter |

150240B8      RDPC ARL P0      RX ARL drop packet counter of Port 0      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_ARL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_ARL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                   |
|--------|-----------------|---------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_ARL_DROP_CNT | The number of events when the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit |

**150240D0      TMIB\_HF\_STS\_PO      TX port MIB counter half full status of Port 0      00000000**

| Bit   | 31            | 30            | 29           | 28           | 27           | 26            | 25            | 24           | 23             | 22            | 21           | 20           | 19           | 18           | 17             | 16             |
|-------|---------------|---------------|--------------|--------------|--------------|---------------|---------------|--------------|----------------|---------------|--------------|--------------|--------------|--------------|----------------|----------------|
| Name  |               |               |              |              |              |               |               |              |                |               |              |              |              | TXOCT_HF_STS | TXL1024_HF_STS | TXL512_HF_STS  |
| Type  |               |               |              |              |              |               |               |              |                |               |              |              |              | W1C          | W1C            | W1C            |
| Reset |               |               |              |              |              |               |               |              |                |               |              |              |              | 0            | 0              | 0              |
| Bit   | 15            | 14            | 13           | 12           | 11           | 10            | 9             | 8            | 7              | 6             | 5            | 4            | 3            | 2            | 1              | 0              |
| Name  | TXL256_HF_STS | TXL128_HF_STS | TXL65_HF_STS | TXL64_HF_STS | TXPAU_HF_STS | TXECOL_HF_STS | TXLCOL_HF_STS | TXDFR_HF_STS | TXMCO_L_HF_STS | TXSCOL_HF_STS | TXCOL_HF_STS | TXBRD_HF_STS | TXMUL_HF_STS | TXUNI_HF_STS | TXCRC_HF_STS   | TXDRO_P_HF_STS |
| Type  | W1C           | W1C           | W1C          | W1C          | W1C          | W1C           | W1C           | W1C          | W1C            | W1C           | W1C          | W1C          | W1C          | W1C          | W1C            | W1C            |
| Reset | 0             | 0             | 0            | 0            | 0            | 0             | 0             | 0            | 0              | 0             | 0            | 0            | 0            | 0            | 0              | 0              |

| Bit(s) | Name           | Description                                                                                      |
|--------|----------------|--------------------------------------------------------------------------------------------------|
| 18     | TXOCT_HF_STS   | <b>TX Octet Counter Half Full Status</b><br><br>0: False<br><br>1: True                          |
| 17     | TXL1024_HF_STS | <b>TX Packet Length above 1024 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 16     | TXL512_HF_STS  | <b>TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 15     | TXL256_HF_STS  | <b>TX Packet Length 256 ~ 511 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True  |
| 14     | TXL128_HF_STS  | <b>TX Packet Length 128 ~ 255 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True  |
| 13     | TXL65_HF_STS   | <b>TX Packet Length 65 ~ 127 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True   |
| 12     | TXL64_HF_STS   | <b>TX Packet Length 64 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True         |
| 11     | TXPAU_HF_STS   | <b>TX Pause Packet Counter Half Full Status</b><br><br>0: False                                  |

| Bit(s) | Name          | Description                                            |
|--------|---------------|--------------------------------------------------------|
|        |               | 1: True                                                |
| 10     | TXECOL_HF_STS | <b>TX Excessive Collision Counter Half Full Status</b> |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 9      | TXLCOL_HF_STS | <b>TX Late Collision Counter Half Full Status</b>      |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 8      | TXDFR_HF_STS  | <b>TX Deferred Counter Half Full Status</b>            |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 7      | TXMCOL_HF_STS | <b>TX Multiple Collision Counter Half Full Status</b>  |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 6      | TXSCOL_HF_STS | <b>TX Single Collision Counter Half Full Status</b>    |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 5      | TXCOL_HF_STS  | <b>TX Collision Event Counter Half Full Status</b>     |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 4      | TXBRD_HF_STS  | <b>TX Broadcast Counter Half Full Status</b>           |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 3      | TXMUL_HF_STS  | <b>TX Multicast Counter Half Full Status</b>           |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 2      | TXUNI_HF_STS  | <b>TX Unicast Counter Half Full Status</b>             |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 1      | TXCRC_HF_STS  | <b>TX CRC Counter Half Full Status</b>                 |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 0      | TXDROP_HF_STS | <b>TX DROP Counter Half Full Status</b>                |

| Bit(s) | Name | Description |
|--------|------|-------------|
|        |      | 0: False    |
|        |      | 1: True     |



150240D4 RMIB HF\_STS\_P0 RX port MIB counter half full status of Port 0 00000000

| Bit   | 31            | 30            | 29           | 28           | 27           | 26           | 25           | 24           | 23           | 22           | 21           | 20           | 19            | 18           | 17             | 16             |
|-------|---------------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|---------------|--------------|----------------|----------------|
| Name  |               |               |              |              |              |              |              |              |              |              | RXARL_HF_STS | RXING_HF_STS | RXCTRL_HF_STS | RXOCT_HF_STS | RXL1024_HF_STS | RXL512_HF_STS  |
| Type  |               |               |              |              |              |              |              |              |              |              | W1C          | W1C          | W1C           | W1C          | W1C            | W1C            |
| Reset |               |               |              |              |              |              |              |              |              |              | 0            | 0            | 0             | 0            | 0              | 0              |
| Bit   | 15            | 14            | 13           | 12           | 11           | 10           | 9            | 8            | 7            | 6            | 5            | 4            | 3             | 2            | 1              | 0              |
| Name  | RXL256_HF_STS | RXL128_HF_STS | RXL65_HF_STS | RXL64_HF_STS | RXPAU_HF_STS | RXJAB_HF_STS | RXOVR_HF_STS | RXFRG_HF_STS | RXUND_HF_STS | RXCRC_HF_STS | RXALG_HF_STS | RXBRD_HF_STS | RXMUL_HF_STS  | RXUNI_HF_STS | RXFIL_HF_STS   | RXDRO_P_HF_STS |
| Type  | W1C           | W1C           | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C           | W1C          | W1C            | W1C            |
| Reset | 0             | 0             | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0             | 0            | 0              | 0              |

| Bit(s) | Name           | Description                                                                                      |
|--------|----------------|--------------------------------------------------------------------------------------------------|
| 21     | RXARL_HF_STS   | <b>RX ARL Drop Counter Half Full Status</b><br><br>0: False<br><br>1: True                       |
| 20     | RXING_HF_STS   | <b>RX Ingress Drop Counter Half Full Status</b><br><br>0: False<br><br>1: True                   |
| 19     | RXCTRL_HF_STS  | <b>RX CTRL Drop Counter Half Full Status</b><br><br>0: False<br><br>1: True                      |
| 18     | RXOCT_HF_STS   | <b>RX Octet Counter Half Full Status</b><br><br>0: False<br><br>1: True                          |
| 17     | RXL1024_HF_STS | <b>RX Packet Length above 1024 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 16     | RXL512_HF_STS  | <b>RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 15     | RXL256_HF_STS  | <b>RX Packet Length 256 ~ 511 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True  |
| 14     | RXL128_HF_STS  | <b>RX Packet Length 128 ~ 255 Bytes Counter Half Full Status</b><br><br>0: False                 |

| Bit(s) | Name         | Description                                                     |
|--------|--------------|-----------------------------------------------------------------|
|        |              | 1: True                                                         |
| 13     | RXL65_HF_STS | <b>RX Packet Length 65 ~ 127 Bytes Counter Half Full Status</b> |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 12     | RXL64_HF_STS | <b>RX Packet Length 64 Bytes Counter Half Full Status</b>       |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 11     | RXPAU_HF_STS | <b>RX Pause Packet Counter Half Full Status</b>                 |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 10     | RXJAB_HF_STS | <b>RX Jabber Error Counter Half Full Status</b>                 |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 9      | RXOVR_HF_STS | <b>RX Oversize Packet Counter Half Full Status</b>              |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 8      | RXFRG_HF_STS | <b>RX Fragment Error Counter Half Full Status</b>               |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 7      | RXUND_HF_STS | <b>RX Undersize Packet Counter Half Full Status</b>             |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 6      | RXCRC_HF_STS | <b>RX CRC ERROR Counter Half Full Status</b>                    |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 5      | RXALG_HF_STS | <b>RX Alignment Error Counter Half Full Status</b>              |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 4      | RXBRD_HF_STS | <b>RX Broadcast Counter Half Full Status</b>                    |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 3      | RXMUL_HF_STS | <b>RX Multicast Counter Half Full Status</b>                    |

| Bit(s) | Name          | Description                                  |
|--------|---------------|----------------------------------------------|
|        |               | 0: False                                     |
|        |               | 1: True                                      |
| 2      | RXUNI_HF_STS  | <b>RX Unicast Counter Half Full Status</b>   |
|        |               | 0: False                                     |
|        |               | 1: True                                      |
| 1      | RXFIL_HF_STS  | <b>RX Filtering Counter Half Full Status</b> |
|        |               | 0: False                                     |
|        |               | 1: True                                      |
| 0      | RXDROP_HF_STS | <b>RX DROP Counter Half Full Status</b>      |
|        |               | 0: False                                     |
|        |               | 1: True                                      |

15024100      TDPC\_P1      TX drop packet counter of Port 1      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                   |
|--------|-------------|---------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_DROP_CNT | The number of events when the frame output should be dropped due to the late collision or excessive collision |

15024104      TCRC\_P1      TX CRC packet counter of Port 1      00000000

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_CRC_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_CRC_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                                          |
|--------|------------|--------------------------------------------------------------------------------------|
| 31:0   | TX_CRC_CNT | The number of events when the frame will output a CRC packet due to TX FIFO underrun |

15024108      TUPC\_P1      TX unicast packet counter of Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                        |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_UCAST_CNT | The number of unicast frames transmitted without any error. It excludes Pause frame but includes MAC and successful retransmission |

1502410C      TMPC\_P1      TX multicast packet counter of Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                  |
|--------|--------------|--------------------------------------------------------------|
| 31:0   | TX_MCAST_CNT | The number of multicast frames transmitted without any error |

15024110      TBPC\_P1      TX broadcast packet counter of Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                  |
|--------|--------------|--------------------------------------------------------------|
| 31:0   | TX_BCAST_CNT | The number of broadcast frames transmitted without any error |



15024114      TCEC\_P1      TX collision event counter of Port 1      00000000

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_COL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_COL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                             |
|--------|------------|-------------------------------------------------------------------------|
| 31:0   | TX_COL_CNT | The total number of collision events occurred during frame transmission |

15024118      TSCEC\_P1      TX single collision event counter of Port 1      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_SCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_SCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                     |
|--------|-------------|---------------------------------------------------------------------------------|
| 31:0   | TX_SCOL_CNT | The number of frames transmitted without any error following a single collision |

1502411C      TMCEC\_P1      TX multiple collision event counter of Port 1      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_MCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_MCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                      |
|--------|-------------|----------------------------------------------------------------------------------|
| 31:0   | TX_MCOL_CNT | The number of frames transmitted without any error following multiple collisions |

15024120      TDEC\_P1      TX deferred event counter of Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DEFER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DEFER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                    |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_DEFER_CNT | <p>The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode</p> <p>Frame involved in collision is not counted.</p> |

15024124 TLCEC\_P1 TX late collision event counter of Port 1 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_LCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_LCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                   |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_LCOL_CNT | The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet |

15024128      TXCEC\_P1      TX excessive collision event counter of Port 1      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_XCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_XCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                       |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_XCOL_CNT | The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions |

1502412C      TPPC\_P1      TX pause packet counter of Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                |
|--------|--------------|------------------------------------------------------------|
| 31:0   | TX_PAUSE_CNT | The number of correctly transmitted MAC flow-control frame |

15024130

TL64PC\_P1

TX packet length in 64-byte slot packet counter  
of Port 1

00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                |
|--------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_64_CNT | It indicates the total number of packets, including bad packets transmitted equal to 64 octets in length, excluding framing bits but including FCS octets. |



15024134

TL65PC\_P1

TX packet length in 65-byte slot packet counter  
of Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                       |
|--------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_65TO127_CNT | It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, excluding framing bits but including FCS octets. |

15024138

TL128PC P1

TX packet length in 128-byte slot packet counter  
of Port 1

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                        |
|--------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_128TO255_CNT | It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets. |

1502413C

TL256PC P1

TX packet length in 256-byte slot packet counter  
of Port 1

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                        |
|--------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_256TO511_CNT | It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, excluding framing bits but including FCS octets. |

15024140

TL512PC\_P1

TX packet length in 512-byte slot packet counter  
of Port 1

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                         |
|--------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_512TO1023_CNT | It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, excluding framing bits but including FCS octets. |

15024144

TL1024PC P1

TX packet length in 1024-byte slot packet  
counter of Port 1

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                    |
|--------|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_1024TOMAX_CNT | It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets. |

15024148 TOCL P1 TX octet counter low double word of Port 1 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_OCT_CNT_L | <p><b>{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets.</b></p> <p>TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.</p> <p>TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted.</p> <p>TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted.</p> <p>TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.</p> |

1502414C      TOCH\_P1      TX octet counter high double word of Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                    |
|--------|--------------|--------------------------------|
| 31:0   | TX_OCT_CNT_H | Refer to TX_OCT_CNT_L (above). |

15024160 RDPC P1 RX drop packet counter of Port 1 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                                |
|--------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_DROP_CNT | <p><b>The number of events when the frame should be dropped due to</b></p> <ol style="list-style-type: none"> <li>1. an internal buffer shortage by RX_CTRL</li> <li>2. ingress rate limit by Ingress rate limiter</li> <li>3. broadcast Storm Control, trTCM or ACL Rate Limit</li> </ol> |



15024164      RFPC\_P1      RX filtering packet counter of Port 1      00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_FILTER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_FILTER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                  |
|--------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_FILTER_CNT | The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or when the port map is equal to zero |

15024168      RUPC\_P1      RX unicast packet counter of Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                            |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_UCAST_CNT | The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC frames |

1502416C      RMPC\_P1      RX multicast packet counter of Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                              |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_MCAST_CNT | The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC frames |

15024170      RBPC\_P1      RX broadcast packet counter of Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                              |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_BCAST_CNT | The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC frames |

15024174      RAEPC\_P1      RX alignment error packet counter of Port 1      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_ALIGN_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_ALIGN_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                                                                                                                                  |
|--------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_ALIGN_ERR_CNT | The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted |

15024178      RCEPC\_P1      RX CRC(FCS) error packet counter of Port 1      00000000

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_FCS_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_FCS_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                                                                               |
|--------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_FCS_ERR_CNT | The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted |

1502417C      RUSPC\_P1      RX undersized packet counter of Port 1      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_UNDERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_UNDERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                                                                                                                             |
|--------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_UNDERSIZE_CNT | The total number of packets received that are less than 64 octets long excluding framing bits, but including FCS octets which are otherwise well formed |

15024180 RFEPC\_P1 RX fragmented error packet counter of Port 1 00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_FRAG_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_FRAG_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                      |
|--------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_FRAG_ERR_CNT | The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and have either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error). |



15024184      ROSPC\_P1      RX oversized packet counter of Port 1      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_OVERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_OVERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                     |
|--------|-----------------|-------------------------------------------------------------------------------------------------|
| 31:0   | RX_OVERSIZE_CNT | The number of frames with length larger than the maximum frame size, received without any error |

15024188 RJEP\_C P1 RX Jabber error packet counter of Port 1 00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_JABB_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_JABB_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                               |
|--------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_JABB_ERR_CNT | The total number of packets received that are longer than 1518 octets excluding framing bits, but including FCS octets and have either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error) |

1502418C      RPPC\_P1      RX pause packet counter of Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                             |
|--------|--------------|---------------------------------------------------------|
| 31:0   | RX_PAUSE_CNT | The number of correctly received MAC flow-control frame |

15024190

RL64PC\_P1RX packet length in 64-byte slot packet counter  
of Port 1

00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                 |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_64_CNT | It indicates the total number of packets, including bad packets received and equal to 64 octets in length, excluding framing bits but including FCS octets. |

15024194

RL65PC\_P1RX packet length in 65-byte slot packet counter  
of Port 1

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                    |
|--------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_65TO127_CNT | It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets. |

15024198

RL128PC\_P1RX packet length in 128-byte slot packet counter  
of Port 1

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                                     |
|--------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_128TO255_CNT | It indicates the total number of packets, including bad packets received and transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets. |

1502419C

RL256PC\_P1RX packet length in 256-byte slot packet counter  
of Port 1

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                     |
|--------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_256TO511_CNT | It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets. |

150241A0

RL512PC\_P1RX packet length in 512-byte slot packet counter  
of Port 1

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                      |
|--------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_512TO1023_CNT | It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets. |



150241A4

RL1024PC P1RX packet length in 1024-byte slot packet  
counter of Port 1

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                 |
|--------|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_1024TOMAX_CNT | It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets. |

150241A8      ROCL P1      RX octet counter low double word of Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|--------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_OCT_CNT_L | <p><b>{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets.</b></p> <p>RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.</p> <p>RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted.</p> <p>RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted.</p> <p>RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.</p> |

150241AC      ROCH\_P1      Rx octet counter high double word of Port 1      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                   |
|--------|--------------|-------------------------------|
| 31:0   | RX_OCT_CNT_H | Refer to RX_OCT_CNT_L (above) |

150241B0 RDPC\_CTRL\_P1 RX CTRL drop packet counter of Port 1 00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_CTRL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_CTRL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                                                                    |
|--------|------------------|------------------------------------------------------------------------------------------------|
| 31:0   | RX_CTRL_DROP_CNT | The number of events when the frame should be dropped due to error interrupt issued by RX_CTRL |

150241B4      RDPC\_ING\_P1      RX ingress drop packet counter of Port 1      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_ING_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_ING_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                               |
|--------|-----------------|-----------------------------------------------------------------------------------------------------------|
| 31:0   | RX_ING_DROP_CNT | The number of events when the frame should be dropped due to a ingress rate limit by Ingress rate limiter |

150241B8      RDPC ARL P1      RX ARL drop packet counter of Port 1      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_ARL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_ARL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                   |
|--------|-----------------|---------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_ARL_DROP_CNT | The number of events when the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit |

**150241D0      TMIB\_HF\_STS\_P1      TX port MIB counter half full status of Port 1      00000000**

| Bit   | 31            | 30            | 29           | 28           | 27           | 26            | 25            | 24           | 23             | 22            | 21           | 20           | 19           | 18           | 17             | 16             |
|-------|---------------|---------------|--------------|--------------|--------------|---------------|---------------|--------------|----------------|---------------|--------------|--------------|--------------|--------------|----------------|----------------|
| Name  |               |               |              |              |              |               |               |              |                |               |              |              |              | TXOCT_HF_STS | TXL1024_HF_STS | TXL512_HF_STS  |
| Type  |               |               |              |              |              |               |               |              |                |               |              |              |              | W1C          | W1C            | W1C            |
| Reset |               |               |              |              |              |               |               |              |                |               |              |              |              | 0            | 0              | 0              |
| Bit   | 15            | 14            | 13           | 12           | 11           | 10            | 9             | 8            | 7              | 6             | 5            | 4            | 3            | 2            | 1              | 0              |
| Name  | TXL256_HF_STS | TXL128_HF_STS | TXL65_HF_STS | TXL64_HF_STS | TXPAU_HF_STS | TXECOL_HF_STS | TXLCOL_HF_STS | TXDFR_HF_STS | TXMCO_L_HF_STS | TXSCOL_HF_STS | TXCOL_HF_STS | TXBRD_HF_STS | TXMUL_HF_STS | TXUNI_HF_STS | TXCRC_HF_STS   | TXDRO_P_HF_STS |
| Type  | W1C           | W1C           | W1C          | W1C          | W1C          | W1C           | W1C           | W1C          | W1C            | W1C           | W1C          | W1C          | W1C          | W1C          | W1C            | W1C            |
| Reset | 0             | 0             | 0            | 0            | 0            | 0             | 0             | 0            | 0              | 0             | 0            | 0            | 0            | 0            | 0              | 0              |

| Bit(s) | Name           | Description                                                                                      |
|--------|----------------|--------------------------------------------------------------------------------------------------|
| 18     | TXOCT_HF_STS   | <b>TX Octet Counter Half Full Status</b><br><br>0: False<br><br>1: True                          |
| 17     | TXL1024_HF_STS | <b>TX Packet Length above 1024 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 16     | TXL512_HF_STS  | <b>TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 15     | TXL256_HF_STS  | <b>TX Packet Length 256 ~ 511 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True  |
| 14     | TXL128_HF_STS  | <b>TX Packet Length 128 ~ 255 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True  |
| 13     | TXL65_HF_STS   | <b>TX Packet Length 65 ~ 127 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True   |
| 12     | TXL64_HF_STS   | <b>TX Packet Length 64 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True         |
| 11     | TXPAU_HF_STS   | <b>TX Pause Packet Counter Half Full Status</b><br><br>0: False                                  |

| Bit(s) | Name          | Description                                            |
|--------|---------------|--------------------------------------------------------|
|        |               | 1: True                                                |
| 10     | TXECOL_HF_STS | <b>TX Excessive Collision Counter Half Full Status</b> |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 9      | TXLCOL_HF_STS | <b>TX Late Collision Counter Half Full Status</b>      |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 8      | TXDFR_HF_STS  | <b>TX Deferred Counter Half Full Status</b>            |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 7      | TXMCOL_HF_STS | <b>TX Multiple Collision Counter Half Full Status</b>  |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 6      | TXSCOL_HF_STS | <b>TX Single Collision Counter Half Full Status</b>    |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 5      | TXCOL_HF_STS  | <b>TX Collision Event Counter Half Full Status</b>     |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 4      | TXBRD_HF_STS  | <b>TX Broadcast Counter Half Full Status</b>           |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 3      | TXMUL_HF_STS  | <b>TX Multicast Counter Half Full Status</b>           |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 2      | TXUNI_HF_STS  | <b>TX Unicast Counter Half Full Status</b>             |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 1      | TXCRC_HF_STS  | <b>TX CRC Counter Half Full Status</b>                 |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 0      | TXDROP_HF_STS | <b>TX DROP Counter Half Full Status</b>                |



| Bit(s) | Name | Description |
|--------|------|-------------|
|        |      | 0: False    |
|        |      | 1: True     |

150241D4 RMIB HF\_STS\_P1 RX port MIB counter half full status of Port 1 00000000

| Bit   | 31            | 30            | 29           | 28           | 27           | 26           | 25           | 24           | 23           | 22           | 21           | 20           | 19            | 18           | 17             | 16             |
|-------|---------------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|---------------|--------------|----------------|----------------|
| Name  |               |               |              |              |              |              |              |              |              |              | RXARL_HF_STS | RXING_HF_STS | RXCTRL_HF_STS | RXOCT_HF_STS | RXL1024_HF_STS | RXL512_HF_STS  |
| Type  |               |               |              |              |              |              |              |              |              |              | W1C          | W1C          | W1C           | W1C          | W1C            | W1C            |
| Reset |               |               |              |              |              |              |              |              |              |              | 0            | 0            | 0             | 0            | 0              | 0              |
| Bit   | 15            | 14            | 13           | 12           | 11           | 10           | 9            | 8            | 7            | 6            | 5            | 4            | 3             | 2            | 1              | 0              |
| Name  | RXL256_HF_STS | RXL128_HF_STS | RXL65_HF_STS | RXL64_HF_STS | RXPAU_HF_STS | RXJAB_HF_STS | RXOVR_HF_STS | RXFRG_HF_STS | RXUND_HF_STS | RXCRC_HF_STS | RXALG_HF_STS | RXBRD_HF_STS | RXMUL_HF_STS  | RXUNI_HF_STS | RXFIL_HF_STS   | RXDRO_P_HF_STS |
| Type  | W1C           | W1C           | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C           | W1C          | W1C            | W1C            |
| Reset | 0             | 0             | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0             | 0            | 0              | 0              |

| Bit(s) | Name           | Description                                                                                      |
|--------|----------------|--------------------------------------------------------------------------------------------------|
| 21     | RXARL_HF_STS   | <b>RX ARL Drop Counter Half Full Status</b><br><br>0: False<br><br>1: True                       |
| 20     | RXING_HF_STS   | <b>RX Ingress Drop Counter Half Full Status</b><br><br>0: False<br><br>1: True                   |
| 19     | RXCTRL_HF_STS  | <b>RX CTRL Drop Counter Half Full Status</b><br><br>0: False<br><br>1: True                      |
| 18     | RXOCT_HF_STS   | <b>RX Octet Counter Half Full Status</b><br><br>0: False<br><br>1: True                          |
| 17     | RXL1024_HF_STS | <b>RX Packet Length above 1024 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 16     | RXL512_HF_STS  | <b>RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 15     | RXL256_HF_STS  | <b>RX Packet Length 256 ~ 511 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True  |
| 14     | RXL128_HF_STS  | <b>RX Packet Length 128 ~ 255 Bytes Counter Half Full Status</b><br><br>0: False                 |

| Bit(s) | Name         | Description                                                     |
|--------|--------------|-----------------------------------------------------------------|
|        |              | 1: True                                                         |
| 13     | RXL65_HF_STS | <b>RX Packet Length 65 ~ 127 Bytes Counter Half Full Status</b> |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 12     | RXL64_HF_STS | <b>RX Packet Length 64 Bytes Counter Half Full Status</b>       |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 11     | RXPAU_HF_STS | <b>RX Pause Packet Counter Half Full Status</b>                 |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 10     | RXJAB_HF_STS | <b>RX Jabber Error Counter Half Full Status</b>                 |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 9      | RXOVR_HF_STS | <b>RX Oversize Packet Counter Half Full Status</b>              |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 8      | RXFRG_HF_STS | <b>RX Fragment Error Counter Half Full Status</b>               |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 7      | RXUND_HF_STS | <b>RX Undersize Packet Counter Half Full Status</b>             |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 6      | RXCRC_HF_STS | <b>RX CRC ERROR Counter Half Full Status</b>                    |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 5      | RXALG_HF_STS | <b>RX Alignment Error Counter Half Full Status</b>              |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 4      | RXBRD_HF_STS | <b>RX Broadcast Counter Half Full Status</b>                    |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 3      | RXMUL_HF_STS | <b>RX Multicast Counter Half Full Status</b>                    |

| Bit(s) | Name          | Description                                  |
|--------|---------------|----------------------------------------------|
|        |               | 0: False                                     |
|        |               | 1: True                                      |
| 2      | RXUNI_HF_STS  | <b>RX Unicast Counter Half Full Status</b>   |
|        |               | 0: False                                     |
|        |               | 1: True                                      |
| 1      | RXFIL_HF_STS  | <b>RX Filtering Counter Half Full Status</b> |
|        |               | 0: False                                     |
|        |               | 1: True                                      |
| 0      | RXDROP_HF_STS | <b>RX DROP Counter Half Full Status</b>      |
|        |               | 0: False                                     |
|        |               | 1: True                                      |

15024200 TDPC\_P2 TX drop packet counter of Port 2 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                      |
|--------|-------------|------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_DROP_CNT | The number of events when the frame should be dropped on output due to the late collision or excessive collision |

15024204      TCRC\_P2      TX CRC packet counter of Port 2      00000000

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_CRC_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_CRC_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                                          |
|--------|------------|--------------------------------------------------------------------------------------|
| 31:0   | TX_CRC_CNT | The number of events when the frame will output a CRC packet due to TX FIFO underrun |

15024208      TUPC\_P2      TX unicast packet counter of Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                           |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_UCAST_CNT | The number of unicast frames transmitted without any error, which excludes Pause frame but includes MAC and successful retransmission |

1502420C      TMPC\_P2      TX multicast packet counter of Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                  |
|--------|--------------|--------------------------------------------------------------|
| 31:0   | TX_MCAST_CNT | The number of multicast frames transmitted without any error |



15024210      TBPC\_P2      TX broadcast packet counter of Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                  |
|--------|--------------|--------------------------------------------------------------|
| 31:0   | TX_BCAST_CNT | The number of broadcast frames transmitted without any error |

15024214      TCEC\_P2      TX collision event counter of Port 2      00000000

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_COL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_COL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                               |
|--------|------------|---------------------------------------------------------------------------|
| 31:0   | TX_COL_CNT | The total number of collision events occurrence during frame transmission |

15024218      TSCEC\_P2      TX single collision event counter of Port 2      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_SCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_SCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                     |
|--------|-------------|---------------------------------------------------------------------------------|
| 31:0   | TX_SCOL_CNT | The number of frames transmitted without any error following a single collision |

1502421C      TMCEC\_P2      TX multiple collision event counter of Port 2      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_MCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_MCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                      |
|--------|-------------|----------------------------------------------------------------------------------|
| 31:0   | TX_MCOL_CNT | The number of frames transmitted without any error following multiple collisions |

15024220      TDEC\_P2      TX deferred event counter of Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DEFER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DEFER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                       |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_DEFER_CNT | The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode. Frame involved in collision is not counted. |

15024224 TLCEC\_P2 TX late collision event counter of Port 2 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_LCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_LCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                   |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_LCOL_CNT | The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet |

15024228 TXCEC\_P2 TX excessive collision event counter of Port 2 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_XCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_XCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                       |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_XCOL_CNT | The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions |

1502422C      TPPC\_P2      TX pause packet counter of Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                |
|--------|--------------|------------------------------------------------------------|
| 31:0   | TX_PAUSE_CNT | The number of correctly transmitted MAC flow-control frame |



15024230

TL64PC\_P2

TX packet length in 64-byte slot packet counter  
of Port 2

00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                |
|--------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_64_CNT | It indicates the total number of packets, including bad packets transmitted equal to 64 octets in length, excluding framing bits but including FCS octets. |

15024234

TL65PC\_P2

TX packet length in 65-byte slot packet counter  
of Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                       |
|--------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_65TO127_CNT | It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, excluding framing bits but including FCS octets. |

15024238

TL128PC\_P2

TX packet length in 128-byte slot packet counter  
of Port 2

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                        |
|--------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_128TO255_CNT | It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets. |

1502423C

TL256PC\_P2

TX packet length in 256-byte slot packet counter  
of Port 2

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                        |
|--------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_256TO511_CNT | It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, excluding framing bits but including FCS octets. |

15024240

TL512PC\_P2

TX packet length in 512-byte slot packet counter  
of Port 2

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                         |
|--------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_512TO1023_CNT | It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, excluding framing bits but including FCS octets. |

15024244

TL1024PC\_P2

TX packet length in 1024-byte slot packet  
counter of Port 2

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                    |
|--------|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_1024TOMAX_CNT | It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets. |

15024248      TOCL\_P2      TX octet counter low double word of Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_OCT_CNT_L | <p><b>{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets.</b></p> <p>TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.</p> <p>TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted.</p> <p>TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted.</p> <p>TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.</p> |

1502424C      TOCH\_P2      TX octet counter high double word of Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                    |
|--------|--------------|--------------------------------|
| 31:0   | TX_OCT_CNT_H | Refer to TX_OCT_CNT_L (above). |



15024260 **RDPC\_P2** RX drop packet counter of Port 2 00000000

| Bit          | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | RX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | RX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                                |
|--------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_DROP_CNT | <p><b>The number of events when the frame should be dropped due to</b></p> <ol style="list-style-type: none"> <li>1. an internal buffer shortage by RX_CTRL</li> <li>2. ingress rate limit by Ingress rate limiter</li> <li>3. broadcast Storm Control, trTCM or ACL Rate Limit</li> </ol> |

15024264      RFPC\_P2      RX filtering packet counter of Port 2      00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_FILTER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_FILTER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                         |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_FILTER_CNT | The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or port map is equal to zero |

15024268      RUPC\_P2      RX unicast packet counter of Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                            |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_UCAST_CNT | The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC frames |

1502426C      RMPC\_P2      RX multicast packet counter of Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                              |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_MCAST_CNT | The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC frames |

15024270      RBPC\_P2      RX broadcast packet counter of Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                              |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_BCAST_CNT | The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC frames |

15024274      RAEPC\_P2      RX alignment error packet counter of Port 2      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_ALIGN_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_ALIGN_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                                                                                                                                  |
|--------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_ALIGN_ERR_CNT | The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted |

15024278      RCEPC\_P2      RX CRC(FCS) error packet counter of Port 2      00000000

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_FCS_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_FCS_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                                                                               |
|--------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_FCS_ERR_CNT | The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted |

1502427C      RUSPC\_P2      RX undersized packet counter of Port 2      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_UNDERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_UNDERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                                                                                                                             |
|--------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_UNDERSIZE_CNT | The total number of packets received that are less than 64 octets long, excluding framing bits but including FCS octets which are otherwise well formed |



15024280      RFEPC\_P2      RX fragmented error packet counter of Port 2      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_FRAG_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_FRAG_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                     |
|--------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_FRAG_ERR_CNT | The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and have either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error) |

15024284      ROSPC\_P2      RX oversized packet counter of Port 2      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_OVERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_OVERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                     |
|--------|-----------------|-------------------------------------------------------------------------------------------------|
| 31:0   | RX_OVERSIZE_CNT | The number of frames with length larger than the maximum frame size, received without any error |

15024288      RJEP\_C\_P2      RX Jabber error packet counter of Port 2      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_JABB_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_JABB_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                |
|--------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_JABB_ERR_CNT | The total number of packets received that are longer than 1518 octets, excluding framing bits but including FCS octets, and have either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error) |

1502428C      RPPC\_P2      RX pause packet counter of Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                             |
|--------|--------------|---------------------------------------------------------|
| 31:0   | RX_PAUSE_CNT | The number of correctly received MAC flow-control frame |

15024290

RL64PC\_P2RX packet length in 64-byte slot packet counter  
of Port 2

00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                             |
|--------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_64_CNT | It indicates the total number of packets, including bad packets received equal to 64 octets in length, excluding framing bits but including FCS octets. |

15024294

RL65PC\_P2RX packet length in 65-byte slot packet counter  
of Port 2

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                    |
|--------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_65TO127_CNT | It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets. |

15024298

RL128PC\_P2RX packet length in 128-byte slot packet counter  
of Port 2

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                                 |
|--------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_128TO255_CNT | It indicates the total number of packets, including bad packets received transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets. |

1502429C

RL256PC\_P2RX packet length in 256-byte slot packet counter  
of Port 2

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                     |
|--------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_256TO511_CNT | It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets. |



150242A0

RL512PC\_P2RX packet length in 512-byte slot packet counter  
of Port 2

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                      |
|--------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_512TO1023_CNT | It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets. |

150242A4

RL1024PC P2RX packet length in 1024-byte slot packet  
counter of Port 2

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                 |
|--------|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_1024TOMAX_CNT | It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets. |

150242A8      ROCL P2      RX octet counter low double word of Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_OCT_CNT_L | <p>{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets.</p> <p>RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.</p> <p>RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted.</p> <p>RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted.</p> <p>RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.</p> |

150242AC      ROCH\_P2      Rx octet counter high double word of Port 2      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                    |
|--------|--------------|--------------------------------|
| 31:0   | RX_OCT_CNT_H | Refer to RX_OCT_CNT_L (above). |

150242B0 RDPC\_CTRL\_P2 RX CTRL drop packet counter of Port 2 00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_CTRL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_CTRL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                                                                    |
|--------|------------------|------------------------------------------------------------------------------------------------|
| 31:0   | RX_CTRL_DROP_CNT | The number of events when the frame should be dropped due to error interrupt issued by RX_CTRL |

150242B4      RDPC\_ING\_P2      RX ingress drop packet counter of Port 2      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_ING_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_ING_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                               |
|--------|-----------------|-----------------------------------------------------------------------------------------------------------|
| 31:0   | RX_ING_DROP_CNT | The number of events when the frame should be dropped due to a ingress rate limit by Ingress rate limiter |

150242B8      RDPC ARL P2      RX ARL drop packet counter of Port 2      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_ARL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_ARL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                   |
|--------|-----------------|---------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_ARL_DROP_CNT | The number of events when the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit |

**150242D0      TMIB\_HF\_STS\_P2      TX port MIB counter half full status of Port 2      00000000**

| Bit   | 31            | 30            | 29           | 28           | 27           | 26            | 25            | 24           | 23             | 22            | 21           | 20           | 19           | 18           | 17             | 16             |
|-------|---------------|---------------|--------------|--------------|--------------|---------------|---------------|--------------|----------------|---------------|--------------|--------------|--------------|--------------|----------------|----------------|
| Name  |               |               |              |              |              |               |               |              |                |               |              |              |              | TXOCT_HF_STS | TXL1024_HF_STS | TXL512_HF_STS  |
| Type  |               |               |              |              |              |               |               |              |                |               |              |              |              | W1C          | W1C            | W1C            |
| Reset |               |               |              |              |              |               |               |              |                |               |              |              |              | 0            | 0              | 0              |
| Bit   | 15            | 14            | 13           | 12           | 11           | 10            | 9             | 8            | 7              | 6             | 5            | 4            | 3            | 2            | 1              | 0              |
| Name  | TXL256_HF_STS | TXL128_HF_STS | TXL65_HF_STS | TXL64_HF_STS | TXPAU_HF_STS | TXECOL_HF_STS | TXLCOL_HF_STS | TXDFR_HF_STS | TXMCO_L_HF_STS | TXSCOL_HF_STS | TXCOL_HF_STS | TXBRD_HF_STS | TXMUL_HF_STS | TXUNI_HF_STS | TXCRC_HF_STS   | TXDRO_P_HF_STS |
| Type  | W1C           | W1C           | W1C          | W1C          | W1C          | W1C           | W1C           | W1C          | W1C            | W1C           | W1C          | W1C          | W1C          | W1C          | W1C            | W1C            |
| Reset | 0             | 0             | 0            | 0            | 0            | 0             | 0             | 0            | 0              | 0             | 0            | 0            | 0            | 0            | 0              | 0              |

| Bit(s) | Name           | Description                                                                                  |
|--------|----------------|----------------------------------------------------------------------------------------------|
| 18     | TXOCT_HF_STS   | <b>TX Octet Counter Half Full Status</b><br><br>0: False<br>1: True                          |
| 17     | TXL1024_HF_STS | <b>TX Packet Length above 1024 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True |
| 16     | TXL512_HF_STS  | <b>TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True |
| 15     | TXL256_HF_STS  | <b>TX Packet Length 256 ~ 511 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True  |
| 14     | TXL128_HF_STS  | <b>TX Packet Length 128 ~ 255 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True  |
| 13     | TXL65_HF_STS   | <b>TX Packet Length 65 ~ 127 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True   |
| 12     | TXL64_HF_STS   | <b>TX Packet Length 64 Bytes Counter Half Full Status</b><br><br>0:<br>False<br>1: True      |
| 11     | TXPAU_HF_STS   | <b>TX Pause Packet Counter Half Full Status</b><br><br>0: False<br>1: True                   |
| 10     | TXECOL_HF_STS  | <b>TX Excessive Collision Counter Half Full Status</b><br><br>0: False<br>1: True            |



| Bit(s) | Name          | Description                                                                  |
|--------|---------------|------------------------------------------------------------------------------|
| 9      | TXLCOL_HF_STS | <b>TX Late Collision Counter Half Full Status</b><br>0: False<br>1: True     |
| 8      | TXDFR_HF_STS  | <b>TX Deferred Counter Half Full Status</b><br>0: False<br>1: True           |
| 7      | TXMCOL_HF_STS | <b>TX Multiple Collision Counter Half Full Status</b><br>0: False<br>1: True |
| 6      | TXSCOL_HF_STS | <b>TX Single Collision Counter Half Full Status</b><br>0: False<br>1: True   |
| 5      | TXCOL_HF_STS  | <b>TX Collision Event Counter Half Full Status</b><br>0: False<br>1: True    |
| 4      | TXBRD_HF_STS  | <b>TX Broadcast Counter Half Full Status</b><br>0: False<br>1: True          |
| 3      | TXMUL_HF_STS  | <b>TX Multicast Counter Half Full Status</b><br>0: False<br>1: True          |
| 2      | TXUNI_HF_STS  | <b>TX Unicast Counter Half Full Status</b><br>0: False<br>1: True            |
| 1      | TXCRC_HF_STS  | <b>TX CRC Counter Half Full Status</b><br>0: False<br>1: True                |
| 0      | TXDROP_HF_STS | <b>TX DROP Counter Half Full Status</b><br>0: False<br>1: True               |

150242D4 RMIB HF\_STS\_P2 RX port MIB counter half full status of Port 2 00000000

| Bit   | 31            | 30            | 29           | 28           | 27           | 26           | 25           | 24           | 23           | 22           | 21           | 20           | 19            | 18           | 17             | 16            |
|-------|---------------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|---------------|--------------|----------------|---------------|
| Name  |               |               |              |              |              |              |              |              |              |              | RXARL_HF_STS | RXING_HF_STS | RXCTRL_HF_STS | RXOCT_HF_STS | RXL1024_HF_STS | RXL512_HF_STS |
| Type  |               |               |              |              |              |              |              |              |              |              | W1C          | W1C          | W1C           | W1C          | W1C            | W1C           |
| Reset |               |               |              |              |              |              |              |              |              |              | 0            | 0            | 0             | 0            | 0              | 0             |
| Bit   | 15            | 14            | 13           | 12           | 11           | 10           | 9            | 8            | 7            | 6            | 5            | 4            | 3             | 2            | 1              | 0             |
| Name  | RXL256_HF_STS | RXL128_HF_STS | RXL65_HF_STS | RXL64_HF_STS | RXPAU_HF_STS | RXJAB_HF_STS | RXOVR_HF_STS | RXFRG_HF_STS | RXUND_HF_STS | RXCRC_HF_STS | RXALG_HF_STS | RXBRD_HF_STS | RXMUL_HF_STS  | RXUNI_HF_STS | RXFIL_P_HF_STS | RXDRO_HF_STS  |
| Type  | W1C           | W1C           | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C           | W1C          | W1C            | W1C           |
| Reset | 0             | 0             | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0             | 0            | 0              | 0             |

| Bit(s) | Name           | Description                                                                                    |
|--------|----------------|------------------------------------------------------------------------------------------------|
| 21     | RXARL_HF_STS   | <b>RX ARL Drop Counter Half Full Status</b><br><br>0:<br>False<br>1: True                      |
| 20     | RXING_HF_STS   | <b>RX Ingress Drop Counter Half Full Status</b><br><br>0: False<br>1: True                     |
| 19     | RXCTRL_HF_STS  | <b>RX CTRL Drop Counter Half Full Status</b><br><br>0: False<br>1: True                        |
| 18     | RXOCT_HF_STS   | <b>RX Octet Counter Half Full Status</b><br><br>0: False<br>1: True                            |
| 17     | RXL1024_HF_STS | <b>RX Packet Length above 1024 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True   |
| 16     | RXL512_HF_STS  | <b>RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True   |
| 15     | RXL256_HF_STS  | <b>RX Packet Length 256 ~ 511 Bytes Counter Half Full Status</b><br><br>0:<br>False<br>1: True |
| 14     | RXL128_HF_STS  | <b>RX Packet Length 128 ~ 255 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True    |
| 13     | RXL65_HF_STS   | <b>RX Packet Length 65 ~ 127 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True     |

| Bit(s) | Name          | Description                                                                          |
|--------|---------------|--------------------------------------------------------------------------------------|
| 12     | RXL64_HF_STS  | <b>RX Packet Length 64 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True |
| 11     | RXPAU_HF_STS  | <b>RX Pause Packet Counter Half Full Status</b><br><br>0: False<br>1: True           |
| 10     | RXJAB_HF_STS  | <b>RX Jabber Error Counter Half Full Status</b><br><br>0: False<br>1: True           |
| 9      | RXOVR_HF_STS  | <b>RX Oversize Packet Counter Half Full Status</b><br><br>0: False<br>1: True        |
| 8      | RXFRG_HF_STS  | <b>RX Fragment Error Counter Half Full Status</b><br><br>0: False<br>1: True         |
| 7      | RXUND_HF_STS  | <b>RX Undersize Packet Counter Half Full Status</b><br><br>0: False<br>1: True       |
| 6      | RXCRC_HF_STS  | <b>RX CRC ERROR Counter Half Full Status</b><br><br>0: False<br>1: True              |
| 5      | RXALG_HF_STS  | <b>RX Alignment Error Counter Half Full Status</b><br><br>0: False<br>1: True        |
| 4      | RXBRD_HF_STS  | <b>RX Broadcast Counter Half Full Status</b><br><br>0: False<br>1: True              |
| 3      | RXMUL_HF_STS  | <b>RX Multicast Counter Half Full Status</b><br><br>0: False<br>1: True              |
| 2      | RXUNI_HF_STS  | <b>RX Unicast Counter Half Full Status</b><br><br>0: False<br>1: True                |
| 1      | RXFIL_HF_STS  | <b>RX Filtering Counter Half Full Status</b><br><br>0: False<br>1: True              |
| 0      | RXDROP_HF_STS | <b>RX DROP Counter Half Full Status</b>                                              |

| Bit(s) | Name | Description |
|--------|------|-------------|
|        |      | 0: False    |
|        |      | 1: True     |

15024300 TDPC\_P3 TX drop packet counter of Port 3 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                  |
|--------|-------------|--------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_DROP_CNT | The number of events when the frame should be dropped on output due to late collision or excessive collision |

15024304      TCRC\_P3      TX CRC packet counter of Port 3      00000000

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_CRC_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_CRC_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                                          |
|--------|------------|--------------------------------------------------------------------------------------|
| 31:0   | TX_CRC_CNT | The number of events when the frame will output a CRC packet due to TX FIFO underrun |

15024308      TUPC\_P3      TX unicast packet counter of Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                         |
|--------|--------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_UCAST_CNT | The number of unicast frames transmitted without any error. It excludes Pause frame but includes MAC and successful retransmission. |

1502430C      TMPC\_P3      TX multicast packet counter of Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                  |
|--------|--------------|--------------------------------------------------------------|
| 31:0   | TX_MCAST_CNT | The number of multicast frames transmitted without any error |



15024310      TBPC\_P3      TX broadcast packet counter of Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                  |
|--------|--------------|--------------------------------------------------------------|
| 31:0   | TX_BCAST_CNT | The number of broadcast frames transmitted without any error |

15024314      TCEC\_P3      TX collision event counter of Port 3      00000000

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_COL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_COL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                               |
|--------|------------|---------------------------------------------------------------------------|
| 31:0   | TX_COL_CNT | The total number of collision events occurrence during frame transmission |

15024318      TSCEC\_P3      TX single collision event counter of Port 3      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_SCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_SCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                     |
|--------|-------------|---------------------------------------------------------------------------------|
| 31:0   | TX_SCOL_CNT | The number of frames transmitted without any error following a single collision |

1502431C      TMCEC\_P3      TX multiple collision event counter of Port 3      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_MCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_MCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                      |
|--------|-------------|----------------------------------------------------------------------------------|
| 31:0   | TX_MCOL_CNT | The number of frames transmitted without any error following multiple collisions |

15024320      TDEC\_P3      TX deferred event counter of Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DEFER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DEFER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                       |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_DEFER_CNT | The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode. Frame involved in collision is not counted. |

15024324 TLCEC\_P3 TX late collision event counter of Port 3 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_LCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_LCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                   |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_LCOL_CNT | The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet |

15024328 TXCEC\_P3 TX excessive collision event counter of Port 3 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_XCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_XCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                       |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_XCOL_CNT | The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions |

1502432C      TPPC P3      TX pause packet counter of Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                              |
|--------|--------------|----------------------------------------------------------|
| 31:0   | TX_PAUSE_CNT | The number of correct transmitted MAC flow-control frame |



15024330

TL64PC\_P3

TX packet length in 64-byte slot packet counter  
of Port 3

00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                        |
|--------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_64_CNT | It indicates the total number of packets, including bad packets transmitted and equal to 64 octets in length, and excluding framing bits but including FCS octets. |

15024334

TL65PC\_P3

TX packet length in 65-byte slot packet counter  
of Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                           |
|--------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_65TO127_CNT | It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, and excluding framing bits but including FCS octets. |

15024338

TL128PC\_P3

TX packet length in 128-byte slot packet counter  
of Port 3

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                            |
|--------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_128TO255_CNT | It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, and excluding framing bits but including FCS octets. |

1502433C

TL256PC\_P3

TX packet length in 256-byte slot packet counter  
of Port 3

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                            |
|--------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_256TO511_CNT | It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, and excluding framing bits but including FCS octets. |

15024340

TL512PC\_P3

TX packet length in 512-byte slot packet counter  
of Port 3

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                             |
|--------|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_512TO1023_CNT | It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, and excluding framing bits but including FCS octets. |

15024344

TL1024PC P3

TX packet length in 1024-byte slot packet  
counter of Port 3

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                        |
|--------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_1024TOMAX_CNT | It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, and excluding framing bits but including FCS octets. |

15024348      TOCL P3      TX octet counter low double word of Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_OCT_CNT_L | <p><b>{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets.</b></p> <p>TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.</p> <p>TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted.</p> <p>TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted.</p> <p>TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.</p> |

1502434C      TOCH\_P3      TX octet counter high double word of Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                    |
|--------|--------------|--------------------------------|
| 31:0   | TX_OCT_CNT_H | Refer to TX_OCT_CNT_L (above). |



15024360 **RDPC P3** RX drop packet counter of Port 3 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                                 |
|--------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_DROP_CNT | <p><b>The number of events when the frame should be dropped due to</b></p> <ol style="list-style-type: none"> <li>1. an internal buffer shortage by RX_CTRL</li> <li>2. ingress rate limit by Ingress rate limiter</li> <li>3. broadcast Storm Control, trTCM or ACL Rate Limit.</li> </ol> |

15024364      RFPC\_P3      RX filtering packet counter of Port 3      00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_FILTER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_FILTER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                         |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_FILTER_CNT | The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or port map is equal to zero |

15024368      RUPC\_P3      RX unicast packet counter of Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                            |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_UCAST_CNT | The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC frames |

1502436C      RMPC\_P3      RX multicast packet counter of Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                              |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_MCAST_CNT | The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC frames |

15024370      **RBPC\_P3**      **RX broadcast packet counter of Port 3**      **00000000**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                              |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_BCAST_CNT | The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC frames |

15024374      **RAEPC\_P3**      RX alignment error packet counter of Port 3      00000000

| Bit          | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | RX_ALIGN_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | RX_ALIGN_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                                                                                                                                  |
|--------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_ALIGN_ERR_CNT | The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted |

15024378      RCEPC\_P3      RX CRC(FCS) error packet counter of Port 3      00000000

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_FCS_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_FCS_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                                                                               |
|--------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_FCS_ERR_CNT | The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted |

1502437C      RUSPC\_P3      RX undersized packet counter of Port 3      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_UNDERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_UNDERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                                                                                                                             |
|--------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_UNDERSIZE_CNT | The total number of packets received that are less than 64 octets long, excluding framing bits but including FCS octets which are otherwise well formed |



15024380      RFEPC\_P3      RX fragmented error packet counter of Port 3      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_FRAG_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_FRAG_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                    |
|--------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_FRAG_ERR_CNT | The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error) |

15024384      **ROSPC\_P3**      RX oversized packet counter of Port 3      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_OVERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_OVERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                     |
|--------|-----------------|-------------------------------------------------------------------------------------------------|
| 31:0   | RX_OVERSIZE_CNT | The number of frames with length larger than the maximum frame size, received without any error |

15024388      RJEP\_C\_P3      RX Jabber error packet counter of Port 3      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_JABB_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_JABB_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                               |
|--------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_JABB_ERR_CNT | The total number of packets received that are longer than 1518 octets excluding framing bits, but including FCS octets, and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error) |

1502438C      RPPC\_P3      RX pause packet counter of Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                             |
|--------|--------------|---------------------------------------------------------|
| 31:0   | RX_PAUSE_CNT | The number of correctly received MAC flow-control frame |

15024390

RL64PC\_P3RX packet length in 64-byte slot packet counter  
of Port 3

00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                             |
|--------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_64_CNT | It indicates the total number of packets, including bad packets received equal to 64 octets in length, excluding framing bits but including FCS octets. |

15024394

RL65PC\_P3

RX packet length in 65-byte slot packet counter  
of Port 3

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                    |
|--------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_65TO127_CNT | It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets. |

15024398

RL128PC\_P3RX packet length in 128-byte slot packet counter  
of Port 3

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                                 |
|--------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_128TO255_CNT | It indicates the total number of packets, including bad packets received transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets. |

1502439C

RL256PC\_P3RX packet length in 256-byte slot packet counter  
of Port 3

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                     |
|--------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_256TO511_CNT | It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets. |



150243A0

RL512PC\_P3RX packet length in 512-byte slot packet counter  
of Port 3

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                      |
|--------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_512TO1023_CNT | It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets. |

150243A4

RL1024PC P3RX packet length in 1024-byte slot packet  
counter of Port 3

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                 |
|--------|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_1024TOMAX_CNT | It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets. |

150243A8      ROCL P3      RX octet counter low double word of Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_OCT_CNT_L | <p>{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets.</p> <p>RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.</p> <p>RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted.</p> <p>RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted.</p> <p>RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.</p> |

150243AC      ROCH\_P3      Rx octet counter high double word of Port 3      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                    |
|--------|--------------|--------------------------------|
| 31:0   | RX_OCT_CNT_H | Refer to RX_OCT_CNT_L (above). |

150243B0 RDPC\_CTRL\_P3 RX CTRL drop packet counter of Port 3 00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_CTRL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_CTRL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                                                                    |
|--------|------------------|------------------------------------------------------------------------------------------------|
| 31:0   | RX_CTRL_DROP_CNT | The number of events when the frame should be dropped due to error interrupt issued by RX_CTRL |

150243B4 RDPC\_ING\_P3 RX ingress drop packet counter of Port 3 00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_ING_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_ING_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                               |
|--------|-----------------|-----------------------------------------------------------------------------------------------------------|
| 31:0   | RX_ING_DROP_CNT | The number of events when the frame should be dropped due to a ingress rate limit by Ingress rate limiter |

150243B8      RDPC ARL P3      RX ARL drop packet counter of Port 3      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_ARL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_ARL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                   |
|--------|-----------------|---------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_ARL_DROP_CNT | The number of events when the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit |

**150243D0      TMIB\_HF\_STS\_P3      TX port MIB counter half full status of Port 3      00000000**

| Bit   | 31            | 30            | 29           | 28           | 27           | 26            | 25            | 24           | 23             | 22            | 21           | 20           | 19           | 18           | 17             | 16             |
|-------|---------------|---------------|--------------|--------------|--------------|---------------|---------------|--------------|----------------|---------------|--------------|--------------|--------------|--------------|----------------|----------------|
| Name  |               |               |              |              |              |               |               |              |                |               |              |              |              | TXOCT_HF_STS | TXL1024_HF_STS | TXL512_HF_STS  |
| Type  |               |               |              |              |              |               |               |              |                |               |              |              |              | W1C          | W1C            | W1C            |
| Reset |               |               |              |              |              |               |               |              |                |               |              |              |              | 0            | 0              | 0              |
| Bit   | 15            | 14            | 13           | 12           | 11           | 10            | 9             | 8            | 7              | 6             | 5            | 4            | 3            | 2            | 1              | 0              |
| Name  | TXL256_HF_STS | TXL128_HF_STS | TXL65_HF_STS | TXL64_HF_STS | TXPAU_HF_STS | TXECOL_HF_STS | TXLCOL_HF_STS | TXDFR_HF_STS | TXMCO_L_HF_STS | TXSCOL_HF_STS | TXCOL_HF_STS | TXBRD_HF_STS | TXMUL_HF_STS | TXUNI_HF_STS | TXCRC_HF_STS   | TXDRO_P_HF_STS |
| Type  | W1C           | W1C           | W1C          | W1C          | W1C          | W1C           | W1C           | W1C          | W1C            | W1C           | W1C          | W1C          | W1C          | W1C          | W1C            | W1C            |
| Reset | 0             | 0             | 0            | 0            | 0            | 0             | 0             | 0            | 0              | 0             | 0            | 0            | 0            | 0            | 0              | 0              |

| Bit(s) | Name           | Description                                                                                   |
|--------|----------------|-----------------------------------------------------------------------------------------------|
| 18     | TXOCT_HF_STS   | <b>TX Octet Counter Half Full Status</b><br><br>0:<br>False<br>1: True                        |
| 17     | TXL1024_HF_STS | <b>TX Packet Length above 1024 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True  |
| 16     | TXL512_HF_STS  | <b>TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True  |
| 15     | TXL256_HF_STS  | <b>TX Packet Length 256 ~ 511 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True   |
| 14     | TXL128_HF_STS  | <b>TX Packet Length 128 ~ 255 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True   |
| 13     | TXL65_HF_STS   | <b>TX Packet Length 65 ~ 127 Bytes Counter Half Full Status</b><br><br>0:<br>False<br>1: True |
| 12     | TXL64_HF_STS   | <b>TX Packet Length 64 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True          |
| 11     | TXPAU_HF_STS   | <b>TX Pause Packet Counter Half Full Status</b><br><br>0: False<br>1: True                    |
| 10     | TXECOL_HF_STS  | <b>TX Excessive Collision Counter Half Full Status</b><br><br>0: False<br>1: True             |



| Bit(s) | Name          | Description                                                                  |
|--------|---------------|------------------------------------------------------------------------------|
| 9      | TXCOL_HF_STS  | <b>TX Late Collision Counter Half Full Status</b><br>0: False<br>1: True     |
| 8      | TXDFR_HF_STS  | <b>TX Deferred Counter Half Full Status</b><br>0: False<br>1: True           |
| 7      | TXMCOL_HF_STS | <b>TX Multiple Collision Counter Half Full Status</b><br>0: False<br>1: True |
| 6      | TXSCOL_HF_STS | <b>TX Single Collision Counter Half Full Status</b><br>0: False<br>1: True   |
| 5      | TXCOL_HF_STS  | <b>TX Collision Event Counter Half Full Status</b><br>0: False<br>1: True    |
| 4      | TXBRD_HF_STS  | <b>TX Broadcast Counter Half Full Status</b><br>0: False<br>1: True          |
| 3      | TXMUL_HF_STS  | <b>TX Multicast Counter Half Full Status</b><br>0: False<br>1: True          |
| 2      | TXUNI_HF_STS  | <b>TX Unicast Counter Half Full Status</b><br>0: False<br>1: True            |
| 1      | TXCRC_HF_STS  | <b>TX CRC Counter Half Full Status</b><br>0: False<br>1: True                |
| 0      | TXDROP_HF_STS | <b>TX DROP Counter Half Full Status</b><br>0: False<br>1: True               |

150243D4 RMIB HF\_STS\_P3 RX port MIB counter half full status of Port 3 00000000

| Bit   | 31            | 30            | 29           | 28           | 27           | 26           | 25           | 24           | 23           | 22           | 21           | 20           | 19            | 18           | 17             | 16             |
|-------|---------------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|---------------|--------------|----------------|----------------|
| Name  |               |               |              |              |              |              |              |              |              |              | RXARL_HF_STS | RXING_HF_STS | RXCTRL_HF_STS | RXOCT_HF_STS | RXL1024_HF_STS | RXL512_HF_STS  |
| Type  |               |               |              |              |              |              |              |              |              |              | W1C          | W1C          | W1C           | W1C          | W1C            | W1C            |
| Reset |               |               |              |              |              |              |              |              |              |              | 0            | 0            | 0             | 0            | 0              | 0              |
| Bit   | 15            | 14            | 13           | 12           | 11           | 10           | 9            | 8            | 7            | 6            | 5            | 4            | 3             | 2            | 1              | 0              |
| Name  | RXL256_HF_STS | RXL128_HF_STS | RXL65_HF_STS | RXL64_HF_STS | RXPAU_HF_STS | RXJAB_HF_STS | RXOVR_HF_STS | RXFRG_HF_STS | RXUND_HF_STS | RXCRC_HF_STS | RXALG_HF_STS | RXBRD_HF_STS | RXMUL_HF_STS  | RXUNI_HF_STS | RXFIL_HF_STS   | RXDRO_P_HF_STS |
| Type  | W1C           | W1C           | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C           | W1C          | W1C            | W1C            |
| Reset | 0             | 0             | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0             | 0            | 0              | 0              |

| Bit(s) | Name           | Description                                                                                  |
|--------|----------------|----------------------------------------------------------------------------------------------|
| 21     | RXARL_HF_STS   | <b>RX ARL Drop Counter Half Full Status</b><br><br>0: False<br>1: True                       |
| 20     | RXING_HF_STS   | <b>RX Ingress Drop Counter Half Full Status</b><br><br>0: False<br>1: True                   |
| 19     | RXCTRL_HF_STS  | <b>RX CTRL Drop Counter Half Full Status</b><br><br>0: False<br>1: True                      |
| 18     | RXOCT_HF_STS   | <b>RX Octet Counter Half Full Status</b><br><br>0: False<br>1: True                          |
| 17     | RXL1024_HF_STS | <b>RX Packet Length above 1024 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True |
| 16     | RXL512_HF_STS  | <b>RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True |
| 15     | RXL256_HF_STS  | <b>RX Packet Length 256 ~ 511 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True  |
| 14     | RXL128_HF_STS  | <b>RX Packet Length 128 ~ 255 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True  |
| 13     | RXL65_HF_STS   | <b>RX Packet Length 65 ~ 127 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True   |

| Bit(s) | Name          | Description                                                                          |
|--------|---------------|--------------------------------------------------------------------------------------|
| 12     | RXL64_HF_STS  | <b>RX Packet Length 64 Bytes Counter Half Full Status</b><br><br>0: False<br>1: True |
| 11     | RXPAU_HF_STS  | <b>RX Pause Packet Counter Half Full Status</b><br><br>0: False<br>1: True           |
| 10     | RXJAB_HF_STS  | <b>RX Jabber Error Counter Half Full Status</b><br><br>0: False<br>1: True           |
| 9      | RXOVR_HF_STS  | <b>RX Oversize Packet Counter Half Full Status</b><br><br>0: False<br>1: True        |
| 8      | RXFRG_HF_STS  | <b>RX Fragment Error Counter Half Full Status</b><br><br>0: False<br>1: True         |
| 7      | RXUND_HF_STS  | <b>RX Undersize Packet Counter Half Full Status</b><br><br>0: False<br>1: True       |
| 6      | RXCRC_HF_STS  | <b>RX CRC ERROR Counter Half Full Status</b><br><br>0: False<br>1: True              |
| 5      | RXALG_HF_STS  | <b>RX Alignment Error Counter Half Full Status</b><br><br>0: False<br>1: True        |
| 4      | RXBRD_HF_STS  | <b>RX Broadcast Counter Half Full Status</b><br><br>0: False<br>1: True              |
| 3      | RXMUL_HF_STS  | <b>RX Multicast Counter Half Full Status</b><br><br>0: False<br>1: True              |
| 2      | RXUNI_HF_STS  | <b>RX Unicast Counter Half Full Status</b><br><br>0: False<br>1: True                |
| 1      | RXFIL_HF_STS  | <b>RX Filtering Counter Half Full Status</b><br><br>0: False<br>1: True              |
| 0      | RXDROP_HF_STS | <b>RX DROP Counter Half Full Status</b>                                              |

| Bit(s) | Name | Description |
|--------|------|-------------|
|        |      | 0: False    |
|        |      | 1: True     |

15024600      TDPC\_P6      TX drop packet counter of Port 6      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                      |
|--------|-------------|------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_DROP_CNT | The number of events when the frame should be dropped on output due to the late collision or excessive collision |

15024604      TCRC\_P6      TX CRC packet counter of Port 6      00000000

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_CRC_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_CRC_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                                          |
|--------|------------|--------------------------------------------------------------------------------------|
| 31:0   | TX_CRC_CNT | The number of events when the frame will output a CRC packet due to TX FIFO underrun |

15024608      TUPC\_P6      TX unicast packet counter of Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                         |
|--------|--------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_UCAST_CNT | The number of unicast frames transmitted without any error. It excludes Pause frame but includes MAC and successful retransmission. |

1502460C      **TMPC\_P6**      TX multicast packet counter of Port 6      00000000

| Bit          | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | TX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | TX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                  |
|--------|--------------|--------------------------------------------------------------|
| 31:0   | TX_MCAST_CNT | The number of multicast frames transmitted without any error |



15024610      **TBPC\_P6**      **TX broadcast packet counter of Port 6**      **00000000**

| Bit          | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | TX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | TX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                  |
|--------|--------------|--------------------------------------------------------------|
| 31:0   | TX_BCAST_CNT | The number of broadcast frames transmitted without any error |

15024614      TCEC\_P6      TX collision event counter of Port 6      00000000

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_COL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_COL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                               |
|--------|------------|---------------------------------------------------------------------------|
| 31:0   | TX_COL_CNT | The total number of collision events occurrence during frame transmission |

15024618      TSCEC\_P6      TX single collision event counter of Port 6      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_SCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_SCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                     |
|--------|-------------|---------------------------------------------------------------------------------|
| 31:0   | TX_SCOL_CNT | The number of frames transmitted without any error following a single collision |

1502461C      TMCEC\_P6      TX multiple collision event counter of Port 6      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_MCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_MCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                      |
|--------|-------------|----------------------------------------------------------------------------------|
| 31:0   | TX_MCOL_CNT | The number of frames transmitted without any error following multiple collisions |

15024620      TDEC\_P6      TX deferred event counter of Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DEFER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DEFER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                       |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_DEFER_CNT | The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode. Frame involved in collision is not counted. |

15024624 TLCEC\_P6 TX late collision event counter of Port 6 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_LCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_LCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                   |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_LCOL_CNT | The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet |

15024628      TXCEC\_P6      TX excessive collision event counter of Port 6      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_XCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_XCOL_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                       |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_XCOL_CNT | The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions |

1502462C      TPPC\_P6      TX pause packet counter of Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                              |
|--------|--------------|----------------------------------------------------------|
| 31:0   | TX_PAUSE_CNT | The number of correct transmitted MAC flow-control frame |



15024630

TL64PC\_P6

TX packet length in 64-byte slot packet counter  
of Port 6

00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                |
|--------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_64_CNT | It indicates the total number of packets, including bad packets transmitted equal to 64 octets in length, excluding framing bits but including FCS octets. |

15024634

TL65PC\_P6

TX packet length in 65-byte slot packet counter  
of Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                       |
|--------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_65TO127_CNT | It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, excluding framing bits but including FCS octets. |

15024638

TL128PC\_P6

TX packet length in 128-byte slot packet counter  
of Port 6

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                        |
|--------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_128TO255_CNT | It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets. |

1502463C

TL256PC\_P6

TX packet length in 256-byte slot packet counter  
of Port 6

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                        |
|--------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_256TO511_CNT | It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, excluding framing bits but including FCS octets. |

15024640

TL512PC\_P6

TX packet length in 512-byte slot packet counter  
of Port 6

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                         |
|--------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_512TO1023_CNT | It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, excluding framing bits but including FCS octets. |

15024644

TL1024PC P6

TX packet length in 1024-byte slot packet  
counter of Port 6

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                    |
|--------|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_PKT_1024TOMAX_CNT | It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets. |

15024648      TOCL\_P6      TX octet counter low double word of Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | TX_OCT_CNT_L | <p><b>{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets.</b></p> <p>TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.</p> <p>TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted.</p> <p>TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted.</p> <p>TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.</p> |

1502464C      TOCH\_P6      TX octet counter high double word of Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                    |
|--------|--------------|--------------------------------|
| 31:0   | TX_OCT_CNT_H | Refer to TX_OCT_CNT_L (above). |



15024660 **RDPC\_P6** RX drop packet counter of Port 6 00000000

| Bit          | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | RX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | RX_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                                 |
|--------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_DROP_CNT | <p><b>The number of events when the frame should be dropped due to</b></p> <ol style="list-style-type: none"> <li>1. an internal buffer shortage by RX_CTRL</li> <li>2. ingress rate limit by Ingress rate limiter</li> <li>3. broadcast Storm Control, trTCM or ACL Rate Limit.</li> </ol> |

15024664      RFPC\_P6      RX filtering packet counter of Port 6      00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_FILTER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_FILTER_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                         |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_FILTER_CNT | The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or port map is equal to zero |

15024668      RUPC\_P6      RX unicast packet counter of Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_UCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                            |
|--------|--------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_UCAST_CNT | The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC frames |

1502466C      RMPC\_P6      RX multicast packet counter of Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_MCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                              |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_MCAST_CNT | The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC frames |

15024670      RBPC\_P6      RX broadcast packet counter of Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_BCAST_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                              |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_BCAST_CNT | The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC frames |

15024674      **RAEPC\_P6**      RX alignment error packet counter of Port 6      00000000

| Bit          | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | RX_ALIGN_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | RX_ALIGN_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                                                                                                                                  |
|--------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_ALIGN_ERR_CNT | The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted |

15024678      RCEPC\_P6      RX CRC(FCS) error packet counter of Port 6      00000000

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_FCS_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_FCS_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                                                                               |
|--------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_FCS_ERR_CNT | The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted |

1502467C      RUSPC\_P6      RX undersized packet counter of Port 6      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_UNDERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_UNDERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                                                                                                                             |
|--------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_UNDERSIZE_CNT | The total number of packets received that are less than 64 octets long, excluding framing bits but including FCS octets which are otherwise well formed |



15024680      RFEPC\_P6      RX fragmented error packet counter of Port 6      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_FRAG_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_FRAG_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                    |
|--------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_FRAG_ERR_CNT | The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error) |

15024684      ROSPC\_P6      RX oversized packet counter of Port 6      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_OVERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_OVERSIZE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                     |
|--------|-----------------|-------------------------------------------------------------------------------------------------|
| 31:0   | RX_OVERSIZE_CNT | The number of frames with length larger than the maximum frame size, received without any error |

15024688      RJEP\_C\_P6      RX Jabber error packet counter of Port 6      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_JABB_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_JABB_ERR_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                               |
|--------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_JABB_ERR_CNT | The total number of packets received that are longer than 1518 octets excluding framing bits, but including FCS octets, and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error) |

1502468C      RPPC\_P6      RX pause packet counter of Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PAUSE_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                             |
|--------|--------------|---------------------------------------------------------|
| 31:0   | RX_PAUSE_CNT | The number of correctly received MAC flow-control frame |

15024690

RL64PC\_P6RX packet length in 64-byte slot packet counter  
of Port 6

00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_64_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                             |
|--------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_64_CNT | It indicates the total number of packets, including bad packets received equal to 64 octets in length, excluding framing bits but including FCS octets. |

15024694

RL65PC\_P6

RX packet length in 65-byte slot packet counter  
of Port 6

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_65TO127_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                    |
|--------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_65TO127_CNT | It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets. |

15024698

RL128PC\_P6

RX packet length in 128-byte slot packet counter  
of Port 6

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_128TO255_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                                 |
|--------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_128TO255_CNT | It indicates the total number of packets, including bad packets received transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets. |

1502469C

RL256PC\_P6RX packet length in 256-byte slot packet counter  
of Port 6

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_256TO511_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                     |
|--------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_256TO511_CNT | It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets. |



150246A0

RL512PC\_P6

RX packet length in 512-byte slot packet counter  
of Port 6

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_512TO1023_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                      |
|--------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_512TO1023_CNT | It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets. |

150246A4

RL1024PC P6RX packet length in 1024-byte slot packet  
counter of Port 6

00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_PKT_1024TOMAX_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                 |
|--------|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_PKT_1024TOMAX_CNT | It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets. |

150246A8      ROCL P6      RX octet counter low double word of Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_OCT_CNT_L |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_OCT_CNT_L | <p>{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets.</p> <p>RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted.</p> <p>RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted.</p> <p>RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted.</p> <p>RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.</p> |

150246AC      ROCH\_P6      Rx octet counter high double word of Port 6      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_OCT_CNT_H |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                    |
|--------|--------------|--------------------------------|
| 31:0   | RX_OCT_CNT_H | Refer to RX_OCT_CNT_L (above). |

150246B0 RDPC\_CTRL\_P6 RX CTRL drop packet counter of Port 6 00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_CTRL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_CTRL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                                                                    |
|--------|------------------|------------------------------------------------------------------------------------------------|
| 31:0   | RX_CTRL_DROP_CNT | The number of events when the frame should be dropped due to error interrupt issued by RX_CTRL |

150246B4      RDPC\_ING\_P6      RX ingress drop packet counter of Port 6      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_ING_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_ING_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                               |
|--------|-----------------|-----------------------------------------------------------------------------------------------------------|
| 31:0   | RX_ING_DROP_CNT | The number of events when the frame should be dropped due to a ingress rate limit by Ingress rate limiter |

150246B8 RDPC ARL P6 RX ARL drop packet counter of Port 6 00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_ARL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_ARL_DROP_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                   |
|--------|-----------------|---------------------------------------------------------------------------------------------------------------|
| 31:0   | RX_ARL_DROP_CNT | The number of events when the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit |

**150246D0      TMIB\_HF\_STS\_P6      TX port MIB counter half full status of Port 6      00000000**

| Bit   | 31            | 30            | 29           | 28           | 27           | 26            | 25            | 24           | 23             | 22            | 21           | 20           | 19           | 18           | 17             | 16             |
|-------|---------------|---------------|--------------|--------------|--------------|---------------|---------------|--------------|----------------|---------------|--------------|--------------|--------------|--------------|----------------|----------------|
| Name  |               |               |              |              |              |               |               |              |                |               |              |              |              | TXOCT_HF_STS | TXL1024_HF_STS | TXL512_HF_STS  |
| Type  |               |               |              |              |              |               |               |              |                |               |              |              |              | W1C          | W1C            | W1C            |
| Reset |               |               |              |              |              |               |               |              |                |               |              |              |              | 0            | 0              | 0              |
| Bit   | 15            | 14            | 13           | 12           | 11           | 10            | 9             | 8            | 7              | 6             | 5            | 4            | 3            | 2            | 1              | 0              |
| Name  | TXL256_HF_STS | TXL128_HF_STS | TXL65_HF_STS | TXL64_HF_STS | TXPAU_HF_STS | TXECOL_HF_STS | TXLCOL_HF_STS | TXDFR_HF_STS | TXMCO_L_HF_STS | TXSCOL_HF_STS | TXCOL_HF_STS | TXBRD_HF_STS | TXMUL_HF_STS | TXUNI_HF_STS | TXCRC_HF_STS   | TXDRO_P_HF_STS |
| Type  | W1C           | W1C           | W1C          | W1C          | W1C          | W1C           | W1C           | W1C          | W1C            | W1C           | W1C          | W1C          | W1C          | W1C          | W1C            | W1C            |
| Reset | 0             | 0             | 0            | 0            | 0            | 0             | 0             | 0            | 0              | 0             | 0            | 0            | 0            | 0            | 0              | 0              |

| Bit(s) | Name           | Description                                                                                      |
|--------|----------------|--------------------------------------------------------------------------------------------------|
| 18     | TXOCT_HF_STS   | <b>TX Octet Counter Half Full Status</b><br><br>0: False<br><br>1: True                          |
| 17     | TXL1024_HF_STS | <b>TX Packet Length above 1024 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 16     | TXL512_HF_STS  | <b>TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 15     | TXL256_HF_STS  | <b>TX Packet Length 256 ~ 511 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True  |
| 14     | TXL128_HF_STS  | <b>TX Packet Length 128 ~ 255 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True  |
| 13     | TXL65_HF_STS   | <b>TX Packet Length 65 ~ 127 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True   |
| 12     | TXL64_HF_STS   | <b>TX Packet Length 64 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True         |
| 11     | TXPAU_HF_STS   | <b>TX Pause Packet Counter Half Full Status</b><br><br>0: False                                  |



| Bit(s) | Name          | Description                                            |
|--------|---------------|--------------------------------------------------------|
|        |               | 1: True                                                |
| 10     | TXECOL_HF_STS | <b>TX Excessive Collision Counter Half Full Status</b> |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 9      | TXLCOL_HF_STS | <b>TX Late Collision Counter Half Full Status</b>      |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 8      | TXDFR_HF_STS  | <b>TX Deferred Counter Half Full Status</b>            |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 7      | TXMCOL_HF_STS | <b>TX Multiple Collision Counter Half Full Status</b>  |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 6      | TXSCOL_HF_STS | <b>TX Single Collision Counter Half Full Status</b>    |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 5      | TXCOL_HF_STS  | <b>TX Collision Event Counter Half Full Status</b>     |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 4      | TXBRD_HF_STS  | <b>TX Broadcast Counter Half Full Status</b>           |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 3      | TXMUL_HF_STS  | <b>TX Multicast Counter Half Full Status</b>           |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 2      | TXUNI_HF_STS  | <b>TX Unicast Counter Half Full Status</b>             |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 1      | TXCRC_HF_STS  | <b>TX CRC Counter Half Full Status</b>                 |
|        |               | 0: False                                               |
|        |               | 1: True                                                |
| 0      | TXDROP_HF_STS | <b>TX DROP Counter Half Full Status</b>                |

| Bit(s) | Name | Description |
|--------|------|-------------|
|        |      | 0: False    |
|        |      | 1: True     |

150246D4 RMIB HF\_STS\_P6 RX port MIB counter half full status of Port 6 00000000

| Bit   | 31            | 30            | 29           | 28           | 27           | 26           | 25           | 24           | 23           | 22           | 21           | 20           | 19            | 18           | 17             | 16             |
|-------|---------------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|---------------|--------------|----------------|----------------|
| Name  |               |               |              |              |              |              |              |              |              |              | RXARL_HF_STS | RXING_HF_STS | RXCTRL_HF_STS | RXOCT_HF_STS | RXL1024_HF_STS | RXL512_HF_STS  |
| Type  |               |               |              |              |              |              |              |              |              |              | W1C          | W1C          | W1C           | W1C          | W1C            | W1C            |
| Reset |               |               |              |              |              |              |              |              |              |              | 0            | 0            | 0             | 0            | 0              | 0              |
| Bit   | 15            | 14            | 13           | 12           | 11           | 10           | 9            | 8            | 7            | 6            | 5            | 4            | 3             | 2            | 1              | 0              |
| Name  | RXL256_HF_STS | RXL128_HF_STS | RXL65_HF_STS | RXL64_HF_STS | RXPAU_HF_STS | RXJAB_HF_STS | RXOVR_HF_STS | RXFRG_HF_STS | RXUND_HF_STS | RXCRC_HF_STS | RXALG_HF_STS | RXBRD_HF_STS | RXMUL_HF_STS  | RXUNI_HF_STS | RXFIL_HF_STS   | RXDRO_P_HF_STS |
| Type  | W1C           | W1C           | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C          | W1C           | W1C          | W1C            | W1C            |
| Reset | 0             | 0             | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0            | 0             | 0            | 0              | 0              |

| Bit(s) | Name           | Description                                                                                      |
|--------|----------------|--------------------------------------------------------------------------------------------------|
| 21     | RXARL_HF_STS   | <b>RX ARL Drop Counter Half Full Status</b><br><br>0: False<br><br>1: True                       |
| 20     | RXING_HF_STS   | <b>RX Ingress Drop Counter Half Full Status</b><br><br>0: False<br><br>1: True                   |
| 19     | RXCTRL_HF_STS  | <b>RX CTRL Drop Counter Half Full Status</b><br><br>0: False<br><br>1: True                      |
| 18     | RXOCT_HF_STS   | <b>RX Octet Counter Half Full Status</b><br><br>0: False<br><br>1: True                          |
| 17     | RXL1024_HF_STS | <b>RX Packet Length above 1024 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 16     | RXL512_HF_STS  | <b>RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 15     | RXL256_HF_STS  | <b>RX Packet Length 256 ~ 511 Bytes Counter Half Full Status</b><br><br>0: False<br><br>1: True  |
| 14     | RXL128_HF_STS  | <b>RX Packet Length 128 ~ 255 Bytes Counter Half Full Status</b><br><br>0: False                 |

| Bit(s) | Name         | Description                                                     |
|--------|--------------|-----------------------------------------------------------------|
|        |              | 1: True                                                         |
| 13     | RXL65_HF_STS | <b>RX Packet Length 65 ~ 127 Bytes Counter Half Full Status</b> |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 12     | RXL64_HF_STS | <b>RX Packet Length 64 Bytes Counter Half Full Status</b>       |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 11     | RXPAU_HF_STS | <b>RX Pause Packet Counter Half Full Status</b>                 |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 10     | RXJAB_HF_STS | <b>RX Jabber Error Counter Half Full Status</b>                 |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 9      | RXOVR_HF_STS | <b>RX Oversize Packet Counter Half Full Status</b>              |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 8      | RXFRG_HF_STS | <b>RX Fragment Error Counter Half Full Status</b>               |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 7      | RXUND_HF_STS | <b>RX Undersize Packet Counter Half Full Status</b>             |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 6      | RXCRC_HF_STS | <b>RX CRC ERROR Counter Half Full Status</b>                    |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 5      | RXALG_HF_STS | <b>RX Alignment Error Counter Half Full Status</b>              |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 4      | RXBRD_HF_STS | <b>RX Broadcast Counter Half Full Status</b>                    |
|        |              | 0: False                                                        |
|        |              | 1: True                                                         |
| 3      | RXMUL_HF_STS | <b>RX Multicast Counter Half Full Status</b>                    |

| Bit(s) | Name          | Description                                  |
|--------|---------------|----------------------------------------------|
|        |               | 0: False                                     |
|        |               | 1: True                                      |
| 2      | RXUNI_HF_STS  | <b>RX Unicast Counter Half Full Status</b>   |
|        |               | 0: False                                     |
|        |               | 1: True                                      |
| 1      | RXFIL_HF_STS  | <b>RX Filtering Counter Half Full Status</b> |
|        |               | 0: False                                     |
|        |               | 1: True                                      |
| 0      | RXDROP_HF_STS | <b>RX DROP Counter Half Full Status</b>      |
|        |               | 0: False                                     |
|        |               | 1: True                                      |

15024F00      AE0CNT      ACL event 0 counter      00000000

| Bit   | 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | AE0CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | AE0CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name   | Description                          |
|--------|--------|--------------------------------------|
| 31:0   | AE0CNT | Total number of ARL event 0 occurred |

15024F04      AE1CNT      ACL event 1 counter      00000000

| Bit   | 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | AE1CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | AE1CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name   | Description                          |
|--------|--------|--------------------------------------|
| 31:0   | AE1CNT | Total number of ARL event 1 occurred |

15024F08      AE2CNT      ACL event 2 counter      00000000

| Bit   | 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | AE2CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | AE2CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name   | Description                          |
|--------|--------|--------------------------------------|
| 31:0   | AE2CNT | Total number of ARL event 2 occurred |



15024F0C      AE3CNT      ACL event 3 counter      00000000

| Bit   | 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | AE3CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | AE3CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name   | Description                          |
|--------|--------|--------------------------------------|
| 31:0   | AE3CNT | Total number of ARL event 3 occurred |

15024F10      AE4CNT      ACL event 4 counter      00000000

| Bit   | 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | AE4CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | AE4CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name   | Description                          |
|--------|--------|--------------------------------------|
| 31:0   | AE4CNT | Total number of ARL event 4 occurred |

15024F14      AE5CNT      ACL event 5 counter      00000000

| Bit   | 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | AE5CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | AE5CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name   | Description                          |
|--------|--------|--------------------------------------|
| 31:0   | AE5CNT | Total number of ARL event 5 occurred |

15024F18      AE6CNT      ACL event 6 counter      00000000

| Bit   | 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | AE6CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | AE6CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name   | Description                          |
|--------|--------|--------------------------------------|
| 31:0   | AE6CNT | Total number of ARL event 6 occurred |

15024F1C      AE7CNT      ACL event 7 counter      00000000

| Bit   | 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | AE7CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | AE7CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name   | Description                          |
|--------|--------|--------------------------------------|
| 31:0   | AE7CNT | Total number of ARL event 7 occurred |

| 15024FE0 |            | MIBCCR |    |    |    | MIB counter control |    |    |                  |                 |                  |                 |    | 800000F0 |    |    |  |
|----------|------------|--------|----|----|----|---------------------|----|----|------------------|-----------------|------------------|-----------------|----|----------|----|----|--|
| Bit      | 31         | 30     | 29 | 28 | 27 | 26                  | 25 | 24 | 23               | 22              | 21               | 20              | 19 | 18       | 17 | 16 |  |
| Name     | MIB_ENABLE |        |    |    |    |                     |    |    |                  |                 |                  |                 |    |          |    |    |  |
| Type     | RW         |        |    |    |    |                     |    |    |                  |                 |                  |                 |    |          |    |    |  |
| Reset    | 1          |        |    |    |    |                     |    |    |                  |                 |                  |                 |    |          |    |    |  |
| Bit      | 15         | 14     | 13 | 12 | 11 | 10                  | 9  | 8  | 7                | 6               | 5                | 4               | 3  | 2        | 1  | 0  |  |
| Name     |            |        |    |    |    |                     |    |    | RX_OC_T_CNT_GOOD | RX_OC_T_CNT_BAD | TX_OC_T_CNT_GOOD | TX_OC_T_CNT_BAD |    |          |    |    |  |
| Type     |            |        |    |    |    |                     |    |    | RW               | RW              | RW               | RW              |    |          |    |    |  |
| Reset    |            |        |    |    |    |                     |    |    | 1                | 1               | 1                | 1               |    |          |    |    |  |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                                                                                    |
|--------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | MIB_ENABLE      | <p><b>Enable MIB counter.</b></p> <p>1'b0: Disable MIB counter and set all counter values to zero.</p> <p>1'b1: Enable MIB counter.</p>                                                                                                                                                                                                                        |
| 7      | RX_OCT_CNT_GOOD | <p><b>Enable octets count of good received packets.</b></p> <p>1'b0: Octets of good received packets are not counted in RX_OCT_L_CNT and RX_OCT_H_CNT.</p> <p>1'b1: Octets of good received packets are counted in RX_OCT_L_CNT and RX_OCT_H_CNT.</p>                                                                                                          |
| 6      | RX_OCT_CNT_BAD  | <p><b>Enable octets count of bad received packets</b></p> <p>1'b0: Octets of bad received packets are not counted in RX_OCT_L_CNT and RX_OCT_H_CNT.</p> <p>1'b1: Octets of bad received packets are counted in RX_OCT_L_CNT and RX_OCT_H_CNT.</p>                                                                                                              |
| 5      | TX_OCT_CNT_GOOD | <p><b>Enable octets count of good transmitted packets</b></p> <p>Good transmitted packets are frames transmitted successfully.</p> <p>1'b0: Octets of good transmitted packets are not counted in TX_OCT_L_CNT and TX_OCT_H_CNT.</p> <p>1'b1: Octets of good transmitted packets are counted in TX_OCT_L_CNT and TX_OCT_H_CNT.</p>                             |
| 4      | TX_OCT_CNT_BAD  | <p><b>Enable octets count of bad transmitted packets</b></p> <p>Bad transmitted packets are frames transmitted in collision with deliberately destroyed CRC.</p> <p>1'b0: Octets of bad transmitted packets are not counted in TX_OCT_L_CNT and TX_OCT_H_CNT.</p> <p>1'b1: Octets of bad transmitted packets are counted in TX_OCT_L_CNT and TX_OCT_H_CNT.</p> |

| 15024FE4 |            | AECR |    |    |    | ARL event counter control |    |    |    |    |    |    |    |    |    | 80000000 |  |
|----------|------------|------|----|----|----|---------------------------|----|----|----|----|----|----|----|----|----|----------|--|
| Bit      | 31         | 30   | 29 | 28 | 27 | 26                        | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16       |  |
| Name     | AEC_ENABLE |      |    |    |    |                           |    |    |    |    |    |    |    |    |    |          |  |
| Type     | RW         |      |    |    |    |                           |    |    |    |    |    |    |    |    |    |          |  |
| Reset    | 1          |      |    |    |    |                           |    |    |    |    |    |    |    |    |    |          |  |
| Bit      | 15         | 14   | 13 | 12 | 11 | 10                        | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0        |  |
| Name     |            |      |    |    |    |                           |    |    |    |    |    |    |    |    |    |          |  |
| Type     |            |      |    |    |    |                           |    |    |    |    |    |    |    |    |    |          |  |
| Reset    |            |      |    |    |    |                           |    |    |    |    |    |    |    |    |    |          |  |

| Bit(s) | Name       | Description                                                                                                                                                       |
|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | AEC_ENABLE | <p><b>Enable ARL event counter.</b></p> <p>1'b0: Disable ARL event counter function and set all counter value to zero.</p> <p>1'b1: Enable ARL event counter.</p> |

15024FE8      AEMIB\_HF\_STS      ARL event MIB counter half full status      00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23            | 22            | 21            | 20            | 19            | 18            | 17            | 16            |
|-------|----|----|----|----|----|----|----|----|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Name  |    |    |    |    |    |    |    |    |               |               |               |               |               |               |               |               |
| Type  |    |    |    |    |    |    |    |    |               |               |               |               |               |               |               |               |
| Reset |    |    |    |    |    |    |    |    |               |               |               |               |               |               |               |               |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7             | 6             | 5             | 4             | 3             | 2             | 1             | 0             |
| Name  |    |    |    |    |    |    |    |    | ARLEV7_HF_STS | ARLEV6_HF_STS | ARLEV5_HF_STS | ARLEV4_HF_STS | ARLEV3_HF_STS | ARLEV2_HF_STS | ARLEV1_HF_STS | ARLEV0_HF_STS |
| Type  |    |    |    |    |    |    |    |    | W1C           | W1C           | W1C           | W1C           | W1C           | W1C           | W1C           | W1C           |
| Reset |    |    |    |    |    |    |    |    | 0             | 0             | 0             | 0             | 0             | 0             | 0             | 0             |

| Bit(s) | Name          | Description                                                                    |
|--------|---------------|--------------------------------------------------------------------------------|
| 7      | ARLEV7_HF_STS | <b>ARL Event 7 MIB Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 6      | ARLEV6_HF_STS | <b>ARL Event 6 MIB Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 5      | ARLEV5_HF_STS | <b>ARL Event 5 MIB Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 4      | ARLEV4_HF_STS | <b>ARL Event 4 MIB Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 3      | ARLEV3_HF_STS | <b>ARL Event 3 MIB Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 2      | ARLEV2_HF_STS | <b>ARL Event 2 MIB Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 1      | ARLEV1_HF_STS | <b>ARL Event 1 MIB Counter Half Full Status</b><br><br>0: False<br><br>1: True |
| 0      | ARLEV0_HF_STS | <b>ARL Event 0 MIB Counter Half Full Status</b><br><br>0: False<br><br>1: True |



| Bit(s) | Name | Description |
|--------|------|-------------|
|--------|------|-------------|

15024FF0      MIBHF\_INT\_EN      Port/ARL MIB counter half full interrupt enable      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22          | 21 | 20 | 19          | 18          | 17          | 16          |
|-------|--------------|----|----|----|----|----|----|----|----|-------------|----|----|-------------|-------------|-------------|-------------|
| Name  | HFSTS_ARL_EN |    |    |    |    |    |    |    |    |             |    |    |             |             |             |             |
| Type  | RW           |    |    |    |    |    |    |    |    |             |    |    |             |             |             |             |
| Reset | 0            |    |    |    |    |    |    |    |    |             |    |    |             |             |             |             |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6           | 5  | 4  | 3           | 2           | 1           | 0           |
| Name  |              |    |    |    |    |    |    |    |    | HFSTS_P6_EN |    |    | HFSTS_P3_EN | HFSTS_P2_EN | HFSTS_P1_EN | HFSTS_P0_EN |
| Type  |              |    |    |    |    |    |    |    |    | RW          |    |    | RW          | RW          | RW          | RW          |
| Reset |              |    |    |    |    |    |    |    |    | 0           |    |    | 0           | 0           | 0           | 0           |

| Bit(s) | Name         | Description                                                                                                                                                                                                        |
|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | HFSTS_ARL_EN | <b>ARL MIB Half Full Interrupt Enable.</b><br><b>When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software.</b><br><br>0: Disable<br><br>1: Enable    |
| 6      | HFSTS_P6_EN  | <b>Port 6 MIB Half Full Interrupt Enable.</b><br><b>When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software.</b><br><br>0: Disable<br><br>1: Enable |
| 3      | HFSTS_P3_EN  | <b>Port 3 MIB Half Full Interrupt Enable.</b><br><b>When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software.</b><br><br>0: Disable<br><br>1: Enable |
| 2      | HFSTS_P2_EN  | <b>Port 2 MIB Half Full Interrupt Enable.</b><br><b>When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software.</b><br><br>0: Disable<br><br>1: Enable |
| 1      | HFSTS_P1_EN  | <b>Port 1 MIB Half Full Interrupt Enable.</b><br><b>When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software.</b><br><br>0: Disable<br><br>1: Enable |
| 0      | HFSTS_P0_EN  | <b>Port 0 MIB Half Full Interrupt Enable.</b><br><b>When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software.</b><br><br>0: Disable                  |

| Bit(s) | Name | Description |
|--------|------|-------------|
|        |      | 1: Enable   |

15024FF4      MIBHF\_INT\_STS      Port/ARL MIB counter half full interrupt status      00000000

| Bit   | 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22       | 21 | 20 | 19       | 18       | 17       | 16       |
|-------|-----------|----|----|----|----|----|----|----|----|----------|----|----|----------|----------|----------|----------|
| Name  | HFSTS_ARL |    |    |    |    |    |    |    |    |          |    |    |          |          |          |          |
| Type  | W1C       |    |    |    |    |    |    |    |    |          |    |    |          |          |          |          |
| Reset | 0         |    |    |    |    |    |    |    |    |          |    |    |          |          |          |          |
| Bit   | 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6        | 5  | 4  | 3        | 2        | 1        | 0        |
| Name  |           |    |    |    |    |    |    |    |    | HFSTS_P6 |    |    | HFSTS_P3 | HFSTS_P2 | HFSTS_P1 | HFSTS_P0 |
| Type  |           |    |    |    |    |    |    |    |    | W1C      |    |    | W1C      | W1C      | W1C      | W1C      |
| Reset |           |    |    |    |    |    |    |    |    | 0        |    |    | 0        | 0        | 0        | 0        |

| Bit(s) | Name      | Description                                                                 |
|--------|-----------|-----------------------------------------------------------------------------|
| 31     | HFSTS_ARL | <b>ARL MIB Half Full Interrupt Status</b><br><br>0: False<br><br>1: True    |
| 6      | HFSTS_P6  | <b>Port 6 MIB Half Full Interrupt Status</b><br><br>0: False<br><br>1: True |
| 3      | HFSTS_P3  | <b>Port 3 MIB Half Full Interrupt Status</b><br><br>0: False<br><br>1: True |
| 2      | HFSTS_P2  | <b>Port 2 MIB Half Full Interrupt Status</b><br><br>0: False<br><br>1: True |
| 1      | HFSTS_P1  | <b>Port 1 MIB Half Full Interrupt Status</b><br><br>0: False<br><br>1: True |
| 0      | HFSTS_P0  | <b>Port 0 MIB Half Full Interrupt Status</b><br><br>0: False<br><br>1: True |

| 15027000 | SYS_CTRL     |                |               |               |               |              |              |             | System control |              |              |               |    |    |             | 00000000     |
|----------|--------------|----------------|---------------|---------------|---------------|--------------|--------------|-------------|----------------|--------------|--------------|---------------|----|----|-------------|--------------|
| Bit      | 31           | 30             | 29            | 28            | 27            | 26           | 25           | 24          | 23             | 22           | 21           | 20            | 19 | 18 | 17          | 16           |
| Name     |              |                |               |               |               |              |              |             |                | ACL_TAB_INIT | MAC_TAB_INIT | VLAN_TAB_INIT |    |    |             | BMU_MEM_INIT |
| Type     |              |                |               |               |               |              |              |             |                | RO           | RO           | RO            |    |    |             | RO           |
| Reset    |              |                |               |               |               |              |              |             |                | 0            | 0            | 0             |    |    |             | 0            |
| Bit      | 15           | 14             | 13            | 12            | 11            | 10           | 9            | 8           | 7              | 6            | 5            | 4             | 3  | 2  | 1           | 0            |
| Name     | COL_BIST_STS | TRTCM_BIST_STS | MASK_BIST_STS | CTRL_BIST_STS | ADDR_BIST_STS | VLN_BIST_STS | MIB_BIST_STS | PB_BIST_STS | PL_BIST_STS    | FL_BIST_STS  | MBIST_CMP    | MBIST_EN      |    |    | SW_SYST_RST |              |
| Type     | RO           | RO             | RO            | RO            | RO            | RO           | RO           | RO          | RO             | RO           | RO           | RW            |    |    | W1S         |              |
| Reset    | 0            | 0              | 0             | 0             | 0             | 0            | 0            | 0           | 0              | 0            | 0            | 0             |    |    | 0           |              |

| Bit(s) | Name           | Description                                                                                                        |
|--------|----------------|--------------------------------------------------------------------------------------------------------------------|
| 22     | ACL_TAB_INIT   | <b>ACL Table Initialization Complete</b><br><br>1: Complete<br><br>0: Not Ready                                    |
| 21     | MAC_TAB_INIT   | <b>MAC Table Initialization Complete</b><br><br>1: Complete<br><br>0: Not Ready                                    |
| 20     | VLAN_TAB_INIT  | <b>VLAN Table Initialization Complete</b><br><br>1: Complete<br><br>0: Not Ready                                   |
| 16     | BMU_MEM_INIT   | <b>BMU Memory Initialization Complete</b><br><br>1: Complete<br><br>0: Not Ready                                   |
| 15     | COL_BIST_STS   | <b>COL BIST Status</b><br><br>This bit is valid only when MBIST_CMP is true.<br><br>1: OK<br><br>0: Failed         |
| 14     | TRTCM_BIST_STS | <b>TRTCM BIST Status</b><br><br>This bit is valid only when MBIST_CMP is true.<br><br>1: OK<br><br>0: Failed       |
| 13     | MASK_BIST_STS  | <b>Mask Memory BIST Status</b><br><br>This bit is valid only when MBIST_CMP is true.<br><br>1: OK<br><br>0: Failed |

| Bit(s) | Name          | Description                                                                                                                     |
|--------|---------------|---------------------------------------------------------------------------------------------------------------------------------|
| 12     | CTRL_BIST_STS | <b>CTRL Memory BIST Status</b><br><br>This bit is valid only when MBIST_CMP is true.<br><br>1: OK<br><br>0: Failed              |
| 11     | ADDR_BIST_STS | <b>Address Memory BIST Status</b><br><br>This bit is valid only when MBIST_CMP is true.<br><br>1: OK<br><br>0: Failed           |
| 10     | VLN_BIST_STS  | <b>VLAN Memory BIST Status</b><br><br>This bit is valid only when MBIST_CMP is true.<br><br>1: OK<br><br>0: Failed              |
| 9      | MIB_BIST_STS  | <b>MIB Memory BIST Status (Port0~Port6)</b><br><br>This bit is valid only when MBIST_CMP is true.<br><br>1: OK<br><br>0: Failed |
| 8      | PB_BIST_STS   | <b>Pack Buffer Memory BIST Status</b><br><br>This bit is valid only when MBIST_CMP is true.<br><br>1: OK<br><br>0: Failed       |
| 7      | PL_BIST_STS   | <b>Page Link Memory BIST Status</b><br><br>This bit is valid only when MBIST_CMP is true.<br><br>1: OK<br><br>0: Failed         |
| 6      | FL_BIST_STS   | <b>Frame Link Memory BIST Status</b><br><br>This bit is valid only when MBIST_CMP is true<br><br>1: OK<br><br>0: Failed         |
| 5      | MBIST_CMP     | <b>Memory BIST Complete</b><br><br>1: Complete<br><br>0: Idle or not finish yet                                                 |
| 4      | MBIST_EN      | <b>No used</b>                                                                                                                  |
| 1      | SW_SYS_RST    | <b>Software System Reset</b>                                                                                                    |

| Bit(s) | Name | Description                                                                                                                                                  |
|--------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |      | 1: Write 1 to reset switch's states to default (excluding PHY and registers). Please note that all MACs must be forced to link-down before setting this bit. |
|        |      | 0: Reset done/reset is inactive.                                                                                                                             |

**15027008      SYS\_INT\_EN      System interrupt enable      00000000**

| Bit   | 31         | 30                 | 29                  | 28                  | 27                | 26                | 25                  | 24                 | 23                 | 22                 | 21 | 20 | 19           | 18           | 17           | 16             |
|-------|------------|--------------------|---------------------|---------------------|-------------------|-------------------|---------------------|--------------------|--------------------|--------------------|----|----|--------------|--------------|--------------|----------------|
| Name  | ACL_INT_EN | ARL_SEC_TAG_INT_EN | ARL_SEC_VLAN_INT_EN | ARL_SEC_1G1X_INT_EN | ARL_PKT_BC_INT_EN | ARL_EQ_ERR_INT_EN | ARL_PKT_QERR_INT_EN | ARL_TBL_ERR_INT_EN | ARL_COL_FUL_INT_EN | ARL_COL_FUL_INT_EN |    |    |              | MIB_INT_EN   | BMU_INT_EN   | MAC_P_C_INT_EN |
| Type  | RW         | RW                 | RW                  | RW                  | RW                | RW                | RW                  | RW                 | RW                 | RW                 |    |    |              | RW           | RW           | RW             |
| Reset | 0          | 0                  | 0                   | 0                   | 0                 | 0                 | 0                   | 0                  | 0                  | 0                  |    |    |              | 0            | 0            | 0              |
| Bit   | 15         | 14                 | 13                  | 12                  | 11                | 10                | 9                   | 8                  | 7                  | 6                  | 5  | 4  | 3            | 2            | 1            | 0              |
| Name  |            |                    |                     |                     |                   |                   |                     |                    |                    | PHY6_LC_INTE       |    |    | PHY3_LC_INTE | PHY2_LC_INTE | PHY1_LC_INTE | PHY0_LC_INTE   |
| Type  |            |                    |                     |                     |                   |                   |                     |                    |                    | RW                 |    |    | RW           | RW           | RW           | RW             |
| Reset |            |                    |                     |                     |                   |                   |                     |                    |                    | 0                  |    |    | 0            | 0            | 0            | 0              |

| Bit(s) | Name                | Description                                                                          |
|--------|---------------------|--------------------------------------------------------------------------------------|
| 31     | ACL_INT_EN          | <b>ACL Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable                       |
| 30     | ARL_SEC_TAG_INT_EN  | <b>ARL Security Tag Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable          |
| 29     | ARL_SEC_VLAN_INT_EN | <b>ARL Security VLAN Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable         |
| 28     | ARL_SEC_1G1X_INT_EN | <b>ARL Security 1G Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable           |
| 27     | ARL_PKT_BC_INT_EN   | <b>ARL Broadcast Packet Drop Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable |
| 26     | ARL_EQ_ERR_INT_EN   | <b>ARL Enqueue Error Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable         |
| 25     | ARL_PKT_QERR_INT_EN | <b>ARL Packet Queue Error Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable    |
| 24     | ARL_TBL_ERR_INT_EN  | <b>ARL Table Error Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable           |



| Bit(s) | Name                    | Description                                                                                               |
|--------|-------------------------|-----------------------------------------------------------------------------------------------------------|
| 23     | ARL_COL_FULL_INT_EN     | <b>ARL Collision Pool Full Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable                        |
| 22     | ARL_COL_FULL_COL_INT_EN | <b>ARL Collision Pool Full and Collision Detected Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable |
| 18     | MIB_INT_EN              | <b>MIB Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable                                            |
| 17     | BMU_INT_EN              | <b>BMU Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable                                            |
| 16     | MAC_PC_INT_EN           | <b>MAC/Port Controller Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable                            |
| 6      | PHY6_LC_INTE            | <b>PHY 6 Link-up Change Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable                           |
| 3      | PHY3_LC_INTE            | <b>PHY 3 Link-up Change Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable                           |
| 2      | PHY2_LC_INTE            | <b>PHY 2 Link-up Change Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable                           |
| 1      | PHY1_LC_INTE            | <b>PHY 1 Link-up Change Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable                           |
| 0      | PHY0_LC_INTE            | <b>PHY 0 Link-up Change Interrupt Enable</b><br><br>1: Enable<br><br>0: Disable                           |

**1502700C      SYS\_INT\_STS      System interrupt status      00000000**

| Bit   | 31      | 30              | 29               | 28               | 27             | 26             | 25               | 24              | 23              | 22              | 21 | 20 | 19           | 18           | 17           | 16           |
|-------|---------|-----------------|------------------|------------------|----------------|----------------|------------------|-----------------|-----------------|-----------------|----|----|--------------|--------------|--------------|--------------|
| Name  | ACL_INT | ARL_SEC_TAG_INT | ARL_SEC_VLAN_INT | ARL_SEC_1G1X_INT | ARL_PKT_BC_INT | ARL_EQ_ERR_INT | ARL_PKT_QERR_INT | ARL_TBL_ERR_INT | ARL_COL_FUL_INT | ARL_COL_FUL_INT |    |    |              | MIB_INT      | BMU_INT      | MAC_P_C_INT  |
| Type  | W1C     | W1C             | W1C              | W1C              | W1C            | W1C            | W1C              | W1C             | W1C             | W1C             |    |    |              | W1C          | W1C          | W1C          |
| Reset | 0       | 0               | 0                | 0                | 0              | 0              | 0                | 0               | 0               | 0               |    |    |              | 0            | 0            | 0            |
| Bit   | 15      | 14              | 13               | 12               | 11             | 10             | 9                | 8               | 7               | 6               | 5  | 4  | 3            | 2            | 1            | 0            |
| Name  |         |                 |                  |                  |                |                |                  |                 |                 | PHY6_L_C_INT    |    |    | PHY3_L_C_INT | PHY2_L_C_INT | PHY1_L_C_INT | PHY0_L_C_INT |
| Type  |         |                 |                  |                  |                |                |                  |                 |                 | W1C             |    |    | W1C          | W1C          | W1C          | W1C          |
| Reset |         |                 |                  |                  |                |                |                  |                 |                 | 0               |    |    | 0            | 0            | 0            | 0            |

| Bit(s) | Name             | Description                                                                      |
|--------|------------------|----------------------------------------------------------------------------------|
| 31     | ACL_INT          | <b>ACL Interrupt Status</b><br><br>1: True<br><br>0: False                       |
| 30     | ARL_SEC_TAG_INT  | <b>ARL Security Tag Interrupt Status</b><br><br>1: True<br><br>0: False          |
| 29     | ARL_SEC_VLAN_INT | <b>ARL Security VLAN Interrupt Status</b><br><br>1: True<br><br>0: False         |
| 28     | ARL_SEC_1G1X_INT | <b>ARL Security 1G Interrupt Status</b><br><br>1: True<br><br>0: False           |
| 27     | ARL_PKT_BC_INT   | <b>ARL Broadcast Packet Drop Interrupt Status</b><br><br>1: True<br><br>0: False |
| 26     | ARL_EQ_ERR_INT   | <b>ARL Enqueue Error Status</b><br><br>1: True<br><br>0: False                   |
| 25     | ARL_PKT_QERR_INT | <b>ARL Packet Queue Error Status</b><br><br>1: True<br><br>0: False              |
| 24     | ARL_TBL_ERR_INT  | <b>ARL Table Error Interrupt Status</b><br><br>1: True<br><br>0: False           |

| Bit(s) | Name                 | Description                                                                                           |
|--------|----------------------|-------------------------------------------------------------------------------------------------------|
| 23     | ARL_COL_FULL_INT     | <b>ARL Collision Pool Full Interrupt Status</b><br><br>1: True<br><br>0: False                        |
| 22     | ARL_COL_FULL_COL_INT | <b>ARL Collision Pool Full and Collision Detected Interrupt Status</b><br><br>1: True<br><br>0: False |
| 18     | MIB_INT              | <b>MIB Interrupt Status</b><br><br>1: True<br><br>0: False                                            |
| 17     | BMU_INT              | <b>BMU Interrupt Status</b><br><br>1: True<br><br>0: False                                            |
| 16     | MAC_PC_INT           | <b>MAC/Port Controller Interrupt Status</b><br><br>1: True<br><br>0: False                            |
| 6      | PHY6_LC_INT          | <b>PHY 6 Link-up Change Interrupt Status</b><br><br>1: True<br><br>0: False                           |
| 3      | PHY3_LC_INT          | <b>PHY 3 Link-up Change Interrupt Status</b><br><br>1: True<br><br>0: False                           |
| 2      | PHY2_LC_INT          | <b>PHY 2 Link-up Change Interrupt Status</b><br><br>1: True<br><br>0: False                           |
| 1      | PHY1_LC_INT          | <b>PHY 1 Link-up Change Interrupt Status</b><br><br>1: True<br><br>0: False                           |
| 0      | PHY0_LC_INT          | <b>PHY 0 Link-up Change Interrupt Status</b><br><br>1: True<br><br>0: False                           |

15027014      **PMDC\_CFG**      **PMDC control register**      00000032

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24       | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----------|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    |    |    |          |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    |    |    |          |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    |    |    |          |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8        | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    |    |    | PMDC_CFG |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    |    |    | RW       |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    |    |    | 0        | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 0  |

| Bit(s) | Name     | Description                                                                                                                                                                                                                                                                                                                     |
|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8:0    | PMDC_CFG | <p><b>PHY MDC Clock Configuration</b></p> <p>It is used to configure the divider N for MDC clock frequency. The MDC clock is from 125MHz and is divided by N.</p> <p>Note: 1. MDC clock should not be over the MDC clock maximum value of PHY.</p> <p>2. MDC Clock will be disabled when the setting value is equals to 0~4</p> |

**15027018**      **PHY\_POLL**      **PHY polling and SMI master control register**      **007F8600**

| Bit   | 31             | 30                     | 29 | 28           | 27 | 26 | 25 | 24 | 23                    | 22          | 21 | 20          | 19 | 18 | 17 | 16 |
|-------|----------------|------------------------|----|--------------|----|----|----|----|-----------------------|-------------|----|-------------|----|----|----|----|
| Name  | PHY_AP_EN      |                        |    |              |    |    |    |    |                       | EEE_POLL_EN |    |             |    |    |    |    |
| Type  | RW             |                        |    |              |    |    |    |    |                       | RW          |    |             |    |    |    |    |
| Reset |                | 0                      | 0  | 0            | 0  | 0  | 0  | 0  |                       | 1           | 1  | 1           | 1  | 1  | 1  | 1  |
| Bit   | 15             | 14                     | 13 | 12           | 11 | 10 | 9  | 8  | 7                     | 6           | 5  | 4           | 3  | 2  | 1  | 0  |
| Name  | PHY_P<br>RE_EN | RX_TA<br>1_CHK<br>_OFF |    | PHY_END_ADDR |    |    |    |    | C45_AT<br>POLL_E<br>N |             |    | PHY_ST_ADDR |    |    |    |    |
| Type  | RW             | RW                     |    | RW           |    |    |    |    | RW                    |             |    | RW          |    |    |    |    |
| Reset | 1              | 0                      |    | 0            | 0  | 1  | 1  | 0  | 0                     |             |    | 0           | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                                                                                                                                                                                                               |
|--------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 30:24  | PHY_AP_EN      | <b>PHY Auto-Polling Enable</b><br><br>It indicates the updating PHY status by auto-polling or side-band signals.<br><br>bit 24 => port 0<br><br>bit 25 => port 1<br><br>bit 30 => port 6<br><br>1: PHY status obtained by Auto-polling<br><br>0: PHY status obtained by side-band signals |
| 22:16  | EEE_POLL_EN    | <b>PHY EEE Polling Enable</b><br><br>It indicates polling the EEE capability of each PHY.<br><br>bit 16 => port 0<br><br>bit 17 => port 1<br><br>bit 22 => port 6<br><br>1: Enable<br><br>0: Disable                                                                                      |
| 15     | PHY_PRE_EN     | <b>PHY Preamble Enable</b><br><br>It indicates that the SMI master will send preamble bits (32 bits) at each MDIO read/write transaction.<br><br>1: Enable<br><br>0: Disable<br><br>Note: This bit will affect both PHY auto-polling mode and PHY indirect access mode.                   |
| 14     | RX_TA1_CHK_OFF | <b>Disable the checking of RX_TA1 value.</b><br><br>1: Do not check the value of RX_TA1 state<br><br>0: Check the value of RX_TA1. If this value is not 0, it means that there is no response from PHYs, and all rx_data are invalid.                                                     |
| 12:8   | PHY_END_ADDR   | <b>PHY Polling End Address</b>                                                                                                                                                                                                                                                            |

| Bit(s) | Name          | Description                                                                                                                                                                                                                       |
|--------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7      | C45_ATPOLL_EN | <p>It indicates the end address of PHY auto-polling process.</p> <p><b>Clause 45 PHY Polling Enable</b></p> <p>Enable Clause 45 auto-polling for link status only.</p> <p>1: Enable (Clause 45)</p> <p>0: Disable (Clause 22)</p> |
| 4:0    | PHY_ST_ADDR   | <p><b>PHY Polling Start Address</b></p> <p>It indicates the start address of PHY auto-polling process.</p>                                                                                                                        |

1502701C      PHY\_IAC      PHY indirect access control      00090000

| Bit   | 31           | 30 | 29            | 28 | 27 | 26 | 25 | 24            | 23 | 22 | 21 | 20 | 19       | 18 | 17      | 16 |
|-------|--------------|----|---------------|----|----|----|----|---------------|----|----|----|----|----------|----|---------|----|
| Name  | PHY_ACS_ST   |    | MDIO_REG_ADDR |    |    |    |    | MDIO_PHY_ADDR |    |    |    |    | MDIO_CMD |    | MDIO_ST |    |
| Type  | W1S          |    | RW            |    |    |    |    | RW            |    |    |    |    | RW       |    | RW      |    |
| Reset | 0            |    | 0             | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 1        | 0  | 0       | 1  |
| Bit   | 15           | 14 | 13            | 12 | 11 | 10 | 9  | 8             | 7  | 6  | 5  | 4  | 3        | 2  | 1       | 0  |
| Name  | MDIO_RW_DATA |    |               |    |    |    |    |               |    |    |    |    |          |    |         |    |
| Type  | RW           |    |               |    |    |    |    |               |    |    |    |    |          |    |         |    |
| Reset | 0            | 0  | 0             | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0        | 0  | 0       | 0  |

| Bit(s) | Name          | Description                                                                                                                                                                                                                     |
|--------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | PHY_ACS_ST    | <b>PHY Access Start</b><br><br>Start the indirect accessing of PHY's register. When the accessing is completed, this bit will be self-cleared to 0.<br><br>1: Start<br><br>0: Idle or indirect accessing is completed           |
| 29:25  | MDIO_REG_ADDR | <b>MDIO Reg/Dev Address Fields</b><br><br>Configure the Register Address Field. (Clause 22)<br><br>Configure the Device Address Filed (Clause 45)                                                                               |
| 24:20  | MDIO_PHY_ADDR | <b>MDIO PHY Address Field</b><br><br>Configure the PHY address field.                                                                                                                                                           |
| 19:18  | MDIO_CMD      | <b>MDIO Command Field</b><br><br>Configure the MDIO command field.<br><br>2'b00: MDIO Address (Clause 45)<br><br>2'b01: MDIO Write<br><br>2'b10: MDIO Read (or Clause 45 - Continuous Read)<br><br>2'b11: MDIO Read (Clause 45) |
| 17:16  | MDIO_ST       | <b>MDIO Start Field</b><br><br>Configure the MDIO start field.<br><br>2'b00: Start (Clause 45)<br><br>2'b01: Start (Clause 22)<br><br>Others: Reserved                                                                          |
| 15:0   | MDIO_RW_DATA  | <b>MDIO Read/Write Data Field</b><br><br>It indicates the MDIO data field for Read/Write accessing.<br><br>When READ, this is used as MDIO read data (Read Only).<br><br>When Write, this is used as MDIO write data (R/W).     |

**15027020 PSR\_P3\_P0 PHY status register for Port 3 ~ Port 0 00000000**

| Bit   | 31           | 30             | 29            | 28         | 27            | 26           | 25 | 24            | 23           | 22             | 21            | 20         | 19            | 18           | 17 | 16            |
|-------|--------------|----------------|---------------|------------|---------------|--------------|----|---------------|--------------|----------------|---------------|------------|---------------|--------------|----|---------------|
| Name  | LP_AN_CAP_P3 | PHY_EEE1000_P3 | PHY_EEE100_P3 | PHY_XFC_P3 | PHY_DUPLEX_P3 | PHY_SPEED_P3 |    | PHY_LINKUP_P3 | LP_AN_CAP_P2 | PHY_EEE1000_P2 | PHY_EEE100_P2 | PHY_XFC_P2 | PHY_DUPLEX_P2 | PHY_SPEED_P2 |    | PHY_LINKUP_P2 |
| Type  | RO           | RO             | RO            | RO         | RO            | RO           |    | RO            | RO           | RO             | RO            | RO         | RO            | RO           |    | RO            |
| Reset | 0            | 0              | 0             | 0          | 0             | 0            | 0  | 0             | 0            | 0              | 0             | 0          | 0             | 0            | 0  | 0             |
| Bit   | 15           | 14             | 13            | 12         | 11            | 10           | 9  | 8             | 7            | 6              | 5             | 4          | 3             | 2            | 1  | 0             |
| Name  | LP_AN_CAP_P1 | PHY_EEE1000_P1 | PHY_EEE100_P1 | PHY_XFC_P1 | PHY_DUPLEX_P1 | PHY_SPEED_P1 |    | PHY_LINKUP_P1 | LP_AN_CAP_P0 | PHY_EEE1000_P0 | PHY_EEE100_P0 | PHY_XFC_P0 | PHY_DUPLEX_P0 | PHY_SPEED_P0 |    | PHY_LINKUP_P0 |
| Type  | RO           | RO             | RO            | RO         | RO            | RO           |    | RO            | RO           | RO             | RO            | RO         | RO            | RO           |    | RO            |
| Reset | 0            | 0              | 0             | 0          | 0             | 0            | 0  | 0             | 0            | 0              | 0             | 0          | 0             | 0            | 0  | 0             |

| Bit(s) | Name           | Description                                                                                                                                                                               |
|--------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | LP_AN_CAP_P3   | <b>Port 3 Link Partner Auto-Negotiation Capability</b><br><br>1: Link Partner supports AN<br><br>0: Link Partner does not support AN                                                      |
| 30     | PHY_EEE1000_P3 | <b>Port 3 EEE ability at 1000Base-T</b><br><br>1: Support EEE at 1000Base-T<br><br>0: Do not support 3000Base-T EEE                                                                       |
| 29     | PHY_EEE100_P3  | <b>Port 3 EEE ability at 100Base-Tx</b><br><br>1: Support EEE at 100Base-Tx<br><br>0: Do not support 300Base-Tx EEE                                                                       |
| 28     | PHY_XFC_P3     | <b>Port 3 MAC Flow Control Status</b><br><br>1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames).<br><br>0: Do not support MAC flow control |
| 27     | PHY_DUPLEX_P3  | <b>Port 3 PHY Duplex status</b><br><br>1: Full-duplex<br><br>0: Half-duplex                                                                                                               |
| 26:25  | PHY_SPEED_P3   | <b>Port 3 PHY Speed Status</b><br><br>2'b00: 10Mbps<br><br>2'b01: 100Mbps<br><br>2'b10: 1000Mbps<br><br>2'b11: Reserved                                                                   |
| 24     | PHY_LINKUP_P3  | <b>Port 3 PHY Link Status</b><br><br>1: Link-up<br><br>0: Link-down                                                                                                                       |



| Bit(s) | Name           | Description                                                                                                                                                                       |
|--------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23     | LP_AN_CAP_P2   | <b>Port 2 Link Partner Auto-Negotiation Capability</b><br>1: Link Partner supports AN<br>0: Link Partner does not support AN                                                      |
| 22     | PHY_EEE1000_P2 | <b>Port 2 EEE ability at 1000Base-T</b><br>1: Support EEE at 1000Base-T<br>0: Do not support 2000Base-T EEE                                                                       |
| 21     | PHY_EEE100_P2  | <b>Port 2 EEE ability at 100Base-Tx</b><br>1: Support EEE at 100Base-Tx<br>0: Do not support 200Base-Tx EEE                                                                       |
| 20     | PHY_XFC_P2     | <b>Port 2 MAC Flow Control Status</b><br>1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames).<br>0: Do not support MAC flow control |
| 19     | PHY_DUPLEX_P2  | <b>Port 2 PHY Duplex status</b><br>1: Full-duplex<br>0: Half-duplex                                                                                                               |
| 18:17  | PHY_SPEED_P2   | <b>Port 2 PHY Speed Status</b><br>2'b00: 10Mbps<br>2'b01: 100Mbps<br>2'b10: 1000Mbps<br>2'b11: Reserved                                                                           |
| 16     | PHY_LINKUP_P2  | <b>Port 2 PHY Link Status</b><br>1: Link-up<br>0: Link-down                                                                                                                       |
| 15     | LP_AN_CAP_P1   | <b>Port 1 Link Partner Auto-Negotiation Capability</b><br>1: Link Partner supports AN<br>0: Link Partner does not support AN                                                      |
| 14     | PHY_EEE1000_P1 | <b>Port 1 EEE ability at 1000Base-T</b><br>1: Support EEE at 1000Base-T<br>0: Do not support 1000Base-T EEE                                                                       |
| 13     | PHY_EEE100_P1  | <b>Port 1 EEE ability at 100Base-Tx</b><br>1: Support EEE at 100Base-Tx<br>0: Do not support 100Base-Tx EEE                                                                       |
| 12     | PHY_XFC_P1     | <b>Port 1 MAC Flow Control Status</b>                                                                                                                                             |

| Bit(s) | Name           | Description                                                                                                                                                                                                                                                                                                                                                                                                                               |
|--------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                | 1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames).                                                                                                                                                                                                                                                                                                                                        |
|        |                | 0: Do not support MAC flow control                                                                                                                                                                                                                                                                                                                                                                                                        |
| 11     | PHY_DUPLEX_P1  | <b>Port 1 PHY Duplex status</b><br>1: Full-duplex<br>0: Half-duplex                                                                                                                                                                                                                                                                                                                                                                       |
| 10:9   | PHY_SPEED_P1   | <b>Port 1 PHY Speed Status</b><br>2'b00: 10Mbps<br>2'b01: 100Mbps<br>2'b10: 1000Mbps<br>2'b11: Reserved                                                                                                                                                                                                                                                                                                                                   |
| 8      | PHY_LINKUP_P1  | <b>Port 1 PHY Link Status</b><br>1: Link-up<br>0: Link-down                                                                                                                                                                                                                                                                                                                                                                               |
| 7      | LP_AN_CAP_P0   | <b>Port 0 Link Partner Auto-Negotiation Capability</b><br>1: Link Partner is Auto-negotiable<br>0: Link Partner is not Auto-negotiable<br><br>Note: While PHY is link-up but LP_AN_CAP is false, it means that the current link-up state is generated by Parallel Detection. So the current phy_speed and phy_duplex bits are updated from PHY's Link Partner advertisement register (REG 05). No speed or duplex validity is guaranteed. |
| 6      | PHY_EEE1000_P0 | <b>Port 0 EEE ability at 1000Base-T</b><br>1: Support EEE at 1000Base-T<br>0: Do not support 1000Base-T EEE                                                                                                                                                                                                                                                                                                                               |
| 5      | PHY_EEE100_P0  | <b>Port 0 EEE ability at 100Base-Tx</b><br>1: Support EEE at 100Base-Tx<br>0: Do not support 100Base-Tx EEE                                                                                                                                                                                                                                                                                                                               |
| 4      | PHY_XFC_P0     | <b>Port 0 MAC Flow Control Status</b><br>1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames).<br>0: Do not support MAC flow control                                                                                                                                                                                                                                                         |
| 3      | PHY_DUPLEX_P0  | <b>Port 0 PHY Duplex status</b><br>1: Full-duplex<br>0: Half-duplex                                                                                                                                                                                                                                                                                                                                                                       |
| 2:1    | PHY_SPEED_P0   | <b>Port 0 PHY Speed Status</b>                                                                                                                                                                                                                                                                                                                                                                                                            |

| Bit(s) | Name          | Description                   |
|--------|---------------|-------------------------------|
|        |               | 2'b00: 10Mbps                 |
|        |               | 2'b01: 100Mbps                |
|        |               | 2'b10: 1000Mbps               |
|        |               | 2'b11: Reserved               |
| 0      | PHY_LINKUP_P0 | <b>Port 0 PHY Link Status</b> |
|        |               | 1: Link-up                    |
|        |               | 0: Link-down                  |

**15027024 PSR\_P6\_P4 PHY status register for Port 6 ~ Port 4 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23           | 22             | 21            | 20         | 19            | 18           | 17 | 16            |
|-------|----|----|----|----|----|----|----|----|--------------|----------------|---------------|------------|---------------|--------------|----|---------------|
| Name  |    |    |    |    |    |    |    |    | LP_AN_CAP_P6 | PHY_EEE1000_P6 | PHY_EEE100_P6 | PHY_XFC_P6 | PHY_DUPLEX_P6 | PHY_SPEED_P6 |    | PHY_LINKUP_P6 |
| Type  |    |    |    |    |    |    |    |    | RO           | RO             | RO            | RO         | RO            | RO           |    | RO            |
| Reset |    |    |    |    |    |    |    |    | 0            | 0              | 0             | 0          | 0             | 0            | 0  | 0             |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7            | 6              | 5             | 4          | 3             | 2            | 1  | 0             |
| Name  |    |    |    |    |    |    |    |    |              |                |               |            |               |              |    |               |
| Type  |    |    |    |    |    |    |    |    |              |                |               |            |               |              |    |               |
| Reset |    |    |    |    |    |    |    |    |              |                |               |            |               |              |    |               |

| Bit(s) | Name           | Description                                                                                                                                                                               |
|--------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23     | LP_AN_CAP_P6   | <b>Port 6 Link Partner Auto-Negotiation Capability</b><br><br>1: Link Partner supports AN<br><br>0: Link Partner does not support AN                                                      |
| 22     | PHY_EEE1000_P6 | <b>Port 6 EEE ability at 1000Base-T</b><br><br>1: Support EEE at 1000Base-T<br><br>0: Do not support 6000Base-T EEE                                                                       |
| 21     | PHY_EEE100_P6  | <b>Port 6 EEE ability at 100Base-Tx</b><br><br>1: Support EEE at 100Base-Tx<br><br>0: Do not support 600Base-Tx EEE                                                                       |
| 20     | PHY_XFC_P6     | <b>Port 6 MAC Flow Control Status</b><br><br>1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames).<br><br>0: Do not support MAC flow control |
| 19     | PHY_DUPLEX_P6  | <b>Port 6 PHY Duplex status</b><br><br>1: Full-duplex<br><br>0: Half-duplex                                                                                                               |
| 18:17  | PHY_SPEED_P6   | <b>Port 6 PHY Speed Status</b><br><br>2'b00: 10Mbps<br>2'b01: 100Mbps<br>2'b10: 1000Mbps<br>2'b11: Reserved                                                                               |
| 16     | PHY_LINKUP_P6  | <b>Port 6 PHY Link Status</b><br><br>1: Link-up<br><br>0: Link-down                                                                                                                       |

15027028 PAUSE\_CAP\_P6\_P0MAC pause TX/RX capability register for Port 6 ~  
Port 0

00000000

| Bit   | 31 | 30 | 29              | 28              | 27 | 26 | 25 | 24 | 23              | 22              | 21              | 20              | 19              | 18              | 17              | 16              |
|-------|----|----|-----------------|-----------------|----|----|----|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name  |    |    |                 |                 |    |    |    |    |                 |                 |                 |                 |                 |                 |                 |                 |
| Type  |    |    |                 |                 |    |    |    |    |                 |                 |                 |                 |                 |                 |                 |                 |
| Reset |    |    |                 |                 |    |    |    |    |                 |                 |                 |                 |                 |                 |                 |                 |
| Bit   | 15 | 14 | 13              | 12              | 11 | 10 | 9  | 8  | 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |
| Name  |    |    | MAC_R<br>XFC_P6 | MAC_T<br>XFC_P6 |    |    |    |    | MAC_R<br>XFC_P3 | MAC_T<br>XFC_P3 | MAC_R<br>XFC_P2 | MAC_T<br>XFC_P2 | MAC_R<br>XFC_P1 | MAC_T<br>XFC_P1 | MAC_R<br>XFC_P0 | MAC_T<br>XFC_P0 |
| Type  |    |    | RO              | RO              |    |    |    |    | RO              | RO              | RO              | RO              | RO              | RO              | RO              | RO              |
| Reset |    |    | 0               | 0               |    |    |    |    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               |

| Bit(s) | Name        | Description                                                                                                              |
|--------|-------------|--------------------------------------------------------------------------------------------------------------------------|
| 13     | MAC_RXFC_P6 | <b>Port 6 MAC Rx Pause Capability</b><br>1: Support MAC Rx Pause Capability<br>0: Do not support MAC Rx Pause Capability |
| 12     | MAC_TXFC_P6 | <b>Port 6 MAC Tx Pause Capability</b><br>1: Support MAC Tx Pause Capability<br>0: Do not support MAC Tx Pause Capability |
| 7      | MAC_RXFC_P3 | <b>Port 3 MAC Rx Pause Capability</b><br>1: Support MAC Rx Pause Capability<br>0: Do not support MAC Rx Pause Capability |
| 6      | MAC_TXFC_P3 | <b>Port 3 MAC Tx Pause Capability</b><br>1: Support MAC Tx Pause Capability<br>0: Do not support MAC Tx Pause Capability |
| 5      | MAC_RXFC_P2 | <b>Port 2 MAC Rx Pause Capability</b><br>1: Support MAC Rx Pause Capability<br>0: Do not support MAC Rx Pause Capability |
| 4      | MAC_TXFC_P2 | <b>Port 2 MAC Tx Pause Capability</b><br>1: Support MAC Tx Pause Capability<br>0: Do not support MAC Tx Pause Capability |
| 3      | MAC_RXFC_P1 | <b>Port 1 MAC Rx Pause Capability</b><br>1: Support MAC Rx Pause Capability<br>0: Do not support MAC Rx Pause Capability |
| 2      | MAC_TXFC_P1 | <b>Port 1 MAC Tx Pause Capability</b><br>1: Support MAC Tx Pause Capability<br>0: Do not support MAC Tx Pause Capability |

| Bit(s) | Name        | Description                                                                                                                      |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------|
| 1      | MAC_RXFC_P0 | <b>Port 0 MAC Rx Pause Capability</b><br><br>1: Support MAC Rx Pause Capability<br><br>0: Do not support MAC Rx Pause Capability |
| 0      | MAC_TXFC_P0 | <b>Port 0 MAC Tx Pause Capability</b><br><br>1: Support MAC Tx Pause Capability<br><br>0: Do not support MAC Tx Pause Capability |

15027124 **EEPR\_STS** **EEPROM status register** 00000001

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17               | 16         |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------|------------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |            |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |            |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |            |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1                | 0          |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    | EP_AL_DONE_2_SMI | EP_AL_DONE |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RO               | RO         |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                | 1          |

| Bit(s) | Name             | Description                                                                                                                                                                                                                                 |
|--------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1      | EP_AL_DONE_2_SMI | <b>After EEPROM auto-load, whether switch to SMI nor not</b><br><br>1: Detected ROM code command with "0xFFFC" address, EEPROM I2C master SCL/SDA pins switch to SMI MDC/MDIO slave function<br><br>0: Keeps EEPROM I2C master SCL/SDA pins |
| 0      | EP_AL_DONE       | <b>EEPROM auto-load status indicator</b><br><br>1: DONE<br><br>0: Not yet                                                                                                                                                                   |

## 4.3 Frame Engine

### 4.3.1 Register Definition

Module name: FE Base address: (+0x15100000)

| Address  | Name                     | Width | Register Function                         |
|----------|--------------------------|-------|-------------------------------------------|
| 15100000 | <u>FE_GLO_CFG</u>        | 32    | Frame Engine global configuration         |
| 15100004 | <u>FE_RST_GLO</u>        | 32    | Frame Engine global reset                 |
| 15100008 | <u>FE_INT_STATUS</u>     | 32    | Frame Engine interrupt status             |
| 1510000C | <u>FE_INT_ENABLE</u>     | 32    | Frame Engine interrupt enable             |
| 15100010 | <u>FE_FOE_TS_T</u>       | 32    | Frame Engine timestamp                    |
| 15100014 | <u>FE_IPV6_EXT</u>       | 32    | Frame Engine IPv6 extension header        |
| 15100018 | <u>FE_RATE_COMP</u>      | 32    | Frame Engine rate limit compensation      |
| 15100020 | <u>FE_INT_GRP</u>        | 32    | Frame Engine interrupt group              |
| 15100024 | <u>FE_GLO_CFG2</u>       | 32    | Frame Engine global configuration part2   |
| 15100028 | <u>FE_INT_STATUS2</u>    | 32    | Frame Engine interrupt status part2       |
| 1510002C | <u>FE_INT_ENABLE2</u>    | 32    | Frame Engine interrupt enable part2       |
| 151000C0 | <u>PSE_IQ_REV_RLS1</u>   | 32    | PSE input queue reservation release part1 |
| 151000C4 | <u>PSE_IQ_REV_RLS2</u>   | 32    | PSE input queue reservation release part2 |
| 151000C8 | <u>PSE_IQ_REV_RLS3</u>   | 32    | PSE input queue reservation release part3 |
| 151000CC | <u>PSE_IQ_REV_RLS4</u>   | 32    | PSE input queue reservation release part4 |
| 151000D0 | <u>PSE_IQ_REV_RLS5</u>   | 32    | PSE input queue reservation release part5 |
| 151000D4 | <u>PSE_IQ_REV_RLS6</u>   | 32    | PSE input queue reservation release part6 |
| 151000D8 | <u>PSE_IQ_REV_RLS7</u>   | 32    | PSE input queue reservation release part7 |
| 151000DC | <u>PSE_IQ_REV_RLS8</u>   | 32    | PSE input queue reservation release part8 |
| 151000E0 | <u>PSE_TDM_TBL8</u>      | 32    | PSE TDM arbiter table8                    |
| 151000E4 | <u>PSE_TDM_TBL9</u>      | 32    | PSE TDM arbiter table9                    |
| 151000E8 | <u>PSE_TDM_TBL10</u>     | 32    | PSE TDM arbiter table10                   |
| 151000EC | <u>PSE_TDM_TBL11</u>     | 32    | PSE TDM arbiter table11                   |
| 151000F0 | <u>PSE_TDM_TBL12</u>     | 32    | PSE TDM arbiter table12                   |
| 151000F4 | <u>PSE_TDM_TBL13</u>     | 32    | PSE TDM arbiter table13                   |
| 151000F8 | <u>PSE_TDM_TBL14</u>     | 32    | PSE TDM arbiter table14                   |
| 151000FC | <u>PSE_TDM_TBL15</u>     | 32    | PSE TDM arbiter table15                   |
| 15100100 | <u>PSE_FQFC_CFG1</u>     | 32    | PSE free queue flow control part1         |
| 15100104 | <u>PSE_FQFC_CFG2</u>     | 32    | PSE free queue flow control part2         |
| 1510010C | <u>PSE_DUMMY_REQ</u>     | 32    | PSE last FreeQ page request control       |
| 15100110 | <u>PSE_PPE0_DROP</u>     | 32    | PPE0 drop packet enable port              |
| 15100114 | <u>PSE_PPE1_DROP</u>     | 32    | PPE1 drop packet enable port              |
| 15100118 | <u>PSE_PPE2_DROP</u>     | 32    | PPE2 drop packet enable port              |
| 1510011C | <u>PSE_DUMMY_FLG_CLR</u> | 32    | Per-Port PSE dummy page flag clear        |
| 15100120 | <u>PSE_DUMMY_FLG</u>     | 32    | Per-Port PSE dummy page flag              |
| 1510012C | <u>PSE_IQ_REV9</u>       | 32    | PSE input queue reservation part9         |
| 15100130 | <u>FE_GDM_RXID1</u>      | 32    | FE GDM RXID control 1                     |
| 15100134 | <u>FE_GDM_RXID2</u>      | 32    | FE GDM RXID control 2                     |
| 15100140 | <u>PSE_IQ_REV1</u>       | 32    | PSE input queue reservation part1         |
| 15100144 | <u>PSE_IQ_REV2</u>       | 32    | PSE input queue reservation part2         |
| 15100148 | <u>PSE_IQ_REV3</u>       | 32    | PSE input queue reservation part3         |
| 1510014C | <u>PSE_IQ_REV4</u>       | 32    | PSE input queue reservation part4         |
| 15100150 | <u>PSE_IQ_REV5</u>       | 32    | PSE input queue reservation part5         |



| Address  | Name                | Width | Register Function                   |
|----------|---------------------|-------|-------------------------------------|
| 15100154 | <u>PSE IQ REV6</u>  | 32    | PSE input queue reservation part6   |
| 15100158 | <u>PSE IQ REV7</u>  | 32    | PSE input queue reservation part7   |
| 1510015C | <u>PSE IQ REV8</u>  | 32    | PSE input queue reservation part8   |
| 15100160 | <u>PSE OQ TH1</u>   | 32    | PSE output queue threshold part1    |
| 15100164 | <u>PSE OQ TH2</u>   | 32    | PSE output queue threshold part2    |
| 15100168 | <u>PSE OQ TH3</u>   | 32    | PSE output queue threshold part3    |
| 1510016C | <u>PSE OQ TH4</u>   | 32    | PSE output queue threshold part4    |
| 15100170 | <u>PSE OQ TH5</u>   | 32    | PSE output queue threshold part5    |
| 15100174 | <u>PSE OQ TH6</u>   | 32    | PSE output queue threshold part6    |
| 15100178 | <u>PSE OQ TH7</u>   | 32    | PSE output queue threshold part7    |
| 1510017C | <u>PSE OQ TH8</u>   | 32    | PSE output queue threshold part8    |
| 15100180 | <u>PSE IQ STA1</u>  | 32    | PSE input queue status part1        |
| 15100184 | <u>PSE IQ STA2</u>  | 32    | PSE input queue status part2        |
| 15100188 | <u>PSE IQ STA3</u>  | 32    | PSE input queue status part3        |
| 1510018C | <u>PSE IQ STA4</u>  | 32    | PSE input queue status part4        |
| 15100190 | <u>PSE IQ STA5</u>  | 32    | PSE input queue status part5        |
| 15100194 | <u>PSE IQ STA6</u>  | 32    | PSE input queue status part6        |
| 15100198 | <u>PSE IQ STA7</u>  | 32    | PSE input queue status part7        |
| 1510019C | <u>PSE IQ STA8</u>  | 32    | PSE input queue status part8        |
| 151001A0 | <u>PSE OQ STA1</u>  | 32    | PSE output queue status part1       |
| 151001A4 | <u>PSE OQ STA2</u>  | 32    | PSE output queue status part2       |
| 151001A8 | <u>PSE OQ STA3</u>  | 32    | PSE output queue status part3       |
| 151001AC | <u>PSE OQ STA4</u>  | 32    | PSE output queue status part4       |
| 151001B0 | <u>PSE OQ STA5</u>  | 32    | PSE output queue status part5       |
| 151001B4 | <u>PSE OQ STA6</u>  | 32    | PSE output queue status part6       |
| 151001B8 | <u>PSE OQ STA7</u>  | 32    | PSE output queue status part7       |
| 151001BC | <u>PSE OQ STA8</u>  | 32    | PSE output queue status part8       |
| 151001C0 | <u>PSE TDM TBL0</u> | 32    | PSE TDM arbiter table0              |
| 151001C4 | <u>PSE TDM TBL1</u> | 32    | PSE TDM arbiter table1              |
| 151001C8 | <u>PSE TDM TBL2</u> | 32    | PSE TDM arbiter table2              |
| 151001CC | <u>PSE TDM TBL3</u> | 32    | PSE TDM arbiter table3              |
| 151001D0 | <u>PSE TDM TBL4</u> | 32    | PSE TDM arbiter table4              |
| 151001D4 | <u>PSE TDM TBL5</u> | 32    | PSE TDM arbiter table5              |
| 151001D8 | <u>PSE TDM TBL6</u> | 32    | PSE TDM arbiter table6              |
| 151001DC | <u>PSE TDM TBL7</u> | 32    | PSE TDM arbiter table7              |
| 151001E0 | <u>PSE SP CFG0</u>  | 32    | PSE strict priority configuration 0 |
| 151001E4 | <u>PSE SP CFG1</u>  | 32    | PSE strict priority configuration 1 |
| 151001E8 | <u>PSE TDM CFG</u>  | 32    | PSE TDM arbiter configuration       |
| 151001EC | <u>CDM SRAM RD</u>  | 32    | CDM CR read 8K SRAM                 |
| 15100200 | <u>FE CDM1 DBG1</u> | 32    | FE CDM1 debug part1                 |
| 15100204 | <u>FE CDM1 DBG2</u> | 32    | FE CDM1 debug part2                 |
| 15100208 | <u>FE CDM2 DBG1</u> | 32    | FE CDM2 debug part1                 |
| 1510020C | <u>FE CDM2 DBG2</u> | 32    | FE CDM2 debug part2                 |
| 15100210 | <u>FE GDM1 DBG1</u> | 32    | FE GDM1 debug part1                 |
| 15100214 | <u>FE GDM1 DBG2</u> | 32    | FE GDM1 debug part2                 |
| 15100218 | <u>FE GDM2 DBG1</u> | 32    | FE GDM2 debug part1                 |
| 1510021C | <u>FE GDM2 DBG2</u> | 32    | FE GDM2 debug part2                 |
| 15100220 | <u>FE CDM1 FSM</u>  | 32    | FE CDM1 FSM status                  |
| 15100224 | <u>FE CDM2 FSM</u>  | 32    | FE CDM2 FSM status                  |

| Address  | Name                       | Width | Register Function                        |
|----------|----------------------------|-------|------------------------------------------|
| 15100228 | <u>FE_GDM1_FSM</u>         | 32    | FE GDM1 FSM status                       |
| 1510022C | <u>FE_GDM2_FSM</u>         | 32    | FE GDM2 FSM status                       |
| 15100230 | <u>FE_CDM3_DBG1</u>        | 32    | FE CDM3 debug part1                      |
| 15100234 | <u>FE_CDM3_DBG2</u>        | 32    | FE CDM3 debug part2                      |
| 15100238 | <u>FE_CDM3_FSM</u>         | 32    | FE CDM3 FSM status                       |
| 15100240 | <u>FE_PSE_FREE</u>         | 32    | PSE free page Count                      |
| 15100244 | <u>FE_DROP_FQ</u>          | 32    | FE packet drop by free queue             |
| 15100248 | <u>FE_DROP_FC</u>          | 32    | FE packet drop by flow control           |
| 1510024C | <u>FE_DROP_PPE1</u>        | 32    | FE packet drop by PPE1                   |
| 15100250 | <u>FE_DROP_PD_6</u>        | 32    | FE packet drop by Port 6 disabled        |
| 15100254 | <u>FE_DROP_PD_5</u>        | 32    | FE packet drop by Port 5 disabled        |
| 15100258 | <u>FE_DROP_PD_4</u>        | 32    | FE packet drop by Port 4 disabled        |
| 1510025C | <u>FE_DROP_PD_3</u>        | 32    | FE packet drop by Port 3 disabled        |
| 15100260 | <u>FE_DROP_PD_2</u>        | 32    | FE packet drop by Port 2 disabled        |
| 15100264 | <u>FE_DROP_PD_1</u>        | 32    | FE packet drop by Port 1 disabled        |
| 15100268 | <u>FE_DROP_PD_0</u>        | 32    | FE packet drop by Port 0 disabled        |
| 15100270 | <u>FE_DROP_PD_14</u>       | 32    | FE packet drop by Port 14 disabled       |
| 15100274 | <u>FE_DROP_PD_13</u>       | 32    | FE packet drop by Port 13 disabled       |
| 15100278 | <u>FE_DROP_PD_12</u>       | 32    | FE packet drop by Port 12 disabled       |
| 1510027C | <u>FE_DROP_PD_11</u>       | 32    | FE packet drop by Port 11 disabled       |
| 15100280 | <u>FE_DROP_PD_10</u>       | 32    | FE packet drop by Port 10 disabled       |
| 15100284 | <u>FE_DROP_PD_9</u>        | 32    | FE packet drop by Port 9 disabled        |
| 15100288 | <u>FE_DROP_PD_8</u>        | 32    | FE packet drop by Port 8 disabled        |
| 1510028C | <u>FE_DROP_PD_7</u>        | 32    | FE packet drop by Port 7 disabled        |
| 15100290 | <u>FE_CDM4_DBG1</u>        | 32    | FE CDM4 debug part1                      |
| 15100294 | <u>FE_CDM4_DBG2</u>        | 32    | FE CDM4 debug part2                      |
| 15100298 | <u>FE_CDM4_FSM</u>         | 32    | FE CDM4 FSM status                       |
| 1510029C | <u>FE_DROP_PPE2</u>        | 32    | FE packet drop by PPE2                   |
| 151002A0 | <u>FE_DROP_PPE0</u>        | 32    | FE packet drop by PPE0                   |
| 151002A4 | <u>FE_DROP_PPE0_P0_R01</u> | 32    | FE packet to Port0 Ring 0&1 drop by PPE0 |
| 151002A8 | <u>FE_DROP_PPE0_P0_R23</u> | 32    | FE packet to Port0 Ring 2&3 drop by PPE0 |
| 151002AC | <u>FE_DROP_PPE0_P5</u>     | 32    | FE packet to Port5 drop by PPE0          |
| 151002B0 | <u>FE_DROP_PPE0_P8</u>     | 32    | FE packet to Port8 drop by PPE0          |
| 151002B4 | <u>FE_DROP_PPE0_P9</u>     | 32    | FE packet to Port9 drop by PPE0          |
| 151002B8 | <u>FE_DROP_PPE0_P10</u>    | 32    | FE packet to Port10 drop by PPE0         |
| 151002BC | <u>FE_DROP_PPE0_P11</u>    | 32    | FE packet to Port11 drop by PPE0         |
| 151002C0 | <u>FE_DROP_PPE0_P12</u>    | 32    | FE packet to Port12 drop by PPE0         |
| 151002C4 | <u>FE_DROP_PPE1_P0_R01</u> | 32    | FE packet to Port0 Ring 0&1 drop by PPE1 |
| 151002C8 | <u>FE_DROP_PPE1_P0_R23</u> | 32    | FE packet to Port0 Ring 2&3 drop by PPE1 |
| 151002CC | <u>FE_DROP_PPE1_P5</u>     | 32    | FE packet to Port5 drop by PPE1          |
| 151002D0 | <u>FE_DROP_PPE1_P8</u>     | 32    | FE packet to Port8 drop by PPE1          |
| 151002D4 | <u>FE_DROP_PPE1_P9</u>     | 32    | FE packet to Port9 drop by PPE1          |
| 151002D8 | <u>FE_DROP_PPE1_P10</u>    | 32    | FE packet to Port10 drop by PPE1         |
| 151002DC | <u>FE_DROP_PPE1_P11</u>    | 32    | FE packet to Port11 drop by PPE1         |
| 151002E0 | <u>FE_DROP_PPE1_P12</u>    | 32    | FE packet to Port12 drop by PPE1         |
| 151002E4 | <u>FE_DROP_PPE0_P13</u>    | 32    | FE packet to Port13 drop by PPE0         |
| 151002E8 | <u>FE_DROP_PPE0_P14</u>    | 32    | FE packet to Port14 drop by PPE0         |
| 151002EC | <u>FE_DROP_PPE1_P13</u>    | 32    | FE packet to Port13 drop by PPE1         |
| 151002F0 | <u>FE_DROP_PPE1_P14</u>    | 32    | FE packet to Port14 drop by PPE1         |

| Address  | Name                        | Width | Register Function               |
|----------|-----------------------------|-------|---------------------------------|
| 15100310 | <u>FE_CDM5_DBG1</u>         | 32    | FE CDM5 debug part1             |
| 15100314 | <u>FE_CDM5_DBG2</u>         | 32    | FE CDM5 debug part2             |
| 15100318 | <u>FE_CDM5_FSM</u>          | 32    | FE CDM5 FSM status              |
| 15100320 | <u>FE_CDM6_DBG1</u>         | 32    | FE CDM6 debug part1             |
| 15100324 | <u>FE_CDM6_DBG2</u>         | 32    | FE CDM6 debug part2             |
| 15100328 | <u>FE_CDM6_FSM</u>          | 32    | FE CDM6 FSM status              |
| 15100330 | <u>FE_CDM7_DBG1</u>         | 32    | FE CDM7 debug part1             |
| 15100334 | <u>FE_CDM7_DBG2</u>         | 32    | FE CDM7 debug part2             |
| 15100338 | <u>FE_CDM7_FSM</u>          | 32    | FE CDM7 FSM status              |
| 1510033C | <u>FE_CDM8_DBG1</u>         | 32    | FE CDM8 debug part1             |
| 15100340 | <u>FE_CDM8_DBG2</u>         | 32    | FE CDM8 debug part2             |
| 15100344 | <u>FE_CDM8_FSM</u>          | 32    | FE CDM8 FSM status              |
| 15100348 | <u>FE_CDM9_DBG1</u>         | 32    | FE CDM9 debug part1             |
| 1510034C | <u>FE_CDM9_DBG2</u>         | 32    | FE CDM9 debug part2             |
| 15100350 | <u>FE_CDM9_FSM</u>          | 32    | FE CDM9 FSM status              |
| 1510038C | <u>FE_CDM3_FS_DFIFO</u>     | 32    | FE CDM3 FS data path FIFO debug |
| 15100390 | <u>FE_CDM3_FS_INFO_FIFO</u> | 32    | FE CDM3 FS info path FIFO debug |
| 15100394 | <u>FE_CDM3_TS_DFIFO</u>     | 32    | FE CDM3 TS data path FIFO debug |
| 15100398 | <u>FE_CDM3_TS_INFO_FIFO</u> | 32    | FE CDM3 TS info path FIFO debug |
| 1510039C | <u>FE_CDM4_FS_DFIFO</u>     | 32    | FE CDM4 FS data path FIFO debug |
| 151003A0 | <u>FE_CDM4_FS_INFO_FIFO</u> | 32    | FE CDM4 FS info path FIFO debug |
| 151003A4 | <u>FE_CDM4_TS_DFIFO</u>     | 32    | FE CDM4 TS data path FIFO debug |
| 151003A8 | <u>FE_CDM4_TS_INFO_FIFO</u> | 32    | FE CDM4 TS info path FIFO debug |
| 151003AC | <u>FE_CDM5_FS_DFIFO</u>     | 32    | FE CDM5 FS data path FIFO debug |
| 151003B0 | <u>FE_CDM5_FS_INFO_FIFO</u> | 32    | FE CDM5 FS info path FIFO debug |
| 151003B4 | <u>FE_CDM5_TS_DFIFO</u>     | 32    | FE CDM5 TS data path FIFO debug |
| 151003B8 | <u>FE_CDM5_TS_INFO_FIFO</u> | 32    | FE CDM5 TS info path FIFO debug |
| 151003BC | <u>FE_CDM6_FS_DFIFO</u>     | 32    | FE CDM6 FS data path FIFO debug |
| 151003C0 | <u>FE_CDM6_FS_INFO_FIFO</u> | 32    | FE CDM6 FS info path FIFO debug |
| 151003C4 | <u>FE_CDM6_TS_DFIFO</u>     | 32    | FE CDM6 TS data path FIFO debug |
| 151003C8 | <u>FE_CDM6_TS_INFO_FIFO</u> | 32    | FE CDM6 TS info path FIFO debug |
| 151003CC | <u>FE_CDM7_FS_DFIFO</u>     | 32    | FE CDM7 FS data path FIFO debug |
| 151003D0 | <u>FE_CDM7_FS_INFO_FIFO</u> | 32    | FE CDM7 FS info path FIFO debug |
| 151003D4 | <u>FE_CDM7_TS_DFIFO</u>     | 32    | FE CDM7 TS data path FIFO debug |
| 151003D8 | <u>FE_CDM7_TS_INFO_FIFO</u> | 32    | FE CDM7 TS info path FIFO debug |
| 151003DC | <u>FE_CDM1_1_FIFO_DBG1</u>  | 32    | FE CDM1_1 FIFO status debug1    |
| 151003F0 | <u>FE_CDM1_1_FIFO_DBG2</u>  | 32    | FE CDM1_1 FIFO status debug2    |
| 151003F4 | <u>FE_CDM2_FIFO_DBG1</u>    | 32    | FE CDM2 FIFO status debug1      |
| 151003F8 | <u>FE_CDM2_FIFO_DBG2</u>    | 32    | FE CDM2 FIFO status debug2      |
| 15100400 | <u>CDMP_IG_CTRL</u>         | 32    | CDM ingress control             |
| 15100404 | <u>CDMP_EG_CTRL</u>         | 32    | CDM egress control              |
| 15100408 | <u>CDMP_PPE_GEN</u>         | 32    | CDM PPPoE generation            |
| 15100500 | <u>GDM1_IG_CTRL</u>         | 32    | GDM ingress control             |
| 15100504 | <u>GDM1_EG_CTRL</u>         | 32    | GDM egress control              |
| 15100508 | <u>GDM1_MAC_LSB</u>         | 32    | GDM MY_MAC address LSB          |
| 1510050C | <u>GDM1_MAC_MSB</u>         | 32    | GDM MY_MAC address MSB          |
| 15100510 | <u>GDM1_VLAN_GEN</u>        | 32    | GDM VLAN generation             |
| 15100520 | <u>GDM1_DOS_CFG_0</u>       | 32    | GDM DOS configuration 0         |
| 15100524 | <u>GDM1_DOS_CFG_1</u>       | 32    | GDM DOS configuration 1         |

| Address  | Name                  | Width | Register Function                |
|----------|-----------------------|-------|----------------------------------|
| 15100528 | <u>GDM1_DOS_CFG_2</u> | 32    | GDM DOS configuration 2          |
| 1510052C | <u>GDM1_DOS_CFG_3</u> | 32    | GDM DOS configuration 3          |
| 15100540 | <u>GDM3_IG_CTRL</u>   | 32    | GDM ingress control              |
| 15100544 | <u>GDM3_EG_CTRL</u>   | 32    | GDM egress control               |
| 15100548 | <u>GDM3_MAC_LSB</u>   | 32    | GDM MY_MAC address LSB           |
| 1510054C | <u>GDM3_MAC_MSB</u>   | 32    | GDM MY_MAC address MSB           |
| 15100550 | <u>GDM3_VLAN_GEN</u>  | 32    | GDM VLAN generation              |
| 15100560 | <u>GDM3_DOS_CFG_0</u> | 32    | GDM DOS configuration 0          |
| 15100564 | <u>GDM3_DOS_CFG_1</u> | 32    | GDM DOS configuration 1          |
| 15100568 | <u>GDM3_DOS_CFG_2</u> | 32    | GDM DOS configuration 2          |
| 1510056C | <u>GDM3_DOS_CFG_3</u> | 32    | GDM DOS configuration 3          |
| 15100600 | <u>GLO_MEM_CFG</u>    | 32    | Global memory configurations     |
| 15100604 | <u>GLO_MEM_CTRL</u>   | 32    | Global memory interface control  |
| 15100608 | <u>GLO_MEM_DATA0</u>  | 32    | Global memory data 0             |
| 1510060C | <u>GLO_MEM_DATA1</u>  | 32    | Global memory data 1             |
| 15100610 | <u>GLO_MEM_DATA2</u>  | 32    | Global memory data 2             |
| 15100614 | <u>GLO_MEM_DATA3</u>  | 32    | Global memory data 3             |
| 15100618 | <u>GLO_MEM_DATA4</u>  | 32    | Global memory data 4             |
| 1510061C | <u>GLO_MEM_DATA5</u>  | 32    | Global memory data 5             |
| 15100620 | <u>GLO_MEM_DATA6</u>  | 32    | Global memory data 6             |
| 15100624 | <u>GLO_MEM_DATA7</u>  | 32    | Global memory data 7             |
| 15100628 | <u>GLO_MEM_DATA8</u>  | 32    | Global memory data 8             |
| 1510062C | <u>GLO_MEM_DATA9</u>  | 32    | Global memory data 9             |
| 15100C00 | <u>PFC_CFG_0</u>      | 32    | PFC GMAC1 input priority ReMap 0 |
| 15100C04 | <u>PFC_CFG_1</u>      | 32    | PFC GMAC1 input priority ReMap 1 |
| 15100C08 | <u>PFC_CFG_2</u>      | 32    | PFC GMAC2 input priority ReMap 0 |
| 15100C0C | <u>PFC_CFG_3</u>      | 32    | PFC GMAC2 input priority ReMap 1 |
| 15100C20 | <u>PFC_CFG_2_3</u>    | 32    | PFC GMAC3 input priority ReMap 0 |
| 15100C24 | <u>PFC_CFG_3_3</u>    | 32    | PFC GMAC3 input priority ReMap 1 |
| 15100C60 | <u>PFC_CFG_5</u>      | 32    | PFC QDMA input priority ReMap 0  |
| 15100C64 | <u>PFC_CFG_6</u>      | 32    | PFC QDMA input priority ReMap 1  |
| 15100C68 | <u>PFC_CFG_7</u>      | 32    | PFC QDMA input priority ReMap 2  |
| 15100C6C | <u>PFC_CFG_8</u>      | 32    | PFC QDMA input priority ReMap 3  |
| 15100C70 | <u>PFC_CFG_9</u>      | 32    | PFC QDMA input priority ReMap 4  |
| 15100C74 | <u>PFC_CFG_10</u>     | 32    | PFC QDMA input priority ReMap 5  |
| 15100C78 | <u>PFC_CFG_11</u>     | 32    | PFC QDMA input priority ReMap 6  |
| 15100C7C | <u>PFC_CFG_12</u>     | 32    | PFC QDMA input priority ReMap 7  |
| 15100C80 | <u>PFC_CFG_13</u>     | 32    | PFC QDMA input priority ReMap 8  |
| 15100C84 | <u>PFC_CFG_14</u>     | 32    | PFC QDMA input priority ReMap 9  |
| 15100C88 | <u>PFC_CFG_15</u>     | 32    | PFC QDMA input priority ReMap 10 |
| 15100C8C | <u>PFC_CFG_16</u>     | 32    | PFC QDMA input priority ReMap 11 |
| 15100C90 | <u>PFC_CFG_17</u>     | 32    | PFC QDMA input priority ReMap 12 |
| 15100C94 | <u>PFC_CFG_18</u>     | 32    | PFC QDMA input priority ReMap 13 |
| 15100C98 | <u>PFC_CFG_19</u>     | 32    | PFC QDMA input priority ReMap 14 |
| 15100C9C | <u>PFC_CFG_20</u>     | 32    | PFC QDMA input priority ReMap 15 |
| 15100CA0 | <u>PFC_CFG_21</u>     | 32    | PFC QDMA input priority ReMap 16 |
| 15100CA4 | <u>PFC_CFG_22</u>     | 32    | PFC QDMA input priority ReMap 17 |
| 15100CA8 | <u>PFC_CFG_23</u>     | 32    | PFC QDMA input priority ReMap 18 |
| 15100CAC | <u>PFC_CFG_24</u>     | 32    | PFC QDMA input priority ReMap 19 |

| Address  | Name                | Width | Register Function                 |
|----------|---------------------|-------|-----------------------------------|
| 15100CB0 | <u>PFC_CFG_25</u>   | 32    | PFC QDMA input priority ReMap 20  |
| 15100CB4 | <u>PFC_CFG_26</u>   | 32    | PFC QDMA input priority ReMap 21  |
| 15100CB8 | <u>PFC_CFG_27</u>   | 32    | PFC QDMA input priority ReMap 22  |
| 15100CBC | <u>PFC_CFG_28</u>   | 32    | PFC QDMA input priority ReMap 23  |
| 15100CC0 | <u>PFC_CFG_29</u>   | 32    | PFC QDMA input priority ReMap 24  |
| 15100CC4 | <u>PFC_CFG_30</u>   | 32    | PFC QDMA input priority ReMap 25  |
| 15100CC8 | <u>PFC_CFG_31</u>   | 32    | PFC QDMA input priority ReMap 26  |
| 15100CCC | <u>PFC_CFG_32</u>   | 32    | PFC QDMA input priority ReMap 27  |
| 15100CD0 | <u>PFC_CFG_33</u>   | 32    | PFC QDMA input priority ReMap 28  |
| 15100CD4 | <u>PFC_CFG_34</u>   | 32    | PFC QDMA input priority ReMap 29  |
| 15100CD8 | <u>PFC_CFG_35</u>   | 32    | PFC QDMA input priority ReMap 30  |
| 15100CDC | <u>PFC_CFG_36</u>   | 32    | PFC QDMA input priority ReMap 31  |
| 15100D60 | <u>PFC_CFG_37</u>   | 32    | PFC GMAC1 output priority ReMap 0 |
| 15100D64 | <u>PFC_CFG_38</u>   | 32    | PFC GMAC1 output priority ReMap 1 |
| 15100D68 | <u>PFC_CFG_39</u>   | 32    | PFC GMAC2 output priority ReMap 0 |
| 15100D6C | <u>PFC_CFG_40</u>   | 32    | PFC GMAC2 output priority ReMap 1 |
| 15100D90 | <u>PFC_CFG_39_3</u> | 32    | PFC GMAC3 output priority ReMap 0 |
| 15100D94 | <u>PFC_CFG_40_3</u> | 32    | PFC GMAC3 output priority ReMap 1 |
| 15100DA0 | <u>PFC_CFG_43</u>   | 32    | PFC QDMA output priority ReMap 0  |
| 15100DA4 | <u>PFC_CFG_44</u>   | 32    | PFC QDMA output priority ReMap 1  |
| 15100DA8 | <u>PFC_CFG_45</u>   | 32    | PFC QDMA output priority ReMap 2  |
| 15100DAC | <u>PFC_CFG_46</u>   | 32    | PFC QDMA output priority ReMap 3  |
| 15100DB0 | <u>PFC_CFG_47</u>   | 32    | PFC QDMA output priority ReMap 4  |
| 15100DB4 | <u>PFC_CFG_48</u>   | 32    | PFC QDMA output priority ReMap 5  |
| 15100DB8 | <u>PFC_CFG_49</u>   | 32    | PFC QDMA output priority ReMap 6  |
| 15100DBC | <u>PFC_CFG_50</u>   | 32    | PFC QDMA output priority ReMap 7  |
| 15100DC0 | <u>PFC_CFG_51</u>   | 32    | PFC QDMA output priority ReMap 8  |
| 15100DC4 | <u>PFC_CFG_52</u>   | 32    | PFC QDMA output priority ReMap 9  |
| 15100DC8 | <u>PFC_CFG_53</u>   | 32    | PFC QDMA output priority ReMap 10 |
| 15100DCC | <u>PFC_CFG_54</u>   | 32    | PFC QDMA output priority ReMap 11 |
| 15100DD0 | <u>PFC_CFG_55</u>   | 32    | PFC QDMA output priority ReMap 12 |
| 15100DD4 | <u>PFC_CFG_56</u>   | 32    | PFC QDMA output priority ReMap 13 |
| 15100DD8 | <u>PFC_CFG_57</u>   | 32    | PFC QDMA output priority ReMap 14 |
| 15100DDC | <u>PFC_CFG_58</u>   | 32    | PFC QDMA output priority ReMap 15 |
| 15100DE0 | <u>PFC_CFG_59</u>   | 32    | PFC QDMA output priority ReMap 16 |
| 15100DE4 | <u>PFC_CFG_60</u>   | 32    | PFC QDMA output priority ReMap 17 |
| 15100DE8 | <u>PFC_CFG_61</u>   | 32    | PFC QDMA output priority ReMap 18 |
| 15100DEC | <u>PFC_CFG_62</u>   | 32    | PFC QDMA output priority ReMap 19 |
| 15100DF0 | <u>PFC_CFG_63</u>   | 32    | PFC QDMA output priority ReMap 20 |
| 15100DF4 | <u>PFC_CFG_64</u>   | 32    | PFC QDMA output priority ReMap 21 |
| 15100DF8 | <u>PFC_CFG_65</u>   | 32    | PFC QDMA output priority ReMap 22 |
| 15100DFC | <u>PFC_CFG_66</u>   | 32    | PFC QDMA output priority ReMap 23 |
| 15100E00 | <u>PFC_CFG_67</u>   | 32    | PFC QDMA output priority ReMap 24 |
| 15100E04 | <u>PFC_CFG_68</u>   | 32    | PFC QDMA output priority ReMap 25 |
| 15100E08 | <u>PFC_CFG_69</u>   | 32    | PFC QDMA output priority ReMap 26 |
| 15100E0C | <u>PFC_CFG_70</u>   | 32    | PFC QDMA output priority ReMap 27 |
| 15100E10 | <u>PFC_CFG_71</u>   | 32    | PFC QDMA output priority ReMap 28 |
| 15100E14 | <u>PFC_CFG_72</u>   | 32    | PFC QDMA output priority ReMap 29 |
| 15100E18 | <u>PFC_CFG_73</u>   | 32    | PFC QDMA output priority ReMap 30 |

| Address  | Name                    | Width | Register Function                 |
|----------|-------------------------|-------|-----------------------------------|
| 15100E1C | <u>PFC_CFG_74</u>       | 32    | PFC QDMA output priority ReMap 31 |
| 15100EA0 | <u>PFC_CFG_75</u>       | 32    | PFC enable control to GMAC1       |
| 15100EA4 | <u>PFC_CFG_76</u>       | 32    | PFC enable control to GMAC1       |
| 15100EA8 | <u>PFC_CFG_77</u>       | 32    | PFC enable control to GMAC2       |
| 15100EAC | <u>PFC_CFG_78</u>       | 32    | PFC enable control to GMAC2       |
| 15100EB0 | <u>PFC_CFG_79</u>       | 32    | PFC enable control to GMAC3       |
| 15100EB4 | <u>PFC_CFG_80</u>       | 32    | PFC enable control to GMAC3       |
| 15100EC0 | <u>PFC_CFG_83</u>       | 32    | PFC enable control to QDMA        |
| 15100EF0 | <u>PFC_CFG_85</u>       | 32    | PFC debug 0                       |
| 15100EF4 | <u>PFC_CFG_86</u>       | 32    | PFC debug 1                       |
| 15100EF8 | <u>PFC_CFG_87</u>       | 32    | PFC debug 2                       |
| 15100EFC | <u>PFC_CFG_88</u>       | 32    | PFC debug 3                       |
| 15100F00 | <u>PFC_CFG_89</u>       | 32    | PFC debug 4                       |
| 15100F04 | <u>PFC_CFG_90</u>       | 32    | PFC configuration                 |
| 15101400 | <u>CDMQ_IG_CTRL</u>     | 32    | CDM VLAN control                  |
| 15101404 | <u>CDMQ_EG_CTRL</u>     | 32    | CDM egress control                |
| 15101408 | <u>CDMQ_PPP_GEN</u>     | 32    | CDM PPPoE generation              |
| 15101500 | <u>GDM2_IG_CTRL</u>     | 32    | GDM ingress control               |
| 15101504 | <u>GDM2_EG_CTRL</u>     | 32    | GDM egress control                |
| 15101508 | <u>GDM2_MAC_LSB</u>     | 32    | GDM MY_MAC address LSB            |
| 1510150C | <u>GDM2_MAC_MSB</u>     | 32    | GDM MY_MAC address MSB            |
| 15101510 | <u>GDM2_VLAN_GEN</u>    | 32    | GDM VLAN generation               |
| 15101514 | <u>GDM2_FILTER_CTRL</u> | 32    | GDM filter control                |
| 15101518 | <u>GDM2_VIDF01</u>      | 32    | GDM VID filter control 01         |
| 1510151C | <u>GDM2_VIDF23</u>      | 32    | GDM VID filter control 23         |
| 15101520 | <u>GDM2_DOS_CFG_0</u>   | 32    | GDM DOS configuration 0           |
| 15101524 | <u>GDM2_DOS_CFG_1</u>   | 32    | GDM DOS configuration 1           |
| 15101528 | <u>GDM2_DOS_CFG_2</u>   | 32    | GDM DOS configuration 2           |
| 1510152C | <u>GDM2_DOS_CFG_3</u>   | 32    | GDM DOS configuration 3           |
| 15101534 | <u>CDM2_THRES</u>       | 32    | CDM2 threshold                    |
| 15101600 | <u>CDMW0_IG_CTRL</u>    | 32    | CDM VLAN control                  |
| 15101604 | <u>CDMW0_EG_CTRL</u>    | 32    | CDM egress control                |
| 15101608 | <u>CDMW0_PPP_GEN</u>    | 32    | CDM PPPoE generation              |
| 15101610 | <u>CDMW1_IG_CTRL</u>    | 32    | CDM VLAN control                  |
| 15101614 | <u>CDMW1_EG_CTRL</u>    | 32    | CDM egress control                |
| 15101618 | <u>CDMW1_PPP_GEN</u>    | 32    | CDM PPPoE generation              |
| 1510161C | <u>CDMT_PPP_GEN</u>     | 32    | CDM PPPoE generation              |
| 15101620 | <u>CDME0_IG_CTRL</u>    | 32    | CDM VLAN control                  |
| 15101624 | <u>CDME0_EG_CTRL</u>    | 32    | CDM egress control                |
| 15101628 | <u>CDME0_PPP_GEN</u>    | 32    | CDM PPPoE generation              |
| 1510162C | <u>CDMT_EG_CTRL</u>     | 32    | CDM egress control                |
| 15101630 | <u>CDME1_IG_CTRL</u>    | 32    | CDM VLAN control                  |
| 15101634 | <u>CDME1_EG_CTRL</u>    | 32    | CDM egress control                |
| 15101638 | <u>CDME1_PPP_GEN</u>    | 32    | CDM PPPoE generation              |
| 1510163C | <u>CDMT_IG_CTRL</u>     | 32    | CDM VLAN control                  |
| 15101640 | <u>CDMM_IG_CTRL</u>     | 32    | CDM VLAN control                  |
| 15101644 | <u>CDMM_EG_CTRL</u>     | 32    | CDM egress control                |
| 15101648 | <u>CDMM_PPP_GEN</u>     | 32    | CDM PPPoE generation              |
| 1510164C | <u>CDM_THRES0</u>       | 32    | CDM threshold 0                   |



| Address  | Name                      | Width | Register Function                    |
|----------|---------------------------|-------|--------------------------------------|
| 15101650 | <u>CDM_THRES1</u>         | 32    | CDM threshold 1                      |
| 15101654 | <u>CDM_THRES2</u>         | 32    | CDM threshold 2                      |
| 15101658 | <u>CDM_THRES3</u>         | 32    | CDM threshold 3                      |
| 1510165C | <u>CDM_THRES4</u>         | 32    | CDM threshold 4                      |
| 151016A8 | <u>CDMW2_IG_CTRL</u>      | 32    | CDM VLAN control                     |
| 151016AC | <u>CDMW2_EG_CTRL</u>      | 32    | CDM egress control                   |
| 151016B0 | <u>CDMW2_PPP_GEN</u>      | 32    | CDM PPPoE generation                 |
| 151016B4 | <u>CDME2_IG_CTRL</u>      | 32    | CDM VLAN control                     |
| 151016B8 | <u>CDME2_EG_CTRL</u>      | 32    | CDM egress control                   |
| 151016BC | <u>CDME2_PPP_GEN</u>      | 32    | CDM PPPoE generation                 |
| 151016C0 | <u>CDMEIP_IG_CTRL</u>     | 32    | CDM VLAN control                     |
| 151016C4 | <u>CDMEIP_EG_CTRL</u>     | 32    | CDM egress control                   |
| 151016C8 | <u>CDMEIP_PPP_GEN</u>     | 32    | CDM PPPoE generation                 |
| 15102800 | <u>RSS_GLO_CFG</u>        | 32    | RSS global configuration             |
| 15102820 | <u>RSS_HASH_KEY_DW0</u>   | 32    | RSS hash Key DW0                     |
| 15102824 | <u>RSS_HASH_KEY_DW1</u>   | 32    | RSS hash Key DW1                     |
| 15102828 | <u>RSS_HASH_KEY_DW2</u>   | 32    | RSS hash Key DW2                     |
| 1510282C | <u>RSS_HASH_KEY_DW3</u>   | 32    | RSS hash Key DW3                     |
| 15102830 | <u>RSS_HASH_KEY_DW4</u>   | 32    | RSS hash Key DW4                     |
| 15102834 | <u>RSS_HASH_KEY_DW5</u>   | 32    | RSS hash Key DW5                     |
| 15102838 | <u>RSS_HASH_KEY_DW6</u>   | 32    | RSS hash Key DW6                     |
| 1510283C | <u>RSS_HASH_KEY_DW7</u>   | 32    | RSS hash Key DW7                     |
| 15102840 | <u>RSS_HASH_KEY_DW8</u>   | 32    | RSS hash Key DW8                     |
| 15102844 | <u>RSS_HASH_KEY_DW9</u>   | 32    | RSS hash Key DW9                     |
| 15102848 | <u>RSS_LFB_CFG0</u>       | 32    | RSS low flow balance configuration 0 |
| 15102850 | <u>RSS_INDR_TABLE_DW0</u> | 32    | RSS indirection table DW0            |
| 15102854 | <u>RSS_INDR_TABLE_DW1</u> | 32    | RSS indirection table DW1            |
| 15102858 | <u>RSS_INDR_TABLE_DW2</u> | 32    | RSS indirection table DW2            |
| 1510285C | <u>RSS_INDR_TABLE_DW3</u> | 32    | RSS indirection table DW3            |
| 15102860 | <u>RSS_INDR_TABLE_DW4</u> | 32    | RSS indirection table DW4            |
| 15102864 | <u>RSS_INDR_TABLE_DW5</u> | 32    | RSS indirection table DW5            |
| 15102868 | <u>RSS_INDR_TABLE_DW6</u> | 32    | RSS indirection table DW6            |
| 1510286C | <u>RSS_INDR_TABLE_DW7</u> | 32    | RSS indirection table DW7            |

**15100000 FE\_GLO\_CFG Frame Engine global configuration 810000B0**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-----------------|----|----|----|------------------|----|----|----|
| <b>Name</b>  | <b>EXT_TPID</b>   |    |    |    |    |    |    |    |                 |    |    |    |                  |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    |                 |    |    |    |                  |    |    |    |
| <b>Reset</b> | 1                 | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0               | 0  | 0  | 0  | 0                | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| <b>Name</b>  | <b>LINK_DWN_0</b> |    |    |    |    |    |    |    | <b>L2_SPACE</b> |    |    |    | <b>INF_SPACE</b> |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW              |    |    |    | RW               |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1               | 0  | 1  | 1  | 0                | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                           |
|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | EXT_TPID   | <b>Extended VLAN TPID</b><br><br>User-defined TPID except for 0x8100, 0x88a8.<br><br>[note] This TPID field is used by CDM/GDM RX direction.                                                                                                          |
| 15:8   | LINK_DWN_0 | <b>Disable PSE Port 0~7</b><br><br>When PSE port is not valid on the Frame Engine, user is suggested to disable the corresponding port.                                                                                                               |
| 7:4    | L2_SPACE   | <b>L2 space</b><br><br>The space unit is 8 bytes.                                                                                                                                                                                                     |
| 3:0    | INF_SPACE  | <b>PKT_INFO space</b><br><br>The space unit is 8 bytes.<br><br>[Note1*] Per received packet has already occupied 8 bytes (1 unit) by default. The actual PKT_INFO space is equal to (INF_SPACE + 1)<br><br>[Note2*] (L2_SPACE + INF_SPACE + 1) <= 0xF |



**15100004 FE\_RST\_GLO Frame Engine global reset 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18      | 17         | 16        |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|------------|-----------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |         |            |           |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |         |            |           |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |         |            |           |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2       | 1          | 0         |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    | PSE_RAM | PSE_MEM_EN | PSE_RESET |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      | RW         | W1S       |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       | 0          | 0         |

| Bit(s) | Name       | Description                                                                                                                                                                                                                                                                                                                                                        |
|--------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2      | PSE_RAM    | <b>PSE accessible RAM mode</b><br><br>[Note*1] When this bit is reset, PSE packet memory is only accessible by Pbus (0xA000~0xDFFF).<br><br>[Note*2] When this bit is set, PSE packet memory is only accessible by Pbus (0x8000~0xDFFF)<br><br>0: Only 8KB PSE memory is left for iNIC initialization.<br><br>1: Make the whole PSE memory is used for Pbus access |
| 1      | PSE_MEM_EN | <b>PSE access enable</b><br><br>0: Disable<br><br>1: Enable PSE memory is accessible by PBUS                                                                                                                                                                                                                                                                       |
| 0      | PSE_RESET  | <b>PSE soft reset (self-cleared)</b><br><br>[note*1] Whenever SW sets this bit, PSE will be initialized again and enter the normal mode.<br><br>0: Invalid<br><br>1: Write 1 to reset PSE                                                                                                                                                                          |

**15100008 FE\_INT\_STATUS Frame Engine interrupt status 00000000**

| Bit   | 31     | 30            | 29              | 28           | 27             | 26             | 25        | 24        | 23          | 22       | 21       | 20       | 19       | 18       | 17             | 16            |
|-------|--------|---------------|-----------------|--------------|----------------|----------------|-----------|-----------|-------------|----------|----------|----------|----------|----------|----------------|---------------|
| Name  | PPE_AF | REVO          | GDM2_AF         | GDM1_AF      | GDM2_DOS_LIMIT | GDM1_DOS_LIMIT | MAC2_LINK | MAC1_LINK | GDM2_ERR    | GDM2_CRC | GDM1_ERR | GDM1_CRC | RFIFO_UF | RFIFO_OV | INFIFO_GET_ERR | AFIFO_GET_ERR |
| Type  | W1C    | RO            | W1C             | W1C          | W1C            | W1C            | W1C       | W1C       | W1C         | W1C      | W1C      | W1C      | W1C      | W1C      | W1C            | W1C           |
| Reset | 0      | 0             | 0               | 0            | 0              | 0              | 0         | 0         | 0           | 0        | 0        | 0        | 0        | 0        | 0              | 0             |
| Bit   | 15     | 14            | 13              | 12           | 11             | 10             | 9         | 8         | 7           | 6        | 5        | 4        | 3        | 2        | 1              | 0             |
| Name  | REV2   | CDM_TSO_ALIGN | CDM_TSO_ILLEGAL | CDM_TSO_FAIL | REV3           |                | PSE_DROP  | FQ_EMPTY  | PSE_FC_ON_0 |          |          |          |          |          |                |               |
| Type  | RO     | W1C           | W1C             | W1C          | RO             |                | W1C       | W1C       | W1C         |          |          |          |          |          |                |               |
| Reset | 0      | 0             | 0               | 0            | 0              | 0              | 0         | 0         | 0           | 0        | 0        | 0        | 0        | 0        | 0              | 0             |

| Bit(s) | Name           | Description                                                                                                                                                                                      |
|--------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | PPE_AF         | MIB counter is almost full on PPE                                                                                                                                                                |
| 30     | REVO           | Reserved                                                                                                                                                                                         |
| 29     | GDM2_AF        | MIB counter is almost full on GDM2                                                                                                                                                               |
| 28     | GDM1_AF        | MIB counter is almost full on GDM1                                                                                                                                                               |
| 27     | GDM2_DOS_LIMIT | Packet rate is reached (TCP SYN, UDP, ICMP) on GDM2                                                                                                                                              |
| 26     | GDM1_DOS_LIMIT | Packet rate is reached (TCP SYN, UDP, ICMP) on GDM1                                                                                                                                              |
| 25     | MAC2_LINK      | Link Status Change on MAC2                                                                                                                                                                       |
| 24     | MAC1_LINK      | Link Status Change on MAC1                                                                                                                                                                       |
| 23     | GDM2_ERR       | Packet error on GDM2 / Reserved on XGDM2<br><br>(GDM2) Including FIFO overflow, checksum error, undersize, oversize<br><br>(XGDM2) n.a.                                                          |
| 22     | GDM2_CRC       | CRC error on GDM2 / Packet Error and CRC Error on XGDM2<br><br>(GDM2) Frame CRC Error only<br><br>(XGDM2) Including frame CRC Error, coding error, FIFO overflow, over/undersize, checksum error |
| 21     | GDM1_ERR       | Packet error on GDM1 / Reserved on XGDM1<br><br>(GDM1) Including FIFO overflow, checksum error, undersize, oversize<br><br>(XGDM1) n.a.                                                          |
| 20     | GDM1_CRC       | CRC error on GDM1 / Packet Error and CRC Error on XGDM1<br><br>(GDM1) Frame CRC Error only<br><br>(XGDM1) Including frame CRC Error, coding error, FIFO overflow, over/undersize, checksum error |
| 19     | RFIFO_UF       | Ring FIFO Underrun Defect                                                                                                                                                                        |
| 18     | RFIFO_OV       | Ring FIFO Overflow Defect                                                                                                                                                                        |
| 17     | INFIFO_GET_ERR | IN FIFO Get Defect                                                                                                                                                                               |

| Bit(s) | Name            | Description                           |
|--------|-----------------|---------------------------------------|
| 16     | AFIFO_GET_ERR   | ASYNC FIFO Get Defect                 |
| 15     | REV2            | Reserved                              |
| 14     | CDM_TSO_ALIGN   | Detects EOF alignment                 |
| 13     | CDM_TSO_ILLEGAL | Ignores illegal packet on CDM TSO     |
| 12     | CDM_TSO_FAIL    | TSO Fail on CDM                       |
| 11:10  | REV3            | Reserved                              |
| 9      | PSE_DROP        | Packet drop by PSE                    |
| 8      | FQ_EMPTY        | PSE free queue is empty               |
| 7:0    | PSE_FC_ON_0     | PSE port flow control is asserted     |
|        |                 | PSE port[n] enables the flow control. |

**1510000C FE\_INT\_ENABLE Frame Engine interrupt enable 00000000**

| Bit   | 31     | 30            | 29              | 28           | 27             | 26             | 25        | 24        | 23          | 22       | 21       | 20       | 19       | 18       | 17             | 16            |
|-------|--------|---------------|-----------------|--------------|----------------|----------------|-----------|-----------|-------------|----------|----------|----------|----------|----------|----------------|---------------|
| Name  | PPE_AF | REVO          | GDM2_AF         | GDM1_AF      | GDM2_DOS_LIMIT | GDM1_DOS_LIMIT | MAC2_LINK | MAC1_LINK | GDM2_ERR    | GDM2_CRC | GDM1_ERR | GDM1_CRC | RFIFO_UF | RFIFO_OV | INFIFO_GET_ERR | AFIFO_GET_ERR |
| Type  | RW     | RW            | RW              | RW           | RW             | RW             | RW        | RW        | RW          | RW       | RW       | RW       | RW       | RW       | RW             | RW            |
| Reset | 0      | 0             | 0               | 0            | 0              | 0              | 0         | 0         | 0           | 0        | 0        | 0        | 0        | 0        | 0              | 0             |
| Bit   | 15     | 14            | 13              | 12           | 11             | 10             | 9         | 8         | 7           | 6        | 5        | 4        | 3        | 2        | 1              | 0             |
| Name  | REV2   | CDM_TSO_ALIGN | CDM_TSO_ILLEGAL | CDM_TSO_FAIL | REV3           |                | PSE_DROP  | FQ_EMPTY  | PSE_FC_ON_0 |          |          |          |          |          |                |               |
| Type  | RW     | RW            | RW              | RW           | RW             |                | RW        | RW        | RW          |          |          |          |          |          |                |               |
| Reset | 0      | 0             | 0               | 0            | 0              | 0              | 0         | 0         | 0           | 0        | 0        | 0        | 0        | 0        | 0              | 0             |

| Bit(s) | Name           | Description                                                                                                                                                                              |
|--------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | PPE_AF         | MIB counter is almost full on PPE                                                                                                                                                        |
| 30     | REVO           | Reserved                                                                                                                                                                                 |
| 29     | GDM2_AF        | MIB counter is almost full on GDM2                                                                                                                                                       |
| 28     | GDM1_AF        | MIB counter is almost full on GDM1                                                                                                                                                       |
| 27     | GDM2_DOS_LIMIT | Packet rate is reached (TCP SYN, UDP, ICMP) on GDM2                                                                                                                                      |
| 26     | GDM1_DOS_LIMIT | Packet rate is reached (TCP SYN, UDP, ICMP) on GDM1                                                                                                                                      |
| 25     | MAC2_LINK      | Link Status Change on MAC2                                                                                                                                                               |
| 24     | MAC1_LINK      | Link Status Change on MAC1                                                                                                                                                               |
| 23     | GDM2_ERR       | Packet error on GDM2 / Reserved on XGDM2<br>(GDM2) Including FIFO overflow, checksum error, undersize, oversize<br>(XGDM2) n.a.                                                          |
| 22     | GDM2_CRC       | CRC error on GDM2 / Packet Error and CRC Error on XGDM2<br>(GDM2) Frame CRC Error only<br>(XGDM2) Including frame CRC Error, coding error, FIFO overflow, over/undersize, checksum error |
| 21     | GDM1_ERR       | Packet error on GDM1 / Reserved on XGDM1<br>(GDM1) Including FIFO overflow, checksum error, undersize, oversize<br>(XGDM1) n.a.                                                          |
| 20     | GDM1_CRC       | CRC error on GDM1 / Packet Error and CRC Error on XGDM1<br>(GDM1) Frame CRC Error only<br>(XGDM1) Including frame CRC Error, coding error, FIFO overflow, over/undersize, checksum error |
| 19     | RFIFO_UF       | Ring FIFO Underrun Defect                                                                                                                                                                |
| 18     | RFIFO_OV       | Ring FIFO Overflow Defect                                                                                                                                                                |
| 17     | INFIFO_GET_ERR | IN FIFO Get Defect                                                                                                                                                                       |

| Bit(s) | Name            | Description                           |
|--------|-----------------|---------------------------------------|
| 16     | AFIFO_GET_ERR   | ASYNCFIFO Get Defect                  |
| 15     | REV2            | Reserved                              |
| 14     | CDM_TSO_ALIGN   | Detects EOF alignment                 |
| 13     | CDM_TSO_ILLEGAL | Ignores illegal packet on CDM TSO     |
| 12     | CDM_TSO_FAIL    | TSO Fail on CDM                       |
| 11:10  | REV3            | Reserved                              |
| 9      | PSE_DROP        | Packet drop by PSE                    |
| 8      | FQ_EMPTY        | PSE free queue is empty               |
| 7:0    | PSE_FC_ON_0     | PSE port flow control is asserted     |
|        |                 | PSE port[n] enables the flow control. |

|          |             |    |    |    |    |    |    |    |    |    |    |    |                        |    |    |    |          |  |  |  |
|----------|-------------|----|----|----|----|----|----|----|----|----|----|----|------------------------|----|----|----|----------|--|--|--|
| 15100010 | FE_FOE_TS_T |    |    |    |    |    |    |    |    |    |    |    | Frame Engine timestamp |    |    |    | 00000000 |  |  |  |
| Bit      | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19                     | 18 | 17 | 16 |          |  |  |  |
| Name     | RESV0       |    |    |    |    |    |    |    |    |    |    |    |                        |    |    |    |          |  |  |  |
| Type     | RW          |    |    |    |    |    |    |    |    |    |    |    |                        |    |    |    |          |  |  |  |
| Reset    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                      | 0  | 0  | 0  |          |  |  |  |
| Bit      | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3                      | 2  | 1  | 0  |          |  |  |  |
| Name     | FOE_TS_T    |    |    |    |    |    |    |    |    |    |    |    |                        |    |    |    |          |  |  |  |
| Type     | RW          |    |    |    |    |    |    |    |    |    |    |    |                        |    |    |    |          |  |  |  |
| Reset    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                      | 0  | 0  | 0  |          |  |  |  |

| Bit(s) | Name     | Description                                              |
|--------|----------|----------------------------------------------------------|
| 31:16  | RESV0    | Reserved                                                 |
| 15:0   | FOE_TS_T | Timestamp                                                |
|        |          | Timestamp unit is 1 sec.                                 |
|        |          | [Note] This timer is driven by free-running 125MHz clock |

15100014      FE\_IPV6\_EXT      Frame Engine IPv6 extension header      00000000

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----|----|----|----|----|----|----|----------|----|----|----|----|----|----|----|
| Name  | IP6_EXT3 |    |    |    |    |    |    |    | IP6_EXT2 |    |    |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    | RW       |    |    |    |    |    |    |    |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | IP6_EXT1 |    |    |    |    |    |    |    | IP6_EXT0 |    |    |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    | RW       |    |    |    |    |    |    |    |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name     | Description              |
|--------|----------|--------------------------|
| 31:24  | IP6_EXT3 | IPv6 extension header #3 |
| 23:16  | IP6_EXT2 | IPv6 extension header #2 |
| 15:8   | IP6_EXT1 | IPv6 extension header #1 |
| 7:0    | IP6_EXT0 | IPv6 extension header #0 |

**15100018**      **FE\_RATE\_COMP**      **Frame Engine rate limit compensation**      **00001818**

| Bit   | 31             | 30            | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22            | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|---------------|----|----|----|----|----|----|----------------|---------------|----|----|----|----|----|----|
| Name  | REVO           |               |    |    |    |    |    |    |                |               |    |    |    |    |    |    |
| Type  | RO             |               |    |    |    |    |    |    |                |               |    |    |    |    |    |    |
| Reset | 0              | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0             | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14            | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6             | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DMA_RATE_MINUS | DMA_RATE_BYTE |    |    |    |    |    |    | PSE_RATE_MINUS | PSE_RATE_BYTE |    |    |    |    |    |    |
| Type  | RW             | RW            |    |    |    |    |    |    | RW             | RW            |    |    |    |    |    |    |
| Reset | 0              | 0             | 0  | 1  | 1  | 0  | 0  | 0  | 0              | 0             | 0  | 1  | 1  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                                                                                                 |
|--------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | REVO           | <b>Reserved</b>                                                                                                                                                             |
| 15     | DMA_RATE_MINUS | 1'b0: a specific byte count is added to the frame length according to FE_GLO_CFG.RATE_BYTE<br><br>1'b1: a specific byte count is subtracted from the incoming frame length. |
| 14:8   | DMA_RATE_BYTE  | <b>Byte number for rate control</b><br><br>The byte number should be subtracted while calculating the rate limit.                                                           |
| 7      | PSE_RATE_MINUS | 1'b0: a specific byte count is added to the frame length according to FE_GLO_CFG.RATE_BYTE<br><br>1'b1: a specific byte count is subtracted from the incoming frame length. |
| 6:0    | PSE_RATE_BYTE  | <b>Byte number for rate control</b><br><br>The byte number should be subtracted while calculating the rate limit.                                                           |

**15100020 FE\_INT\_GRP Frame Engine interrupt group 00000000**

| Bit          | 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|-----------------|----|----|----|-----------------|----|----|----|-----------------|----|----|----|
| <b>Name</b>  | QDMA_INT_G2_ASG |    |    |    | QDMA_INT_G1_ASG |    |    |    | QDMA_INT_G0_ASG |    |    |    | PDMA_INT_G2_ASG |    |    |    |
| <b>Type</b>  | RW              |    |    |    | RW              |    |    |    | RW              |    |    |    | RW              |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0               | 0  | 0  | 0  |
| <b>Bit</b>   | 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| <b>Name</b>  | PDMA_INT_G1_ASG |    |    |    | PDMA_INT_G0_ASG |    |    |    | PDMA_INT_G3_ASG |    |    |    | FE_MISC_INT_ASG |    |    |    |
| <b>Type</b>  | RW              |    |    |    | RW              |    |    |    | RW              |    |    |    | RW              |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0               | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                      |
|--------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | QDMA_INT_G2_ASG | <b>QDMA group 2 interrupt assignment</b><br>4'h0: Assign to fe_int[0]<br>4'h1: Assign to fe_int[1]<br>4'h2: Assign to fe_int[2]<br>4'h3: Assign to fe_int[3]<br>Others: Reserved |
| 27:24  | QDMA_INT_G1_ASG | <b>QDMA group 1 interrupt assignment</b><br>4'h0: Assign to fe_int[0]<br>4'h1: Assign to fe_int[1]<br>4'h2: Assign to fe_int[2]<br>4'h3: Assign to fe_int[3]<br>Others: Reserved |
| 23:20  | QDMA_INT_G0_ASG | <b>QDMA group 0 interrupt assignment</b><br>4'h0: Assign to fe_int[0]<br>4'h1: Assign to fe_int[1]<br>4'h2: Assign to fe_int[2]<br>4'h3: Assign to fe_int[3]<br>Others: Reserved |
| 19:16  | PDMA_INT_G2_ASG | <b>PDMA group 2 interrupt assignment</b><br>4'h0: Assign to fe_int[0]<br>4'h1: Assign to fe_int[1]<br>4'h2: Assign to fe_int[2]<br>4'h3: Assign to fe_int[3]<br>Others: Reserved |
| 15:12  | PDMA_INT_G1_ASG | <b>PDMA group 1 interrupt assignment</b>                                                                                                                                         |



| Bit(s) | Name            | Description                                    |
|--------|-----------------|------------------------------------------------|
|        |                 | 4'h0: Assign to fe_int[0]                      |
|        |                 | 4'h1: Assign to fe_int[1]                      |
|        |                 | 4'h2: Assign to fe_int[2]                      |
|        |                 | 4'h3: Assign to fe_int[3]                      |
|        |                 | Others: Reserved                               |
| 11:8   | PDMA_INT_G0_ASG | <b>PDMA group 0 interrupt assignment</b>       |
|        |                 | 4'h0: Assign to fe_int[0]                      |
|        |                 | 4'h1: Assign to fe_int[1]                      |
|        |                 | 4'h2: Assign to fe_int[2]                      |
|        |                 | 4'h3: Assign to fe_int[3]                      |
|        |                 | Others: Reserved                               |
| 7:4    | PDMA_INT_G3_ASG | <b>PDMA group 3 interrupt assignment</b>       |
|        |                 | 4'h0: Assign to fe_int[0]                      |
|        |                 | 4'h1: Assign to fe_int[1]                      |
|        |                 | 4'h2: Assign to fe_int[2]                      |
|        |                 | 4'h3: Assign to fe_int[3]                      |
|        |                 | Others: Reserved                               |
| 3:0    | FE_MISC_INT_ASG | <b>Frame engine misc. interrupt assignment</b> |
|        |                 | 4'h0: Assign to fe_int[0]                      |
|        |                 | 4'h1: Assign to fe_int[1]                      |
|        |                 | 4'h2: Assign to fe_int[2]                      |
|        |                 | 4'h3: Assign to fe_int[3]                      |
|        |                 | Others: Reserved                               |

**15100024 FE\_GLO\_CFG2 Frame Engine global configuration part2 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22         | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|
| Name  |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |    |
| Type  |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |    |
| Reset |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6          | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    | LINK_DWN_1 |    |    |    |    |    |    |
| Type  |    |    |    |    |    |    |    |    |    | RW         |    |    |    |    |    |    |
| Reset |    |    |    |    |    |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                                                                                              |
|--------|------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 6:0    | LINK_DWN_1 | <b>Disable PSE Port 8~14</b><br><br>When PSE port is not valid on the Frame Engine, user is suggested to disable the corresponding port. |

**15100028 FE\_INT\_STATUS2 Frame Engine interrupt status part2 00000000**

| Bit   | 31                    | 30 | 29 | 28 | 27                    | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------------|----|----|----|-----------------------|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  |                       |    |    |    |                       |    |    |    |             |    |    |    |    |    |    |    |
| Type  |                       |    |    |    |                       |    |    |    |             |    |    |    |    |    |    |    |
| Reset |                       |    |    |    |                       |    |    |    |             |    |    |    |    |    |    |    |
| Bit   | 15                    | 14 | 13 | 12 | 11                    | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PPE1_SB_FIFO_FULL_INT |    |    |    | PPE0_SB_FIFO_FULL_INT |    |    |    | PSE_FC_ON_1 |    |    |    |    |    |    |    |
| Type  | W1C                   |    |    |    | W1C                   |    |    |    | W1C         |    |    |    |    |    |    |    |
| Reset | 0                     | 0  | 0  | 0  | 0                     | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                  | Description                                                                           |
|--------|-----------------------|---------------------------------------------------------------------------------------|
| 15:12  | PPE1_SB_FIFO_FULL_INT | <b>PPE1 sideband FIFO full event is asserted</b>                                      |
| 11:8   | PPE0_SB_FIFO_FULL_INT | <b>PPE0 sideband FIFO full event is asserted</b>                                      |
| 7:0    | PSE_FC_ON_1           | <b>PSE port flow control is asserted</b><br><br>PSE port[n] enables the flow control. |

**1510002C FE\_INT\_ENABLE2 Frame Engine interrupt enable part2 00000000**

| Bit   | 31                    | 30 | 29 | 28 | 27                    | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------------|----|----|----|-----------------------|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  |                       |    |    |    |                       |    |    |    |             |    |    |    |    |    |    |    |
| Type  |                       |    |    |    |                       |    |    |    |             |    |    |    |    |    |    |    |
| Reset |                       |    |    |    |                       |    |    |    |             |    |    |    |    |    |    |    |
| Bit   | 15                    | 14 | 13 | 12 | 11                    | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PPE1_SB_FIFO_FULL_INT |    |    |    | PPE0_SB_FIFO_FULL_INT |    |    |    | PSE_FC_ON_1 |    |    |    |    |    |    |    |
| Type  | RW                    |    |    |    | RW                    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0                     | 0  | 0  | 0  | 0                     | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                  | Description |
|--------|-----------------------|-------------|
| 15:12  | PPE1_SB_FIFO_FULL_INT |             |
| 11:8   | PPE0_SB_FIFO_FULL_INT |             |
| 7:0    | PSE_FC_ON_1           |             |

**151000C0 PSE\_IQ\_REV\_RLS1 PSE input queue reservation release part1 000D0007**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26            | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|---------------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P1_IQ_RES_RLS |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW            |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10            | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P0_IQ_RES_RLS |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW            |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  |

| Bit(s) | Name          | Description                                                                                                                                                                                                 |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P1_IQ_RES_RLS | <b>Virtual input Q reservation for pause release threshold</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES_RLS). |
| 10:0   | P0_IQ_RES_RLS | <b>Virtual input Q reservation for pause release threshold</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES_RLS). |

**151000C4**      **PSE IQ\_REV\_RLS2**      **PSE input queue reservation release part2**      **07FF000D**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26            | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|---------------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P3_IQ_RES_RLS |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW            |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 1             | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10            | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P2_IQ_RES_RLS |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW            |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  |

| Bit(s) | Name          | Description                                                                                                                                                                                                 |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P3_IQ_RES_RLS | <b>Virtual input Q reservation for pause release threshold</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES_RLS). |
| 10:0   | P2_IQ_RES_RLS | <b>Virtual input Q reservation for pause release threshold</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES_RLS). |

**151000C8**      **PSE IQ\_REV\_RLS3**      **PSE input queue reservation release part3**      **000707FF**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26            | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|---------------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P5_IQ_RES_RLS |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW            |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10            | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P4_IQ_RES_RLS |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW            |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 1             | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name          | Description                                                                                                                                                                                                 |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P5_IQ_RES_RLS | <b>Virtual input Q reservation for pause release threshold</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES_RLS). |
| 10:0   | P4_IQ_RES_RLS | <b>Virtual input Q reservation for pause release threshold</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES_RLS). |

**151000CC**      **PSE IQ\_REV\_RLS4**      **PSE input queue reservation release part4**      **00070007**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26            | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|---------------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P7_IQ_RES_RLS |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW            |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10            | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P6_IQ_RES_RLS |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW            |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  |

| Bit(s) | Name          | Description                                                                                                                                                                                                 |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P7_IQ_RES_RLS | <b>Virtual input Q reservation for pause release threshold</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES_RLS). |
| 10:0   | P6_IQ_RES_RLS | <b>Virtual input Q reservation for pause release threshold</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES_RLS). |

**151000D0**      **PSE IQ\_REV\_RLS5**      **PSE input queue reservation release part5**      **00070007**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26            | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|---------------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P9_IQ_RES_RLS |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW            |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10            | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P8_IQ_RES_RLS |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW            |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  |

| Bit(s) | Name          | Description                                                                                                                                                                                                 |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P9_IQ_RES_RLS | <b>Virtual input Q reservation for pause release threshold</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES_RLS). |
| 10:0   | P8_IQ_RES_RLS | <b>Virtual input Q reservation for pause release threshold</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES_RLS). |

**151000D4**      **PSE IQ\_REV\_RLS6**      **PSE input queue reservation release part6**      **00070007**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26             | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----------------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P11_IQ_RES_RLS |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW             |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10             | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P10_IQ_RES_RLS |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW             |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  |

| Bit(s) | Name           | Description                                                                                                                                                                                                 |
|--------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P11_IQ_RES_RLS | <b>Virtual input Q reservation for pause release threshold</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES_RLS). |
| 10:0   | P10_IQ_RES_RLS | <b>Virtual input Q reservation for pause release threshold</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES_RLS). |

**151000D8**      **PSE IQ\_REV\_RLS7**      **PSE input queue reservation release part7**      **000707FF**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26             | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----------------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P13_IQ_RES_RLS |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW             |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10             | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P12_IQ_RES_RLS |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW             |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 1              | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name           | Description                                                                                                                                                                                                 |
|--------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P13_IQ_RES_RLS | <b>Virtual input Q reservation for pause release threshold</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES_RLS). |
| 10:0   | P12_IQ_RES_RLS | <b>Virtual input Q reservation for pause release threshold</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES_RLS). |

**151000DC**      **PSE IQ\_REV\_RLS8**      **PSE input queue reservation release part8**      **000D0007**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26             | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----------------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P15_IQ_RES_RLS |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW             |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10             | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P14_IQ_RES_RLS |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW             |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  |

| Bit(s) | Name           | Description                                                                                                                                                                                                 |
|--------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P15_IQ_RES_RLS | <b>Virtual input Q reservation for pause release threshold</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES_RLS). |
| 10:0   | P14_IQ_RES_RLS | <b>Virtual input Q reservation for pause release threshold</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES_RLS). |

**151000E0**      **PSE TDM\_TBL8**      **PSE TDM arbiter table8**      **498E6213**

| Bit   | 31         | 30 | 29 | 28 | 27 | 26         | 25 | 24 | 23 | 22         | 21 | 20 | 19 | 18         | 17 | 16 |
|-------|------------|----|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|----|
| Name  | TDM_TBL_71 |    |    |    |    | TDM_TBL_70 |    |    |    | TDM_TBL_69 |    |    |    | TDM_TBL_68 |    |    |
| Type  | RW         |    |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |
| Reset | 0          | 1  | 0  | 0  | 1  | 0          | 0  | 1  | 1  | 0          | 0  | 0  | 1  | 1          | 1  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10         | 9  | 8  | 7  | 6          | 5  | 4  | 3  | 2          | 1  | 0  |
| Name  | TDM_TBL_67 |    |    |    |    | TDM_TBL_66 |    |    |    | TDM_TBL_65 |    |    |    | TDM_TBL_64 |    |    |
| Type  | RW         |    |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |
| Reset | 0          | 1  | 1  | 0  | 0  | 0          | 1  | 0  | 0  | 0          | 0  | 1  | 0  | 0          | 1  | 1  |

| Bit(s) | Name       | Description                           |
|--------|------------|---------------------------------------|
| 31:28  | TDM_TBL_71 | <b>PSE TDM arbiter table entry 71</b> |
| 27:24  | TDM_TBL_70 | <b>PSE TDM arbiter table entry 70</b> |
| 23:20  | TDM_TBL_69 | <b>PSE TDM arbiter table entry 69</b> |
| 19:16  | TDM_TBL_68 | <b>PSE TDM arbiter table entry 68</b> |
| 15:12  | TDM_TBL_67 | <b>PSE TDM arbiter table entry 67</b> |
| 11:8   | TDM_TBL_66 | <b>PSE TDM arbiter table entry 66</b> |
| 7:4    | TDM_TBL_65 | <b>PSE TDM arbiter table entry 65</b> |
| 3:0    | TDM_TBL_64 | <b>PSE TDM arbiter table entry 64</b> |

**151000E4      PSE\_TDM\_TBL9      PSE TDM arbiter table9      8DA5213C**

| Bit          | 31         | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
|--------------|------------|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|----|----|
| <b>Name</b>  | TDM_TBL_79 |    |    |    | TDM_TBL_78 |    |    |    | TDM_TBL_77 |    |    |    | TDM_TBL_76 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 1          | 0  | 0  | 0  | 1          | 1  | 0  | 1  | 1          | 0  | 1  | 0  | 0          | 1  | 0  | 1  |
| Bit          | 15         | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| <b>Name</b>  | TDM_TBL_75 |    |    |    | TDM_TBL_74 |    |    |    | TDM_TBL_73 |    |    |    | TDM_TBL_72 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 0          | 0  | 1  | 0  | 0          | 0  | 0  | 1  | 0          | 0  | 1  | 1  | 1          | 1  | 0  | 0  |

| Bit(s) | Name       | Description                    |
|--------|------------|--------------------------------|
| 31:28  | TDM_TBL_79 | PSE TDM arbiter table entry 79 |
| 27:24  | TDM_TBL_78 | PSE TDM arbiter table entry 78 |
| 23:20  | TDM_TBL_77 | PSE TDM arbiter table entry 77 |
| 19:16  | TDM_TBL_76 | PSE TDM arbiter table entry 76 |
| 15:12  | TDM_TBL_75 | PSE TDM arbiter table entry 75 |
| 11:8   | TDM_TBL_74 | PSE TDM arbiter table entry 74 |
| 7:4    | TDM_TBL_73 | PSE TDM arbiter table entry 73 |
| 3:0    | TDM_TBL_72 | PSE TDM arbiter table entry 72 |



**151000E8      PSE\_TDM\_TBL10      PSE TDM arbiter table10      9E621FC4**

| Bit          | 31         | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
|--------------|------------|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|----|----|
| <b>Name</b>  | TDM_TBL_87 |    |    |    | TDM_TBL_86 |    |    |    | TDM_TBL_85 |    |    |    | TDM_TBL_84 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 1          | 0  | 0  | 1  | 1          | 1  | 1  | 0  | 0          | 1  | 1  | 0  | 0          | 0  | 1  | 0  |
| <b>Bit</b>   | 15         | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| <b>Name</b>  | TDM_TBL_83 |    |    |    | TDM_TBL_82 |    |    |    | TDM_TBL_81 |    |    |    | TDM_TBL_80 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 0          | 0  | 0  | 1  | 1          | 1  | 1  | 1  | 1          | 1  | 0  | 0  | 0          | 1  | 0  | 0  |

| Bit(s) | Name       | Description                    |
|--------|------------|--------------------------------|
| 31:28  | TDM_TBL_87 | PSE TDM arbiter table entry 87 |
| 27:24  | TDM_TBL_86 | PSE TDM arbiter table entry 86 |
| 23:20  | TDM_TBL_85 | PSE TDM arbiter table entry 85 |
| 19:16  | TDM_TBL_84 | PSE TDM arbiter table entry 84 |
| 15:12  | TDM_TBL_83 | PSE TDM arbiter table entry 83 |
| 11:8   | TDM_TBL_82 | PSE TDM arbiter table entry 82 |
| 7:4    | TDM_TBL_81 | PSE TDM arbiter table entry 81 |
| 3:0    | TDM_TBL_80 | PSE TDM arbiter table entry 80 |

**151000EC      PSE\_TDM\_TBL11      PSE TDM arbiter table11      7777770D**

| Bit          | 31         | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
|--------------|------------|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|----|----|
| <b>Name</b>  | TDM_TBL_95 |    |    |    | TDM_TBL_94 |    |    |    | TDM_TBL_93 |    |    |    | TDM_TBL_92 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 0          | 1  | 1  | 1  | 0          | 1  | 1  | 1  | 0          | 1  | 1  | 1  | 0          | 1  | 1  | 1  |
| Bit          | 15         | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| <b>Name</b>  | TDM_TBL_91 |    |    |    | TDM_TBL_90 |    |    |    | TDM_TBL_89 |    |    |    | TDM_TBL_88 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 0          | 1  | 1  | 1  | 0          | 1  | 1  | 1  | 0          | 0  | 0  | 0  | 1          | 1  | 0  | 1  |

| Bit(s) | Name       | Description                    |
|--------|------------|--------------------------------|
| 31:28  | TDM_TBL_95 | PSE TDM arbiter table entry 95 |
| 27:24  | TDM_TBL_94 | PSE TDM arbiter table entry 94 |
| 23:20  | TDM_TBL_93 | PSE TDM arbiter table entry 93 |
| 19:16  | TDM_TBL_92 | PSE TDM arbiter table entry 92 |
| 15:12  | TDM_TBL_91 | PSE TDM arbiter table entry 91 |
| 11:8   | TDM_TBL_90 | PSE TDM arbiter table entry 90 |
| 7:4    | TDM_TBL_89 | PSE TDM arbiter table entry 89 |
| 3:0    | TDM_TBL_88 | PSE TDM arbiter table entry 88 |

**151000F0      PSE\_TDM\_TBL12      PSE TDM arbiter table12      77777777**

| Bit          | 31          | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19          | 18 | 17 | 16 |
|--------------|-------------|----|----|----|-------------|----|----|----|-------------|----|----|----|-------------|----|----|----|
| <b>Name</b>  | TDM_TBL_103 |    |    |    | TDM_TBL_102 |    |    |    | TDM_TBL_101 |    |    |    | TDM_TBL_100 |    |    |    |
| <b>Type</b>  | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    |
| <b>Reset</b> | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  |
| Bit          | 15          | 14 | 13 | 12 | 11          | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3           | 2  | 1  | 0  |
| <b>Name</b>  | TDM_TBL_99  |    |    |    | TDM_TBL_98  |    |    |    | TDM_TBL_97  |    |    |    | TDM_TBL_96  |    |    |    |
| <b>Type</b>  | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    |
| <b>Reset</b> | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  |

| Bit(s) | Name        | Description                     |
|--------|-------------|---------------------------------|
| 31:28  | TDM_TBL_103 | PSE TDM arbiter table entry 103 |
| 27:24  | TDM_TBL_102 | PSE TDM arbiter table entry 102 |
| 23:20  | TDM_TBL_101 | PSE TDM arbiter table entry 101 |
| 19:16  | TDM_TBL_100 | PSE TDM arbiter table entry 100 |
| 15:12  | TDM_TBL_99  | PSE TDM arbiter table entry 99  |
| 11:8   | TDM_TBL_98  | PSE TDM arbiter table entry 98  |
| 7:4    | TDM_TBL_97  | PSE TDM arbiter table entry 97  |
| 3:0    | TDM_TBL_96  | PSE TDM arbiter table entry 96  |

**151000F4      PSE\_TDM\_TBL13      PSE TDM arbiter table13      77777777**

| Bit          | 31          | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19          | 18 | 17 | 16 |
|--------------|-------------|----|----|----|-------------|----|----|----|-------------|----|----|----|-------------|----|----|----|
| <b>Name</b>  | TDM_TBL_111 |    |    |    | TDM_TBL_110 |    |    |    | TDM_TBL_109 |    |    |    | TDM_TBL_108 |    |    |    |
| <b>Type</b>  | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    |
| <b>Reset</b> | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  |
| Bit          | 15          | 14 | 13 | 12 | 11          | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3           | 2  | 1  | 0  |
| <b>Name</b>  | TDM_TBL_107 |    |    |    | TDM_TBL_106 |    |    |    | TDM_TBL_105 |    |    |    | TDM_TBL_104 |    |    |    |
| <b>Type</b>  | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    |
| <b>Reset</b> | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  |

| Bit(s) | Name        | Description                     |
|--------|-------------|---------------------------------|
| 31:28  | TDM_TBL_111 | PSE TDM arbiter table entry 111 |
| 27:24  | TDM_TBL_110 | PSE TDM arbiter table entry 110 |
| 23:20  | TDM_TBL_109 | PSE TDM arbiter table entry 109 |
| 19:16  | TDM_TBL_108 | PSE TDM arbiter table entry 108 |
| 15:12  | TDM_TBL_107 | PSE TDM arbiter table entry 107 |
| 11:8   | TDM_TBL_106 | PSE TDM arbiter table entry 106 |
| 7:4    | TDM_TBL_105 | PSE TDM arbiter table entry 105 |
| 3:0    | TDM_TBL_104 | PSE TDM arbiter table entry 104 |

**151000F8      PSE\_TDM\_TBL14      PSE TDM arbiter table14      77777777**

| Bit          | 31          | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19          | 18 | 17 | 16 |
|--------------|-------------|----|----|----|-------------|----|----|----|-------------|----|----|----|-------------|----|----|----|
| <b>Name</b>  | TDM_TBL_119 |    |    |    | TDM_TBL_118 |    |    |    | TDM_TBL_117 |    |    |    | TDM_TBL_116 |    |    |    |
| <b>Type</b>  | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    |
| <b>Reset</b> | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  |
| Bit          | 15          | 14 | 13 | 12 | 11          | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3           | 2  | 1  | 0  |
| <b>Name</b>  | TDM_TBL_115 |    |    |    | TDM_TBL_114 |    |    |    | TDM_TBL_113 |    |    |    | TDM_TBL_112 |    |    |    |
| <b>Type</b>  | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    |
| <b>Reset</b> | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  |

| Bit(s) | Name        | Description                     |
|--------|-------------|---------------------------------|
| 31:28  | TDM_TBL_119 | PSE TDM arbiter table entry 119 |
| 27:24  | TDM_TBL_118 | PSE TDM arbiter table entry 118 |
| 23:20  | TDM_TBL_117 | PSE TDM arbiter table entry 117 |
| 19:16  | TDM_TBL_116 | PSE TDM arbiter table entry 116 |
| 15:12  | TDM_TBL_115 | PSE TDM arbiter table entry 115 |
| 11:8   | TDM_TBL_114 | PSE TDM arbiter table entry 114 |
| 7:4    | TDM_TBL_113 | PSE TDM arbiter table entry 113 |
| 3:0    | TDM_TBL_112 | PSE TDM arbiter table entry 112 |

**151000FC      PSE\_TDM\_TBL15      PSE TDM arbiter table15      77777777**

| Bit          | 31          | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19          | 18 | 17 | 16 |
|--------------|-------------|----|----|----|-------------|----|----|----|-------------|----|----|----|-------------|----|----|----|
| <b>Name</b>  | TDM_TBL_127 |    |    |    | TDM_TBL_126 |    |    |    | TDM_TBL_125 |    |    |    | TDM_TBL_124 |    |    |    |
| <b>Type</b>  | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    |
| <b>Reset</b> | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  |
| Bit          | 15          | 14 | 13 | 12 | 11          | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3           | 2  | 1  | 0  |
| <b>Name</b>  | TDM_TBL_123 |    |    |    | TDM_TBL_122 |    |    |    | TDM_TBL_121 |    |    |    | TDM_TBL_120 |    |    |    |
| <b>Type</b>  | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    |
| <b>Reset</b> | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  |

| Bit(s) | Name        | Description                     |
|--------|-------------|---------------------------------|
| 31:28  | TDM_TBL_127 | PSE TDM arbiter table entry 127 |
| 27:24  | TDM_TBL_126 | PSE TDM arbiter table entry 126 |
| 23:20  | TDM_TBL_125 | PSE TDM arbiter table entry 125 |
| 19:16  | TDM_TBL_124 | PSE TDM arbiter table entry 124 |
| 15:12  | TDM_TBL_123 | PSE TDM arbiter table entry 123 |
| 11:8   | TDM_TBL_122 | PSE TDM arbiter table entry 122 |
| 7:4    | TDM_TBL_121 | PSE TDM arbiter table entry 121 |
| 3:0    | TDM_TBL_120 | PSE TDM arbiter table entry 120 |

**15100100      PSE\_FQFC\_CFG1      PSE free queue flow control part1      07FF07FF**

| Bit   | 31 | 30 | 29 | 28 | 27      | 26          | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|---------|-------------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | FQ_PCNT |             |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO      |             |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0       | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11      | 10          | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |         | FQ_MAX_PCNT |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |         | RW          |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |         | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s)                                              | Name        | Description                |
|-----------------------------------------------------|-------------|----------------------------|
| 27:16                                               | FQ_PCNT     | Free queue page count      |
| 10:0                                                | FQ_MAX_PCNT | Maximum free Q page count. |
| Please reset PSE after re-programming this register |             |                            |

**15100104      PSE\_FQFC\_CFG2      PSE free queue flow control part2      04400400**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26      | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|---------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | FQ_HIGH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW      |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 1       | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10      | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | FQ_LOW  |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW      |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 1       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                  |
|--------|---------|------------------------------|
| 26:16  | FQ_HIGH | High threshold to release FC |
| 10:0   | FQ_LOW  | Low threshold to trigger FC  |

1510010C      PSE\_DUMMY\_REQ      PSE last FreeQ page request control      00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26             | 25 | 24 | 23 | 22 | 21 | 20 | 19                | 18                | 17                | 16               |
|-------|----|----|----|----|----|----------------|----|----|----|----|----|----|-------------------|-------------------|-------------------|------------------|
| Name  |    |    |    |    |    |                |    |    |    |    |    |    | PSE_DUMMY_WORK_G3 | PSE_DUMMY_WORK_G2 | PSE_DUMMY_WORK_G1 | PSE_DUMMY_WORK_K |
| Type  |    |    |    |    |    |                |    |    |    |    |    |    | RW                | RW                | RW                | RW               |
| Reset |    |    |    |    |    |                |    |    |    |    |    |    | 0                 | 0                 | 0                 | 0                |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10             | 9  | 8  | 7  | 6  | 5  | 4  | 3                 | 2                 | 1                 | 0                |
| Name  |    |    |    |    |    | DUMMY_PAGE_THR |    |    |    |    |    |    |                   |                   |                   |                  |
| Type  |    |    |    |    |    | RW             |    |    |    |    |    |    |                   |                   |                   |                  |
| Reset |    |    |    |    |    | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0                 | 0                 | 0                |

| Bit(s) | Name              | Description                                                                                                           |
|--------|-------------------|-----------------------------------------------------------------------------------------------------------------------|
| 19     | PSE_DUMMY_WORK_G3 | <p>Enable for GDM3 to get page 2047(dummy page) when freeQ &lt; DUMMY_PAGE_THR</p> <p>0: Disable</p> <p>1: Enable</p> |
| 18     | PSE_DUMMY_WORK_G2 | <p>Enable for GDM2 to get page 2047(dummy page) when freeQ &lt; DUMMY_PAGE_THR</p> <p>0: Disable</p> <p>1: Enable</p> |
| 17     | PSE_DUMMY_WORK_G1 | <p>Enable for GDM1 to get page 2047(dummy page) when freeQ &lt; DUMMY_PAGE_THR</p> <p>0: Disable</p> <p>1: Enable</p> |
| 16     | PSE_DUMMY_WORK    | <p>Enable for CDM to get page 2047(dummy page) when freeQ &lt; DUMMY_PAGE_THR</p> <p>0: Disable</p> <p>1: Enable</p>  |
| 10:0   | DUMMY_PAGE_THR    | Dummy drop threshold, for dummy page modules to judge the packet drop                                                 |



15100110      **PSE\_PPE0\_DROP**      **PPE0 drop packet enable port**      00000000

| Bit   | 31   | 30               | 29               | 28               | 27               | 26               | 25              | 24              | 23              | 22              | 21              | 20              | 19              | 18              | 17              | 16              |
|-------|------|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name  | REVO |                  |                  |                  |                  |                  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| Type  | RO   |                  |                  |                  |                  |                  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| Reset | 0    | 0                | 0                | 0                | 0                | 0                | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               |
| Bit   | 15   | 14               | 13               | 12               | 11               | 10               | 9               | 8               | 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |
| Name  | REV  | PPE0_DROP_P14_EN | PPE0_DROP_P13_EN | PPE0_DROP_P12_EN | PPE0_DROP_P11_EN | PPE0_DROP_P10_EN | PPE0_DROP_P9_EN | PPE0_DROP_P8_EN | PPE0_DROP_P7_EN | PPE0_DROP_P6_EN | PPE0_DROP_P5_EN | PPE0_DROP_P4_EN | PPE0_DROP_P3_EN | PPE0_DROP_P2_EN | PPE0_DROP_P1_EN | PPE0_DROP_P0_EN |
| Type  | RW   | RW               | RW               | RW               | RW               | RW               | RW              | RW              | RW              | RW              | RW              | RW              | RW              | RW              | RW              | RW              |
| Reset | 0    | 0                | 0                | 0                | 0                | 0                | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               |

| Bit(s) | Name             | Description                                                                       |
|--------|------------------|-----------------------------------------------------------------------------------|
| 31:16  | REVO             | Reserved                                                                          |
| 15     | REV              | Reserved                                                                          |
| 14     | PPE0_DROP_P14_EN | Enable PPE0 drop packet to port 14 due to RX ring full<br>0: Disable<br>1: Enable |
| 13     | PPE0_DROP_P13_EN | Enable PPE0 drop packet to port 13 due to RX ring full<br>0: Disable<br>1: Enable |
| 12     | PPE0_DROP_P12_EN | Enable PPE0 drop packet to port 12 due to RX ring full<br>0: Disable<br>1: Enable |
| 11     | PPE0_DROP_P11_EN | Enable PPE0 drop packet to port 11 due to RX ring full<br>0: Disable<br>1: Enable |
| 10     | PPE0_DROP_P10_EN | Enable PPE0 drop packet to port 10 due to RX ring full<br>0: Disable<br>1: Enable |
| 9      | PPE0_DROP_P9_EN  | Enable PPE0 drop packet to port 9 due to RX ring full<br>0: Disable<br>1: Enable  |
| 8      | PPE0_DROP_P8_EN  | Enable PPE0 drop packet to port 8 due to RX ring full<br>0: Disable<br>1: Enable  |
| 7      | PPE0_DROP_P7_EN  | Enable PPE0 drop packet to port 7 due to RX ring full                             |

| Bit(s) | Name            | Description                                                  |
|--------|-----------------|--------------------------------------------------------------|
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 6      | PPE0_DROP_P6_EN | <b>Enable PPE0 drop packet to port 6 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 5      | PPE0_DROP_P5_EN | <b>Enable PPE0 drop packet to port 5 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 4      | PPE0_DROP_P4_EN | <b>Enable PPE0 drop packet to port 4 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 3      | PPE0_DROP_P3_EN | <b>Enable PPE0 drop packet to port 3 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 2      | PPE0_DROP_P2_EN | <b>Enable PPE0 drop packet to port 2 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 1      | PPE0_DROP_P1_EN | <b>Enable PPE0 drop packet to port 1 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 0      | PPE0_DROP_P0_EN | <b>Enable PPE0 drop packet to port 0 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |

15100114      **PSE\_PPE1\_DROP**      **PPE1 drop packet enable port**      00000000

| Bit   | 31   | 30               | 29               | 28               | 27               | 26               | 25              | 24              | 23              | 22              | 21              | 20              | 19              | 18              | 17              | 16              |
|-------|------|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name  | REVO |                  |                  |                  |                  |                  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| Type  | RO   |                  |                  |                  |                  |                  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| Reset | 0    | 0                | 0                | 0                | 0                | 0                | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               |
| Bit   | 15   | 14               | 13               | 12               | 11               | 10               | 9               | 8               | 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |
| Name  | REV  | PPE1_DROP_P14_EN | PPE1_DROP_P13_EN | PPE1_DROP_P12_EN | PPE1_DROP_P11_EN | PPE1_DROP_P10_EN | PPE1_DROP_P9_EN | PPE1_DROP_P8_EN | PPE1_DROP_P7_EN | PPE1_DROP_P6_EN | PPE1_DROP_P5_EN | PPE1_DROP_P4_EN | PPE1_DROP_P3_EN | PPE1_DROP_P2_EN | PPE1_DROP_P1_EN | PPE1_DROP_P0_EN |
| Type  | RW   | RW               | RW               | RW               | RW               | RW               | RW              | RW              | RW              | RW              | RW              | RW              | RW              | RW              | RW              | RW              |
| Reset | 0    | 0                | 0                | 0                | 0                | 0                | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               |

| Bit(s) | Name             | Description                                                                       |
|--------|------------------|-----------------------------------------------------------------------------------|
| 31:16  | REVO             | Reserved                                                                          |
| 15     | REV              | Reserved                                                                          |
| 14     | PPE1_DROP_P14_EN | Enable PPE1 drop packet to port 14 due to RX ring full<br>0: Disable<br>1: Enable |
| 13     | PPE1_DROP_P13_EN | Enable PPE1 drop packet to port 13 due to RX ring full<br>0: Disable<br>1: Enable |
| 12     | PPE1_DROP_P12_EN | Enable PPE1 drop packet to port 12 due to RX ring full<br>0: Disable<br>1: Enable |
| 11     | PPE1_DROP_P11_EN | Enable PPE1 drop packet to port 11 due to RX ring full<br>0: Disable<br>1: Enable |
| 10     | PPE1_DROP_P10_EN | Enable PPE1 drop packet to port 10 due to RX ring full<br>0: Disable<br>1: Enable |
| 9      | PPE1_DROP_P9_EN  | Enable PPE1 drop packet to port 9 due to RX ring full<br>0: Disable<br>1: Enable  |
| 8      | PPE1_DROP_P8_EN  | Enable PPE1 drop packet to port 8 due to RX ring full<br>0: Disable<br>1: Enable  |
| 7      | PPE1_DROP_P7_EN  | Enable PPE1 drop packet to port 7 due to RX ring full                             |

| Bit(s) | Name            | Description                                                  |
|--------|-----------------|--------------------------------------------------------------|
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 6      | PPE1_DROP_P6_EN | <b>Enable PPE1 drop packet to port 6 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 5      | PPE1_DROP_P5_EN | <b>Enable PPE1 drop packet to port 5 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 4      | PPE1_DROP_P4_EN | <b>Enable PPE1 drop packet to port 4 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 3      | PPE1_DROP_P3_EN | <b>Enable PPE1 drop packet to port 3 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 2      | PPE1_DROP_P2_EN | <b>Enable PPE1 drop packet to port 2 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 1      | PPE1_DROP_P1_EN | <b>Enable PPE1 drop packet to port 1 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 0      | PPE1_DROP_P0_EN | <b>Enable PPE1 drop packet to port 0 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |

15100118      **PSE\_PPE2\_DROP**      **PPE2 drop packet enable port**      00000000

| Bit   | 31   | 30               | 29               | 28               | 27               | 26               | 25              | 24              | 23              | 22              | 21              | 20              | 19              | 18              | 17              | 16              |
|-------|------|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Name  | REV0 |                  |                  |                  |                  |                  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| Type  | RO   |                  |                  |                  |                  |                  |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| Reset | 0    | 0                | 0                | 0                | 0                | 0                | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               |
| Bit   | 15   | 14               | 13               | 12               | 11               | 10               | 9               | 8               | 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |
| Name  | REV  | PPE1_DROP_P14_EN | PPE1_DROP_P13_EN | PPE1_DROP_P12_EN | PPE1_DROP_P11_EN | PPE1_DROP_P10_EN | PPE1_DROP_P9_EN | PPE1_DROP_P8_EN | PPE1_DROP_P7_EN | PPE1_DROP_P6_EN | PPE1_DROP_P5_EN | PPE1_DROP_P4_EN | PPE1_DROP_P3_EN | PPE1_DROP_P2_EN | PPE1_DROP_P1_EN | PPE1_DROP_P0_EN |
| Type  | RW   | RW               | RW               | RW               | RW               | RW               | RW              | RW              | RW              | RW              | RW              | RW              | RW              | RW              | RW              | RW              |
| Reset | 0    | 0                | 0                | 0                | 0                | 0                | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               |

| Bit(s) | Name             | Description                                                                       |
|--------|------------------|-----------------------------------------------------------------------------------|
| 31:16  | REV0             | Reserved                                                                          |
| 15     | REV              | Reserved                                                                          |
| 14     | PPE1_DROP_P14_EN | Enable PPE2 drop packet to port 14 due to RX ring full<br>0: Disable<br>1: Enable |
| 13     | PPE1_DROP_P13_EN | Enable PPE2 drop packet to port 13 due to RX ring full<br>0: Disable<br>1: Enable |
| 12     | PPE1_DROP_P12_EN | Enable PPE2 drop packet to port 12 due to RX ring full<br>0: Disable<br>1: Enable |
| 11     | PPE1_DROP_P11_EN | Enable PPE2 drop packet to port 11 due to RX ring full<br>0: Disable<br>1: Enable |
| 10     | PPE1_DROP_P10_EN | Enable PPE2 drop packet to port 10 due to RX ring full<br>0: Disable<br>1: Enable |
| 9      | PPE1_DROP_P9_EN  | Enable PPE2 drop packet to port 9 due to RX ring full<br>0: Disable<br>1: Enable  |
| 8      | PPE1_DROP_P8_EN  | Enable PPE2 drop packet to port 8 due to RX ring full<br>0: Disable<br>1: Enable  |
| 7      | PPE1_DROP_P7_EN  | Enable PPE2 drop packet to port 7 due to RX ring full                             |

| Bit(s) | Name            | Description                                                  |
|--------|-----------------|--------------------------------------------------------------|
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 6      | PPE1_DROP_P6_EN | <b>Enable PPE2 drop packet to port 6 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 5      | PPE1_DROP_P5_EN | <b>Enable PPE2 drop packet to port 5 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 4      | PPE1_DROP_P4_EN | <b>Enable PPE2 drop packet to port 4 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 3      | PPE1_DROP_P3_EN | <b>Enable PPE2 drop packet to port 3 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 2      | PPE1_DROP_P2_EN | <b>Enable PPE2 drop packet to port 2 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 1      | PPE1_DROP_P1_EN | <b>Enable PPE2 drop packet to port 1 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |
| 0      | PPE1_DROP_P0_EN | <b>Enable PPE2 drop packet to port 0 due to RX ring full</b> |
|        |                 | 0: Disable                                                   |
|        |                 | 1: Enable                                                    |

**1510011C PSE\_DUMMY\_FLG\_CLR Per-Port PSE dummy page flag clear 00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26                       | 25                         | 24                       | 23                       | 22                       | 21                       | 20                       | 19                       | 18                       | 17                       | 16                       |
|-------|------|----|----|----|----|--------------------------|----------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| Name  | REV0 |    |    |    |    |                          |                            |                          |                          |                          |                          |                          |                          |                          |                          |                          |
| Type  | RO   |    |    |    |    |                          |                            |                          |                          |                          |                          |                          |                          |                          |                          |                          |
| Reset | 0    | 0  | 0  | 0  | 0  | 0                        | 0                          | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10                       | 9                          | 8                        | 7                        | 6                        | 5                        | 4                        | 3                        | 2                        | 1                        | 0                        |
| Name  | REV  |    |    |    |    | cdm1_dumy_pag_flag_clear | cdm1_1_dumy_pag_flag_clear | cdm2_dumy_pag_flag_clear | cdm3_dumy_pag_flag_clear | cdm4_dumy_pag_flag_clear | cdm5_dumy_pag_flag_clear | cdm6_dumy_pag_flag_clear | cdm7_dumy_pag_flag_clear | gdm1_dumy_pag_flag_clear | gdm2_dumy_pag_flag_clear | gdm3_dumy_pag_flag_clear |
| Type  | RW   |    |    |    |    | RW                       | RW                         | RW                       | RW                       | RW                       | RW                       | RW                       | RW                       | RW                       | RW                       | RW                       |
| Reset | 0    | 0  | 0  | 0  | 0  | 0                        | 0                          | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        |

| Bit(s) | Name                       | Description                                                                          |
|--------|----------------------------|--------------------------------------------------------------------------------------|
| 31:16  | REV0                       | Reserved                                                                             |
| 15:11  | REV                        | Reserved                                                                             |
| 10     | cdm1_dumy_pag_flag_clear   | <b>Enable cdm1 dummy page flag clear</b><br>0: Disable<br>1: Dummy page flag clear   |
| 9      | cdm1_1_dumy_pag_flag_clear | <b>Enable cdm1_1 dummy page flag clear</b><br>0: Disable<br>1: Dummy page flag clear |
| 8      | cdm2_dumy_pag_flag_clear   | <b>Enable cdm2 dummy page flag clear</b><br>0: Disable<br>1: Dummy page flag clear   |
| 7      | cdm3_dumy_pag_flag_clear   | <b>Enable cdm3 dummy page flag clear</b><br>0: Disable<br>1: Dummy page flag clear   |
| 6      | cdm4_dumy_pag_flag_clear   | <b>Enable cdm4 dummy page flag clear</b><br>0: Disable<br>1: Dummy page flag clear   |
| 5      | cdm5_dumy_pag_flag_clear   | <b>Enable cdm5 dummy page flag clear</b><br>0: Disable<br>1: Dummy page flag clear   |
| 4      | cdm6_dumy_pag_flag_clear   | <b>Enable cdm6 dummy page flag clear</b><br>0: Disable<br>1: Dummy page flag clear   |

| Bit(s) | Name                     | Description                                                                                |
|--------|--------------------------|--------------------------------------------------------------------------------------------|
| 3      | cdm7_dumy_pag_flag_clear | <b>Enable cdm7 dummy page flag clear</b><br><br>0: Disable<br><br>1: Dummy page flag clear |
| 2      | gdm1_dumy_pag_flag_clear | <b>Enable gdm1 dummy page flag clear</b><br><br>0: Disable<br><br>1: Dummy page flag clear |
| 1      | gdm2_dumy_pag_flag_clear | <b>Enable gdm2 dummy page flag clear</b><br><br>0: Disable<br><br>1: Dummy page flag clear |
| 0      | gdm3_dumy_pag_flag_clear | <b>Enable gdm3 dummy page flag clear</b><br><br>0: Disable<br><br>1: Dummy page flag clear |



**15100120 PSE\_DUMMY\_FLG Per-Port PSE dummy page flag 00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26                 | 25                   | 24                 | 23                 | 22                 | 21                 | 20                 | 19                 | 18                 | 17                 | 16                 |
|-------|------|----|----|----|----|--------------------|----------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| Name  | REVO |    |    |    |    |                    |                      |                    |                    |                    |                    |                    |                    |                    |                    |                    |
| Type  | RO   |    |    |    |    |                    |                      |                    |                    |                    |                    |                    |                    |                    |                    |                    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0                  | 0                    | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10                 | 9                    | 8                  | 7                  | 6                  | 5                  | 4                  | 3                  | 2                  | 1                  | 0                  |
| Name  | REVO |    |    |    |    | cdm1_dumy_pag_flag | cdm1_1_dumy_pag_flag | cdm2_dumy_pag_flag | cdm3_dumy_pag_flag | cdm4_dumy_pag_flag | cdm5_dumy_pag_flag | cdm6_dumy_pag_flag | cdm7_dumy_pag_flag | gdm1_dumy_pag_flag | gdm2_dumy_pag_flag | gdm3_dumy_pag_flag |
| Type  | RO   |    |    |    |    | RO                 | RO                   | RO                 | RO                 | RO                 | RO                 | RO                 | RO                 | RO                 | RO                 | RO                 |
| Reset | 0    | 0  | 0  | 0  | 0  | 0                  | 0                    | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  |

| Bit(s) | Name                 | Description                                                                                                               |
|--------|----------------------|---------------------------------------------------------------------------------------------------------------------------|
| 31:11  | REVO                 | <b>Reserved</b><br><br>0: No PSE dummy page case<br><br>1: PSE dummy page case assertion                                  |
| 10     | cdm1_dumy_pag_flag   | <b>cdm1 PSE dummy page case assertion flag</b><br><br>0: No PSE dummy page case<br><br>1: PSE dummy page case assertion   |
| 9      | cdm1_1_dumy_pag_flag | <b>cdm1_1 PSE dummy page case assertion flag</b><br><br>0: No PSE dummy page case<br><br>1: PSE dummy page case assertion |
| 8      | cdm2_dumy_pag_flag   | <b>cdm2 PSE dummy page case assertion flag</b><br><br>0: No PSE dummy page case<br><br>1: PSE dummy page case assertion   |
| 7      | cdm3_dumy_pag_flag   | <b>cdm3 PSE dummy page case assertion flag</b><br><br>0: No PSE dummy page case<br><br>1: PSE dummy page case assertion   |
| 6      | cdm4_dumy_pag_flag   | <b>cdm4 PSE dummy page case assertion flag</b><br><br>0: No PSE dummy page case<br><br>1: PSE dummy page case assertion   |
| 5      | cdm5_dumy_pag_flag   | <b>cdm5 PSE dummy page case assertion flag</b><br><br>0: No PSE dummy page case<br><br>1: PSE dummy page case assertion   |
| 4      | cdm6_dumy_pag_flag   | <b>cdm6 PSE dummy page case assertion flag</b><br><br>0: No PSE dummy page case<br><br>1: PSE dummy page case assertion   |

| Bit(s) | Name               | Description                                                                                                             |
|--------|--------------------|-------------------------------------------------------------------------------------------------------------------------|
| 3      | cdm7_dumy_pag_flag | <b>cdm7 PSE dummy page case assertion flag</b><br><br>0: No PSE dummy page case<br><br>1: PSE dummy page case assertion |
| 2      | gdm1_dumy_pag_flag | <b>gdm1 PSE dummy page case assertion flag</b><br><br>0: No PSE dummy page case<br><br>1: PSE dummy page case assertion |
| 1      | gdm2_dumy_pag_flag | <b>gdm2 PSE dummy page case assertion flag</b><br><br>0: No PSE dummy page case<br><br>1: PSE dummy page case assertion |
| 0      | gdm3_dumy_pag_flag | <b>gdm3 PSE dummy page case assertion flag</b><br><br>0: No PSE dummy page case<br><br>1: PSE dummy page case assertion |

| 1510012C | <u>PSE_IQ_REV9</u> |    |    |    |    | PSE input queue reservation part9 |    |    |    |    |    |    |    |    |    | 0000001A |
|----------|--------------------|----|----|----|----|-----------------------------------|----|----|----|----|----|----|----|----|----|----------|
| Bit      | 31                 | 30 | 29 | 28 | 27 | 26                                | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16       |
| Name     |                    |    |    |    |    |                                   |    |    |    |    |    |    |    |    |    |          |
| Type     |                    |    |    |    |    |                                   |    |    |    |    |    |    |    |    |    |          |
| Reset    |                    |    |    |    |    |                                   |    |    |    |    |    |    |    |    |    |          |
| Bit      | 15                 | 14 | 13 | 12 | 11 | 10                                | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0        |
| Name     |                    |    |    |    |    | P15_IQ_RES                        |    |    |    |    |    |    |    |    |    |          |
| Type     |                    |    |    |    |    | RW                                |    |    |    |    |    |    |    |    |    |          |
| Reset    |                    |    |    |    |    | 0                                 | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0        |

| Bit(s) | Name       | Description                                                                                                                                                                   |
|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10:0   | P15_IQ_RES | <b>Virtual input Q reservation</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2). |

15100130 FE\_GDM\_RXID1 FE GDM RXID control 1 00000000

| Bit   | 31                     | 30 | 29                     | 28 | 27                     | 26 | 25                     | 24 | 23                     | 22 | 21                     | 20 | 19                     | 18               | 17                     | 16 |
|-------|------------------------|----|------------------------|----|------------------------|----|------------------------|----|------------------------|----|------------------------|----|------------------------|------------------|------------------------|----|
| Name  | GDM_VLAN_PRI7_RXID_SEL |    | GDM_VLAN_PRI6_RXID_SEL |    | GDM_VLAN_PRI5_RXID_SEL |    | GDM_VLAN_PRI4_RXID_SEL |    | GDM_VLAN_PRI3_RXID_SEL |    | GDM_VLAN_PRI2_RXID_SEL |    | GDM_VLAN_PRI1_RXID_SEL |                  | GDM_VLAN_PRI0_RXID_SEL |    |
| Type  | RW                     |    | RW                     |    | RW                     |    | RW                     |    | RW                     |    | RW                     |    | RW                     |                  | RW                     |    |
| Reset | 0                      | 0  | 0                      | 0  | 0                      | 0  | 0                      | 0  | 0                      | 0  | 0                      | 0  | 0                      | 0                | 0                      | 0  |
| Bit   | 15                     | 14 | 13                     | 12 | 11                     | 10 | 9                      | 8  | 7                      | 6  | 5                      | 4  | 3                      | 2                | 1                      | 0  |
| Name  |                        |    |                        |    |                        |    |                        |    |                        |    | GDM_TCP_ACK_RXID_SEL   |    | GDM_TCP_ACK_WZPC       | GDM_RXID_PRI_SEL |                        |    |
| Type  |                        |    |                        |    |                        |    |                        |    |                        |    | RW                     |    | RW                     | RW               |                        |    |
| Reset |                        |    |                        |    |                        |    |                        |    |                        |    | 0                      | 0  | 0                      | 0                | 0                      | 0  |

| Bit(s) | Name                   | Description                                                                                                                                                                                                      |
|--------|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30  | GDM_VLAN_PRI7_RXID_SEL | <b>GDM RXID Select for VLAN Priority = 7</b><br>2'b00: Select PDMA RX Ring 0 (RXID=0)<br>2'b01: Select PDMA RX Ring 1 (RXID=1)<br>2'b10: Select PDMA RX Ring 2 (RXID=2)<br>2'b11: Select PDMA RX Ring 3 (RXID=3) |
| 29:28  | GDM_VLAN_PRI6_RXID_SEL | <b>GDM RXID Select for VLAN Priority = 6</b><br>2'b00: Select PDMA RX Ring 0 (RXID=0)<br>2'b01: Select PDMA RX Ring 1 (RXID=1)<br>2'b10: Select PDMA RX Ring 2 (RXID=2)<br>2'b11: Select PDMA RX Ring 3 (RXID=3) |
| 27:26  | GDM_VLAN_PRI5_RXID_SEL | <b>GDM RXID Select for VLAN Priority = 5</b><br>2'b00: Select PDMA RX Ring 0 (RXID=0)<br>2'b01: Select PDMA RX Ring 1 (RXID=1)<br>2'b10: Select PDMA RX Ring 2 (RXID=2)<br>2'b11: Select PDMA RX Ring 3 (RXID=3) |
| 25:24  | GDM_VLAN_PRI4_RXID_SEL | <b>GDM RXID Select for VLAN Priority = 4</b><br>2'b00: Select PDMA RX Ring 0 (RXID=0)<br>2'b01: Select PDMA RX Ring 1 (RXID=1)<br>2'b10: Select PDMA RX Ring 2 (RXID=2)<br>2'b11: Select PDMA RX Ring 3 (RXID=3) |
| 23:22  | GDM_VLAN_PRI3_RXID_SEL | <b>GDM RXID Select for VLAN Priority = 3</b><br>2'b00: Select PDMA RX Ring 0 (RXID=0)<br>2'b01: Select PDMA RX Ring 1 (RXID=1)                                                                                   |

| Bit(s) | Name                   | Description                                                         |
|--------|------------------------|---------------------------------------------------------------------|
| 21:20  | GDM_VLAN_PRI2_RXID_SEL | 2'b10: Select PDMA RX Ring 2 (RXID=2)                               |
|        |                        | 2'b11: Select PDMA RX Ring 3 (RXID=3)                               |
|        |                        | <b>GDM RXID Select for VLAN Priority = 2</b>                        |
|        |                        | 2'b00: Select PDMA RX Ring 0 (RXID=0)                               |
|        |                        | 2'b01: Select PDMA RX Ring 1 (RXID=1)                               |
|        |                        | 2'b10: Select PDMA RX Ring 2 (RXID=2)                               |
| 19:18  | GDM_VLAN_PRI1_RXID_SEL | 2'b11: Select PDMA RX Ring 3 (RXID=3)                               |
|        |                        | <b>GDM RXID Select for VLAN Priority = 1</b>                        |
|        |                        | 2'b00: Select PDMA RX Ring 0 (RXID=0)                               |
|        |                        | 2'b01: Select PDMA RX Ring 1 (RXID=1)                               |
|        |                        | 2'b10: Select PDMA RX Ring 2 (RXID=2)                               |
|        |                        | 2'b11: Select PDMA RX Ring 3 (RXID=3)                               |
| 17:16  | GDM_VLAN_PRI0_RXID_SEL | <b>GDM RXID Select for VLAN Priority = 0</b>                        |
|        |                        | 2'b00: Select PDMA RX Ring 0 (RXID=0)                               |
|        |                        | 2'b01: Select PDMA RX Ring 1 (RXID=1)                               |
|        |                        | 2'b10: Select PDMA RX Ring 2 (RXID=2)                               |
|        |                        | 2'b11: Select PDMA RX Ring 3 (RXID=3)                               |
| 5:4    | GDM_TCP_ACK_RXID_SEL   | <b>GDM RXID Select for TCP ACK</b>                                  |
|        |                        | 2'b00: Select PDMA RX Ring 0 (RXID=0)                               |
|        |                        | 2'b01: Select PDMA RX Ring 1 (RXID=1)                               |
|        |                        | 2'b10: Select PDMA RX Ring 2 (RXID=2)                               |
|        |                        | 2'b11: Select PDMA RX Ring 3 (RXID=3)                               |
| 3      | GDM_TCP_ACK_WZPC       | <b>GDM TCP ACK with zero payload check (L3 payload = L4 header)</b> |
| 2:0    | GDM_RXID_PRI_SEL       | <b>GDM RXID Select Priority Setting</b>                             |
|        |                        | Select Priority by PID/STAG, VLAN_PRI, and TCP_ACK                  |
|        |                        | 3'b000: PID/STAG                                                    |
|        |                        | 3'b001: VLAN_PRI --> PID/STAG                                       |
|        |                        | 3'b010: TCP_ACK --> PID/STAG                                        |
|        |                        | 3'b011: VLAN_PRI --> TCP_ACK --> PID/STAG                           |
|        |                        | 3'b100: TCP_ACK --> VLAN_PRI --> PID/STAG                           |

**15100134 FE\_GDM\_RXID2 FE GDM RXID control 2 00000000**

| Bit   | 31                 | 30 | 29                 | 28 | 27                 | 26 | 25                 | 24 | 23                 | 22 | 21                 | 20 | 19                 | 18 | 17                 | 16 |
|-------|--------------------|----|--------------------|----|--------------------|----|--------------------|----|--------------------|----|--------------------|----|--------------------|----|--------------------|----|
| Name  | GDM_STAG7_RXID_SEL |    | GDM_STAG6_RXID_SEL |    | GDM_STAG5_RXID_SEL |    | GDM_STAG4_RXID_SEL |    | GDM_STAG3_RXID_SEL |    | GDM_STAG2_RXID_SEL |    | GDM_STAG1_RXID_SEL |    | GDM_STAG0_RXID_SEL |    |
| Type  | RW                 |    | RW                 |    | RW                 |    | RW                 |    | RW                 |    | RW                 |    | RW                 |    | RW                 |    |
| Reset | 0                  | 0  | 0                  | 0  | 0                  | 0  | 0                  | 0  | 0                  | 0  | 0                  | 0  | 0                  | 0  | 0                  | 0  |
| Bit   | 15                 | 14 | 13                 | 12 | 11                 | 10 | 9                  | 8  | 7                  | 6  | 5                  | 4  | 3                  | 2  | 1                  | 0  |
| Name  |                    |    |                    |    |                    |    |                    |    |                    |    |                    |    | GDM_PID2_RXID_SEL  |    | GDM_PID1_RXID_SEL  |    |
| Type  |                    |    |                    |    |                    |    |                    |    |                    |    |                    |    | RW                 |    | RW                 |    |
| Reset |                    |    |                    |    |                    |    |                    |    |                    |    |                    |    | 0                  | 0  | 0                  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                                                             |
|--------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30  | GDM_STAG7_RXID_SEL | <b>GDM RXID Select for STAG = 7</b><br>2'b00: Select PDMA RX Ring 0 (RXID=0)<br>2'b01: Select PDMA RX Ring 1 (RXID=1)<br>2'b10: Select PDMA RX Ring 2 (RXID=2)<br>2'b11: Select PDMA RX Ring 3 (RXID=3) |
| 29:28  | GDM_STAG6_RXID_SEL | <b>GDM RXID Select for STAG = 6</b><br>2'b00: Select PDMA RX Ring 0 (RXID=0)<br>2'b01: Select PDMA RX Ring 1 (RXID=1)<br>2'b10: Select PDMA RX Ring 2 (RXID=2)<br>2'b11: Select PDMA RX Ring 3 (RXID=3) |
| 27:26  | GDM_STAG5_RXID_SEL | <b>GDM RXID Select for STAG = 5</b><br>2'b00: Select PDMA RX Ring 0 (RXID=0)<br>2'b01: Select PDMA RX Ring 1 (RXID=1)<br>2'b10: Select PDMA RX Ring 2 (RXID=2)<br>2'b11: Select PDMA RX Ring 3 (RXID=3) |
| 25:24  | GDM_STAG4_RXID_SEL | <b>GDM RXID Select for STAG = 4</b><br>2'b00: Select PDMA RX Ring 0 (RXID=0)<br>2'b01: Select PDMA RX Ring 1 (RXID=1)<br>2'b10: Select PDMA RX Ring 2 (RXID=2)<br>2'b11: Select PDMA RX Ring 3 (RXID=3) |
| 23:22  | GDM_STAG3_RXID_SEL | <b>GDM RXID Select for STAG = 3</b><br>2'b00: Select PDMA RX Ring 0 (RXID=0)<br>2'b01: Select PDMA RX Ring 1 (RXID=1)<br>2'b10: Select PDMA RX Ring 2 (RXID=2)                                          |

| Bit(s) | Name               | Description                                   |
|--------|--------------------|-----------------------------------------------|
|        |                    | 2'b11: Select PDMA RX Ring 3 (RXID=3)         |
| 21:20  | GDM_STAG2_RXID_SEL | <b>GDM RXID Select for STAG = 2</b>           |
|        |                    | 2'b00: Select PDMA RX Ring 0 (RXID=0)         |
|        |                    | 2'b01: Select PDMA RX Ring 1 (RXID=1)         |
|        |                    | 2'b10: Select PDMA RX Ring 2 (RXID=2)         |
|        |                    | 2'b11: Select PDMA RX Ring 3 (RXID=3)         |
| 19:18  | GDM_STAG1_RXID_SEL | <b>GDM RXID Select for STAG = 1</b>           |
|        |                    | 2'b00: Select PDMA RX Ring 0 (RXID=0)         |
|        |                    | 2'b01: Select PDMA RX Ring 1 (RXID=1)         |
|        |                    | 2'b10: Select PDMA RX Ring 2 (RXID=2)         |
|        |                    | 2'b11: Select PDMA RX Ring 3 (RXID=3)         |
| 17:16  | GDM_STAG0_RXID_SEL | <b>GDM RXID Select for STAG = 0</b>           |
|        |                    | 2'b00: Select PDMA RX Ring 0 (RXID=0)         |
|        |                    | 2'b01: Select PDMA RX Ring 1 (RXID=1)         |
|        |                    | 2'b10: Select PDMA RX Ring 2 (RXID=2)         |
|        |                    | 2'b11: Select PDMA RX Ring 3 (RXID=3)         |
| 3:2    | GDM_PID2_RXID_SEL  | <b>GDM RXID Select for GDM2 (Port ID = 2)</b> |
|        |                    | 2'b00: Select PDMA RX Ring 0 (RXID=0)         |
|        |                    | 2'b01: Select PDMA RX Ring 1 (RXID=1)         |
|        |                    | 2'b10: Select PDMA RX Ring 2 (RXID=2)         |
|        |                    | 2'b11: Select PDMA RX Ring 3 (RXID=3)         |
| 1:0    | GDM_PID1_RXID_SEL  | <b>GDM RXID Select for GDM1 (Port ID = 1)</b> |
|        |                    | 2'b00: Select PDMA RX Ring 0 (RXID=0)         |
|        |                    | 2'b01: Select PDMA RX Ring 1 (RXID=1)         |
|        |                    | 2'b10: Select PDMA RX Ring 2 (RXID=2)         |
|        |                    | 2'b11: Select PDMA RX Ring 3 (RXID=3)         |

**15100140**      **PSE IQ\_REV1**      **PSE input queue reservation part1**      **001A0009**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26        | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|-----------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P1_IQ_RES |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10        | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P0_IQ_RES |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  |

| Bit(s) | Name      | Description                                                                                                                                                                   |
|--------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P1_IQ_RES | <b>Virtual input Q reservation</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2). |
| 10:0   | P0_IQ_RES | <b>Virtual input Q reservation</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2). |

**15100144**      **PSE IQ\_REV2**      **PSE input queue reservation part2**      **07FF001A**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26        | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|-----------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P3_IQ_RES |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 1         | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10        | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P2_IQ_RES |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  |

| Bit(s) | Name      | Description                                                                                                                                                                   |
|--------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P3_IQ_RES | <b>Virtual input Q reservation</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2). |
| 10:0   | P2_IQ_RES | <b>Virtual input Q reservation</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2). |

**15100148 PSE IQ\_REV3 PSE input queue reservation part3 000907FF**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26        | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|-----------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P5_IQ_RES |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10        | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P4_IQ_RES |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 1         | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name      | Description                                                                                                                                                                   |
|--------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P5_IQ_RES | <b>Virtual input Q reservation</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2). |
| 10:0   | P4_IQ_RES | <b>Virtual input Q reservation</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2). |

**1510014C PSE IQ\_REV4 PSE input queue reservation part4 00090009**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26        | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|-----------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P7_IQ_RES |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10        | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P6_IQ_RES |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  |

| Bit(s) | Name      | Description                                                                                                                                                                   |
|--------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P7_IQ_RES | <b>Virtual input Q reservation</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2). |
| 10:0   | P6_IQ_RES | <b>Virtual input Q reservation</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2). |



**15100150 PSE\_IQ\_REV5 PSE input queue reservation part5 00090009**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26        | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|-----------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P9_IQ_RES |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10        | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P8_IQ_RES |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  |

| Bit(s) | Name      | Description                                                                                                                                                                   |
|--------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P9_IQ_RES | <b>Virtual input Q reservation</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2). |
| 10:0   | P8_IQ_RES | <b>Virtual input Q reservation</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2). |

**15100154 PSE\_IQ\_REV6 PSE input queue reservation part6 00090009**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26         | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P11_IQ_RES |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10         | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P10_IQ_RES |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  |

| Bit(s) | Name       | Description                                                                                                                                                                   |
|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P11_IQ_RES | <b>Virtual input Q reservation</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2). |
| 10:0   | P10_IQ_RES | <b>Virtual input Q reservation</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2). |

**15100158 PSE\_IQ\_REV7 PSE input queue reservation part7 000907FF**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26         | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P13_IQ_RES |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10         | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P12_IQ_RES |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 1          | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name       | Description                                                                                                                                                                   |
|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P13_IQ_RES | <b>Virtual input Q reservation</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2). |
| 10:0   | P12_IQ_RES | <b>Virtual input Q reservation</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2). |

**1510015C PSE\_IQ\_REV8 PSE input queue reservation part8 00200009**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26         | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | FREE_DROP  |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10         | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P14_IQ_RES |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  |

| Bit(s) | Name       | Description                                                                                                                                                                   |
|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | FREE_DROP  | <b>Free Buffer Drop Threshold</b>                                                                                                                                             |
| 10:0   | P14_IQ_RES | <b>Virtual input Q reservation</b><br><br>[note*] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2). |

**15100160 PSE\_OQ\_TH1 PSE output queue threshold part1 000F000A**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26       | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P1_OQ_TH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW       |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10       | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P0_OQ_TH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW       |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0  |

| Bit(s) | Name     | Description                                                                                                                                                                  |
|--------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P1_OQ_TH | <b>Output Queue FC Threshold</b><br><br>[note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH. |
| 10:0   | P0_OQ_TH | <b>Output Queue FC Threshold</b><br><br>[note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH. |

**15100164 PSE\_OQ\_TH2 PSE output queue threshold part2 001A000F**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26       | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P3_OQ_TH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW       |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0        | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10       | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P2_OQ_TH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW       |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name     | Description                                                                                                                                                                  |
|--------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P3_OQ_TH | <b>Output Queue FC Threshold</b><br><br>[note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH. |
| 10:0   | P2_OQ_TH | <b>Output Queue FC Threshold</b><br><br>[note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH. |

**15100168 PSE\_OQ\_TH3 PSE output queue threshold part3 000F001A**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26       | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P5_OQ_TH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW       |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10       | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P4_OQ_TH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW       |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0        | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  |

| Bit(s) | Name     | Description                                                                                                                                                                  |
|--------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P5_OQ_TH | <b>Output Queue FC Threshold</b><br><br>[note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH. |
| 10:0   | P4_OQ_TH | <b>Output Queue FC Threshold</b><br><br>[note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH. |

**1510016C PSE\_OQ\_TH4 PSE output queue threshold part4 07FF000F**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26       | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P7_OQ_TH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW       |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 1        | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10       | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P6_OQ_TH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW       |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name     | Description                                                                                                                                                                  |
|--------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P7_OQ_TH | <b>Output Queue FC Threshold</b><br><br>[note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH. |
| 10:0   | P6_OQ_TH | <b>Output Queue FC Threshold</b><br><br>[note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH. |

**15100170 PSE\_OQ\_TH5 PSE output queue threshold part5 000F000F**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26       | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P9_OQ_TH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW       |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10       | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P8_OQ_TH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW       |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name     | Description                                                                                                                                                                  |
|--------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P9_OQ_TH | <b>Output Queue FC Threshold</b><br><br>[note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH. |
| 10:0   | P8_OQ_TH | <b>Output Queue FC Threshold</b><br><br>[note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH. |

**15100174 PSE\_OQ\_TH6 PSE output queue threshold part6 07FF000F**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26        | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|-----------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P11_OQ_TH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 1         | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10        | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P10_OQ_TH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name      | Description                                                                                                                                                                  |
|--------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P11_OQ_TH | <b>Output Queue FC Threshold</b><br><br>[note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH. |
| 10:0   | P10_OQ_TH | <b>Output Queue FC Threshold</b><br><br>[note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH. |

**15100178      PSE\_OQ\_TH7      PSE output queue threshold part7      000F001A**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26        | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|-----------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P13_OQ_TH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10        | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P12_OQ_TH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  |

| Bit(s) | Name      | Description                                                                                                                                                                  |
|--------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P13_OQ_TH | <b>Output Queue FC Threshold</b><br><br>[note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH. |
| 10:0   | P12_OQ_TH | <b>Output Queue FC Threshold</b><br><br>[note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH. |

**1510017C      PSE\_OQ\_TH8      PSE output queue threshold part8      000F000F**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26        | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|-----------|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    | P15_OQ_TH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10        | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | P14_OQ_TH |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name      | Description                                                                                                                                                                  |
|--------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:16  | P15_OQ_TH | <b>Reserved</b>                                                                                                                                                              |
| 10:0   | P14_OQ_TH | <b>Output Queue FC Threshold</b><br><br>[note*] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH. |

**15100180 PSE IQ\_STA1 PSE input queue status part1 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | P1_IQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | P0_IQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                |
|--------|------------|----------------------------|
| 27:16  | P1_IQ_PCNT | Virtual input Q page count |
| 11:0   | P0_IQ_PCNT | Virtual input Q page count |

**15100184 PSE IQ\_STA2 PSE input queue status part2 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | P3_IQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | P2_IQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                |
|--------|------------|----------------------------|
| 27:16  | P3_IQ_PCNT | Virtual input Q page count |
| 11:0   | P2_IQ_PCNT | Virtual input Q page count |

**15100188 PSE IQ\_STA3 PSE input queue status part3 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | P5_IQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | P4_IQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                |
|--------|------------|----------------------------|
| 27:16  | P5_IQ_PCNT | Virtual input Q page count |
| 11:0   | P4_IQ_PCNT | Virtual input Q page count |

**1510018C PSE IQ\_STA4 PSE input queue status part4 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | P7_IQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | P6_IQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                |
|--------|------------|----------------------------|
| 27:16  | P7_IQ_PCNT | Virtual input Q page count |
| 11:0   | P6_IQ_PCNT | Virtual input Q page count |



**15100190 PSE\_IQ\_STA5 PSE input queue status part5 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | P9_IQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | P8_IQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                |
|--------|------------|----------------------------|
| 27:16  | P9_IQ_PCNT | Virtual input Q page count |
| 11:0   | P8_IQ_PCNT | Virtual input Q page count |

**15100194 PSE\_IQ\_STA6 PSE input queue status part6 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | P11_IQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | P10_IQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                |
|--------|-------------|----------------------------|
| 27:16  | P11_IQ_PCNT | Virtual input Q page count |
| 11:0   | P10_IQ_PCNT | Virtual input Q page count |

**15100198      PSE\_IQ\_STA7      PSE input queue status part7      00000000**

| Bit   | 31 | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | P13_IQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | P12_IQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                |
|--------|-------------|----------------------------|
| 27:16  | P13_IQ_PCNT | Virtual input Q page count |
| 11:0   | P12_IQ_PCNT | Virtual input Q page count |

**1510019C      PSE\_IQ\_STA8      PSE input queue status part8      00000000**

| Bit   | 31 | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | P15_IQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | P14_IQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                |
|--------|-------------|----------------------------|
| 27:16  | P15_IQ_PCNT | Virtual input Q page count |
| 11:0   | P14_IQ_PCNT |                            |

**151001A0      PSE\_OQ\_STA1      PSE output queue status part1      00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | P1_OQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | P0_OQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description         |
|--------|------------|---------------------|
| 27:16  | P1_OQ_PCNT | Output Q page count |
| 11:0   | P0_OQ_PCNT | Output Q page count |

**151001A4      PSE\_OQ\_STA2      PSE output queue status part2      00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | P3_OQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | P2_OQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description         |
|--------|------------|---------------------|
| 27:16  | P3_OQ_PCNT | Output Q page count |
| 11:0   | P2_OQ_PCNT | Output Q page count |

**151001A8      PSE\_OQ\_STA3      PSE output queue status part3      00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | P5_OQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | P4_OQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description         |
|--------|------------|---------------------|
| 27:16  | P5_OQ_PCNT | Output Q page count |
| 11:0   | P4_OQ_PCNT | Output Q page count |

**151001AC      PSE\_OQ\_STA4      PSE output queue status part4      00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | P7_OQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | P6_OQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description         |
|--------|------------|---------------------|
| 27:16  | P7_OQ_PCNT | Output Q page count |
| 11:0   | P6_OQ_PCNT | Output Q page count |

**151001B0      PSE\_OQ\_STA5      PSE output queue status part5      00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | P9_OQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | P8_OQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description         |
|--------|------------|---------------------|
| 27:16  | P9_OQ_PCNT | Output Q page count |
| 11:0   | P8_OQ_PCNT | Output Q page count |

**151001B4      PSE\_OQ\_STA6      PSE output queue status part6      00000000**

| Bit   | 31 | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | P11_OQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | P10_OQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description         |
|--------|-------------|---------------------|
| 27:16  | P11_OQ_PCNT | Output Q page count |
| 11:0   | P10_OQ_PCNT | Output Q page count |

**151001B8      PSE\_OQ\_STA7      PSE output queue status part7      00000000**

| Bit   | 31 | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | P13_OQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | P12_OQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description         |
|--------|-------------|---------------------|
| 27:16  | P13_OQ_PCNT | Output Q page count |
| 11:0   | P12_OQ_PCNT | Output Q page count |

**151001BC      PSE\_OQ\_STA8      PSE output queue status part8      00000000**

| Bit   | 31 | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | P15_OQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | P14_OQ_PCNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description         |
|--------|-------------|---------------------|
| 27:16  | P15_OQ_PCNT | Output Q page count |
| 11:0   | P14_OQ_PCNT | Output Q page count |

**151001C0      PSE\_TDM\_TBL0      PSE TDM arbiter table0      FA521C43**

| Bit          | 31        | 30 | 29 | 28 | 27        | 26 | 25 | 24 | 23        | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
|--------------|-----------|----|----|----|-----------|----|----|----|-----------|----|----|----|-----------|----|----|----|
| <b>Name</b>  | TDM_TBL_7 |    |    |    | TDM_TBL_6 |    |    |    | TDM_TBL_5 |    |    |    | TDM_TBL_4 |    |    |    |
| <b>Type</b>  | RW        |    |    |    | RW        |    |    |    | RW        |    |    |    | RW        |    |    |    |
| <b>Reset</b> | 1         | 1  | 1  | 1  | 1         | 0  | 1  | 0  | 0         | 1  | 0  | 1  | 0         | 0  | 1  | 0  |
| Bit          | 15        | 14 | 13 | 12 | 11        | 10 | 9  | 8  | 7         | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| <b>Name</b>  | TDM_TBL_3 |    |    |    | TDM_TBL_2 |    |    |    | TDM_TBL_1 |    |    |    | TDM_TBL_0 |    |    |    |
| <b>Type</b>  | RW        |    |    |    | RW        |    |    |    | RW        |    |    |    | RW        |    |    |    |
| <b>Reset</b> | 0         | 0  | 0  | 1  | 1         | 1  | 0  | 0  | 0         | 1  | 0  | 0  | 0         | 0  | 1  | 1  |

| Bit(s) | Name      | Description                   |
|--------|-----------|-------------------------------|
| 31:28  | TDM_TBL_7 | PSE TDM arbiter table entry 7 |
| 27:24  | TDM_TBL_6 | PSE TDM arbiter table entry 6 |
| 23:20  | TDM_TBL_5 | PSE TDM arbiter table entry 5 |
| 19:16  | TDM_TBL_4 | PSE TDM arbiter table entry 4 |
| 15:12  | TDM_TBL_3 | PSE TDM arbiter table entry 3 |
| 11:8   | TDM_TBL_2 | PSE TDM arbiter table entry 2 |
| 7:4    | TDM_TBL_1 | PSE TDM arbiter table entry 1 |
| 3:0    | TDM_TBL_0 | PSE TDM arbiter table entry 0 |

**151001C4      PSE\_TDM\_TBL1      PSE TDM arbiter table1      E621C438**

| Bit          | 31         | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
|--------------|------------|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|----|----|
| <b>Name</b>  | TDM_TBL_15 |    |    |    | TDM_TBL_14 |    |    |    | TDM_TBL_13 |    |    |    | TDM_TBL_12 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 1          | 1  | 1  | 0  | 0          | 1  | 1  | 0  | 0          | 0  | 1  | 0  | 0          | 0  | 0  | 1  |
| Bit          | 15         | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| <b>Name</b>  | TDM_TBL_11 |    |    |    | TDM_TBL_10 |    |    |    | TDM_TBL_9  |    |    |    | TDM_TBL_8  |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 1          | 1  | 0  | 0  | 0          | 1  | 0  | 0  | 0          | 0  | 1  | 1  | 1          | 0  | 0  | 0  |

| Bit(s) | Name       | Description                    |
|--------|------------|--------------------------------|
| 31:28  | TDM_TBL_15 | PSE TDM arbiter table entry 15 |
| 27:24  | TDM_TBL_14 | PSE TDM arbiter table entry 14 |
| 23:20  | TDM_TBL_13 | PSE TDM arbiter table entry 13 |
| 19:16  | TDM_TBL_12 | PSE TDM arbiter table entry 12 |
| 15:12  | TDM_TBL_11 | PSE TDM arbiter table entry 11 |
| 11:8   | TDM_TBL_10 | PSE TDM arbiter table entry 10 |
| 7:4    | TDM_TBL_9  | PSE TDM arbiter table entry 9  |
| 3:0    | TDM_TBL_8  | PSE TDM arbiter table entry 8  |



**151001C8      PSE\_TDM\_TBL2      PSE TDM arbiter table2      521C43D9**

| Bit          | 31         | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
|--------------|------------|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|----|----|
| <b>Name</b>  | TDM_TBL_23 |    |    |    | TDM_TBL_22 |    |    |    | TDM_TBL_21 |    |    |    | TDM_TBL_20 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 0          | 1  | 0  | 1  | 0          | 0  | 1  | 0  | 0          | 0  | 0  | 1  | 1          | 1  | 0  | 0  |
| Bit          | 15         | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| <b>Name</b>  | TDM_TBL_19 |    |    |    | TDM_TBL_18 |    |    |    | TDM_TBL_17 |    |    |    | TDM_TBL_16 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 0          | 1  | 0  | 0  | 0          | 0  | 1  | 1  | 1          | 1  | 0  | 1  | 1          | 0  | 0  | 1  |

| Bit(s) | Name       | Description                    |
|--------|------------|--------------------------------|
| 31:28  | TDM_TBL_23 | PSE TDM arbiter table entry 23 |
| 27:24  | TDM_TBL_22 | PSE TDM arbiter table entry 22 |
| 23:20  | TDM_TBL_21 | PSE TDM arbiter table entry 21 |
| 19:16  | TDM_TBL_20 | PSE TDM arbiter table entry 20 |
| 15:12  | TDM_TBL_19 | PSE TDM arbiter table entry 19 |
| 11:8   | TDM_TBL_18 | PSE TDM arbiter table entry 18 |
| 7:4    | TDM_TBL_17 | PSE TDM arbiter table entry 17 |
| 3:0    | TDM_TBL_16 | PSE TDM arbiter table entry 16 |

**151001CC      PSE\_TDM\_TBL3      PSE TDM arbiter table3      21F4398A**

| Bit          | 31         | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
|--------------|------------|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|----|----|
| <b>Name</b>  | TDM_TBL_31 |    |    |    | TDM_TBL_30 |    |    |    | TDM_TBL_29 |    |    |    | TDM_TBL_28 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 0          | 0  | 1  | 0  | 0          | 0  | 0  | 1  | 1          | 1  | 1  | 1  | 0          | 1  | 0  | 0  |
| Bit          | 15         | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| <b>Name</b>  | TDM_TBL_27 |    |    |    | TDM_TBL_26 |    |    |    | TDM_TBL_25 |    |    |    | TDM_TBL_24 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 0          | 0  | 1  | 1  | 1          | 0  | 0  | 1  | 1          | 0  | 0  | 0  | 1          | 0  | 1  | 0  |

| Bit(s) | Name       | Description                    |
|--------|------------|--------------------------------|
| 31:28  | TDM_TBL_31 | PSE TDM arbiter table entry 31 |
| 27:24  | TDM_TBL_30 | PSE TDM arbiter table entry 30 |
| 23:20  | TDM_TBL_29 | PSE TDM arbiter table entry 29 |
| 19:16  | TDM_TBL_28 | PSE TDM arbiter table entry 28 |
| 15:12  | TDM_TBL_27 | PSE TDM arbiter table entry 27 |
| 11:8   | TDM_TBL_26 | PSE TDM arbiter table entry 26 |
| 7:4    | TDM_TBL_25 | PSE TDM arbiter table entry 25 |
| 3:0    | TDM_TBL_24 | PSE TDM arbiter table entry 24 |

**151001D0      PSE\_TDM\_TBL4      PSE TDM arbiter table4      2143CDE6**

| Bit          | 31         | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
|--------------|------------|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|----|----|
| <b>Name</b>  | TDM_TBL_39 |    |    |    | TDM_TBL_38 |    |    |    | TDM_TBL_37 |    |    |    | TDM_TBL_36 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 0          | 0  | 1  | 0  | 0          | 0  | 0  | 1  | 0          | 1  | 0  | 0  | 0          | 0  | 1  | 1  |
| Bit          | 15         | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| <b>Name</b>  | TDM_TBL_35 |    |    |    | TDM_TBL_34 |    |    |    | TDM_TBL_33 |    |    |    | TDM_TBL_32 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 1          | 1  | 0  | 0  | 1          | 1  | 0  | 1  | 1          | 1  | 1  | 0  | 0          | 1  | 1  | 0  |

| Bit(s) | Name       | Description                    |
|--------|------------|--------------------------------|
| 31:28  | TDM_TBL_39 | PSE TDM arbiter table entry 39 |
| 27:24  | TDM_TBL_38 | PSE TDM arbiter table entry 38 |
| 23:20  | TDM_TBL_37 | PSE TDM arbiter table entry 37 |
| 19:16  | TDM_TBL_36 | PSE TDM arbiter table entry 36 |
| 15:12  | TDM_TBL_35 | PSE TDM arbiter table entry 35 |
| 11:8   | TDM_TBL_34 | PSE TDM arbiter table entry 34 |
| 7:4    | TDM_TBL_33 | PSE TDM arbiter table entry 33 |
| 3:0    | TDM_TBL_32 | PSE TDM arbiter table entry 32 |

**151001D4      PSE\_TDM\_TBL5      PSE TDM arbiter table5      143C98A5**

| Bit          | 31         | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
|--------------|------------|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|----|----|
| <b>Name</b>  | TDM_TBL_47 |    |    |    | TDM_TBL_46 |    |    |    | TDM_TBL_45 |    |    |    | TDM_TBL_44 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 0          | 0  | 0  | 1  | 0          | 1  | 0  | 0  | 0          | 0  | 1  | 1  | 1          | 1  | 0  | 0  |
| Bit          | 15         | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| <b>Name</b>  | TDM_TBL_43 |    |    |    | TDM_TBL_42 |    |    |    | TDM_TBL_41 |    |    |    | TDM_TBL_40 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 1          | 0  | 0  | 1  | 1          | 0  | 0  | 0  | 1          | 0  | 1  | 0  | 0          | 1  | 0  | 1  |

| Bit(s) | Name       | Description                    |
|--------|------------|--------------------------------|
| 31:28  | TDM_TBL_47 | PSE TDM arbiter table entry 47 |
| 27:24  | TDM_TBL_46 | PSE TDM arbiter table entry 46 |
| 23:20  | TDM_TBL_45 | PSE TDM arbiter table entry 45 |
| 19:16  | TDM_TBL_44 | PSE TDM arbiter table entry 44 |
| 15:12  | TDM_TBL_43 | PSE TDM arbiter table entry 43 |
| 11:8   | TDM_TBL_42 | PSE TDM arbiter table entry 42 |
| 7:4    | TDM_TBL_41 | PSE TDM arbiter table entry 41 |
| 3:0    | TDM_TBL_40 | PSE TDM arbiter table entry 40 |

**151001D8      PSE\_TDM\_TBL6      PSE TDM arbiter table6      F3C8DE62**

| Bit          | 31         | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
|--------------|------------|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|----|----|
| <b>Name</b>  | TDM_TBL_55 |    |    |    | TDM_TBL_54 |    |    |    | TDM_TBL_53 |    |    |    | TDM_TBL_52 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 1          | 1  | 1  | 1  | 0          | 0  | 1  | 1  | 1          | 1  | 0  | 0  | 1          | 0  | 0  | 0  |
| Bit          | 15         | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| <b>Name</b>  | TDM_TBL_51 |    |    |    | TDM_TBL_50 |    |    |    | TDM_TBL_49 |    |    |    | TDM_TBL_48 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 1          | 1  | 0  | 1  | 1          | 1  | 1  | 0  | 0          | 1  | 1  | 0  | 0          | 0  | 1  | 0  |

| Bit(s) | Name       | Description                    |
|--------|------------|--------------------------------|
| 31:28  | TDM_TBL_55 | PSE TDM arbiter table entry 55 |
| 27:24  | TDM_TBL_54 | PSE TDM arbiter table entry 54 |
| 23:20  | TDM_TBL_53 | PSE TDM arbiter table entry 53 |
| 19:16  | TDM_TBL_52 | PSE TDM arbiter table entry 52 |
| 15:12  | TDM_TBL_51 | PSE TDM arbiter table entry 51 |
| 11:8   | TDM_TBL_50 | PSE TDM arbiter table entry 50 |
| 7:4    | TDM_TBL_49 | PSE TDM arbiter table entry 49 |
| 3:0    | TDM_TBL_48 | PSE TDM arbiter table entry 48 |

**151001DC      PSE\_TDM\_TBL7      PSE TDM arbiter table7      C4D9A521**

| Bit          | 31         | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
|--------------|------------|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|----|----|
| <b>Name</b>  | TDM_TBL_63 |    |    |    | TDM_TBL_62 |    |    |    | TDM_TBL_61 |    |    |    | TDM_TBL_60 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 1          | 1  | 0  | 0  | 0          | 1  | 0  | 0  | 1          | 1  | 0  | 1  | 1          | 0  | 0  | 1  |
| Bit          | 15         | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| <b>Name</b>  | TDM_TBL_59 |    |    |    | TDM_TBL_58 |    |    |    | TDM_TBL_57 |    |    |    | TDM_TBL_56 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 1          | 0  | 1  | 0  | 0          | 1  | 0  | 1  | 0          | 0  | 1  | 0  | 0          | 0  | 0  | 1  |

| Bit(s) | Name       | Description                    |
|--------|------------|--------------------------------|
| 31:28  | TDM_TBL_63 | PSE TDM arbiter table entry 63 |
| 27:24  | TDM_TBL_62 | PSE TDM arbiter table entry 62 |
| 23:20  | TDM_TBL_61 | PSE TDM arbiter table entry 61 |
| 19:16  | TDM_TBL_60 | PSE TDM arbiter table entry 60 |
| 15:12  | TDM_TBL_59 | PSE TDM arbiter table entry 59 |
| 11:8   | TDM_TBL_58 | PSE TDM arbiter table entry 58 |
| 7:4    | TDM_TBL_57 | PSE TDM arbiter table entry 57 |
| 3:0    | TDM_TBL_56 | PSE TDM arbiter table entry 56 |

**151001E0      PSE\_SP\_CFG0      PSE strict priority configuration 0      65C43F12**

| Bit          | 31         | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
|--------------|------------|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|----|----|
| <b>Name</b>  | PRIORITY_7 |    |    |    | PRIORITY_6 |    |    |    | PRIORITY_5 |    |    |    | PRIORITY_4 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 0          | 1  | 1  | 0  | 0          | 1  | 0  | 1  | 1          | 1  | 0  | 0  | 0          | 1  | 0  | 0  |
| Bit          | 15         | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| <b>Name</b>  | PRIORITY_3 |    |    |    | PRIORITY_2 |    |    |    | PRIORITY_1 |    |    |    | PRIORITY_0 |    |    |    |
| <b>Type</b>  | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    |
| <b>Reset</b> | 0          | 0  | 1  | 1  | 1          | 1  | 1  | 1  | 0          | 0  | 0  | 1  | 0          | 0  | 1  | 0  |

| Bit(s) | Name       | Description                |
|--------|------------|----------------------------|
| 31:28  | PRIORITY_7 | PSE port num at priority 7 |
| 27:24  | PRIORITY_6 | PSE port num at priority 6 |
| 23:20  | PRIORITY_5 | PSE port num at priority 5 |
| 19:16  | PRIORITY_4 | PSE port num at priority 4 |
| 15:12  | PRIORITY_3 | PSE port num at priority 3 |
| 11:8   | PRIORITY_2 | PSE port num at priority 2 |
| 7:4    | PRIORITY_1 | PSE port num at priority 1 |
| 3:0    | PRIORITY_0 | PSE port num at priority 0 |

**151001E4      PSE\_SP\_CFG1      PSE strict priority configuration 1      77EA0D98**

| Bit          | 31          | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19          | 18 | 17 | 16 |
|--------------|-------------|----|----|----|-------------|----|----|----|-------------|----|----|----|-------------|----|----|----|
| <b>Name</b>  | PRIORITY_15 |    |    |    | PRIORITY_14 |    |    |    | PRIORITY_13 |    |    |    | PRIORITY_12 |    |    |    |
| <b>Type</b>  | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    |
| <b>Reset</b> | 0           | 1  | 1  | 1  | 0           | 1  | 1  | 1  | 1           | 1  | 1  | 0  | 1           | 0  | 1  | 0  |
| <b>Bit</b>   | 15          | 14 | 13 | 12 | 11          | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3           | 2  | 1  | 0  |
| <b>Name</b>  | PRIORITY_11 |    |    |    | PRIORITY_10 |    |    |    | PRIORITY_9  |    |    |    | PRIORITY_8  |    |    |    |
| <b>Type</b>  | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    |
| <b>Reset</b> | 0           | 0  | 0  | 0  | 1           | 1  | 0  | 1  | 1           | 0  | 0  | 1  | 1           | 0  | 0  | 0  |

| Bit(s) | Name        | Description                 |
|--------|-------------|-----------------------------|
| 31:28  | PRIORITY_15 | PSE port num at priority 15 |
| 27:24  | PRIORITY_14 | PSE port num at priority 14 |
| 23:20  | PRIORITY_13 | PSE port num at priority 13 |
| 19:16  | PRIORITY_12 | PSE port num at priority 12 |
| 15:12  | PRIORITY_11 | PSE port num at priority 11 |
| 11:8   | PRIORITY_10 | PSE port num at priority 10 |
| 7:4    | PRIORITY_9  | PSE port num at priority 9  |
| 3:0    | PRIORITY_8  | PSE port num at priority 8  |



**151001E8      PSE\_TDM\_CFG      PSE TDM arbiter configuration      00590003**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22              | 21 | 20 | 19 | 18 | 17            | 16             |
|-------|----|----|----|----|----|----|----|----|----|-----------------|----|----|----|----|---------------|----------------|
| Name  |    |    |    |    |    |    |    |    |    | PSE_TDM_ARB_NUM |    |    |    |    |               |                |
| Type  |    |    |    |    |    |    |    |    |    | RW              |    |    |    |    |               |                |
| Reset |    |    |    |    |    |    |    |    |    | 1               | 0  | 1  | 1  | 0  | 0             | 1              |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6               | 5  | 4  | 3  | 2  | 1             | 0              |
| Name  |    |    |    |    |    |    |    |    |    |                 |    |    |    |    | PSE_SP_ARB_EN | PSE_TDM_ARB_EN |
| Type  |    |    |    |    |    |    |    |    |    |                 |    |    |    |    | RW            | RW             |
| Reset |    |    |    |    |    |    |    |    |    |                 |    |    |    |    | 1             | 1              |

| Bit(s) | Name            | Description                                                                                                                                             |
|--------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 22:16  | PSE_TDM_ARB_NUM | <b>TDM table entry number</b>                                                                                                                           |
| 1      | PSE_SP_ARB_EN   | <b>Enable PSE Strict priority arbiter, it works if no request match current TDM slot</b><br><br>1'b1: Enable SP arbiter<br><br>1'b0: Disable SP arbiter |
| 0      | PSE_TDM_ARB_EN  | <b>Enable PSE TDM arbiter</b><br><br>1'b1: Enable TDM arbiter<br><br>1'b0: Disable PSE TDM arbiter, back to RR                                          |

151001EC CDM SRAM RD CDM CR read 8K SRAM 00000000

| Bit   | 31              | 30 | 29 | 28 | 27                | 26 | 25 | 24 | 23                        | 22                              | 21                            | 20                            | 19                        | 18                              | 17                            | 16                            |
|-------|-----------------|----|----|----|-------------------|----|----|----|---------------------------|---------------------------------|-------------------------------|-------------------------------|---------------------------|---------------------------------|-------------------------------|-------------------------------|
| Name  |                 |    |    |    |                   |    |    |    |                           |                                 |                               | CDM_DBG_CNT_DIS               | CDM_DBG_IDX               |                                 |                               |                               |
| Type  |                 |    |    |    |                   |    |    |    |                           |                                 |                               | RW                            | RW                        |                                 |                               |                               |
| Reset |                 |    |    |    |                   |    |    |    |                           |                                 |                               | 0                             | 0                         | 0                               | 0                             | 0                             |
| Bit   | 15              | 14 | 13 | 12 | 11                | 10 | 9  | 8  | 7                         | 6                               | 5                             | 4                             | 3                         | 2                               | 1                             | 0                             |
| Name  | CDM_DBG_CNT_SEL |    |    |    | CDM_SRAM_OPT_PORT |    |    |    | CDM_F<br>S_SRA<br>M_RD_EN | CDM_F<br>S_SRA<br>M_DAT<br>A_RD | CDM_F<br>S_SRA<br>M_SOF<br>RD | CDM_F<br>S_SRA<br>M_EOF<br>RD | CDM_T<br>S_SRA<br>M_RD_EN | CDM_T<br>S_SRA<br>M_DAT<br>A_RD | CDM_T<br>S_SRA<br>M_SOF<br>RD | CDM_T<br>S_SRA<br>M_EOF<br>RD |
| Type  | RW              |    |    |    | RW                |    |    |    | RW                        | RW                              | RW                            | RW                            | RW                        | RW                              | RW                            | RW                            |
| Reset | 0               | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0                         | 0                               | 0                             | 0                             | 0                         | 0                               | 0                             | 0                             |

| Bit(s) | Name              | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|--------|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20     | CDM_DBG_CNT_DIS   | <b>Disable CDM debug counter, CDM debug counter is 0 when counter disable</b><br><br>1'b0: Enable CDM debug counter<br><br>1'b1: Disable CDM debug counter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 19:16  | CDM_DBG_IDX       | <b>Index for CDM debug select</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 15:12  | CDM_DBG_CNT_SEL   | <b>CDM debug counter selection</b><br><br>4'd0: Packet count by CDM parsing<br><br>4'd1: Bytes count by CDM parsing<br><br>4'd2: Packet count by CDM data AFIFO write<br><br>4'd3: Info count by SOF AFIFO (CDM3)/info count epse AFIFO (CDM2)<br><br>4'd4: Info count by EOF AFIFO (CDM3)/data AFIFO overflow count (CDM2)<br><br>4'd5: Data AFIFO overflow count (CDM3)/data AFIFO underflow count (CDM2)<br><br>4'd6: Data AFIFO underflow count (CDM3)/epse AFIFO overflow count (CDM2)<br><br>4'd7: SOF AFIFO overflow count (CDM3)/epse AFIFO underflow count (CDM2)<br><br>4'd8: SOF AFIFO underflow count (CDM3)<br><br>4'd9: EOF AFIFO overflow count (CDM3)<br><br>4'd10: EOF AFIFO underflow count (CDM3)<br><br>4'd11: DFIFO invalid write count (CDM3)<br><br>4'd12: DFIFO invalid read count (CDM3) |
| 11:8   | CDM_SRAM_OPT_PORT | <b>Port number of the CDM which use CR to read out SRAM data</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 7      | CDM_FS_SRAM_RD_EN | <b>Enable CDM FS part to read out SRAM by CR control</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

| Bit(s) | Name                | Description                                                                      |
|--------|---------------------|----------------------------------------------------------------------------------|
|        |                     | 1'b1: Enable CDM FS part CR read SRAM                                            |
|        |                     | 1'b0: Disable CDM FS part CR read SRAM                                           |
| 6      | CDM_FS_SRAM_DATA_RD | <b>Switch the bit 0/1 repeatedly to read out the CDM FS part data SRAM by CR</b> |
|        |                     | 1'b1: Excite CDM FS part read data SRAM                                          |
|        |                     | 1'b0: Ready to excite CDM FS part read data SRAM                                 |
| 5      | CDM_FS_SRAM_SOF_RD  | <b>Switch the bit 0/1 repeatedly to read out the CDM FS part SOF AFIFO by CR</b> |
|        |                     | 1'b1: Excite CDM FS part read SOF data AFIFO                                     |
|        |                     | 1'b0: Ready to excite CDM FS part read SOF data AFIFO                            |
| 4      | CDM_FS_SRAM_EOF_RD  | <b>Switch the bit 0/1 repeatedly to read out the CDM FS part EOF AFIFO by CR</b> |
|        |                     | 1'b1: Excite CDM FS part read EOF data AFIFO                                     |
|        |                     | 1'b0: Ready to excite CDM FS part read EOF data AFIFO                            |
| 3      | CDM_TS_SRAM_RD_EN   | <b>Enable CDM TS part to read out SRAM by CR control</b>                         |
|        |                     | 1'b1: Enable CDM TS part CR read SRAM                                            |
|        |                     | 1'b0: Disable CDM TS part CR read SRAM                                           |
| 2      | CDM_TS_SRAM_DATA_RD | <b>Switch the bit 0/1 repeatedly to read out the CDM TS part data SRAM by CR</b> |
|        |                     | 1'b1: Excite CDM TS part read data SRAM                                          |
|        |                     | 1'b0: Ready to excite CDM TS part read data SRAM                                 |
| 1      | CDM_TS_SRAM_SOF_RD  | <b>Switch the bit 0/1 repeatedly to read out the CDM TS part SOF AFIFO by CR</b> |
|        |                     | 1'b1: Excite CDM TS part read SOF data AFIFO                                     |
|        |                     | 1'b0: Ready to excite CDM TS part read SOF data AFIFO                            |
| 0      | CDM_TS_SRAM_EOF_RD  | <b>Switch the bit 0/1 repeatedly to read out the CDM TS part EOF AFIFO by CR</b> |
|        |                     | 1'b1: Excite CDM TS part read EOF data AFIFO                                     |
|        |                     | 1'b0: Ready to excite CDM TS part read EOF data AFIFO                            |

**15100200      FE\_CDM1\_DBG1      FE CDM1 debug part1      00000000**

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM1_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM1_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                |
|--------|------------------|----------------------------|
| 31:0   | CDM1_FS_RINF_LSB | CDM1 FS packet info [31:0] |

**15100204      FE\_CDM1\_DBG2      FE CDM1 debug part2      00000000**

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM1_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM1_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                 |
|--------|------------------|-----------------------------|
| 31:0   | CDM1_FS_RINF_MSB | CDM1 FS packet info [63:32] |

**15100208      FE\_CDM2\_DBG1      FE CDM2 debug part1      00000000**

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM2_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM2_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                |
|--------|------------------|----------------------------|
| 31:0   | CDM2_FS_RINF_LSB | CDM2 FS packet info [31:0] |

1510020C      FE\_CDM2\_DBG2      FE CDM2 debug part2      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM2_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM2_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                 |
|--------|------------------|-----------------------------|
| 31:0   | CDM2_FS_RINF_MSB | CDM2 FS packet info [63:32] |

15100210      FE\_GDM1\_DBG1      FE GDM1 debug part1      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | GDM1_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | GDM1_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                |
|--------|------------------|----------------------------|
| 31:0   | GDM1_FS_RINF_LSB | GDM1 FS packet info [31:0] |

15100214      FE\_GDM1\_DBG2      FE GDM1 debug part2      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | GDM1_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | GDM1_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                 |
|--------|------------------|-----------------------------|
| 31:0   | GDM1_FS_RINF_MSB | GDM1 FS packet info [63:32] |

15100218      FE\_GDM2\_DBG1      FE GDM2 debug part1      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | GDM2_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | GDM2_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                |
|--------|------------------|----------------------------|
| 31:0   | GDM2_FS_RINF_LSB | GDM2 FS packet info [31:0] |

1510021C      FE\_GDM2\_DBG2      FE GDM2 debug part2      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | GDM2_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | GDM2_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                 |
|--------|------------------|-----------------------------|
| 31:0   | GDM2_FS_RINF_MSB | GDM2 FS packet info [63:32] |

**15100220      FE\_CDM1\_FSM      FE\_CDM1\_FSM status      00000000**

| Bit   | 31 | 30 | 29 | 28 | 27            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
|-------|----|----|----|----|---------------|----|----|----|----|----|----|----|--------|----|----|----|
| Name  |    |    |    |    | FS_PARSER_FSM |    |    |    |    |    |    |    | FS_FSM |    |    |    |
| Type  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| Reset |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11            | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| Name  |    |    |    |    | TS_PARSER_FSM |    |    |    |    |    |    |    | TS_FSM |    |    |    |
| Type  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| Reset |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |

| Bit(s) | Name          | Description                 |
|--------|---------------|-----------------------------|
| 27:24  | FS_PARSER_FSM | FSM status in cdm_fs_parser |
| 19:16  | FS_FSM        | FSM status in cdm_fs_fsm    |
| 12:8   | TS_PARSER_FSM | FSM status in cdm_ts_parser |
| 3:0    | TS_FSM        | FSM status in cdm_ts_fsm    |

**15100224      FE\_CDM2\_FSM      FE\_CDM2\_FSM status      00000000**

| Bit   | 31 | 30 | 29 | 28 | 27            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
|-------|----|----|----|----|---------------|----|----|----|----|----|----|----|--------|----|----|----|
| Name  |    |    |    |    | FS_PARSER_FSM |    |    |    |    |    |    |    | FS_FSM |    |    |    |
| Type  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| Reset |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11            | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| Name  |    |    |    |    | TS_PARSER_FSM |    |    |    |    |    |    |    | TS_FSM |    |    |    |
| Type  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| Reset |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |

| Bit(s) | Name          | Description                 |
|--------|---------------|-----------------------------|
| 27:24  | FS_PARSER_FSM | FSM status in cdm_fs_parser |
| 19:16  | FS_FSM        | FSM status in cdm_fs_fsm    |
| 12:8   | TS_PARSER_FSM | FSM status in cdm_ts_parser |
| 3:0    | TS_FSM        | FSM status in cdm_ts_fsm    |

**15100228**      **FE\_GDM1\_FSM**      **FE GDM1 FSM status**      **00000000**

| Bit   | 31 | 30 | 29 | 28          | 27 | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
|-------|----|----|----|-------------|----|----|----|----|---------------|----|----|----|--------|----|----|----|
| Name  |    |    |    | FS_FIFO_FSM |    |    |    |    | FS_PARSER_FSM |    |    |    | FS_FSM |    |    |    |
| Type  |    |    |    | RO          |    |    |    |    | RO            |    |    |    | RO     |    |    |    |
| Reset |    |    |    | 0           | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0      | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12          | 11 | 10 | 9  | 8  | 7             | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| Name  |    |    |    |             |    |    |    |    | TS_PARSER_FSM |    |    |    | TS_FSM |    |    |    |
| Type  |    |    |    |             |    |    |    |    | RO            |    |    |    | RO     |    |    |    |
| Reset |    |    |    |             |    |    |    |    | 0             | 0  | 0  | 0  | 0      | 0  | 0  | 0  |

| Bit(s) | Name          | Description                 |
|--------|---------------|-----------------------------|
| 28:24  | FS_FIFO_FSM   | FSM status in gdm_fs_fifo   |
| 23:20  | FS_PARSER_FSM | FSM status in gdm_fs_parser |
| 19:16  | FS_FSM        | FSM status in gdm_fs_fsm    |
| 7:4    | TS_PARSER_FSM | FSM status in gdm_ts_parser |
| 3:0    | TS_FSM        | FSM status in gdm_ts_fsm    |

**1510022C**      **FE\_GDM2\_FSM**      **FE GDM2 FSM status**      **00000000**

| Bit   | 31 | 30 | 29 | 28          | 27 | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
|-------|----|----|----|-------------|----|----|----|----|---------------|----|----|----|--------|----|----|----|
| Name  |    |    |    | FS_FIFO_FSM |    |    |    |    | FS_PARSER_FSM |    |    |    | FS_FSM |    |    |    |
| Type  |    |    |    | RO          |    |    |    |    | RO            |    |    |    | RO     |    |    |    |
| Reset |    |    |    | 0           | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0      | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12          | 11 | 10 | 9  | 8  | 7             | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| Name  |    |    |    |             |    |    |    |    | TS_PARSER_FSM |    |    |    | TS_FSM |    |    |    |
| Type  |    |    |    |             |    |    |    |    | RO            |    |    |    | RO     |    |    |    |
| Reset |    |    |    |             |    |    |    |    | 0             | 0  | 0  | 0  | 0      | 0  | 0  | 0  |

| Bit(s) | Name          | Description                 |
|--------|---------------|-----------------------------|
| 28:24  | FS_FIFO_FSM   | FSM status in gdm_fs_fifo   |
| 23:20  | FS_PARSER_FSM | FSM status in gdm_fs_parser |
| 19:16  | FS_FSM        | FSM status in gdm_fs_fsm    |
| 7:4    | TS_PARSER_FSM | FSM status in gdm_ts_parser |
| 3:0    | TS_FSM        | FSM status in gdm_ts_fsm    |



15100230      FE\_CDM3\_DBG1      FE CDM3 debug part1      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM3_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM3_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                |
|--------|------------------|----------------------------|
| 31:0   | CDM3_FS_RINF_LSB | CDM3 FS packet info [31:0] |

15100234      FE\_CDM3\_DBG2      FE CDM3 debug part2      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM3_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM3_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                 |
|--------|------------------|-----------------------------|
| 31:0   | CDM3_FS_RINF_MSB | CDM3 FS packet info [63:32] |

15100238      **FE\_CDM3\_FSM**      **FE\_CDM3\_FSM status**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
|-------|----|----|----|----|---------------|----|----|----|----|----|----|----|--------|----|----|----|
| Name  |    |    |    |    | FS_PARSER_FSM |    |    |    |    |    |    |    | FS_FSM |    |    |    |
| Type  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| Reset |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11            | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| Name  |    |    |    |    | TS_PARSER_FSM |    |    |    |    |    |    |    | TS_FSM |    |    |    |
| Type  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| Reset |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |

| Bit(s) | Name          | Description                 |
|--------|---------------|-----------------------------|
| 27:24  | FS_PARSER_FSM | FSM status in cdm_fs_parser |
| 19:16  | FS_FSM        | FSM status in cdm_fs_fsm    |
| 12:8   | TS_PARSER_FSM | FSM status in cdm_ts_parser |
| 3:0    | TS_FSM        | FSM status in cdm_ts_fsm    |

15100240      **FE\_PSE\_FREE**      **PSE free page Count**      **07FF07FF**

| Bit   | 31 | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    | FQ_PCNT_MIN |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RC          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15 | 14 | 13 | 12 | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | FQ_PCNT     |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO          |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name        | Description                                                                                                                                                                                                           |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 27:16  | FQ_PCNT_MIN | Free queue minimum page count since the last read<br><br>The minimum free page count will update the value whenever the free page is lower than the current record. The field will be reset to FF after MCU reads it. |
| 11:0   | FQ_PCNT     | Free queue page count                                                                                                                                                                                                 |

**15100244 FE\_DROP\_FQ FE packet drop by free queue 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | PSE_DROP_FQ |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_FQ |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | PSE_DROP_FQ | <p><b>Packet dropped by PSE when the free queue is low.</b></p> <p>When GDM is receiving a packet and the free buffer is almost exhausted, PSE will drop any received packet no matter if FC is on or off. The filed is reset to 0 after MCU reads it.</p> |

**15100248 FE\_DROP\_FC FE packet drop by flow control 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | PSE_DROP_FC |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_FC |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                            |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | PSE_DROP_FC | <p><b>Packet dropped by PSE when the flow control is off</b></p> <p>When GDM receive the packets over the FC threshold and the flow control is off, PSE will drop the received packet to prevent the free buffer from being exhausted. The filed is reset to 0 after MCU reads it.</p> |

1510024C **FE\_DROP\_PPE1** FE packet drop by PPE1 00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | PSE_DROP_PPE1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_PPE1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                                                        |
|--------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | PSE_DROP_PPE1 | <b>Packet dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to PDMA RX Ring is almost full when PSE_MIR_PORT.PO_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

15100250 **FE\_DROP\_PD\_6** FE packet drop by Port 6 disabled 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_P6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                |
|--------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0   | PSE_DROP_P6 | <b>MIB counter for packet dropped by destination port P6 is disabled</b><br><br>Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[6] = 1<br><br>The filed is reset to 0 after MCU reads it. |

15100254 **FE\_DROP\_PD\_5** FE packet drop by Port 5 disabled 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_P5 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                       |
|--------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0   | PSE_DROP_P5 | <p><b>MIB counter for packet dropped by destination port P5 is disabled</b></p> <p>Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[5] = 1</p> <p>The filed is reset to 0 after MCU reads it.</p> |

15100258 **FE\_DROP\_PD\_4** FE packet drop by Port 4 disabled 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_P4 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                 |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0   | PSE_DROP_P4 | <p><b>MIB counter for packet dropped by destination port P4 is disabled</b></p> <p>Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[4] = 1 or PPE_GLO_CFG.PPE_EN = 0</p> <p>The filed is reset to 0 after MCU reads it.</p> |

**1510025C FE\_DROP\_PD\_3 FE packet drop by Port 3 disabled 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_P3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                |
|--------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0   | PSE_DROP_P3 | <b>MIB counter for packet dropped by destination port P3 is disabled</b><br><br>Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[3] = 1<br><br>The filed is reset to 0 after MCU reads it. |

**15100260 FE\_DROP\_PD\_2 FE packet drop by Port 2 disabled 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_P2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0   | PSE_DROP_P2 | <b>MIB counter for packet dropped by destination port P2 is disabled</b><br><br>Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[2] = 1 or<br>MAC_P2_SR.LINK_STATUS = 0<br><br>The filed is reset to 0 after MCU reads it. |

15100264      **FE\_DROP\_PD\_1**      **FE packet drop by Port 1 disabled**      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_P1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0   | PSE_DROP_P1 | <b>MIB counter for packet dropped by destination port P1 is disabled</b><br><br>Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[1] = 1 or<br>MAC_P1_SR.LINK_STATUS = 0<br><br>The filed is reset to 0 after MCU reads it. |

15100268      **FE\_DROP\_PD\_0**      **FE packet drop by Port 0 disabled**      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_P0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                |
|--------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0   | PSE_DROP_P0 | <b>MIB counter for packet dropped by destination port P0 is disabled</b><br><br>Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[0] = 1<br><br>The filed is reset to 0 after MCU reads it. |

15100270 **FE\_DROP\_PD\_14** **FE packet drop by Port 14 disabled** 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_P14 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                         |
|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0   | PSE_DROP_P14 | <p><b>MIB counter for packet dropped by destination port P14 is disabled</b></p> <p>Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[6] = 1</p> <p>The filed is reset to 0 after MCU reads it.</p> |

15100274 **FE\_DROP\_PD\_13** **FE packet drop by Port 13 disabled** 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_P13 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                         |
|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0   | PSE_DROP_P13 | <p><b>MIB counter for packet dropped by destination port P13 is disabled</b></p> <p>Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[5] = 1</p> <p>The filed is reset to 0 after MCU reads it.</p> |



15100278 **FE\_DROP\_PD\_12** FE packet drop by Port 12 disabled 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_P12 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                         |
|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0   | PSE_DROP_P12 | <p><b>MIB counter for packet dropped by destination port P12 is disabled</b></p> <p>Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[4] = 1</p> <p>The filed is reset to 0 after MCU reads it.</p> |

1510027C **FE\_DROP\_PD\_11** FE packet drop by Port 11 disabled 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_P11 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                         |
|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0   | PSE_DROP_P11 | <p><b>MIB counter for packet dropped by destination port P11 is disabled</b></p> <p>Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[3] = 1</p> <p>The filed is reset to 0 after MCU reads it.</p> |

15100280      **FE\_DROP\_PD\_10**      **FE packet drop by Port 10 disabled**      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_P10 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                          |
|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0   | PSE_DROP_P10 | <b>MIB counter for packet dropped by destination port P10 is disabled</b><br>Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[2] = 1<br>The filed is reset to 0 after MCU reads it. |

15100284      **FE\_DROP\_PD\_9**      **FE packet drop by Port 9 disabled**      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_P9 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                         |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0   | PSE_DROP_P9 | <b>MIB counter for packet dropped by destination port P9 is disabled</b><br>Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[1] = 1<br>The filed is reset to 0 after MCU reads it. |

15100288      **FE\_DROP\_PD\_8**      **FE packet drop by Port 8 disabled**      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_P8 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                        |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0   | PSE_DROP_P8 | <p><b>MIB counter for packet dropped by destination port P8 is disabled</b></p> <p>Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[0] = 1</p> <p>The filed is reset to 0 after MCU reads it.</p> |

1510028C      **FE\_DROP\_PD\_7**      **FE packet drop by Port 7 disabled**      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_P7 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                       |
|--------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0   | PSE_DROP_P7 | <p><b>MIB counter for packet dropped by destination port P7 is disabled</b></p> <p>Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[7] = 1</p> <p>The filed is reset to 0 after MCU reads it.</p> |

15100290      FE\_CDM4\_DBG1      FE CDM4 debug part1      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM4_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM4_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                |
|--------|------------------|----------------------------|
| 31:0   | CDM4_FS_RINF_LSB | CDM4 FS packet info [31:0] |

15100294      FE\_CDM4\_DBG2      FE CDM4 debug part2      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM4_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM4_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                 |
|--------|------------------|-----------------------------|
| 31:0   | CDM4_FS_RINF_MSB | CDM4 FS packet info [63:32] |

**15100298**      **FE\_CDM4\_FSM**      **FE\_CDM4\_FSM status**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
|-------|----|----|----|----|---------------|----|----|----|----|----|----|----|--------|----|----|----|
| Name  |    |    |    |    | FS_PARSER_FSM |    |    |    |    |    |    |    | FS_FSM |    |    |    |
| Type  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| Reset |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11            | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| Name  |    |    |    |    | TS_PARSER_FSM |    |    |    |    |    |    |    | TS_FSM |    |    |    |
| Type  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| Reset |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |

| Bit(s) | Name          | Description                 |
|--------|---------------|-----------------------------|
| 27:24  | FS_PARSER_FSM | FSM status in cdm_fs_parser |
| 19:16  | FS_FSM        | FSM status in cdm_fs_fsm    |
| 12:8   | TS_PARSER_FSM | FSM status in cdm_ts_parser |
| 3:0    | TS_FSM        | FSM status in cdm_ts_fsm    |

**1510029C**      **FE\_DROP\_PPE2**      **FE packet drop by PPE2**      **00000000**

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | PSE_DROP_PPE2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_PPE2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                                                        |
|--------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | PSE_DROP_PPE2 | <b>Packet dropped by PPE2</b><br><br>The PPE1 forwarded packet is dropped due to PDMA RX Ring is almost full when PSE_MIR_PORT.P0_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

**151002A0**      **FE\_DROP\_PPE0**      **FE packet drop by PPE0**      **00000000**

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | PSE_DROP_PPE0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_PPE0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                                                        |
|--------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | PSE_DROP_PPE0 | <b>Packet dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to PDMA RX Ring is almost full when PSE_MIR_PORT.PO_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

**151002A4**      **FE\_DROP\_PPE0\_PO\_R01**      **FE packet to Port0 Ring 0&1 drop by PPE0**      **00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | PSE_DROP_PPE0_PO_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_PPE0_PO_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                                                                         |
|--------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE0_PO_R1 | <b>Packet to ADMA Ring 1 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to ADMA RX Ring 1 is almost full when FE_DROP_PPE0.PO_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE0_PO_R0 | <b>Packet to ADMA Ring 0 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to ADMA RX Ring 0 is almost full when FE_DROP_PPE0.PO_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

**151002A8 FE\_DROP\_PPE0\_P0\_R23 FE packet to Port0 Ring 2&3 drop by PPE0 00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | PSE_DROP_PPE0_P0_R3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_PPE0_P0_R2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                                                                         |
|--------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE0_P0_R3 | <b>Packet to ADMA Ring 3 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to ADMA RX Ring 3 is almost full when FE_DROP_PPE0.P0_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE0_P0_R2 | <b>Packet to ADMA Ring 2 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to ADMA RX Ring 2 is almost full when FE_DROP_PPE0.P0_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

**151002AC FE\_DROP\_PPE0\_P5 FE packet to Port5 drop by PPE0 00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | PSE_DROP_PPE0_P5_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_PPE0_P5_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                                                                         |
|--------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE0_P5_R1 | <b>Packet to QDMA Ring 1 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to QDMA RX Ring 1 is almost full when FE_DROP_PPE0.P5_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE0_P5_R0 | <b>Packet to QDMA Ring 0 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to QDMA RX Ring 0 is almost full when FE_DROP_PPE0.P5_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

**151002B0**      **FE\_DROP\_PPE0\_P8**      **FE packet to Port8 drop by PPE0**      **00000000**

| Bit          | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | PSE_DROP_PPE0_P8_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | PSE_DROP_PPE0_P8_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                                                                           |
|--------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE0_P8_R1 | <b>Packet to WDMA0 Ring 1 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to WDMA0 RX Ring 1 is almost full when FE_DROP_PPE0.P8_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE0_P8_R0 | <b>Packet to WDMA0 Ring 0 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to WDMA0 RX Ring 0 is almost full when FE_DROP_PPE0.P8_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

**151002B4**      **FE\_DROP\_PPE0\_P9**      **FE packet to Port9 drop by PPE0**      **00000000**

| Bit          | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | PSE_DROP_PPE0_P9_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | PSE_DROP_PPE0_P9_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                                                                           |
|--------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE0_P9_R1 | <b>Packet to WDMA1 Ring 1 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to WDMA1 RX Ring 1 is almost full when FE_DROP_PPE0.P9_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE0_P9_R0 | <b>Packet to WDMA1 Ring 0 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to WDMA1 RX Ring 0 is almost full when FE_DROP_PPE0.P9_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |



151002B8      **FE\_DROP\_PPE0\_P10**      **FE packet to Port10 drop by PPE0**      00000000

| Bit          | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | PSE_DROP_PPE0_P10_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | PSE_DROP_PPE0_P10_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                                                          |
|--------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE0_P10_R1 | <b>Packet to MDMA Ring 1 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to MDMA RX Ring 1 is almost full when FE_DROP_PPE0.P10_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE0_P10_R0 | <b>Packet to MDMA Ring 0 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to MDMA RX Ring 0 is almost full when FE_DROP_PPE0.P10_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

151002BC      **FE\_DROP\_PPE0\_P11**      **FE packet to Port11 drop by PPE0**      00000000

| Bit          | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | PSE_DROP_PPE0_P11_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | PSE_DROP_PPE0_P11_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                                                            |
|--------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE0_P11_R1 | <b>Packet to EDMA0 Ring 1 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to EDMA0 RX Ring 1 is almost full when FE_DROP_PPE0.P11_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE0_P11_R0 | <b>Packet to EDMA0 Ring 0 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to EDMA0 RX Ring 0 is almost full when FE_DROP_PPE0.P11_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

151002C0      FE\_DROP\_PPE0\_P12      FE packet to Port12 drop by PPE0      00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | PSE_DROP_PPE0_P12_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_PPE0_P12_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                                                            |
|--------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE0_P12_R1 | <b>Packet to EDMA1 Ring 1 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to EDMA1 RX Ring 1 is almost full when FE_DROP_PPE0.P12_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE0_P12_R0 | <b>Packet to EDMA1 Ring 0 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to EDMA1 RX Ring 0 is almost full when FE_DROP_PPE0.P12_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

151002C4      FE\_DROP\_PPE1\_P0\_R01      FE packet to Port0 Ring 0&1 drop by PPE1      00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | PSE_DROP_PPE1_P0_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_PPE1_P0_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                                                                         |
|--------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE1_P0_R1 | <b>Packet to ADMA Ring 1 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to ADMA RX Ring 1 is almost full when FE_DROP_PPE1.P0_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE1_P0_R0 | <b>Packet to ADMA Ring 0 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to ADMA RX Ring 0 is almost full when FE_DROP_PPE1.P0_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

**151002C8      FE\_DROP\_PPE1\_P0\_R23      FE packet to Port0 Ring 2&3 drop by PPE1      00000000**

| Bit          | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | PSE_DROP_PPE1_P0_R3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | PSE_DROP_PPE1_P0_R2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                                                                         |
|--------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE1_P0_R3 | <b>Packet to ADMA Ring 3 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to ADMA RX Ring 3 is almost full when FE_DROP_PPE1.P0_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE1_P0_R2 | <b>Packet to ADMA Ring 2 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to ADMA RX Ring 2 is almost full when FE_DROP_PPE1.P0_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

**151002CC      FE\_DROP\_PPE1\_P5      FE packet to Port5 drop by PPE1      00000000**

| Bit          | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | PSE_DROP_PPE1_P5_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | PSE_DROP_PPE1_P5_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                                                                         |
|--------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE1_P5_R1 | <b>Packet to QDMA Ring 1 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to QDMA RX Ring 1 is almost full when FE_DROP_PPE1.P5_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE1_P5_R0 | <b>Packet to QDMA Ring 0 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to QDMA RX Ring 0 is almost full when FE_DROP_PPE1.P5_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

**151002D0      FE\_DROP\_PPE1\_P8      FE packet to Port8 drop by PPE1      00000000**

| Bit          | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | PSE_DROP_PPE1_P8_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | PSE_DROP_PPE1_P8_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                                                                           |
|--------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE1_P8_R1 | <b>Packet to WDMA0 Ring 1 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to WDMA0 RX Ring 1 is almost full when FE_DROP_PPE1.P8_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE1_P8_R0 | <b>Packet to WDMA0 Ring 0 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to WDMA0 RX Ring 0 is almost full when FE_DROP_PPE1.P8_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

**151002D4      FE\_DROP\_PPE1\_P9      FE packet to Port9 drop by PPE1      00000000**

| Bit          | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | PSE_DROP_PPE1_P9_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | PSE_DROP_PPE1_P9_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                                                                                                                                                                           |
|--------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE1_P9_R1 | <b>Packet to WDMA1 Ring 1 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to WDMA1 RX Ring 1 is almost full when FE_DROP_PPE1.P9_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE1_P9_R0 | <b>Packet to WDMA1 Ring 0 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to WDMA1 RX Ring 0 is almost full when FE_DROP_PPE1.P9_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

**151002D8      FE\_DROP\_PPE1\_P10      FE packet to Port10 drop by PPE1      00000000**

| Bit          | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | PSE_DROP_PPE1_P10_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | PSE_DROP_PPE1_P10_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                                                          |
|--------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE1_P10_R1 | <b>Packet to MDMA Ring 1 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to MDMA RX Ring 1 is almost full when FE_DROP_PPE1.P10_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE1_P10_R0 | <b>Packet to MDMA Ring 0 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to MDMA RX Ring 0 is almost full when FE_DROP_PPE1.P10_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

**151002DC      FE\_DROP\_PPE1\_P11      FE packet to Port11 drop by PPE1      00000000**

| Bit          | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | PSE_DROP_PPE1_P11_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | PSE_DROP_PPE1_P11_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                                                            |
|--------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE1_P11_R1 | <b>Packet to EDMA0 Ring 1 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to EDMA0 RX Ring 1 is almost full when FE_DROP_PPE1.P11_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE1_P11_R0 | <b>Packet to EDMA0 Ring 0 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to EDMA0 RX Ring 0 is almost full when FE_DROP_PPE1.P11_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

151002E0      **FE\_DROP\_PPE1\_P12**      **FE packet to Port12 drop by PPE1**      00000000

| Bit          | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | PSE_DROP_PPE1_P12_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | PSE_DROP_PPE1_P12_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                                                            |
|--------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE1_P12_R1 | <b>Packet to EDMA1 Ring 1 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to EDMA1 RX Ring 1 is almost full when FE_DROP_PPE1.P12_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE1_P12_R0 | <b>Packet to EDMA1 Ring 0 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to EDMA1 RX Ring 0 is almost full when FE_DROP_PPE1.P12_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

151002E4      **FE\_DROP\_PPE0\_P13**      **FE packet to Port13 drop by PPE0**      00000000

| Bit          | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | PSE_DROP_PPE0_P13_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | PSE_DROP_PPE0_P13_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                                                            |
|--------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE0_P13_R1 | <b>Packet to WDMA2 Ring 1 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to WDMA2 RX Ring 1 is almost full when FE_DROP_PPE0.P13_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE0_P13_R0 | <b>Packet to WDMA2 Ring 0 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to WDMA2 RX Ring 0 is almost full when FE_DROP_PPE0.P13_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

151002E8      **FE\_DROP\_PPE0\_P14**      **FE packet to Port14 drop by PPE0**      00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | PSE_DROP_PPE0_P14_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_PPE0_P14_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                                                            |
|--------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE0_P14_R1 | <b>Packet to EDMA2 Ring 1 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to EDMA2 RX Ring 1 is almost full when FE_DROP_PPE0.P14_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE0_P14_R0 | <b>Packet to EDMA2 Ring 0 dropped by PPE0</b><br><br>The PPE0 forwarded packet is dropped due to EDMA2 RX Ring 0 is almost full when FE_DROP_PPE0.P14_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

151002EC      **FE\_DROP\_PPE1\_P13**      **FE packet to Port13 drop by PPE1**      00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | PSE_DROP_PPE1_P13_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_PPE1_P13_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                                                            |
|--------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE1_P13_R1 | <b>Packet to WDMA2 Ring 1 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to WDMA2 RX Ring 1 is almost full when FE_DROP_PPE1.P13_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE1_P13_R0 | <b>Packet to WDMA2 Ring 0 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to WDMA2 RX Ring 0 is almost full when FE_DROP_PPE1.P13_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

151002F0      FE\_DROP\_PPE1\_P14      FE packet to Port14 drop by PPE1      00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | PSE_DROP_PPE1_P14_R1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | PSE_DROP_PPE1_P14_R0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                                                                                                            |
|--------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | PSE_DROP_PPE1_P14_R1 | <b>Packet to EDMA2 Ring 1 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to EDMA2 RX Ring 1 is almost full when FE_DROP_PPE1.P14_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |
| 15:0   | PSE_DROP_PPE1_P14_R0 | <b>Packet to EDMA2 Ring 0 dropped by PPE1</b><br><br>The PPE1 forwarded packet is dropped due to EDMA2 RX Ring 0 is almost full when FE_DROP_PPE1.P14_DROP_PPE is enabled. The filed is reset to 0 after MCU reads it. |

15100310      FE\_CDM5\_DBG1      FE CDM5 debug part1      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM5_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM5_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                       |
|--------|------------------|-----------------------------------|
| 31:0   | CDM5_FS_RINF_LSB | <b>CDM5 FS packet info [31:0]</b> |



15100314      **FE\_CDM5\_DBG2**      **FE CDM5 debug part2**      **00000000**

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM5_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM5_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                 |
|--------|------------------|-----------------------------|
| 31:0   | CDM5_FS_RINF_MSB | CDM5 FS packet info [63:32] |

15100318      **FE\_CDM5\_FSM**      **FE CDM5 FSM status**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
|-------|----|----|----|----|---------------|----|----|----|----|----|----|----|--------|----|----|----|
| Name  |    |    |    |    | FS_PARSER_FSM |    |    |    |    |    |    |    | FS_FSM |    |    |    |
| Type  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| Reset |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11            | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| Name  |    |    |    |    | TS_PARSER_FSM |    |    |    |    |    |    |    | TS_FSM |    |    |    |
| Type  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| Reset |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |

| Bit(s) | Name          | Description                 |
|--------|---------------|-----------------------------|
| 27:24  | FS_PARSER_FSM | FSM status in cdm_fs_parser |
| 19:16  | FS_FSM        | FSM status in cdm_fs_fsm    |
| 12:8   | TS_PARSER_FSM | FSM status in cdm_ts_parser |
| 3:0    | TS_FSM        | FSM status in cdm_ts_fsm    |

15100320      FE\_CDM6\_DBG1      FE CDM6 debug part1      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM6_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM6_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                |
|--------|------------------|----------------------------|
| 31:0   | CDM6_FS_RINF_LSB | CDM6 FS packet info [31:0] |

15100324      FE\_CDM6\_DBG2      FE CDM6 debug part2      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM6_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM6_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                 |
|--------|------------------|-----------------------------|
| 31:0   | CDM6_FS_RINF_MSB | CDM6 FS packet info [63:32] |

**15100328**      **FE\_CDM6\_FSM**      **FE CDM6 FSM status**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
|-------|----|----|----|----|---------------|----|----|----|----|----|----|----|--------|----|----|----|
| Name  |    |    |    |    | FS_PARSER_FSM |    |    |    |    |    |    |    | FS_FSM |    |    |    |
| Type  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| Reset |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11            | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| Name  |    |    |    |    | TS_PARSER_FSM |    |    |    |    |    |    |    | TS_FSM |    |    |    |
| Type  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| Reset |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |

| Bit(s) | Name          | Description                 |
|--------|---------------|-----------------------------|
| 27:24  | FS_PARSER_FSM | FSM status in cdm_fs_parser |
| 19:16  | FS_FSM        | FSM status in cdm_fs_fsm    |
| 12:8   | TS_PARSER_FSM | FSM status in cdm_ts_parser |
| 3:0    | TS_FSM        | FSM status in cdm_ts_fsm    |

**15100330**      **FE\_CDM7\_DBG1**      **FE CDM7 debug part1**      **00000000**

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM7_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM7_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                |
|--------|------------------|----------------------------|
| 31:0   | CDM7_FS_RINF_LSB | CDM7 FS packet info [31:0] |

15100334      **FE\_CDM7\_DBG2**      **FE CDM7 debug part2**      **00000000**

| Bit          | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | CDM7_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | CDM7_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                 |
|--------|------------------|-----------------------------|
| 31:0   | CDM7_FS_RINF_MSB | CDM7 FS packet info [63:32] |

15100338      **FE\_CDM7\_FSM**      **FE CDM7 FSM status**      **00000000**

| Bit          | 31 | 30 | 29 | 28 | 27            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
|--------------|----|----|----|----|---------------|----|----|----|----|----|----|----|--------|----|----|----|
| <b>Name</b>  |    |    |    |    | FS_PARSER_FSM |    |    |    |    |    |    |    | FS_FSM |    |    |    |
| <b>Type</b>  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| <b>Reset</b> |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |
| Bit          | 15 | 14 | 13 | 12 | 11            | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| <b>Name</b>  |    |    |    |    | TS_PARSER_FSM |    |    |    |    |    |    |    | TS_FSM |    |    |    |
| <b>Type</b>  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| <b>Reset</b> |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |

| Bit(s) | Name          | Description                 |
|--------|---------------|-----------------------------|
| 27:24  | FS_PARSER_FSM | FSM status in cdm_fs_parser |
| 19:16  | FS_FSM        | FSM status in cdm_fs_fsm    |
| 12:8   | TS_PARSER_FSM | FSM status in cdm_ts_parser |
| 3:0    | TS_FSM        | FSM status in cdm_ts_fsm    |

1510033C      FE\_CDM8\_DBG1      FE CDM8 debug part1      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM8_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM8_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                |
|--------|------------------|----------------------------|
| 31:0   | CDM8_FS_RINF_LSB | CDM8 FS packet info [31:0] |

15100340      FE\_CDM8\_DBG2      FE CDM8 debug part2      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM8_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM8_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                 |
|--------|------------------|-----------------------------|
| 31:0   | CDM8_FS_RINF_MSB | CDM8 FS packet info [63:32] |

**15100344**      **FE\_CDM8\_FSM**      **FE CDM8 FSM status**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
|-------|----|----|----|----|---------------|----|----|----|----|----|----|----|--------|----|----|----|
| Name  |    |    |    |    | FS_PARSER_FSM |    |    |    |    |    |    |    | FS_FSM |    |    |    |
| Type  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| Reset |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11            | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| Name  |    |    |    |    | TS_PARSER_FSM |    |    |    |    |    |    |    | TS_FSM |    |    |    |
| Type  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| Reset |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |

| Bit(s) | Name          | Description                 |
|--------|---------------|-----------------------------|
| 27:24  | FS_PARSER_FSM | FSM status in cdm_fs_parser |
| 19:16  | FS_FSM        | FSM status in cdm_fs_fsm    |
| 12:8   | TS_PARSER_FSM | FSM status in cdm_ts_parser |
| 3:0    | TS_FSM        | FSM status in cdm_ts_fsm    |

**15100348**      **FE\_CDM9\_DBG1**      **FE CDM9 debug part1**      **00000000**

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM9_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM9_FS_RINF_LSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                |
|--------|------------------|----------------------------|
| 31:0   | CDM9_FS_RINF_LSB | CDM9 FS packet info [31:0] |

1510034C      **FE\_CDM9\_DBG2**      **FE CDM9 debug part2**      **00000000**

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | CDM9_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM9_FS_RINF_MSB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                 |
|--------|------------------|-----------------------------|
| 31:0   | CDM9_FS_RINF_MSB | CDM9 FS packet info [63:32] |

15100350      **FE\_CDM9\_FSM**      **FE CDM9 FSM status**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27            | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
|-------|----|----|----|----|---------------|----|----|----|----|----|----|----|--------|----|----|----|
| Name  |    |    |    |    | FS_PARSER_FSM |    |    |    |    |    |    |    | FS_FSM |    |    |    |
| Type  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| Reset |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11            | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| Name  |    |    |    |    | TS_PARSER_FSM |    |    |    |    |    |    |    | TS_FSM |    |    |    |
| Type  |    |    |    |    | RO            |    |    |    |    |    |    |    | RO     |    |    |    |
| Reset |    |    |    |    | 0             | 0  | 0  | 0  |    |    |    |    | 0      | 0  | 0  | 0  |

| Bit(s) | Name          | Description                 |
|--------|---------------|-----------------------------|
| 27:24  | FS_PARSER_FSM | FSM status in cdm_fs_parser |
| 19:16  | FS_FSM        | FSM status in cdm_fs_fsm    |
| 12:8   | TS_PARSER_FSM | FSM status in cdm_ts_parser |
| 3:0    | TS_FSM        | FSM status in cdm_ts_fsm    |

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| Bit   | 31                      | 30                       | 29                           | 28                          | 27                        | 26                       | 25               | 24 | 23 | 22 | 21                       | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------------|--------------------------|------------------------------|-----------------------------|---------------------------|--------------------------|------------------|----|----|----|--------------------------|----|----|----|----|----|
| Name  | CDM3_FS_DATA_AFIFO_FULL | CDM3_FS_DATA_AFIFO_EMPTY | CDM3_FS_DATA_AFIFO_UNDERFLOW | CDM3_FS_DATA_AFIFO_OVERFLOW | CDM3_FS_DATA_AFIFO_W_CNT  |                          |                  |    |    |    | CDM3_FS_DATA_AFIFO_R_CNT |    |    |    |    |    |
| Type  | RO                      | RO                       | RO                           | RO                          | RO                        |                          |                  |    |    |    | RO                       |    |    |    |    |    |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                         | 0                        | 0                | 0  | 0  | 0  | 0                        | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                      | 14                       | 13                           | 12                          | 11                        | 10                       | 9                | 8  | 7  | 6  | 5                        | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM3_SRAM_WR_ENABLE     | CDM3_SRAM_RD_ENABLE      | CDM3_FS_DFIFO_INVLD_WR       | CDM3_FS_DFIFO_INVLD_RD      | CDM3_FS_PARSER_FIFO_EMPTY | CDM3_FS_PARSER_FIFO_FULL | CDM3_RX_FIFO_CNT |    |    |    |                          |    |    |    |    |    |
| Type  | RO                      | RO                       | RO                           | RO                          | RO                        | RO                       | RO               |    |    |    |                          |    |    |    |    |    |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                         | 0                        | 0                | 0  | 0  | 0  | 0                        | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                         | Description                             |
|--------|------------------------------|-----------------------------------------|
| 31     | CDM3_FS_DATA_AFIFO_FULL      | CDM FS data AFIFO full                  |
| 30     | CDM3_FS_DATA_AFIFO_EMPTY     | CDM FS data AFIFO empty                 |
| 29     | CDM3_FS_DATA_AFIFO_UNDERFLOW | CDM FS data AFIFO read when AFIFO empty |
| 28     | CDM3_FS_DATA_AFIFO_OVERFLOW  | CDM FS data AFIFO write when AFIFO full |
| 27:22  | CDM3_FS_DATA_AFIFO_W_CNT     | CDM FS data AFIFO write count           |
| 21:16  | CDM3_FS_DATA_AFIFO_R_CNT     | CDM FS data AFIFO read count            |
| 15     | CDM3_SRAM_WR_ENABLE          | CDM FS 8K SRAM write enable             |
| 14     | CDM3_SRAM_RD_ENABLE          | CDM FS 8K SRAM read enable              |
| 13     | CDM3_FS_DFIFO_INVLD_WR       | CDM FS 8K SRAM invalid write            |
| 12     | CDM3_FS_DFIFO_INVLD_RD       | CDM FS 8K SRAM invalid read             |
| 11     | CDM3_FS_PARSER_FIFO_EMPTY    | CDM FS parser FIFO empty                |
| 10     | CDM3_FS_PARSER_FIFO_FULL     | CDM FS parser FIFO full                 |
| 9:0    | CDM3_RX_FIFO_CNT             | CDM FS 8K SRAM count                    |



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| Bit   | 31                         | 30                          | 29                    | 28                    | 27                    | 26 | 25 | 24                    | 23 | 22                    | 21 | 20 | 19 | 18 | 17                     | 16                      |
|-------|----------------------------|-----------------------------|-----------------------|-----------------------|-----------------------|----|----|-----------------------|----|-----------------------|----|----|----|----|------------------------|-------------------------|
| Name  | CDM3_FS_EOF_AFIFO_FULL     | CDM3_FS_EOF_AFIFO_EMPTY     | CDM3_FS_EOF_OVERFLOW  | CDM3_FS_EOF_UNDERFLOW | CDM3_FS_EOF_WFIFO_CNT |    |    |                       |    | CDM3_FS_EOF_RFIFO_CNT |    |    |    |    | CDM3_FS_SOF_AFIFO_FULL | CDM3_FS_SOF_AFIFO_EMPTY |
| Type  | RO                         | RO                          | RO                    | RO                    | RO                    |    |    |                       |    | RO                    |    |    |    |    | RO                     | RO                      |
| Reset | 0                          | 0                           | 0                     | 0                     | 0                     | 0  | 0  | 0                     | 0  | 0                     | 0  | 0  | 0  | 0  | 0                      | 0                       |
| Bit   | 15                         | 14                          | 13                    | 12                    | 11                    | 10 | 9  | 8                     | 7  | 6                     | 5  | 4  | 3  | 2  | 1                      | 0                       |
| Name  | CDM3_FS_SOF_AFIFO_OVERFLOW | CDM3_FS_SOF_AFIFO_UNDERFLOW | CDM3_FS_SOF_WFIFO_CNT |                       |                       |    |    | CDM3_FS_SOF_RFIFO_CNT |    |                       |    |    |    |    |                        |                         |
| Type  | RO                         | RO                          | RO                    |                       |                       |    |    | RO                    |    |                       |    |    |    |    |                        |                         |
| Reset | 0                          | 0                           | 0                     | 0                     | 0                     | 0  | 0  | 0                     | 0  | 0                     | 0  | 0  |    |    |                        |                         |

| Bit(s) | Name                        | Description                              |
|--------|-----------------------------|------------------------------------------|
| 31     | CDM3_FS_EOF_AFIFO_FULL      | CDM FS EOF AFIFO FULL                    |
| 30     | CDM3_FS_EOF_AFIFO_EMPTY     | CDM FS EOF AFIFO EMPTY                   |
| 29     | CDM3_FS_EOF_OVERFLOW        | CDM FS EOF AFIFO write when FIFO is full |
| 28     | CDM3_FS_EOF_UNDERFLOW       | CDM FS EOF AFIFO read when FIFO is empty |
| 27:23  | CDM3_FS_EOF_WFIFO_CNT       | CDM FS EOF AFIFO write count             |
| 22:18  | CDM3_FS_EOF_RFIFO_CNT       | CDM FS EOF AFIFO read count              |
| 17     | CDM3_FS_SOF_AFIFO_FULL      | CDM FS SOF AFIFO full                    |
| 16     | CDM3_FS_SOF_AFIFO_EMPTY     | CDM FS SOF AFIFO empty                   |
| 15     | CDM3_FS_SOF_AFIFO_OVERFLOW  | CDM FS SOF AFIFO write when FIFO is full |
| 14     | CDM3_FS_SOF_AFIFO_UNDERFLOW | CDM FS SOF AFIFO read when FIFO is empty |
| 13:9   | CDM3_FS_SOF_WFIFO_CNT       | CDM FS SOF AFIFO write count             |
| 8:4    | CDM3_FS_SOF_RFIFO_CNT       | CDM FS SOF AFIFO read count              |

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| Bit   | 31                      | 30                       | 29                           | 28                          | 27                      | 26 | 25 | 24 | 23                      | 22 | 21                        | 20                       | 19                          | 18                         | 17                         | 16                        |
|-------|-------------------------|--------------------------|------------------------------|-----------------------------|-------------------------|----|----|----|-------------------------|----|---------------------------|--------------------------|-----------------------------|----------------------------|----------------------------|---------------------------|
| Name  | CDM3_TS_DATA_AFIFO_FULL | CDM3_TS_DATA_AFIFO_EMPTY | CDM3_TS_DATA_AFIFO_UNDERFLOW | CDM3_TS_DATA_AFIFO_OVERFLOW | CDM3_TS_DATA_AFIFO_WCNT |    |    |    | CDM3_TS_DATA_AFIFO_RCNT |    |                           |                          | CDM3_TS_DFIFO_INVALID_WRITE | CDM3_TS_DFIFO_WRITE_ENABLE | CDM3_TS_DFIFO_INVALID_READ | CDM3_TS_DFIFO_READ_ENABLE |
| Type  | RO                      | RO                       | RO                           | RO                          | RO                      |    |    |    | RO                      |    |                           |                          | RO                          | RO                         | RO                         | RO                        |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                       | 0  | 0  | 0  | 0                       | 0  | 0                         | 0                        | 0                           | 0                          | 0                          | 0                         |
| Bit   | 15                      | 14                       | 13                           | 12                          | 11                      | 10 | 9  | 8  | 7                       | 6  | 5                         | 4                        | 3                           | 2                          | 1                          | 0                         |
| Name  | CDM3_TS_DFIFO_CNT       |                          |                              |                             |                         |    |    |    |                         |    | CDM3_TS_PARSER_FIFO_EMPTY | CDM3_TS_PARSER_FIFO_FULL |                             |                            |                            |                           |
| Type  | RO                      |                          |                              |                             |                         |    |    |    |                         |    | RO                        | RO                       |                             |                            |                            |                           |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                       | 0  | 0  | 0  | 0                       | 0  | 0                         | 0                        |                             |                            |                            |                           |

| Bit(s) | Name                         | Description                             |
|--------|------------------------------|-----------------------------------------|
| 31     | CDM3_TS_DATA_AFIFO_FULL      | CDM TS DATA AFIFO full                  |
| 30     | CDM3_TS_DATA_AFIFO_EMPTY     | CDM TS DATA AFIFO empty                 |
| 29     | CDM3_TS_DATA_AFIFO_UNDERFLOW | CDM TS data AFIFO read when AFIFO empty |
| 28     | CDM3_TS_DATA_AFIFO_OVERFLOW  | CDM TS data AFIFO write when AFIFO full |
| 27:24  | CDM3_TS_DATA_AFIFO_WCNT      | CDM TS data AFIFO write count           |
| 23:20  | CDM3_TS_DATA_AFIFO_RCNT      | CDM TS data AFIFO read count            |
| 19     | CDM3_TS_DFIFO_INVALID_WRITE  | CDM TS 8K SRAM invalid write            |
| 18     | CDM3_TS_DFIFO_WRITE_ENABLE   | CDM TS 8K SRAM write enable             |
| 17     | CDM3_TS_DFIFO_INVALID_READ   | CDM TS 8K SRAM invalid read             |
| 16     | CDM3_TS_DFIFO_READ_ENABLE    | CDM TS 8K SRAM read enable              |
| 15:6   | CDM3_TS_DFIFO_CNT            | CDM TS 8K SRAM count                    |
| 5      | CDM3_TS_PARSER_FIFO_EMPTY    | CDM TS parser FIFO empty                |
| 4      | CDM3_TS_PARSER_FIFO_FULL     | CDM TS parser FIFO full                 |

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| Bit   | 31                         | 30                          | 29                         | 28                          | 27                     | 26 | 25 | 24                     | 23 | 22                     | 21 | 20 | 19 | 18 | 17                     | 16                      |
|-------|----------------------------|-----------------------------|----------------------------|-----------------------------|------------------------|----|----|------------------------|----|------------------------|----|----|----|----|------------------------|-------------------------|
| Name  | CDM3_TS_EOF_AFIFO_FULL     | CDM3_TS_EOF_AFIFO_EMPTY     | CDM3_TS_EOF_AFIFO_OVERFLOW | CDM3_TS_EOF_AFIFO_UNDERFLOW | CDM3_TS_EOF_AFIFO_WCNT |    |    |                        |    | CDM3_TS_EOF_AFIFO_RCNT |    |    |    |    | CDM3_TS_SOF_AFIFO_FULL | CDM3_TS_SOF_AFIFO_EMPTY |
| Type  | RO                         | RO                          | RO                         | RO                          | RO                     |    |    |                        |    | RO                     |    |    |    |    | RO                     | RO                      |
| Reset | 0                          | 0                           | 0                          | 0                           | 0                      | 0  | 0  | 0                      | 0  | 0                      | 0  | 0  | 0  | 0  | 0                      | 0                       |
| Bit   | 15                         | 14                          | 13                         | 12                          | 11                     | 10 | 9  | 8                      | 7  | 6                      | 5  | 4  | 3  | 2  | 1                      | 0                       |
| Name  | CDM3_TS_SOF_AFIFO_OVERFLOW | CDM3_TS_SOF_AFIFO_UNDERFLOW | CDM3_TS_SOF_AFIFO_WCNT     |                             |                        |    |    | CDM3_TS_SOF_AFIFO_RCNT |    |                        |    |    |    |    |                        |                         |
| Type  | RO                         | RO                          | RO                         |                             |                        |    |    | RO                     |    |                        |    |    |    |    |                        |                         |
| Reset | 0                          | 0                           | 0                          | 0                           | 0                      | 0  | 0  | 0                      | 0  | 0                      | 0  | 0  |    |    |                        |                         |

| Bit(s) | Name                        | Description                              |
|--------|-----------------------------|------------------------------------------|
| 31     | CDM3_TS_EOF_AFIFO_FULL      | CDM TS EOF AFIFO full                    |
| 30     | CDM3_TS_EOF_AFIFO_EMPTY     | CDM TS EOF AFIFO empty                   |
| 29     | CDM3_TS_EOF_AFIFO_OVERFLOW  | CDM TS EOF AFIFO write when FIFO is full |
| 28     | CDM3_TS_EOF_AFIFO_UNDERFLOW | CDM TS EOF AFIFO read when FIFO is empty |
| 27:23  | CDM3_TS_EOF_AFIFO_WCNT      | CDM TS EOF AFIFO write count             |
| 22:18  | CDM3_TS_EOF_AFIFO_RCNT      | CDM TS EOF AFIFO read count              |
| 17     | CDM3_TS_SOF_AFIFO_FULL      | CDM TS SOF AFIFO full                    |
| 16     | CDM3_TS_SOF_AFIFO_EMPTY     | CDM TS SOF AFIFO empty                   |
| 15     | CDM3_TS_SOF_AFIFO_OVERFLOW  | CDM TS SOF AFIFO write when FIFO is full |
| 14     | CDM3_TS_SOF_AFIFO_UNDERFLOW | CDM TS SOF AFIFO read when FIFO is empty |
| 13:9   | CDM3_TS_SOF_AFIFO_WCNT      | CDM TS SOF AFIFO write count             |
| 8:4    | CDM3_TS_SOF_AFIFO_RCNT      | CDM TS SOF AFIFO read count              |

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| Bit   | 31                      | 30                       | 29                           | 28                          | 27                        | 26                       | 25               | 24 | 23 | 22 | 21                       | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------------|--------------------------|------------------------------|-----------------------------|---------------------------|--------------------------|------------------|----|----|----|--------------------------|----|----|----|----|----|
| Name  | CDM4_FS_DATA_AFIFO_FULL | CDM4_FS_DATA_AFIFO_EMPTY | CDM4_FS_DATA_AFIFO_UNDERFLOW | CDM4_FS_DATA_AFIFO_OVERFLOW | CDM4_FS_DATA_AFIFO_W_CNT  |                          |                  |    |    |    | CDM4_FS_DATA_AFIFO_R_CNT |    |    |    |    |    |
| Type  | RO                      | RO                       | RO                           | RO                          | RO                        |                          |                  |    |    |    | RO                       |    |    |    |    |    |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                         | 0                        | 0                | 0  | 0  | 0  | 0                        | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                      | 14                       | 13                           | 12                          | 11                        | 10                       | 9                | 8  | 7  | 6  | 5                        | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM4_SRAM_WR_ENABLE     | CDM4_SRAM_RD_ENABLE      | CDM4_FS_DFIFO_INVLD_WR       | CDM4_FS_DFIFO_INVLD_RD      | CDM4_FS_PARSER_FIFO_EMPTY | CDM4_FS_PARSER_FIFO_FULL | CDM4_RX_FIFO_CNT |    |    |    |                          |    |    |    |    |    |
| Type  | RO                      | RO                       | RO                           | RO                          | RO                        | RO                       | RO               |    |    |    |                          |    |    |    |    |    |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                         | 0                        | 0                | 0  | 0  | 0  | 0                        | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                         | Description                             |
|--------|------------------------------|-----------------------------------------|
| 31     | CDM4_FS_DATA_AFIFO_FULL      | CDM FS data AFIFO full                  |
| 30     | CDM4_FS_DATA_AFIFO_EMPTY     | CDM FS data AFIFO empty                 |
| 29     | CDM4_FS_DATA_AFIFO_UNDERFLOW | CDM FS data AFIFO read when AFIFO empty |
| 28     | CDM4_FS_DATA_AFIFO_OVERFLOW  | CDM FS data AFIFO write when AFIFO full |
| 27:22  | CDM4_FS_DATA_AFIFO_W_CNT     | CDM FS data AFIFO write count           |
| 21:16  | CDM4_FS_DATA_AFIFO_R_CNT     | CDM FS data AFIFO read count            |
| 15     | CDM4_SRAM_WR_ENABLE          | CDM FS 8K SRAM write enable             |
| 14     | CDM4_SRAM_RD_ENABLE          | CDM FS 8K SRAM read enable              |
| 13     | CDM4_FS_DFIFO_INVLD_WR       | CDM FS 8K SRAM invalid write            |
| 12     | CDM4_FS_DFIFO_INVLD_RD       | CDM FS 8K SRAM invalid read             |
| 11     | CDM4_FS_PARSER_FIFO_EMPTY    | CDM FS parser FIFO empty                |
| 10     | CDM4_FS_PARSER_FIFO_FULL     | CDM FS parser FIFO full                 |
| 9:0    | CDM4_RX_FIFO_CNT             | CDM FS 8K SRAM count                    |

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| Bit   | 31                         | 30                          | 29                    | 28                    | 27                    | 26 | 25 | 24                    | 23 | 22                    | 21 | 20 | 19 | 18 | 17                     | 16                      |
|-------|----------------------------|-----------------------------|-----------------------|-----------------------|-----------------------|----|----|-----------------------|----|-----------------------|----|----|----|----|------------------------|-------------------------|
| Name  | CDM4_FS_EOF_AFIFO_FULL     | CDM4_FS_EOF_AFIFO_EMPTY     | CDM4_FS_EOF_OVERFLOW  | CDM4_FS_EOF_UNDERFLOW | CDM4_FS_EOF_WFIFO_CNT |    |    |                       |    | CDM4_FS_EOF_RFIFO_CNT |    |    |    |    | CDM4_FS_SOF_AFIFO_FULL | CDM4_FS_SOF_AFIFO_EMPTY |
| Type  | RO                         | RO                          | RO                    | RO                    | RO                    |    |    |                       |    | RO                    |    |    |    |    | RO                     | RO                      |
| Reset | 0                          | 0                           | 0                     | 0                     | 0                     | 0  | 0  | 0                     | 0  | 0                     | 0  | 0  | 0  | 0  | 0                      | 0                       |
| Bit   | 15                         | 14                          | 13                    | 12                    | 11                    | 10 | 9  | 8                     | 7  | 6                     | 5  | 4  | 3  | 2  | 1                      | 0                       |
| Name  | CDM4_FS_SOF_AFIFO_OVERFLOW | CDM4_FS_SOF_AFIFO_UNDERFLOW | CDM4_FS_SOF_WFIFO_CNT |                       |                       |    |    | CDM4_FS_SOF_RFIFO_CNT |    |                       |    |    |    |    |                        |                         |
| Type  | RO                         | RO                          | RO                    |                       |                       |    |    | RO                    |    |                       |    |    |    |    |                        |                         |
| Reset | 0                          | 0                           | 0                     | 0                     | 0                     | 0  | 0  | 0                     | 0  | 0                     | 0  | 0  |    |    |                        |                         |

| Bit(s) | Name                        | Description                              |
|--------|-----------------------------|------------------------------------------|
| 31     | CDM4_FS_EOF_AFIFO_FULL      | CDM FS EOF AFIFO FULL                    |
| 30     | CDM4_FS_EOF_AFIFO_EMPTY     | CDM FS EOF AFIFO EMPTY                   |
| 29     | CDM4_FS_EOF_OVERFLOW        | CDM FS EOF AFIFO write when FIFO is full |
| 28     | CDM4_FS_EOF_UNDERFLOW       | CDM FS EOF AFIFO read when FIFO is empty |
| 27:23  | CDM4_FS_EOF_WFIFO_CNT       | CDM FS EOF AFIFO write count             |
| 22:18  | CDM4_FS_EOF_RFIFO_CNT       | CDM FS EOF AFIFO read count              |
| 17     | CDM4_FS_SOF_AFIFO_FULL      | CDM FS SOF AFIFO full                    |
| 16     | CDM4_FS_SOF_AFIFO_EMPTY     | CDM FS SOF AFIFO empty                   |
| 15     | CDM4_FS_SOF_AFIFO_OVERFLOW  | CDM FS SOF AFIFO write when FIFO is full |
| 14     | CDM4_FS_SOF_AFIFO_UNDERFLOW | CDM FS SOF AFIFO read when FIFO is empty |
| 13:9   | CDM4_FS_SOF_WFIFO_CNT       | CDM FS SOF AFIFO write count             |
| 8:4    | CDM4_FS_SOF_RFIFO_CNT       | CDM FS SOF AFIFO read count              |

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| Bit   | 31                      | 30                       | 29                           | 28                          | 27                      | 26 | 25 | 24 | 23                      | 22 | 21                        | 20                       | 19                          | 18                         | 17                         | 16                        |
|-------|-------------------------|--------------------------|------------------------------|-----------------------------|-------------------------|----|----|----|-------------------------|----|---------------------------|--------------------------|-----------------------------|----------------------------|----------------------------|---------------------------|
| Name  | CDM4_TS_DATA_AFIFO_FULL | CDM4_TS_DATA_AFIFO_EMPTY | CDM4_TS_DATA_AFIFO_UNDERFLOW | CDM4_TS_DATA_AFIFO_OVERFLOW | CDM4_TS_DATA_AFIFO_WCNT |    |    |    | CDM4_TS_DATA_AFIFO_RCNT |    |                           |                          | CDM4_TS_DFIFO_INVALID_WRITE | CDM4_TS_DFIFO_WRITE_ENABLE | CDM4_TS_DFIFO_INVALID_READ | CDM4_TS_DFIFO_READ_ENABLE |
| Type  | RO                      | RO                       | RO                           | RO                          | RO                      |    |    |    | RO                      |    |                           |                          | RO                          | RO                         | RO                         | RO                        |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                       | 0  | 0  | 0  | 0                       | 0  | 0                         | 0                        | 0                           | 0                          | 0                          | 0                         |
| Bit   | 15                      | 14                       | 13                           | 12                          | 11                      | 10 | 9  | 8  | 7                       | 6  | 5                         | 4                        | 3                           | 2                          | 1                          | 0                         |
| Name  | CDM4_TS_DFIFO_CNT       |                          |                              |                             |                         |    |    |    |                         |    | CDM4_TS_PARSER_FIFO_EMPTY | CDM4_TS_PARSER_FIFO_FULL |                             |                            |                            |                           |
| Type  | RO                      |                          |                              |                             |                         |    |    |    |                         |    | RO                        | RO                       |                             |                            |                            |                           |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                       | 0  | 0  | 0  | 0                       | 0  | 0                         | 0                        |                             |                            |                            |                           |

| Bit(s) | Name                         | Description                             |
|--------|------------------------------|-----------------------------------------|
| 31     | CDM4_TS_DATA_AFIFO_FULL      | CDM TS DATA AFIFO full                  |
| 30     | CDM4_TS_DATA_AFIFO_EMPTY     | CDM TS DATA AFIFO empty                 |
| 29     | CDM4_TS_DATA_AFIFO_UNDERFLOW | CDM TS data AFIFO read when AFIFO empty |
| 28     | CDM4_TS_DATA_AFIFO_OVERFLOW  | CDM TS data AFIFO write when AFIFO full |
| 27:24  | CDM4_TS_DATA_AFIFO_WCNT      | CDM TS data AFIFO write count           |
| 23:20  | CDM4_TS_DATA_AFIFO_RCNT      | CDM TS data AFIFO read count            |
| 19     | CDM4_TS_DFIFO_INVALID_WRITE  | CDM TS 8K SRAM invalid write            |
| 18     | CDM4_TS_DFIFO_WRITE_ENABLE   | CDM TS 8K SRAM write enable             |
| 17     | CDM4_TS_DFIFO_INVALID_READ   | CDM TS 8K SRAM invalid read             |
| 16     | CDM4_TS_DFIFO_READ_ENABLE    | CDM TS 8K SRAM read enable              |
| 15:6   | CDM4_TS_DFIFO_CNT            | CDM TS 8K SRAM count                    |
| 5      | CDM4_TS_PARSER_FIFO_EMPTY    | CDM TS parser FIFO empty                |
| 4      | CDM4_TS_PARSER_FIFO_FULL     | CDM TS parser FIFO full                 |

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| Bit   | 31                         | 30                          | 29                         | 28                          | 27                     | 26 | 25 | 24                     | 23 | 22                     | 21 | 20 | 19 | 18 | 17                     | 16                      |
|-------|----------------------------|-----------------------------|----------------------------|-----------------------------|------------------------|----|----|------------------------|----|------------------------|----|----|----|----|------------------------|-------------------------|
| Name  | CDM4_TS_EOF_AFIFO_FULL     | CDM4_TS_EOF_AFIFO_EMPTY     | CDM4_TS_EOF_AFIFO_OVERFLOW | CDM4_TS_EOF_AFIFO_UNDERFLOW | CDM4_TS_EOF_AFIFO_WCNT |    |    |                        |    | CDM4_TS_EOF_AFIFO_RCNT |    |    |    |    | CDM4_TS_SOF_AFIFO_FULL | CDM4_TS_SOF_AFIFO_EMPTY |
| Type  | RO                         | RO                          | RO                         | RO                          | RO                     |    |    |                        |    | RO                     |    |    |    |    | RO                     | RO                      |
| Reset | 0                          | 0                           | 0                          | 0                           | 0                      | 0  | 0  | 0                      | 0  | 0                      | 0  | 0  | 0  | 0  | 0                      | 0                       |
| Bit   | 15                         | 14                          | 13                         | 12                          | 11                     | 10 | 9  | 8                      | 7  | 6                      | 5  | 4  | 3  | 2  | 1                      | 0                       |
| Name  | CDM4_TS_SOF_AFIFO_OVERFLOW | CDM4_TS_SOF_AFIFO_UNDERFLOW | CDM4_TS_SOF_AFIFO_WCNT     |                             |                        |    |    | CDM4_TS_SOF_AFIFO_RCNT |    |                        |    |    |    |    |                        |                         |
| Type  | RO                         | RO                          | RO                         |                             |                        |    |    | RO                     |    |                        |    |    |    |    |                        |                         |
| Reset | 0                          | 0                           | 0                          | 0                           | 0                      | 0  | 0  | 0                      | 0  | 0                      | 0  | 0  |    |    |                        |                         |

| Bit(s) | Name                        | Description                              |
|--------|-----------------------------|------------------------------------------|
| 31     | CDM4_TS_EOF_AFIFO_FULL      | CDM TS EOF AFIFO full                    |
| 30     | CDM4_TS_EOF_AFIFO_EMPTY     | CDM TS EOF AFIFO empty                   |
| 29     | CDM4_TS_EOF_AFIFO_OVERFLOW  | CDM TS EOF AFIFO write when FIFO is full |
| 28     | CDM4_TS_EOF_AFIFO_UNDERFLOW | CDM TS EOF AFIFO read when FIFO is empty |
| 27:23  | CDM4_TS_EOF_AFIFO_WCNT      | CDM TS EOF AFIFO write count             |
| 22:18  | CDM4_TS_EOF_AFIFO_RCNT      | CDM TS EOF AFIFO read count              |
| 17     | CDM4_TS_SOF_AFIFO_FULL      | CDM TS SOF AFIFO full                    |
| 16     | CDM4_TS_SOF_AFIFO_EMPTY     | CDM TS SOF AFIFO empty                   |
| 15     | CDM4_TS_SOF_AFIFO_OVERFLOW  | CDM TS SOF AFIFO write when FIFO is full |
| 14     | CDM4_TS_SOF_AFIFO_UNDERFLOW | CDM TS SOF AFIFO read when FIFO is empty |
| 13:9   | CDM4_TS_SOF_AFIFO_WCNT      | CDM TS SOF AFIFO write count             |
| 8:4    | CDM4_TS_SOF_AFIFO_RCNT      | CDM TS SOF AFIFO read count              |

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| Bit   | 31                      | 30                       | 29                           | 28                          | 27                        | 26                       | 25               | 24 | 23 | 22 | 21                       | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------------|--------------------------|------------------------------|-----------------------------|---------------------------|--------------------------|------------------|----|----|----|--------------------------|----|----|----|----|----|
| Name  | CDM5_FS_DATA_AFIFO_FULL | CDM5_FS_DATA_AFIFO_EMPTY | CDM5_FS_DATA_AFIFO_UNDERFLOW | CDM5_FS_DATA_AFIFO_OVERFLOW | CDM5_FS_DATA_AFIFO_W_CNT  |                          |                  |    |    |    | CDM5_FS_DATA_AFIFO_R_CNT |    |    |    |    |    |
| Type  | RO                      | RO                       | RO                           | RO                          | RO                        |                          |                  |    |    |    | RO                       |    |    |    |    |    |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                         | 0                        | 0                | 0  | 0  | 0  | 0                        | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                      | 14                       | 13                           | 12                          | 11                        | 10                       | 9                | 8  | 7  | 6  | 5                        | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM5_SRAM_WR_ENABLE     | CDM5_SRAM_RD_ENABLE      | CDM5_FS_DFIFO_INVLD_WR       | CDM5_FS_DFIFO_INVLD_RD      | CDM5_FS_PARSER_FIFO_EMPTY | CDM5_FS_PARSER_FIFO_FULL | CDM5_RX_FIFO_CNT |    |    |    |                          |    |    |    |    |    |
| Type  | RO                      | RO                       | RO                           | RO                          | RO                        | RO                       | RO               |    |    |    |                          |    |    |    |    |    |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                         | 0                        | 0                | 0  | 0  | 0  | 0                        | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                         | Description                             |
|--------|------------------------------|-----------------------------------------|
| 31     | CDM5_FS_DATA_AFIFO_FULL      | CDM FS data AFIFO full                  |
| 30     | CDM5_FS_DATA_AFIFO_EMPTY     | CDM FS data AFIFO empty                 |
| 29     | CDM5_FS_DATA_AFIFO_UNDERFLOW | CDM FS data AFIFO read when AFIFO empty |
| 28     | CDM5_FS_DATA_AFIFO_OVERFLOW  | CDM FS data AFIFO write when AFIFO full |
| 27:22  | CDM5_FS_DATA_AFIFO_W_CNT     | CDM FS data AFIFO write count           |
| 21:16  | CDM5_FS_DATA_AFIFO_R_CNT     | CDM FS data AFIFO read count            |
| 15     | CDM5_SRAM_WR_ENABLE          | CDM FS 8K SRAM write enable             |
| 14     | CDM5_SRAM_RD_ENABLE          | CDM FS 8K SRAM read enable              |
| 13     | CDM5_FS_DFIFO_INVLD_WR       | CDM FS 8K SRAM invalid write            |
| 12     | CDM5_FS_DFIFO_INVLD_RD       | CDM FS 8K SRAM invalid read             |
| 11     | CDM5_FS_PARSER_FIFO_EMPTY    | CDM FS parser FIFO empty                |
| 10     | CDM5_FS_PARSER_FIFO_FULL     | CDM FS parser FIFO full                 |
| 9:0    | CDM5_RX_FIFO_CNT             | CDM FS 8K SRAM count                    |



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| Bit   | 31                         | 30                          | 29                    | 28                    | 27                    | 26 | 25 | 24                    | 23 | 22                    | 21 | 20 | 19 | 18 | 17                     | 16                      |
|-------|----------------------------|-----------------------------|-----------------------|-----------------------|-----------------------|----|----|-----------------------|----|-----------------------|----|----|----|----|------------------------|-------------------------|
| Name  | CDM5_FS_EOF_AFIFO_FULL     | CDM5_FS_EOF_AFIFO_EMPTY     | CDM5_FS_EOF_OVERFLOW  | CDM5_FS_EOF_UNDERFLOW | CDM5_FS_EOF_WFIFO_CNT |    |    |                       |    | CDM5_FS_EOF_RFIFO_CNT |    |    |    |    | CDM5_FS_SOF_AFIFO_FULL | CDM5_FS_SOF_AFIFO_EMPTY |
| Type  | RO                         | RO                          | RO                    | RO                    | RO                    |    |    |                       |    | RO                    |    |    |    |    | RO                     | RO                      |
| Reset | 0                          | 0                           | 0                     | 0                     | 0                     | 0  | 0  | 0                     | 0  | 0                     | 0  | 0  | 0  | 0  | 0                      | 0                       |
| Bit   | 15                         | 14                          | 13                    | 12                    | 11                    | 10 | 9  | 8                     | 7  | 6                     | 5  | 4  | 3  | 2  | 1                      | 0                       |
| Name  | CDM5_FS_SOF_AFIFO_OVERFLOW | CDM5_FS_SOF_AFIFO_UNDERFLOW | CDM5_FS_SOF_WFIFO_CNT |                       |                       |    |    | CDM5_FS_SOF_RFIFO_CNT |    |                       |    |    |    |    |                        |                         |
| Type  | RO                         | RO                          | RO                    |                       |                       |    |    | RO                    |    |                       |    |    |    |    |                        |                         |
| Reset | 0                          | 0                           | 0                     | 0                     | 0                     | 0  | 0  | 0                     | 0  | 0                     | 0  | 0  |    |    |                        |                         |

| Bit(s) | Name                        | Description                              |
|--------|-----------------------------|------------------------------------------|
| 31     | CDM5_FS_EOF_AFIFO_FULL      | CDM FS EOF AFIFO FULL                    |
| 30     | CDM5_FS_EOF_AFIFO_EMPTY     | CDM FS EOF AFIFO EMPTY                   |
| 29     | CDM5_FS_EOF_OVERFLOW        | CDM FS EOF AFIFO write when FIFO is full |
| 28     | CDM5_FS_EOF_UNDERFLOW       | CDM FS EOF AFIFO read when FIFO is empty |
| 27:23  | CDM5_FS_EOF_WFIFO_CNT       | CDM FS EOF AFIFO write count             |
| 22:18  | CDM5_FS_EOF_RFIFO_CNT       | CDM FS EOF AFIFO read count              |
| 17     | CDM5_FS_SOF_AFIFO_FULL      | CDM FS SOF AFIFO full                    |
| 16     | CDM5_FS_SOF_AFIFO_EMPTY     | CDM FS SOF AFIFO empty                   |
| 15     | CDM5_FS_SOF_AFIFO_OVERFLOW  | CDM FS SOF AFIFO write when FIFO is full |
| 14     | CDM5_FS_SOF_AFIFO_UNDERFLOW | CDM FS SOF AFIFO read when FIFO is empty |
| 13:9   | CDM5_FS_SOF_WFIFO_CNT       | CDM FS SOF AFIFO write count             |
| 8:4    | CDM5_FS_SOF_RFIFO_CNT       | CDM FS SOF AFIFO read count              |

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| Bit   | 31                      | 30                       | 29                           | 28                          | 27                      | 26 | 25 | 24 | 23                      | 22 | 21                        | 20                       | 19                          | 18                         | 17                         | 16                        |
|-------|-------------------------|--------------------------|------------------------------|-----------------------------|-------------------------|----|----|----|-------------------------|----|---------------------------|--------------------------|-----------------------------|----------------------------|----------------------------|---------------------------|
| Name  | CDM5_TS_DATA_AFIFO_FULL | CDM5_TS_DATA_AFIFO_EMPTY | CDM5_TS_DATA_AFIFO_UNDERFLOW | CDM5_TS_DATA_AFIFO_OVERFLOW | CDM5_TS_DATA_AFIFO_WCNT |    |    |    | CDM5_TS_DATA_AFIFO_RCNT |    |                           |                          | CDM5_TS_DFIFO_INVALID_WRITE | CDM5_TS_DFIFO_WRITE_ENABLE | CDM5_TS_DFIFO_INVALID_READ | CDM5_TS_DFIFO_READ_ENABLE |
| Type  | RO                      | RO                       | RO                           | RO                          | RO                      |    |    |    | RO                      |    |                           |                          | RO                          | RO                         | RO                         | RO                        |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                       | 0  | 0  | 0  | 0                       | 0  | 0                         | 0                        | 0                           | 0                          | 0                          | 0                         |
| Bit   | 15                      | 14                       | 13                           | 12                          | 11                      | 10 | 9  | 8  | 7                       | 6  | 5                         | 4                        | 3                           | 2                          | 1                          | 0                         |
| Name  | CDM5_TS_DFIFO_CNT       |                          |                              |                             |                         |    |    |    |                         |    | CDM5_TS_PARSER_FIFO_EMPTY | CDM5_TS_PARSER_FIFO_FULL |                             |                            |                            |                           |
| Type  | RO                      |                          |                              |                             |                         |    |    |    |                         |    | RO                        | RO                       |                             |                            |                            |                           |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                       | 0  | 0  | 0  | 0                       | 0  | 0                         | 0                        |                             |                            |                            |                           |

| Bit(s) | Name                         | Description                             |
|--------|------------------------------|-----------------------------------------|
| 31     | CDM5_TS_DATA_AFIFO_FULL      | CDM TS DATA AFIFO full                  |
| 30     | CDM5_TS_DATA_AFIFO_EMPTY     | CDM TS DATA AFIFO empty                 |
| 29     | CDM5_TS_DATA_AFIFO_UNDERFLOW | CDM TS data AFIFO read when AFIFO empty |
| 28     | CDM5_TS_DATA_AFIFO_OVERFLOW  | CDM TS data AFIFO write when AFIFO full |
| 27:24  | CDM5_TS_DATA_AFIFO_WCNT      | CDM TS data AFIFO write count           |
| 23:20  | CDM5_TS_DATA_AFIFO_RCNT      | CDM TS data AFIFO read count            |
| 19     | CDM5_TS_DFIFO_INVALID_WRITE  | CDM TS 8K SRAM invalid write            |
| 18     | CDM5_TS_DFIFO_WRITE_ENABLE   | CDM TS 8K SRAM write enable             |
| 17     | CDM5_TS_DFIFO_INVALID_READ   | CDM TS 8K SRAM invalid read             |
| 16     | CDM5_TS_DFIFO_READ_ENABLE    | CDM TS 8K SRAM read enable              |
| 15:6   | CDM5_TS_DFIFO_CNT            | CDM TS 8K SRAM count                    |
| 5      | CDM5_TS_PARSER_FIFO_EMPTY    | CDM TS parser FIFO empty                |
| 4      | CDM5_TS_PARSER_FIFO_FULL     | CDM TS parser FIFO full                 |

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| Bit   | 31                         | 30                          | 29                         | 28                          | 27                     | 26 | 25 | 24                     | 23 | 22                     | 21 | 20 | 19 | 18 | 17                     | 16                      |
|-------|----------------------------|-----------------------------|----------------------------|-----------------------------|------------------------|----|----|------------------------|----|------------------------|----|----|----|----|------------------------|-------------------------|
| Name  | CDM5_TS_EOF_AFIFO_FULL     | CDM5_TS_EOF_AFIFO_EMPTY     | CDM5_TS_EOF_AFIFO_OVERFLOW | CDM5_TS_EOF_AFIFO_UNDERFLOW | CDM5_TS_EOF_AFIFO_WCNT |    |    |                        |    | CDM5_TS_EOF_AFIFO_RCNT |    |    |    |    | CDM5_TS_SOF_AFIFO_FULL | CDM5_TS_SOF_AFIFO_EMPTY |
| Type  | RO                         | RO                          | RO                         | RO                          | RO                     |    |    |                        |    | RO                     |    |    |    |    | RO                     | RO                      |
| Reset | 0                          | 0                           | 0                          | 0                           | 0                      | 0  | 0  | 0                      | 0  | 0                      | 0  | 0  | 0  | 0  | 0                      | 0                       |
| Bit   | 15                         | 14                          | 13                         | 12                          | 11                     | 10 | 9  | 8                      | 7  | 6                      | 5  | 4  | 3  | 2  | 1                      | 0                       |
| Name  | CDM5_TS_SOF_AFIFO_OVERFLOW | CDM5_TS_SOF_AFIFO_UNDERFLOW | CDM5_TS_SOF_AFIFO_WCNT     |                             |                        |    |    | CDM5_TS_SOF_AFIFO_RCNT |    |                        |    |    |    |    |                        |                         |
| Type  | RO                         | RO                          | RO                         |                             |                        |    |    | RO                     |    |                        |    |    |    |    |                        |                         |
| Reset | 0                          | 0                           | 0                          | 0                           | 0                      | 0  | 0  | 0                      | 0  | 0                      | 0  | 0  |    |    |                        |                         |

| Bit(s) | Name                        | Description                              |
|--------|-----------------------------|------------------------------------------|
| 31     | CDM5_TS_EOF_AFIFO_FULL      | CDM TS EOF AFIFO full                    |
| 30     | CDM5_TS_EOF_AFIFO_EMPTY     | CDM TS EOF AFIFO empty                   |
| 29     | CDM5_TS_EOF_AFIFO_OVERFLOW  | CDM TS EOF AFIFO write when FIFO is full |
| 28     | CDM5_TS_EOF_AFIFO_UNDERFLOW | CDM TS EOF AFIFO read when FIFO is empty |
| 27:23  | CDM5_TS_EOF_AFIFO_WCNT      | CDM TS EOF AFIFO write count             |
| 22:18  | CDM5_TS_EOF_AFIFO_RCNT      | CDM TS EOF AFIFO read count              |
| 17     | CDM5_TS_SOF_AFIFO_FULL      | CDM TS SOF AFIFO full                    |
| 16     | CDM5_TS_SOF_AFIFO_EMPTY     | CDM TS SOF AFIFO empty                   |
| 15     | CDM5_TS_SOF_AFIFO_OVERFLOW  | CDM TS SOF AFIFO write when FIFO is full |
| 14     | CDM5_TS_SOF_AFIFO_UNDERFLOW | CDM TS SOF AFIFO read when FIFO is empty |
| 13:9   | CDM5_TS_SOF_AFIFO_WCNT      | CDM TS SOF AFIFO write count             |
| 8:4    | CDM5_TS_SOF_AFIFO_RCNT      | CDM TS SOF AFIFO read count              |

151003BC FE\_CDM6\_FS\_DFIFO FE CDM6 FS data path FIFO debug 00000000

| Bit   | 31                      | 30                       | 29                           | 28                          | 27                        | 26                       | 25               | 24 | 23 | 22 | 21                       | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------------|--------------------------|------------------------------|-----------------------------|---------------------------|--------------------------|------------------|----|----|----|--------------------------|----|----|----|----|----|
| Name  | CDM6_FS_DATA_AFIFO_FULL | CDM6_FS_DATA_AFIFO_EMPTY | CDM6_FS_DATA_AFIFO_UNDERFLOW | CDM6_FS_DATA_AFIFO_OVERFLOW | CDM6_FS_DATA_AFIFO_W_CNT  |                          |                  |    |    |    | CDM6_FS_DATA_AFIFO_R_CNT |    |    |    |    |    |
| Type  | RO                      | RO                       | RO                           | RO                          | RO                        |                          |                  |    |    |    | RO                       |    |    |    |    |    |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                         | 0                        | 0                | 0  | 0  | 0  | 0                        | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                      | 14                       | 13                           | 12                          | 11                        | 10                       | 9                | 8  | 7  | 6  | 5                        | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM6_SRAM_WR_ENABLE     | CDM6_SRAM_RD_ENABLE      | CDM6_FS_DFIFO_INVLD_WR       | CDM6_FS_DFIFO_INVLD_RD      | CDM6_FS_PARSER_FIFO_EMPTY | CDM6_FS_PARSER_FIFO_FULL | CDM6_RX_FIFO_CNT |    |    |    |                          |    |    |    |    |    |
| Type  | RO                      | RO                       | RO                           | RO                          | RO                        | RO                       | RO               |    |    |    |                          |    |    |    |    |    |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                         | 0                        | 0                | 0  | 0  | 0  | 0                        | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                         | Description                             |
|--------|------------------------------|-----------------------------------------|
| 31     | CDM6_FS_DATA_AFIFO_FULL      | CDM FS data AFIFO full                  |
| 30     | CDM6_FS_DATA_AFIFO_EMPTY     | CDM FS data AFIFO empty                 |
| 29     | CDM6_FS_DATA_AFIFO_UNDERFLOW | CDM FS data AFIFO read when AFIFO empty |
| 28     | CDM6_FS_DATA_AFIFO_OVERFLOW  | CDM FS data AFIFO write when AFIFO full |
| 27:22  | CDM6_FS_DATA_AFIFO_W_CNT     | CDM FS data AFIFO write count           |
| 21:16  | CDM6_FS_DATA_AFIFO_R_CNT     | CDM FS data AFIFO read count            |
| 15     | CDM6_SRAM_WR_ENABLE          | CDM FS 8K SRAM write enable             |
| 14     | CDM6_SRAM_RD_ENABLE          | CDM FS 8K SRAM read enable              |
| 13     | CDM6_FS_DFIFO_INVLD_WR       | CDM FS 8K SRAM invalid write            |
| 12     | CDM6_FS_DFIFO_INVLD_RD       | CDM FS 8K SRAM invalid read             |
| 11     | CDM6_FS_PARSER_FIFO_EMPTY    | CDM FS parser FIFO empty                |
| 10     | CDM6_FS_PARSER_FIFO_FULL     | CDM FS parser FIFO full                 |
| 9:0    | CDM6_RX_FIFO_CNT             | CDM FS 8K SRAM count                    |

151003C0 FE\_CDM6\_FS\_INFO\_FIFO FE\_CDM6\_FS\_info\_path\_FIFO\_debug 00000000

| Bit   | 31                         | 30                          | 29                    | 28                    | 27                    | 26 | 25 | 24                    | 23 | 22                    | 21 | 20 | 19 | 18 | 17                     | 16                      |
|-------|----------------------------|-----------------------------|-----------------------|-----------------------|-----------------------|----|----|-----------------------|----|-----------------------|----|----|----|----|------------------------|-------------------------|
| Name  | CDM6_FS_EOF_AFIFO_FULL     | CDM6_FS_EOF_AFIFO_EMPTY     | CDM6_FS_EOF_OVERFLOW  | CDM6_FS_EOF_UNDERFLOW | CDM6_FS_EOF_WFIFO_CNT |    |    |                       |    | CDM6_FS_EOF_RFIFO_CNT |    |    |    |    | CDM6_FS_SOF_AFIFO_FULL | CDM6_FS_SOF_AFIFO_EMPTY |
| Type  | RO                         | RO                          | RO                    | RO                    | RO                    |    |    |                       |    | RO                    |    |    |    |    | RO                     | RO                      |
| Reset | 0                          | 0                           | 0                     | 0                     | 0                     | 0  | 0  | 0                     | 0  | 0                     | 0  | 0  | 0  | 0  | 0                      | 0                       |
| Bit   | 15                         | 14                          | 13                    | 12                    | 11                    | 10 | 9  | 8                     | 7  | 6                     | 5  | 4  | 3  | 2  | 1                      | 0                       |
| Name  | CDM6_FS_SOF_AFIFO_OVERFLOW | CDM6_FS_SOF_AFIFO_UNDERFLOW | CDM6_FS_SOF_WFIFO_CNT |                       |                       |    |    | CDM6_FS_SOF_RFIFO_CNT |    |                       |    |    |    |    |                        |                         |
| Type  | RO                         | RO                          | RO                    |                       |                       |    |    | RO                    |    |                       |    |    |    |    |                        |                         |
| Reset | 0                          | 0                           | 0                     | 0                     | 0                     | 0  | 0  | 0                     | 0  | 0                     | 0  | 0  |    |    |                        |                         |

| Bit(s) | Name                        | Description                              |
|--------|-----------------------------|------------------------------------------|
| 31     | CDM6_FS_EOF_AFIFO_FULL      | CDM FS EOF AFIFO FULL                    |
| 30     | CDM6_FS_EOF_AFIFO_EMPTY     | CDM FS EOF AFIFO EMPTY                   |
| 29     | CDM6_FS_EOF_OVERFLOW        | CDM FS EOF AFIFO write when FIFO is full |
| 28     | CDM6_FS_EOF_UNDERFLOW       | CDM FS EOF AFIFO read when FIFO is empty |
| 27:23  | CDM6_FS_EOF_WFIFO_CNT       | CDM FS EOF AFIFO write count             |
| 22:18  | CDM6_FS_EOF_RFIFO_CNT       | CDM FS EOF AFIFO read count              |
| 17     | CDM6_FS_SOF_AFIFO_FULL      | CDM FS SOF AFIFO full                    |
| 16     | CDM6_FS_SOF_AFIFO_EMPTY     | CDM FS SOF AFIFO empty                   |
| 15     | CDM6_FS_SOF_AFIFO_OVERFLOW  | CDM FS SOF AFIFO write when FIFO is full |
| 14     | CDM6_FS_SOF_AFIFO_UNDERFLOW | CDM FS SOF AFIFO read when FIFO is empty |
| 13:9   | CDM6_FS_SOF_WFIFO_CNT       | CDM FS SOF AFIFO write count             |
| 8:4    | CDM6_FS_SOF_RFIFO_CNT       | CDM FS SOF AFIFO read count              |

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| Bit   | 31                      | 30                       | 29                           | 28                          | 27                      | 26 | 25 | 24 | 23                      | 22 | 21                        | 20                       | 19                          | 18                         | 17                         | 16                        |
|-------|-------------------------|--------------------------|------------------------------|-----------------------------|-------------------------|----|----|----|-------------------------|----|---------------------------|--------------------------|-----------------------------|----------------------------|----------------------------|---------------------------|
| Name  | CDM6_TS_DATA_AFIFO_FULL | CDM6_TS_DATA_AFIFO_EMPTY | CDM6_TS_DATA_AFIFO_UNDERFLOW | CDM6_TS_DATA_AFIFO_OVERFLOW | CDM6_TS_DATA_AFIFO_WCNT |    |    |    | CDM6_TS_DATA_AFIFO_RCNT |    |                           |                          | CDM6_TS_DFIFO_INVALID_WRITE | CDM6_TS_DFIFO_WRITE_ENABLE | CDM6_TS_DFIFO_INVALID_READ | CDM6_TS_DFIFO_READ_ENABLE |
| Type  | RO                      | RO                       | RO                           | RO                          | RO                      |    |    |    | RO                      |    |                           |                          | RO                          | RO                         | RO                         | RO                        |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                       | 0  | 0  | 0  | 0                       | 0  | 0                         | 0                        | 0                           | 0                          | 0                          | 0                         |
| Bit   | 15                      | 14                       | 13                           | 12                          | 11                      | 10 | 9  | 8  | 7                       | 6  | 5                         | 4                        | 3                           | 2                          | 1                          | 0                         |
| Name  | CDM6_TS_DFIFO_CNT       |                          |                              |                             |                         |    |    |    |                         |    | CDM6_TS_PARSER_FIFO_EMPTY | CDM6_TS_PARSER_FIFO_FULL |                             |                            |                            |                           |
| Type  | RO                      |                          |                              |                             |                         |    |    |    |                         |    | RO                        | RO                       |                             |                            |                            |                           |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                       | 0  | 0  | 0  | 0                       | 0  | 0                         | 0                        |                             |                            |                            |                           |

| Bit(s) | Name                         | Description                             |
|--------|------------------------------|-----------------------------------------|
| 31     | CDM6_TS_DATA_AFIFO_FULL      | CDM TS DATA AFIFO full                  |
| 30     | CDM6_TS_DATA_AFIFO_EMPTY     | CDM TS DATA AFIFO empty                 |
| 29     | CDM6_TS_DATA_AFIFO_UNDERFLOW | CDM TS data AFIFO read when AFIFO empty |
| 28     | CDM6_TS_DATA_AFIFO_OVERFLOW  | CDM TS data AFIFO write when AFIFO full |
| 27:24  | CDM6_TS_DATA_AFIFO_WCNT      | CDM TS data AFIFO write count           |
| 23:20  | CDM6_TS_DATA_AFIFO_RCNT      | CDM TS data AFIFO read count            |
| 19     | CDM6_TS_DFIFO_INVALID_WRITE  | CDM TS 8K SRAM invalid write            |
| 18     | CDM6_TS_DFIFO_WRITE_ENABLE   | CDM TS 8K SRAM write enable             |
| 17     | CDM6_TS_DFIFO_INVALID_READ   | CDM TS 8K SRAM invalid read             |
| 16     | CDM6_TS_DFIFO_READ_ENABLE    | CDM TS 8K SRAM read enable              |
| 15:6   | CDM6_TS_DFIFO_CNT            | CDM TS 8K SRAM count                    |
| 5      | CDM6_TS_PARSER_FIFO_EMPTY    | CDM TS parser FIFO empty                |
| 4      | CDM6_TS_PARSER_FIFO_FULL     | CDM TS parser FIFO full                 |

151003C8 FE\_CDM6\_TS\_INFO\_FIFO FE\_CDM6\_TS\_info\_path\_FIFO\_debug 00000000

| Bit   | 31                         | 30                          | 29                         | 28                          | 27                     | 26 | 25 | 24                     | 23 | 22                     | 21 | 20 | 19 | 18 | 17                     | 16                      |
|-------|----------------------------|-----------------------------|----------------------------|-----------------------------|------------------------|----|----|------------------------|----|------------------------|----|----|----|----|------------------------|-------------------------|
| Name  | CDM6_TS_EOF_AFIFO_FULL     | CDM6_TS_EOF_AFIFO_EMPTY     | CDM6_TS_EOF_AFIFO_OVERFLOW | CDM6_TS_EOF_AFIFO_UNDERFLOW | CDM6_TS_EOF_AFIFO_WCNT |    |    |                        |    | CDM6_TS_EOF_AFIFO_RCNT |    |    |    |    | CDM6_TS_SOF_AFIFO_FULL | CDM6_TS_SOF_AFIFO_EMPTY |
| Type  | RO                         | RO                          | RO                         | RO                          | RO                     |    |    |                        |    | RO                     |    |    |    |    | RO                     | RO                      |
| Reset | 0                          | 0                           | 0                          | 0                           | 0                      | 0  | 0  | 0                      | 0  | 0                      | 0  | 0  | 0  | 0  | 0                      | 0                       |
| Bit   | 15                         | 14                          | 13                         | 12                          | 11                     | 10 | 9  | 8                      | 7  | 6                      | 5  | 4  | 3  | 2  | 1                      | 0                       |
| Name  | CDM6_TS_SOF_AFIFO_OVERFLOW | CDM6_TS_SOF_AFIFO_UNDERFLOW | CDM6_TS_SOF_AFIFO_WCNT     |                             |                        |    |    | CDM6_TS_SOF_AFIFO_RCNT |    |                        |    |    |    |    |                        |                         |
| Type  | RO                         | RO                          | RO                         |                             |                        |    |    | RO                     |    |                        |    |    |    |    |                        |                         |
| Reset | 0                          | 0                           | 0                          | 0                           | 0                      | 0  | 0  | 0                      | 0  | 0                      | 0  | 0  |    |    |                        |                         |

| Bit(s) | Name                        | Description                              |
|--------|-----------------------------|------------------------------------------|
| 31     | CDM6_TS_EOF_AFIFO_FULL      | CDM TS EOF AFIFO full                    |
| 30     | CDM6_TS_EOF_AFIFO_EMPTY     | CDM TS EOF AFIFO empty                   |
| 29     | CDM6_TS_EOF_AFIFO_OVERFLOW  | CDM TS EOF AFIFO write when FIFO is full |
| 28     | CDM6_TS_EOF_AFIFO_UNDERFLOW | CDM TS EOF AFIFO read when FIFO is empty |
| 27:23  | CDM6_TS_EOF_AFIFO_WCNT      | CDM TS EOF AFIFO write count             |
| 22:18  | CDM6_TS_EOF_AFIFO_RCNT      | CDM TS EOF AFIFO read count              |
| 17     | CDM6_TS_SOF_AFIFO_FULL      | CDM TS SOF AFIFO full                    |
| 16     | CDM6_TS_SOF_AFIFO_EMPTY     | CDM TS SOF AFIFO empty                   |
| 15     | CDM6_TS_SOF_AFIFO_OVERFLOW  | CDM TS SOF AFIFO write when FIFO is full |
| 14     | CDM6_TS_SOF_AFIFO_UNDERFLOW | CDM TS SOF AFIFO read when FIFO is empty |
| 13:9   | CDM6_TS_SOF_AFIFO_WCNT      | CDM TS SOF AFIFO write count             |
| 8:4    | CDM6_TS_SOF_AFIFO_RCNT      | CDM TS SOF AFIFO read count              |

151003CC FE CDM7\_FS\_DFIFO FE CDM7 FS data path FIFO debug 00000000

| Bit   | 31                      | 30                       | 29                           | 28                          | 27                        | 26                       | 25               | 24 | 23 | 22 | 21                       | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------------|--------------------------|------------------------------|-----------------------------|---------------------------|--------------------------|------------------|----|----|----|--------------------------|----|----|----|----|----|
| Name  | CDM7_FS_DATA_AFIFO_FULL | CDM7_FS_DATA_AFIFO_EMPTY | CDM7_FS_DATA_AFIFO_UNDERFLOW | CDM7_FS_DATA_AFIFO_OVERFLOW | CDM7_FS_DATA_AFIFO_W_CNT  |                          |                  |    |    |    | CDM7_FS_DATA_AFIFO_R_CNT |    |    |    |    |    |
| Type  | RO                      | RO                       | RO                           | RO                          | RO                        |                          |                  |    |    |    | RO                       |    |    |    |    |    |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                         | 0                        | 0                | 0  | 0  | 0  | 0                        | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                      | 14                       | 13                           | 12                          | 11                        | 10                       | 9                | 8  | 7  | 6  | 5                        | 4  | 3  | 2  | 1  | 0  |
| Name  | CDM7_SRAM_WR_ENABLE     | CDM7_SRAM_RD_ENABLE      | CDM7_FS_DFIFO_INVLD_WR       | CDM7_FS_DFIFO_INVLD_RD      | CDM7_FS_PARSER_FIFO_EMPTY | CDM7_FS_PARSER_FIFO_FULL | CDM7_RX_FIFO_CNT |    |    |    |                          |    |    |    |    |    |
| Type  | RO                      | RO                       | RO                           | RO                          | RO                        | RO                       | RO               |    |    |    |                          |    |    |    |    |    |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                         | 0                        | 0                | 0  | 0  | 0  | 0                        | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                         | Description                             |
|--------|------------------------------|-----------------------------------------|
| 31     | CDM7_FS_DATA_AFIFO_FULL      | CDM FS data AFIFO full                  |
| 30     | CDM7_FS_DATA_AFIFO_EMPTY     | CDM FS data AFIFO empty                 |
| 29     | CDM7_FS_DATA_AFIFO_UNDERFLOW | CDM FS data AFIFO read when AFIFO empty |
| 28     | CDM7_FS_DATA_AFIFO_OVERFLOW  | CDM FS data AFIFO write when AFIFO full |
| 27:22  | CDM7_FS_DATA_AFIFO_W_CNT     | CDM FS data AFIFO write count           |
| 21:16  | CDM7_FS_DATA_AFIFO_R_CNT     | CDM FS data AFIFO read count            |
| 15     | CDM7_SRAM_WR_ENABLE          | CDM FS 8K SRAM write enable             |
| 14     | CDM7_SRAM_RD_ENABLE          | CDM FS 8K SRAM read enable              |
| 13     | CDM7_FS_DFIFO_INVLD_WR       | CDM FS 8K SRAM invalid write            |
| 12     | CDM7_FS_DFIFO_INVLD_RD       | CDM FS 8K SRAM invalid read             |
| 11     | CDM7_FS_PARSER_FIFO_EMPTY    | CDM FS parser FIFO empty                |
| 10     | CDM7_FS_PARSER_FIFO_FULL     | CDM FS parser FIFO full                 |
| 9:0    | CDM7_RX_FIFO_CNT             | CDM FS 8K SRAM count                    |



151003D0 FE\_CDM7\_FS\_INFO\_FIFO FE\_CDM7\_FS\_info\_path\_FIFO\_debug 00000000

| Bit   | 31                         | 30                          | 29                    | 28                    | 27                    | 26 | 25 | 24                    | 23 | 22                    | 21 | 20 | 19 | 18 | 17                     | 16                      |
|-------|----------------------------|-----------------------------|-----------------------|-----------------------|-----------------------|----|----|-----------------------|----|-----------------------|----|----|----|----|------------------------|-------------------------|
| Name  | CDM7_FS_EOF_AFIFO_FULL     | CDM7_FS_EOF_AFIFO_EMPTY     | CDM7_FS_EOF_OVERFLOW  | CDM7_FS_EOF_UNDERFLOW | CDM7_FS_EOF_WFIFO_CNT |    |    |                       |    | CDM7_FS_EOF_RFIFO_CNT |    |    |    |    | CDM7_FS_SOF_AFIFO_FULL | CDM7_FS_SOF_AFIFO_EMPTY |
| Type  | RO                         | RO                          | RO                    | RO                    | RO                    |    |    |                       |    | RO                    |    |    |    |    | RO                     | RO                      |
| Reset | 0                          | 0                           | 0                     | 0                     | 0                     | 0  | 0  | 0                     | 0  | 0                     | 0  | 0  | 0  | 0  | 0                      | 0                       |
| Bit   | 15                         | 14                          | 13                    | 12                    | 11                    | 10 | 9  | 8                     | 7  | 6                     | 5  | 4  | 3  | 2  | 1                      | 0                       |
| Name  | CDM7_FS_SOF_AFIFO_OVERFLOW | CDM7_FS_SOF_AFIFO_UNDERFLOW | CDM7_FS_SOF_WFIFO_CNT |                       |                       |    |    | CDM7_FS_SOF_RFIFO_CNT |    |                       |    |    |    |    |                        |                         |
| Type  | RO                         | RO                          | RO                    |                       |                       |    |    | RO                    |    |                       |    |    |    |    |                        |                         |
| Reset | 0                          | 0                           | 0                     | 0                     | 0                     | 0  | 0  | 0                     | 0  | 0                     | 0  | 0  |    |    |                        |                         |

| Bit(s) | Name                        | Description                              |
|--------|-----------------------------|------------------------------------------|
| 31     | CDM7_FS_EOF_AFIFO_FULL      | CDM FS EOF AFIFO FULL                    |
| 30     | CDM7_FS_EOF_AFIFO_EMPTY     | CDM FS EOF AFIFO EMPTY                   |
| 29     | CDM7_FS_EOF_OVERFLOW        | CDM FS EOF AFIFO write when FIFO is full |
| 28     | CDM7_FS_EOF_UNDERFLOW       | CDM FS EOF AFIFO read when FIFO is empty |
| 27:23  | CDM7_FS_EOF_WFIFO_CNT       | CDM FS EOF AFIFO write count             |
| 22:18  | CDM7_FS_EOF_RFIFO_CNT       | CDM FS EOF AFIFO read count              |
| 17     | CDM7_FS_SOF_AFIFO_FULL      | CDM FS SOF AFIFO full                    |
| 16     | CDM7_FS_SOF_AFIFO_EMPTY     | CDM FS SOF AFIFO empty                   |
| 15     | CDM7_FS_SOF_AFIFO_OVERFLOW  | CDM FS SOF AFIFO write when FIFO is full |
| 14     | CDM7_FS_SOF_AFIFO_UNDERFLOW | CDM FS SOF AFIFO read when FIFO is empty |
| 13:9   | CDM7_FS_SOF_WFIFO_CNT       | CDM FS SOF AFIFO write count             |
| 8:4    | CDM7_FS_SOF_RFIFO_CNT       | CDM FS SOF AFIFO read count              |

151003D4 FE\_CDM7\_TS\_DFIFO FE CDM7 TS data path FIFO debug 00000000

| Bit   | 31                      | 30                       | 29                           | 28                          | 27                      | 26 | 25 | 24 | 23                      | 22 | 21                        | 20                       | 19                          | 18                         | 17                         | 16                        |
|-------|-------------------------|--------------------------|------------------------------|-----------------------------|-------------------------|----|----|----|-------------------------|----|---------------------------|--------------------------|-----------------------------|----------------------------|----------------------------|---------------------------|
| Name  | CDM7_TS_DATA_AFIFO_FULL | CDM7_TS_DATA_AFIFO_EMPTY | CDM7_TS_DATA_AFIFO_UNDERFLOW | CDM7_TS_DATA_AFIFO_OVERFLOW | CDM7_TS_DATA_AFIFO_WCNT |    |    |    | CDM7_TS_DATA_AFIFO_RCNT |    |                           |                          | CDM7_TS_DFIFO_INVALID_WRITE | CDM7_TS_DFIFO_WRITE_ENABLE | CDM7_TS_DFIFO_INVALID_READ | CDM7_TS_DFIFO_READ_ENABLE |
| Type  | RO                      | RO                       | RO                           | RO                          | RO                      |    |    |    | RO                      |    |                           |                          | RO                          | RO                         | RO                         | RO                        |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                       | 0  | 0  | 0  | 0                       | 0  | 0                         | 0                        | 0                           | 0                          | 0                          | 0                         |
| Bit   | 15                      | 14                       | 13                           | 12                          | 11                      | 10 | 9  | 8  | 7                       | 6  | 5                         | 4                        | 3                           | 2                          | 1                          | 0                         |
| Name  | CDM7_TS_DFIFO_CNT       |                          |                              |                             |                         |    |    |    |                         |    | CDM7_TS_PARSER_FIFO_EMPTY | CDM7_TS_PARSER_FIFO_FULL |                             |                            |                            |                           |
| Type  | RO                      |                          |                              |                             |                         |    |    |    |                         |    | RO                        | RO                       |                             |                            |                            |                           |
| Reset | 0                       | 0                        | 0                            | 0                           | 0                       | 0  | 0  | 0  | 0                       | 0  | 0                         | 0                        |                             |                            |                            |                           |

| Bit(s) | Name                         | Description                             |
|--------|------------------------------|-----------------------------------------|
| 31     | CDM7_TS_DATA_AFIFO_FULL      | CDM TS DATA AFIFO full                  |
| 30     | CDM7_TS_DATA_AFIFO_EMPTY     | CDM TS DATA AFIFO empty                 |
| 29     | CDM7_TS_DATA_AFIFO_UNDERFLOW | CDM TS data AFIFO read when AFIFO empty |
| 28     | CDM7_TS_DATA_AFIFO_OVERFLOW  | CDM TS data AFIFO write when AFIFO full |
| 27:24  | CDM7_TS_DATA_AFIFO_WCNT      | CDM TS data AFIFO write count           |
| 23:20  | CDM7_TS_DATA_AFIFO_RCNT      | CDM TS data AFIFO read count            |
| 19     | CDM7_TS_DFIFO_INVALID_WRITE  | CDM TS 8K SRAM invalid write            |
| 18     | CDM7_TS_DFIFO_WRITE_ENABLE   | CDM TS 8K SRAM write enable             |
| 17     | CDM7_TS_DFIFO_INVALID_READ   | CDM TS 8K SRAM invalid read             |
| 16     | CDM7_TS_DFIFO_READ_ENABLE    | CDM TS 8K SRAM read enable              |
| 15:6   | CDM7_TS_DFIFO_CNT            | CDM TS 8K SRAM count                    |
| 5      | CDM7_TS_PARSER_FIFO_EMPTY    | CDM TS parser FIFO empty                |
| 4      | CDM7_TS_PARSER_FIFO_FULL     | CDM TS parser FIFO full                 |

151003D8 FE\_CDM7\_TS\_INFO\_FIFO FE CDM7 TS info path FIFO debug 00000000

| Bit   | 31                         | 30                          | 29                         | 28                          | 27                     | 26 | 25 | 24                     | 23 | 22                     | 21 | 20 | 19 | 18 | 17                     | 16                      |
|-------|----------------------------|-----------------------------|----------------------------|-----------------------------|------------------------|----|----|------------------------|----|------------------------|----|----|----|----|------------------------|-------------------------|
| Name  | CDM7_TS_EOF_AFIFO_FULL     | CDM7_TS_EOF_AFIFO_EMPTY     | CDM7_TS_EOF_AFIFO_OVERFLOW | CDM7_TS_EOF_AFIFO_UNDERFLOW | CDM7_TS_EOF_AFIFO_WCNT |    |    |                        |    | CDM7_TS_EOF_AFIFO_RCNT |    |    |    |    | CDM7_TS_SOF_AFIFO_FULL | CDM7_TS_SOF_AFIFO_EMPTY |
| Type  | RO                         | RO                          | RO                         | RO                          | RO                     |    |    |                        |    | RO                     |    |    |    |    | RO                     | RO                      |
| Reset | 0                          | 0                           | 0                          | 0                           | 0                      | 0  | 0  | 0                      | 0  | 0                      | 0  | 0  | 0  | 0  | 0                      | 0                       |
| Bit   | 15                         | 14                          | 13                         | 12                          | 11                     | 10 | 9  | 8                      | 7  | 6                      | 5  | 4  | 3  | 2  | 1                      | 0                       |
| Name  | CDM7_TS_SOF_AFIFO_OVERFLOW | CDM7_TS_SOF_AFIFO_UNDERFLOW | CDM7_TS_SOF_AFIFO_WCNT     |                             |                        |    |    | CDM7_TS_SOF_AFIFO_RCNT |    |                        |    |    |    |    |                        |                         |
| Type  | RO                         | RO                          | RO                         |                             |                        |    |    | RO                     |    |                        |    |    |    |    |                        |                         |
| Reset | 0                          | 0                           | 0                          | 0                           | 0                      | 0  | 0  | 0                      | 0  | 0                      | 0  | 0  |    |    |                        |                         |

| Bit(s) | Name                        | Description                              |
|--------|-----------------------------|------------------------------------------|
| 31     | CDM7_TS_EOF_AFIFO_FULL      | CDM TS EOF AFIFO full                    |
| 30     | CDM7_TS_EOF_AFIFO_EMPTY     | CDM TS EOF AFIFO empty                   |
| 29     | CDM7_TS_EOF_AFIFO_OVERFLOW  | CDM TS EOF AFIFO write when FIFO is full |
| 28     | CDM7_TS_EOF_AFIFO_UNDERFLOW | CDM TS EOF AFIFO read when FIFO is empty |
| 27:23  | CDM7_TS_EOF_AFIFO_WCNT      | CDM TS EOF AFIFO write count             |
| 22:18  | CDM7_TS_EOF_AFIFO_RCNT      | CDM TS EOF AFIFO read count              |
| 17     | CDM7_TS_SOF_AFIFO_FULL      | CDM TS SOF AFIFO full                    |
| 16     | CDM7_TS_SOF_AFIFO_EMPTY     | CDM TS SOF AFIFO empty                   |
| 15     | CDM7_TS_SOF_AFIFO_OVERFLOW  | CDM TS SOF AFIFO write when FIFO is full |
| 14     | CDM7_TS_SOF_AFIFO_UNDERFLOW | CDM TS SOF AFIFO read when FIFO is empty |
| 13:9   | CDM7_TS_SOF_AFIFO_WCNT      | CDM TS SOF AFIFO write count             |
| 8:4    | CDM7_TS_SOF_AFIFO_RCNT      | CDM TS SOF AFIFO read count              |

151003DC FE\_CDM1\_1\_FIFO\_DBG1 FE\_CDM1\_1\_FIFO\_status\_debug1 00000000

| Bit   | 31                    | 30 | 29 | 28 | 27                      | 26                      | 25                       | 24                       | 23                    | 22 | 21 | 20 | 19                        | 18 | 17                       | 16 |
|-------|-----------------------|----|----|----|-------------------------|-------------------------|--------------------------|--------------------------|-----------------------|----|----|----|---------------------------|----|--------------------------|----|
| Name  | cdm1_1_fs_infifo_cnt  |    |    |    | cdm1_1_fs_infifo_rvalid | cdm1_1_fs_infifo_wvalid | cdm1_1_fs_outfifo_rvalid | cdm1_1_fs_outfifo_wvalid | cdm1_1_fs_outfifo_cnt |    |    |    | cdm1_1_ts_infifo_cnt      |    |                          |    |
| Type  | RO                    |    |    |    | RO                      | RO                      | RO                       | RO                       | RO                    |    |    |    | RO                        |    |                          |    |
| Reset | 0                     | 0  | 0  | 0  | 0                       | 0                       | 0                        | 0                        | 0                     | 0  | 0  | 0  | 0                         | 0  | 0                        | 0  |
| Bit   | 15                    | 14 | 13 | 12 | 11                      | 10                      | 9                        | 8                        | 7                     | 6  | 5  | 4  | 3                         | 2  | 1                        | 0  |
| Name  | cdm1_1_ts_outfifo_cnt |    |    |    | cdm1_1_ts_infifo_rvalid | cdm1_1_ts_infifo_wvalid | cdm1_1_ts_outfifo_rvalid | cdm1_1_ts_outfifo_wvalid | cdm1_1_tso_fifo_cnt   |    |    |    | cdm1_1_fs_data_fifo_empty |    | cdm1_1_fs_data_fifo_full |    |
| Type  | RO                    |    |    |    | RO                      | RO                      | RO                       | RO                       | RO                    |    |    |    | RO                        |    | RO                       |    |
| Reset | 0                     | 0  | 0  | 0  | 0                       | 0                       | 0                        | 0                        | 0                     | 0  | 0  | 0  | 0                         | 0  | 0                        | 0  |

| Bit(s) | Name                       | Description                                         |
|--------|----------------------------|-----------------------------------------------------|
| 31:28  | cdm1_1_fs_infifo_cnt       | CDM FS parser infifo count                          |
| 27     | cdm1_1_fs_infifo_rvalid    | CDM FS parser infifo read valid                     |
| 26     | cdm1_1_fs_infifo_wvalid    | CDM FS parser infifo write valid                    |
| 25     | cdm1_1_fs_outfifo_rvalid   | CDM FS parser outfifo read valid                    |
| 24     | cdm1_1_fs_outfifo_wvalid   | CDM FS parser outfifo write valid                   |
| 23:20  | cdm1_1_fs_outfifo_cnt      | CDM FS parser outfifo count                         |
| 19:16  | cdm1_1_ts_infifo_cnt       | CDM TS parser infifo count                          |
| 15:12  | cdm1_1_ts_outfifo_cnt      | CDM TS parser outfifo count                         |
| 11     | cdm1_1_ts_infifo_rvalid    | CDM TS parser infifo read valid                     |
| 10     | cdm1_1_ts_infifo_wvalid    | CDM TS parser infifo write valid                    |
| 9      | cdm1_1_ts_outfifo_rvalid   | CDM TS parser outfifo read valid                    |
| 8      | cdm1_1_ts_outfifo_wvalid   | CDM TS parser outfifo write valid                   |
| 7:2    | cdm1_1_tso_fifo_cnt        | CDM TSO FIFO count                                  |
| 1      | cdm1_1_fs_data_afifo_empty | FS Data path Async FIFO in CDM fs_fifo module empty |
| 0      | cdm1_1_fs_data_afifo_full  | FS Data path Async FIFO in CDM fs_fifo module full  |

151003F0 FE CDM1\_1 FIFO DBG2 FE CDM1\_1 FIFO status debug2 00000000

| Bit   | 31                            | 30                             | 29                            | 28                             | 27                       | 26 | 25 | 24 | 23                                | 22                                 | 21                               | 20                                | 19                                 | 18                               | 17 | 16 |
|-------|-------------------------------|--------------------------------|-------------------------------|--------------------------------|--------------------------|----|----|----|-----------------------------------|------------------------------------|----------------------------------|-----------------------------------|------------------------------------|----------------------------------|----|----|
| Name  | cdm1_1_fs_data_afifo_overflow | cdm1_1_fs_data_afifo_underflow | cdm1_1_fs_data_afifo_cnt      |                                |                          |    |    |    | cdm1_1_cdm_rx_info_sof_afifo_full | cdm1_1_cdm_rx_info_sof_afifo_empty | cdm1_1_cdm_rx_info_sof_afifo_cnt | cdm1_1_cdm_rx_info_eof_afifo_full | cdm1_1_cdm_rx_info_eof_afifo_empty | cdm1_1_cdm_rx_info_eof_afifo_cnt |    |    |
| Type  | RO                            | RO                             | RO                            |                                |                          |    |    |    | RO                                | RO                                 | RO                               | RO                                | RO                                 | RO                               | RO | RO |
| Reset | 0                             | 0                              | 0                             | 0                              | 0                        | 0  | 0  | 0  | 0                                 | 0                                  | 0                                | 0                                 | 0                                  | 0                                | 0  | 0  |
| Bit   | 15                            | 14                             | 13                            | 12                             | 11                       | 10 | 9  | 8  | 7                                 | 6                                  | 5                                | 4                                 | 3                                  | 2                                | 1  | 0  |
| Name  | cdm1_1_ts_data_afifo_empty    | cdm1_1_ts_data_afifo_full      | cdm1_1_ts_data_afifo_overflow | cdm1_1_ts_data_afifo_underflow | cdm1_1_ts_data_afifo_cnt |    |    |    | cdm1_1_ts_epse_afifo_empty        | cdm1_1_ts_epse_afifo_full          | cdm1_1_ts_epse_afifo_overflow    | cdm1_1_ts_epse_afifo_underflow    | cdm1_1_ts_epse_afifo_cnt           |                                  |    |    |
| Type  | RO                            | RO                             | RO                            | RO                             | RO                       |    |    |    | RO                                | RO                                 | RO                               | RO                                | RO                                 |                                  |    |    |
| Reset | 0                             | 0                              | 0                             | 0                              | 0                        | 0  | 0  | 0  | 0                                 | 0                                  | 0                                | 0                                 | 0                                  | 0                                | 0  | 0  |

| Bit(s) | Name                               | Description                                                           |
|--------|------------------------------------|-----------------------------------------------------------------------|
| 31     | cdm1_1_fs_data_afifo_overflow      | FS Data path Async FIFO in CDM fs_fifo module write when FIFO is full |
| 30     | cdm1_1_fs_data_afifo_underflow     | FS Data path Async FIFO in CDM fs_fifo module read when FIFO is empty |
| 29:24  | cdm1_1_fs_data_afifo_cnt           | CDM fs_fifo Data path Async FIFO count                                |
| 23     | cdm1_1_cdm_rx_info_sof_afifo_full  | CDM FS SOF info Async FIFO full                                       |
| 22     | cdm1_1_cdm_rx_info_sof_afifo_empty | CDM FS SOF info Async FIFO empty                                      |
| 21:20  | cdm1_1_cdm_rx_info_sof_afifo_cnt   | CDM FS SOF info Async FIFO count                                      |
| 19     | cdm1_1_cdm_rx_info_eof_afifo_full  | CDM FS EOF info Async FIFO full                                       |
| 18     | cdm1_1_cdm_rx_info_eof_afifo_empty | CDM FS EOF info Async FIFO empty                                      |
| 17:16  | cdm1_1_cdm_rx_info_eof_afifo_cnt   | CDM FS EOF info Async FIFO count                                      |
| 15     | cdm1_1_ts_data_afifo_empty         | TS Data path Async FIFO in CDM ts_fifo module empty                   |
| 14     | cdm1_1_ts_data_afifo_full          | TS Data path Async FIFO in CDM ts_fifo module full                    |
| 13     | cdm1_1_ts_data_afifo_overflow      | TS Data path Async FIFO in CDM ts_fifo module write when full         |
| 12     | cdm1_1_ts_data_afifo_underflow     | TS Data path Async FIFO in CDM ts_fifo module read when empty         |
| 11:8   | cdm1_1_ts_data_afifo_cnt           | CDM ts_fifo Data path Async FIFO count                                |
| 7      | cdm1_1_ts_epse_afifo_empty         | CDM TS info Async FIFO empty                                          |
| 6      | cdm1_1_ts_epse_afifo_full          | CDM TS info Async FIFO full                                           |
| 5      | cdm1_1_ts_epse_afifo_overflow      | CDM TS info Async FIFO write when full                                |
| 4      | cdm1_1_ts_epse_afifo_underflow     | CDM TS info Async FIFO read when empty                                |
| 3:0    | cdm1_1_ts_epse_afifo_cnt           | CDM TS info Async FIFO count                                          |

**151003F4**      **FE\_CDM2\_FIFO\_DBG1**      **FE\_CDM2\_FIFO\_status\_debug1**      **00000000**

| Bit   | 31                 | 30 | 29 | 28 | 27                    | 26                    | 25                      | 24                    | 23                 | 22 | 21 | 20 | 19                       | 18                      | 17 | 16 |
|-------|--------------------|----|----|----|-----------------------|-----------------------|-------------------------|-----------------------|--------------------|----|----|----|--------------------------|-------------------------|----|----|
| Name  | cdm2_fs_infifo_cnt |    |    |    | cdm2_fs_infifo_rvalid | cdm2_fs_infifo_wvalid | cdm2_fs_outfifor_rvalid | cdm2_fs_outfifowvalid | cdm2_fs_outfif_cnt |    |    |    | cdm2_ts_infifo_cnt       |                         |    |    |
| Type  | RO                 |    |    |    | RO                    | RO                    | RO                      | RO                    | RO                 |    |    |    | RO                       |                         |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0                     | 0                     | 0                       | 0                     | 0                  | 0  | 0  | 0  | 0                        | 0                       | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11                    | 10                    | 9                       | 8                     | 7                  | 6  | 5  | 4  | 3                        | 2                       | 1  | 0  |
| Name  | cdm2_ts_outfif_cnt |    |    |    | cdm2_ts_infifo_rvalid | cdm2_ts_infifo_wvalid | cdm2_ts_outfifor_rvalid | cdm2_ts_outfifowvalid | cdm2_tso_fifo_cnt  |    |    |    | cdm2_fs_data_afifo_empty | cdm2_fs_data_afifo_full |    |    |
| Type  | RO                 |    |    |    | RO                    | RO                    | RO                      | RO                    | RO                 |    |    |    | RO                       | RO                      |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0                     | 0                     | 0                       | 0                     | 0                  | 0  | 0  | 0  | 0                        | 0                       | 0  | 0  |

| Bit(s) | Name                     | Description                                         |
|--------|--------------------------|-----------------------------------------------------|
| 31:28  | cdm2_fs_infifo_cnt       | CDM FS parser infifo count                          |
| 27     | cdm2_fs_infifo_rvalid    | CDM FS parser infifo read valid                     |
| 26     | cdm2_fs_infifo_wvalid    | CDM FS parser infifo write valid                    |
| 25     | cdm2_fs_outfifor_rvalid  | CDM FS parser outfifo read valid                    |
| 24     | cdm2_fs_outfifowvalid    | CDM FS parser outfifo write valid                   |
| 23:20  | cdm2_fs_outfif_cnt       | CDM FS parser outfifo count                         |
| 19:16  | cdm2_ts_infifo_cnt       | CDM TS parser infifo count                          |
| 15:12  | cdm2_ts_outfif_cnt       | CDM TS parser outfifo count                         |
| 11     | cdm2_ts_infifo_rvalid    | CDM TS parser infifo read valid                     |
| 10     | cdm2_ts_infifo_wvalid    | CDM TS parser infifo write valid                    |
| 9      | cdm2_ts_outfifor_rvalid  | CDM TS parser outfifo read valid                    |
| 8      | cdm2_ts_outfifowvalid    | CDM TS parser outfifo write valid                   |
| 7:2    | cdm2_tso_fifo_cnt        | CDM TSO FIFO count                                  |
| 1      | cdm2_fs_data_afifo_empty | FS Data path Async FIFO in CDM fs_fifo module empty |
| 0      | cdm2_fs_data_afifo_full  | FS Data path Async FIFO in CDM fs_fifo module full  |

151003F8 FE\_CDM2\_FIFO\_DBG2 FE\_CDM2\_FIFO\_status\_degug2 00000000

| Bit   | 31                          | 30                           | 29                          | 28                           | 27                     | 26 | 25 | 24 | 23                              | 22                               | 21                             | 20                              | 19                               | 18                             | 17 | 16 |
|-------|-----------------------------|------------------------------|-----------------------------|------------------------------|------------------------|----|----|----|---------------------------------|----------------------------------|--------------------------------|---------------------------------|----------------------------------|--------------------------------|----|----|
| Name  | cdm2_fs_data_afifo_overflow | cdm2_fs_data_afifo_underflow | cdm2_fs_data_afifo_cnt      |                              |                        |    |    |    | cdm2_cdm_rx_info_sof_afifo_full | cdm2_cdm_rx_info_sof_afifo_empty | cdm2_cdm_rx_info_sof_afifo_cnt | cdm2_cdm_rx_info_eof_afifo_full | cdm2_cdm_rx_info_eof_afifo_empty | cdm2_cdm_rx_info_eof_afifo_cnt |    |    |
| Type  | RO                          | RO                           | RO                          |                              |                        |    |    |    | RO                              | RO                               | RO                             | RO                              | RO                               | RO                             | RO | RO |
| Reset | 0                           | 0                            | 0                           | 0                            | 0                      | 0  | 0  | 0  | 0                               | 0                                | 0                              | 0                               | 0                                | 0                              | 0  | 0  |
| Bit   | 15                          | 14                           | 13                          | 12                           | 11                     | 10 | 9  | 8  | 7                               | 6                                | 5                              | 4                               | 3                                | 2                              | 1  | 0  |
| Name  | cdm2_ts_data_afifo_empty    | cdm2_ts_data_afifo_full      | cdm2_ts_data_afifo_overflow | cdm2_ts_data_afifo_underflow | cdm2_ts_data_afifo_cnt |    |    |    | cdm2_ts_epse_afifo_empty        | cdm2_ts_epse_afifo_full          | cdm2_ts_epse_afifo_overflow    | cdm2_ts_epse_afifo_underflow    | cdm2_ts_epse_afifo_cnt           |                                |    |    |
| Type  | RO                          | RO                           | RO                          | RO                           | RO                     |    |    |    | RO                              | RO                               | RO                             | RO                              | RO                               |                                |    |    |
| Reset | 0                           | 0                            | 0                           | 0                            | 0                      | 0  | 0  | 0  | 0                               | 0                                | 0                              | 0                               | 0                                | 0                              | 0  | 0  |

| Bit(s) | Name                             | Description                                                           |
|--------|----------------------------------|-----------------------------------------------------------------------|
| 31     | cdm2_fs_data_afifo_overflow      | FS Data path Async FIFO in CDM fs_fifo module write when FIFO is full |
| 30     | cdm2_fs_data_afifo_underflow     | FS Data path Async FIFO in CDM fs_fifo module read when FIFO is empty |
| 29:24  | cdm2_fs_data_afifo_cnt           | CDM fs_fifo Data path Async FIFO count                                |
| 23     | cdm2_cdm_rx_info_sof_afifo_full  | CDM FS SOF info Async FIFO full                                       |
| 22     | cdm2_cdm_rx_info_sof_afifo_empty | CDM FS SOF info Async FIFO empty                                      |
| 21:20  | cdm2_cdm_rx_info_sof_afifo_cnt   | CDM FS SOF info Async FIFO count                                      |
| 19     | cdm2_cdm_rx_info_eof_afifo_full  | CDM FS EOF info Async FIFO full                                       |
| 18     | cdm2_cdm_rx_info_eof_afifo_empty | CDM FS EOF info Async FIFO empty                                      |
| 17:16  | cdm2_cdm_rx_info_eof_afifo_cnt   | CDM FS EOF info Async FIFO count                                      |
| 15     | cdm2_ts_data_afifo_empty         | TS Data path Async FIFO in CDM ts_fifo module empty                   |
| 14     | cdm2_ts_data_afifo_full          | TS Data path Async FIFO in CDM ts_fifo module full                    |
| 13     | cdm2_ts_data_afifo_overflow      | TS Data path Async FIFO in CDM ts_fifo module write when full         |
| 12     | cdm2_ts_data_afifo_underflow     | TS Data path Async FIFO in CDM ts_fifo module read when empty         |
| 11:8   | cdm2_ts_data_afifo_cnt           | CDM ts_fifo Data path Async FIFO count                                |
| 7      | cdm2_ts_epse_afifo_empty         | CDM TS info Async FIFO empty                                          |
| 6      | cdm2_ts_epse_afifo_full          | CDM TS info Async FIFO full                                           |
| 5      | cdm2_ts_epse_afifo_overflow      | CDM TS info Async FIFO write when full                                |
| 4      | cdm2_ts_epse_afifo_underflow     | CDM TS info Async FIFO read when empty                                |
| 3:0    | cdm2_ts_epse_afifo_cnt           | CDM TS info Async FIFO count                                          |

15100400      CDMP\_IG\_CTRL      CDM ingress control      81000000

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17     | 16 |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|
| Name  | CDM_TPID |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |
| Reset | 1        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0      | 0  |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1      | 0  |
| Name  |          |    |    |    |    |    |    |    |    |    |    |    |    |    | MD_CDM |    |
| Type  |          |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     |    |
| Reset |          |    |    |    |    |    |    |    |    |    |    |    |    |    | 0      |    |

| Bit(s) | Name     | Description                                                                                                                               |
|--------|----------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | CDM_TPID | Inserted VLAN TPID                                                                                                                        |
| 1      | MD_CDM   | <p>To indicate whether the CDM is connected to MDMA</p> <p>0: The CDM is not connected to MDMA</p> <p>1: The CDM is connected to MDMA</p> |



15100404      **CDMP EG\_CTRL**      **CDM egress control**      00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22                           | 21           | 20 | 19           | 18 | 17 | 16       |
|-------|----|----|----|----|----|----|----|----|-------------|------------------------------|--------------|----|--------------|----|----|----------|
| Name  |    |    |    |    |    |    |    |    |             |                              |              |    |              |    |    |          |
| Type  |    |    |    |    |    |    |    |    |             |                              |              |    |              |    |    |          |
| Reset |    |    |    |    |    |    |    |    |             |                              |              |    |              |    |    |          |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6                            | 5            | 4  | 3            | 2  | 1  | 0        |
| Name  |    |    |    |    |    |    |    |    | DIS_TSO_SUM | fs_parser_l3_ignore_wait_emp | TACK2RING_ID |    | TACK2RING_EN |    |    | UNTAG_EN |
| Type  |    |    |    |    |    |    |    |    | RW          | RW                           | RW           |    | RW           |    |    | RW       |
| Reset |    |    |    |    |    |    |    |    | 0           | 0                            | 0            | 0  | 0            | 0  |    | 0        |

| Bit(s) | Name                         | Description                                                                                                                                                                                                                                        |
|--------|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7      | DIS_TSO_SUM                  | <b>Disable TSO, IP/TCP/UDP checksum generation on CDM port, not matter whether DMAD enable it.</b><br><br>0: TSO/CHKSUM control from DMAD<br><br>1: Disable TSO/CHKSUM                                                                             |
| 6      | fs_parser_l3_ignore_wait_emp | <b>safety for fs_parser to generate the EOF signal</b><br><br>0: fs_parser use wait_emp state to generate the EOF signal.<br><br>1: fs_parser not use wait_emp state to generate the EOF signal.                                                   |
| 5:4    | TACK2RING_ID                 | <b>Force mode ring selection of TCP ACK to dedicate Rx Ring function</b><br><br>0: Ring 0<br><br>1: Ring 1<br><br>2: Ring 2<br><br>3: Ring 3                                                                                                       |
| 3:2    | TACK2RING_EN                 | <b>Enable TCP ACK to dedicate Rx Ring function</b><br><br>2'b00: Disable<br><br>2'b10: Disable<br><br>2'b01: Enable force mode (select ring according to control register)<br><br>2'b11: Enable PSE mode (select ring according to PSE assignment) |
| 0      | UNTAG_EN                     | <b>VLAN un-tag</b><br><br>Un-tag the egress packets which are transmitted from CDM to CPU<br><br>0: Disable<br><br>1: The first 4-byte VLAN tag after Source Address will be untagged                                                              |

15100408      CDMP\_PPE\_GEN      CDM PPPoE generation      00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|
| Name  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PPP_INS |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| Name  | SESS_ID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       |

| Bit(s) | Name    | Description            |
|--------|---------|------------------------|
| 16     | PPP_INS | PPPoE Header Insertion |
| 15:0   | SESS_ID | PPPoE Session ID       |

**15100500 GDM1 IG\_CTRL GDM ingress control C0717777**

| Bit   | 31         | 30 | 29 | 28 | 27    | 26 | 25      | 24      | 23    | 22        | 21        | 20        | 19        | 18 | 17 | 16       |
|-------|------------|----|----|----|-------|----|---------|---------|-------|-----------|-----------|-----------|-----------|----|----|----------|
| Name  | L3_MAX_LEN |    |    |    |       |    | INSV_EN | STAG_EN |       | GDM_ICSEN | GDM_TCSEN | GDM_UCSEN | DROP_256B |    |    | STRP_CRC |
| Type  | RW         |    |    |    |       |    | RW      | RW      |       | RW        | RW        | RW        | RW        |    |    | RW       |
| Reset | 1          | 1  | 0  | 0  |       |    | 0       | 0       |       | 1         | 1         | 1         | 0         |    |    | 1        |
| Bit   | 15         | 14 | 13 | 12 | 11    | 10 | 9       | 8       | 7     | 6         | 5         | 4         | 3         | 2  | 1  | 0        |
| Name  | MYMAC_DP   |    |    |    | BC_DP |    |         |         | MC_DP |           |           |           | UN_DP     |    |    |          |
| Type  | RW         |    |    |    | RW    |    |         |         | RW    |           |           |           | RW        |    |    |          |
| Reset | 0          | 1  | 1  | 1  | 0     | 1  | 1       | 1       | 0     | 1         | 1         | 1         | 0         | 1  | 1  | 1        |

| Bit(s) | Name       | Description                                                                                                                                                                                                  |
|--------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | L3_MAX_LEN | <b>maximum L3 length allowed = {L3_MAX_LEN,10'b0}</b>                                                                                                                                                        |
| 25     | INSV_EN    | <b>VLAN insertion</b><br>Insert Port VID on the received packets on the corresponding GDM port.<br>0: Disable<br>1: Insert 4-byte VLAN tag after Source Address                                              |
| 24     | STAG_EN    | <b>Special tag indication</b><br>Indicate that the received packet is carrying the special tag from GDM port.<br>0: No special tag inserted.<br>1: The first 2-byte after Source Address is the special tag. |
| 22     | GDM_ICSEN  | <b>IPv4 header checksum error drop</b><br>0: checksum error status reported on RX descriptor (IP4F)<br>1: checksum error packet will be dropped                                                              |
| 21     | GDM_TCSEN  | <b>TCP checksum error drop</b><br>0: checksum error status reported on RX descriptor (L4F)<br>1: checksum error packet will be dropped                                                                       |
| 20     | GDM_UCSEN  | <b>UDP checksum error drop</b><br>0: checksum error status reported on RX descriptor (L4F)<br>1: checksum error packet will be dropped                                                                       |
| 19     | DROP_256B  | <b>A special mode to drop packets with payload &gt; 256 bytes</b><br>0: Drop packets according to the standard Ethernet frame length limitation.<br>1: Drop packets with payload > 256 bytes                 |
| 16     | STRP_CRC   | <b>GDM RX CRC Stripping</b><br>1'b: Disable GDM RX CRC stripping                                                                                                                                             |

| Bit(s) | Name     | Description                             |
|--------|----------|-----------------------------------------|
|        |          | 1'b1: Enable GDM RX CRC stripping       |
| 15:12  | MYMAC_DP | <b>MY_MAC frames destination port</b>   |
|        |          | 4'b0000: ADMA                           |
|        |          | 4'b0001: GDM1                           |
|        |          | 4'b0010: GDM2                           |
|        |          | 4'b0011: PPE0                           |
|        |          | 4'b0100: PPE1                           |
|        |          | 4'b0101: QDMA                           |
|        |          | 4'b0110: Reserved                       |
|        |          | 4'b0111: Discard                        |
|        |          | 4'b1000: WDMA0                          |
|        |          | 4'b1001: WDMA1                          |
|        |          | 4'b1010: MDMA                           |
|        |          | 4'b1011: EDMA0                          |
|        |          | 4'b1100: EDMA1                          |
|        |          | 4'b1101: WDMA2                          |
|        |          | 4'b1110: EDMA2                          |
| 11:8   | BC_DP    | <b>Broadcast frame destination port</b> |
|        |          | 4'b0000: ADMA                           |
|        |          | 4'b0001: GDM1                           |
|        |          | 4'b0010: GDM2                           |
|        |          | 4'b0011: PPE0                           |
|        |          | 4'b0100: PPE1                           |
|        |          | 4'b0101: QDMA                           |
|        |          | 4'b0110: Reserved                       |
|        |          | 4'b0111: Discard                        |
|        |          | 4'b1000: WDMA0                          |
|        |          | 4'b1001: WDMA1                          |
|        |          | 4'b1010: MDMA                           |
|        |          | 4'b1011: EDMA0                          |
|        |          | 4'b1100: EDMA1                          |

| Bit(s) | Name  | Description                             |
|--------|-------|-----------------------------------------|
| 7:4    | MC_DP | 4'b1101: WDMA2                          |
|        |       | 4'b1110: EDMA2                          |
|        |       | <b>Multicast frame destination port</b> |
|        |       | 4'b0000: ADMA                           |
|        |       | 4'b0001: GDM1                           |
|        |       | 4'b0010: GDM2                           |
|        |       | 4'b0011: PPE0                           |
|        |       | 4'b0100: PPE1                           |
|        |       | 4'b0101: QDMA                           |
|        |       | 4'b0110: Reserved                       |
|        |       | 4'b0111: Discard                        |
|        |       | 4'b1000: WDMA0                          |
|        |       | 4'b1001: WDMA1                          |
|        |       | 4'b1010: MDMA                           |
|        |       | 4'b1011: EDMA0                          |
|        |       | 4'b1100: EDMA1                          |
|        |       | 4'b1101: WDMA2                          |
|        |       | 4'b1110: EDMA2                          |
| 3:0    | UN_DP | <b>Other frame destination port</b>     |
|        |       | 4'b0000: ADMA                           |
|        |       | 4'b0001: GDM1                           |
|        |       | 4'b0010: GDM2                           |
|        |       | 4'b0011: PPE0                           |
|        |       | 4'b0100: PPE1                           |
|        |       | 4'b0101: QDMA                           |
|        |       | 4'b0110: Reserved                       |
|        |       | 4'b0111: Discard                        |
|        |       | 4'b1000: WDMA0                          |
|        |       | 4'b1001: WDMA1                          |
|        |       | 4'b1010: MDMA                           |
|        |       | 4'b1011: EDMA0                          |

| Bit(s) | Name | Description    |
|--------|------|----------------|
|        |      | 4'b1100: EDMA1 |
|        |      | 4'b1101: WDMA2 |
|        |      | 4'b1110: EDMA2 |

15100504      **GDM1 EG\_CTRL**      **GDM egress control**      00000000

| Bit   | 31       | 30       | 29      | 28      | 27 | 26 | 25 | 24      | 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----------|---------|---------|----|----|----|---------|---------|----|----|----|----|----|----|----|
| Name  | XGDM_SEL | UNTAG_EN | DIS_PAD | DIS_CRC |    |    |    | SHPR_EN | BK_SIZE |    |    |    |    |    |    |    |
| Type  | RW       | RW       | RW      | RW      |    |    |    | RW      | RW      |    |    |    |    |    |    |    |
| Reset | 0        | 0        | 0       | 0       |    |    |    | 0       | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15       | 14       | 13      | 12      | 11 | 10 | 9  | 8       | 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TK_TICK  |          | TK_RATE |         |    |    |    |         |         |    |    |    |    |    |    |    |
| Type  | RW       |          | RW      |         |    |    |    |         |         |    |    |    |    |    |    |    |
| Reset | 0        |          | 0       | 0       | 0  | 0  | 0  | 0       | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name     | Description                                                                                                                                                                     |
|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | XGDM_SEL | <b>GDM path selection for 10G Ethernet</b><br><br>0: GDM path<br><br>1: XGDM path                                                                                               |
| 30     | UNTAG_EN | <b>VLAN un-tag</b><br><br>Un-tag the egress packets which are transmitted from GDM.<br><br>0: Disable<br><br>1: The first 4-byte VLAN tag after Source Address will be untagged |
| 29     | DIS_PAD  | <b>GMAC TX padding function</b><br><br>1'b0: Enable GMAC TX padding<br><br>1'b1: Disable GMAC TX padding                                                                        |
| 28     | DIS_CRC  | <b>GMAC TX CRC generation</b><br><br>1'b0: Enable GMAC TX CRC generation<br><br>1'b1: Disable GMAC TX CRC generation                                                            |
| 24     | SHPR_EN  | <b>GDM output shaper enable</b><br><br>1'b0: Disable<br><br>1'b1: Enable                                                                                                        |
| 23:16  | BK_SIZE  | <b>GDM output shaper bucket size.</b><br><br>This unit is 1K-byte                                                                                                               |
| 15     | TK_TICK  | <b>GDM shaper token period</b><br><br>1'b0: GDM shaper adds token every 1ms<br><br>1'b1: GDM shaper adds token every 20us                                                       |
| 13:0   | TK_RATE  | <b>GDM output shaper token rate</b><br><br>The unit is 8 bytes/ms or 8 bytes/20us according to TK_TICK.                                                                         |

**15100508      GDM1\_MAC\_LSB      GDM MY\_MAC address LSB      00000000**

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | MAC_ADR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAC_ADR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description           |
|--------|---------|-----------------------|
| 31:0   | MAC_ADR | MY_MAC Address [31:0] |

**1510050C      GDM1\_MAC\_MSB      GDM MY\_MAC address MSB      00000000**

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAC_ADR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description            |
|--------|---------|------------------------|
| 15:0   | MAC_ADR | MY_MAC Address [47:32] |



15100510      **GDM1\_VLAN\_GEN**      GDM VLAN generation      81000000

| Bit   | 31       | 30 | 29 | 28      | 27      | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----|----|---------|---------|----|----|----|----|----|----|----|----|----|----|----|
| Name  | GDM_TPID |    |    |         |         |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    |         |         |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1        | 0  | 0  | 0       | 0       | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15       | 14 | 13 | 12      | 11      | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | GDM_PRI  |    |    | GDM_CFI | GDM_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    | RW      | RW      |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0        | 0  | 0  | 0       | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name     | Description        |
|--------|----------|--------------------|
| 31:16  | GDM_TPID | Inserted VLAN TPID |
| 15:13  | GDM_PRI  | Inserted PRI       |
| 12     | GDM_CFI  | Inserted CFI       |
| 11:0   | GDM_VID  | Inserted VLAN ID   |

15100520 GDM1 DOS CFG 0 GDM DOS configuration 0 00000000

| Bit   | 31                        | 30                   | 29                        | 28                     | 27             | 26             | 25 | 24 | 23                         | 22                    | 21                         | 20                         | 19                 | 18                 | 17 | 16 |
|-------|---------------------------|----------------------|---------------------------|------------------------|----------------|----------------|----|----|----------------------------|-----------------------|----------------------------|----------------------------|--------------------|--------------------|----|----|
| Name  | SPD_2P5G_MODE             | ICMP_AND_TOS_EQ_ZERO | MY_MAC_CHECK              |                        |                |                |    |    | TCP_DROP_INTERRUPT_STATUS  | TCP_RATE_LIMITER_RST  | TCP_DROP_INTERRUPT_ENABLE  | TCP_SYN_PACKET_DROP_ENABLE | TCP_SYN_LIMIT_MODE | TCP_SYN_LIMIT_UNIT |    |    |
| Type  | RW                        | RW                   | RW                        |                        |                |                |    |    | W1C                        | RW                    | RW                         | RW                         | RW                 | RW                 |    |    |
| Reset | 0                         | 0                    | 0                         |                        |                |                |    |    | 0                          | 0                     | 0                          | 0                          | 0                  | 0                  | 0  | 0  |
| Bit   | 15                        | 14                   | 13                        | 12                     | 11             | 10             | 9  | 8  | 7                          | 6                     | 5                          | 4                          | 3                  | 2                  | 1  | 0  |
| Name  | UDP_DROP_INTERRUPT_STATUS | UDP_RATE_LIMITER_RST | UDP_DROP_INTERRUPT_ENABLE | UDP_PACKET_DROP_ENABLE | UDP_LIMIT_MODE | UDP_LIMIT_UNIT |    |    | ICMP_DROP_INTERRUPT_STATUS | ICMP_RATE_LIMITER_RST | ICMP_DROP_INTERRUPT_ENABLE | ICMP_PACKET_DROP_ENABLE    | ICMP_LIMIT_MODE    | ICMP_LIMIT_UNIT    |    |    |
| Type  | W1C                       | RW                   | RW                        | RW                     | RW             | RW             |    |    | W1C                        | RW                    | RW                         | RW                         | RW                 | RW                 |    |    |
| Reset | 0                         | 0                    | 0                         | 0                      | 0              | 0              | 0  | 0  | 0                          | 0                     | 0                          | 0                          | 0                  | 0                  | 0  | 0  |

| Bit(s) | Name                      | Description                                                                                                                                                                                                                                                                                                               |
|--------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | SPD_2P5G_MODE             | <p><b>Only apply "_LIMIT_2P5G" Setting for DoS Rate Limitation (Don't care about link speed change)</b></p> <p>1'b0: Disable</p> <p>1'b1: Enable</p>                                                                                                                                                                      |
| 30     | ICMP_AND_TOS_EQ_ZERO      | <p><b>IPv4 ICMP Packet Recognition Control</b></p> <p>1'b0: Ignore TOS field of IPv4 header, only check PROTOCOL field equal to 1 to regard as IPv4 ICMP packet</p> <p>1'b1: It will also check TOS field equal to 0 besides PROTOCOL field equal to 1</p>                                                                |
| 29     | MY_MAC_CHECK              | <p><b>MY MAC Address Check Control</b></p> <p>1'b0: Ignore DA checking of incoming packet that involve in rate limit mechanism directly</p> <p>1'b1: It will check DA of incoming packet whether equals MY_MAC address, if YES, given packet will involve in rate limit mechanism otherwise pass this packet directly</p> |
| 23     | TCP_DROP_INTERRUPT_STATUS | <p><b>TCP Packet Drop Interrupt Event Status</b></p> <p>1'b0: No interrupt</p> <p>1'b1: Interrupt event trigger</p>                                                                                                                                                                                                       |
| 22     | TCP_RATE_LIMITER_RST      | <p><b>TCP Rate Limiter Reset Control</b></p> <p>1'b0: Reset asserted</p> <p>1'b1: Reset de-asserted</p>                                                                                                                                                                                                                   |
| 21     | TCP_DROP_INTERRUPT_EN     | <p><b>TCP Packet Drop Interrupt Event Control</b></p> <p>1'b0: Disable interrupt event to final interrupt</p> <p>1'b1: Enable interrupt event to final interrupt</p>                                                                                                                                                      |
| 20     | TCP_SYN_PACKET_DROP_EN    | <p><b>TCP SYN Packet Drop Control when Reaching Rate Limitation</b></p>                                                                                                                                                                                                                                                   |

| Bit(s) | Name                 | Description                                                  |
|--------|----------------------|--------------------------------------------------------------|
|        |                      | 1'b0: No packet drop                                         |
|        |                      | 1'b1: Packet drop for following TCP SYN packet               |
| 19     | TCP_SYN_LIMIT_MODE   | <b>TCP SYN Rate Limitation Mode</b>                          |
|        |                      | 1'b0: Packet-based (1 second period)                         |
|        |                      | 1'b1: Rate-based                                             |
| 18:16  | TCP_SYN_LIMIT_UNIT   | <b>Unit of TCP SYN Rate Limitation</b>                       |
|        |                      | 3'b000: 64 packets or 64 Kbps                                |
|        |                      | 3'b001: 256 packets or 256 Kbps                              |
|        |                      | 3'b010: 1 K packets or 1 Mbps                                |
|        |                      | 3'b011: 4 K packets or 4 Mbps                                |
|        |                      | 3'b100: 16 K packets or 16 Mbps                              |
|        |                      | 3'b101: 64K packets or 64 Mbps                               |
|        |                      | 3'b110: 256K packets or 256 Mbps                             |
|        |                      | 3'b111: 1M packets or 1 Gbps                                 |
| 15     | UDP_DROP_INT_STATUS  | <b>UDP Packet Drop Interrupt Event Status</b>                |
|        |                      | 1'b0: No interrupt                                           |
|        |                      | 1'b1: Interrupt event trigger                                |
| 14     | UDP_RATE_LIMITER_RST | <b>UDP Rate Limiter Reset Control</b>                        |
|        |                      | 1'b0: Reset asserted                                         |
|        |                      | 1'b1: Reset de-asserted                                      |
| 13     | UDP_DROP_INT_EN      | <b>UDP Packet Drop Interrupt Event Control</b>               |
|        |                      | 1'b0: Disable interrupt event to final interrupt             |
|        |                      | 1'b1: Enable interrupt event to final interrupt              |
| 12     | UDP_PKT_DROP_EN      | <b>UDP Packet Drop Control when Reaching Rate Limitation</b> |
|        |                      | 1'b0: No packet drop                                         |
|        |                      | 1'b1: Packet drop for following UDP packet                   |
| 11     | UDP_LIMIT_MODE       | <b>UDP Rate Limitation Mode</b>                              |
|        |                      | 1'b0: Packet-based (1 second period)                         |
|        |                      | 1'b1: Rate-based                                             |
| 10:8   | UDP_LIMIT_UNIT       | <b>Unit of UDP Rate Limitation</b>                           |
|        |                      | 3'b000: 64 packets or 64 Kbps                                |
|        |                      | 3'b001: 256 packets or 256 Kbps                              |

| Bit(s) | Name                  | Description                                                   |
|--------|-----------------------|---------------------------------------------------------------|
|        |                       | 3'b010: 1 K packets or 1 Mbps                                 |
|        |                       | 3'b011: 4 K packets or 4 Mbps                                 |
|        |                       | 3'b100: 16 K packets or 16 Mbps                               |
|        |                       | 3'b101: 64K packets or 64 Mbps                                |
|        |                       | 3'b110: 256K packets or 256 Mbps                              |
|        |                       | 3'b111: 1M packets or 1 Gbps                                  |
| 7      | ICMP_DROP_INT_STATUS  | <b>ICMP Packet Drop Interrupt Event Status</b>                |
|        |                       | 1'b0: No interrupt                                            |
|        |                       | 1'b1: Interrupt event trigger                                 |
| 6      | ICMP_RATE_LIMITER_RST | <b>ICMP Rate Limiter Reset Control</b>                        |
|        |                       | 1'b0: Reset asserted                                          |
|        |                       | 1'b1: Reset de-asserted                                       |
| 5      | ICMP_DROP_INT_EN      | <b>ICMP Packet Drop Interrupt Event Control</b>               |
|        |                       | 1'b0: Disable interrupt event to final interrupt              |
|        |                       | 1'b1: Enable interrupt event to final interrupt               |
| 4      | ICMP_PKT_DROP_EN      | <b>ICMP Packet Drop Control when Reaching Rate Limitation</b> |
|        |                       | 1'b0: No packet drop                                          |
|        |                       | 1'b1: Packet drop for following ICMP packet                   |
| 3      | ICMP_LIMIT_MODE       | <b>ICMP Rate Limitation Mode</b>                              |
|        |                       | 1'b0: Packet-based (1 second period)                          |
|        |                       | 1'b1: Rate-based                                              |
| 2:0    | ICMP_LIMIT_UNIT       | <b>Unit of ICMP Rate Limitation</b>                           |
|        |                       | 3'b000: 64 packets or 64 Kbps                                 |
|        |                       | 3'b001: 256 packets or 256 Kbps                               |
|        |                       | 3'b010: 1 K packets or 1 Mbps                                 |
|        |                       | 3'b011: 4 K packets or 4 Mbps                                 |
|        |                       | 3'b100: 16 K packets or 16 Mbps                               |
|        |                       | 3'b101: 64K packets or 64 Mbps                                |
|        |                       | 3'b110: 256K packets or 256 Mbps                              |
|        |                       | 3'b111: 1M packets or 1 Gbps                                  |

15100524      **GDM1 DOS CFG 1**      **GDM DOS configuration 1**      00000000

| Bit          | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|--------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | TCP_SYN_LIMIT_2P5G |    |    |    |    |    |    |    | TCP_SYN_LIMIT_1G  |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | TCP_SYN_LIMIT_100M |    |    |    |    |    |    |    | TCP_SYN_LIMIT_10M |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                                                     |
|--------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | TCP_SYN_LIMIT_2P5G | <b>SGMII+ 2500Mbps or USXGMII 10Gbps TCP_SYN Rate Limit Control</b><br>The TCP_SYN rate limit<br>8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps<br>8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps   |
| 23:16  | TCP_SYN_LIMIT_1G   | <b>SGMII 1000Mbps or USXGMII 5Gbps TCP_SYN Rate Limit Control</b><br>The TCP_SYN rate limit<br>8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps<br>8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps     |
| 15:8   | TCP_SYN_LIMIT_100M | <b>SGMII 100Mbps or USXGMII 2.5Gbps TCP_SYN Rate Limit Control</b><br>The TCP_SYN rate limit<br>8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps<br>8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps    |
| 7:0    | TCP_SYN_LIMIT_10M  | <b>SGMII 10Mbps or USXGMII 1Gbps below TCP_SYN Rate Limit Control</b><br>The TCP_SYN rate limit<br>8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps<br>8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps |

15100528      **GDM1 DOS CFG 2**      **GDM DOS configuration 2**      00000000

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| <b>Name</b>  | UDP_LIMIT_2P5G |    |    |    |    |    |    |    | UDP_LIMIT_1G  |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW            |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | UDP_LIMIT_100M |    |    |    |    |    |    |    | UDP_LIMIT_10M |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW            |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                                                                                                     |
|--------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | UDP_LIMIT_2P5G | <b>SGMII+ 2500Mbps or USXGMII 10Gbps UDP Rate Limit Control</b><br>The UDP rate limit<br>8'h0: (0* UDP_LIMIT_UNIT) packets or bps<br>8'h1: (1* UDP_LIMIT_UNIT) packets or bps   |
| 23:16  | UDP_LIMIT_1G   | <b>SGMII 1000Mbps or USXGMII 5Gbps UDP Rate Limit Control</b><br>The UDP rate limit<br>8'h0: (0* UDP_LIMIT_UNIT) packets or bps<br>8'h1: (1* UDP_LIMIT_UNIT) packets or bps     |
| 15:8   | UDP_LIMIT_100M | <b>SGMII 100Mbps or USXGMII 2.5Gbps UDP Rate Limit Control</b><br>The UDP rate limit<br>8'h0: (0* UDP_LIMIT_UNIT) packets or bps<br>8'h1: (1* UDP_LIMIT_UNIT) packets or bps    |
| 7:0    | UDP_LIMIT_10M  | <b>SGMII 10Mbps or USXGMII 1Gbps below UDP Rate Limit Control</b><br>The UDP rate limit<br>8'h0: (0* UDP_LIMIT_UNIT) packets or bps<br>8'h1: (1* UDP_LIMIT_UNIT) packets or bps |

1510052C      **GDM1 DOS CFG 3**      **GDM DOS configuration 3**      00000000

| Bit          | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | ICMP_LIMIT_2P5G |    |    |    |    |    |    |    | ICMP_LIMIT_1G  |    |    |    |    |    |    |    |
| <b>Type</b>  | RW              |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | ICMP_LIMIT_100M |    |    |    |    |    |    |    | ICMP_LIMIT_10M |    |    |    |    |    |    |    |
| <b>Type</b>  | RW              |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                         |
|--------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | ICMP_LIMIT_2P5G | <b>SGMII+ 2500Mbps or USXGMII 10Gbps ICMP Rate Limit Control</b><br>The ICMP rate limit<br>8'h0: (0* ICMP_LIMIT_UNIT) packets or bps<br>8'h1: (1* ICMP_LIMIT_UNIT) packets or bps   |
| 23:16  | ICMP_LIMIT_1G   | <b>SGMII 1000Mbps or USXGMII 5Gbps ICMP Rate Limit Control</b><br>The ICMP rate limit<br>8'h0: (0* ICMP_LIMIT_UNIT) packets or bps<br>8'h1: (1* ICMP_LIMIT_UNIT) packets or bps     |
| 15:8   | ICMP_LIMIT_100M | <b>SGMII 100Mbps or USXGMII 2.5Gbps ICMP Rate Limit Control</b><br>The ICMP rate limit<br>8'h0: (0* ICMP_LIMIT_UNIT) packets or bps<br>8'h1: (1* ICMP_LIMIT_UNIT) packets or bps    |
| 7:0    | ICMP_LIMIT_10M  | <b>SGMII 10Mbps or USXGMII 1Gbps below ICMP Rate Limit Control</b><br>The ICMP rate limit<br>8'h0: (0* ICMP_LIMIT_UNIT) packets or bps<br>8'h1: (1* ICMP_LIMIT_UNIT) packets or bps |

**15100540**      **GDM3 IG\_CTRL**      **GDM ingress control**      **C0717777**

| Bit   | 31         | 30 | 29 | 28 | 27    | 26 | 25      | 24      | 23    | 22        | 21        | 20        | 19        | 18 | 17 | 16       |
|-------|------------|----|----|----|-------|----|---------|---------|-------|-----------|-----------|-----------|-----------|----|----|----------|
| Name  | L3_MAX_LEN |    |    |    |       |    | INSV_EN | STAG_EN |       | GDM_ICSEN | GDM_TCSEN | GDM_UCSEN | DROP_256B |    |    | STRP_CRC |
| Type  | RW         |    |    |    |       |    | RW      | RW      |       | RW        | RW        | RW        | RW        |    |    | RW       |
| Reset | 1          | 1  | 0  | 0  |       |    | 0       | 0       |       | 1         | 1         | 1         | 0         |    |    | 1        |
| Bit   | 15         | 14 | 13 | 12 | 11    | 10 | 9       | 8       | 7     | 6         | 5         | 4         | 3         | 2  | 1  | 0        |
| Name  | MYMAC_DP   |    |    |    | BC_DP |    |         |         | MC_DP |           |           |           | UN_DP     |    |    |          |
| Type  | RW         |    |    |    | RW    |    |         |         | RW    |           |           |           | RW        |    |    |          |
| Reset | 0          | 1  | 1  | 1  | 0     | 1  | 1       | 1       | 0     | 1         | 1         | 1         | 0         | 1  | 1  | 1        |

| Bit(s) | Name       | Description                                                                                                                                                                                                              |
|--------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | L3_MAX_LEN | <b>maximum L3 length allowed = {L3_MAX_LEN,10'b0}</b>                                                                                                                                                                    |
| 25     | INSV_EN    | <b>VLAN insertion</b><br><br>Insert Port VID on the received packets on the corresponding GDM port.<br><br>0: Disable<br><br>1: Insert 4-byte VLAN tag after Source Address                                              |
| 24     | STAG_EN    | <b>Special tag indication</b><br><br>Indicate that the received packet is carrying the special tag from GDM port.<br><br>0: No special tag inserted.<br><br>1: The first 2-byte after Source Address is the special tag. |
| 22     | GDM_ICSEN  | <b>IPv4 header checksum error drop</b><br><br>0: checksum error status reported on RX descriptor (IP4F)<br><br>1: checksum error packet will be dropped                                                                  |
| 21     | GDM_TCSEN  | <b>TCP checksum error drop</b><br><br>0: checksum error status reported on RX descriptor (L4F)<br><br>1: checksum error packet will be dropped                                                                           |
| 20     | GDM_UCSEN  | <b>UDP checksum error drop</b><br><br>0: checksum error status reported on RX descriptor (L4F)<br><br>1: checksum error packet will be dropped                                                                           |
| 19     | DROP_256B  | <b>A special mode to drop packets with payload &gt; 256 bytes</b><br><br>0: Drop packets according to the standard Ethernet frame length limitation.<br><br>1: Drop packets with payload > 256 bytes                     |
| 16     | STRP_CRC   | <b>GDM RX CRC Stripping</b><br><br>1'b: Disable GDM RX CRC stripping                                                                                                                                                     |



| Bit(s) | Name     | Description                             |
|--------|----------|-----------------------------------------|
|        |          | 1'b1: Enable GDM RX CRC stripping       |
| 15:12  | MYMAC_DP | <b>MY_MAC frames destination port</b>   |
|        |          | 4'b0000: ADMA                           |
|        |          | 4'b0001: GDM1                           |
|        |          | 4'b0010: GDM2                           |
|        |          | 4'b0011: PPE0                           |
|        |          | 4'b0100: PPE1                           |
|        |          | 4'b0101: QDMA                           |
|        |          | 4'b0110: Reserved                       |
|        |          | 4'b0111: Discard                        |
|        |          | 4'b1000: WDMA0                          |
|        |          | 4'b1001: WDMA1                          |
|        |          | 4'b1010: MDMA                           |
|        |          | 4'b1011: EDMA0                          |
|        |          | 4'b1100: EDMA1                          |
|        |          | 4'b1101: WDMA2                          |
|        |          | 4'b1110: EDMA2                          |
| 11:8   | BC_DP    | <b>Broadcast frame destination port</b> |
|        |          | 4'b0000: ADMA                           |
|        |          | 4'b0001: GDM1                           |
|        |          | 4'b0010: GDM2                           |
|        |          | 4'b0011: PPE0                           |
|        |          | 4'b0100: PPE1                           |
|        |          | 4'b0101: QDMA                           |
|        |          | 4'b0110: Reserved                       |
|        |          | 4'b0111: Discard                        |
|        |          | 4'b1000: WDMA0                          |
|        |          | 4'b1001: WDMA1                          |
|        |          | 4'b1010: MDMA                           |
|        |          | 4'b1011: EDMA0                          |
|        |          | 4'b1100: EDMA1                          |

| Bit(s) | Name  | Description                             |
|--------|-------|-----------------------------------------|
| 7:4    | MC_DP | 4'b1101: WDMA2                          |
|        |       | 4'b1110: EDMA2                          |
|        |       | <b>Multicast frame destination port</b> |
|        |       | 4'b0000: ADMA                           |
|        |       | 4'b0001: GDM1                           |
|        |       | 4'b0010: GDM2                           |
|        |       | 4'b0011: PPE0                           |
|        |       | 4'b0100: PPE1                           |
|        |       | 4'b0101: QDMA                           |
|        |       | 4'b0110: Reserved                       |
|        |       | 4'b0111: Discard                        |
|        |       | 4'b1000: WDMA0                          |
|        |       | 4'b1001: WDMA1                          |
|        |       | 4'b1010: MDMA                           |
|        |       | 4'b1011: EDMA0                          |
|        |       | 4'b1100: EDMA1                          |
|        |       | 4'b1101: WDMA2                          |
|        |       | 4'b1110: EDMA2                          |
| 3:0    | UN_DP | <b>Other frame destination port</b>     |
|        |       | 4'b0000: ADMA                           |
|        |       | 4'b0001: GDM1                           |
|        |       | 4'b0010: GDM2                           |
|        |       | 4'b0011: PPE0                           |
|        |       | 4'b0100: PPE1                           |
|        |       | 4'b0101: QDMA                           |
|        |       | 4'b0110: Reserved                       |
|        |       | 4'b0111: Discard                        |
|        |       | 4'b1000: WDMA0                          |
|        |       | 4'b1001: WDMA1                          |
|        |       | 4'b1010: MDMA                           |
|        |       | 4'b1011: EDMA0                          |

| Bit(s) | Name | Description    |
|--------|------|----------------|
|        |      | 4'b1100: EDMA1 |
|        |      | 4'b1101: WDMA2 |
|        |      | 4'b1110: EDMA2 |

15100544      **GDM3 EG\_CTRL**      **GDM egress control**      00000000

| Bit   | 31       | 30       | 29      | 28      | 27 | 26 | 25 | 24      | 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----------|---------|---------|----|----|----|---------|---------|----|----|----|----|----|----|----|
| Name  | XGDM_SEL | UNTAG_EN | DIS_PAD | DIS_CRC |    |    |    | SHPR_EN | BK_SIZE |    |    |    |    |    |    |    |
| Type  | RW       | RW       | RW      | RW      |    |    |    | RW      | RW      |    |    |    |    |    |    |    |
| Reset | 0        | 0        | 0       | 0       |    |    |    | 0       | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15       | 14       | 13      | 12      | 11 | 10 | 9  | 8       | 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TK_TICK  |          | TK_RATE |         |    |    |    |         |         |    |    |    |    |    |    |    |
| Type  | RW       |          | RW      |         |    |    |    |         |         |    |    |    |    |    |    |    |
| Reset | 0        |          | 0       | 0       | 0  | 0  | 0  | 0       | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name     | Description                                                                                                                                                                     |
|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | XGDM_SEL | <b>GDM path selection for 10G Ethernet</b><br><br>0: GDM path<br><br>1: XGDM path                                                                                               |
| 30     | UNTAG_EN | <b>VLAN un-tag</b><br><br>Un-tag the egress packets which are transmitted from GDM.<br><br>0: Disable<br><br>1: The first 4-byte VLAN tag after Source Address will be untagged |
| 29     | DIS_PAD  | <b>GMAC TX padding function</b><br><br>1'b0: Enable GMAC TX padding<br><br>1'b1: Disable GMAC TX padding                                                                        |
| 28     | DIS_CRC  | <b>GMAC TX CRC generation</b><br><br>1'b0: Enable GMAC TX CRC generation<br><br>1'b1: Disable GMAC TX CRC generation                                                            |
| 24     | SHPR_EN  | <b>GDM output shaper enable</b><br><br>1'b0: Disable<br><br>1'b1: Enable                                                                                                        |
| 23:16  | BK_SIZE  | <b>GDM output shaper bucket size.</b><br><br>This unit is 1K-byte                                                                                                               |
| 15     | TK_TICK  | <b>GDM shaper token period</b><br><br>1'b0: GDM shaper adds token every 1ms<br><br>1'b1: GDM shaper adds token every 20us                                                       |
| 13:0   | TK_RATE  | <b>GDM output shaper token rate</b><br><br>The unit is 8 bytes/ms or 8 bytes/20us according to TK_TICK.                                                                         |

15100548 GDM3 MAC LSB GDM MY\_MAC address LSB 00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | MAC_ADR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAC_ADR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description           |
|--------|---------|-----------------------|
| 31:0   | MAC_ADR | MY_MAC Address [31:0] |

1510054C GDM3 MAC MSB GDM MY\_MAC address MSB 00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAC_ADR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description            |
|--------|---------|------------------------|
| 15:0   | MAC_ADR | MY_MAC Address [47:32] |

15100550      **GDM3\_VLAN\_GEN**      GDM VLAN generation      81000000

| Bit   | 31       | 30 | 29 | 28      | 27      | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----|----|---------|---------|----|----|----|----|----|----|----|----|----|----|----|
| Name  | GDM_TPID |    |    |         |         |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    |         |         |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1        | 0  | 0  | 0       | 0       | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15       | 14 | 13 | 12      | 11      | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | GDM_PRI  |    |    | GDM_CFI | GDM_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    | RW      | RW      |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0        | 0  | 0  | 0       | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name     | Description        |
|--------|----------|--------------------|
| 31:16  | GDM_TPID | Inserted VLAN TPID |
| 15:13  | GDM_PRI  | Inserted PRI       |
| 12     | GDM_CFI  | Inserted CFI       |
| 11:0   | GDM_VID  | Inserted VLAN ID   |

15100560 GDM3 DOS CFG 0 GDM DOS configuration 0 00000000

| Bit   | 31                        | 30                   | 29                        | 28                     | 27             | 26             | 25 | 24 | 23                         | 22                    | 21                         | 20                         | 19                 | 18                 | 17 | 16 |
|-------|---------------------------|----------------------|---------------------------|------------------------|----------------|----------------|----|----|----------------------------|-----------------------|----------------------------|----------------------------|--------------------|--------------------|----|----|
| Name  | SPD_2P5G_MODE             | ICMP_AND_TOS_EQ_ZERO | MY_MAC_CHECK              |                        |                |                |    |    | TCP_DROP_INTERRUPT_STATUS  | TCP_RATE_LIMITER_RST  | TCP_DROP_INTERRUPT_ENABLE  | TCP_SYN_PACKET_DROP_ENABLE | TCP_SYN_LIMIT_MODE | TCP_SYN_LIMIT_UNIT |    |    |
| Type  | RW                        | RW                   | RW                        |                        |                |                |    |    | W1C                        | RW                    | RW                         | RW                         | RW                 | RW                 |    |    |
| Reset | 0                         | 0                    | 0                         |                        |                |                |    |    | 0                          | 0                     | 0                          | 0                          | 0                  | 0                  | 0  | 0  |
| Bit   | 15                        | 14                   | 13                        | 12                     | 11             | 10             | 9  | 8  | 7                          | 6                     | 5                          | 4                          | 3                  | 2                  | 1  | 0  |
| Name  | UDP_DROP_INTERRUPT_STATUS | UDP_RATE_LIMITER_RST | UDP_DROP_INTERRUPT_ENABLE | UDP_PACKET_DROP_ENABLE | UDP_LIMIT_MODE | UDP_LIMIT_UNIT |    |    | ICMP_DROP_INTERRUPT_STATUS | ICMP_RATE_LIMITER_RST | ICMP_DROP_INTERRUPT_ENABLE | ICMP_PACKET_DROP_ENABLE    | ICMP_LIMIT_MODE    | ICMP_LIMIT_UNIT    |    |    |
| Type  | W1C                       | RW                   | RW                        | RW                     | RW             | RW             |    |    | W1C                        | RW                    | RW                         | RW                         | RW                 | RW                 |    |    |
| Reset | 0                         | 0                    | 0                         | 0                      | 0              | 0              | 0  | 0  | 0                          | 0                     | 0                          | 0                          | 0                  | 0                  | 0  | 0  |

| Bit(s) | Name                      | Description                                                                                                                                                                                                                                                                                                               |
|--------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | SPD_2P5G_MODE             | <p><b>Only apply "_LIMIT_2P5G" Setting for DoS Rate Limitation (Don't care about link speed change)</b></p> <p>1'b0: Disable</p> <p>1'b1: Enable</p>                                                                                                                                                                      |
| 30     | ICMP_AND_TOS_EQ_ZERO      | <p><b>IPv4 ICMP Packet Recognition Control</b></p> <p>1'b0: Ignore TOS field of IPv4 header, only check PROTOCOL field equal to 1 to regard as IPv4 ICMP packet</p> <p>1'b1: It will also check TOS field equal to 0 besides PROTOCOL field equal to 1</p>                                                                |
| 29     | MY_MAC_CHECK              | <p><b>MY MAC Address Check Control</b></p> <p>1'b0: Ignore DA checking of incoming packet that involve in rate limit mechanism directly</p> <p>1'b1: It will check DA of incoming packet whether equals MY_MAC address, if YES, given packet will involve in rate limit mechanism otherwise pass this packet directly</p> |
| 23     | TCP_DROP_INTERRUPT_STATUS | <p><b>TCP Packet Drop Interrupt Event Status</b></p> <p>1'b0: No interrupt</p> <p>1'b1: Interrupt event trigger</p>                                                                                                                                                                                                       |
| 22     | TCP_RATE_LIMITER_RST      | <p><b>TCP Rate Limiter Reset Control</b></p> <p>1'b0: Reset asserted</p> <p>1'b1: Reset de-asserted</p>                                                                                                                                                                                                                   |
| 21     | TCP_DROP_INTERRUPT_EN     | <p><b>TCP Packet Drop Interrupt Event Control</b></p> <p>1'b0: Disable interrupt event to final interrupt</p> <p>1'b1: Enable interrupt event to final interrupt</p>                                                                                                                                                      |
| 20     | TCP_SYN_PACKET_DROP_EN    | <p><b>TCP SYN Packet Drop Control when Reaching Rate Limitation</b></p>                                                                                                                                                                                                                                                   |

| Bit(s) | Name                 | Description                                                  |
|--------|----------------------|--------------------------------------------------------------|
|        |                      | 1'b0: No packet drop                                         |
|        |                      | 1'b1: Packet drop for following TCP SYN packet               |
| 19     | TCP_SYN_LIMIT_MODE   | <b>TCP SYN Rate Limitation Mode</b>                          |
|        |                      | 1'b0: Packet-based (1 second period)                         |
|        |                      | 1'b1: Rate-based                                             |
| 18:16  | TCP_SYN_LIMIT_UNIT   | <b>Unit of TCP SYN Rate Limitation</b>                       |
|        |                      | 3'b000: 64 packets or 64 Kbps                                |
|        |                      | 3'b001: 256 packets or 256 Kbps                              |
|        |                      | 3'b010: 1 K packets or 1 Mbps                                |
|        |                      | 3'b011: 4 K packets or 4 Mbps                                |
|        |                      | 3'b100: 16 K packets or 16 Mbps                              |
|        |                      | 3'b101: 64K packets or 64 Mbps                               |
|        |                      | 3'b110: 256K packets or 256 Mbps                             |
|        |                      | 3'b111: 1M packets or 1 Gbps                                 |
| 15     | UDP_DROP_INT_STATUS  | <b>UDP Packet Drop Interrupt Event Status</b>                |
|        |                      | 1'b0: No interrupt                                           |
|        |                      | 1'b1: Interrupt event trigger                                |
| 14     | UDP_RATE_LIMITER_RST | <b>UDP Rate Limiter Reset Control</b>                        |
|        |                      | 1'b0: Reset asserted                                         |
|        |                      | 1'b1: Reset de-asserted                                      |
| 13     | UDP_DROP_INT_EN      | <b>UDP Packet Drop Interrupt Event Control</b>               |
|        |                      | 1'b0: Disable interrupt event to final interrupt             |
|        |                      | 1'b1: Enable interrupt event to final interrupt              |
| 12     | UDP_PKT_DROP_EN      | <b>UDP Packet Drop Control when Reaching Rate Limitation</b> |
|        |                      | 1'b0: No packet drop                                         |
|        |                      | 1'b1: Packet drop for following UDP packet                   |
| 11     | UDP_LIMIT_MODE       | <b>UDP Rate Limitation Mode</b>                              |
|        |                      | 1'b0: Packet-based (1 second period)                         |
|        |                      | 1'b1: Rate-based                                             |
| 10:8   | UDP_LIMIT_UNIT       | <b>Unit of UDP Rate Limitation</b>                           |
|        |                      | 3'b000: 64 packets or 64 Kbps                                |
|        |                      | 3'b001: 256 packets or 256 Kbps                              |



| Bit(s) | Name                  | Description                                                   |
|--------|-----------------------|---------------------------------------------------------------|
|        |                       | 3'b010: 1 K packets or 1 Mbps                                 |
|        |                       | 3'b011: 4 K packets or 4 Mbps                                 |
|        |                       | 3'b100: 16 K packets or 16 Mbps                               |
|        |                       | 3'b101: 64K packets or 64 Mbps                                |
|        |                       | 3'b110: 256K packets or 256 Mbps                              |
|        |                       | 3'b111: 1M packets or 1 Gbps                                  |
| 7      | ICMP_DROP_INT_STATUS  | <b>ICMP Packet Drop Interrupt Event Status</b>                |
|        |                       | 1'b0: No interrupt                                            |
|        |                       | 1'b1: Interrupt event trigger                                 |
| 6      | ICMP_RATE_LIMITER_RST | <b>ICMP Rate Limiter Reset Control</b>                        |
|        |                       | 1'b0: Reset asserted                                          |
|        |                       | 1'b1: Reset de-asserted                                       |
| 5      | ICMP_DROP_INT_EN      | <b>ICMP Packet Drop Interrupt Event Control</b>               |
|        |                       | 1'b0: Disable interrupt event to final interrupt              |
|        |                       | 1'b1: Enable interrupt event to final interrupt               |
| 4      | ICMP_PKT_DROP_EN      | <b>ICMP Packet Drop Control when Reaching Rate Limitation</b> |
|        |                       | 1'b0: No packet drop                                          |
|        |                       | 1'b1: Packet drop for following ICMP packet                   |
| 3      | ICMP_LIMIT_MODE       | <b>ICMP Rate Limitation Mode</b>                              |
|        |                       | 1'b0: Packet-based (1 second period)                          |
|        |                       | 1'b1: Rate-based                                              |
| 2:0    | ICMP_LIMIT_UNIT       | <b>Unit of ICMP Rate Limitation</b>                           |
|        |                       | 3'b000: 64 packets or 64 Kbps                                 |
|        |                       | 3'b001: 256 packets or 256 Kbps                               |
|        |                       | 3'b010: 1 K packets or 1 Mbps                                 |
|        |                       | 3'b011: 4 K packets or 4 Mbps                                 |
|        |                       | 3'b100: 16 K packets or 16 Mbps                               |
|        |                       | 3'b101: 64K packets or 64 Mbps                                |
|        |                       | 3'b110: 256K packets or 256 Mbps                              |
|        |                       | 3'b111: 1M packets or 1 Gbps                                  |

15100564      **GDM3 DOS CFG 1**      **GDM DOS configuration 1**      00000000

| Bit          | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|--------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | TCP_SYN_LIMIT_2P5G |    |    |    |    |    |    |    | TCP_SYN_LIMIT_1G  |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | TCP_SYN_LIMIT_100M |    |    |    |    |    |    |    | TCP_SYN_LIMIT_10M |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                                                     |
|--------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | TCP_SYN_LIMIT_2P5G | <b>SGMII+ 2500Mbps or USXGMII 10Gbps TCP_SYN Rate Limit Control</b><br>The TCP_SYN rate limit<br>8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps<br>8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps   |
| 23:16  | TCP_SYN_LIMIT_1G   | <b>SGMII 1000Mbps or USXGMII 5Gbps TCP_SYN Rate Limit Control</b><br>The TCP_SYN rate limit<br>8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps<br>8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps     |
| 15:8   | TCP_SYN_LIMIT_100M | <b>SGMII 100Mbps or USXGMII 2.5Gbps TCP_SYN Rate Limit Control</b><br>The TCP_SYN rate limit<br>8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps<br>8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps    |
| 7:0    | TCP_SYN_LIMIT_10M  | <b>SGMII 10Mbps or USXGMII 1Gbps below TCP_SYN Rate Limit Control</b><br>The TCP_SYN rate limit<br>8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps<br>8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps |

15100568      **GDM3 DOS CFG 2**      **GDM DOS configuration 2**      00000000

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| <b>Name</b>  | UDP_LIMIT_2P5G |    |    |    |    |    |    |    | UDP_LIMIT_1G  |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW            |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | UDP_LIMIT_100M |    |    |    |    |    |    |    | UDP_LIMIT_10M |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW            |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                                                                                                     |
|--------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | UDP_LIMIT_2P5G | <b>SGMII+ 2500Mbps or USXGMII 10Gbps UDP Rate Limit Control</b><br>The UDP rate limit<br>8'h0: (0* UDP_LIMIT_UNIT) packets or bps<br>8'h1: (1* UDP_LIMIT_UNIT) packets or bps   |
| 23:16  | UDP_LIMIT_1G   | <b>SGMII 1000Mbps or USXGMII 5Gbps UDP Rate Limit Control</b><br>The UDP rate limit<br>8'h0: (0* UDP_LIMIT_UNIT) packets or bps<br>8'h1: (1* UDP_LIMIT_UNIT) packets or bps     |
| 15:8   | UDP_LIMIT_100M | <b>SGMII 100Mbps or USXGMII 2.5Gbps UDP Rate Limit Control</b><br>The UDP rate limit<br>8'h0: (0* UDP_LIMIT_UNIT) packets or bps<br>8'h1: (1* UDP_LIMIT_UNIT) packets or bps    |
| 7:0    | UDP_LIMIT_10M  | <b>SGMII 10Mbps or USXGMII 1Gbps below UDP Rate Limit Control</b><br>The UDP rate limit<br>8'h0: (0* UDP_LIMIT_UNIT) packets or bps<br>8'h1: (1* UDP_LIMIT_UNIT) packets or bps |

1510056C      **GDM3 DOS CFG 3**      **GDM DOS configuration 3**      00000000

| Bit          | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | ICMP_LIMIT_2P5G |    |    |    |    |    |    |    | ICMP_LIMIT_1G  |    |    |    |    |    |    |    |
| <b>Type</b>  | RW              |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | ICMP_LIMIT_100M |    |    |    |    |    |    |    | ICMP_LIMIT_10M |    |    |    |    |    |    |    |
| <b>Type</b>  | RW              |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                         |
|--------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | ICMP_LIMIT_2P5G | <b>SGMII+ 2500Mbps or USXGMII 10Gbps ICMP Rate Limit Control</b><br>The ICMP rate limit<br>8'h0: (0* ICMP_LIMIT_UNIT) packets or bps<br>8'h1: (1* ICMP_LIMIT_UNIT) packets or bps   |
| 23:16  | ICMP_LIMIT_1G   | <b>SGMII 1000Mbps or USXGMII 5Gbps ICMP Rate Limit Control</b><br>The ICMP rate limit<br>8'h0: (0* ICMP_LIMIT_UNIT) packets or bps<br>8'h1: (1* ICMP_LIMIT_UNIT) packets or bps     |
| 15:8   | ICMP_LIMIT_100M | <b>SGMII 100Mbps or USXGMII 2.5Gbps ICMP Rate Limit Control</b><br>The ICMP rate limit<br>8'h0: (0* ICMP_LIMIT_UNIT) packets or bps<br>8'h1: (1* ICMP_LIMIT_UNIT) packets or bps    |
| 7:0    | ICMP_LIMIT_10M  | <b>SGMII 10Mbps or USXGMII 1Gbps below ICMP Rate Limit Control</b><br>The ICMP rate limit<br>8'h0: (0* ICMP_LIMIT_UNIT) packets or bps<br>8'h1: (1* ICMP_LIMIT_UNIT) packets or bps |

**15100600      GLO\_MEM\_CFG      Global memory configurations      00000000**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18          | 17         | 16             |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|------------|----------------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |             |            |                |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |             |            |                |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |             |            |                |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2           | 1          | 0              |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    | CDM_CDRT_EN | GDM_CLS_EN | GDM_DIPFLTR_EN |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    | RW          | RW         | RW             |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    | 0           | 0          | 0              |

| Bit(s) | Name           | Description                                                              |
|--------|----------------|--------------------------------------------------------------------------|
| 2      | CDM_CDRT_EN    | <b>CDM CDR template memory enable</b><br><br>0: Disable<br><br>1: Enable |
| 1      | GDM_CLS_EN     | <b>CDM CLS CAM enable</b><br><br>0: Disable<br><br>1: Enable             |
| 0      | GDM_DIPFLTR_EN | <b>CDM DIP filter CAM enable</b><br><br>0: Disable<br><br>1: Enable      |

**15100604 GLO\_MEM\_CTRL Global memory interface control 00000000**

| Bit          | 31   | 30 | 29    | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
|--------------|------|----|-------|----|----|----|----|----|----|----|----|----|------|----|----|----|
| <b>Name</b>  | CMD  |    | INDEX |    |    |    |    |    |    |    |    |    | ADDR |    |    |    |
| <b>Type</b>  | RW   |    | RW    |    |    |    |    |    |    |    |    |    | RW   |    |    |    |
| <b>Reset</b> | 0    | 0  | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0    | 0  | 0  | 0  |
| <b>Bit</b>   | 15   | 14 | 13    | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| <b>Name</b>  | ADDR |    |       |    |    |    |    |    |    |    |    |    |      |    |    |    |
| <b>Type</b>  | RW   |    |       |    |    |    |    |    |    |    |    |    |      |    |    |    |
| <b>Reset</b> | 0    | 0  | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0    | 0  | 0  | 0  |

| Bit(s) | Name  | Description                                                                                                                                                                                                                              |
|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30  | CMD   | <b>2'h0: none, 2'h1: write, 2'h2: read</b><br><br>Set command, back to none when done<br><br>For writing, write DATA0~DATA7 first, then issue write command<br><br>For reading, issue read command first, then get DATA0~DATA7 when done |
| 29:20  | INDEX | <b>Memory index</b><br><br>0: CLS<br><br>1: CDM CDR                                                                                                                                                                                      |
| 19:0   | ADDR  | <b>Memory address</b>                                                                                                                                                                                                                    |

**15100608 GLO\_MEM\_DATA0 Global memory data 0 00000000**

| Bit          | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| <b>Bit</b>   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description         |
|--------|------|---------------------|
| 31:0   | DATA | <b>Data 031:000</b> |

**1510060C      GLO\_MEM\_DATA1      Global memory data 1      00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description  |
|--------|------|--------------|
| 31:0   | DATA | Data 063:032 |

**15100610      GLO\_MEM\_DATA2      Global memory data 2      00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description  |
|--------|------|--------------|
| 31:0   | DATA | Data 095:064 |

**15100614      GLO\_MEM\_DATA3      Global memory data 3      00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description  |
|--------|------|--------------|
| 31:0   | DATA | Data 127:096 |

**15100618      GLO\_MEM\_DATA4      Global memory data 4      00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description  |
|--------|------|--------------|
| 31:0   | DATA | Data 159:128 |

**1510061C      GLO\_MEM\_DATA5      Global memory data 5      00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description  |
|--------|------|--------------|
| 31:0   | DATA | Data 191:160 |

**15100620      GLO\_MEM\_DATA6      Global memory data 6      00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description  |
|--------|------|--------------|
| 31:0   | DATA | Data 223:192 |



**15100624      GLO\_MEM\_DATA7      Global memory data 7      00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description  |
|--------|------|--------------|
| 31:0   | DATA | Data 255:224 |

**15100628      GLO\_MEM\_DATA8      Global memory data 8      00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description  |
|--------|------|--------------|
| 31:0   | DATA | Data 287:256 |

**1510062C      GLO\_MEM\_DATA9      Global memory data 9      00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description  |
|--------|------|--------------|
| 31:0   | DATA | Data 319:288 |

**15100C00      PFC\_CFG\_0      PFC GMAC1 input priority ReMap 0      08040201**

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | GMAC1_IN_PRI_3 |    |    |    |    |    |    |    | GMAC1_IN_PRI_2 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | GMAC1_IN_PRI_1 |    |    |    |    |    |    |    | GMAC1_IN_PRI_0 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name           | Description                                          |
|--------|----------------|------------------------------------------------------|
| 31:24  | GMAC1_IN_PRI_3 | GMAC1 Input Priority Re-Map Selection for Priority 3 |
| 23:16  | GMAC1_IN_PRI_2 | GMAC1 Input Priority Re-Map Selection for Priority 2 |
| 15:8   | GMAC1_IN_PRI_1 | GMAC1 Input Priority Re-Map Selection for Priority 1 |
| 7:0    | GMAC1_IN_PRI_0 | GMAC1 Input Priority Re-Map Selection for Priority 0 |

**15100C04      PFC\_CFG\_1      PFC GMAC1 input priority ReMap 1      80402010**

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | GMAC1_IN_PRI_7 |    |    |    |    |    |    |    | GMAC1_IN_PRI_6 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 1              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 1  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | GMAC1_IN_PRI_5 |    |    |    |    |    |    |    | GMAC1_IN_PRI_4 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                          |
|--------|----------------|------------------------------------------------------|
| 31:24  | GMAC1_IN_PRI_7 | GMAC1 Input Priority Re-Map Selection for Priority 7 |
| 23:16  | GMAC1_IN_PRI_6 | GMAC1 Input Priority Re-Map Selection for Priority 6 |
| 15:8   | GMAC1_IN_PRI_5 | GMAC1 Input Priority Re-Map Selection for Priority 5 |
| 7:0    | GMAC1_IN_PRI_4 | GMAC1 Input Priority Re-Map Selection for Priority 4 |

**15100C08      PFC\_CFG\_2      PFC GMAC2 input priority ReMap 0      08040201**

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | GMAC2_IN_PRI_3 |    |    |    |    |    |    |    | GMAC2_IN_PRI_2 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | GMAC2_IN_PRI_1 |    |    |    |    |    |    |    | GMAC2_IN_PRI_0 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name           | Description                                          |
|--------|----------------|------------------------------------------------------|
| 31:24  | GMAC2_IN_PRI_3 | GMAC2 Input Priority Re-Map Selection for Priority 3 |
| 23:16  | GMAC2_IN_PRI_2 | GMAC2 Input Priority Re-Map Selection for Priority 2 |
| 15:8   | GMAC2_IN_PRI_1 | GMAC2 Input Priority Re-Map Selection for Priority 1 |
| 7:0    | GMAC2_IN_PRI_0 | GMAC2 Input Priority Re-Map Selection for Priority 0 |

**15100C0C      PFC\_CFG\_3      PFC GMAC2 input priority ReMap 1      80402010**

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | GMAC2_IN_PRI_7 |    |    |    |    |    |    |    | GMAC2_IN_PRI_6 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 1              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 1  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | GMAC2_IN_PRI_5 |    |    |    |    |    |    |    | GMAC2_IN_PRI_4 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                          |
|--------|----------------|------------------------------------------------------|
| 31:24  | GMAC2_IN_PRI_7 | GMAC2 Input Priority Re-Map Selection for Priority 7 |
| 23:16  | GMAC2_IN_PRI_6 | GMAC2 Input Priority Re-Map Selection for Priority 6 |
| 15:8   | GMAC2_IN_PRI_5 | GMAC2 Input Priority Re-Map Selection for Priority 5 |
| 7:0    | GMAC2_IN_PRI_4 | GMAC2 Input Priority Re-Map Selection for Priority 4 |

**15100C20      PFC\_CFG\_2\_3      PFC GMAC3 input priority ReMap 0      08040201**

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | GMAC3_IN_PRI_3 |    |    |    |    |    |    |    | GMAC3_IN_PRI_2 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | GMAC3_IN_PRI_1 |    |    |    |    |    |    |    | GMAC3_IN_PRI_0 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name           | Description                                          |
|--------|----------------|------------------------------------------------------|
| 31:24  | GMAC3_IN_PRI_3 | GMAC3 Input Priority Re-Map Selection for Priority 3 |
| 23:16  | GMAC3_IN_PRI_2 | GMAC3 Input Priority Re-Map Selection for Priority 2 |
| 15:8   | GMAC3_IN_PRI_1 | GMAC3 Input Priority Re-Map Selection for Priority 1 |
| 7:0    | GMAC3_IN_PRI_0 | GMAC3 Input Priority Re-Map Selection for Priority 0 |

**15100C24      PFC\_CFG\_3\_3      PFC GMAC3 input priority ReMap 1      80402010**

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | GMAC3_IN_PRI_7 |    |    |    |    |    |    |    | GMAC3_IN_PRI_6 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 1              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 1  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | GMAC3_IN_PRI_5 |    |    |    |    |    |    |    | GMAC3_IN_PRI_4 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                          |
|--------|----------------|------------------------------------------------------|
| 31:24  | GMAC3_IN_PRI_7 | GMAC3 Input Priority Re-Map Selection for Priority 7 |
| 23:16  | GMAC3_IN_PRI_6 | GMAC3 Input Priority Re-Map Selection for Priority 6 |
| 15:8   | GMAC3_IN_PRI_5 | GMAC3 Input Priority Re-Map Selection for Priority 5 |
| 7:0    | GMAC3_IN_PRI_4 | GMAC3 Input Priority Re-Map Selection for Priority 4 |

**15100C60      PFC\_CFG\_5      PFC QDMA input priority ReMap 0      00000000**

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_0_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_0_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                |
|--------|--------------------|------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_0_31_0 | QDMA Input Priority Re-Map Selection for Priority 0 [31:0] |

**15100C64      PFC\_CFG\_6      PFC QDMA input priority ReMap 1      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_0_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_0_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                 |
|--------|---------------------|-------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_0_63_32 | QDMA Input Priority Re-Map Selection for Priority 0 [63:32] |

**15100C68      PFC\_CFG\_7      PFC QDMA input priority ReMap 2      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_0_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_0_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                 |
|--------|---------------------|-------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_0_95_64 | QDMA Input Priority Re-Map Selection for Priority 0 [95:64] |

**15100C6C      PFC\_CFG\_8      PFC QDMA input priority ReMap 3      00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_0_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_0_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                  |
|--------|----------------------|--------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_0_127_96 | QDMA Input Priority Re-Map Selection for Priority 0 [127:96] |

**15100C70      PFC\_CFG\_9      PFC QDMA input priority ReMap 4      00000000**

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_1_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_1_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                |
|--------|--------------------|------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_1_31_0 | QDMA Input Priority Re-Map Selection for Priority 1 [31:0] |

**15100C74      PFC\_CFG\_10      PFC QDMA input priority ReMap 5      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_1_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_1_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                 |
|--------|---------------------|-------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_1_63_32 | QDMA Input Priority Re-Map Selection for Priority 1 [63:32] |

**15100C78      PFC\_CFG\_11      PFC QDMA input priority ReMap 6      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_1_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_1_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                 |
|--------|---------------------|-------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_1_95_64 | QDMA Input Priority Re-Map Selection for Priority 1 [95:64] |

**15100C7C      PFC\_CFG\_12      PFC QDMA input priority ReMap 7      00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_1_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_1_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                  |
|--------|----------------------|--------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_1_127_96 | QDMA Input Priority Re-Map Selection for Priority 1 [127:96] |

**15100C80      PFC\_CFG\_13      PFC QDMA input priority ReMap 8      00000000**

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_2_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_2_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                |
|--------|--------------------|------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_2_31_0 | QDMA Input Priority Re-Map Selection for Priority 2 [31:0] |

**15100C84      PFC\_CFG\_14      PFC QDMA input priority ReMap 9      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_2_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_2_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                 |
|--------|---------------------|-------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_2_63_32 | QDMA Input Priority Re-Map Selection for Priority 2 [63:32] |

**15100C88      PFC\_CFG\_15      PFC QDMA input priority ReMap 10      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_2_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_2_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                 |
|--------|---------------------|-------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_2_95_64 | QDMA Input Priority Re-Map Selection for Priority 2 [95:64] |

**15100C8C      PFC\_CFG\_16      PFC QDMA input priority ReMap 11      00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_2_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_2_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                  |
|--------|----------------------|--------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_2_127_96 | QDMA Input Priority Re-Map Selection for Priority 2 [127:96] |



**15100C90      PFC\_CFG\_17      PFC QDMA input priority ReMap 12      00000000**

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_3_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_3_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                |
|--------|--------------------|------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_3_31_0 | QDMA Input Priority Re-Map Selection for Priority 3 [31:0] |

**15100C94      PFC\_CFG\_18      PFC QDMA input priority ReMap 13      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_3_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_3_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                 |
|--------|---------------------|-------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_3_63_32 | QDMA Input Priority Re-Map Selection for Priority 3 [63:32] |

**15100C98      PFC\_CFG\_19      PFC QDMA input priority ReMap 14      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_3_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_3_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                 |
|--------|---------------------|-------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_3_95_64 | QDMA Input Priority Re-Map Selection for Priority 3 [95:64] |

**15100C9C      PFC\_CFG\_20      PFC QDMA input priority ReMap 15      00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_3_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_3_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                  |
|--------|----------------------|--------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_3_127_96 | QDMA Input Priority Re-Map Selection for Priority 3 [127:96] |

**15100CA0      PFC\_CFG\_21      PFC QDMA input priority ReMap 16      00000000**

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_4_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_4_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                |
|--------|--------------------|------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_4_31_0 | QDMA Input Priority Re-Map Selection for Priority 4 [31:0] |

**15100CA4      PFC\_CFG\_22      PFC QDMA input priority ReMap 17      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_4_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_4_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                 |
|--------|---------------------|-------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_4_63_32 | QDMA Input Priority Re-Map Selection for Priority 4 [63:32] |

**15100CA8      PFC\_CFG\_23      PFC QDMA input priority ReMap 18      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_4_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_4_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                 |
|--------|---------------------|-------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_4_95_64 | QDMA Input Priority Re-Map Selection for Priority 4 [95:64] |

**15100CAC      PFC\_CFG\_24      PFC QDMA input priority ReMap 19      00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_4_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_4_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                  |
|--------|----------------------|--------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_4_127_96 | QDMA Input Priority Re-Map Selection for Priority 4 [127:96] |

**15100CB0      PFC\_CFG\_25      PFC QDMA input priority ReMap 20      00000000**

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_5_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_5_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                |
|--------|--------------------|------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_5_31_0 | QDMA Input Priority Re-Map Selection for Priority 5 [31:0] |

**15100CB4 PFC\_CFG\_26 PFC QDMA input priority ReMap 21 00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_5_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_5_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                 |
|--------|---------------------|-------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_5_63_32 | QDMA Input Priority Re-Map Selection for Priority 5 [63:32] |

**15100CB8 PFC\_CFG\_27 PFC QDMA input priority ReMap 22 00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_5_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_5_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                 |
|--------|---------------------|-------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_5_95_64 | QDMA Input Priority Re-Map Selection for Priority 5 [95:64] |

**15100CBC PFC\_CFG\_28 PFC QDMA input priority ReMap 23 00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_5_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_5_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                  |
|--------|----------------------|--------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_5_127_96 | QDMA Input Priority Re-Map Selection for Priority 5 [127:96] |

**15100CC0      PFC\_CFG\_29      PFC QDMA input priority ReMap 24      00000000**

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_6_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_6_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                |
|--------|--------------------|------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_6_31_0 | QDMA Input Priority Re-Map Selection for Priority 6 [31:0] |

**15100CC4      PFC\_CFG\_30      PFC QDMA input priority ReMap 25      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_6_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_6_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                 |
|--------|---------------------|-------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_6_63_32 | QDMA Input Priority Re-Map Selection for Priority 6 [63:32] |

**15100CC8      PFC\_CFG\_31      PFC QDMA input priority ReMap 26      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_6_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_6_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                 |
|--------|---------------------|-------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_6_95_64 | QDMA Input Priority Re-Map Selection for Priority 6 [95:64] |

**15100CCC      PFC\_CFG\_32      PFC QDMA input priority ReMap 27      00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_6_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_6_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                  |
|--------|----------------------|--------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_6_127_96 | QDMA Input Priority Re-Map Selection for Priority 6 [127:96] |

**15100CD0      PFC\_CFG\_33      PFC QDMA input priority ReMap 28      00000000**

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_7_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_7_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                |
|--------|--------------------|------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_7_31_0 | QDMA Input Priority Re-Map Selection for Priority 7 [31:0] |

**15100CD4      PFC\_CFG\_34      PFC QDMA input priority ReMap 29      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_7_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_7_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                 |
|--------|---------------------|-------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_7_63_32 | QDMA Input Priority Re-Map Selection for Priority 7 [63:32] |

**15100CD8      PFC\_CFG\_35      PFC QDMA input priority ReMap 30      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_7_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_7_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                 |
|--------|---------------------|-------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_7_95_64 | QDMA Input Priority Re-Map Selection for Priority 7 [95:64] |

**15100CDC      PFC\_CFG\_36      PFC QDMA input priority ReMap 31      00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_IN_PRI_7_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_IN_PRI_7_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                  |
|--------|----------------------|--------------------------------------------------------------|
| 31:0   | QDMA_IN_PRI_7_127_96 | QDMA Input Priority Re-Map Selection for Priority 7 [127:96] |

**15100D60      PFC\_CFG\_37      PFC GMAC1 output priority ReMap 0      08040201**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | GMAC1_OUT_PRI_Q_3 |    |    |    |    |    |    |    | GMAC1_OUT_PRI_Q_2 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | GMAC1_OUT_PRI_Q_1 |    |    |    |    |    |    |    | GMAC1_OUT_PRI_Q_0 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | GMAC1_OUT_PRI_Q_3 | GMAC1 Output Priority Queue 3 Re-Map Selection |
| 23:16  | GMAC1_OUT_PRI_Q_2 | GMAC1 Output Priority Queue 2 Re-Map Selection |
| 15:8   | GMAC1_OUT_PRI_Q_1 | GMAC1 Output Priority Queue 1 Re-Map Selection |
| 7:0    | GMAC1_OUT_PRI_Q_0 | GMAC1 Output Priority Queue 0 Re-Map Selection |

**15100D64      PFC\_CFG\_38      PFC GMAC1 output priority ReMap 1      80402010**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | GMAC1_OUT_PRI_Q_7 |    |    |    |    |    |    |    | GMAC1_OUT_PRI_Q_6 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 1                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 1  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | GMAC1_OUT_PRI_Q_5 |    |    |    |    |    |    |    | GMAC1_OUT_PRI_Q_4 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | GMAC1_OUT_PRI_Q_7 | GMAC1 Output Priority Queue 7 Re-Map Selection |
| 23:16  | GMAC1_OUT_PRI_Q_6 | GMAC1 Output Priority Queue 6 Re-Map Selection |
| 15:8   | GMAC1_OUT_PRI_Q_5 | GMAC1 Output Priority Queue 5 Re-Map Selection |
| 7:0    | GMAC1_OUT_PRI_Q_4 | GMAC1 Output Priority Queue 4 Re-Map Selection |



**15100D68      PFC\_CFG\_39      PFC GMAC2 output priority ReMap 0      08040201**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | GMAC2_OUT_PRI_Q_3 |    |    |    |    |    |    |    | GMAC2_OUT_PRI_Q_2 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | GMAC2_OUT_PRI_Q_1 |    |    |    |    |    |    |    | GMAC2_OUT_PRI_Q_0 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | GMAC2_OUT_PRI_Q_3 | GMAC2 Output Priority Queue 3 Re-Map Selection |
| 23:16  | GMAC2_OUT_PRI_Q_2 | GMAC2 Output Priority Queue 2 Re-Map Selection |
| 15:8   | GMAC2_OUT_PRI_Q_1 | GMAC2 Output Priority Queue 1 Re-Map Selection |
| 7:0    | GMAC2_OUT_PRI_Q_0 | GMAC2 Output Priority Queue 0 Re-Map Selection |

**15100D6C      PFC\_CFG\_40      PFC GMAC2 output priority ReMap 1      80402010**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | GMAC2_OUT_PRI_Q_7 |    |    |    |    |    |    |    | GMAC2_OUT_PRI_Q_6 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 1                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 1  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | GMAC2_OUT_PRI_Q_5 |    |    |    |    |    |    |    | GMAC2_OUT_PRI_Q_4 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | GMAC2_OUT_PRI_Q_7 | GMAC2 Output Priority Queue 7 Re-Map Selection |
| 23:16  | GMAC2_OUT_PRI_Q_6 | GMAC2 Output Priority Queue 6 Re-Map Selection |
| 15:8   | GMAC2_OUT_PRI_Q_5 | GMAC2 Output Priority Queue 5 Re-Map Selection |
| 7:0    | GMAC2_OUT_PRI_Q_4 | GMAC2 Output Priority Queue 4 Re-Map Selection |

**15100D90      PFC\_CFG\_39\_3      PFC GMAC3 output priority ReMap 0      08040201**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | GMAC3_OUT_PRI_Q_3 |    |    |    |    |    |    |    | GMAC3_OUT_PRI_Q_2 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | GMAC3_OUT_PRI_Q_1 |    |    |    |    |    |    |    | GMAC3_OUT_PRI_Q_0 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | GMAC3_OUT_PRI_Q_3 | GMAC3 Output Priority Queue 3 Re-Map Selection |
| 23:16  | GMAC3_OUT_PRI_Q_2 | GMAC3 Output Priority Queue 2 Re-Map Selection |
| 15:8   | GMAC3_OUT_PRI_Q_1 | GMAC3 Output Priority Queue 1 Re-Map Selection |
| 7:0    | GMAC3_OUT_PRI_Q_0 | GMAC3 Output Priority Queue 0 Re-Map Selection |

**15100D94      PFC\_CFG\_40\_3      PFC GMAC3 output priority ReMap 1      80402010**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | GMAC3_OUT_PRI_Q_7 |    |    |    |    |    |    |    | GMAC3_OUT_PRI_Q_6 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 1                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 1  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | GMAC3_OUT_PRI_Q_5 |    |    |    |    |    |    |    | GMAC3_OUT_PRI_Q_4 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | GMAC3_OUT_PRI_Q_7 | GMAC3 Output Priority Queue 7 Re-Map Selection |
| 23:16  | GMAC3_OUT_PRI_Q_6 | GMAC3 Output Priority Queue 6 Re-Map Selection |
| 15:8   | GMAC3_OUT_PRI_Q_5 | GMAC3 Output Priority Queue 5 Re-Map Selection |
| 7:0    | GMAC3_OUT_PRI_Q_4 | GMAC3 Output Priority Queue 4 Re-Map Selection |

**15100DA0      PFC\_CFG\_43      PFC QDMA output priority ReMap 0      00000000**

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|------------------|----|----|----|----|----|----|----|
| Name  | QDMA_OUT_PRI_Q_3 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_2 |    |    |    |    |    |    |    |
| Type  | RW               |    |    |    |    |    |    |    | RW               |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_OUT_PRI_Q_1 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_0 |    |    |    |    |    |    |    |
| Type  | RW               |    |    |    |    |    |    |    | RW               |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                   |
|--------|------------------|-----------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_3 | QDMA Output Priority Queue 3 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_2 | QDMA Output Priority Queue 2 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_1 | QDMA Output Priority Queue 1 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_0 | QDMA Output Priority Queue 0 Re-Map Selection |

**15100DA4      PFC\_CFG\_44      PFC QDMA output priority ReMap 1      00000000**

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|------------------|----|----|----|----|----|----|----|
| Name  | QDMA_OUT_PRI_Q_7 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_6 |    |    |    |    |    |    |    |
| Type  | RW               |    |    |    |    |    |    |    | RW               |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_OUT_PRI_Q_5 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_4 |    |    |    |    |    |    |    |
| Type  | RW               |    |    |    |    |    |    |    | RW               |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                                   |
|--------|------------------|-----------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_7 | QDMA Output Priority Queue 7 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_6 | QDMA Output Priority Queue 6 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_5 | QDMA Output Priority Queue 5 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_4 | QDMA Output Priority Queue 4 Re-Map Selection |

**15100DA8      PFC\_CFG\_45      PFC QDMA output priority ReMap 2      00000000**

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| Name  | QDMA_OUT_PRI_Q_11 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_10 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_OUT_PRI_Q_9  |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_8  |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_11 | QDMA Output Priority Queue 11 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_10 | QDMA Output Priority Queue 10 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_9  | QDMA Output Priority Queue 9 Re-Map Selection  |
| 7:0    | QDMA_OUT_PRI_Q_8  | QDMA Output Priority Queue 8 Re-Map Selection  |

**15100DAC      PFC\_CFG\_46      PFC QDMA output priority ReMap 3      00000000**

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| Name  | QDMA_OUT_PRI_Q_15 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_14 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_OUT_PRI_Q_13 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_12 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_15 | QDMA Output Priority Queue 15 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_14 | QDMA Output Priority Queue 14 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_13 | QDMA Output Priority Queue 13 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_12 | QDMA Output Priority Queue 12 Re-Map Selection |

**15100DB0      PFC\_CFG\_47      PFC QDMA output priority ReMap 4      00000000**

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| Name  | QDMA_OUT_PRI_Q_19 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_18 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_OUT_PRI_Q_17 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_16 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_19 | QDMA Output Priority Queue 19 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_18 | QDMA Output Priority Queue 18 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_17 | QDMA Output Priority Queue 17 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_16 | QDMA Output Priority Queue 16 Re-Map Selection |

**15100DB4      PFC\_CFG\_48      PFC QDMA output priority ReMap 5      00000000**

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| Name  | QDMA_OUT_PRI_Q_23 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_22 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_OUT_PRI_Q_21 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_20 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_23 | QDMA Output Priority Queue 23 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_22 | QDMA Output Priority Queue 22 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_21 | QDMA Output Priority Queue 21 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_20 | QDMA Output Priority Queue 20 Re-Map Selection |

**15100DB8      PFC\_CFG\_49      PFC QDMA output priority ReMap 6      00000000**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_27 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_26 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_25 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_24 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_27 | QDMA Output Priority Queue 27 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_26 | QDMA Output Priority Queue 26 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_25 | QDMA Output Priority Queue 25 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_24 | QDMA Output Priority Queue 24 Re-Map Selection |

**15100DBC      PFC\_CFG\_50      PFC QDMA output priority ReMap 7      00000000**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_31 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_30 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_29 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_28 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_31 | QDMA Output Priority Queue 31 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_30 | QDMA Output Priority Queue 30 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_29 | QDMA Output Priority Queue 29 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_28 | QDMA Output Priority Queue 28 Re-Map Selection |

**15100DC0      PFC\_CFG\_51      PFC QDMA output priority ReMap 8      00000000**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_35 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_34 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_33 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_32 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_35 | QDMA Output Priority Queue 35 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_34 | QDMA Output Priority Queue 34 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_33 | QDMA Output Priority Queue 33 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_32 | QDMA Output Priority Queue 32 Re-Map Selection |

**15100DC4      PFC\_CFG\_52      PFC QDMA output priority ReMap 9      00000000**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_39 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_38 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_37 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_36 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_39 | QDMA Output Priority Queue 39 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_38 | QDMA Output Priority Queue 38 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_37 | QDMA Output Priority Queue 37 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_36 | QDMA Output Priority Queue 36 Re-Map Selection |

**15100DC8      PFC\_CFG\_53      PFC QDMA output priority ReMap 10      00000000**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_43 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_42 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_41 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_40 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_43 | QDMA Output Priority Queue 43 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_42 | QDMA Output Priority Queue 42 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_41 | QDMA Output Priority Queue 41 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_40 | QDMA Output Priority Queue 40 Re-Map Selection |

**15100DCC      PFC\_CFG\_54      PFC QDMA output priority ReMap 11      00000000**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_47 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_46 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_45 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_44 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_47 | QDMA Output Priority Queue 47 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_46 | QDMA Output Priority Queue 46 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_45 | QDMA Output Priority Queue 45 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_44 | QDMA Output Priority Queue 44 Re-Map Selection |



**15100DD0      PFC\_CFG\_55      PFC QDMA output priority ReMap 12      00000000**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_51 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_50 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_49 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_48 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_51 | QDMA Output Priority Queue 51 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_50 | QDMA Output Priority Queue 50 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_49 | QDMA Output Priority Queue 49 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_48 | QDMA Output Priority Queue 48 Re-Map Selection |

**15100DD4      PFC\_CFG\_56      PFC QDMA output priority ReMap 13      00000000**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_55 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_54 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_53 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_52 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_55 | QDMA Output Priority Queue 55 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_54 | QDMA Output Priority Queue 54 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_53 | QDMA Output Priority Queue 53 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_52 | QDMA Output Priority Queue 52 Re-Map Selection |

**15100DD8      PFC\_CFG\_57      PFC QDMA output priority ReMap 14      00000000**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_59 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_58 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_57 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_56 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_59 | QDMA Output Priority Queue 59 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_58 | QDMA Output Priority Queue 58 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_57 | QDMA Output Priority Queue 57 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_56 | QDMA Output Priority Queue 56 Re-Map Selection |

**15100DDC      PFC\_CFG\_58      PFC QDMA output priority ReMap 15      00000000**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_63 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_62 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_61 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_60 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_63 | QDMA Output Priority Queue 63 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_62 | QDMA Output Priority Queue 62 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_61 | QDMA Output Priority Queue 61 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_60 | QDMA Output Priority Queue 60 Re-Map Selection |

**15100DE0      PFC\_CFG\_59      PFC QDMA output priority ReMap 16      00000000**

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| Name  | QDMA_OUT_PRI_Q_67 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_66 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_OUT_PRI_Q_65 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_64 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_67 | QDMA Output Priority Queue 67 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_66 | QDMA Output Priority Queue 66 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_65 | QDMA Output Priority Queue 65 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_64 | QDMA Output Priority Queue 64 Re-Map Selection |

**15100DE4      PFC\_CFG\_60      PFC QDMA output priority ReMap 17      00000000**

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| Name  | QDMA_OUT_PRI_Q_71 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_70 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_OUT_PRI_Q_69 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_68 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_71 | QDMA Output Priority Queue 71 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_70 | QDMA Output Priority Queue 70 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_69 | QDMA Output Priority Queue 69 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_68 | QDMA Output Priority Queue 68 Re-Map Selection |

**15100DE8      PFC\_CFG\_61      PFC QDMA output priority ReMap 18      00000000**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_75 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_74 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_73 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_72 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_75 | QDMA Output Priority Queue 75 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_74 | QDMA Output Priority Queue 74 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_73 | QDMA Output Priority Queue 73 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_72 | QDMA Output Priority Queue 72 Re-Map Selection |

**15100DEC      PFC\_CFG\_62      PFC QDMA output priority ReMap 19      00000000**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_79 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_78 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_77 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_76 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_79 | QDMA Output Priority Queue 79 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_78 | QDMA Output Priority Queue 78 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_77 | QDMA Output Priority Queue 77 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_76 | QDMA Output Priority Queue 76 Re-Map Selection |

**15100DF0      PFC\_CFG\_63      PFC QDMA output priority ReMap 20      00000000**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_83 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_82 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_81 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_80 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_83 | QDMA Output Priority Queue 83 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_82 | QDMA Output Priority Queue 82 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_81 | QDMA Output Priority Queue 81 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_80 | QDMA Output Priority Queue 80 Re-Map Selection |

**15100DF4      PFC\_CFG\_64      PFC QDMA output priority ReMap 21      00000000**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_87 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_86 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_85 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_84 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_87 | QDMA Output Priority Queue 87 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_86 | QDMA Output Priority Queue 86 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_85 | QDMA Output Priority Queue 85 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_84 | QDMA Output Priority Queue 84 Re-Map Selection |

**15100DF8      PFC\_CFG\_65      PFC QDMA output priority ReMap 22      00000000**

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| Name  | QDMA_OUT_PRI_Q_91 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_90 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_OUT_PRI_Q_89 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_88 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_91 | QDMA Output Priority Queue 91 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_90 | QDMA Output Priority Queue 90 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_89 | QDMA Output Priority Queue 89 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_88 | QDMA Output Priority Queue 88 Re-Map Selection |

**15100DFC      PFC\_CFG\_66      PFC QDMA output priority ReMap 23      00000000**

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| Name  | QDMA_OUT_PRI_Q_95 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_94 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_OUT_PRI_Q_93 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_92 |    |    |    |    |    |    |    |
| Type  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_95 | QDMA Output Priority Queue 95 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_94 | QDMA Output Priority Queue 94 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_93 | QDMA Output Priority Queue 93 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_92 | QDMA Output Priority Queue 92 Re-Map Selection |

**15100E00      PFC\_CFG\_67      PFC QDMA output priority ReMap 24      00000000**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_99 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_98 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_97 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_96 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                    |
|--------|-------------------|------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_99 | QDMA Output Priority Queue 99 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_98 | QDMA Output Priority Queue 98 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_97 | QDMA Output Priority Queue 97 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_96 | QDMA Output Priority Queue 96 Re-Map Selection |

**15100E04      PFC\_CFG\_68      PFC QDMA output priority ReMap 25      00000000**

| Bit          | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|--------------------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_103 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_102 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_101 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_100 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                     |
|--------|--------------------|-------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_103 | QDMA Output Priority Queue 103 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_102 | QDMA Output Priority Queue 102 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_101 | QDMA Output Priority Queue 101 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_100 | QDMA Output Priority Queue 100 Re-Map Selection |

**15100E08      PFC\_CFG\_69      PFC QDMA output priority ReMap 26      00000000**

| Bit          | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|--------------------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_107 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_106 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_105 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_104 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                     |
|--------|--------------------|-------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_107 | QDMA Output Priority Queue 107 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_106 | QDMA Output Priority Queue 106 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_105 | QDMA Output Priority Queue 105 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_104 | QDMA Output Priority Queue 104 Re-Map Selection |

**15100E0C      PFC\_CFG\_70      PFC QDMA output priority ReMap 27      00000000**

| Bit          | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|--------------------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_111 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_110 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_109 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_108 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                     |
|--------|--------------------|-------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_111 | QDMA Output Priority Queue 111 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_110 | QDMA Output Priority Queue 110 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_109 | QDMA Output Priority Queue 109 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_108 | QDMA Output Priority Queue 108 Re-Map Selection |



**15100E10      PFC\_CFG\_71      PFC QDMA output priority ReMap 28      00000000**

| Bit          | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|--------------------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_115 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_114 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_113 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_112 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                     |
|--------|--------------------|-------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_115 | QDMA Output Priority Queue 115 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_114 | QDMA Output Priority Queue 114 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_113 | QDMA Output Priority Queue 113 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_112 | QDMA Output Priority Queue 112 Re-Map Selection |

**15100E14      PFC\_CFG\_72      PFC QDMA output priority ReMap 29      00000000**

| Bit          | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|--------------------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_119 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_118 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_117 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_116 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                     |
|--------|--------------------|-------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_119 | QDMA Output Priority Queue 119 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_118 | QDMA Output Priority Queue 118 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_117 | QDMA Output Priority Queue 117 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_116 | QDMA Output Priority Queue 116 Re-Map Selection |

**15100E18      PFC\_CFG\_73      PFC QDMA output priority ReMap 30      00000000**

| Bit          | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|--------------------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_123 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_122 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_121 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_120 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                     |
|--------|--------------------|-------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_123 | QDMA Output Priority Queue 123 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_122 | QDMA Output Priority Queue 122 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_121 | QDMA Output Priority Queue 121 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_120 | QDMA Output Priority Queue 120 Re-Map Selection |

**15100E1C      PFC\_CFG\_74      PFC QDMA output priority ReMap 31      00000000**

| Bit          | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|--------------------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | QDMA_OUT_PRI_Q_127 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_126 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QDMA_OUT_PRI_Q_125 |    |    |    |    |    |    |    | QDMA_OUT_PRI_Q_124 |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                 |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                     |
|--------|--------------------|-------------------------------------------------|
| 31:24  | QDMA_OUT_PRI_Q_127 | QDMA Output Priority Queue 127 Re-Map Selection |
| 23:16  | QDMA_OUT_PRI_Q_126 | QDMA Output Priority Queue 126 Re-Map Selection |
| 15:8   | QDMA_OUT_PRI_Q_125 | QDMA Output Priority Queue 125 Re-Map Selection |
| 7:0    | QDMA_OUT_PRI_Q_124 | QDMA Output Priority Queue 124 Re-Map Selection |

**15100EA0 PFC\_CFG\_75 PFC enable control to GMAC1 00FFFF00**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  |                |    |    |    |    |    |    |    | EN_GMAC3_GMAC1 |    |    |    |    |    |    |    |
| Type  |                |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| Reset |                |    |    |    |    |    |    |    | 1              | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | EN_GMAC2_GMAC1 |    |    |    |    |    |    |    | EN_GMAC1_GMAC1 |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| Reset | 1              | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                        |
|--------|----------------|------------------------------------|
| 23:16  | EN_GMAC3_GMAC1 | Enable Control from GMAC3 to GMAC1 |
| 15:8   | EN_GMAC2_GMAC1 | Enable Control from GMAC2 to GMAC1 |
| 7:0    | EN_GMAC1_GMAC1 | Enable Control from GMAC1 to GMAC1 |

**15100EA4 PFC\_CFG\_76 PFC enable control to GMAC1 000000FF**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    |    |    |    |               |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    |    |    |    |               |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    |    |    |    |               |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    | EN_QDMA_GMAC1 |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    |    |    |    | RW            |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    |    |    |    | 1             | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name          | Description                       |
|--------|---------------|-----------------------------------|
| 7:0    | EN_QDMA_GMAC1 | Enable Control from QDMA to GMAC1 |

**15100EA8 PFC\_CFG\_77 PFC enable control to GMAC2 00FF00FF**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  |                |    |    |    |    |    |    |    | EN_GMAC3_GMAC2 |    |    |    |    |    |    |    |
| Type  |                |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| Reset |                |    |    |    |    |    |    |    | 1              | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | EN_GMAC2_GMAC2 |    |    |    |    |    |    |    | EN_GMAC1_GMAC2 |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1              | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name           | Description                        |
|--------|----------------|------------------------------------|
| 23:16  | EN_GMAC3_GMAC2 | Enable Control from GMAC3 to GMAC2 |
| 15:8   | EN_GMAC2_GMAC2 | Enable Control from GMAC2 to GMAC2 |
| 7:0    | EN_GMAC1_GMAC2 | Enable Control from GMAC1 to GMAC2 |

**15100EAC PFC\_CFG\_78 PFC enable control to GMAC2 000000FF**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    |    |    |    |               |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    |    |    |    |               |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    |    |    |    |               |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    | EN_QDMA_GMAC2 |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    |    |    |    | RW            |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    |    |    |    | 1             | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name          | Description                       |
|--------|---------------|-----------------------------------|
| 7:0    | EN_QDMA_GMAC2 | Enable Control from QDMA to GMAC2 |

**15100EB0 PFC\_CFG\_79 PFC enable control to GMAC3 0000FFFF**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  |                |    |    |    |    |    |    |    | EN_GMAC3_GMAC3 |    |    |    |    |    |    |    |
| Type  |                |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| Reset |                |    |    |    |    |    |    |    | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | EN_GMAC2_GMAC3 |    |    |    |    |    |    |    | EN_GMAC1_GMAC3 |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| Reset | 1              | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1              | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name           | Description                        |
|--------|----------------|------------------------------------|
| 23:16  | EN_GMAC3_GMAC3 | Enable Control from GMAC3 to GMAC3 |
| 15:8   | EN_GMAC2_GMAC3 | Enable Control from GMAC2 to GMAC3 |
| 7:0    | EN_GMAC1_GMAC3 | Enable Control from GMAC1 to GMAC3 |

**15100EB4 PFC\_CFG\_80 PFC enable control to GMAC3 000000FF**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| Name  |    |    |    |    |    |    |    |    |               |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    |    |    |    |               |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    |    |    |    |               |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    | EN_QDMA_GMAC3 |    |    |    |    |    |    |    |
| Type  |    |    |    |    |    |    |    |    | RW            |    |    |    |    |    |    |    |
| Reset |    |    |    |    |    |    |    |    | 1             | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name          | Description                       |
|--------|---------------|-----------------------------------|
| 7:0    | EN_QDMA_GMAC3 | Enable Control from QDMA to GMAC3 |

**15100EC0 PFC\_CFG\_83 PFC enable control to QDMA 00FFFFFF**

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| Name  |               |    |    |    |    |    |    |    | EN_GMAC3_QDMA |    |    |    |    |    |    |    |
| Type  |               |    |    |    |    |    |    |    | RW            |    |    |    |    |    |    |    |
| Reset |               |    |    |    |    |    |    |    | 1             | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | EN_GMAC2_QDMA |    |    |    |    |    |    |    | EN_GMAC1_QDMA |    |    |    |    |    |    |    |
| Type  | RW            |    |    |    |    |    |    |    | RW            |    |    |    |    |    |    |    |
| Reset | 1             | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1             | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name          | Description                       |
|--------|---------------|-----------------------------------|
| 23:16  | EN_GMAC3_QDMA | Enable Control from GMAC3 to QDMA |
| 15:8   | EN_GMAC2_QDMA | Enable Control from GMAC2 to QDMA |
| 7:0    | EN_GMAC1_QDMA | Enable Control from GMAC1 to QDMA |

**15100EF0 PFC\_CFG\_85 PFC debug 0 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  |             |    |    |    |    |    |    |    | DEBUG_GMAC3 |    |    |    |    |    |    |    |
| Type  |             |    |    |    |    |    |    |    | RO          |    |    |    |    |    |    |    |
| Reset |             |    |    |    |    |    |    |    | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DEBUG_GMAC2 |    |    |    |    |    |    |    | DEBUG_GMAC1 |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    | RO          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                  |
|--------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:16  | DEBUG_GMAC3 | <b>Debug for Output Module: GMAC3</b><br><br>This debug is for PFC vector source from MAC/QDMA in central, MAC TX will ignore this event in half duplex mode |
| 15:8   | DEBUG_GMAC2 | <b>Debug for Output Module: GMAC2</b><br><br>This debug is for PFC vector source from MAC/QDMA in central, MAC TX will ignore this event in half duplex mode |
| 7:0    | DEBUG_GMAC1 | <b>Debug for Output Module: GMAC1</b><br><br>This debug is for PFC vector source from MAC/QDMA in central, MAC TX will ignore this event in half duplex mode |

15100EF4      PFC\_CFG\_86      PFC debug 1      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DEBUG_QDMA_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DEBUG_QDMA_31_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                            |
|--------|-----------------|----------------------------------------|
| 31:0   | DEBUG_QDMA_31_0 | Debug for Output Module: QDMA bit 31~0 |

15100EF8      PFC\_CFG\_87      PFC debug 2      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DEBUG_QDMA_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DEBUG_QDMA_63_32 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                             |
|--------|------------------|-----------------------------------------|
| 31:0   | DEBUG_QDMA_63_32 | Debug for Output Module: QDMA bit 63~32 |

15100EFC      PFC\_CFG\_88      PFC debug 3      00000000

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DEBUG_QDMA_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DEBUG_QDMA_95_64 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                             |
|--------|------------------|-----------------------------------------|
| 31:0   | DEBUG_QDMA_95_64 | Debug for Output Module: QDMA bit 95~64 |

15100F00      PFC\_CFG\_89      PFC debug 4      00000000

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DEBUG_QDMA_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DEBUG_QDMA_127_96 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                              |
|--------|-------------------|------------------------------------------|
| 31:0   | DEBUG_QDMA_127_96 | Debug for Output Module: QDMA bit 127~96 |



|          |                     |                      |    |    |                      |                       |    |    |    |    |    |    |          |                          |    |    |
|----------|---------------------|----------------------|----|----|----------------------|-----------------------|----|----|----|----|----|----|----------|--------------------------|----|----|
| 15100F04 | PFC_CFG_90          |                      |    |    | PFC configuration    |                       |    |    |    |    |    |    | 00000000 |                          |    |    |
| Bit      | 31                  | 30                   | 29 | 28 | 27                   | 26                    | 25 | 24 | 23 | 22 | 21 | 20 | 19       | 18                       | 17 | 16 |
| Name     |                     |                      |    |    |                      |                       |    |    |    |    |    |    |          |                          |    |    |
| Type     |                     |                      |    |    |                      |                       |    |    |    |    |    |    |          |                          |    |    |
| Reset    |                     |                      |    |    |                      |                       |    |    |    |    |    |    |          |                          |    |    |
| Bit      | 15                  | 14                   | 13 | 12 | 11                   | 10                    | 9  | 8  | 7  | 6  | 5  | 4  | 3        | 2                        | 1  | 0  |
| Name     | QDMA_IN_PRI_PAGE_WR | QDMA_IN_PRI_PAGE_SEL |    |    | QDMA_OUT_PRI_PAGE_WR | QDMA_OUT_PRI_PAGE_SEL |    |    |    |    |    |    |          | STATUS_UPDATE_PERIOD_SEL |    |    |
| Type     | RW                  | RW                   |    |    | RW                   | RW                    |    |    |    |    |    |    |          | RW                       |    |    |
| Reset    | 0                   | 0                    | 0  | 0  | 0                    | 0                     | 0  | 0  |    |    |    |    |          | 0                        | 0  | 0  |

| Bit(s) | Name                     | Description                                                                                                                                                                                                                                                                                                                                                                            |
|--------|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15     | QDMA_IN_PRI_PAGE_WR      | <b>QDMA Input Priority Page Write Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                                                                                                        |
| 14:12  | QDMA_IN_PRI_PAGE_SEL     | <b>QDMA Input Priority Page Selection</b><br><br>It will latch input priority remap setting (PFC_CFG_5~PFC_CFG_36) to selected page when QDMA_IN_PRI_PAGE_WR = 1.<br><br>It will be read back into PFC_CFG_5~PFC_CFG_36 according to select source when QDMA_IN_PRI_PAGE_WR = 0.<br><br>3'b000: GMAC1<br><br>3'b001: GMAC2<br><br>3'b010: GMAC3<br><br>3'b011 ~ 3'b111: Reserved       |
| 11     | QDMA_OUT_PRI_PAGE_WR     | <b>QDMA Output Priority Page Write Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                                                                                                       |
| 10:8   | QDMA_OUT_PRI_PAGE_SEL    | <b>QDMA Output Priority Page Selection</b><br><br>It will latch output priority remap setting (PFC_CFG_43~PFC_CFG_74) to selected page when QDMA_OUT_PRI_PAGE_WR = 1.<br><br>It will be read back into PFC_CFG_43~PFC_CFG_74 according to select source when QDMA_OUT_PRI_PAGE_WR = 0.<br><br>3'b000: GMAC1<br><br>3'b001: GMAC2<br><br>3'b010: GMAC3<br><br>3'b011 ~ 3'b111: Reserved |
| 2:0    | STATUS_UPDATE_PERIOD_SEL | <b>Status Update Period Selection</b>                                                                                                                                                                                                                                                                                                                                                  |

| Bit(s) | Name | Description    |
|--------|------|----------------|
|        |      | 3'b000: Bypass |
|        |      | 3'b001: 1us    |
|        |      | 3'b010: 20us   |
|        |      | 3'b011: 125us  |
|        |      | 3'b100: 1ms    |

15101400      CDMQ IG\_CTRL      CDM VLAN control      81000000

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17     | 16 |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|
| Name  | CDM_TPID |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |
| Reset | 1        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0      | 0  |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1      | 0  |
| Name  |          |    |    |    |    |    |    |    |    |    |    |    |    |    | MD_CDM |    |
| Type  |          |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     |    |
| Reset |          |    |    |    |    |    |    |    |    |    |    |    |    |    | 0      |    |

| Bit(s) | Name     | Description                                                                                                                               |
|--------|----------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | CDM_TPID | Inserted VLAN TPID                                                                                                                        |
| 1      | MD_CDM   | <p>To indicate whether the CDM is connected to MDMA</p> <p>0: The CDM is not connected to MDMA</p> <p>1: The CDM is connected to MDMA</p> |

15101404 CDMQ\_EG\_CTRL CDM egress control 00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17                           | 16       |
|-------|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|------------------------------|----------|
| Name  |    |    |    |    |    |    |    |    |             |    |    |    |    |    |                              |          |
| Type  |    |    |    |    |    |    |    |    |             |    |    |    |    |    |                              |          |
| Reset |    |    |    |    |    |    |    |    |             |    |    |    |    |    |                              |          |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1                            | 0        |
| Name  |    |    |    |    |    |    |    |    | DIS_TSO_SUM |    |    |    |    |    | fs_parser_l3_ignore_wait_emp | UNTAG_EN |
| Type  |    |    |    |    |    |    |    |    | RW          |    |    |    |    |    | RW                           | RW       |
| Reset |    |    |    |    |    |    |    |    | 0           |    |    |    |    |    | 0                            | 0        |

| Bit(s) | Name                         | Description                                                                                                                                                                                            |
|--------|------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7      | DIS_TSO_SUM                  | <p><b>Disable TSO, IP/TCP/UDP checksum generation on CDM port, not matter whether DMAD enable it.</b></p> <p>0: TSO/CHKSUM control from DMAD</p> <p>1: Disable TSO/CHKSUM</p>                          |
| 1      | fs_parser_l3_ignore_wait_emp | <p><b>Safety for fs_parser to generate the EOF signal</b></p> <p>0: fs_parser use wait_emp state to generate the EOF signal.</p> <p>1:fs_parser not use wait_emp state to generate the EOF signal.</p> |
| 0      | UNTAG_EN                     | <p><b>VLAN un-tag</b></p> <p>Un-tag the egress packets which are transmitted from CDM to CPU</p> <p>0: Disable</p> <p>1: The first 4-byte VLAN tag after Source Address will be untagged</p>           |

15101408      CDMQ\_PPP\_GEN      CDM PPPoE generation      00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|
| Name  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PPP_INS |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| Name  | SESS_ID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       |

| Bit(s) | Name    | Description            |
|--------|---------|------------------------|
| 16     | PPP_INS | PPPoE Header Insertion |
| 15:0   | SESS_ID | PPPoE Session ID       |

**15101500 GDM2 IG\_CTRL GDM ingress control C0717777**

| Bit   | 31         | 30 | 29 | 28 | 27    | 26 | 25      | 24      | 23    | 22        | 21        | 20        | 19        | 18 | 17 | 16       |
|-------|------------|----|----|----|-------|----|---------|---------|-------|-----------|-----------|-----------|-----------|----|----|----------|
| Name  | L3_MAX_LEN |    |    |    |       |    | INSV_EN | STAG_EN |       | GDM_ICSEN | GDM_TCSEN | GDM_UCSEN | DROP_256B |    |    | STRP_CRC |
| Type  | RW         |    |    |    |       |    | RW      | RW      |       | RW        | RW        | RW        | RW        |    |    | RW       |
| Reset | 1          | 1  | 0  | 0  |       |    | 0       | 0       |       | 1         | 1         | 1         | 0         |    |    | 1        |
| Bit   | 15         | 14 | 13 | 12 | 11    | 10 | 9       | 8       | 7     | 6         | 5         | 4         | 3         | 2  | 1  | 0        |
| Name  | MYMAC_DP   |    |    |    | BC_DP |    |         |         | MC_DP |           |           |           | UN_DP     |    |    |          |
| Type  | RW         |    |    |    | RW    |    |         |         | RW    |           |           |           | RW        |    |    |          |
| Reset | 0          | 1  | 1  | 1  | 0     | 1  | 1       | 1       | 0     | 1         | 1         | 1         | 0         | 1  | 1  | 1        |

| Bit(s) | Name       | Description                                                                                                                                                                                                  |
|--------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | L3_MAX_LEN | <b>Maximum L3 length allowed = {L3_MAX_LEN,10'b0}</b>                                                                                                                                                        |
| 25     | INSV_EN    | <b>VLAN insertion</b><br>Insert Port VID on the received packets on the corresponding GDM port.<br>0: Disable<br>1: Insert 4-byte VLAN tag after Source Address                                              |
| 24     | STAG_EN    | <b>Special tag indication</b><br>Indicate that the received packet is carrying the special tag from GDM port.<br>0: No special tag inserted.<br>1: The first 2-byte after Source Address is the special tag. |
| 22     | GDM_ICSEN  | <b>IPv4 header checksum error drop</b><br>0: checksum error status reported on RX descriptor (IP4F)<br>1: checksum error packet will be dropped                                                              |
| 21     | GDM_TCSEN  | <b>TCP checksum error drop</b><br>0: checksum error status reported on RX descriptor (L4F)<br>1: checksum error packet will be dropped                                                                       |
| 20     | GDM_UCSEN  | <b>UDP checksum error drop</b><br>0: checksum error status reported on RX descriptor (L4F)<br>1: checksum error packet will be dropped                                                                       |
| 19     | DROP_256B  | <b>A special mode to drop packets with payload &gt; 256 bytes</b><br>1'b0: Drop packets according to the standard Ethernet frame length limitation.<br>1'b1: Drop packets with payload > 256 bytes           |
| 16     | STRP_CRC   | <b>GDM RX CRC Stripping</b><br>1'b: Disable GDM RX CRC stripping                                                                                                                                             |

| Bit(s) | Name     | Description                             |
|--------|----------|-----------------------------------------|
|        |          | 1'b1: Enable GDM RX CRC stripping       |
| 15:12  | MYMAC_DP | <b>MY_MAC frames destination port</b>   |
|        |          | 4'b0000: ADMA                           |
|        |          | 4'b0001: GDM1                           |
|        |          | 4'b0010: GDM2                           |
|        |          | 4'b0011: PPE0                           |
|        |          | 4'b0100: PPE1                           |
|        |          | 4'b0101: QDMA                           |
|        |          | 4'b0110: Reserved                       |
|        |          | 4'b0111: Discard                        |
|        |          | 4'b1000: WDMA0                          |
|        |          | 4'b1001: WDMA1                          |
|        |          | 4'b1010: MDMA                           |
|        |          | 4'b1011: EDMA0                          |
|        |          | 4'b1100: EDMA1                          |
|        |          | 4'b1101: WDMA2                          |
|        |          | 4'b1110: EDMA2                          |
| 11:8   | BC_DP    | <b>Broadcast frame destination port</b> |
|        |          | 4'b0000: ADMA                           |
|        |          | 4'b0001: GDM1                           |
|        |          | 4'b0010: GDM2                           |
|        |          | 4'b0011: PPE0                           |
|        |          | 4'b0100: PPE1                           |
|        |          | 4'b0101: QDMA                           |
|        |          | 4'b0110: Reserved                       |
|        |          | 4'b0111: Discard                        |
|        |          | 4'b1000: WDMA0                          |
|        |          | 4'b1001: WDMA1                          |
|        |          | 4'b1010: MDMA                           |
|        |          | 4'b1011: EDMA0                          |
|        |          | 4'b1100: EDMA1                          |

| Bit(s) | Name  | Description                             |
|--------|-------|-----------------------------------------|
| 7:4    | MC_DP | 4'b1101: WDMA2                          |
|        |       | 4'b1110: EDMA2                          |
|        |       | <b>Multicast frame destination port</b> |
|        |       | 4'b0000: ADMA                           |
|        |       | 4'b0001: GDM1                           |
|        |       | 4'b0010: GDM2                           |
|        |       | 4'b0011: PPE0                           |
|        |       | 4'b0100: PPE1                           |
|        |       | 4'b0101: QDMA                           |
|        |       | 4'b0110: Reserved                       |
|        |       | 4'b0111: Discard                        |
|        |       | 4'b1000: WDMA0                          |
|        |       | 4'b1001: WDMA1                          |
|        |       | 4'b1010: MDMA                           |
|        |       | 4'b1011: EDMA0                          |
|        |       | 4'b1100: EDMA1                          |
|        |       | 4'b1101: WDMA2                          |
|        |       | 4'b1110: EDMA2                          |
| 3:0    | UN_DP | <b>Other frame destination port</b>     |
|        |       | 4'b0000: ADMA                           |
|        |       | 4'b0001: GDM1                           |
|        |       | 4'b0010: GDM2                           |
|        |       | 4'b0011: PPE0                           |
|        |       | 4'b0100: PPE1                           |
|        |       | 4'b0101: QDMA                           |
|        |       | 4'b0110: Reserved                       |
|        |       | 4'b0111: Discard                        |
|        |       | 4'b1000: WDMA0                          |
|        |       | 4'b1001: WDMA1                          |
|        |       | 4'b1010: MDMA                           |
|        |       | 4'b1011: EDMA0                          |



| Bit(s) | Name | Description    |
|--------|------|----------------|
|        |      | 4'b1100: EDMA1 |
|        |      | 4'b1101: WDMA2 |
|        |      | 4'b1110: EDMA2 |

15101504      **GDM2 EG\_CTRL**      **GDM egress control**      00000000

| Bit   | 31       | 30       | 29      | 28      | 27 | 26 | 25 | 24      | 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----------|---------|---------|----|----|----|---------|---------|----|----|----|----|----|----|----|
| Name  | XGDM_SEL | UNTAG_EN | DIS_PAD | DIS_CRC |    |    |    | SHPR_EN | BK_SIZE |    |    |    |    |    |    |    |
| Type  | RW       | RW       | RW      | RW      |    |    |    | RW      | RW      |    |    |    |    |    |    |    |
| Reset | 0        | 0        | 0       | 0       |    |    |    | 0       | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15       | 14       | 13      | 12      | 11 | 10 | 9  | 8       | 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TK_TICK  |          | TK_RATE |         |    |    |    |         |         |    |    |    |    |    |    |    |
| Type  | RW       |          | RW      |         |    |    |    |         |         |    |    |    |    |    |    |    |
| Reset | 0        |          | 0       | 0       | 0  | 0  | 0  | 0       | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name     | Description                                                                                                                                                                     |
|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | XGDM_SEL | <b>GDM path selection for 10G Ethernet</b><br><br>0: GDM path<br><br>1: XGDM path                                                                                               |
| 30     | UNTAG_EN | <b>VLAN un-tag</b><br><br>Un-tag the egress packets which are transmitted from GDM.<br><br>0: Disable<br><br>1: The first 4-byte VLAN tag after Source Address will be untagged |
| 29     | DIS_PAD  | <b>GMAC TX padding function</b><br><br>1'b0: Enable GMAC TX padding<br><br>1'b1: Disable GMAC TX padding                                                                        |
| 28     | DIS_CRC  | <b>GMAC TX CRC generation</b><br><br>1'b0: Enable GMAC TX CRC generation<br><br>1'b1: Disable GMAC TX CRC generation                                                            |
| 24     | SHPR_EN  | <b>GDM output shaper enable</b><br><br>1'b0: Disable<br><br>1'b1: Enable                                                                                                        |
| 23:16  | BK_SIZE  | <b>GDM output shaper bucket size.</b><br><br>This unit is 1K-byte                                                                                                               |
| 15     | TK_TICK  | <b>GDM shaper token period</b><br><br>1'b0: GDM shaper adds token every 1ms<br><br>1'b1: GDM shaper adds token every 20us                                                       |
| 13:0   | TK_RATE  | <b>GDM output shaper token rate</b><br><br>The unit is 8 bytes/ms or 8 bytes/20us according to TK_TICK.                                                                         |

15101508 GDM2 MAC LSB GDM MY\_MAC address LSB 00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | MAC_ADR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAC_ADR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description           |
|--------|---------|-----------------------|
| 31:0   | MAC_ADR | MY_MAC Address [31:0] |

1510150C GDM2 MAC MSB GDM MY\_MAC address MSB 00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAC_ADR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description            |
|--------|---------|------------------------|
| 15:0   | MAC_ADR | MY_MAC Address [47:32] |

15101510      **GDM2\_VLAN\_GEN**      GDM VLAN generation      81000000

| Bit   | 31       | 30 | 29 | 28      | 27      | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----|----|---------|---------|----|----|----|----|----|----|----|----|----|----|----|
| Name  | GDM_TPID |    |    |         |         |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    |         |         |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1        | 0  | 0  | 0       | 0       | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15       | 14 | 13 | 12      | 11      | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | GDM_PRI  |    |    | GDM_CFI | GDM_VID |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    | RW      | RW      |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0        | 0  | 0  | 0       | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name     | Description        |
|--------|----------|--------------------|
| 31:16  | GDM_TPID | Inserted VLAN TPID |
| 15:13  | GDM_PRI  | Inserted PRI       |
| 12     | GDM_CFI  | Inserted CFI       |
| 11:0   | GDM_VID  | Inserted VLAN ID   |

15101514 GDM2\_FILTER\_CTRL GDM filter control 00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19          | 18           | 17           | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|-------------|--------------|--------------|----|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |             |              |              |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |             |              |              |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |             |              |              |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3           | 2            | 1            | 0  |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    | GDM_VIDF_EN | GMD_HASH_ALG | GDM_DAF_MODE |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    | RW          | RW           | RW           |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    | 0           | 0            | 0            | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                   |
|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3      | GDM_VIDF_EN  | <b>GDM VLAN ID filter enable</b>                                                                                                                                                                                                              |
| 2      | GMD_HASH_ALG | <b>Hash Algorithm setting</b><br><br>0: Direct map - Using DA40 and DA 7~0 as hash key. Receive packet if corresponding bit is set.<br><br>1: CRC32 - Using 32-bit CRC bit 8~0 of DA as hash key. Receive packet if corresponding bit is set. |
| 1:0    | GDM_DAF_MODE | <b>Receive packet with DA Filter function</b><br><br>0: Promiscuous mode - Receive all packets.<br><br>1: Filter packet by MAC_MAC/Broadcast/Hash table<br><br>2: Filter packet by MAC_MAC/Broadcast<br><br>3: Reserved                       |

**15101518      GDM2\_VIDF01      GDM VID filter control 01      00000000**

| Bit   | 31            | 30 | 29 | 28 | 27        | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|-----------|----|----|----|----|----|----|----|----|----|----|----|
| Name  | GDM2_VID1_VLD |    |    |    | GDM2_VID1 |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW            |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11        | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | GDM2_VID0_VLD |    |    |    | GDM2_VID0 |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW            |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description          |
|--------|---------------|----------------------|
| 31     | GDM2_VID1_VLD | VLAN ID #1 valid bit |
| 27:16  | GDM2_VID1     | VLAN ID #1           |
| 15     | GDM2_VID0_VLD | VLAN ID #0 valid bit |
| 11:0   | GDM2_VID0     | VLAN ID #0           |

**1510151C      GDM2\_VIDF23      GDM VID filter control 23      00000000**

| Bit   | 31            | 30 | 29 | 28 | 27        | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|-----------|----|----|----|----|----|----|----|----|----|----|----|
| Name  | GDM2_VID3_VLD |    |    |    | GDM2_VID3 |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW            |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11        | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | GDM2_VID2_VLD |    |    |    | GDM2_VID2 |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW            |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             |    |    |    | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description          |
|--------|---------------|----------------------|
| 31     | GDM2_VID3_VLD | VLAN ID #3 valid bit |
| 27:16  | GDM2_VID3     | VLAN ID #3           |
| 15     | GDM2_VID2_VLD | VLAN ID #2 valid bit |
| 11:0   | GDM2_VID2     | VLAN ID #2           |

**15101520 GDM2\_DOS\_CFG\_0 GDM DOS configuration 0 00000000**

| Bit   | 31                        | 30                   | 29                        | 28                     | 27             | 26             | 25 | 24 | 23                         | 22                    | 21                         | 20                         | 19                 | 18                 | 17 | 16 |
|-------|---------------------------|----------------------|---------------------------|------------------------|----------------|----------------|----|----|----------------------------|-----------------------|----------------------------|----------------------------|--------------------|--------------------|----|----|
| Name  | SPD_2P5G_MODE             | ICMP_AND_TOS_EQ_ZERO | MY_MAC_CHECK              |                        |                |                |    |    | TCP_DROP_INTERRUPT_STATUS  | TCP_RATE_LIMITER_RST  | TCP_DROP_INTERRUPT_ENABLE  | TCP_SYN_PACKET_DROP_ENABLE | TCP_SYN_LIMIT_MODE | TCP_SYN_LIMIT_UNIT |    |    |
| Type  | RW                        | RW                   | RW                        |                        |                |                |    |    | W1C                        | RW                    | RW                         | RW                         | RW                 | RW                 |    |    |
| Reset | 0                         | 0                    | 0                         |                        |                |                |    |    | 0                          | 0                     | 0                          | 0                          | 0                  | 0                  | 0  | 0  |
| Bit   | 15                        | 14                   | 13                        | 12                     | 11             | 10             | 9  | 8  | 7                          | 6                     | 5                          | 4                          | 3                  | 2                  | 1  | 0  |
| Name  | UDP_DROP_INTERRUPT_STATUS | UDP_RATE_LIMITER_RST | UDP_DROP_INTERRUPT_ENABLE | UDP_PACKET_DROP_ENABLE | UDP_LIMIT_MODE | UDP_LIMIT_UNIT |    |    | ICMP_DROP_INTERRUPT_STATUS | ICMP_RATE_LIMITER_RST | ICMP_DROP_INTERRUPT_ENABLE | ICMP_PACKET_DROP_ENABLE    | ICMP_LIMIT_MODE    | ICMP_LIMIT_UNIT    |    |    |
| Type  | W1C                       | RW                   | RW                        | RW                     | RW             | RW             |    |    | W1C                        | RW                    | RW                         | RW                         | RW                 | RW                 |    |    |
| Reset | 0                         | 0                    | 0                         | 0                      | 0              | 0              | 0  | 0  | 0                          | 0                     | 0                          | 0                          | 0                  | 0                  | 0  | 0  |

| Bit(s) | Name                      | Description                                                                                                                                                                                                                                                                                                        |
|--------|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | SPD_2P5G_MODE             | <b>Reference *_LIMIT_2P5G Setting for Rate Limitation</b><br><br>1'b0: Disable<br><br>1'b1: Enable                                                                                                                                                                                                                 |
| 30     | ICMP_AND_TOS_EQ_ZERO      | <b>IPv4 ICMP Packet Recognition Control</b><br><br>1'b0: Ignore TOS field of IPv4 header, only check PROTOCOL field equal to 1 to regard as IPv4 ICMP packet<br><br>1'b1: It will also check TOS field equal to 0 besides PROTOCOL field equal to 1                                                                |
| 29     | MY_MAC_CHECK              | <b>MY MAC Address Check Control</b><br><br>1'b0: Ignore DA checking of incoming packet that involve in rate limit mechanism directly<br><br>1'b1: It will check DA of incoming packet whether equals MY_MAC address, if YES, given packet will involve in rate limit mechanism otherwise pass this packet directly |
| 23     | TCP_DROP_INTERRUPT_STATUS | <b>TCP Packet Drop Interrupt Event Status</b><br><br>1'b0: No interrupt<br><br>1'b1: Interrupt event trigger                                                                                                                                                                                                       |
| 22     | TCP_RATE_LIMITER_RST      | <b>TCP Rate Limiter Reset Control</b><br><br>1'b0: Reset asserted<br><br>1'b1: Reset de-asserted                                                                                                                                                                                                                   |
| 21     | TCP_DROP_INTERRUPT_EN     | <b>TCP Packet Drop Interrupt Event Control</b><br><br>1'b0: Disable interrupt event to final interrupt<br><br>1'b1: Enable interrupt event to final interrupt                                                                                                                                                      |
| 20     | TCP_SYN_PACKET_DROP_EN    | <b>TCP SYN Packet Drop Control when Reaching Rate Limitation</b>                                                                                                                                                                                                                                                   |

| Bit(s) | Name                 | Description                                                  |
|--------|----------------------|--------------------------------------------------------------|
|        |                      | 1'b0: No packet drop                                         |
|        |                      | 1'b1: Packet drop for following TCP SYN packet               |
| 19     | TCP_SYN_LIMIT_MODE   | <b>TCP SYN Rate Limitation Mode</b>                          |
|        |                      | 1'b0: Packet-based (1 second period)                         |
|        |                      | 1'b1: Rate-based                                             |
| 18:16  | TCP_SYN_LIMIT_UNIT   | <b>Unit of TCP SYN Rate Limitation</b>                       |
|        |                      | 3'b000: 64 packets or 64 Kbps                                |
|        |                      | 3'b001: 256 packets or 256 Kbps                              |
|        |                      | 3'b010: 1 K packets or 1 Mbps                                |
|        |                      | 3'b011: 4 K packets or 4 Mbps                                |
|        |                      | 3'b100: 16 K packets or 16 Mbps                              |
|        |                      | 3'b101: 64K packets or 64 Mbps                               |
|        |                      | 3'b110: 256K packets or 256 Mbps                             |
|        |                      | 3'b111: 1M packets or 1 Gbps                                 |
| 15     | UDP_DROP_INT_STATUS  | <b>UDP Packet Drop Interrupt Event Status</b>                |
|        |                      | 1'b0: No interrupt                                           |
|        |                      | 1'b1: Interrupt event trigger                                |
| 14     | UDP_RATE_LIMITER_RST | <b>UDP Rate Limiter Reset Control</b>                        |
|        |                      | 1'b0: Reset asserted                                         |
|        |                      | 1'b1: Reset de-asserted                                      |
| 13     | UDP_DROP_INT_EN      | <b>UDP Packet Drop Interrupt Event Control</b>               |
|        |                      | 1'b0: Disable interrupt event to final interrupt             |
|        |                      | 1'b1: Enable interrupt event to final interrupt              |
| 12     | UDP_PKT_DROP_EN      | <b>UDP Packet Drop Control when Reaching Rate Limitation</b> |
|        |                      | 1'b0: No packet drop                                         |
|        |                      | 1'b1: Packet drop for following UDP packet                   |
| 11     | UDP_LIMIT_MODE       | <b>UDP Rate Limitation Mode</b>                              |
|        |                      | 1'b0: Packet-based (1 second period)                         |
|        |                      | 1'b1: Rate-based                                             |
| 10:8   | UDP_LIMIT_UNIT       | <b>Unit of UDP Rate Limitation</b>                           |
|        |                      | 3'b000: 64 packets or 64 Kbps                                |
|        |                      | 3'b001: 256 packets or 256 Kbps                              |



| Bit(s) | Name                  | Description                                                   |
|--------|-----------------------|---------------------------------------------------------------|
|        |                       | 3'b010: 1 K packets or 1 Mbps                                 |
|        |                       | 3'b011: 4 K packets or 4 Mbps                                 |
|        |                       | 3'b100: 16 K packets or 16 Mbps                               |
|        |                       | 3'b101: 64K packets or 64 Mbps                                |
|        |                       | 3'b110: 256K packets or 256 Mbps                              |
|        |                       | 3'b111: 1M packets or 1 Gbps                                  |
| 7      | ICMP_DROP_INT_STATUS  | <b>ICMP Packet Drop Interrupt Event Status</b>                |
|        |                       | 1'b0: No interrupt                                            |
|        |                       | 1'b1: Interrupt event trigger                                 |
| 6      | ICMP_RATE_LIMITER_RST | <b>ICMP Rate Limiter Reset Control</b>                        |
|        |                       | 1'b0: Reset asserted                                          |
|        |                       | 1'b1: Reset de-asserted                                       |
| 5      | ICMP_DROP_INT_EN      | <b>ICMP Packet Drop Interrupt Event Control</b>               |
|        |                       | 1'b0: Disable interrupt event to final interrupt              |
|        |                       | 1'b1: Enable interrupt event to final interrupt               |
| 4      | ICMP_PKT_DROP_EN      | <b>ICMP Packet Drop Control when Reaching Rate Limitation</b> |
|        |                       | 1'b0: No packet drop                                          |
|        |                       | 1'b1: Packet drop for following ICMP packet                   |
| 3      | ICMP_LIMIT_MODE       | <b>ICMP Rate Limitation Mode</b>                              |
|        |                       | 1'b0: Packet-based (1 second period)                          |
|        |                       | 1'b1: Rate-based                                              |
| 2:0    | ICMP_LIMIT_UNIT       | <b>Unit of ICMP Rate Limitation</b>                           |
|        |                       | 3'b000: 64 packets or 64 Kbps                                 |
|        |                       | 3'b001: 256 packets or 256 Kbps                               |
|        |                       | 3'b010: 1 K packets or 1 Mbps                                 |
|        |                       | 3'b011: 4 K packets or 4 Mbps                                 |
|        |                       | 3'b100: 16 K packets or 16 Mbps                               |
|        |                       | 3'b101: 64K packets or 64 Mbps                                |
|        |                       | 3'b110: 256K packets or 256 Mbps                              |
|        |                       | 3'b111: 1M packets or 1 Gbps                                  |

15101524 **GDM2 DOS CFG 1** **GDM DOS configuration 1** 00000000

| Bit          | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|--------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| <b>Name</b>  | TCP_SYN_LIMIT_2P5G |    |    |    |    |    |    |    | TCP_SYN_LIMIT_1G  |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | TCP_SYN_LIMIT_100M |    |    |    |    |    |    |    | TCP_SYN_LIMIT_10M |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                 |    |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                                                     |
|--------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | TCP_SYN_LIMIT_2P5G | <b>SGMII+ 2500Mbps or USXGMII 10Gbps TCP_SYN Rate Limit Control</b><br>The TCP_SYN rate limit<br>8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps<br>8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps   |
| 23:16  | TCP_SYN_LIMIT_1G   | <b>SGMII 1000Mbps or USXGMII 5Gbps TCP_SYN Rate Limit Control</b><br>The TCP_SYN rate limit<br>8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps<br>8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps     |
| 15:8   | TCP_SYN_LIMIT_100M | <b>SGMII 100Mbps or USXGMII 2.5Gbps TCP_SYN Rate Limit Control</b><br>The TCP_SYN rate limit<br>8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps<br>8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps    |
| 7:0    | TCP_SYN_LIMIT_10M  | <b>SGMII 10Mbps or USXGMII 1Gbps below TCP_SYN Rate Limit Control</b><br>The TCP_SYN rate limit<br>8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps<br>8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps |

15101528      **GDM2 DOS CFG 2**      **GDM DOS configuration 2**      00000000

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|----------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| <b>Name</b>  | UDP_LIMIT_2P5G |    |    |    |    |    |    |    | UDP_LIMIT_1G  |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW            |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | UDP_LIMIT_100M |    |    |    |    |    |    |    | UDP_LIMIT_10M |    |    |    |    |    |    |    |
| <b>Type</b>  | RW             |    |    |    |    |    |    |    | RW            |    |    |    |    |    |    |    |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                                                                                                     |
|--------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | UDP_LIMIT_2P5G | <b>SGMII+ 2500Mbps or USXGMII 10Gbps UDP Rate Limit Control</b><br>The UDP rate limit<br>8'h0: (0* UDP_LIMIT_UNIT) packets or bps<br>8'h1: (1* UDP_LIMIT_UNIT) packets or bps   |
| 23:16  | UDP_LIMIT_1G   | <b>SGMII 1000Mbps or USXGMII 5Gbps UDP Rate Limit Control</b><br>The UDP rate limit<br>8'h0: (0* UDP_LIMIT_UNIT) packets or bps<br>8'h1: (1* UDP_LIMIT_UNIT) packets or bps     |
| 15:8   | UDP_LIMIT_100M | <b>SGMII 100Mbps or USXGMII 2.5Gbps UDP Rate Limit Control</b><br>The UDP rate limit<br>8'h0: (0* UDP_LIMIT_UNIT) packets or bps<br>8'h1: (1* UDP_LIMIT_UNIT) packets or bps    |
| 7:0    | UDP_LIMIT_10M  | <b>SGMII 10Mbps or USXGMII 1Gbps below UDP Rate Limit Control</b><br>The UDP rate limit<br>8'h0: (0* UDP_LIMIT_UNIT) packets or bps<br>8'h1: (1* UDP_LIMIT_UNIT) packets or bps |

1510152C      **GDM2 DOS CFG 3**      **GDM DOS configuration 3**      00000000

| Bit          | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| <b>Name</b>  | ICMP_LIMIT_2P5G |    |    |    |    |    |    |    | ICMP_LIMIT_1G  |    |    |    |    |    |    |    |
| <b>Type</b>  | RW              |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | ICMP_LIMIT_100M |    |    |    |    |    |    |    | ICMP_LIMIT_10M |    |    |    |    |    |    |    |
| <b>Type</b>  | RW              |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                         |
|--------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | ICMP_LIMIT_2P5G | <b>SGMII+ 2500Mbps or USXGMII 10Gbps ICMP Rate Limit Control</b><br>The ICMP rate limit<br>8'h0: (0* ICMP_LIMIT_UNIT) packets or bps<br>8'h1: (1* ICMP_LIMIT_UNIT) packets or bps   |
| 23:16  | ICMP_LIMIT_1G   | <b>SGMII 1000Mbps or USXGMII 5Gbps ICMP Rate Limit Control</b><br>The ICMP rate limit<br>8'h0: (0* ICMP_LIMIT_UNIT) packets or bps<br>8'h1: (1* ICMP_LIMIT_UNIT) packets or bps     |
| 15:8   | ICMP_LIMIT_100M | <b>SGMII 100Mbps or USXGMII 2.5Gbps ICMP Rate Limit Control</b><br>The ICMP rate limit<br>8'h0: (0* ICMP_LIMIT_UNIT) packets or bps<br>8'h1: (1* ICMP_LIMIT_UNIT) packets or bps    |
| 7:0    | ICMP_LIMIT_10M  | <b>SGMII 10Mbps or USXGMII 1Gbps below ICMP Rate Limit Control</b><br>The ICMP rate limit<br>8'h0: (0* ICMP_LIMIT_UNIT) packets or bps<br>8'h1: (1* ICMP_LIMIT_UNIT) packets or bps |

15101534      CDM2\_THRES      CDM2 threshold      00000008

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |                |    |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |                |    |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |                |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    | high_threshold |    |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    | RW             |    |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    | 1              | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                    |
|--------|----------------|----------------------------------------------------------------|
| 3:0    | high_threshold | memory high threshold value<br>memory size: high_threshold*1KB |

15101600      CDMW0\_IG\_CTRL      CDM VLAN control      81000000

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21     | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|
| Name  | CDM_TPID |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |
| Reset | 1        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0      | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5      | 4  | 3  | 2  | 1  | 0  |
| Name  |          |    |    |    |    |    |    |    |    |    | MD_CDM |    |    |    |    |    |
| Type  |          |    |    |    |    |    |    |    |    |    | RW     |    |    |    |    |    |
| Reset |          |    |    |    |    |    |    |    |    |    | 0      |    |    |    |    |    |

| Bit(s) | Name     | Description                                                                              |
|--------|----------|------------------------------------------------------------------------------------------|
| 31:16  | CDM_TPID | Inserted VLAN TPID                                                                       |
| 5      | MD_CDM   | CDM connects to MDMA<br>1'b0: CDM does not connect to MDMA<br>1'b1: CDM connects to MDMA |

15101604 CDMW0 EG\_CTRL CDM egress control 00000182

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24          | 23 | 22         | 21 | 20 | 19 | 18 | 17                 | 16       |
|-------|----|----|----|----|----|----|----|-------------|----|------------|----|----|----|----|--------------------|----------|
| Name  |    |    |    |    |    |    |    |             |    |            |    |    |    |    |                    |          |
| Type  |    |    |    |    |    |    |    |             |    |            |    |    |    |    |                    |          |
| Reset |    |    |    |    |    |    |    |             |    |            |    |    |    |    |                    |          |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8           | 7  | 6          | 5  | 4  | 3  | 2  | 1                  | 0        |
| Name  |    |    |    |    |    |    |    | RR_RING_NUM |    | RR_RING_EN |    |    |    |    | CDM_FS_SOF_WR_TIME | UNTAG_EN |
| Type  |    |    |    |    |    |    |    | RW          |    | RW         |    |    |    |    | RW                 | RW       |
| Reset |    |    |    |    |    |    |    | 1           | 1  | 0          |    |    |    |    | 1                  | 0        |

| Bit(s) | Name               | Description                                                                                                                                                                                                                                                |
|--------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8:7    | RR_RING_NUM        | <b>Maximum Round Rubin ring index for CDM to generate RX ring index</b>                                                                                                                                                                                    |
| 6      | RR_RING_EN         | <b>Enable CDM generate RX ring index by Round Rubin method for TOPS</b><br><br>0: RX ring index from PSE info<br><br>1: RX ring index generate by Round-Rubin                                                                                              |
| 1      | CDM_FS_SOF_WR_TIME | <b>CDM SOF information</b><br><br>The time CDM write the start-of-frame Information to async-fifo for XDMA3.0<br><br>0: CDM FS part SOF info write to FIFO after VLAN tag processing<br><br>1: CDM FS part SOF info write to FIFO after L2 data processing |
| 0      | UNTAG_EN           | <b>VLAN un-tag</b><br><br>Un-tag the egress packets which are transmitted from CDM to CPU<br><br>0: Disable<br><br>1: The first 4-byte VLAN tag after Source Address will be untagged                                                                      |

15101608      CDMW0\_PPP\_GEN      CDM PPPoE generation      00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|
| Name  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PPP_INS |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| Name  | SESS_ID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       |

| Bit(s) | Name    | Description            |
|--------|---------|------------------------|
| 16     | PPP_INS | PPPoE Header Insertion |
| 15:0   | SESS_ID | PPPoE Session ID       |

15101610      CDMW1\_IG\_CTRL      CDM VLAN control      81000000

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21     | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|
| Name  | CDM_TPID |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |
| Reset | 1        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0      | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5      | 4  | 3  | 2  | 1  | 0  |
| Name  |          |    |    |    |    |    |    |    |    |    | MD_CDM |    |    |    |    |    |
| Type  |          |    |    |    |    |    |    |    |    |    | RW     |    |    |    |    |    |
| Reset |          |    |    |    |    |    |    |    |    |    | 0      |    |    |    |    |    |

| Bit(s) | Name     | Description                        |
|--------|----------|------------------------------------|
| 31:16  | CDM_TPID | Inserted VLAN TPID                 |
| 5      | MD_CDM   | CDM connects to MDMA               |
|        |          | 1'b0: CDM does not connect to MDMA |
|        |          | 1'b1: CDM connects to MDMA         |

15101614 CDMW1 EG\_CTRL CDM egress control 00000182

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24          | 23 | 22         | 21 | 20 | 19 | 18 | 17                 | 16       |
|-------|----|----|----|----|----|----|----|-------------|----|------------|----|----|----|----|--------------------|----------|
| Name  |    |    |    |    |    |    |    |             |    |            |    |    |    |    |                    |          |
| Type  |    |    |    |    |    |    |    |             |    |            |    |    |    |    |                    |          |
| Reset |    |    |    |    |    |    |    |             |    |            |    |    |    |    |                    |          |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8           | 7  | 6          | 5  | 4  | 3  | 2  | 1                  | 0        |
| Name  |    |    |    |    |    |    |    | RR_RING_NUM |    | RR_RING_EN |    |    |    |    | CDM_FS_SOF_WR_TIME | UNTAG_EN |
| Type  |    |    |    |    |    |    |    | RW          |    | RW         |    |    |    |    | RW                 | RW       |
| Reset |    |    |    |    |    |    |    | 1           | 1  | 0          |    |    |    |    | 1                  | 0        |

| Bit(s) | Name               | Description                                                                                                                                                                                                                                                |
|--------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8:7    | RR_RING_NUM        | <b>Maximum Round Rubin ring index for CDM to generate RX ring index</b>                                                                                                                                                                                    |
| 6      | RR_RING_EN         | <b>Enable CDM generate RX ring index by Round Rubin method for TOPS</b><br><br>0: RX ring index from PSE info<br><br>1: RX ring index generate by Round-Rubin                                                                                              |
| 1      | CDM_FS_SOF_WR_TIME | <b>CDM SOF information</b><br><br>The time CDM write the start-of-frame Information to async-fifo for XDMA3.0<br><br>0: CDM FS part SOF info write to FIFO after VLAN tag processing<br><br>1: CDM FS part SOF info write to FIFO after L2 data processing |
| 0      | UNTAG_EN           | <b>VLAN un-tag</b><br><br>Un-tag the egress packets which are transmitted from CDM to CPU<br><br>0: Disable<br><br>1: The first 4-byte VLAN tag after Source Address will be untagged                                                                      |



15101618 CDMW1\_PPP\_GEN CDM PPPoE generation 00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|
| Name  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PPP_INS |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| Name  | SESS_ID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       |

| Bit(s) | Name    | Description            |
|--------|---------|------------------------|
| 16     | PPP_INS | PPPoE Header Insertion |
| 15:0   | SESS_ID | PPPoE Session ID       |

1510161C CDMT\_PPP\_GEN CDM PPPoE generation 00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|
| Name  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PPP_INS |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| Name  | SESS_ID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       |

| Bit(s) | Name    | Description            |
|--------|---------|------------------------|
| 16     | PPP_INS | PPPoE Header Insertion |
| 15:0   | SESS_ID | PPPoE Session ID       |

15101620 CDME0\_IG\_CTRL CDM VLAN control 81000000

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|
| Name  | CDM_TPID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Reset | 1        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| Name  |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    | STAG_EN |
| Type  |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |
| Reset |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       |

| Bit(s) | Name     | Description                                                                                                                                                                                                        |
|--------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | CDM_TPID | Inserted VLAN TPID                                                                                                                                                                                                 |
| 0      | STAG_EN  | <b>Special tag indication</b><br><br>Indicate that the received packet is carrying the special tag from CPU<br><br>0: No special tag inserted.<br><br>1: The first 2-byte after Source Address is the special tag. |

15101624 CDME0\_EG\_CTRL CDM egress control 00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16       |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0        |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | UNTAG_EN |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW       |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0        |

| Bit(s) | Name     | Description                                                                                                                                                                           |
|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0      | UNTAG_EN | <b>VLAN un-tag</b><br><br>Un-tag the egress packets which are transmitted from CDM to CPU<br><br>0: Disable<br><br>1: The first 4-byte VLAN tag after Source Address will be untagged |

15101628      CDME0\_PPP\_GEN      CDM PPPoE generation      00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|
| Name  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PPP_INS |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| Name  | SESS_ID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       |

| Bit(s) | Name    | Description            |
|--------|---------|------------------------|
| 16     | PPP_INS | PPPoE Header Insertion |
| 15:0   | SESS_ID | PPPoE Session ID       |

**1510162C CDMT\_EG\_CTRL CDM egress control 00000182**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24          | 23 | 22         | 21 | 20 | 19 | 18 | 17                 | 16       |
|-------|----|----|----|----|----|----|----|-------------|----|------------|----|----|----|----|--------------------|----------|
| Name  |    |    |    |    |    |    |    |             |    |            |    |    |    |    |                    |          |
| Type  |    |    |    |    |    |    |    |             |    |            |    |    |    |    |                    |          |
| Reset |    |    |    |    |    |    |    |             |    |            |    |    |    |    |                    |          |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8           | 7  | 6          | 5  | 4  | 3  | 2  | 1                  | 0        |
| Name  |    |    |    |    |    |    |    | RR_RING_NUM |    | RR_RING_EN |    |    |    |    | CDM_FS_SOF_WR_TIME | UNTAG_EN |
| Type  |    |    |    |    |    |    |    | RW          |    | RW         |    |    |    |    | RW                 | RW       |
| Reset |    |    |    |    |    |    |    | 1           | 1  | 0          |    |    |    |    | 1                  | 0        |

| Bit(s) | Name               | Description                                                                                                                                                                                                                                                |
|--------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8:7    | RR_RING_NUM        | <b>Maximum Round Rubin ring index for CDM to generate RX ring index</b>                                                                                                                                                                                    |
| 6      | RR_RING_EN         | <b>Enable CDM generate RX ring index by Round Rubin method for TOPS</b><br><br>0: RX ring index from PSE info<br><br>1: RX ring index generate by Round-Rubin                                                                                              |
| 1      | CDM_FS_SOF_WR_TIME | <b>CDM SOF information</b><br><br>The time CDM write the start-of-frame Information to async-fifo for XDMA3.0<br><br>0: CDM FS part SOF info write to FIFO after VLAN tag processing<br><br>1: CDM FS part SOF info write to FIFO after L2 data processing |
| 0      | UNTAG_EN           | <b>VLAN un-tag</b><br><br>Un-tag the egress packets which are transmitted from CDM to CPU<br><br>0: Disable<br><br>1: The first 4-byte VLAN tag after Source Address will be untagged                                                                      |

15101630 CDME1\_IG\_CTRL CDM VLAN control 81000000

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|
| Name  | CDM_TPID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Reset | 1        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| Name  |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    | STAG_EN |
| Type  |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |
| Reset |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       |

| Bit(s) | Name     | Description                                                                                                                                                                                                        |
|--------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | CDM_TPID | Inserted VLAN TPID                                                                                                                                                                                                 |
| 0      | STAG_EN  | <b>Special tag indication</b><br><br>Indicate that the received packet is carrying the special tag from CPU<br><br>0: No special tag inserted.<br><br>1: The first 2-byte after Source Address is the special tag. |

15101634 CDME1\_EG\_CTRL CDM egress control 00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16       |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0        |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | UNTAG_EN |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW       |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0        |

| Bit(s) | Name     | Description                                                                                                                                                                           |
|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0      | UNTAG_EN | <b>VLAN un-tag</b><br><br>Un-tag the egress packets which are transmitted from CDM to CPU<br><br>0: Disable<br><br>1: The first 4-byte VLAN tag after Source Address will be untagged |

**15101638 CDME1\_PPP\_GEN CDM PPPoE generation 00000000**

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|
| Name  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PPP_INS |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| Name  | SESS_ID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       |

| Bit(s) | Name    | Description            |
|--------|---------|------------------------|
| 16     | PPP_INS | PPPoE Header Insertion |
| 15:0   | SESS_ID | PPPoE Session ID       |

**1510163C CDMT\_IG\_CTRL CDM VLAN control 81000000**

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21     | 20 | 19 | 18 | 17         | 16           |
|-------|----------|----|----|----|----|----|----|----|----|----|--------|----|----|----|------------|--------------|
| Name  | CDM_TPID |    |    |    |    |    |    |    |    |    |        |    |    |    |            |              |
| Type  | RW       |    |    |    |    |    |    |    |    |    |        |    |    |    |            |              |
| Reset | 1        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0      | 0  | 0  | 0  | 0          | 0            |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5      | 4  | 3  | 2  | 1          | 0            |
| Name  |          |    |    |    |    |    |    |    |    |    | MD_CDM |    |    |    | UDPLITE_EN | TPORT_CLS_EN |
| Type  |          |    |    |    |    |    |    |    |    |    | RW     |    |    |    | RW         | RW           |
| Reset |          |    |    |    |    |    |    |    |    |    | 0      |    |    |    | 0          | 0            |

| Bit(s) | Name         | Description                                                                                                                           |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | CDM_TPID     | Inserted VLAN TPID                                                                                                                    |
| 5      | MD_CDM       | CDM connects to MDMA<br>1'b0: CDM does not connect to MDMA<br>1'b1: CDM connects to MDMA                                              |
| 1      | UDPLITE_EN   | udplite enable for CDM parser<br>1'b0: CDM3.0 disable udplite parsing<br>1'b1: CDM3.0 enable udplite parsing                          |
| 0      | TPORT_CLS_EN | CDM through port enable the CLS function<br>1'b0: CDM through port disable CLS function<br>1'b1: CDM through port enable CLS function |

15101640      CDMM IG\_CTRL      CDM VLAN control      81000000

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|
| Name  | CDM_TPID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Reset | 1        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| Name  |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    | STAG_EN |
| Type  |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |
| Reset |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       |

| Bit(s) | Name     | Description                                                                                                                                                                                                        |
|--------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | CDM_TPID | <b>Inserted VLAN TPID</b>                                                                                                                                                                                          |
| 0      | STAG_EN  | <b>Special tag indication</b><br><br>Indicate that the received packet is carrying the special tag from CPU<br><br>0: No special tag inserted.<br><br>1: The first 2-byte after Source Address is the special tag. |

15101644      CDMM\_EG\_CTRL      CDM egress control      00000002

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18               | 17               | 16           |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------|------------------|--------------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |                  |              |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |                  |              |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |                  |              |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2                | 1                | 0            |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    | TACK2<br>RING_ID | TACK2<br>RING_EN | UNTAG<br>_EN |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    | RW               | RW               | RW           |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                | 1                | 0            |

| Bit(s) | Name         | Description                                                                                                                                                                           |
|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2      | TACK2RING_ID | <b>Ring selection of TCP ACK to dedicate Rx Ring</b><br><br>0: Ring 0<br><br>1: Ring 1                                                                                                |
| 1      | TACK2RING_EN | <b>Enable TCP ACK to dedicate Rx Ring</b><br><br>0: Disable<br><br>1: Enable                                                                                                          |
| 0      | UNTAG_EN     | <b>VLAN un-tag</b><br><br>Un-tag the egress packets which are transmitted from CDM to CPU<br><br>0: Disable<br><br>1: The first 4-byte VLAN tag after Source Address will be untagged |



15101648      CDMM\_PPP\_GEN      CDM PPPoE generation      00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|
| Name  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PPP_INS |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| Name  | SESS_ID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       |

| Bit(s) | Name    | Description            |
|--------|---------|------------------------|
| 16     | PPP_INS | PPPoE Header Insertion |
| 15:0   | SESS_ID | PPPoE Session ID       |

| 1510164C | CDM_THRES0 |    |    |    | CDM threshold 0      |    |    |    |    |    |               |                 | 08000808             |    |    |    |
|----------|------------|----|----|----|----------------------|----|----|----|----|----|---------------|-----------------|----------------------|----|----|----|
| Bit      | 31         | 30 | 29 | 28 | 27                   | 26 | 25 | 24 | 23 | 22 | 21            | 20              | 19                   | 18 | 17 | 16 |
| Name     |            |    |    |    | cdma_high_threshold  |    |    |    |    |    |               |                 |                      |    |    |    |
| Type     |            |    |    |    | RW                   |    |    |    |    |    |               |                 |                      |    |    |    |
| Reset    |            |    |    |    | 1                    | 0  | 0  | 0  |    |    |               |                 |                      |    |    |    |
| Bit      | 15         | 14 | 13 | 12 | 11                   | 10 | 9  | 8  | 7  | 6  | 5             | 4               | 3                    | 2  | 1  | 0  |
| Name     |            |    |    |    | cdmw2_high_threshold |    |    |    |    |    | dfifo_gff_dis | cdmw_udplite_en | cdmw0_high_threshold |    |    |    |
| Type     |            |    |    |    | RW                   |    |    |    |    |    | RW            | RW              | RW                   |    |    |    |
| Reset    |            |    |    |    | 1                    | 0  | 0  | 0  |    |    | 0             | 0               | 1                    | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                                                                                        |
|--------|----------------------|------------------------------------------------------------------------------------------------------------------------------------|
| 27:24  | cdma_high_threshold  | <b>memory high threshold value</b><br>memory size: high_threshold*1KB                                                              |
| 11:8   | cdmw2_high_threshold | <b>memory high threshold value</b><br>memory size: high_threshold*1KB                                                              |
| 5      | dfifo_gff_dis        | <b>The DFIFO in CDM/GDM use extra memory when disable</b><br>0: Disable, DFIFO use extra mem<br>1: Enable, DFIFO use SRAM directly |
| 4      | cdmw_udplite_en      | <b>CDM for WDMA enable udplite parsing</b><br>0: CDM for WDMA disable udplite parsing<br>1: CDM for WDMA enable udplite parsing    |
| 3:0    | cdmw0_high_threshold | <b>memory high threshold value</b><br>memory size: high_threshold*1KB                                                              |

15101650      CDM\_THRES1      CDM threshold 1      00000088

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                  | 22 | 21 | 20 | 19                   | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|---------------------|----|----|----|----------------------|----|----|----|
| Name  |    |    |    |    |    |    |    |    |                     |    |    |    |                      |    |    |    |
| Type  |    |    |    |    |    |    |    |    |                     |    |    |    |                      |    |    |    |
| Reset |    |    |    |    |    |    |    |    |                     |    |    |    |                      |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                   | 6  | 5  | 4  | 3                    | 2  | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    | cdmt_high_threshold |    |    |    | cdmw1_high_threshold |    |    |    |
| Type  |    |    |    |    |    |    |    |    | RW                  |    |    |    | RW                   |    |    |    |
| Reset |    |    |    |    |    |    |    |    | 1                   | 0  | 0  | 0  | 1                    | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                                           |
|--------|----------------------|-----------------------------------------------------------------------|
| 7:4    | cdmt_high_threshold  | <b>memory high threshold value</b><br>memory size: high_threshold*1KB |
| 3:0    | cdmw1_high_threshold | <b>memory high threshold value</b><br>memory size: high_threshold*1KB |

**15101654**      **CDM\_THRES2**      **CDM threshold 2**      **00006E08**

| Bit   | 31  | 30 | 29 | 28 | 27                   | 26 | 25 | 24 | 23                   | 22 | 21 | 20 | 19                   | 18 | 17 | 16 |
|-------|-----|----|----|----|----------------------|----|----|----|----------------------|----|----|----|----------------------|----|----|----|
| Name  |     |    |    |    |                      |    |    |    |                      |    |    |    |                      |    |    |    |
| Type  |     |    |    |    |                      |    |    |    |                      |    |    |    |                      |    |    |    |
| Reset |     |    |    |    |                      |    |    |    |                      |    |    |    |                      |    |    |    |
| Bit   | 15  | 14 | 13 | 12 | 11                   | 10 | 9  | 8  | 7                    | 6  | 5  | 4  | 3                    | 2  | 1  | 0  |
| Name  | REV |    |    |    | cdme2_high_threshold |    |    |    | cdme1_high_threshold |    |    |    | cdme0_high_threshold |    |    |    |
| Type  | RW  |    |    |    | RW                   |    |    |    | RW                   |    |    |    | RW                   |    |    |    |
| Reset | 0   | 1  | 1  | 0  | 1                    | 1  | 1  | 0  | 0                    | 0  | 0  | 0  | 1                    | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                        |
|--------|----------------------|----------------------------------------------------|
| 15:12  | REV                  | <b>Reserved</b><br>memory size: high_threshold*1KB |
| 11:8   | cdme2_high_threshold | <b>Reserved</b><br>memory size: high_threshold*1KB |
| 7:4    | cdme1_high_threshold | <b>Reserved</b><br>memory size: high_threshold*1KB |
| 3:0    | cdme0_high_threshold | <b>Reserved</b><br>memory size: high_threshold*1KB |

**15101658**      **CDM\_THRES3**      **CDM threshold 3**      **00000008**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19                    | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|-----------------------|----|----|----|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |                       |    |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |                       |    |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |                       |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3                     | 2  | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    | cdmeip_high_threshold |    |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    | RW                    |    |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    | 1                     | 0  | 0  | 0  |

| Bit(s) | Name                  | Description                                                           |
|--------|-----------------------|-----------------------------------------------------------------------|
| 3:0    | cdmeip_high_threshold | <b>memory high threshold value</b><br>memory size: high_threshold*1KB |

**1510165C CDM\_THRES4 CDM threshold 4 00000008**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|---------------------|----|----|----|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |                     |    |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |                     |    |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |                     |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    | cdmm_high_threshold |    |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    | RW                  |    |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    | 1                   | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                                    |
|--------|---------------------|----------------------------------------------------------------|
| 3:0    | cdmm_high_threshold | memory high threshold value<br>memory size: high_threshold*1KB |

**151016A8 CDMW2\_IG\_CTRL CDM VLAN control 81000000**

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21     | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|
| Name  | CDM_TPID |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |
| Reset | 1        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0      | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5      | 4  | 3  | 2  | 1  | 0  |
| Name  |          |    |    |    |    |    |    |    |    |    | MD_CDM |    |    |    |    |    |
| Type  |          |    |    |    |    |    |    |    |    |    | RW     |    |    |    |    |    |
| Reset |          |    |    |    |    |    |    |    |    |    | 0      |    |    |    |    |    |

| Bit(s) | Name     | Description                                                                              |
|--------|----------|------------------------------------------------------------------------------------------|
| 31:16  | CDM_TPID | Inserted VLAN TPID                                                                       |
| 5      | MD_CDM   | CDM connects to MDMA<br>1'b0: CDM does not connect to MDMA<br>1'b1: CDM connects to MDMA |

151016AC CDMW2 EG\_CTRL CDM egress control 00000182

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24          | 23 | 22         | 21 | 20 | 19 | 18 | 17                 | 16       |
|-------|----|----|----|----|----|----|----|-------------|----|------------|----|----|----|----|--------------------|----------|
| Name  |    |    |    |    |    |    |    |             |    |            |    |    |    |    |                    |          |
| Type  |    |    |    |    |    |    |    |             |    |            |    |    |    |    |                    |          |
| Reset |    |    |    |    |    |    |    |             |    |            |    |    |    |    |                    |          |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8           | 7  | 6          | 5  | 4  | 3  | 2  | 1                  | 0        |
| Name  |    |    |    |    |    |    |    | RR_RING_NUM |    | RR_RING_EN |    |    |    |    | CDM_FS_SOF_WR_TIME | UNTAG_EN |
| Type  |    |    |    |    |    |    |    | RW          |    | RW         |    |    |    |    | RW                 | RW       |
| Reset |    |    |    |    |    |    |    | 1           | 1  | 0          |    |    |    |    | 1                  | 0        |

| Bit(s) | Name               | Description                                                                                                                                                                                                                                                |
|--------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8:7    | RR_RING_NUM        | <b>Maximum Round Rubin ring index for CDM to generate RX ring index</b>                                                                                                                                                                                    |
| 6      | RR_RING_EN         | <b>Enable CDM generate RX ring index by Round Rubin method for TOPS</b><br><br>0: RX ring index from PSE info<br><br>1: RX ring index generate by Round-Rubin                                                                                              |
| 1      | CDM_FS_SOF_WR_TIME | <b>CDM SOF information</b><br><br>The time CDM write the start-of-frame Information to async-fifo for XDMA3.0<br><br>0: CDM FS part SOF info write to FIFO after VLAN tag processing<br><br>1: CDM FS part SOF info write to FIFO after L2 data processing |
| 0      | UNTAG_EN           | <b>VLAN un-tag</b><br><br>Un-tag the egress packets which are transmitted from CDM to CPU<br><br>0: Disable<br><br>1: The first 4-byte VLAN tag after Source Address will be untagged                                                                      |

**151016B0 CDMW2\_PPP\_GEN CDM PPPoE generation 00000000**

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|
| Name  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PPP_INS |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| Name  | SESS_ID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       |

| Bit(s) | Name    | Description            |
|--------|---------|------------------------|
| 16     | PPP_INS | PPPoE Header Insertion |
| 15:0   | SESS_ID | PPPoE Session ID       |

**151016B4 CDME2\_IG\_CTRL CDM VLAN control 81000000**

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|
| Name  | CDM_TPID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Reset | 1        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| Name  |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    | STAG_EN |
| Type  |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |
| Reset |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       |

| Bit(s) | Name     | Description                                                            |
|--------|----------|------------------------------------------------------------------------|
| 31:16  | CDM_TPID | Inserted VLAN TPID                                                     |
| 0      | STAG_EN  | Special tag indication                                                 |
|        |          | Indicate that the received packet is carrying the special tag from CPU |
|        |          | 0: No special tag inserted.                                            |
|        |          | 1: The first 2-byte after Source Address is the special tag.           |

**151016B8**      **CDME2\_EG\_CTRL**      **CDM egress control**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16       |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0        |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | UNTAG_EN |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW       |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0        |

| Bit(s) | Name     | Description                                                                                                                                                               |
|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0      | UNTAG_EN | <b>VLAN un-tag</b><br>Un-tag the egress packets which are transmitted from CDM to CPU<br>0: Disable<br>1: The first 4-byte VLAN tag after Source Address will be untagged |

**151016BC**      **CDME2\_PPP\_GEN**      **CDM PPPoE generation**      **00000000**

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|
| Name  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PPP_INS |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| Name  | SESS_ID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       |

| Bit(s) | Name    | Description                   |
|--------|---------|-------------------------------|
| 16     | PPP_INS | <b>PPPoE Header Insertion</b> |
| 15:0   | SESS_ID | <b>PPPoE Session ID</b>       |



151016C0      CDMEIP IG\_CTRL      CDM VLAN control      81000000

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21     | 20 | 19 | 18 | 17         | 16           |
|-------|----------|----|----|----|----|----|----|----|----|----|--------|----|----|----|------------|--------------|
| Name  | CDM_TPID |    |    |    |    |    |    |    |    |    |        |    |    |    |            |              |
| Type  | RW       |    |    |    |    |    |    |    |    |    |        |    |    |    |            |              |
| Reset | 1        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0      | 0  | 0  | 0  | 0          | 0            |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5      | 4  | 3  | 2  | 1          | 0            |
| Name  |          |    |    |    |    |    |    |    |    |    | MD_CDM |    |    |    | UDPLITE_EN | TPORT_CLS_EN |
| Type  |          |    |    |    |    |    |    |    |    |    | RW     |    |    |    | RW         | RW           |
| Reset |          |    |    |    |    |    |    |    |    |    | 0      |    |    |    | 0          | 0            |

| Bit(s) | Name         | Description                                                                                                                                    |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | CDM_TPID     | Inserted VLAN TPID                                                                                                                             |
| 5      | MD_CDM       | <b>CDM connect to MDMA</b><br>1'b0: CDM does not connect to MDMA<br>1'b1: CDM connects to MDMA                                                 |
| 1      | UDPLITE_EN   | <b>udplite enable for CDM parser</b><br>1'b0: CDM3.0 disables udplite parsing<br>1'b1: CDM3.0 enables udplite parsing                          |
| 0      | TPORT_CLS_EN | <b>CDM through port enable the CLS function</b><br>1'b0: CDM through port disables CLS function<br>1'b1: CDM through port enables CLS function |

151016C4 CDMEIP\_EG\_CTRL CDM egress control 00000002

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22         | 21 | 20 | 19 | 18 | 17                 | 16       |
|-------|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|--------------------|----------|
| Name  |    |    |    |    |    |    |    |    |    |            |    |    |    |    |                    |          |
| Type  |    |    |    |    |    |    |    |    |    |            |    |    |    |    |                    |          |
| Reset |    |    |    |    |    |    |    |    |    |            |    |    |    |    |                    |          |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6          | 5  | 4  | 3  | 2  | 1                  | 0        |
| Name  |    |    |    |    |    |    |    |    |    | RR_RING_EN |    |    |    |    | CDM_FS_SOF_WR_TIME | UNTAG_EN |
| Type  |    |    |    |    |    |    |    |    |    | RW         |    |    |    |    | RW                 | RW       |
| Reset |    |    |    |    |    |    |    |    |    | 0          |    |    |    |    | 1                  | 0        |

| Bit(s) | Name               | Description                                                                                                                                                                                                                                                       |
|--------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6      | RR_RING_EN         | <p><b>Enable CDM generate RX ring index by Round Rubin method for TOPS</b></p> <p>0: RX ring index from PSE info</p> <p>1: RX ring index generate by Round-Rubin</p>                                                                                              |
| 1      | CDM_FS_SOF_WR_TIME | <p><b>CDM SOF information</b></p> <p>The time CDM write the start-of-frame Information to async-fifo for XDMA3.0</p> <p>0: CDM FS part SOF info write to FIFO after VLAN tag processing</p> <p>1: CDM FS part SOF info write to FIFO after L2 data processing</p> |
| 0      | UNTAG_EN           | <p><b>VLAN un-tag</b></p> <p>Un-tag the egress packets which are transmitted from CDM to CPU</p> <p>0: Disable</p> <p>1: The first 4-byte VLAN tag after Source Address will be untagged</p>                                                                      |

151016C8      CDMEIP\_PPP\_GEN      CDM PPPoE generation      00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|
| Name  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PPP_INS |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| Name  | SESS_ID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       |

| Bit(s) | Name    | Description            |
|--------|---------|------------------------|
| 16     | PPP_INS | PPPoE Header Insertion |
| 15:0   | SESS_ID | PPPoE Session ID       |

**15102800 RSS\_GLO\_CFG RSS global configuration 1F1F3370**

| Bit   | 31 | 30        | 29 | 28            | 27 | 26        | 25 | 24 | 23 | 22            | 21 | 20            | 19          | 18          | 17        | 16         |
|-------|----|-----------|----|---------------|----|-----------|----|----|----|---------------|----|---------------|-------------|-------------|-----------|------------|
| Name  |    |           |    | IPV4_TUPLE_EN |    |           |    |    |    |               |    | IPV6_TUPLE_EN |             |             |           |            |
| Type  |    |           |    | RW            |    |           |    |    |    |               |    | RW            |             |             |           |            |
| Reset |    |           |    | 1             | 1  | 1         | 1  | 1  |    |               |    | 1             | 1           | 1           | 1         | 1          |
| Bit   | 15 | 14        | 13 | 12            | 11 | 10        | 9  | 8  | 7  | 6             | 5  | 4             | 3           | 2           | 1         | 0          |
| Name  |    | IPV4_TYPE |    |               |    | IPV6_TYPE |    |    |    | INDR_TBL_SIZE |    |               | RSS_CFG_RDY | RSS_CFG_REQ | RSS_B_USY | RSS_ENABLE |
| Type  |    | RW        |    |               |    | RW        |    |    |    | RW            |    |               | RO          | RW          | RO        | RW         |
| Reset |    | 0         | 1  | 1             |    | 0         | 1  | 1  |    | 1             | 1  | 1             | 0           | 0           | 0         | 0          |

| Bit(s) | Name          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|--------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 28:24  | IPV4_TUPLE_EN | <p><b>IPv4 Hash Tuple Global Enable</b></p> <p>This field controls which hash tuple is valid for IPv4 hash calculation. The invalid(disabled) tuple can be seem as 0x0 when calculating HASH.</p> <p>For example, when SIP is disabled, 2-tuple and 4-tuple hash will not consider SIP. Another example, when DPORT is disabled, 4-tuple hash will not consider DPORT.</p> <p>Bit Maps: {DPROT,SPORT,DIP,SIP,Reserved}</p> <p>Set the bits to 1 to enable corresponding hash tuple for hash calculation.</p> <p>Set the bits to 0 to disable corresponding hash tuple for hash calculation.</p> <p>5'b00000: Disable All</p> <p>5'b00010: Enable SIP for HASH</p> <p>5'b00100: Enable DIP for HASH</p> <p>5'b01000: Enable SPORT for HASH</p> <p>5'b10000: Enable DPORT for HASH</p> <p>5'b11111: Enable DPORT,SPORT,DIP,SIP for HASH</p> <p>Others: Combinations of the above hash tuple</p> |
| 20:16  | IPV6_TUPLE_EN | <p><b>IPv6 Hash Tuple Global Enable</b></p> <p>This field controls which hash tuple is valid for IPv6 hash calculation.</p> <p>See description of IPV4_TUPLE_EN for more detail.</p> <p>Bit Maps: {DPROT,SPORT,DIP,SIP,Reserved}</p> <p>Set the bits to 1 to enable corresponding hash tuple for hash calculation.</p> <p>Set the bits to 0 to disable corresponding hash tuple for hash calculation.</p> <p>5'b00000: Disable All</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

| Bit(s) | Name      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|--------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |           | 5'b00010: Enable SIP for HASH                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|        |           | 5'b00100: Enable DIP for HASH                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|        |           | 5'b01000: Enable SPORT for HASH                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|        |           | 5'b10000: Enable DPORT for HASH                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|        |           | 5'b11111: Enable DPORT,SPORT,DIP,SIP for HASH                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|        |           | Others: Combinations of the above hash tuple                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 14:12  | IPV4_TYPE | <p><b>IPv4 Hash Type Selection Flag</b></p> <p>This field controls the selection of hash 2-tuple and 4-tuple for different kinds of IPv4 packet.</p> <p>Bit Maps: {UDP 4-tuple,TCP4-tuple,IP 2-tuple}</p> <p>RSS performs the hash calculations as specified for the enabled case.</p> <p>For example, IPV4_TYPE=3'b011, RSS will use 4-tuple hash for IPv4 TCP packets and 2-tuple hash for IPv4 non-TCP packets (such as IPv4 fragment packet).</p> <p>3'b000: Disable IPv4 packets for RSS. RSS does not accept IPv4 packets</p> <p>3'b001: Enable IPv4 2-tuple hash</p> <p>3'b010: Enable TCP 4-tuple hash</p> <p>3'b100: Enable UDP 4-tuple hash</p> <p>3'b011: Enable IPv4 2-tuple hash + TCP 4-tuple hash</p> <p>3'b101: Enable IPv4 2-tuple hash + UDP 4-tuple hash</p> <p>3'b110: TCP 4-tuple hash + UDP 4-tuple hash</p> <p>3'b111: IPv4 2-tuple hash + TCP 4-tuple hash + UDP 4-tuple hash</p> |
| 10:8   | IPV6_TYPE | <p><b>IPv6 Hash Type Selection Flag</b></p> <p>This field controls the selection of hash 2-tuple and 4-tuple for different kinds of IPv6 packet.</p> <p>Bit Maps: {UDP 4-tuple,TCP4-tuple,IP 2-tuple}</p> <p>See description of IPV4_TYPE for more detail.</p> <p>3'b000: Disable IPv6 packets for RSS. RSS does not accept IPv4 packets</p> <p>3'b001: Enable IPv6 2-tuple hash</p> <p>3'b010: Enable TCP 4-tuple hash</p> <p>3'b100: Enable UDP 4-tuple hash</p> <p>3'b011: Enable IPv6 2-tuple hash + TCP 4-tuple hash</p> <p>3'b101: Enable IPv6 2-tuple hash + UDP 4-tuple hash</p>                                                                                                                                                                                                                                                                                                                  |

| Bit(s) | Name          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|--------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |               | 3'b110: TCP 4-tuple hash + UDP 4-tuple hash                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|        |               | 3'b111: IPv6 2-tuple hash + TCP 4-tuple hash + UDP 4-tuple hash                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 6:4    | INDR_TBL_SIZE | <p><b>Change the size of indirection table.</b></p> <p>This register field affects how many bits of hash result will be used as the entry of indirection table.</p> <p>For example, INDR_TBL_SIZE=6 means RSS use only 6 bits of hash result as indirection table entry, which also means that indirection table has <math>2^6=64</math> entries.</p> <p>3'd1: Indirection table size = 2 entries</p> <p>3'd2: Indirection table size = 4 entries</p> <p>3'd3: Indirection table size = 8 entries</p> <p>3'd4: Indirection table size = 16 entries</p> <p>3'd5: Indirection table size = 32 entries</p> <p>3'd6: Indirection table size = 64 entries</p> <p>3'd7: Indirection table size = 128 entries</p> <p>Other: Invalid value</p> |
| 3      | RSS_CFG_RDY   | <p><b>RSS is ready to accept new register configuration.</b></p> <p>This register will be asserted after RSS accepted the request from RSS_CFG_REQ. See description of RSS_CFG_REQ for more detail.</p> <p>0: Not Ready</p> <p>1: Ready</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 2      | RSS_CFG_REQ   | <p><b>Request to change RSS register configuration.</b></p> <p>When Request asserted, RSS will be paused after the process of current packet has finished. It is worth to notice that assert RSS_CFG_REQ is required before enable RSS or changing other register setting(such as indirection table). Must wait RSS_CFG_RDY=1 before changing RSS register value(including RSS_ENABLE).</p> <p>0: Request deassert</p> <p>1: Request assert</p>                                                                                                                                                                                                                                                                                        |
| 1      | RSS_BUSY      | <p><b>RSS is working or not</b></p> <p>0: RSS IDLE</p> <p>1: RSS BUSY</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 0      | RSS_ENABLE    | <p><b>Enable/Disable RSS</b></p> <p>0: Disable RSS</p> <p>1: Enable RSS</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

| Bit(s) | Name | Description |
|--------|------|-------------|
|--------|------|-------------|

**15102820**      **RSS\_HASH\_KEY\_DW0**      **RSS hash Key DW0**      **BEAC01FA**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | HASH_KEY_DW0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1            | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HASH_KEY_DW0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 0  |

| Bit(s) | Name         | Description       |
|--------|--------------|-------------------|
| 31:0   | HASH_KEY_DW0 | Hash Key bit 31~0 |

**15102824**      **RSS\_HASH\_KEY\_DW1**      **RSS hash Key DW1**      **6A42B73B**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | HASH_KEY_DW1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HASH_KEY_DW1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1            | 0  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 0  | 1  | 1  | 1  | 0  | 1  | 1  |

| Bit(s) | Name         | Description        |
|--------|--------------|--------------------|
| 31:0   | HASH_KEY_DW1 | Hash Key bit 63~32 |

**15102828**      **RSS\_HASH\_KEY\_DW2**      **RSS hash Key DW2**      **8030F20C**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | HASH_KEY_DW2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HASH_KEY_DW2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1            | 1  | 1  | 1  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  |

| Bit(s) | Name         | Description        |
|--------|--------------|--------------------|
| 31:0   | HASH_KEY_DW2 | Hash Key bit 95~64 |

**1510282C**      **RSS\_HASH\_KEY\_DW3**      **RSS hash Key DW3**      **77CB2DA3**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | HASH_KEY_DW3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 0  | 1  | 0  | 1  | 1  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HASH_KEY_DW3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 1  | 0  | 1  | 0  | 0  | 0  | 1  | 1  |

| Bit(s) | Name         | Description         |
|--------|--------------|---------------------|
| 31:0   | HASH_KEY_DW3 | Hash Key bit 127~96 |

**15102830**      **RSS\_HASH\_KEY\_DW4**      **RSS hash Key DW4**      **AE7B30B4**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | HASH_KEY_DW4 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1            | 0  | 1  | 0  | 1  | 1  | 1  | 0  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 1  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HASH_KEY_DW4 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 0  | 0  |

| Bit(s) | Name         | Description          |
|--------|--------------|----------------------|
| 31:0   | HASH_KEY_DW4 | Hash Key bit 159~128 |



**15102834**      **RSS\_HASH\_KEY\_DW5**      **RSS hash Key DW5**      **D0CA2BCB**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | HASH_KEY_DW5 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1            | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 0  | 1  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HASH_KEY_DW5 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 0  | 1  | 0  | 1  | 1  |

| Bit(s) | Name         | Description          |
|--------|--------------|----------------------|
| 31:0   | HASH_KEY_DW5 | Hash Key bit 191~160 |

**15102838**      **RSS\_HASH\_KEY\_DW6**      **RSS hash Key DW6**      **43A38FB0**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | HASH_KEY_DW6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 1  | 0  | 0  | 0  | 1  | 1  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HASH_KEY_DW6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1            | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description          |
|--------|--------------|----------------------|
| 31:0   | HASH_KEY_DW6 | Hash Key bit 223~192 |

**1510283C**      **RSS\_HASH\_KEY\_DW7**      **RSS hash Key DW7**      **4167253D**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | HASH_KEY_DW7 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 0  | 1  | 1  | 1  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HASH_KEY_DW7 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 1  | 1  | 1  | 0  | 1  |

| Bit(s) | Name         | Description          |
|--------|--------------|----------------------|
| 31:0   | HASH_KEY_DW7 | Hash Key bit 255~224 |

**15102840**      **RSS\_HASH\_KEY\_DW8**      **RSS hash Key DW8**      **255B0EC2**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | HASH_KEY_DW8 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 1  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HASH_KEY_DW8 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 1  | 0  |

| Bit(s) | Name         | Description          |
|--------|--------------|----------------------|
| 31:0   | HASH_KEY_DW8 | Hash Key bit 287~256 |

**15102844**      **RSS\_HASH\_KEY\_DW9**      **RSS hash Key DW9**      **6D5A56DA**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | HASH_KEY_DW9 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 1  | 1  | 0  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HASH_KEY_DW9 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 1  | 0  | 1  | 1  | 0  | 1  | 0  |

| Bit(s) | Name         | Description          |
|--------|--------------|----------------------|
| 31:0   | HASH_KEY_DW9 | Hash Key bit 319~288 |

**15102848**      **RSS\_LFB\_CFG0**      **RSS low flow balance configuration 0**      **00C7FF02**

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18              | 17                    | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|-----------------|-----------------------|----|
| Name  | TICK_TIMER |    |    |    |    |    |    |    |    |    |    |    |    |                 |                       |    |
| Type  | RW         |    |    |    |    |    |    |    |    |    |    |    |    |                 |                       |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 1               | 1                     | 1  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2               | 1                     | 0  |
| Name  | AGE_TIMER  |    |    |    |    |    |    |    |    |    |    |    |    | CMP_T<br>CP_UDP | CMP_I<br>PV4_IP<br>V6 | EN |
| Type  | RW         |    |    |    |    |    |    |    |    |    |    |    |    | RW              | RW                    | RW |
| Reset | 1          | 1  | 1  | 1  | 1  | 1  | 1  | 1  |    |    |    |    |    | 0               | 1                     | 0  |

| Bit(s) | Name          | Description                                                                                                                                                                                                                                                                                           |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | TICK_TIMER    | <b>Low Flow balance Table Age Tick Timer</b><br><br>An internal generated timeout timer based on 20us tick time. When timeout, it will trigger a tick to age timer to count forward.<br><br>If set to zero: tick timer is disabled and the trigger of age timer is the copy of raw 20us tick instead. |
| 15:8   | AGE_TIMER     | <b>Low Flow balance Table Age Timer</b><br><br>Entry ageout timer of low flow balance table.<br><br>The applied age out timer is equal to (AGE_TIMER+1)*(TICK_TIMER)*20us                                                                                                                             |
| 2      | CMP_TCP_UDP   | <b>Low Flow balance Table TCP/UDP Flow Compare</b><br><br>When enabled, TCP flow and UDP flow will be seen as different flow even if the two have the same DPORT and SPORT.<br><br>0: Disable<br><br>1: Enable                                                                                        |
| 1      | CMP_IPV4_IPV6 | <b>Low Flow balance Table IPv4/IPv6 Flow Compare</b><br><br>When enabled, IPv4 flow and IPv6 flow will be seen as different flow even if the two have the same DIP and SIP.<br><br>0: Disable<br><br>1: Enable                                                                                        |
| 0      | EN            | <b>Low Flow balance Table Enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                               |

**15102850**      **RSS INDR\_TABLE\_DW0**      **RSS indirection table DW0**      **DEADBEEF**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | INDR_TABLE_DW0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | INDR_TABLE_DW0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name           | Description                                          |
|--------|----------------|------------------------------------------------------|
| 31:0   | INDR_TABLE_DW0 | Indirection Table Entry 15~0<br>Each entry has 2bits |

**15102854**      **RSS INDR\_TABLE\_DW1**      **RSS indirection table DW1**      **DEADBEEF**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | INDR_TABLE_DW1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | INDR_TABLE_DW1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name           | Description                                           |
|--------|----------------|-------------------------------------------------------|
| 31:0   | INDR_TABLE_DW1 | Indirection Table Entry 31~16<br>Each entry has 2bits |

**15102858**      **RSS INDR\_TABLE\_DW2**      **RSS indirection table DW2**      **DEADBEEF**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | INDR_TABLE_DW2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | INDR_TABLE_DW2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name | Description |
|--------|------|-------------|
|--------|------|-------------|

|      |                |                               |
|------|----------------|-------------------------------|
| 31:0 | INDR_TABLE_DW2 | Indirection Table Entry 47~32 |
|------|----------------|-------------------------------|

Each entry has 2bits

**1510285C**      **RSS INDR\_TABLE\_DW3**      **RSS indirection table DW3**      **DEADBEEF**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | INDR_TABLE_DW3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | INDR_TABLE_DW3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name | Description |
|--------|------|-------------|
|--------|------|-------------|

|      |                |                               |
|------|----------------|-------------------------------|
| 31:0 | INDR_TABLE_DW3 | Indirection Table Entry 63~48 |
|------|----------------|-------------------------------|

Each entry has 2bits

**15102860**      **RSS INDR\_TABLE\_DW4**      **RSS indirection table DW4**      **DEADBEEF**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | INDR_TABLE_DW4 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | INDR_TABLE_DW4 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name           | Description                                           |
|--------|----------------|-------------------------------------------------------|
| 31:0   | INDR_TABLE_DW4 | Indirection Table Entry 79~64<br>Each entry has 2bits |

**15102864**      **RSS INDR\_TABLE\_DW5**      **RSS indirection table DW5**      **DEADBEEF**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | INDR_TABLE_DW5 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | INDR_TABLE_DW5 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name           | Description                                           |
|--------|----------------|-------------------------------------------------------|
| 31:0   | INDR_TABLE_DW5 | Indirection Table Entry 95~80<br>Each entry has 2bits |

**15102868**      **RSS INDR\_TABLE\_DW6**      **RSS indirection table DW6**      **DEADBEEF**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | INDR_TABLE_DW6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | INDR_TABLE_DW6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name           | Description                                            |
|--------|----------------|--------------------------------------------------------|
| 31:0   | INDR_TABLE_DW6 | Indirection Table Entry 111~96<br>Each entry has 2bits |

**1510286C**      **RSS INDR\_TABLE\_DW7**      **RSS indirection table DW7**      **DEADBEEF**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | INDR_TABLE_DW7 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | INDR_TABLE_DW7 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name           | Description                                             |
|--------|----------------|---------------------------------------------------------|
| 31:0   | INDR_TABLE_DW7 | Indirection Table Entry 127~112<br>Each entry has 2bits |

## 4.4 QDMA

### 4.4.1 Register Definition

Module name: QDMA Base address: (+0x15104400)

| Address  | Name               | Width | Register Function                          |
|----------|--------------------|-------|--------------------------------------------|
| 15104400 | <u>QTX_CFG_0</u>   | 32    | TX queue #0, #(16 * n) configuration       |
| 15104404 | <u>QTX_SCH_0</u>   | 32    | TX queue #0, #(16 * n) schedule            |
| 15104408 | <u>QTX_HEAD_0</u>  | 32    | TX queue #0, #(16 * n) head pointer        |
| 1510440C | <u>QTX_TAIL_0</u>  | 32    | TX queue #0, #(16 * n) tail pointer        |
| 15104410 | <u>QTX_CFG_1</u>   | 32    | TX queue #1, #(16 * n + 1) configuration   |
| 15104414 | <u>QTX_SCH_1</u>   | 32    | TX queue #1, #(16 * n + 1) schedule        |
| 15104418 | <u>QTX_HEAD_1</u>  | 32    | TX queue #1, #(16 * n + 1) head pointer    |
| 1510441C | <u>QTX_TAIL_1</u>  | 32    | TX queue #1, #(16 * n + 1) tail pointer    |
| 15104420 | <u>QTX_CFG_2</u>   | 32    | TX queue #2, #(16 * n + 2) configuration   |
| 15104424 | <u>QTX_SCH_2</u>   | 32    | TX queue #2, #(16 * n + 2) schedule        |
| 15104428 | <u>QTX_HEAD_2</u>  | 32    | TX queue #2, #(16 * n + 2) head pointer    |
| 1510442C | <u>QTX_TAIL_2</u>  | 32    | TX queue #2, #(16 * n + 2) tail pointer    |
| 15104430 | <u>QTX_CFG_3</u>   | 32    | TX queue #3, #(16 * n + 3) configuration   |
| 15104434 | <u>QTX_SCH_3</u>   | 32    | TX queue #3, #(16 * n + 3) schedule        |
| 15104438 | <u>QTX_HEAD_3</u>  | 32    | TX queue #3, #(16 * n + 3) head pointer    |
| 1510443C | <u>QTX_TAIL_3</u>  | 32    | TX queue #3, #(16 * n + 3) tail pointer    |
| 15104440 | <u>QTX_CFG_4</u>   | 32    | TX queue #4, #(16 * n + 4) configuration   |
| 15104444 | <u>QTX_SCH_4</u>   | 32    | TX queue #4, #(16 * n + 4) schedule        |
| 15104448 | <u>QTX_HEAD_4</u>  | 32    | TX queue #4, #(16 * n + 4) head pointer    |
| 1510444C | <u>QTX_TAIL_4</u>  | 32    | TX queue #4, #(16 * n + 4) tail pointer    |
| 15104450 | <u>QTX_CFG_5</u>   | 32    | TX queue #5, #(16 * n + 5) configuration   |
| 15104454 | <u>QTX_SCH_5</u>   | 32    | TX queue #5, #(16 * n + 5) schedule        |
| 15104458 | <u>QTX_HEAD_5</u>  | 32    | TX queue #5, #(16 * n + 5) head pointer    |
| 1510445C | <u>QTX_TAIL_5</u>  | 32    | TX queue #5, #(16 * n + 5) tail pointer    |
| 15104460 | <u>QTX_CFG_6</u>   | 32    | TX queue #6, #(16 * n + 6) configuration   |
| 15104464 | <u>QTX_SCH_6</u>   | 32    | TX queue #6, #(16 * n + 6) schedule        |
| 15104468 | <u>QTX_HEAD_6</u>  | 32    | TX queue #6, #(16 * n + 6) head pointer    |
| 1510446C | <u>QTX_TAIL_6</u>  | 32    | TX queue #6, #(16 * n + 6) tail pointer    |
| 15104470 | <u>QTX_CFG_7</u>   | 32    | TX queue #7, #(16 * n + 7) configuration   |
| 15104474 | <u>QTX_SCH_7</u>   | 32    | TX queue #7, #(16 * n + 7) schedule        |
| 15104478 | <u>QTX_HEAD_7</u>  | 32    | TX queue #7, #(16 * n + 7) head pointer    |
| 1510447C | <u>QTX_TAIL_7</u>  | 32    | TX queue #7, #(16 * n + 7) tail pointer    |
| 15104480 | <u>QTX_CFG_8</u>   | 32    | TX queue #8, #(16 * n + 8) configuration   |
| 15104484 | <u>QTX_SCH_8</u>   | 32    | TX queue #8, #(16 * n + 8) schedule        |
| 15104488 | <u>QTX_HEAD_8</u>  | 32    | TX queue #8, #(16 * n + 8) head pointer    |
| 1510448C | <u>QTX_TAIL_8</u>  | 32    | TX queue #8, #(16 * n + 8) tail pointer    |
| 15104490 | <u>QTX_CFG_9</u>   | 32    | TX queue #9, #(16 * n + 9) configuration   |
| 15104494 | <u>QTX_SCH_9</u>   | 32    | TX queue #9, #(16 * n + 9) schedule        |
| 15104498 | <u>QTX_HEAD_9</u>  | 32    | TX queue #9, #(16 * n + 9) head pointer    |
| 1510449C | <u>QTX_TAIL_9</u>  | 32    | TX queue #9, #(16 * n + 9) tail pointer    |
| 151044A0 | <u>QTX_CFG_10</u>  | 32    | TX queue #10, #(16 * n + 10) configuration |
| 151044A4 | <u>QTX_SCH_10</u>  | 32    | TX queue #10, #(16 * n + 10) schedule      |
| 151044A8 | <u>QTX_HEAD_10</u> | 32    | TX queue #10, #(16 * n + 10) head pointer  |



| Address  | Name                  | Width | Register Function                             |
|----------|-----------------------|-------|-----------------------------------------------|
| 151044AC | <u>QTX TAIL 10</u>    | 32    | TX queue #10, $\#(16 * n + 10)$ tail pointer  |
| 151044B0 | <u>QTX CFG 11</u>     | 32    | TX queue #11, $\#(16 * n + 11)$ configuration |
| 151044B4 | <u>QTX SCH 11</u>     | 32    | TX queue #11, $\#(16 * n + 11)$ schedule      |
| 151044B8 | <u>QTX HEAD 11</u>    | 32    | TX queue #11, $\#(16 * n + 11)$ head pointer  |
| 151044BC | <u>QTX TAIL 11</u>    | 32    | TX queue #11, $\#(16 * n + 11)$ tail pointer  |
| 151044C0 | <u>QTX CFG 12</u>     | 32    | TX queue #12, $\#(16 * n + 12)$ configuration |
| 151044C4 | <u>QTX SCH 12</u>     | 32    | TX queue #12, $\#(16 * n + 12)$ schedule      |
| 151044C8 | <u>QTX HEAD 12</u>    | 32    | TX queue #12, $\#(16 * n + 12)$ head pointer  |
| 151044CC | <u>QTX TAIL 12</u>    | 32    | TX queue #12, $\#(16 * n + 12)$ tail pointer  |
| 151044D0 | <u>QTX CFG 13</u>     | 32    | TX queue #13, $\#(16 * n + 13)$ configuration |
| 151044D4 | <u>QTX SCH 13</u>     | 32    | TX queue #13, $\#(16 * n + 13)$ schedule      |
| 151044D8 | <u>QTX HEAD 13</u>    | 32    | TX queue #13, $\#(16 * n + 13)$ head pointer  |
| 151044DC | <u>QTX TAIL 13</u>    | 32    | TX queue #13, $\#(16 * n + 13)$ tail pointer  |
| 151044E0 | <u>QTX CFG 14</u>     | 32    | TX queue #14, $\#(16 * n + 14)$ configuration |
| 151044E4 | <u>QTX SCH 14</u>     | 32    | TX queue #14, $\#(16 * n + 14)$ schedule      |
| 151044E8 | <u>QTX HEAD 14</u>    | 32    | TX queue #14, $\#(16 * n + 14)$ head pointer  |
| 151044EC | <u>QTX TAIL 14</u>    | 32    | TX queue #14, $\#(16 * n + 14)$ tail pointer  |
| 151044F0 | <u>QTX CFG 15</u>     | 32    | TX queue #15, $\#(16 * n + 15)$ configuration |
| 151044F4 | <u>QTX SCH 15</u>     | 32    | TX queue #15, $\#(16 * n + 15)$ schedule      |
| 151044F8 | <u>QTX HEAD 15</u>    | 32    | TX queue #15, $\#(16 * n + 15)$ head pointer  |
| 151044FC | <u>QTX TAIL 15</u>    | 32    | TX queue #15, $\#(16 * n + 15)$ tail pointer  |
| 15104500 | <u>QRX BASE PTR 0</u> | 32    | RX ring #0 base pointer                       |
| 15104504 | <u>QRX MAX CNT 0</u>  | 32    | RX ring #0 maximum count                      |
| 15104508 | <u>QRX CRX IDX 0</u>  | 32    | RX ring #0 CPU pointer                        |
| 1510450C | <u>QRX DRX IDX 0</u>  | 32    | RX ring #0 DMA pointer                        |
| 15104580 | <u>VQTX TB BASE 0</u> | 32    | TX virtual queue table #0 base address        |
| 15104584 | <u>VQTX TB BASE 1</u> | 32    | TX virtual queue table #1 base address        |
| 15104588 | <u>VQTX TB BASE 2</u> | 32    | TX virtual queue table #2 base address        |
| 1510458C | <u>VQTX TB BASE 3</u> | 32    | TX virtual queue table #3 base address        |
| 15104590 | <u>VQTX TB BASE 4</u> | 32    | TX virtual queue table #4 base address        |
| 15104594 | <u>VQTX TB BASE 5</u> | 32    | TX virtual queue table #5 base address        |
| 15104598 | <u>VQTX TB BASE 6</u> | 32    | TX virtual queue table #6 base address        |
| 1510459C | <u>VQTX TB BASE 7</u> | 32    | TX virtual queue table #7 base address        |
| 151045F0 | <u>QDMA PAGE</u>      | 32    | QDMA configuration page                       |
| 15104600 | <u>QDMA INFO</u>      | 32    | QDMA information                              |
| 15104604 | <u>QDMA GLO_CFG</u>   | 32    | QDMA global configuration                     |
| 15104608 | <u>QDMA_RST_IDX</u>   | 32    | QDMA reset index                              |
| 1510460C | <u>QDMA_DELAY_INT</u> | 32    | Delay interrupt configuration                 |
| 15104610 | <u>QDMA_FC_THRES</u>  | 32    | Flow control threshold                        |
| 15104614 | <u>QDMA_FC_MODE</u>   | 32    | QDMA flow control mode                        |
| 15104618 | <u>QDMA_INT_STS</u>   | 32    | Interrupt status                              |
| 1510461C | <u>QDMA_INT_MASK</u>  | 32    | Interrupt mask                                |
| 15104620 | <u>QDMA_INT_GRP1</u>  | 32    | QDMA interrupt group 1 control                |
| 15104624 | <u>QDMA_INT_GRP2</u>  | 32    | QDMA interrupt group 2 control                |
| 15104628 | <u>QDMA_DROP_PREC</u> | 32    | QDMA drop by FFA percentage control           |
| 15104640 | <u>QDMA_HRED1</u>     | 32    | QDMA HW RED distribution - I                  |
| 15104644 | <u>QDMA_HRED2</u>     | 32    | QDMA HW RED distribution - II                 |
| 15104648 | <u>QDMA_SRED1</u>     | 32    | QDMA SW RED distribution - I                  |
| 1510464C | <u>QDMA_SRED2</u>     | 32    | QDMA SW RED distribution - II                 |

| Address  | Name                      | Width | Register Function                                       |
|----------|---------------------------|-------|---------------------------------------------------------|
| 15104670 | <u>QDMA_INT_STS_G0</u>    | 32    | QDMA interrupt status group 0                           |
| 15104674 | <u>QDMA_INT_STS_G1</u>    | 32    | QDMA interrupt status group 1                           |
| 15104678 | <u>QDMA_INT_STS_G2</u>    | 32    | QDMA interrupt status group 2                           |
| 15104680 | <u>VQTX_GLO</u>           | 32    | TX virtual queue global configuration                   |
| 1510468C | <u>VQTX_INVLD_PTR</u>     | 32    | TX virtual queue Invalid pointer                        |
| 15104690 | <u>VQTX_NUM</u>           | 32    | Number of TX virtual queue configuration                |
| 15104698 | <u>VQTX_SCH</u>           | 32    | TX virtual queue schedule configuration                 |
| 151046A0 | <u>VQTX_HASH_CFG</u>      | 32    | TX virtual queue hash configuration                     |
| 151046A4 | <u>VQTX_HASH_SD</u>       | 32    | TX virtual queue hash seed                              |
| 151046B0 | <u>VQTX_VLD_CFG</u>       | 32    | TX virtual queue valid configuration                    |
| 151046BC | <u>QTX_MIB_IF</u>         | 32    | TX queue MIB interface                                  |
| 151046C0 | <u>VQTX_MIB_PCNT</u>      | 32    | TX virtual queue MIB packet count                       |
| 151046C4 | <u>VQTX_MIB_BCNTL</u>     | 32    | TX virtual queue MIB byte count low bytes               |
| 151046C8 | <u>VQTX_MIB_BCNTH</u>     | 32    | TX virtual queue MIB byte count high bytes              |
| 151046CC | <u>VQTX_MIB_DPCNT</u>     | 32    | TX virtual queue MIB drop packet count                  |
| 151046D0 | <u>QTX_MIB_PCNT</u>       | 32    | TX physical queue MIB forward packet count              |
| 151046D4 | <u>QTX_MIB_DPCNT</u>      | 32    | TX physical queue MIB dropped packet count              |
| 151046D8 | <u>QTX_MIB_BCNTL</u>      | 32    | TX physical queue MIB byte count low bytes              |
| 151046DC | <u>QTX_MIB_BCNTH</u>      | 32    | TX physical queue MIB byte count high bytes             |
| 15104700 | <u>QTX_CTX_PTR</u>        | 32    | TX forward CPU pointer                                  |
| 15104704 | <u>QTX_DTX_PTR</u>        | 32    | TX forward DMA pointer                                  |
| 15104708 | <u>QTX_FWD_CNT</u>        | 32    | TX forward DMA counter                                  |
| 15104710 | <u>QTX_CRX_PTR</u>        | 32    | TX release CPU pointer                                  |
| 15104714 | <u>QTX_DRX_PTR</u>        | 32    | TX release DMA pointer                                  |
| 15104718 | <u>QTX_RLS_CNT</u>        | 32    | TX release DMA counter                                  |
| 15104720 | <u>QDMA_FQ_HEAD</u>       | 32    | Free page head pointer                                  |
| 15104724 | <u>QDMA_FQ_TAIL</u>       | 32    | Free page tail pointer                                  |
| 15104728 | <u>QDMA_FQ_CNT</u>        | 32    | Free page counter                                       |
| 1510472C | <u>QDMA_FQ_BLEN</u>       | 32    | Free page buffer length                                 |
| 15104730 | <u>QDMA_QTX_PTR</u>       | 32    | QDMA TX transmit pointer                                |
| 15104734 | <u>QDMA_QRX_PTR</u>       | 32    | QDMA RX receive pointer                                 |
| 15104798 | <u>QDMA_TX_SCH1_SCH2</u>  | 32    | TX scheduler1 and scheduler2 rate control               |
| 1510479C | <u>QDMA_TX_SCH3_SCH4</u>  | 32    | TX scheduler3 and scheduler4 rate control               |
| 151047C0 | <u>VQTX_0_3_BIND_QID</u>  | 32    | QDMA virtual queue group #0~3 to physical queue binding |
| 151047C4 | <u>VQTX_4_7_BIND_QID</u>  | 32    | QDMA virtual queue group #4~7 to physical queue binding |
| 151047E0 | <u>QTX_FC_SW_STS_0_15</u> | 32    | TX queue#0~15 software path flow control status         |
| 151047EC | <u>QDMA_ULTRA_CFG</u>     | 32    | QDMA AXI ULTRA configuration                            |
| 151047F0 | <u>QDMA_BUS_CFG</u>       | 32    | QDMA AXI BUS configuration                              |
| 151047F4 | <u>QDMA_RBUS_CFG</u>      | 32    | QDMA RBUS configuration                                 |

15104400 QTX\_CFG\_0 TX queue #0, #(16 \* n) configuration 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  | TX_DES_CNT  |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_RESV_CNT |    |    |    |    |    |    |    | SW_RESV_CNT |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                |
|--------|-------------|------------------------------------------------------------------------------------------------------------|
| 31:16  | TX_DES_CNT  | <b>TX descriptor count in queue #</b>                                                                      |
| 15:8   | HW_RESV_CNT | <b>Buffer reserved for hardware path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES. |
| 7:0    | SW_RESV_CNT | <b>Buffer reserved for software path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES. |

15104404      **QTX\_SCH\_0**      **TX queue #0, #(16 \* n) schedule**      00100010

| Bit   | 31            | 30 | 29         | 28 | 27          | 26           | 25 | 24 | 23 | 22 | 21 | 20 | 19           | 18 | 17 | 16 |
|-------|---------------|----|------------|----|-------------|--------------|----|----|----|----|----|----|--------------|----|----|----|
| Name  | TX_SCH_SEL    |    | BUCKET_DEP |    | MIN_RATE_EN | MIN_RATE_MAN |    |    |    |    |    |    | MIN_RATE_EXP |    |    |    |
| Type  | RW            |    | RW         |    | RW          | RW           |    |    |    |    |    |    | RW           |    |    |    |
| Reset | 0             | 0  | 0          | 0  | 0           | 0            | 0  | 0  | 0  | 0  | 0  | 1  | 0            | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13         | 12 | 11          | 10           | 9  | 8  | 7  | 6  | 5  | 4  | 3            | 2  | 1  | 0  |
| Name  | MAX_RATE_WGHT |    |            |    | MAX_RATE_EN | MAX_RATE_MAN |    |    |    |    |    |    | MAX_RATE_EXP |    |    |    |
| Type  | RW            |    |            |    | RW          | RW           |    |    |    |    |    |    | RW           |    |    |    |
| Reset | 0             | 0  | 0          | 0  | 0           | 0            | 0  | 0  | 0  | 0  | 0  | 1  | 0            | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                |
|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30  | TX_SCH_SEL   | <b>TX queue on scheduler no.</b><br><br>0: SCH1 scheduler<br><br>1: SCH2 scheduler<br><br>2: SCH3 scheduler<br><br>3: SCH4 scheduler                                                                                                                                                       |
| 29:28  | BUCKET_DEP   | <b>Bucket depth</b><br><br>0: 2KB<br><br>1: 4KB<br><br>2: 8KB<br><br>3: 16KB                                                                                                                                                                                                               |
| 27     | MIN_RATE_EN  | <b>TX queue min. rate control enable</b><br><br>[Note] Rate control is calculated by 125MHz bus clock, please multiply by a factor when the bus clock is not 125MHz.<br><br>0: Disable. When disabled, shaper will always let the packet pass (infinite rate)<br><br>1: Enable min. shaper |
| 26:20  | MIN_RATE_MAN | <b>Mantissa part of the max. rate control of the TX queue #</b><br><br>Value range: 0~127                                                                                                                                                                                                  |
| 19:16  | MIN_RATE_EXP | <b>Exponent part of the max. rate control of the TX queue #</b><br><br>value selection<br><br>0: QDMA_RATE_EXP0 (default: 1kbps)<br><br>1: QDMA_RATE_EXP1 (default: 10kbps)<br><br>2: QDMA_RATE_EXP2 (default: 100kbps)<br><br>3: QDMA_RATE_EXP3 (default: 1Mbps)                          |

| Bit(s) | Name          | Description                                                                                                                                                                                                                                                                                                                                          |
|--------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |               | 4: QDMA_RATE_EXP4 (default: 10Mbps)                                                                                                                                                                                                                                                                                                                  |
|        |               | 5: QDMA_RATE_EXP5 (default: 100Mbps)                                                                                                                                                                                                                                                                                                                 |
|        |               | Others: 20'd1, 1Gbps                                                                                                                                                                                                                                                                                                                                 |
| 15:12  | MAX_RATE_WGHT | <b>The weighted value of the WFQ for TX queue # maximum rate.</b><br>0: Weight value = 16<br>1: Weight value = 1<br>2: Weight value = 2<br>n: Weight value = n<br>15: Weight value = 15                                                                                                                                                              |
| 11     | MAX_RATE_EN   | <b>TX queue max. rate control enable.</b><br>[Note] Rate control is calculated by 125MHz bus clock, please multiply by a factor when the bus clock is not 125MHz.<br>0: Disable. When disabled, shaper will always let the packet pass (infinite rate)<br>1: Enable max. shaper                                                                      |
| 10:4   | MAX_RATE_MAN  | <b>Mantissa part of the max. rate control of the TX queue #</b><br>Value range: 0~127                                                                                                                                                                                                                                                                |
| 3:0    | MAX_RATE_EXP  | <b>Exponent part of the max. rate control of the TX queue #</b><br>value selection<br>0: QDMA_RATE_EXP0 (default: 1kbps)<br>1: QDMA_RATE_EXP1 (default: 10kbps)<br>2: QDMA_RATE_EXP2 (default: 100kbps)<br>3: QDMA_RATE_EXP3 (default: 1Mbps)<br>4: QDMA_RATE_EXP4 (default: 10Mbps)<br>5: QDMA_RATE_EXP5 (default: 100Mbps)<br>Others: 20'd1, 1Gbps |

15104408 **QTX\_HEAD\_0** TX queue #0, #(16 \* n) head pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_HEAD | TX descriptor head pointer in queue # |

1510440C **QTX\_TAIL\_0** TX queue #0, #(16 \* n) tail pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_TAIL | TX descriptor tail pointer in queue # |

**15104410 QTX\_CFG\_1 TX queue #1, #(16 \* n + 1) configuration 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  | TX_DES_CNT  |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_RESV_CNT |    |    |    |    |    |    |    | SW_RESV_CNT |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                |
|--------|-------------|------------------------------------------------------------------------------------------------------------|
| 31:16  | TX_DES_CNT  | <b>TX descriptor count in queue #</b>                                                                      |
| 15:8   | HW_RESV_CNT | <b>Buffer reserved for hardware path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES. |
| 7:0    | SW_RESV_CNT | <b>Buffer reserved for software path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES. |

**15104414 QTX\_SCH\_1 TX queue #1, #(16 \* n + 1) schedule 00100010**

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                                      |
|--------|---------|----------------------------------------------------------------------------------|
| 31:0   | QTX_SCH | <b>Please refer to the description of QTX_SCH_0. The definition is the same.</b> |

15104418 QTX\_HEAD\_1 TX queue #1, #(16 \* n + 1) head pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_HEAD | TX descriptor head pointer in queue # |

1510441C QTX\_TAIL\_1 TX queue #1, #(16 \* n + 1) tail pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_TAIL | TX descriptor tail pointer in queue # |



**15104420 QTX\_CFG\_2 TX queue #2, #(16 \* n + 2) configuration 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  | TX_DES_CNT  |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_RESV_CNT |    |    |    |    |    |    |    | SW_RESV_CNT |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                |
|--------|-------------|------------------------------------------------------------------------------------------------------------|
| 31:16  | TX_DES_CNT  | <b>TX descriptor count in queue #</b>                                                                      |
| 15:8   | HW_RESV_CNT | <b>Buffer reserved for hardware path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES. |
| 7:0    | SW_RESV_CNT | <b>Buffer reserved for software path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES. |

**15104424 QTX\_SCH\_2 TX queue #2, #(16 \* n + 2) schedule 00100010**

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                                      |
|--------|---------|----------------------------------------------------------------------------------|
| 31:0   | QTX_SCH | <b>Please refer to the description of QTX_SCH_0. The definition is the same.</b> |

15104428 **QTX\_HEAD\_2** TX queue #2, #(16 \* n + 2) head pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_HEAD | TX descriptor head pointer in queue # |

1510442C **QTX\_TAIL\_2** TX queue #2, #(16 \* n + 2) tail pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_TAIL | TX descriptor tail pointer in queue # |

15104430      **QTX\_CFG\_3**      TX queue #3, #(16 \* n + 3) configuration      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  | TX_DES_CNT  |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_RESV_CNT |    |    |    |    |    |    |    | SW_RESV_CNT |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                       |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | TX_DES_CNT  | <b>TX descriptor count in queue #</b>                                                                                                                             |
| 15:8   | HW_RESV_CNT | <b>Buffer reserved for hardware path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |
| 7:0    | SW_RESV_CNT | <b>Buffer reserved for software path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |

15104434      **QTX\_SCH\_3**      TX queue #3, #(16 \* n + 3) schedule      00100010

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                               |
|--------|---------|---------------------------------------------------------------------------|
| 31:0   | QTX_SCH | Please refer to the description of QTX_SCH_0. The definition is the same. |

15104438 **QTX\_HEAD\_3** TX queue #3, #(16 \* n + 3) head pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_HEAD | TX descriptor head pointer in queue # |

1510443C **QTX\_TAIL\_3** TX queue #3, #(16 \* n + 3) tail pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_TAIL | TX descriptor tail pointer in queue # |

15104440      **QTX\_CFG\_4**      TX queue #4, #(16 \* n + 4) configuration      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  | TX_DES_CNT  |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_RESV_CNT |    |    |    |    |    |    |    | SW_RESV_CNT |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                       |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | TX_DES_CNT  | <b>TX descriptor count in queue #</b>                                                                                                                             |
| 15:8   | HW_RESV_CNT | <b>Buffer reserved for hardware path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |
| 7:0    | SW_RESV_CNT | <b>Buffer reserved for software path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |

15104444      **QTX\_SCH\_4**      TX queue #4, #(16 \* n + 4) schedule      00100010

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                               |
|--------|---------|---------------------------------------------------------------------------|
| 31:0   | QTX_SCH | Please refer to the description of QTX_SCH_0. The definition is the same. |

15104448 **QTX\_HEAD\_4** TX queue #4, #(16 \* n + 4) head pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_HEAD | TX descriptor head pointer in queue # |

1510444C **QTX\_TAIL\_4** TX queue #4, #(16 \* n + 4) tail pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_TAIL | TX descriptor tail pointer in queue # |

15104450      **QTX\_CFG\_5**      TX queue #5, #(16 \* n + 5) configuration      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  | TX_DES_CNT  |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_RESV_CNT |    |    |    |    |    |    |    | SW_RESV_CNT |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                       |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | TX_DES_CNT  | <b>TX descriptor count in queue #</b>                                                                                                                             |
| 15:8   | HW_RESV_CNT | <b>Buffer reserved for hardware path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |
| 7:0    | SW_RESV_CNT | <b>Buffer reserved for software path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |

15104454      **QTX\_SCH\_5**      TX queue #5, #(16 \* n + 5) schedule      00100010

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                               |
|--------|---------|---------------------------------------------------------------------------|
| 31:0   | QTX_SCH | Please refer to the description of QTX_SCH_0. The definition is the same. |

15104458 **QTX\_HEAD 5** TX queue #5, #(16 \* n + 5) head pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_HEAD | TX descriptor head pointer in queue # |

1510445C **QTX\_TAIL 5** TX queue #5, #(16 \* n + 5) tail pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_TAIL | TX descriptor tail pointer in queue # |



15104460      **QTX\_CFG\_6**      TX queue #6, #(16 \* n + 6) configuration      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  | TX_DES_CNT  |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_RESV_CNT |    |    |    |    |    |    |    | SW_RESV_CNT |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                       |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | TX_DES_CNT  | <b>TX descriptor count in queue #</b>                                                                                                                             |
| 15:8   | HW_RESV_CNT | <b>Buffer reserved for hardware path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |
| 7:0    | SW_RESV_CNT | <b>Buffer reserved for software path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |

15104464      **QTX\_SCH\_6**      TX queue #6, #(16 \* n + 6) schedule      00100010

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                               |
|--------|---------|---------------------------------------------------------------------------|
| 31:0   | QTX_SCH | Please refer to the description of QTX_SCH_0. The definition is the same. |

15104468 **QTX\_HEAD\_6** TX queue #6, #(16 \* n + 6) head pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_HEAD | TX descriptor head pointer in queue # |

1510446C **QTX\_TAIL\_6** TX queue #6, #(16 \* n + 6) tail pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_TAIL | TX descriptor tail pointer in queue # |

15104470      QTX\_CFG\_7      TX queue #7, #(16 \* n + 7) configuration      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  | TX_DES_CNT  |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_RESV_CNT |    |    |    |    |    |    |    | SW_RESV_CNT |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                       |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | TX_DES_CNT  | <b>TX descriptor count in queue #</b>                                                                                                                             |
| 15:8   | HW_RESV_CNT | <b>Buffer reserved for hardware path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |
| 7:0    | SW_RESV_CNT | <b>Buffer reserved for software path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |

15104474      QTX\_SCH\_7      TX queue #7, #(16 \* n + 7) schedule      00100010

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                               |
|--------|---------|---------------------------------------------------------------------------|
| 31:0   | QTX_SCH | Please refer to the description of QTX_SCH_0. The definition is the same. |

15104478 **QTX\_HEAD 7** TX queue #7, #(16 \* n + 7) head pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_HEAD | TX descriptor head pointer in queue # |

1510447C **QTX\_TAIL 7** TX queue #7, #(16 \* n + 7) tail pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_TAIL | TX descriptor tail pointer in queue # |

15104480      **QTX\_CFG\_8**      TX queue #8, #(16 \* n + 8) configuration      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  | TX_DES_CNT  |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_RESV_CNT |    |    |    |    |    |    |    | SW_RESV_CNT |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                       |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | TX_DES_CNT  | <b>TX descriptor count in queue #</b>                                                                                                                             |
| 15:8   | HW_RESV_CNT | <b>Buffer reserved for hardware path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |
| 7:0    | SW_RESV_CNT | <b>Buffer reserved for software path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |

15104484      **QTX\_SCH\_8**      TX queue #8, #(16 \* n + 8) schedule      00100010

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                               |
|--------|---------|---------------------------------------------------------------------------|
| 31:0   | QTX_SCH | Please refer to the description of QTX_SCH_0. The definition is the same. |

15104488 **QTX\_HEAD 8** TX queue #8, #(16 \* n + 8) head pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_HEAD | TX descriptor head pointer in queue # |

1510448C **QTX\_TAIL 8** TX queue #8, #(16 \* n + 8) tail pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_TAIL | TX descriptor tail pointer in queue # |

15104490      **QTX\_CFG\_9**      TX queue #9, #(16 \* n + 9) configuration      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  | TX_DES_CNT  |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_RESV_CNT |    |    |    |    |    |    |    | SW_RESV_CNT |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                       |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | TX_DES_CNT  | <b>TX descriptor count in queue #</b>                                                                                                                             |
| 15:8   | HW_RESV_CNT | <b>Buffer reserved for hardware path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |
| 7:0    | SW_RESV_CNT | <b>Buffer reserved for software path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |

15104494      **QTX\_SCH\_9**      TX queue #9, #(16 \* n + 9) schedule      00100010

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                               |
|--------|---------|---------------------------------------------------------------------------|
| 31:0   | QTX_SCH | Please refer to the description of QTX_SCH_0. The definition is the same. |

15104498 **QTX\_HEAD\_9** TX queue #9, #(16 \* n + 9) head pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_HEAD | TX descriptor head pointer in queue # |

1510449C **QTX\_TAIL\_9** TX queue #9, #(16 \* n + 9) tail pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_TAIL | TX descriptor tail pointer in queue # |



**151044A0 QTX\_CFG\_10 TX queue #10, #(16 \* n + 10) configuration 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  | TX_DES_CNT  |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_RESV_CNT |    |    |    |    |    |    |    | SW_RESV_CNT |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                       |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | TX_DES_CNT  | <b>TX descriptor count in queue #</b>                                                                                                                             |
| 15:8   | HW_RESV_CNT | <b>Buffer reserved for hardware path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |
| 7:0    | SW_RESV_CNT | <b>Buffer reserved for software path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |

**151044A4 QTX\_SCH\_10 TX queue #10, #(16 \* n + 10) schedule 00100010**

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                                      |
|--------|---------|----------------------------------------------------------------------------------|
| 31:0   | QTX_SCH | <b>Please refer to the description of QTX_SCH_0. The definition is the same.</b> |

151044A8      QTX\_HEAD 10      TX queue #10, #(16 \* n + 10) head pointer      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_HEAD | TX descriptor head pointer in queue # |

151044AC      QTX\_TAIL 10      TX queue #10, #(16 \* n + 10) tail pointer      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_TAIL | TX descriptor tail pointer in queue # |

**151044B0 QTX\_CFG\_11 TX queue #11, #(16 \* n + 11) configuration 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  | TX_DES_CNT  |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_RESV_CNT |    |    |    |    |    |    |    | SW_RESV_CNT |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                       |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | TX_DES_CNT  | <b>TX descriptor count in queue #</b>                                                                                                                             |
| 15:8   | HW_RESV_CNT | <b>Buffer reserved for hardware path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |
| 7:0    | SW_RESV_CNT | <b>Buffer reserved for software path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |

**151044B4 QTX\_SCH\_11 TX queue #11, #(16 \* n + 11) schedule 00100010**

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                                      |
|--------|---------|----------------------------------------------------------------------------------|
| 31:0   | QTX_SCH | <b>Please refer to the description of QTX_SCH_0. The definition is the same.</b> |

151044B8      QTX\_HEAD 11      TX queue #11, #(16 \* n + 11) head pointer      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_HEAD | TX descriptor head pointer in queue # |

151044BC      QTX\_TAIL 11      TX queue #11, #(16 \* n + 11) tail pointer      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_TAIL | TX descriptor tail pointer in queue # |

**151044C0 QTX\_CFG\_12 TX queue #12, #(16 \* n + 12) configuration 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  | TX_DES_CNT  |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_RESV_CNT |    |    |    |    |    |    |    | SW_RESV_CNT |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                       |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | TX_DES_CNT  | <b>TX descriptor count in queue #</b>                                                                                                                             |
| 15:8   | HW_RESV_CNT | <b>Buffer reserved for hardware path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |
| 7:0    | SW_RESV_CNT | <b>Buffer reserved for software path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |

**151044C4 QTX\_SCH\_12 TX queue #12, #(16 \* n + 12) schedule 00100010**

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                                      |
|--------|---------|----------------------------------------------------------------------------------|
| 31:0   | QTX_SCH | <b>Please refer to the description of QTX_SCH_0. The definition is the same.</b> |

151044C8      QTX\_HEAD 12      TX queue #12, #(16 \* n + 12) head pointer      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_HEAD | TX descriptor head pointer in queue # |

151044CC      QTX\_TAIL 12      TX queue #12, #(16 \* n + 12) tail pointer      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_TAIL | TX descriptor tail pointer in queue # |

151044D0      QTX\_CFG\_13      TX queue #13, #(16 \* n + 13) configuration      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  | TX_DES_CNT  |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_RESV_CNT |    |    |    |    |    |    |    | SW_RESV_CNT |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                       |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | TX_DES_CNT  | <b>TX descriptor count in queue #</b>                                                                                                                             |
| 15:8   | HW_RESV_CNT | <b>Buffer reserved for hardware path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |
| 7:0    | SW_RESV_CNT | <b>Buffer reserved for software path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |

**151044D4      QTX\_SCH\_13      TX queue #13, #(16 \* n + 13) schedule      00100010**

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                               |
|--------|---------|---------------------------------------------------------------------------|
| 31:0   | QTX_SCH | Please refer to the description of QTX_SCH_0. The definition is the same. |

**151044D8      QTX\_HEAD\_13      TX queue #13, #(16 \* n + 13) head pointer      00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_HEAD | TX descriptor head pointer in queue # |



**151044DC QTX\_TAIL\_13 TX queue #13, #(16 \* n + 13) tail pointer 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_TAIL | TX descriptor tail pointer in queue # |

**151044E0 QTX\_CFG\_14 TX queue #14, #(16 \* n + 14) configuration 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  | TX_DES_CNT  |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_RESV_CNT |    |    |    |    |    |    |    | SW_RESV_CNT |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                       |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | TX_DES_CNT  | TX descriptor count in queue #                                                                                                                                    |
| 15:8   | HW_RESV_CNT | <b>Buffer reserved for hardware path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |
| 7:0    | SW_RESV_CNT | <b>Buffer reserved for software path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |

**151044E4 QTX\_SCH\_14 TX queue #14, #(16 \* n + 14) schedule 00100010**

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                               |
|--------|---------|---------------------------------------------------------------------------|
| 31:0   | QTX_SCH | Please refer to the description of QTX_SCH_0. The definition is the same. |

**151044E8 QTX\_HEAD\_14 TX queue #14, #(16 \* n + 14) head pointer 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_HEAD | TX descriptor head pointer in queue # |

**151044EC QTX\_TAIL\_14 TX queue #14, #(16 \* n + 14) tail pointer 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_TAIL | TX descriptor tail pointer in queue # |

**151044F0 QTX\_CFG\_15 TX queue #15, #(16 \* n + 15) configuration 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| Name  | TX_DES_CNT  |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_RESV_CNT |    |    |    |    |    |    |    | SW_RESV_CNT |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                       |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | TX_DES_CNT  | <b>TX descriptor count in queue #</b>                                                                                                                             |
| 15:8   | HW_RESV_CNT | <b>Buffer reserved for hardware path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |
| 7:0    | SW_RESV_CNT | <b>Buffer reserved for software path</b><br><br>The reserved buffer number is specified on QDMA_RES_THRES.<br><br>0: No reserved buffer<br><br>1: Buffer Reserved |

**151044F4 QTX\_SCH\_15 TX queue #15, #(16 \* n + 15) schedule 00100010**

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_SCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                                                      |
|--------|---------|----------------------------------------------------------------------------------|
| 31:0   | QTX_SCH | <b>Please refer to the description of QTX_SCH_0. The definition is the same.</b> |

**151044F8 QTX HEAD 15 TX queue #15, #(16 \* n + 15) head pointer 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_HEAD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_HEAD | TX descriptor head pointer in queue # |

**151044FC QTX TAIL 15 TX queue #15, #(16 \* n + 15) tail pointer 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_DES_TAIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                           |
|--------|-------------|---------------------------------------|
| 31:0   | TX_DES_TAIL | TX descriptor tail pointer in queue # |

**15104500 QRX BASE PTR 0 RX ring #0 base pointer 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                   |
|--------|-------------|---------------------------------------------------------------|
| 31:0   | RX_BASE_PTR | Point to the base address of RX ring # (4-DW aligned address) |

15104504 **QRX\_MAX\_CNT\_0** RX ring #0 maximum count 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_MAX_CNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                  |
|--------|------------|----------------------------------------------|
| 11:0   | RX_MAX_CNT | The maximum number of RXD count in RX ring # |

15104508 **QRX\_CRX\_IDX\_0** RX ring #0 CPU pointer 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_CRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                            |
|--------|------------|----------------------------------------|
| 11:0   | RX_CRX_IDX | Point to the next RXD CPU wants to use |

1510450C **QRX\_DRX\_IDX\_0** RX ring #0 DMA pointer 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_DRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                            |
|--------|------------|----------------------------------------|
| 11:0   | RX_DRX_IDX | Point to the next RXD DMA wants to use |

**15104580      VQTX\_TB\_BASE\_0      TX virtual queue table #0 base address      00000000**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | VQTX_TB_BASE_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VQTX_TB_BASE_0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                             |
|--------|----------------|---------------------------------------------------------------------------------------------------------|
| 31:0   | VQTX_TB_BASE_0 | Base address of TX Virtual Queue Table #0<br>This virtual queue table belongs to virtual queue group #0 |

**15104584      VQTX\_TB\_BASE\_1      TX virtual queue table #1 base address      00000000**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | VQTX_TB_BASE_1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VQTX_TB_BASE_1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                             |
|--------|----------------|---------------------------------------------------------------------------------------------------------|
| 31:0   | VQTX_TB_BASE_1 | Base address of TX Virtual Queue Table #1<br>This virtual queue table belongs to virtual queue group #1 |

**15104588**      **VQTX\_TB\_BASE\_2**      **TX virtual queue table #2 base address**      **00000000**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | VQTX_TB_BASE_2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VQTX_TB_BASE_2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                             |
|--------|----------------|---------------------------------------------------------------------------------------------------------|
| 31:0   | VQTX_TB_BASE_2 | Base address of TX Virtual Queue Table #2<br>This virtual queue table belongs to virtual queue group #2 |

**1510458C**      **VQTX\_TB\_BASE\_3**      **TX virtual queue table #3 base address**      **00000000**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | VQTX_TB_BASE_3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VQTX_TB_BASE_3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                             |
|--------|----------------|---------------------------------------------------------------------------------------------------------|
| 31:0   | VQTX_TB_BASE_3 | Base address of TX Virtual Queue Table #3<br>This virtual queue table belongs to virtual queue group #3 |

15104590 **VQTX\_TB\_BASE\_4** TX virtual queue table #4 base address 00000000

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | VQTX_TB_BASE_4 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VQTX_TB_BASE_4 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                             |
|--------|----------------|---------------------------------------------------------------------------------------------------------|
| 31:0   | VQTX_TB_BASE_4 | Base address of TX Virtual Queue Table #4<br>This virtual queue table belongs to virtual queue group #4 |

15104594 **VQTX\_TB\_BASE\_5** TX virtual queue table #5 base address 00000000

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | VQTX_TB_BASE_5 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VQTX_TB_BASE_5 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                             |
|--------|----------------|---------------------------------------------------------------------------------------------------------|
| 31:0   | VQTX_TB_BASE_5 | Base address of TX Virtual Queue Table #5<br>This virtual queue table belongs to virtual queue group #5 |



15104598 **VQTX\_TB\_BASE\_6** TX virtual queue table #6 base address 00000000

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | VQTX_TB_BASE_6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VQTX_TB_BASE_6 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                             |
|--------|----------------|---------------------------------------------------------------------------------------------------------|
| 31:0   | VQTX_TB_BASE_6 | Base address of TX Virtual Queue Table #6<br>This virtual queue table belongs to virtual queue group #6 |

1510459C **VQTX\_TB\_BASE\_7** TX virtual queue table #7 base address 00000000

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | VQTX_TB_BASE_7 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VQTX_TB_BASE_7 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                             |
|--------|----------------|---------------------------------------------------------------------------------------------------------|
| 31:0   | VQTX_TB_BASE_7 | Base address of TX Virtual Queue Table #7<br>This virtual queue table belongs to virtual queue group #7 |

151045F0      QDMA\_PAGE      QDMA configuration page      00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19           | 18 | 17 | 16 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|--------------|----|----|----|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |              |    |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |              |    |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |              |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3            | 2  | 1  | 0  |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    | QTX_CFG_PAGE |    |    |    |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    | RW           |    |    |    |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    | 0            | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|--------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0    | QTX_CFG_PAGE | <p><b>Switch the page of per physical queue configuration registers</b></p> <p>This setting will control following registers:</p> <p>QTX_CFG_*/QTX_SCH_*/QTX_HEAD_*/QTX_TAIL_*/RST_TX_IDX*/QDMA_DROP_PREC/FORCE_QUE</p> <p>0: Mapping to physical queues #0~15, page n = 0</p> <p>1: Mapping to physical queues #16~31, page n = 1</p> <p>2: Mapping to physical queues #32~47, page n = 2</p> <p>3: Mapping to physical queues #48~63, page n = 3</p> <p>4: Mapping to physical queues #64~79, page n = 4</p> <p>5: Mapping to physical queues #80~95, page n = 5</p> <p>6: Mapping to physical queues #96~111, page n = 6</p> <p>7: Mapping to physical queues #112~127, page n = 7</p> <p>Others: Reserved</p> |

**15104600 QDMA\_INFO QDMA information 1C010080**

| Bit   | 31         | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  | REV        |    |    |    | INDEX_WIDTH |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    | RO          |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 1  | 1           | 1  | 0  | 0  |    |    |    |    |    |    |    |    |
| Bit   | 15         | 14 | 13 | 12 | 11          | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_QUE_NUM |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO         |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description      |
|--------|-------------|------------------|
| 31:28  | REV         | QDMA revision    |
| 27:24  | INDEX_WIDTH | Ring index width |
| 15:0   | TX_QUE_NUM  | TX queue number  |

**15104604 QDMA\_GLO\_CFG QDMA global configuration 55404530**

| Bit   | 31           | 30              | 29        | 28 | 27           | 26            | 25 | 24        | 23         | 22 | 21           | 20 | 19           | 18          | 17             | 16          |
|-------|--------------|-----------------|-----------|----|--------------|---------------|----|-----------|------------|----|--------------|----|--------------|-------------|----------------|-------------|
| Name  | RX_2B_OFFSET | CSR_CLKGATE_BYP | BYTE_SWAP |    | PKT_RX_WDONE | DMAD_WR_WDONE |    |           |            |    |              |    |              |             |                |             |
| Type  | RW           | RW              | RW        |    | RW           | RW            |    |           |            |    |              |    |              |             |                |             |
| Reset | 0            | 1               | 0         |    | 0            | 1             |    |           |            |    |              |    |              |             |                |             |
| Bit   | 15           | 14              | 13        | 12 | 11           | 10            | 9  | 8         | 7          | 6  | 5            | 4  | 3            | 2           | 1              | 0           |
| Name  | MUTLI_CNT    |                 |           |    | LEAKY_BK     |               |    | MUTLI_DMA | BIG_ENDIAN |    | QDMA_BT_SIZE |    | RX_DMA_BUS_Y | RX_DMA_A_EN | TX_DMA_A_BUS_Y | TX_DMA_A_EN |
| Type  | RW           |                 |           |    | RW           |               |    | RW        | RW         |    | RW           |    | RO           | RW          | RO             | RW          |
| Reset | 0            | 1               | 0         | 0  | 0            |               |    | 1         | 0          |    | 1            | 1  | 0            | 0           | 0              | 0           |

| Bit(s) | Name            | Description                                                                                                                                                                                                             |
|--------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | RX_2B_OFFSET    | <p><b>Prepend 2-Byte to RX-buffer (packet) for aligning IP header to 32-bit boundary.</b></p> <p>Default MAC header is 14-Byte</p> <p>0: Disable 2-byte prepended</p> <p>1: Enable 2-byte prepended</p>                 |
| 30     | CSR_CLKGATE_BYP | <p><b>Clock gated Bypass</b></p> <p>0: DMA clock is gating as idle</p> <p>1: DMA clock is free-running</p>                                                                                                              |
| 29     | BYTE_SWAP       | <p><b>Byte Swap</b></p> <p>0: QDMA will not do byte swapping for TX/RX packet descriptor</p> <p>1: QDMA will do byte swapping for TX/RX packet descriptor</p>                                                           |
| 27     | PKT_RX_WDONE    | <p><b>Packet Payload Write Done Check</b></p> <p>0: Write transaction finished after AXI write last</p> <p>1: Write transaction finished till AXI response done be asserted</p>                                         |
| 26     | DMAD_WR_WDONE   | <p><b>Packet Descriptor Write Done Check</b></p> <p>0: Write transaction finished after AXI write last</p> <p>1: Write transaction finished till AXI response done be asserted</p>                                      |
| 15:12  | MUTLI_CNT       | <p><b>Number of TX DMA read outstanding transactions when QDMA_GLO_CFG[8] = 1'b1.</b></p> <p>4'h1: Single-issue</p> <p>4'h2: 2 read transactions</p> <p>4'h4: 4 read transactions</p> <p>4'hf: 15 read transactions</p> |

| Bit(s) | Name         | Description                                                                                                                                                             |
|--------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11     | LEAKY_BK     | <b>Select bucket type for TX queue MAX sharper and MIN sharper</b><br><br>0: Token bucket<br><br>1: Leaky bucket                                                        |
| 8      | MUTLI_DMA    | <b>Enable TX DAM AXI read outstanding transaction</b><br><br>0: Disable TX DMA read outstanding transaction<br><br>1: Enable TX DMA read outstanding transaction        |
| 7      | BIG_ENDIAN   | <b>Big-endian</b><br><br>0: QDMA will not do byte swapping for TX/RX packet header and payload<br><br>1: QDMA will do byte swapping for TX/RX packet header and payload |
| 5:4    | QDMA_BT_SIZE | <b>The burst size of QDMA</b><br><br>0: 4 DWORDs (16-bytes)<br>1: 8 DWORDs (32-bytes)<br>2: 16 DWORDs (64-bytes)<br>3: 32 DWORDs (128-bytes)                            |
| 3      | RX_DMA_BUSY  | 0: RX_DMA is not busy<br><br>1: RX_DMA is busy                                                                                                                          |
| 2      | RX_DMA_EN    | 0: Disable RX_DMA (when disabled, RX_DMA will finish the current receiving packet, then stop)<br><br>1: Enable RX_DMA                                                   |
| 1      | TX_DMA_BUSY  | 0: TX_DMA is not busy<br><br>1: TX_DNA is busy                                                                                                                          |
| 0      | TX_DMA_EN    | 0: Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, then stop)<br><br>1: Enable TX_DMA                                                     |

15104608      **QDMA\_RST\_IDX**      QDMA reset index      00000000

| Bit   | 31           | 30           | 29           | 28           | 27           | 26           | 25          | 24          | 23          | 22          | 21          | 20          | 19          | 18          | 17           | 16           |
|-------|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|--------------|--------------|
| Name  |              |              |              | RST_SCH      |              |              |             |             |             |             |             |             |             |             | RST_DRX_IDX1 | RST_DRX_IDX0 |
| Type  |              |              |              | RW           |              |              |             |             |             |             |             |             |             |             | RW           | RW           |
| Reset |              |              |              | 0            |              |              |             |             |             |             |             |             |             |             | 0            | 0            |
| Bit   | 15           | 14           | 13           | 12           | 11           | 10           | 9           | 8           | 7           | 6           | 5           | 4           | 3           | 2           | 1            | 0            |
| Name  | RST_TX_IDX15 | RST_TX_IDX14 | RST_TX_IDX13 | RST_TX_IDX12 | RST_TX_IDX11 | RST_TX_IDX10 | RST_TX_IDX9 | RST_TX_IDX8 | RST_TX_IDX7 | RST_TX_IDX6 | RST_TX_IDX5 | RST_TX_IDX4 | RST_TX_IDX3 | RST_TX_IDX2 | RST_TX_IDX1  | RST_TX_IDX0  |
| Type  | RW           | RW           | RW           | RW           | RW           | RW           | RW          | RW          | RW          | RW          | RW          | RW          | RW          | RW          | RW           | RW           |
| Reset | 0            | 0            | 0            | 0            | 0            | 0            | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0           | 0            | 0            |

| Bit(s) | Name         | Description                                                                             |
|--------|--------------|-----------------------------------------------------------------------------------------|
| 28     | RST_SCH      | Write 1 to reset all token buckets of scheduler<br><br>Only valid when QTX_CFG_PAGE = 0 |
| 17     | RST_DRX_IDX1 | Write 1 to reset RX_DMA RX_IDX1 to 0<br><br>Only valid when QTX_CFG_PAGE = 0            |
| 16     | RST_DRX_IDX0 | Write 1 to reset RX_DMA RX_IDX0 to 0<br><br>Only valid when QTX_CFG_PAGE = 0            |
| 15     | RST_TX_IDX15 | Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 15) to 0                            |
| 14     | RST_TX_IDX14 | Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 14) to 0                            |
| 13     | RST_TX_IDX13 | Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 13) to 0                            |
| 12     | RST_TX_IDX12 | Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 12) to 0                            |
| 11     | RST_TX_IDX11 | Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 11) to 0                            |
| 10     | RST_TX_IDX10 | Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 10) to 0                            |
| 9      | RST_TX_IDX9  | Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 9) to 0                             |
| 8      | RST_TX_IDX8  | Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 8) to 0                             |
| 7      | RST_TX_IDX7  | Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 7) to 0                             |
| 6      | RST_TX_IDX6  | Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 6) to 0                             |
| 5      | RST_TX_IDX5  | Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 5) to 0                             |
| 4      | RST_TX_IDX4  | Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 4) to 0                             |
| 3      | RST_TX_IDX3  | Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 3) to 0                             |
| 2      | RST_TX_IDX2  | Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 2) to 0                             |
| 1      | RST_TX_IDX1  | Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 1) to 0                             |
| 0      | RST_TX_IDX0  | Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 0) to 0                             |

1510460C QDMA\_DELAY\_INT Delay interrupt configuration 00000000

| Bit   | 31           | 30           | 29 | 28 | 27 | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|--------------|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| Name  | RXDLY_INT_EN | RXMAX_PINT   |    |    |    |    |    |    | RXMAX_PTIME   |    |    |    |    |    |    |    |
| Type  | RW           | RW           |    |    |    |    |    |    | RW            |    |    |    |    |    |    |    |
| Reset | 0            | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14           | 13 | 12 | 11 | 10 | 9  | 8  | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RLS_DINT_EN  | RLS_MAX_PINT |    |    |    |    |    |    | RLS_MAX_PTIME |    |    |    |    |    |    |    |
| Type  | RW           | RW           |    |    |    |    |    |    | RW            |    |    |    |    |    |    |    |
| Reset | 0            | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                                                                                                                                                                                  |
|--------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | RXDLY_INT_EN  | 0: Disable RX delayed interrupt mechanism<br><br>1: Enable RX delayed interrupt mechanism                                                                                                                                                                                                                                    |
| 30:24  | RXMAX_PINT    | <b>Specified max. number of pending interrupts</b><br><br>When the number of pending interrupts is equal to or greater than the value specified here or when interrupt pending time reaches the limit (see below), a final RX_DLY_INT is generated.<br><br>[Note] Resetting to 0 can disable pending interrupt count check.  |
| 23:16  | RXMAX_PTIME   | <b>Specified max. pending time</b><br><br>When the pending time is equal to or greater than RXMAX_PTIME x 20us or when the number of pending RX_DONE is equal to or greater than RXMAX_PINT 9 (see above), a final RX_DLY_INT is generated.<br><br>[Note] Resetting to 0 can disable pending interrupt time check.           |
| 15     | RLS_DINT_EN   | 0: Disable RLS delayed interrupt mechanism<br><br>1: Enable RLS delayed interrupt mechanism                                                                                                                                                                                                                                  |
| 14:8   | RLS_MAX_PINT  | <b>Specified max. number of pending interrupts</b><br><br>When the number of pending interrupts is equal to or greater than the value specified here or when interrupt pending time reaches the limit (see below), a final RLS_DLY_INT is generated.<br><br>[Note] Resetting to 0 can disable pending interrupt count check. |
| 7:0    | RLS_MAX_PTIME | <b>Specified max. pending time</b><br><br>When the pending time is equal to or greater than RLS_MAX_PTIME x 20us or when the number of pending RX_DONE is equal to or greater than RLS_MAX_PINT (see above), a final RLS_DLY_INT is generated.<br><br>[Note] Resetting to 0 can disable pending interrupt time check.        |

**15104610 QDMA\_FC\_THRES Flow control threshold 90904444**

| Bit   | 31                 | 30 | 29           | 28 | 27            | 26 | 25          | 24         | 23                 | 22 | 21              | 20 | 19            | 18 | 17            | 16         |
|-------|--------------------|----|--------------|----|---------------|----|-------------|------------|--------------------|----|-----------------|----|---------------|----|---------------|------------|
| Name  | SW_DROP_FSTVQ_MODE |    | SW_DROP_MODE |    | SW_DROP_FSTVQ |    | SW_DROP_FFA | SW_DROP_EN | HW_DROP_FSTVQ_MODE |    | HW_REDDROP_MODE |    | HW_DROP_FSTVQ |    | HW_FC_RELEASE | HW_DROP_EN |
| Type  | RW                 |    | RW           |    | RW            |    | RW          | RW         | RW                 |    | RW              |    | RW            |    | RW            | RW         |
| Reset | 1                  | 0  | 0            | 1  | 0             |    | 0           | 0          | 1                  | 0  | 0               | 1  | 0             |    | 0             | 0          |
| Bit   | 15                 | 14 | 13           | 12 | 11            | 10 | 9           | 8          | 7                  | 6  | 5               | 4  | 3             | 2  | 1             | 0          |
| Name  | SHARE_SW_TH        |    |              |    | SHARE_HW_TH   |    |             |            | FREE_TH            |    |                 |    | RING_TH       |    |               |            |
| Type  | RW                 |    |              |    | RW            |    |             |            | RW                 |    |                 |    | RW            |    |               |            |
| Reset | 0                  | 1  | 0            | 0  | 0             | 1  | 0           | 0          | 0                  | 1  | 0               | 0  | 0             | 1  | 0             | 0          |

| Bit(s) | Name               | Description                                                                                                                                                                                                                                                                                                                                                                                                                     |
|--------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30  | SW_DROP_FSTVQ_MODE | <b>SW drop condition on fullest virtual queue</b><br><br>If the corresponding PQ SW occupied queue depth over the SW_RESV_CNT, the en-queuing packet to fullest VQ will be drop depends on the usage of SW free-for-all buffer.<br><br>2'b00: FFA usage >= 0%<br><br>2'b01: FFA usage >= 25%<br><br>2'b10: FFA usage >= 50%<br><br>2'b11: FFA usage >= 75%                                                                      |
| 29:28  | SW_DROP_MODE       | <b>Drop Distribution Mode for SW Drop</b><br><br>Different drop probability when SW Free for All buffer usage (>75% / >50% / >25% / >0%)<br><br>Drop Probability:<br><br>2'b00: 50%/25%/0%/0%<br><br>2'b01: 75%/50%/25%/0%<br><br>2'b10: 100%/75%/50%/25%<br><br>2'b11: 100%/100%/75%/50%                                                                                                                                       |
| 27     | SW_DROP_FSTVQ      | <b>SW drop en-queuing packet on fullest virtual queue, only take effect on the physical queues those binding with virtual queues.</b>                                                                                                                                                                                                                                                                                           |
| 25     | SW_DROP_FFA        | <b>Flow Control Drop</b><br><br>QDMA asserts FC when FFA is equal to 0 and egress queue count is bigger than the reserved queue count. However, the de-assert condition is specified on this control bit.<br><br>0: QDMA de-assert FC when the egress queue count is less than the reserved queue count.<br><br>1: QDMA de-assert FC when FFA is bigger than 0 or the egress queue count is less than the reserved queue count. |
| 24     | SW_DROP_EN         | <b>Enable Flow Control for SW buffer pool</b>                                                                                                                                                                                                                                                                                                                                                                                   |



| Bit(s) | Name               | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|--------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                    | QDMA drop packets when FFA is equal to 0 and the egress queue count is bigger than the reserved queue count.                                                                                                                                                                                                                                                                                                                                                                                            |
| 23:22  | HW_DROP_FSTVQ_MODE | <p><b>HW drop condition on fullest virtual queue</b></p> <p>If the corresponding PQ SW occupied queue depth over the SW_RESV_CNT, the en-queuing packet to fullest VQ will be drop depends on the usage of HW free-for-all buffer.</p> <p>2'b00: FFA usage &gt;= 0%</p> <p>2'b01: FFA usage &gt;= 25%</p> <p>2'b10: FFA usage &gt;= 50%</p> <p>2'b11: FFA usage &gt;= 75%</p>                                                                                                                           |
| 21:20  | HW_REDDROP_MODE    | <p><b>Random Early Drop Distribution Mode for HW Drop</b></p> <p>Four different drop probability when HW Free-for-all (FFA) buffer usage is (&gt;75% / &gt;50% / &gt;25% / &gt;0%)</p> <p>Drop Probability:</p> <p>2'b00: 50%/25%/0%/0%</p> <p>2'b01: 75%/50%/25%/0%</p> <p>2'b10: 100%/75%/50%/25%</p> <p>2'b11: 100%/100%/75%/50%</p>                                                                                                                                                                 |
| 19     | HW_DROP_FSTVQ      | <b>HW drop en-queuing packet on fullest virtual queue, only take effect on the physical queues those binding with virtual queues.</b>                                                                                                                                                                                                                                                                                                                                                                   |
| 17     | HW_FC_RELEASE      | <p><b>Flow Control Release Condition (not for RED)</b></p> <p>QDMA asserts FC when FFA is equal to DROP/PFC condition and the egress queue count is bigger than the reserved queue count. However, the de-assert condition is specified on this control bit.</p> <p>0: QDMA de-assert FC when the egress queue count is less than the reserved queue count.</p> <p>1: QDMA de-assert FC when FFA is bigger than DROP/PFC condition or the egress queue count is less than the reserved queue count.</p> |
| 16     | HW_DROP_EN         | <p><b>Drop packets when HW flow control is asserted</b></p> <p>QDMA drop packets when Free-for-all (FFA) is equal to 0 and the egress queue count is bigger than the reserved queue count.</p>                                                                                                                                                                                                                                                                                                          |
| 15:12  | SHARE_SW_TH        | <p><b>SW Shared buffer threshold</b></p> <p>QDMA will drop TX packets when the left shared buffer descriptors reach this threshold</p>                                                                                                                                                                                                                                                                                                                                                                  |
| 11:8   | SHARE_HW_TH        | <p><b>HW Shared buffer threshold</b></p> <p>QDMA will drop TX packets when the left shared buffer descriptors reach this threshold</p>                                                                                                                                                                                                                                                                                                                                                                  |
| 7:4    | FREE_TH            | <b>RX free buffer threshold</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

| Bit(s) | Name    | Description                                                                                                        |
|--------|---------|--------------------------------------------------------------------------------------------------------------------|
|        |         | QDMA will pause RXDMA interface when the left free buffer descriptors reach this threshold                         |
| 3:0    | RING_TH | <b>RX ring threshold</b><br>QDMA will pause RXDMA interface when the left RX ring descriptors reach this threshold |

15104614      **QDMA\_FC\_MODE**      **QDMA flow control mode**      00000000

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19             | 18            | 17          | 16 |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|----------------|---------------|-------------|----|
| Name  | Reserved |    |    |    |    |    |    |    |    |    |    |    |                |               |             |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |                |               |             |    |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0             | 0           | 0  |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3              | 2             | 1           | 0  |
| Name  | Reserved |    |    |    |    |    |    |    |    |    |    |    | TX_PFC_RELEASE | TX_PFC_ASSERT | TX_PFC_MODE |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    | RW             | RW            | RW          |    |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0             | 0           | 0  |

| Bit(s) | Name           | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|--------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4   | Reserved       | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 3      | TX_PFC_RELEASE | <b>PFC Loose Release</b><br><br>QDMA TX queue assert PFC signal only if the egress queue count is bigger than the reserved queue count.<br><br>0: PFC is released when FFA and TXQ meet the release condition<br><br>1: Release only if TXQ is less than QDMA_TX threshold                                                                                                                                                                                      |
| 2      | TX_PFC_ASSERT  | <b>PFC Strict Assertion</b><br><br>QDMA TX queue assert PFC signal only if the egress queue count is bigger than the reserved queue count.<br><br>0: PFC is asserted when both FFA and TXQ meet the trigger condition<br><br>1: Ignore FFA condition                                                                                                                                                                                                            |
| 1:0    | TX_PFC_MODE    | <b>Priority Flow Control Assertion Mode</b><br><br>QDMA TXQ asserts PFC signal to PSE when Free-for-all (FFA) usage reach the value and TXQ is bigger than the reserved queue count.<br><br>When PFC is asserted, the de-asserted condition is that FFA is less than the value and TXQ drops a half lower than the reserved queue count.<br><br>2'b00: FFA usage > 0%<br><br>2'b01: FFA usage > 25%<br><br>2'b10: FFA usage > 50%<br><br>2'b11: FFA usage > 75% |

**15104618 QDMA\_INT\_STS Interrupt status 00000000**

| Bit   | 31             | 30             | 29             | 28             | 27 | 26 | 25 | 24          | 23 | 22 | 21 | 20             | 19 | 18 | 17 | 16           |
|-------|----------------|----------------|----------------|----------------|----|----|----|-------------|----|----|----|----------------|----|----|----|--------------|
| Name  | RX_COHERENT    | RX_DLY_INT     | RLS_COHERENT   | RLS_DLY_INT    |    |    |    |             |    |    |    |                |    |    |    | RX_DONE_INT0 |
| Type  | W1C            | W1C            | W1C            | W1C            |    |    |    |             |    |    |    |                |    |    |    | W1C          |
| Reset | 0              | 0              | 0              | 0              |    |    |    |             |    |    |    |                |    |    |    | 0            |
| Bit   | 15             | 14             | 13             | 12             | 11 | 10 | 9  | 8           | 7  | 6  | 5  | 4              | 3  | 2  | 1  | 0            |
| Name  | VQDEP_DEQ_ERR1 | VQDEP_DEQ_ERR0 | VQDEP_ENQ_ERR1 | VQDEP_ENQ_ERR0 |    |    |    | FWD_FIFO_OV |    |    |    | QTX_REQ_EMP_VQ |    |    |    | RLS_DONE_INT |
| Type  | W1C            | W1C            | W1C            | W1C            |    |    |    | W1C         |    |    |    | W1C            |    |    |    | W1C          |
| Reset | 0              | 0              | 0              | 0              |    |    |    | 0           |    |    |    | 0              |    |    |    | 0            |

| Bit(s) | Name           | Description                                                                                                                                         |
|--------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | RX_COHERENT    | RX_DMA finds data coherent event while checking DDONE bit.                                                                                          |
| 30     | RX_DLY_INT     | Summary of the whole QDMA RX related interrupts.                                                                                                    |
| 29     | RLS_COHERENT   | TX_DMA finds data coherent event while checking DDONE bit.                                                                                          |
| 28     | RLS_DLY_INT    | Summary of the whole QDMA TX related interrupts.                                                                                                    |
| 16     | RX_DONE_INT0   | RX ring #0 packet receive interrupt                                                                                                                 |
| 15     | VQDEP_DEQ_ERR1 | VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing.<br>A VQ not empty yet after de-queuing, but the remainder VQ_DEPTH >= 1               |
| 14     | VQDEP_DEQ_ERR0 | VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing.<br>A VQ becomes empty after de-queuing but the remainder VQ_DEPTH = 0                 |
| 13     | VQDEP_ENQ_ERR1 | VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing.<br>A VQ been en-queued the first packet descriptor, but the VQ_DEPTH already >=1.     |
| 12     | VQDEP_ENQ_ERR0 | VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing.<br>A VQ been en-queued a packet descriptor, but the VQ_DEPTH already full = 16'hffff. |
| 8      | FWD_FIFO_OV    | Forwarding engine FIFO overflow interrupt                                                                                                           |
| 4      | QTX_REQ_EMP_VQ | QDMA TX request to transmit an empty VQ                                                                                                             |
| 0      | RLS_DONE_INT   | CPU release transmitted packet interrupt                                                                                                            |

1510461C QDMA\_INT\_MASK Interrupt mask 00000000

| Bit   | 31             | 30             | 29             | 28             | 27 | 26 | 25 | 24          | 23 | 22 | 21 | 20               | 19 | 18 | 17 | 16           |
|-------|----------------|----------------|----------------|----------------|----|----|----|-------------|----|----|----|------------------|----|----|----|--------------|
| Name  | RX_COHERENT    | RX_DLY_INT     | RLS_COHERENT   | RLS_DLY_INT    |    |    |    |             |    |    |    |                  |    |    |    | RX_DONE_INT0 |
| Type  | RW             | RW             | RW             | RW             |    |    |    |             |    |    |    |                  |    |    |    | RW           |
| Reset | 0              | 0              | 0              | 0              |    |    |    |             |    |    |    |                  |    |    |    | 0            |
| Bit   | 15             | 14             | 13             | 12             | 11 | 10 | 9  | 8           | 7  | 6  | 5  | 4                | 3  | 2  | 1  | 0            |
| Name  | VQDEP_DEQ_ERR1 | VQDEP_DEQ_ERR0 | VQDEP_ENQ_ERR1 | VQDEP_ENQ_ERR0 |    |    |    | FWD_FIFO_OV |    |    |    | QTX_REQ_EMPTY_VQ |    |    |    | RLS_DONE_INT |
| Type  | RW             | RW             | RW             | RW             |    |    |    | RW          |    |    |    | RW               |    |    |    | RW           |
| Reset | 0              | 0              | 0              | 0              |    |    |    | 0           |    |    |    | 0                |    |    |    | 0            |

| Bit(s) | Name           | Description                                                                                                                                                                                             |
|--------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | RX_COHERENT    | <b>Interrupt enable for RX_DMA data coherent vent</b><br><br>0: Disable interrupt<br><br>1: Enable interrupt                                                                                            |
| 30     | RX_DLY_INT     | <b>Summary of the whole QDMA RX related interrupts.</b><br><br>0: Disable interrupt<br><br>1: Enable interrupt                                                                                          |
| 29     | RLS_COHERENT   | <b>Interrupt enable for TX_DMA data coherent vent</b><br><br>0: Disable interrupt<br><br>1: Enable interrupt                                                                                            |
| 28     | RLS_DLY_INT    | <b>Summary of the whole QDMA TX related interrupts.</b><br><br>0: Disable interrupt<br><br>1: Enable interrupt                                                                                          |
| 16     | RX_DONE_INT0   | <b>RX ring #0 packet receive interrupt</b><br><br>0: Disable interrupt<br><br>1: Enable interrupt                                                                                                       |
| 15     | VQDEP_DEQ_ERR1 | <b>VQ depth mismatch with the VQHPTR &amp; VQTPTR during de-queuing.</b><br>A VQ not empty yet after de-queuing, but the remainder VQ_DEPTH >= 1<br><br>0: Disable interrupt<br><br>1: Enable interrupt |
| 14     | VQDEP_DEQ_ERR0 | <b>VQ depth mismatch with the VQHPTR &amp; VQTPTR during de-queuing.</b><br>A VQ becomes empty after de-queuing but the remainder VQ_DEPTH = 0<br><br>0: Disable interrupt<br><br>1: Enable interrupt   |

| Bit(s) | Name           | Description                                                                                                                                                                                                     |
|--------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13     | VQDEP_ENQ_ERR1 | <b>VQ depth mismatch with the VQHPTR &amp; VQTPTR during en-queuing.</b><br>A VQ been en-queued the first packet descriptor, but the VQ_DEPTH already $\geq 1$ .<br>0: Disable interrupt<br>1: Enable interrupt |
| 12     | VQDEP_ENQ_ERR0 | <b>VQ depth mismatch with the VQHPTR &amp; VQTPTR during en-queuing.</b><br>A VQ been en-queued a packet descriptor, but the VQ_DEPTH already full = 16'hffff.<br>0: Disable interrupt<br>1: Enable interrupt   |
| 8      | FWD_FIFO_OV    | <b>Forwarding engine FIFO overflow interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt                                                                                                                 |
| 4      | QTX_REQ_EMP_VQ | <b>QDMA TX request to transmit an empty VQ</b>                                                                                                                                                                  |
| 0      | RLS_DONE_INT   | <b>CPU release transmitted packet interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt                                                                                                                  |

**15104620 QDMA\_INT\_GRP1 QDMA interrupt group 1 control 00000000**

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_INT_GRP1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_INT_GRP1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                                                                                      |
|--------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | QDMA_INT_GRP1 | <b>Interrupt group 1 assignment.</b><br><br>Each bit's definition is same as "QDMA_INT_STS"<br><br>0: Leave to QDMA interrupt group 0, if (QDMA_INT_GRP1[n]==0 & QDMA_INT_GRP2[n]==0)<br><br>1: Assign to QDMA interrupt group 1 |

**15104624 QDMA\_INT\_GRP2 QDMA interrupt group 2 control 00000000**

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_INT_GRP2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_INT_GRP2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                                                                                      |
|--------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | QDMA_INT_GRP2 | <b>Interrupt group 2 assignment.</b><br><br>Each bit's definition is same as "QDMA_INT_STS"<br><br>0: Leave to QDMA interrupt group 0, if (QDMA_INT_GRP1[n]==0 & QDMA_INT_GRP2[n]==0)<br><br>1: Assign to QDMA interrupt group 2 |

15104628      **QDMA\_DROP\_PREC**      **QDMA drop by FFA percentage control**      00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | SW_DROP_PREC |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HW_DROP_PREC |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                                             |
|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | SW_DROP_PREC | <p><b>QDMA SW Drop by FFA Percentage Control</b></p> <p>QDMA drop packets based on the full percentage of Free-for-All</p> <p>[31:16] = [PQ#(16 * QTX_CFG_PAGE + 15) : PQ#(16 * QTX_CFG_PAGE + 0)]</p> <p>0: Disable drop by FFA percentage</p> <p>1: Enable drop by FFA percentage</p> |
| 15:0   | HW_DROP_PREC | <p><b>QDMA HW Drop by FFA Percentage Control</b></p> <p>QDMA drop packets based on the full percentage of Free-for-All</p> <p>[15:0] = [PQ#(16 * QTX_CFG_PAGE + 15) : PQ#(16 * QTX_CFG_PAGE + 0)]</p> <p>0: Disable drop by FFA percentage</p> <p>1: Enable drop by FFA percentage</p>  |



**15104640 QDMA\_HRED1 QDMA HW RED distribution - I FFFFFFFF**

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | FFA_LOW_UTIL    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1               | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | FFA_MIDDLE_UTIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1               | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name            | Description                                                                                                                                                            |
|--------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | FFA_LOW_UTIL    | <b>Low Utilization of FFA on HW path</b><br><br>When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 25% probability.    |
| 15:0   | FFA_MIDDLE_UTIL | <b>Middle Utilization of FFA on HW path</b><br><br>When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 50% probability. |

**15104644 QDMA\_HRED2 QDMA HW RED distribution - II FFFFFFFF**

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16           |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------|
| Name  | REVO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    | FFA_UTIL_SEL |
| Type  | RW            |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW           |
| Reset | 1             | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1            |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0            |
| Name  | FFA_HIGH_UTIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |              |
| Type  | RW            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |              |
| Reset | 1             | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1            |

| Bit(s) | Name          | Description                                                                                                                                                          |
|--------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17  | REVO          | <b>Reserved</b>                                                                                                                                                      |
| 16     | FFA_UTIL_SEL  | <b>Manually Set FFA Utilization</b><br><br>When the bit is set, FFA Utilization will be configurable for user.                                                       |
| 15:0   | FFA_HIGH_UTIL | <b>High Utilization of FFA on HW path</b><br><br>When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 75% probability. |

**15104648 QDMA\_SRED1 QDMA SW RED distribution - I FFFFFFFF**

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | FFA_LOW_UTIL    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1               | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | FFA_MIDDLE_UTIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1               | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name            | Description                                                                                                                                                             |
|--------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | FFA_LOW_UTIL    | <b>Low Utilization of FFA on HW path</b><br><br>When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 25% probability.     |
| 15:0   | FFA_MIDDLE_UTIL | <b>Middle Utilization of FFA on CPU path</b><br><br>When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 50% probability. |

**1510464C QDMA\_SRED2 QDMA SW RED distribution - II FFFFFFFF**

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16           |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------|
| Name  | REVO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    | FFA_UTIL_SEL |
| Type  | RW              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW           |
| Reset | 1               | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1            |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0            |
| Name  | FFA_MIDDLE_UTIL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |              |
| Type  | RW              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |              |
| Reset | 1               | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1            |

| Bit(s) | Name            | Description                                                                                                                                                           |
|--------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17  | REVO            | <b>Reserved</b>                                                                                                                                                       |
| 16     | FFA_UTIL_SEL    | <b>Manually Set FFA Utilization</b><br><br>When the bit is set, FFA Utilization will be configurable for user.                                                        |
| 15:0   | FFA_MIDDLE_UTIL | <b>High Utilization of FFA on CPU path</b><br><br>When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 75% probability. |

**15104670 QDMA\_INT\_STS\_G0 QDMA interrupt status group 0 00000000**

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_INT_STS_G0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_INT_STS_G0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                       |
|--------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | QDMA_INT_STS_G0 | Interrupt group 0 status, this information already "and" with "QDMA_INT_IMR"<br><br>Each bit definition is same as "QDMA_INT_STS" |

**15104674 QDMA\_INT\_STS\_G1 QDMA interrupt status group 1 00000000**

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_INT_STS_G1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_INT_STS_G1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                       |
|--------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | QDMA_INT_STS_G1 | Interrupt group 1 status, this information already "and" with "QDMA_INT_IMR"<br><br>Each bit definition is same as "QDMA_INT_STS" |

**15104678 QDMA\_INT\_STS\_G2 QDMA interrupt status group 2 00000000**

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QDMA_INT_STS_G2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QDMA_INT_STS_G2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                       |
|--------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | QDMA_INT_STS_G2 | Interrupt group 2 status, this information already "and" with "QDMA_INT_IMR"<br><br>Each bit definition is same as "QDMA_INT_STS" |

**15104680 VQTX\_GLO TX virtual queue global configuration 000005EA**

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17          | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|
| Name  |            |    |    |    |    |    |    |    |    |    |    |    |    |    | VQTB_MIB_EN |    |
| Type  |            |    |    |    |    |    |    |    |    |    |    |    |    |    | RW          |    |
| Reset |            |    |    |    |    |    |    |    |    |    |    |    |    |    | 0           |    |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1           | 0  |
| Name  | VQTX_GQTUM |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |
| Type  | RW         |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1           | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                                                           |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 17     | VQTB_MIB_EN | Configuration for the MIB packet/byte counter field of virtual queue table<br><br>0: Disable MIB counter field, each virtual table entry is 16bytes<br><br>1: Enable MIB counter field, each virtual table entry extends to 32bytes, to record the amount of transmitted byte and packet count for each virtual queue |
| 15:0   | VQTX_GQTUM  | Number of bytes a virtual queue is allowed to de-queue before the scheduler moves to the next virtual queue. Default is to the MTU of the interface. The minimum value is 1.                                                                                                                                          |

1510468C      **VQTX\_INVLD\_PTR**      TX virtual queue Invalid pointer      DEADBEEF

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | VQTX_INVLD_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VQTX_INVLD_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1              | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name           | Description                                                                                                                                                                                                                                        |
|--------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | VQTX_INVLD_PTR | <p><b>The pointer address indicates a invalid virtual queue head/tail pointer.</b></p> <p>Either "VQHPTR" or "VQTPTR" of VQ table is equal to this invalid pointer VQTX_INVLD_PTR, which means there is no valid packet in this virtual queue.</p> |

15104690 **VQTX\_NUM** Number of TX virtual queue configuration 00000000

| Bit   | 31         | 30 | 29 | 28 | 27 | 26         | 25 | 24 | 23 | 22         | 21 | 20 | 19 | 18         | 17 | 16 |
|-------|------------|----|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|----|
| Name  | VQTX_NUM_7 |    |    |    |    | VQTX_NUM_6 |    |    |    | VQTX_NUM_5 |    |    |    | VQTX_NUM_4 |    |    |
| Type  | RW         |    |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |
| Reset |            | 0  | 0  | 0  |    | 0          | 0  | 0  |    | 0          | 0  | 0  |    | 0          | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10         | 9  | 8  | 7  | 6          | 5  | 4  | 3  | 2          | 1  | 0  |
| Name  | VQTX_NUM_3 |    |    |    |    | VQTX_NUM_2 |    |    |    | VQTX_NUM_1 |    |    |    | VQTX_NUM_0 |    |    |
| Type  | RW         |    |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |
| Reset |            | 0  | 0  | 0  |    | 0          | 0  | 0  |    | 0          | 0  | 0  |    | 0          | 0  | 0  |

| Bit(s) | Name       | Description                                        |
|--------|------------|----------------------------------------------------|
| 30:28  | VQTX_NUM_7 | Number of virtual queues in virtual queue group #7 |
| 26:24  | VQTX_NUM_6 | Number of virtual queues in virtual queue group #6 |
| 22:20  | VQTX_NUM_5 | Number of virtual queues in virtual queue group #5 |
| 18:16  | VQTX_NUM_4 | Number of virtual queues in virtual queue group #4 |
| 14:12  | VQTX_NUM_3 | Number of virtual queues in virtual queue group #3 |
| 10:8   | VQTX_NUM_2 | Number of virtual queues in virtual queue group #2 |
| 6:4    | VQTX_NUM_1 | Number of virtual queues in virtual queue group #1 |
| 2:0    | VQTX_NUM_0 | Number of virtual queues in virtual queue group #0 |
|        |            | 0: Disable virtual queue function                  |
|        |            | 1: 32                                              |
|        |            | 2: 64                                              |
|        |            | 3: 128                                             |
|        |            | 4: 256                                             |
|        |            | 5: 512                                             |
|        |            | 6: 1024                                            |
|        |            | 7: Reserved                                        |

**15104698**      **VQTX\_SCH**      **TX virtual queue schedule configuration**      **00000000**

| Bit   | 31 | 30 | 29         | 28 | 27 | 26 | 25         | 24 | 23 | 22 | 21         | 20 | 19 | 18 | 17         | 16 |
|-------|----|----|------------|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|
| Name  |    |    | VQTX_SCH_7 |    |    |    | VQTX_SCH_6 |    |    |    | VQTX_SCH_5 |    |    |    | VQTX_SCH_4 |    |
| Type  |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |
| Reset |    |    | 0          | 0  |    |    | 0          | 0  |    |    | 0          | 0  |    |    | 0          | 0  |
| Bit   | 15 | 14 | 13         | 12 | 11 | 10 | 9          | 8  | 7  | 6  | 5          | 4  | 3  | 2  | 1          | 0  |
| Name  |    |    | VQTX_SCH_3 |    |    |    | VQTX_SCH_2 |    |    |    | VQTX_SCH_1 |    |    |    | VQTX_SCH_0 |    |
| Type  |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |
| Reset |    |    | 0          | 0  |    |    | 0          | 0  |    |    | 0          | 0  |    |    | 0          | 0  |

| Bit(s) | Name       | Description                                                   |
|--------|------------|---------------------------------------------------------------|
| 29:28  | VQTX_SCH_7 | Virtual queues scheduling strategy for virtual queue group #7 |
| 25:24  | VQTX_SCH_6 | Virtual queues scheduling strategy for virtual queue group #6 |
| 21:20  | VQTX_SCH_5 | Virtual queues scheduling strategy for virtual queue group #5 |
| 17:16  | VQTX_SCH_4 | Virtual queues scheduling strategy for virtual queue group #4 |
| 13:12  | VQTX_SCH_3 | Virtual queues scheduling strategy for virtual queue group #3 |
| 9:8    | VQTX_SCH_2 | Virtual queues scheduling strategy for virtual queue group #2 |
| 5:4    | VQTX_SCH_1 | Virtual queues scheduling strategy for virtual queue group #1 |
| 1:0    | VQTX_SCH_0 | Virtual queues scheduling strategy for virtual queue group #0 |
|        |            | 0: SFQ (packet base round robin)                              |
|        |            | 1: DRR (deficit round robin)                                  |
|        |            | 2: Reserved                                                   |
|        |            | 3: Reserved                                                   |

**151046A0 VQTX\_HASH\_CFG TX virtual queue hash configuration 00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27                             | 26                             | 25                             | 24                             | 23 | 22 | 21               | 20 | 19 | 18 | 17 | 16                   |
|-------|----------------------|----|----|----|--------------------------------|--------------------------------|--------------------------------|--------------------------------|----|----|------------------|----|----|----|----|----------------------|
| Name  |                      |    |    |    | HASH_PT<br>B_M<br>ODE_E<br>N_3 | HASH_PT<br>B_M<br>ODE_E<br>N_2 | HASH_PT<br>B_M<br>ODE_E<br>N_1 | HASH_PT<br>B_M<br>ODE_E<br>N_0 |    |    | HASH_ST_MOD<br>E |    |    |    |    | HASH_PT<br>B_P<br>RD |
| Type  |                      |    |    |    | RW                             | RW                             | RW                             | RW                             |    |    | RW               |    |    |    |    | RW                   |
| Reset |                      |    |    |    | 0                              | 0                              | 0                              | 0                              |    |    | 0                | 0  |    |    |    | 0                    |
| Bit   | 15                   | 14 | 13 | 12 | 11                             | 10                             | 9                              | 8                              | 7  | 6  | 5                | 4  | 3  | 2  | 1  | 0                    |
| Name  | HASH_PT<br>B_P<br>RD |    |    |    |                                |                                |                                |                                |    |    |                  |    |    |    |    |                      |
| Type  | RW                   |    |    |    |                                |                                |                                |                                |    |    |                  |    |    |    |    |                      |
| Reset | 0                    | 0  | 0  | 0  | 0                              | 0                              | 0                              | 0                              | 0  | 0  | 0                | 0  | 0  | 0  | 0  | 0                    |

| Bit(s) | Name                      | Description                                                                                                                                                                                                                                                                                                                |
|--------|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 27     | HASH_PT<br>B_MODE<br>EN_3 | Enable "Exclusive with CRC32" as a candidate algorithm for perturbed hash changing. This field only valid when HASH_PT<br>B_P<br>RD!=0.                                                                                                                                                                                    |
| 26     | HASH_PT<br>B_MODE<br>EN_2 | Enable "Exclusive with (B^(A&~C))" as a candidate algorithm for perturbed hash changing. This field only valid when HASH_PT<br>B_P<br>RD!=0.                                                                                                                                                                               |
| 25     | HASH_PT<br>B_MODE<br>EN_1 | Enable "Exclusive with (A&B) (~A&C)" as a candidate algorithm for perturbed hash changing. This field only valid when HASH_PT<br>B_P<br>RD!=0.                                                                                                                                                                             |
| 24     | HASH_PT<br>B_MODE<br>EN_0 | Enable "Exclusive with HASH_SEED" as a candidate algorithm for perturbed hash changing. This field only valid when HASH_PT<br>B_P<br>RD!=0.<br><br>(If HASH_PT<br>B_MODE<br>EN_0~3 are all "0", hash will be forced on "Exclusive with HASH_SEED" mode.)                                                                   |
| 21:20  | HASH_ST<br>_MODE          | Hash scrambled mode selection, for static hash virtual queue index generating.<br><br>This field only valid when HASH_PT<br>B_P<br>RD=0<br><br>3: Exclusive with CRC32<br><br>2: Exclusive with (B^(A&~C))<br><br>1: Exclusive with (A&B) (~A&C)<br><br>0: Exclusive with HASH_SEED                                        |
| 16:0   | HASH_PT<br>B_P<br>RD      | If HASH_PT<br>B_P<br>RD = 0, means operating in static hash mode, never changing the hash algorithm periodically.<br><br>Otherwise, operating in perturb hash mode when HASH_PT<br>B_P<br>RD != 0. HASH_PT<br>B_P<br>RD Indicates the period to change the hash algorithm for virtual queue index generating, in 1ms unit. |



151046A4      **VQTX HASH\_SD**      TX virtual queue hash seed      00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | HASH_SD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HASH_SD |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name    | Description                                    |
|--------|---------|------------------------------------------------|
| 31:0   | HASH_SD | Hash seed for "Exclusive with HASH_SEED" mode. |

**151046B0 VQTX\_VLD\_CFG TX virtual queue valid configuration 00000000**

| Bit          | 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
|--------------|-----------------|----|----|----|-----------------|----|----|----|-----------------|----|----|----|-----------------|----|----|----|
| <b>Name</b>  | VQTX_VLD_STRG_7 |    |    |    | VQTX_VLD_STRG_6 |    |    |    | VQTX_VLD_STRG_5 |    |    |    | VQTX_VLD_STRG_4 |    |    |    |
| <b>Type</b>  | RW              |    |    |    | RW              |    |    |    | RW              |    |    |    | RW              |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0               | 0  | 0  | 0  |
| Bit          | 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| <b>Name</b>  | VQTX_VLD_STRG_3 |    |    |    | VQTX_VLD_STRG_2 |    |    |    | VQTX_VLD_STRG_1 |    |    |    | VQTX_VLD_STRG_0 |    |    |    |
| <b>Type</b>  | RW              |    |    |    | RW              |    |    |    | RW              |    |    |    | RW              |    |    |    |
| <b>Reset</b> | 0               | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0               | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                        |
|--------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | VQTX_VLD_STRG_7 | Virtual Queue Group #7: Virtual queue valid bit map starting slice number.                                                                         |
| 27:24  | VQTX_VLD_STRG_6 | Virtual Queue Group #6: Virtual queue valid bit map starting slice number.                                                                         |
| 23:20  | VQTX_VLD_STRG_5 | Virtual Queue Group #5: Virtual queue valid bit map starting slice number.                                                                         |
| 19:16  | VQTX_VLD_STRG_4 | Virtual Queue Group #4: Virtual queue valid bit map starting slice number.                                                                         |
| 15:12  | VQTX_VLD_STRG_3 | Virtual Queue Group #3: Virtual queue valid bit map starting slice number.                                                                         |
| 11:8   | VQTX_VLD_STRG_2 | Virtual Queue Group #2: Virtual queue valid bit map starting slice number.                                                                         |
| 7:4    | VQTX_VLD_STRG_1 | Virtual Queue Group #1: Virtual queue valid bit map starting slice number.                                                                         |
| 3:0    | VQTX_VLD_STRG_0 | Virtual Queue Group #0: Virtual queue valid bit map starting slice number.                                                                         |
|        |                 | 1 VQ valid bit slice comprises 64-bit map.                                                                                                         |
|        |                 | The amount of VQ valid slices for 1 VQ group depends on the setting of "VQTX_NUM_#", hardware will allocate VQ valid bit slices for each VQ group. |
|        |                 | 4'h0: VQ valid bit map starting from slice#0                                                                                                       |
|        |                 | 4'h1: VQ valid bit map starting from slice#1                                                                                                       |
|        |                 | 4'h15: VQ valid bit map starting from slice#15                                                                                                     |

151046BC QTX\_MIB\_IF TX queue MIB interface 00000000

| Bit   | 31 | 30 | 29         | 28          | 27 | 26 | 25           | 24             | 23 | 22          | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|------------|-------------|----|----|--------------|----------------|----|-------------|----|----|----|----|----|----|
| Name  |    |    | MIB_RC_DIS | VQTX_MIB_EN |    |    |              | MIB_PQ_SHW_SEP |    | QTX_MIB_QID |    |    |    |    |    |    |
| Type  |    |    | RW         | W1          |    |    |              | RW             |    | RW          |    |    |    |    |    |    |
| Reset |    |    | 0          | 0           |    |    |              | 0              |    | 0           | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15 | 14 | 13         | 12          | 11 | 10 | 9            | 8              | 7  | 6           | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |            |             |    |    | QTX_MIB_VQID |                |    |             |    |    |    |    |    |    |
| Type  |    |    |            |             |    |    | RW           |                |    |             |    |    |    |    |    |    |
| Reset |    |    |            |             |    |    | 0            | 0              | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                                                                                                                                                        |
|--------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29     | MIB_RC_DIS     | <b>Disable the clear action during MIB reading</b><br><br>0: After MIB reading done, the target MIB counter will be clear to 0<br><br>1: Keeps the value of target MIB counter after MIB reading                                   |
| 28     | VQTX_MIB_EN    | <b>Enable VQTB MIB read procedure</b><br><br>0: After MIB accessing done, HW will clear this bit to 0 and put the result in VQTX_MIB_PCNT, VQTX_MIB_DPCNT, VQTX_MIB_BCNT0, VQTX_MIB_BCNT1<br><br>1: Enable MIB accessing procedure |
| 24     | MIB_PQ_SHW_SEP | <b>Separate the PQ's HW/SW MIB counter of QTX_MIB_PCNT and QTX_MIB_DPCNT</b><br><br>0: Use whole 32bits as one MIB counter, which accumulates SW and HW packet count<br><br>1: Separate the SW and HW MIB counter                  |
| 22:16  | QTX_MIB_QID    | <b>Physical queue ID for MIB accessing</b>                                                                                                                                                                                         |
| 9:0    | QTX_MIB_VQID   | <b>Virtual queue ID for MIB accessing</b>                                                                                                                                                                                          |

**151046C0      VQTX\_MIB\_PCNT      TX virtual queue MIB packet count      00000000**

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | VQTX_MIB_PCNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VQTX_MIB_PCNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                             |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------|
| 31:0   | VQTX_MIB_PCNT | Packet count of virtual queue table, according to QTX_MIB_QID and QTX_MIB_VQID.<br><br>Unavailable when VQTB_MIB_EN = 0 |

**151046C4      VQTX\_MIB\_BCNTL      TX virtual queue MIB byte count low bytes      00000000**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | VQTX_MIB_BCNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VQTX_MIB_BCNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                                                  |
|--------|----------------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | VQTX_MIB_BCNTL | Byte count [31:0] of virtual queue table, according to QTX_MIB_QID and QTX_MIB_VQID.<br><br>Unavailable when VQTB_MIB_EN = 0 |

**151046C8      VQTX\_MIB\_BCNTL      TX virtual queue MIB byte count high bytes      00000000**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | VQTX_MIB_BCNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VQTX_MIB_BCNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                                                   |
|--------|----------------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | VQTX_MIB_BCNTL | Byte count [63:32] of virtual queue table, according to QTX_MIB_QID and QTX_MIB_VQID.<br><br>Unavailable when VQTB_MIB_EN = 0 |

**151046CC      VQTX\_MIB\_DPCNT      TX virtual queue MIB drop packet count      00000000**

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | VQTX_MIB_DPCNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VQTX_MIB_DPCNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                                                     |
|--------|----------------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | VQTX_MIB_DPCNT | Dropped packet count of virtual queue table, according to QTX_MIB_QID and QTX_MIB_VQID.<br><br>Unavailable when VQTB_MIB_EN = 0 |

**151046D0 QTX\_MIB\_PCNT TX physical queue MIB forward packet count 00000000**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_MIB_PCNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_MIB_PCNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                                                                                                                                                     |
|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | QTX_MIB_PCNT | <b>Accumulated forwarded packet count, according to QTX_MIB_QID.</b><br><br>If MIB_PO_SHW_SEP = 1, this counter will be separated into two 16bits counter, [31:16] for software path, [15:0] for hardware path. |

**151046D4 QTX\_MIB\_DPCNT TX physical queue MIB dropped packet count 00000000**

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_MIB_DPCNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_MIB_DPCNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                                                                   |
|--------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | QTX_MIB_DPCNT | <b>Accumulated dropped packet count, according to QTX_MIB_QID.</b><br><br>If MIB_PO_SHW_SEP = 1, this counter will be separated into two 16bits counter, [31:16] for software path, [15:0] for hardware path. |

**151046D8 QTX\_MIB\_BCNTL TX physical queue MIB byte count low bytes 00000000**

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_MIB_BCNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_MIB_BCNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                                                                                               |
|--------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | QTX_MIB_BCNTL | <p><b>Accumulated forwarded byte count [31:0] of physical queue #QTX_MIB_QID.</b></p> <p>Read QTX_MIB_BCNTL will not clear the value of QTX_MIB_BCNTL, QTX_MIB_BCNTL will be cleared by reading QTX_MIB_BCNTH when VQTB_MIB_RC_DIS=0.</p> |

**151046DC QTX\_MIB\_BCNTH TX physical queue MIB byte count high bytes 00000000**

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_MIB_BCNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_MIB_BCNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                                                      |
|--------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | QTX_MIB_BCNTH | <p><b>Accumulated forwarded byte count [35:32] of physical queue #QTX_MIB_QID</b></p> <p>If VQTB_MIB_RC_DIS=0, read QTX_MIB_BCNTH will clear the value of QTX_MIB_BCNTH &amp; QTX_MIB_BCNTL.</p> |

15104700      QTX\_CTX\_PTR      TX forward CPU pointer      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | FWD_CTX_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | FWD_CTX_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                  |
|--------|-------------|------------------------------|
| 31:0   | FWD_CTX_PTR | TX forward chain CPU pointer |

15104704      QTX\_DTX\_PTR      TX forward DMA pointer      00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | FWD_DTX_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | FWD_DTX_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                       |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | FWD_DTX_PTR | TX forward chain DMA pointer                                                                                                      |
|        |             | When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only. |



**15104708**      **QTX\_FWD\_CNT**      **TX forward DMA counter**      **00000000**

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | ACC_HW_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | ACC_SW_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                      |
|--------|------------|----------------------------------|
| 31:16  | ACC_HW_CNT | Accumulated HW forwarded counter |
| 15:0   | ACC_SW_CNT | Accumulated SW forwarded counter |

**15104710**      **QTX\_CRX\_PTR**      **TX release CPU pointer**      **00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RLS_CRX_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RLS_CRX_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                  |
|--------|-------------|------------------------------|
| 31:0   | RLS_CRX_PTR | TX release chain CPU pointer |

**15104714**      **QTX\_DRX\_PTR**      **TX release DMA pointer**      **00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RLS_DRX_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RLS_DRX_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                                  |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | RLS_DRX_PTR | <b>TX release chain DMA pointer</b><br><br>When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only. |

**15104718**      **QTX\_RLS\_CNT**      **TX release DMA counter**      **00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | ACC_RLS_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                     |
|--------|-------------|-------------------------------------------------|
| 15:0   | ACC_RLS_CNT | <b>Accumulated TX released descriptor count</b> |

**15104720 QDMA\_FQ\_HEAD Free page head pointer 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | FQ_HEAD_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | FQ_HEAD_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                              |
|--------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | FQ_HEAD_PTR | <b>Free buffer head pointer</b><br><br>When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only. |

**15104724 QDMA\_FQ\_TAIL Free page tail pointer 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | FQ_TAIL_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | FQ_TAIL_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                                                              |
|--------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | FQ_TAIL_PTR | <b>Free buffer tail pointer</b><br><br>When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only. |

**15104728 QDMA\_FQ\_CNT Free page counter 00000000**

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | SWFQ_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | HWFQ_CNT |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name     | Description                                                                                                             |
|--------|----------|-------------------------------------------------------------------------------------------------------------------------|
| 31:16  | SWFQ_CNT | <b>Free buffer on CPU Pool</b><br><br>Initial free buffer count on CPU pool when QDMA_GLO_CFG.TX_DMA_EN is de-asserted. |
| 15:0   | HWFQ_CNT | <b>Free buffer on HW Pool</b><br><br>Initial free buffer count on HW pool when QDMA_GLO_CFG.TX_DMA_EN is de-asserted.   |

**1510472C QDMA\_FQ\_BLEN Free page buffer length 00080000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21          | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|
| Name  |             |    |    |    |    |    |    |    |    |    | FQ_BUF_BLEN |    |    |    |    |    |
| Type  |             |    |    |    |    |    |    |    |    |    | RW          |    |    |    |    |    |
| Reset |             |    |    |    |    |    |    |    |    |    | 0           | 0  | 1  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5           | 4  | 3  | 2  | 1  | 0  |
| Name  | FQ_BUF_BLEN |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |             |    |    |    |    |    |

| Bit(s) | Name        | Description                                                                                                                                                    |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 21:8   | FQ_BUF_BLEN | <b>Free buffer byte length</b><br><br>Configured free buffer length, QDMA RX will fetch the length info to decide the payload length on one descriptor/buffer. |

**15104730 QDMA\_QTX\_PTR QDMA TX transmit pointer 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QTX_ING_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QTX_ING_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                 |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0   | QTX_ING_PTR | <b>QDMA Transmitting DMAD Pointer</b><br><br>TX gets one DMAD from queues and DMA is fetching the payload from DRAM to PSE. |

**15104734 QDMA\_QRX\_PTR QDMA RX receive pointer 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | QRX_ING_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | QRX_ING_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                                                                                        |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | QRX_ING_PTR | <b>QDMA Receiving DMAD Pointer</b><br><br>RX gets one DMAD from descriptor ring and DMA is receiving the payload from PSE to DRAM. |

15104798 QDMA\_TX\_SCH1\_SCH2 TX scheduler1 and scheduler2 rate control 00100010

| Bit   | 31           | 30            | 29              | 28 | 27           | 26            | 25 | 24 | 23 | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
|-------|--------------|---------------|-----------------|----|--------------|---------------|----|----|----|----|----|----|---------------|----|----|----|
| Name  | SCH2_MAX_WFQ | SCH2_LEAKY_BK | SCH2_BUCKET_DEP |    | SCH2_RATE_EN | SCH2_RATE_MAN |    |    |    |    |    |    | SCH2_RATE_EXP |    |    |    |
| Type  | RW           | RW            | RW              |    | RW           | RW            |    |    |    |    |    |    | RW            |    |    |    |
| Reset | 0            | 0             | 0               | 0  | 0            | 0             | 0  | 0  | 0  | 0  | 0  | 1  | 0             | 0  | 0  | 0  |
| Bit   | 15           | 14            | 13              | 12 | 11           | 10            | 9  | 8  | 7  | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| Name  | SCH1_MAX_WFQ | SCH1_LEAKY_BK | SCH1_BUCKET_DEP |    | SCH1_RATE_EN | SCH1_RATE_MAN |    |    |    |    |    |    | SCH1_RATE_EXP |    |    |    |
| Type  | RW           | RW            | RW              |    | RW           | RW            |    |    |    |    |    |    | RW            |    |    |    |
| Reset | 0            | 0             | 0               | 0  | 0            | 0             | 0  | 0  | 0  | 0  | 0  | 1  | 0             | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                               |
|--------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | SCH2_MAX_WFQ    | <b>Physical queue arbitration mechanism between MIN and MAX rate</b><br><br>0: Strict Priority<br><br>1: Weighted Fair Queue                                                                                                                                                              |
| 30     | SCH2_LEAKY_BK   | <b>Select bucket type for scheduler output sharper</b><br><br>0: Token bucket<br><br>1: Leaky bucket                                                                                                                                                                                      |
| 29:28  | SCH2_BUCKET_DEP | <b>Bucket depth</b><br><br>0: 2KB<br><br>1: 4KB<br><br>2: 8KB<br><br>3: 16KB                                                                                                                                                                                                              |
| 27     | SCH2_RATE_EN    | <b>TX SCH2 max. rate control enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                |
| 26:20  | SCH2_RATE_MAN   | <b>Mantissa part of the max. rate control of the TX SCH2</b><br><br>Value range: 0~127                                                                                                                                                                                                    |
| 19:16  | SCH2_RATE_EXP   | <b>Exponent part of the max. rate control of the TX SCH2</b><br><br>value selection<br><br>0: QDMA_RATE_EXP0 (default: 1kbps)<br>1: QDMA_RATE_EXP1 (default: 10kbps)<br>2: QDMA_RATE_EXP2 (default: 100kbps)<br>3: QDMA_RATE_EXP3 (default: 1Mbps)<br>4: QDMA_RATE_EXP4 (default: 10Mbps) |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                                                                       |
|--------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                 | 5: QDMA_RATE_EXP5 (default: 100Mbps)                                                                                                                                                                                                                                                                                                              |
|        |                 | Others: 20'd1, 1Gbps                                                                                                                                                                                                                                                                                                                              |
| 15     | SCH1_MAX_WFQ    | <b>Physical queue arbitration mechanism between MIN and MAX rate</b><br>0: Strict Priority<br>1: Weighted Fair Queue                                                                                                                                                                                                                              |
| 14     | SCH1_LEAKY_BK   | <b>Select bucket type for scheduler output sharper</b><br>0: Token bucket<br>1: Leaky bucket                                                                                                                                                                                                                                                      |
| 13:12  | SCH1_BUCKET_DEP | <b>Bucket depth</b><br>0: 2KB<br>1: 4KB<br>2: 8KB<br>3:16KB                                                                                                                                                                                                                                                                                       |
| 11     | SCH1_RATE_EN    | <b>TX SCH1 max. rate control enable</b><br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                |
| 10:4   | SCH1_RATE_MAN   | <b>Mantissa part of the max. rate control of the TX SCH1</b><br>Value range: 0~127                                                                                                                                                                                                                                                                |
| 3:0    | SCH1_RATE_EXP   | <b>Exponent part of the max. rate control of the TX SCH2</b><br>value selection<br>0: QDMA_RATE_EXP0 (default: 1kbps)<br>1: QDMA_RATE_EXP1 (default: 10kbps)<br>2: QDMA_RATE_EXP2 (default: 100kbps)<br>3: QDMA_RATE_EXP3 (default: 1Mbps)<br>4: QDMA_RATE_EXP4 (default: 10Mbps)<br>5: QDMA_RATE_EXP5 (default: 100Mbps)<br>Others: 20'd1, 1Gbps |

**1510479C QDMA TX SCH3 SCH4 TX scheduler3 and scheduler4 rate control 00100010**

| Bit   | 31           | 30            | 29              | 28 | 27           | 26            | 25 | 24 | 23 | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
|-------|--------------|---------------|-----------------|----|--------------|---------------|----|----|----|----|----|----|---------------|----|----|----|
| Name  | SCH4_MAX_WFQ | SCH4_LEAKY_BK | SCH4_BUCKET_DEP |    | SCH4_RATE_EN | SCH4_RATE_MAN |    |    |    |    |    |    | SCH4_RATE_EXP |    |    |    |
| Type  | RW           | RW            | RW              |    | RW           | RW            |    |    |    |    |    |    | RW            |    |    |    |
| Reset | 0            | 0             | 0               | 0  | 0            | 0             | 0  | 0  | 0  | 0  | 0  | 1  | 0             | 0  | 0  | 0  |
| Bit   | 15           | 14            | 13              | 12 | 11           | 10            | 9  | 8  | 7  | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| Name  | SCH3_MAX_WFQ | SCH3_LEAKY_BK | SCH3_BUCKET_DEP |    | SCH3_RATE_EN | SCH3_RATE_MAN |    |    |    |    |    |    | SCH3_RATE_EXP |    |    |    |
| Type  | RW           | RW            | RW              |    | RW           | RW            |    |    |    |    |    |    | RW            |    |    |    |
| Reset | 0            | 0             | 0               | 0  | 0            | 0             | 0  | 0  | 0  | 0  | 0  | 1  | 0             | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                               |
|--------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | SCH4_MAX_WFQ    | <b>Physical queue arbitration mechanism between MIN and MAX rate</b><br><br>0: Strict Priority<br><br>1: Weighted Fair Queue                                                                                                                                                              |
| 30     | SCH4_LEAKY_BK   | <b>Select bucket type for scheduler output sharper</b><br><br>0: Token bucket<br><br>1: Leaky bucket                                                                                                                                                                                      |
| 29:28  | SCH4_BUCKET_DEP | <b>Bucket depth</b><br><br>0: 2KB<br><br>1: 4KB<br><br>2: 8KB<br><br>3:16KB                                                                                                                                                                                                               |
| 27     | SCH4_RATE_EN    | <b>TX SCH4 max. rate control enable</b><br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                                |
| 26:20  | SCH4_RATE_MAN   | <b>Mantissa part of the max. rate control of the TX SCH4</b><br><br>Value range: 0~127                                                                                                                                                                                                    |
| 19:16  | SCH4_RATE_EXP   | <b>Exponent part of the max. rate control of the TX SCH4</b><br><br>value selection<br><br>0: QDMA_RATE_EXP0 (default: 1kbps)<br>1: QDMA_RATE_EXP1 (default: 10kbps)<br>2: QDMA_RATE_EXP2 (default: 100kbps)<br>3: QDMA_RATE_EXP3 (default: 1Mbps)<br>4: QDMA_RATE_EXP4 (default: 10Mbps) |



| Bit(s) | Name            | Description                                                                                                                                                                                                                                                                                                                                       |
|--------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                 | 5: QDMA_RATE_EXP5 (default: 100Mbps)                                                                                                                                                                                                                                                                                                              |
|        |                 | Others: 20'd1, 1Gbps                                                                                                                                                                                                                                                                                                                              |
| 15     | SCH3_MAX_WFQ    | <b>Physical queue arbitration mechanism between MIN and MAX rate</b><br>0: Strict Priority<br>1: Weighted Fair Queue                                                                                                                                                                                                                              |
| 14     | SCH3_LEAKY_BK   | <b>Select bucket type for scheduler output sharper</b><br>0: Token bucket<br>1: Leaky bucket                                                                                                                                                                                                                                                      |
| 13:12  | SCH3_BUCKET_DEP | <b>Bucket depth</b><br>0: 2KB<br>1: 4KB<br>2: 8KB<br>3:16KB                                                                                                                                                                                                                                                                                       |
| 11     | SCH3_RATE_EN    | <b>TX SCH3 max. rate control enable</b><br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                |
| 10:4   | SCH3_RATE_MAN   | <b>Mantissa part of the max. rate control of the TX SCH3</b><br>Value range: 0~127                                                                                                                                                                                                                                                                |
| 3:0    | SCH3_RATE_EXP   | <b>Exponent part of the max. rate control of the TX SCH3</b><br>value selection<br>0: QDMA_RATE_EXP0 (default: 1kbps)<br>1: QDMA_RATE_EXP1 (default: 10kbps)<br>2: QDMA_RATE_EXP2 (default: 100kbps)<br>3: QDMA_RATE_EXP3 (default: 1Mbps)<br>4: QDMA_RATE_EXP4 (default: 10Mbps)<br>5: QDMA_RATE_EXP5 (default: 100Mbps)<br>Others: 20'd1, 1Gbps |

151047C0

VQTX 0 3 BIND QIDQDMA virtual queue group #0~3 to physical  
queue binding

03020100

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22              | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|
| Name  | VQTX_3_BIND_QID |    |    |    |    |    |    |    |    | VQTX_2_BIND_QID |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    |    | RW              |    |    |    |    |    |    |
| Reset |                 | 0  | 0  | 0  | 0  | 0  | 1  | 1  |    | 0               | 0  | 0  | 0  | 0  | 1  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6               | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VQTX_1_BIND_QID |    |    |    |    |    |    |    |    | VQTX_0_BIND_QID |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    |    | RW              |    |    |    |    |    |    |
| Reset |                 | 0  | 0  | 0  | 0  | 0  | 0  | 1  |    | 0               | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                   |
|--------|-----------------|---------------------------------------------------------------|
| 30:24  | VQTX_3_BIND_QID | Physical queue number which binds with Virtual queue group #3 |
| 22:16  | VQTX_2_BIND_QID | Physical queue number which binds with Virtual queue group #2 |
| 14:8   | VQTX_1_BIND_QID | Physical queue number which binds with Virtual queue group #1 |
| 6:0    | VQTX_0_BIND_QID | Physical queue number which binds with Virtual queue group #0 |

151047C4

VQTX 4 7 BIND QIDQDMA virtual queue group #4~7 to physical  
queue binding

07060504

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22              | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|
| Name  | VQTX_7_BIND_QID |    |    |    |    |    |    |    |    | VQTX_6_BIND_QID |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    |    | RW              |    |    |    |    |    |    |
| Reset |                 | 0  | 0  | 0  | 0  | 1  | 1  | 1  |    | 0               | 0  | 0  | 0  | 1  | 1  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6               | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | VQTX_5_BIND_QID |    |    |    |    |    |    |    |    | VQTX_4_BIND_QID |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    |    | RW              |    |    |    |    |    |    |
| Reset |                 | 0  | 0  | 0  | 0  | 1  | 0  | 1  |    | 0               | 0  | 0  | 0  | 1  | 0  | 0  |

| Bit(s) | Name            | Description                                                   |
|--------|-----------------|---------------------------------------------------------------|
| 30:24  | VQTX_7_BIND_QID | Physical queue number which binds with Virtual queue group #7 |
| 22:16  | VQTX_6_BIND_QID | Physical queue number which binds with Virtual queue group #6 |
| 14:8   | VQTX_5_BIND_QID | Physical queue number which binds with Virtual queue group #5 |
| 6:0    | VQTX_4_BIND_QID | Physical queue number which binds with Virtual queue group #4 |

151047E0      **QTX\_FC\_SW\_STS\_0\_15**      TX queue#0~15 software path flow control status      00000000

| Bit          | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | QTX_FC_SW_STS_0_15 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | QTX_FC_SW_STS_0_15 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RO                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                                                                                                                                                      |
|--------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | QTX_FC_SW_STS_0_15 | <b>TX Queue Software Path Flow Control Status</b><br><br>Each bit indicates the flow control decision on each physical queue's packet from software path.<br><br>[0]: PQ#0<br><br>....<br><br>[15]: PQ#15<br><br>0: Packet could be en-queued<br><br>1: Current incoming packets will be dropped |

151047EC QDMA\_ULTRA\_CFG QDMA AXI ULTRA configuration 00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26                 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|--------------------|----|----|----|----|----|----|----|----|----|----|
| Name  | AXI_ULTRA_EN    |    |    |    |    | AXI_ULTRA_THRES    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    | RW                 |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               |    |    |    |    | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10                 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | AXI_PREULTRA_EN |    |    |    |    | AXI_PREULTRA_THRES |    |    |    |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    | RW                 |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               |    |    |    |    | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                       |
|--------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | AXI_ULTRA_EN       | <b>Enable AXI Ultra transaction</b><br><br>0: Disable<br><br>1: Enable                                                                                            |
| 26:16  | AXI_ULTRA_THRES    | <b>AXI Ultra threshold.</b><br><br>If CDM TX free FIFO count bigger than AXI_ULTRA_THRES, will trigger AXI Ultra transaction when AXI_ULTRA_EN = 1.               |
| 15     | AXI_PREULTRA_EN    | <b>Enable AXI Pre-ultra transaction</b><br><br>0: Disable<br><br>1: Enable                                                                                        |
| 10:0   | AXI_PREULTRA_THRES | <b>AXI Pre-ultra threshold.</b><br><br>If CDM TX free FIFO count bigger than AXI_PREULTRA_THRES, will trigger AXI Pre-ultra transaction when AXI_PREULTRA_EN = 1. |

151047F0 QDMA\_BUS\_CFG QDMA AXI BUS configuration 00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26               | 25         | 24         | 23 | 22             | 21                  | 20                  | 19                     | 18          | 17           | 16             |
|-------|----|----|----|----|----|------------------|------------|------------|----|----------------|---------------------|---------------------|------------------------|-------------|--------------|----------------|
| Name  |    |    |    |    |    |                  |            |            |    |                |                     |                     | CCI_EN                 | CCI_VQTB_EN | CCI_QRXFQ_EN | CCI_FQ_EN      |
| Type  |    |    |    |    |    |                  |            |            |    |                |                     |                     | RW                     | RW          | RW           | RW             |
| Reset |    |    |    |    |    |                  |            |            |    |                |                     |                     | 0                      | 0           | 0            | 0              |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10               | 9          | 8          | 7  | 6              | 5                   | 4                   | 3                      | 2           | 1            | 0              |
| Name  |    |    |    |    |    | AXI_CTRL_UPDATED | AXI_R_BUSY | AXI_W_BUSY |    | AXI_LOCK_ERROR | AXI_ERRMID_SET_RIRQ | AXI_ERRMID_SET_BIRQ | AXI_OUTSTANDING_EXTEND | AXI_QOS_ON  |              | AXI_CG_DISABLE |
| Type  |    |    |    |    |    | RO               | RO         | RO         |    | RO             | RO                  | RO                  | RW                     | RW          |              | RW             |
| Reset |    |    |    |    |    | 0                | 0          | 0          |    | 0              | 0                   | 0                   | 0                      | 0           |              | 0              |

| Bit(s) | Name                   | Description                                                            |
|--------|------------------------|------------------------------------------------------------------------|
| 19     | CCI_EN                 | QDMA CCI global control bit on BMU, QTX and QRX                        |
| 18     | CCI_VQTB_EN            | BMU VQTB access the bus through CCI if CCI_EN=1                        |
| 17     | CCI_QRXFQ_EN           | QRX FQ_DES access the bus through CCI if CCI_EN=1                      |
| 16     | CCI_FQ_EN              | BMU FQ_DES access the bus through CCI if CCI_EN=1                      |
| 10     | AXI_CTRL_UPDATED       | Master interface control signal updated status                         |
| 9      | AXI_R_BUSY             | Read transaction not completed                                         |
| 8      | AXI_W_BUSY             | Write transaction not completed                                        |
| 6      | AXI_LOCK_ERROR         | Detects lock error                                                     |
| 5      | AXI_ERRMID_SET_RIRQ    | Detects error MID from slave in R channel                              |
| 4      | AXI_ERRMID_SET_BIRQ    | Detects error MID from slave in B channel                              |
| 3      | AXI_OUTSTANDING_EXTEND | Auto adds extra outstanding for QoS command<br>0: Disable<br>1: Enable |
| 2      | AXI_QOS_ON             | Enable QoS function<br>0: Disable<br>1: Enable                         |
| 0      | AXI_CG_DISABLE         | Disable auto clock gating of AXI component<br>0: Disable<br>1: Enable  |

151047F4 QDMA\_RBUS\_CFG QDMA RBUS configuration 00000002

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17        | 16         |
|-------|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|-----------|------------|
| Name  |    |    |    |    |    |    |    |    |             |    |    |    |    |    |           |            |
| Type  |    |    |    |    |    |    |    |    |             |    |    |    |    |    |           |            |
| Reset |    |    |    |    |    |    |    |    |             |    |    |    |    |    |           |            |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3  | 2  | 1         | 0          |
| Name  |    |    |    |    |    |    |    |    | R2X_DBG_SEL |    |    |    |    |    | R2X_INT_B | R2X_INT_EN |
| Type  |    |    |    |    |    |    |    |    | RW          |    |    |    |    |    | RO        | RW         |
| Reset |    |    |    |    |    |    |    |    | 0           | 0  | 0  | 0  |    |    | 1         | 0          |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                                                                                         |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4    | R2X_DBG_SEL | <b>Select debug information from R2X</b><br><br>0: r2x interrupt status<br><br>1: r2x interrupt enable and Rbus status<br><br>2: Rbus address<br><br>3: AXI status<br><br>4: AXI write address<br><br>5: AXI read address<br><br>6: Internal buffer handshake<br><br>7: Coherence sequence and Coherence length<br><br>8: Coherence compare address |
| 1      | R2X_INT_B   | <b>R2X interrupt status</b><br><br>R2X wrapper interrupt will set 1'b1 when receive len = 0 cmd from rbus master.                                                                                                                                                                                                                                   |
| 0      | R2X_INT_EN  | <b>R2X Interrupt Enable</b><br><br>Enable R2X wrapper interrupt when receive len = 0 cmd from rbus master.<br><br>0: Disable<br><br>1: Enable                                                                                                                                                                                                       |

## 4.5 ADMA

### 4.5.1 Register Definition

Module name: ADMAv2 Base address: (+0x15106800)

| Address  | Name                      | Width | Register Function        |
|----------|---------------------------|-------|--------------------------|
| 15106800 | <u>ADMA TX BASE PTR 0</u> | 32    | TX ring #0 base pointer  |
| 15106804 | <u>ADMA TX MAX CNT 0</u>  | 32    | TX ring #0 maximum count |
| 15106808 | <u>ADMA TX CTX IDX 0</u>  | 32    | TX ring #0 CPU pointer   |
| 1510680C | <u>ADMA TX DTX IDX 0</u>  | 32    | TX ring #0 DMA pointer   |
| 15106810 | <u>ADMA TX BASE PTR 1</u> | 32    | TX ring #1 base pointer  |
| 15106814 | <u>ADMA TX MAX CNT 1</u>  | 32    | TX ring #1 maximum count |
| 15106818 | <u>ADMA TX CTX IDX 1</u>  | 32    | TX ring #1 CPU pointer   |
| 1510681C | <u>ADMA TX DTX IDX 1</u>  | 32    | TX ring #1 DMA pointer   |
| 15106820 | <u>ADMA TX BASE PTR 2</u> | 32    | TX ring #2 base pointer  |
| 15106824 | <u>ADMA TX MAX CNT 2</u>  | 32    | TX ring #2 maximum count |
| 15106828 | <u>ADMA TX CTX IDX 2</u>  | 32    | TX ring #2 CPU pointer   |
| 1510682C | <u>ADMA TX DTX IDX 2</u>  | 32    | TX ring #2 DMA pointer   |
| 15106830 | <u>ADMA TX BASE PTR 3</u> | 32    | TX ring #3 base pointer  |
| 15106834 | <u>ADMA TX MAX CNT 3</u>  | 32    | TX ring #3 maximum count |
| 15106838 | <u>ADMA TX CTX IDX 3</u>  | 32    | TX ring #3 CPU pointer   |
| 1510683C | <u>ADMA TX DTX IDX 3</u>  | 32    | TX ring #3 DMA pointer   |
| 15106900 | <u>ADMA RX BASE PTR 0</u> | 32    | RX ring #0 base pointer  |
| 15106904 | <u>ADMA RX MAX CNT 0</u>  | 32    | RX ring #0 maximum count |
| 15106908 | <u>ADMA RX CRX IDX 0</u>  | 32    | RX ring #0 CPU pointer   |
| 1510690C | <u>ADMA RX DRX IDX 0</u>  | 32    | RX ring #0 DMA pointer   |
| 15106910 | <u>ADMA RX BASE PTR 1</u> | 32    | RX ring #1 base pointer  |
| 15106914 | <u>ADMA RX MAX CNT 1</u>  | 32    | RX ring #1 maximum count |
| 15106918 | <u>ADMA RX CRX IDX 1</u>  | 32    | RX ring #1 CPU pointer   |
| 1510691C | <u>ADMA RX DRX IDX 1</u>  | 32    | RX ring #1 DMA pointer   |
| 15106920 | <u>ADMA RX BASE PTR 2</u> | 32    | RX ring #2 base pointer  |
| 15106924 | <u>ADMA RX MAX CNT 2</u>  | 32    | RX ring #2 maximum count |
| 15106928 | <u>ADMA RX CRX IDX 2</u>  | 32    | RX ring #2 CPU pointer   |
| 1510692C | <u>ADMA RX DRX IDX 2</u>  | 32    | RX ring #2 DMA pointer   |
| 15106930 | <u>ADMA RX BASE PTR 3</u> | 32    | RX ring #3 base pointer  |
| 15106934 | <u>ADMA RX MAX CNT 3</u>  | 32    | RX ring #3 maximum count |
| 15106938 | <u>ADMA RX CRX IDX 3</u>  | 32    | RX ring #3 CPU pointer   |
| 1510693C | <u>ADMA RX DRX IDX 3</u>  | 32    | RX ring #3 DMA pointer   |
| 15106940 | <u>ADMA RX BASE PTR 4</u> | 32    | RX ring #4 base pointer  |
| 15106944 | <u>ADMA RX MAX CNT 4</u>  | 32    | RX ring #4 maximum count |
| 15106948 | <u>ADMA RX CRX IDX 4</u>  | 32    | RX ring #4 CPU pointer   |
| 1510694C | <u>ADMA RX DRX IDX 4</u>  | 32    | RX ring #4 DMA pointer   |
| 15106950 | <u>ADMA RX BASE PTR 5</u> | 32    | RX ring #5 base pointer  |
| 15106954 | <u>ADMA RX MAX CNT 5</u>  | 32    | RX ring #5 maximum count |
| 15106958 | <u>ADMA RX CRX IDX 5</u>  | 32    | RX ring #5 CPU pointer   |
| 1510695C | <u>ADMA RX DRX IDX 5</u>  | 32    | RX ring #5 DMA pointer   |
| 15106960 | <u>ADMA RX BASE PTR 6</u> | 32    | RX ring #6 base pointer  |
| 15106964 | <u>ADMA RX MAX CNT 6</u>  | 32    | RX ring #6 maximum count |
| 15106968 | <u>ADMA RX CRX IDX 6</u>  | 32    | RX ring #6 CPU pointer   |

| Address  | Name                           | Width | Register Function                       |
|----------|--------------------------------|-------|-----------------------------------------|
| 1510696C | <u>ADMA_RX_DRX_IDX_6</u>       | 32    | RX ring #6 DMA pointer                  |
| 15106970 | <u>ADMA_RX_BASE_PTR_7</u>      | 32    | RX ring #7 base pointer                 |
| 15106974 | <u>ADMA_RX_MAX_CNT_7</u>       | 32    | RX ring #7 maximum count                |
| 15106978 | <u>ADMA_RX_CRX_IDX_7</u>       | 32    | RX ring #7 CPU pointer                  |
| 1510697C | <u>ADMA_RX_DRX_IDX_7</u>       | 32    | RX ring #7 DMA pointer                  |
| 15106A00 | <u>ADMA_INFO</u>               | 32    | ADMA information                        |
| 15106A04 | <u>ADMA_GLO_CFG</u>            | 32    | ADMA global configuration               |
| 15106A08 | <u>ADMA_RST_IDX</u>            | 32    | ADMA reset index                        |
| 15106A10 | <u>ADMA_RX_CFG</u>             | 32    | ADMA RX DMA configuration               |
| 15106A20 | <u>ADMA_INT_STATUS</u>         | 32    | ADMA interrupt status                   |
| 15106A28 | <u>ADMA_INT_MASK</u>           | 32    | ADMA interrupt mask                     |
| 15106A40 | <u>ADMA_INT_STS_GRP0</u>       | 32    | ADMA interrupt status group 0           |
| 15106A44 | <u>ADMA_INT_STS_GRP1</u>       | 32    | ADMA interrupt status group 1           |
| 15106A48 | <u>ADMA_INT_STS_GRP2</u>       | 32    | ADMA interrupt status group 2           |
| 15106A4C | <u>ADMA_INT_STS_GRP3</u>       | 32    | ADMA interrupt status group 3           |
| 15106A50 | <u>ADMA_INT_GRP1</u>           | 32    | ADMA interrupt group 1 control          |
| 15106A54 | <u>ADMA_INT_GRP2</u>           | 32    | ADMA interrupt group 2 control          |
| 15106A58 | <u>ADMA_INT_GRP3</u>           | 32    | ADMA interrupt group 3 control          |
| 15106A60 | <u>ADMA_BUS_CFG</u>            | 32    | ADMA AXI BUS configuration              |
| 15106A64 | <u>ADMA_ULTRA_CFG</u>          | 32    | ADMA AXI ULTRA configuration            |
| 15106A90 | <u>ADMA_INT_STATUS_0</u>       | 32    | ADMA interrupt status 0                 |
| 15106A94 | <u>ADMA_INT_MASK_0</u>         | 32    | ADMA interrupt mask 0                   |
| 15106A98 | <u>ADMA_INT_STATUS_1</u>       | 32    | ADMA interrupt status 1                 |
| 15106A9C | <u>ADMA_INT_MASK_1</u>         | 32    | ADMA interrupt mask 1                   |
| 15106AA0 | <u>ADMA_INT_STATUS_2</u>       | 32    | ADMA interrupt status 2                 |
| 15106AA4 | <u>ADMA_INT_MASK_2</u>         | 32    | ADMA interrupt mask 2                   |
| 15106AA8 | <u>ADMA_INT_STATUS_3</u>       | 32    | ADMA interrupt status 3                 |
| 15106AAC | <u>ADMA_INT_MASK_3</u>         | 32    | ADMA interrupt mask 3                   |
| 15106AB0 | <u>ADMA_TX_DELAY_INT_CFG_0</u> | 32    | ADMA TX delay interrupt configuration 0 |
| 15106AB4 | <u>ADMA_TX_DELAY_INT_CFG_1</u> | 32    | ADMA TX delay interrupt configuration 1 |
| 15106AC0 | <u>ADMA_RX_DELAY_INT_CFG_0</u> | 32    | ADMA RX delay interrupt configuration 0 |



**15106800 ADMA TX\_BASE\_PTR\_0 TX ring #0 base pointer 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                     |
|--------|-------------|-----------------------------------------------------------------|
| 31:0   | TX_BASE_PTR | Points to the base address of TX ring #0 (4-DW aligned address) |

**15106804 ADMA TX\_MAX\_CNT\_0 TX ring #0 maximum count 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | TX_MAX_CNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                               |
|--------|------------|-------------------------------------------|
| 11:0   | TX_MAX_CNT | Maximum number of TXD count in TX ring #0 |

**15106808 ADMA TX\_CTX\_IDX\_0 TX ring #0 CPU pointer 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | TX_CTX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | TX_CTX_IDX | Points to the next TXD CPU is to use |

**1510680C**      **ADMA TX DTX\_IDX\_0**      **TX ring #0 DMA pointer**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | TX_DTX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | TX_DTX_IDX | Points to the next TXD DMA is to use |

**15106810**      **ADMA TX BASE\_PTR\_1**      **TX ring #1 base pointer**      **00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                     |
|--------|-------------|-----------------------------------------------------------------|
| 31:0   | TX_BASE_PTR | Points to the base address of TX ring #1 (4-DW aligned address) |

15106814 **ADMA TX MAX CNT 1** TX ring #1 maximum count 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | TX_MAX_CNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                               |
|--------|------------|-------------------------------------------|
| 11:0   | TX_MAX_CNT | Maximum number of TXD count in TX ring #1 |

15106818 **ADMA TX CTX IDX 1** TX ring #1 CPU pointer 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | TX_CTX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | TX_CTX_IDX | Points to the next TXD CPU is to use |

**1510681C**      **ADMA TX DTX\_IDX\_1**      **TX ring #1 DMA pointer**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | TX_DTX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | TX_DTX_IDX | Points to the next TXD DMA is to use |

**15106820**      **ADMA TX BASE\_PTR\_2**      **TX ring #2 base pointer**      **00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                     |
|--------|-------------|-----------------------------------------------------------------|
| 31:0   | TX_BASE_PTR | Points to the base address of TX ring #2 (4-DW aligned address) |

15106824 **ADMA TX MAX CNT 2** TX ring #2 maximum count 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | TX_MAX_CNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                               |
|--------|------------|-------------------------------------------|
| 11:0   | TX_MAX_CNT | Maximum number of TXD count in TX ring #2 |

15106828 **ADMA TX CTX IDX 2** TX ring #2 CPU pointer 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | TX_CTX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | TX_CTX_IDX | Points to the next TXD CPU is to use |

**1510682C**      **ADMA TX DTX\_IDX\_2**      **TX ring #2 DMA pointer**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | TX_DTX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | TX_DTX_IDX | Points to the next TXD DMA is to use |

**15106830**      **ADMA TX BASE\_PTR\_3**      **TX ring #3 base pointer**      **00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | TX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | TX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                     |
|--------|-------------|-----------------------------------------------------------------|
| 31:0   | TX_BASE_PTR | Points to the base address of TX ring #3 (4-DW aligned address) |

15106834 **ADMA TX MAX CNT 3** TX ring #3 maximum count 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | TX_MAX_CNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                               |
|--------|------------|-------------------------------------------|
| 11:0   | TX_MAX_CNT | Maximum number of TXD count in TX ring #3 |

15106838 **ADMA TX CTX IDX 3** TX ring #3 CPU pointer 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | TX_CTX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | TX_CTX_IDX | Points to the next TXD CPU is to use |

1510683C ADMA TX DTX\_IDX 3 TX ring #3 DMA pointer 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | TX_DTX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | TX_DTX_IDX | Points to the next TXD DMA is to use |

15106900 ADMA RX\_BASE\_PTR 0 RX ring #0 base pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                     |
|--------|-------------|-----------------------------------------------------------------|
| 31:0   | RX_BASE_PTR | Points to the base address of RX ring #0 (4-DW aligned address) |



15106904 ADMA RX MAX CNT 0 RX ring #0 maximum count 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_MAX_CNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                               |
|--------|------------|-------------------------------------------|
| 11:0   | RX_MAX_CNT | Maximum number of RXD count in RX ring #0 |

15106908 ADMA RX CRX IDX 0 RX ring #0 CPU pointer 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_CRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | RX_CRX_IDX | Points to the next RXD CPU is to use |

1510690C ADMA RX DRX IDX 0 RX ring #0 DMA pointer 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_DRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | RX_DRX_IDX | Points to the next RXD DMA is to use |

**15106910**      **ADMA RX\_BASE\_PTR\_1**      **RX ring #1 base pointer**      **00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                     |
|--------|-------------|-----------------------------------------------------------------|
| 31:0   | RX_BASE_PTR | Points to the base address of RX ring #1 (4-DW aligned address) |

**15106914**      **ADMA RX\_MAX\_CNT\_1**      **RX ring #1 maximum count**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_MAX_CNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                               |
|--------|------------|-------------------------------------------|
| 11:0   | RX_MAX_CNT | Maximum number of RXD count in RX ring #1 |

**15106918**      **ADMA RX CRX\_IDX 1**      **RX ring #1 CPU pointer**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_CRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | RX_CRX_IDX | Points to the next RXD CPU is to use |

**1510691C**      **ADMA RX DRX\_IDX 1**      **RX ring #1 DMA pointer**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_DRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | RX_DRX_IDX | Points to the next RXD DMA is to use |

**15106920**      **ADMA RX\_BASE\_PTR 2**      **RX ring #2 base pointer**      **00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                     |
|--------|-------------|-----------------------------------------------------------------|
| 31:0   | RX_BASE_PTR | Points to the base address of RX ring #2 (4-DW aligned address) |

15106924 **ADMA RX MAX CNT 2** RX ring #2 maximum count 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_MAX_CNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                               |
|--------|------------|-------------------------------------------|
| 11:0   | RX_MAX_CNT | Maximum number of RXD count in RX ring #2 |

15106928 **ADMA RX CRX IDX 2** RX ring #2 CPU pointer 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_CRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | RX_CRX_IDX | Points to the next RXD CPU is to use |

1510692C ADMA RX DRX\_IDX\_2 RX ring #2 DMA pointer 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_DRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | RX_DRX_IDX | Points to the next RXD DMA is to use |

15106930 ADMA RX\_BASE\_PTR\_3 RX ring #3 base pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                     |
|--------|-------------|-----------------------------------------------------------------|
| 31:0   | RX_BASE_PTR | Points to the base address of RX ring #3 (4-DW aligned address) |

15106934 **ADMA RX MAX CNT 3** RX ring #3 maximum count 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_MAX_CNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                               |
|--------|------------|-------------------------------------------|
| 11:0   | RX_MAX_CNT | Maximum number of RXD count in RX ring #3 |

15106938 **ADMA RX CRX IDX 3** RX ring #3 CPU pointer 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_CRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | RX_CRX_IDX | Points to the next RXD CPU is to use |

1510693C ADMA RX DRX\_IDX 3 RX ring #3 DMA pointer 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_DRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | RX_DRX_IDX | Points to the next RXD DMA is to use |

15106940 ADMA RX\_BASE\_PTR 4 RX ring #4 base pointer 00000000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                     |
|--------|-------------|-----------------------------------------------------------------|
| 31:0   | RX_BASE_PTR | Points to the base address of RX ring #4 (4-DW aligned address) |

15106944 **ADMA RX MAX CNT 4** RX ring #4 maximum count 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_MAX_CNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                               |
|--------|------------|-------------------------------------------|
| 11:0   | RX_MAX_CNT | Maximum number of RXD count in RX ring #4 |

15106948 **ADMA RX CRX IDX 4** RX ring #4 CPU pointer 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_CRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | RX_CRX_IDX | Points to the next RXD CPU is to use |



**1510694C ADMA RX DRX\_IDX\_4 RX ring #4 DMA pointer 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_DRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | RX_DRX_IDX | Points to the next RXD DMA is to use |

**15106950 ADMA RX\_BASE\_PTR\_5 RX ring #5 base pointer 00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                     |
|--------|-------------|-----------------------------------------------------------------|
| 31:0   | RX_BASE_PTR | Points to the base address of RX ring #5 (4-DW aligned address) |

**15106954 ADMA RX\_MAX\_CNT\_5 RX ring #5 maximum count 00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_MAX_CNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                               |
|--------|------------|-------------------------------------------|
| 11:0   | RX_MAX_CNT | Maximum number of RXD count in RX ring #5 |

**15106958**      **ADMA RX CRX\_IDX 5**      **RX ring #5 CPU pointer**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_CRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | RX_CRX_IDX | Points to the next RXD CPU is to use |

**1510695C**      **ADMA RX DRX\_IDX 5**      **RX ring #5 DMA pointer**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_DRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | RX_DRX_IDX | Points to the next RXD DMA is to use |

**15106960**      **ADMA RX\_BASE\_PTR 6**      **RX ring #6 base pointer**      **00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                     |
|--------|-------------|-----------------------------------------------------------------|
| 31:0   | RX_BASE_PTR | Points to the base address of RX ring #6 (4-DW aligned address) |

15106964 **ADMA RX MAX CNT 6** RX ring #6 maximum count 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_MAX_CNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                               |
|--------|------------|-------------------------------------------|
| 11:0   | RX_MAX_CNT | Maximum number of RXD count in RX ring #6 |

15106968 **ADMA RX CRX IDX 6** RX ring #6 CPU pointer 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_CRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | RX_CRX_IDX | Points to the next RXD CPU is to use |

1510696C **ADMA RX DRX IDX 6** RX ring #6 DMA pointer 00000000

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_DRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | RX_DRX_IDX | Points to the next RXD DMA is to use |

**15106970**      **ADMA RX\_BASE\_PTR\_7**      **RX ring #7 base pointer**      **00000000**

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_BASE_PTR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name        | Description                                                     |
|--------|-------------|-----------------------------------------------------------------|
| 31:0   | RX_BASE_PTR | Points to the base address of RX ring #7 (4-DW aligned address) |

**15106974**      **ADMA RX\_MAX\_CNT\_7**      **RX ring #7 maximum count**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_MAX_CNT |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                               |
|--------|------------|-------------------------------------------|
| 11:0   | RX_MAX_CNT | Maximum number of RXD count in RX ring #7 |

**15106978**      **ADMA RX\_CRX\_IDX\_7**      **RX ring #7 CPU pointer**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_CRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | RX_CRX_IDX | Points to the next RXD CPU is to use |

**1510697C**      **ADMA\_RX\_DRX\_IDX\_7**      **RX ring #7 DMA pointer**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| Name  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11         | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    | RX_DRX_IDX |    |    |    |    |    |    |    |    |    |    |    |
| Type  |    |    |    |    | RO         |    |    |    |    |    |    |    |    |    |    |    |
| Reset |    |    |    |    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 11:0   | RX_DRX_IDX | Points to the next RXD DMA is to use |

**15106A00**      **ADMA\_INFO**      **ADMA information**      **4C000804**

| Bit   | 31          | 30 | 29 | 28 | 27          | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------|----|----|----|-------------|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  |             |    |    |    | INDEX_WIDTH |    |    |    | BASE_PTR_WIDTH |    |    |    |    |    |    |    |
| Type  |             |    |    |    | RO          |    |    |    | RO             |    |    |    |    |    |    |    |
| Reset |             |    |    |    | 1           | 1  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11          | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RX_RING_NUM |    |    |    |             |    |    |    | TX_RING_NUM    |    |    |    |    |    |    |    |
| Type  | RO          |    |    |    |             |    |    |    | RO             |    |    |    |    |    |    |    |
| Reset | 0           | 0  | 0  | 0  | 1           | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 1  | 0  | 0  |

| Bit(s) | Name           | Description                                                                                                                                                                                     |
|--------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 27:24  | INDEX_WIDTH    | Ring index width                                                                                                                                                                                |
| 23:16  | BASE_PTR_WIDTH | Base pointer width, x<br>Base_addr[31:32-x] is shared with all ring base addresses.<br>Only ring #0 base address[31:32-x] field is writable.<br>Note: 0 means no bit of base_address is shared. |
| 15:8   | RX_RING_NUM    | RX ring number                                                                                                                                                                                  |
| 7:0    | TX_RING_NUM    | TX ring number                                                                                                                                                                                  |

**15106A04 ADMA\_GLO\_CFG ADMA global configuration 50404C70**

| Bit   | 31           | 30              | 29        | 28        | 27        | 26                | 25                 | 24            | 23         | 22          | 21          | 20 | 19           | 18          | 17           | 16          |
|-------|--------------|-----------------|-----------|-----------|-----------|-------------------|--------------------|---------------|------------|-------------|-------------|----|--------------|-------------|--------------|-------------|
| Name  | RX_2B_OFFSET | CSR_CLKGATE_BYP | BYTE_SWAP | DEC_WCOMP | PKT_WCOMP | BYTE_SWAP_BIT_SEL | BIG_ENDIAN_BIT_SEL | LB_MODE       |            |             |             |    |              |             |              |             |
| Type  | RW           | RW              | RW        | RW        | RW        | RW                | RW                 | RW            |            |             |             |    |              |             |              |             |
| Reset | 0            | 1               | 0         | 1         | 0         | 0                 | 0                  | 0             |            |             |             |    |              |             |              |             |
| Bit   | 15           | 14              | 13        | 12        | 11        | 10                | 9                  | 8             | 7          | 6           | 5           | 4  | 3            | 2           | 1            | 0           |
| Name  | MULTI_CNT    |                 |           |           | MULTI_EN  | CHK_DONE          |                    | RX_DMA_LRO_EN | BIG_ENDIAN | TX_WB_DDONE | DMA_BT_SIZE |    | RX_DMA_BUS_Y | RX_DMA_A_EN | TX_DMA_BUS_Y | TX_DMA_A_EN |
| Type  | RW           |                 |           |           | RW        | RW                |                    | RW            | RW         | RW          | RW          |    | RO           | RW          | RO           | RW          |
| Reset | 0            | 1               | 0         | 0         | 1         | 1                 |                    | 0             | 0          | 1           | 1           | 1  | 0            | 0           | 0            | 0           |

| Bit(s) | Name               | Description                                                                                                                                                                                                        |
|--------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | RX_2B_OFFSET       | <p><b>Prepends 2 bytes to RX buffer (packet) for aligning IP header to 32-bit boundary</b></p> <p>Default MAC header: 14 bytes</p> <p>0: Disable 2-byte prepended</p> <p>1: Enable 2-byte prepended</p>            |
| 30     | CSR_CLKGATE_BYP    | <p><b>Bypasses clock gating</b></p> <p>0: DMA clock is gated as idle.</p> <p>1: DMA clock is free-running.</p>                                                                                                     |
| 29     | BYTE_SWAP          | <p><b>Swaps byte</b></p> <p>0: DMA does not swap byte for TX/RX packet descriptor.</p> <p>1: DMA swaps byte for TX/RX packet descriptor.</p>                                                                       |
| 28     | DEC_WCOMP          | <p><b>DMA checks WDONE or WCOMPLETE when updating descriptor into DRAM</b></p> <p>0: DMA checks WDONE when updating descriptor into DRAM.</p> <p>1: DMA checking WCOMPLETE when updating descriptor into DRAM.</p> |
| 27     | PKT_WCOMP          | <p><b>RX_DMA checks WDONE or WCOMPLETE when writing packet into DRAM</b></p> <p>0: RX_DMA checks WDONE when writing packet into DRAM.</p> <p>1: RX_DMA checks WCOMPLETE when writing packet into DRAM.</p>         |
| 26     | BYTE_SWAP_BIT_SEL  | <p><b>Selects bit for byte swap function</b></p> <p>0: 64-bit byte swap mode</p> <p>1: 32-bit byte swap mode</p>                                                                                                   |
| 25     | BIG_ENDIAN_BIT_SEL | <p><b>Selects bit for endian control</b></p> <p>0: 64-bit endian mode</p>                                                                                                                                          |

| Bit(s) | Name          | Description                                                                                                                                                                                                      |
|--------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |               | 1: 32-bit endian mode                                                                                                                                                                                            |
| 24     | LB_MODE       | <b>Power correlation</b><br><br>0: Disable loopback R2T xDMA<br><br>1: Enable loopback R2T xDMA                                                                                                                  |
| 15:12  | MUTLI_CNT     | <b>Number of TX DMA read outstanding transactions when ADMA_GLO_CFG[11] = 1'b1</b><br><br>4'h1: Single issue<br><br>4'h2: 2 read transactions<br><br>4'h4: 4 read transactions<br><br>4'hf: 15 read transactions |
| 11     | MULTI_EN      | <b>Enables TX DAM AXI read outstanding transaction</b><br><br>0: Disable TX DMA read outstanding transaction<br><br>1: Enable TX DMA read outstanding transaction                                                |
| 10     | CHK_DDONE     | <b>Enables DMA checking DDONE</b><br><br>If DDONE = 1, DMA enters coherence protection.<br><br>0: Bypass checking DDONE<br><br>1: Check DDONE                                                                    |
| 8      | RX_DMA_LRO_EN | <b>Enables ADMA RX DMA LRO</b><br><br>0: Disable RX LRO ring<br><br>1: Enable RX LRO ring                                                                                                                        |
| 7      | BIG_ENDIAN    | <b>Big endian</b><br><br>0: DMA does not swap byte for TX/RX packet header and payload<br><br>1: DMA swaps byte for TX/RX packet header and payload                                                              |
| 6      | TX_WB_DDONE   | 0: Disable TX_DMA writing back DDONE into TXD<br><br>1: Enable TX_DMA writing back DDONE into TXD                                                                                                                |
| 5:4    | DMA_BT_SIZE   | <b>Burst size of ADMA</b><br><br>0: Reserved<br><br>1: 8 DWORDs (32 bytes)<br><br>2: 16 DWORDs (64 bytes)<br><br>3: 32 DWORDs (128 bytes)                                                                        |
| 3      | RX_DMA_BUSY   | 0: RX_DMA is not busy.<br><br>1: RX_DMA is busy.                                                                                                                                                                 |

| Bit(s) | Name        | Description                                                                                      |
|--------|-------------|--------------------------------------------------------------------------------------------------|
| 2      | RX_DMA_EN   | 0: Disable RX_DMA (RX_DMA finishes the current receiving packet then stops).<br>1: Enable RX_DMA |
| 1      | TX_DMA_BUSY | 0: TX_DMA is not busy.<br>1: TX_DMA is busy.                                                     |
| 0      | TX_DMA_EN   | 0: Disable TX_DMA (TX_DMA finishes the current sending packet then stops).<br>1: Enable TX_DMA   |



**15106A08**      **ADMA\_RST\_IDX**      **ADMA reset index**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                   | 22                   | 21                   | 20                   | 19                   | 18                   | 17                   | 16                   |
|-------|----|----|----|----|----|----|----|----|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| Name  |    |    |    |    |    |    |    |    | RST_D<br>RX_IDX<br>7 | RST_D<br>RX_IDX<br>6 | RST_D<br>RX_IDX<br>5 | RST_D<br>RX_IDX<br>4 | RST_D<br>RX_IDX<br>3 | RST_D<br>RX_IDX<br>2 | RST_D<br>RX_IDX<br>1 | RST_D<br>RX_IDX<br>0 |
| Type  |    |    |    |    |    |    |    |    | WO                   | WO                   | WO                   | WO                   | WO                   | WO                   | WO                   | WO                   |
| Reset |    |    |    |    |    |    |    |    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7                    | 6                    | 5                    | 4                    | 3                    | 2                    | 1                    | 0                    |
| Name  |    |    |    |    |    |    |    |    |                      |                      |                      |                      | RST_DTX_IDX3         | RST_DTX_IDX2         | RST_DTX_IDX1         | RST_DTX_IDX0         |
| Type  |    |    |    |    |    |    |    |    |                      |                      |                      |                      | WO                   | WO                   | WO                   | WO                   |
| Reset |    |    |    |    |    |    |    |    |                      |                      |                      |                      | 0                    | 0                    | 0                    | 0                    |

| Bit(s) | Name         | Description                           |
|--------|--------------|---------------------------------------|
| 23     | RST_DRX_IDX7 | Write 1 to reset RX_DMA RX_IDX7 to 0. |
| 22     | RST_DRX_IDX6 | Write 1 to reset RX_DMA RX_IDX6 to 0. |
| 21     | RST_DRX_IDX5 | Write 1 to reset RX_DMA RX_IDX5 to 0. |
| 20     | RST_DRX_IDX4 | Write 1 to reset RX_DMA RX_IDX4 to 0. |
| 19     | RST_DRX_IDX3 | Write 1 to reset RX_DMA RX_IDX3 to 0. |
| 18     | RST_DRX_IDX2 | Write 1 to reset RX_DMA RX_IDX2 to 0. |
| 17     | RST_DRX_IDX1 | Write 1 to reset RX_DMA RX_IDX1 to 0. |
| 16     | RST_DRX_IDX0 | Write 1 to reset RX_DMA RX_IDX0 to 0. |
| 3      | RST_DTX_IDX3 | Write 1 to reset TX_DMA TX_IDX3 to 0. |
| 2      | RST_DTX_IDX2 | Write 1 to reset TX_DMA TX_IDX2 to 0. |
| 1      | RST_DTX_IDX1 | Write 1 to reset TX_DMA TX_IDX1 to 0. |
| 0      | RST_DTX_IDX0 | Write 1 to reset TX_DMA TX_IDX0 to 0. |

15106A10      ADMA\_RX\_CFG      ADMA RX DMA configuration      00000002

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19          | 18 | 17 | 16 |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|
| Name  | LRO_SDL |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3           | 2  | 1  | 0  |
| Name  |         |    |    |    |    |    |    |    |    |    |    |    | FREEQ_THRES |    |    |    |
| Type  |         |    |    |    |    |    |    |    |    |    |    |    | RW          |    |    |    |
| Reset |         |    |    |    |    |    |    |    |    |    |    |    | 0           | 0  | 1  | 0  |

| Bit(s) | Name        | Description                                                             |
|--------|-------------|-------------------------------------------------------------------------|
| 31:16  | LRO_SDL     | ADMA LRO free buffer SDL                                                |
| 3:0    | FREEQ_THRES | RX free queue threshold                                                 |
|        |             | ADMA stops DMA interface when left RX descriptors reach this threshold. |

**15106A20 ADMA\_INT\_STATUS ADMA interrupt status 00000000**

| Bit   | 31                       | 30                       | 29                       | 28                       | 27                       | 26                       | 25                       | 24                       | 23                       | 22                       | 21                       | 20                       | 19                   | 18                   | 17                   | 16                   |
|-------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|----------------------|----------------------|----------------------|----------------------|
| Name  | RX_DO<br>NE_DL<br>Y_INT7 | RX_DO<br>NE_DL<br>Y_INT6 | RX_DO<br>NE_DL<br>Y_INT5 | RX_DO<br>NE_DL<br>Y_INT4 | RX_DO<br>NE_DL<br>Y_INT3 | RX_DO<br>NE_DL<br>Y_INT2 | RX_DO<br>NE_DL<br>Y_INT1 | RX_DO<br>NE_DL<br>Y_INT0 | RX_DO<br>NE_INT<br>7     | RX_DO<br>NE_INT<br>6     | RX_DO<br>NE_INT<br>5     | RX_DO<br>NE_INT<br>4     | RX_DO<br>NE_INT<br>3 | RX_DO<br>NE_INT<br>2 | RX_DO<br>NE_INT<br>1 | RX_DO<br>NE_INT<br>0 |
| Type  | W1C                      | W1C                      | W1C                      | W1C                      | W1C                      | W1C                      | W1C                      | W1C                      | W1C                      | W1C                      | W1C                      | W1C                      | W1C                  | W1C                  | W1C                  | W1C                  |
| Reset | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                        | 0                    | 0                    | 0                    | 0                    |
| Bit   | 15                       | 14                       | 13                       | 12                       | 11                       | 10                       | 9                        | 8                        | 7                        | 6                        | 5                        | 4                        | 3                    | 2                    | 1                    | 0                    |
| Name  | RX_CO<br>HEREN<br>T      | RX_DLY<br>_INT           | TX_CO<br>HEREN<br>T      | TX_DLY<br>_INT           |                          |                          |                          |                          | TX_DO<br>NE_DL<br>Y_INT3 | TX_DO<br>NE_DL<br>Y_INT2 | TX_DO<br>NE_DL<br>Y_INT1 | TX_DO<br>NE_DL<br>Y_INT0 | TX_DO<br>NE_INT<br>3 | TX_DO<br>NE_INT<br>2 | TX_DO<br>NE_INT<br>1 | TX_DO<br>NE_INT<br>0 |
| Type  | W1C                      | W1C                      | W1C                      | W1C                      |                          |                          |                          |                          | W1C                      | W1C                      | W1C                      | W1C                      | W1C                  | W1C                  | W1C                  | W1C                  |
| Reset | 0                        | 0                        | 0                        | 0                        |                          |                          |                          |                          | 0                        | 0                        | 0                        | 0                        | 0                    | 0                    | 0                    | 0                    |

| Bit(s) | Name             | Description                                                |
|--------|------------------|------------------------------------------------------------|
| 31     | RX_DONE_DLY_INT7 | RX ring #7 packet receive delay interrupt                  |
| 30     | RX_DONE_DLY_INT6 | RX ring #6 packet receive delay interrupt                  |
| 29     | RX_DONE_DLY_INT5 | RX ring #5 packet receive delay interrupt                  |
| 28     | RX_DONE_DLY_INT4 | RX ring #4 packet receive delay interrupt                  |
| 27     | RX_DONE_DLY_INT3 | RX ring #3 packet receive delay interrupt                  |
| 26     | RX_DONE_DLY_INT2 | RX ring #2 packet receive delay interrupt                  |
| 25     | RX_DONE_DLY_INT1 | RX ring #1 packet receive delay interrupt                  |
| 24     | RX_DONE_DLY_INT0 | RX ring #0 packet receive delay interrupt                  |
| 23     | RX_DONE_INT7     | RX ring #7 packet receive interrupt                        |
| 22     | RX_DONE_INT6     | RX ring #6 packet receive interrupt                        |
| 21     | RX_DONE_INT5     | RX ring #5 packet receive interrupt                        |
| 20     | RX_DONE_INT4     | RX ring #4 packet receive interrupt                        |
| 19     | RX_DONE_INT3     | RX ring #3 packet receive interrupt                        |
| 18     | RX_DONE_INT2     | RX ring #2 packet receive interrupt                        |
| 17     | RX_DONE_INT1     | RX ring #1 packet receive interrupt                        |
| 16     | RX_DONE_INT0     | RX ring #0 packet receive interrupt                        |
| 15     | RX_COHERENT      | RX_DMA finds data coherent event while checking DDONE bit. |
| 14     | RX_DLY_INT       | Summary of entire ADMA RX related interrupts               |
| 13     | TX_COHERENT      | TX_DMA finds data coherent event while checking DDONE bit. |
| 12     | TX_DLY_INT       | Summary of entire ADMA TX related interrupts               |
| 7      | TX_DONE_DLY_INT3 | TX ring #3 packet transmit delay interrupt                 |
| 6      | TX_DONE_DLY_INT2 | TX ring #2 packet transmit delay interrupt                 |
| 5      | TX_DONE_DLY_INT1 | TX ring #1 packet transmit delay interrupt                 |
| 4      | TX_DONE_DLY_INT0 | TX ring #0 packet transmit delay interrupt                 |

| Bit(s) | Name         | Description                          |
|--------|--------------|--------------------------------------|
| 3      | TX_DONE_INT3 | TX ring #3 packet transmit interrupt |
| 2      | TX_DONE_INT2 | TX ring #2 packet transmit interrupt |
| 1      | TX_DONE_INT1 | TX ring #1 packet transmit interrupt |
| 0      | TX_DONE_INT0 | TX ring #0 packet transmit interrupt |

15106A28 ADMA\_INT\_MASK ADMA interrupt mask 00000000

| Bit   | 31                            | 30                            | 29                            | 28                            | 27                            | 26                            | 25                            | 24                            | 23                        | 22                        | 21                        | 20                        | 19                        | 18                        | 17                        | 16                        |
|-------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| Name  | RX_DONE_DL<br>NE_DL<br>Y_INT7 | RX_DONE_DL<br>NE_DL<br>Y_INT6 | RX_DONE_DL<br>NE_DL<br>Y_INT5 | RX_DONE_DL<br>NE_DL<br>Y_INT4 | RX_DONE_DL<br>NE_DL<br>Y_INT3 | RX_DONE_DL<br>NE_DL<br>Y_INT2 | RX_DONE_DL<br>NE_DL<br>Y_INT1 | RX_DONE_DL<br>NE_DL<br>Y_INT0 | RX_DONE_DL<br>NE_INT<br>7 | RX_DONE_DL<br>NE_INT<br>6 | RX_DONE_DL<br>NE_INT<br>5 | RX_DONE_DL<br>NE_INT<br>4 | RX_DONE_DL<br>NE_INT<br>3 | RX_DONE_DL<br>NE_INT<br>2 | RX_DONE_DL<br>NE_INT<br>1 | RX_DONE_DL<br>NE_INT<br>0 |
| Type  | RW                            | RW                            | RW                            | RW                            | RW                            | RW                            | RW                            | RW                            | RW                        | RW                        | RW                        | RW                        | RW                        | RW                        | RW                        | RW                        |
| Reset | 0                             | 0                             | 0                             | 0                             | 0                             | 0                             | 0                             | 0                             | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         |
| Bit   | 15                            | 14                            | 13                            | 12                            | 11                            | 10                            | 9                             | 8                             | 7                         | 6                         | 5                         | 4                         | 3                         | 2                         | 1                         | 0                         |
| Name  | RX_CO<br>HEREN<br>T           | RX_DLY<br>_INT                | TX_CO<br>HEREN<br>T           | TX_DLY<br>_INT                |                               |                               |                               |                               | TX_DO<br>NE_DL<br>Y_INT3  | TX_DO<br>NE_DL<br>Y_INT2  | TX_DO<br>NE_DL<br>Y_INT1  | TX_DO<br>NE_DL<br>Y_INT0  | TX_DO<br>NE_INT<br>3      | TX_DO<br>NE_INT<br>2      | TX_DO<br>NE_INT<br>1      | TX_DO<br>NE_INT<br>0      |
| Type  | RW                            | RW                            | RW                            | RW                            |                               |                               |                               |                               | RW                        | RW                        | RW                        | RW                        | RW                        | RW                        | RW                        | RW                        |
| Reset | 0                             | 0                             | 0                             | 0                             |                               |                               |                               |                               | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         | 0                         |

| Bit(s) | Name             | Description                                                                                     |
|--------|------------------|-------------------------------------------------------------------------------------------------|
| 31     | RX_DONE_DLY_INT7 | <b>RX ring #7 packet receive delay interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt |
| 30     | RX_DONE_DLY_INT6 | <b>RX ring #6 packet receive delay interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt |
| 29     | RX_DONE_DLY_INT5 | <b>RX ring #5 packet receive delay interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt |
| 28     | RX_DONE_DLY_INT4 | <b>RX ring #4 packet receive delay interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt |
| 27     | RX_DONE_DLY_INT3 | <b>RX ring #3 packet receive delay interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt |
| 26     | RX_DONE_DLY_INT2 | <b>RX ring #2 packet receive delay interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt |
| 25     | RX_DONE_DLY_INT1 | <b>RX ring #1 packet receive delay interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt |
| 24     | RX_DONE_DLY_INT0 | <b>RX ring #0 packet receive delay interrupt</b><br>0: Disable interrupt                        |

| Bit(s) | Name         | Description                                                                                                      |
|--------|--------------|------------------------------------------------------------------------------------------------------------------|
|        |              | 1: Enable interrupt                                                                                              |
| 23     | RX_DONE_INT7 | <b>RX ring #7 packet receive interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt                        |
| 22     | RX_DONE_INT6 | <b>RX ring #6 packet receive interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt                        |
| 21     | RX_DONE_INT5 | <b>RX ring #5 packet receive interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt                        |
| 20     | RX_DONE_INT4 | <b>RX ring #4 packet receive interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt                        |
| 19     | RX_DONE_INT3 | <b>RX ring #3 packet receive interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt                        |
| 18     | RX_DONE_INT2 | <b>RX ring #2 packet receive interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt                        |
| 17     | RX_DONE_INT1 | <b>RX ring #1 packet receive interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt                        |
| 16     | RX_DONE_INT0 | <b>RX ring #0 packet receive interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt                        |
| 15     | RX_COHERENT  | <b>RX_DMA finds data coherent event while checking DDONE bit.</b><br>0: Disable interrupt<br>1: Enable interrupt |
| 14     | RX_DLY_INT   | <b>Summary of entire ADMA RX related interrupts</b><br>0: Disable interrupt<br>1: Enable interrupt               |
| 13     | TX_COHERENT  | <b>TX_DMA finds data coherent event while checking DDONE bit.</b>                                                |

| Bit(s) | Name             | Description                                                                                        |
|--------|------------------|----------------------------------------------------------------------------------------------------|
|        |                  | 0: Disable interrupt<br>1: Enable interrupt                                                        |
| 12     | TX_DLY_INT       | <b>Summary of entire ADMA TX related interrupts</b><br>0: Disable interrupt<br>1: Enable interrupt |
| 7      | TX_DONE_DLY_INT3 | <b>TX ring #3 packet transmit delay interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt   |
| 6      | TX_DONE_DLY_INT2 | <b>TX ring #2 packet transmit delay interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt   |
| 5      | TX_DONE_DLY_INT1 | <b>TX ring #1 packet transmit delay interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt   |
| 4      | TX_DONE_DLY_INT0 | <b>TX ring #0 packet transmit delay interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt   |
| 3      | TX_DONE_INT3     | <b>TX ring #3 packet transmit interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt         |
| 2      | TX_DONE_INT2     | <b>TX ring #2 packet transmit interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt         |
| 1      | TX_DONE_INT1     | <b>TX ring #1 packet transmit interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt         |
| 0      | TX_DONE_INT0     | <b>TX ring #0 packet transmit interrupt</b><br>0: Disable interrupt<br>1: Enable interrupt         |

**15106A40**      **ADMA\_INT\_STS\_GRP0**      **ADMA interrupt status group 0**      **00000000**

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | ADMA_INT_STS_GRP0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | ADMA_INT_STS_GRP0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                                                                                                                                                 |
|--------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | ADMA_INT_STS_GRP0 | <b>Interrupt group 0 status</b><br><br>This information already "and" with "~ADMA_INT_GRP1 & ~ADMA_INT_GRP2"<br><br>Each bit's definition is the same as "ADMA_INT_STATUS". |

**15106A44**      **ADMA\_INT\_STS\_GRP1**      **ADMA interrupt status group 1**      **00000000**

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | ADMA_INT_STS_GRP1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | ADMA_INT_STS_GRP1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                                                                                                                               |
|--------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | ADMA_INT_STS_GRP1 | <b>Interrupt group 1 status</b><br><br>This information already "and" with "ADMA_INT_GRP1"<br><br>Each bit's definition is the same as "ADMA_INT_STATUS". |



**15106A48**      **ADMA\_INT\_STS\_GRP2**      **ADMA interrupt status group 2**      **00000000**

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | ADMA_INT_STS_GRP2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | ADMA_INT_STS_GRP2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                                                                                                                               |
|--------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | ADMA_INT_STS_GRP2 | <b>Interrupt group 2 status</b><br><br>This information already "and" with "ADMA_INT_GRP2"<br><br>Each bit's definition is the same as "ADMA_INT_STATUS". |

**15106A4C**      **ADMA\_INT\_STS\_GRP3**      **ADMA interrupt status group 3**      **00000000**

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | ADMA_INT_STS_GRP3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | ADMA_INT_STS_GRP3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                                                                                                                                               |
|--------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | ADMA_INT_STS_GRP3 | <b>Interrupt group 3 status</b><br><br>This information already "and" with "ADMA_INT_GRP3"<br><br>Each bit's definition is the same as "ADMA_INT_STATUS". |

**15106A50 ADMA\_INT\_GRP1 ADMA interrupt group 1 control 00000000**

| Bit          | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | ADMA_INT_GRP1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | ADMA_INT_GRP1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                                                                                                                   |
|--------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | ADMA_INT_GRP1 | <b>Interrupt group 1 assignment</b><br><br>Each bit's definition is the same as "ADMA_INT_STATUS".<br><br>0: Leave to ADMA interrupt group 0, if (ADMA_INT_GRP1[n]==0 & ADMA_INT_GRP2[n]==0 & ADMA_INT_GRP3[n]==0)<br><br>1: Assign to ADMA interrupt group 1 |

**15106A54 ADMA\_INT\_GRP2 ADMA interrupt group 2 control 00000000**

| Bit          | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | ADMA_INT_GRP2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | ADMA_INT_GRP2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                                                                                                                   |
|--------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | ADMA_INT_GRP2 | <b>Interrupt group 2 assignment</b><br><br>Each bit's definition is the same as "ADMA_INT_STATUS".<br><br>0: Leave to ADMA interrupt group 0, if (ADMA_INT_GRP1[n]==0 & ADMA_INT_GRP2[n]==0 & ADMA_INT_GRP3[n]==0)<br><br>1: Assign to ADMA interrupt group 2 |

15106A58      **ADMA\_INT\_GRP3**      **ADMA interrupt group 3 control**      00000000

| Bit          | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | ADMA_INT_GRP3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | ADMA_INT_GRP3 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                                                                                                                                                                                                                  |
|--------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0   | ADMA_INT_GRP3 | <p><b>Interrupt group 3 assignment</b></p> <p>Each bit's definition is the same as "ADMA_INT_STATUS".</p> <p>0: Leave to ADMA interrupt group 0, if (ADMA_INT_GRP1[n]==0 &amp; ADMA_INT_GRP2[n]==0 &amp; ADMA_INT_GRP3[n]==0)</p> <p>1: Assign to ADMA interrupt group 3</p> |

15106A60 ADMA\_BUS\_CFG ADMA AXI BUS configuration 00000400

| Bit   | 31 | 30 | 29 | 28 | 27 | 26               | 25         | 24         | 23 | 22             | 21                  | 20                  | 19                     | 18         | 17 | 16             |
|-------|----|----|----|----|----|------------------|------------|------------|----|----------------|---------------------|---------------------|------------------------|------------|----|----------------|
| Name  |    |    |    |    |    |                  |            |            |    |                |                     |                     |                        |            |    |                |
| Type  |    |    |    |    |    |                  |            |            |    |                |                     |                     |                        |            |    |                |
| Reset |    |    |    |    |    |                  |            |            |    |                |                     |                     |                        |            |    |                |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10               | 9          | 8          | 7  | 6              | 5                   | 4                   | 3                      | 2          | 1  | 0              |
| Name  |    |    |    |    |    | AXI_CTRL_UPDATED | AXI_R_BUSY | AXI_W_BUSY |    | AXI_LOCK_ERROR | AXI_ERRMID_SET_RIRQ | AXI_ERRMID_SET_BIRQ | AXI_OUTSTANDING_EXTEND | AXI_QOS_ON |    | AXI_CG_DISABLE |
| Type  |    |    |    |    |    | RO               | RO         | RO         |    | RO             | RO                  | RO                  | RW                     | RW         |    | RW             |
| Reset |    |    |    |    |    | 1                | 0          | 0          |    | 0              | 0                   | 0                   | 0                      | 0          |    | 0              |

| Bit(s) | Name                   | Description                                                            |
|--------|------------------------|------------------------------------------------------------------------|
| 10     | AXI_CTRL_UPDATED       | Master interface control signal updated status                         |
| 9      | AXI_R_BUSY             | Read transaction not complete                                          |
| 8      | AXI_W_BUSY             | Write transaction not complete                                         |
| 6      | AXI_LOCK_ERROR         | Detects lock error                                                     |
| 5      | AXI_ERRMID_SET_RIRQ    | Detects error MID from slave in R channel                              |
| 4      | AXI_ERRMID_SET_BIRQ    | Detects error MID from slave in B channel                              |
| 3      | AXI_OUTSTANDING_EXTEND | Auto-adds extra outstanding for QoS command<br>0: Disable<br>1: Enable |
| 2      | AXI_QOS_ON             | Enables QoS function<br>0: Disable<br>1: Enable                        |
| 0      | AXI_CG_DISABLE         | Disables auto clock gating of AXI component<br>0: Disable<br>1: Enable |

15106A64 ADMA\_ULTRA\_CFG ADMA AXI ULTRA configuration 00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26                 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|--------------------|----|----|----|----|----|----|----|----|----|----|
| Name  | AXI_ULTRA_EN    |    |    |    |    | AXI_ULTRA_THRES    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    | RW                 |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               |    |    |    |    | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10                 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | AXI_PREULTRA_EN |    |    |    |    | AXI_PREULTRA_THRES |    |    |    |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    | RW                 |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               |    |    |    |    | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                       |
|--------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | AXI_ULTRA_EN       | <b>Enables AXI ultra transaction</b><br><br>0: Disable<br><br>1: Enable                                                                                           |
| 26:16  | AXI_ULTRA_THRES    | <b>AXI ultra threshold</b><br><br>If CDM TX free FIFO count is bigger than AXI_ULTRA_THRES, AXI ultra transaction is triggered when AXI_ULTRA_EN = 1.             |
| 15     | AXI_PREULTRA_EN    | <b>Enables AXI preultra transaction</b><br><br>0: Disable<br><br>1: Enable                                                                                        |
| 10:0   | AXI_PREULTRA_THRES | <b>AXI preultra threshold</b><br><br>If CDM TX free FIFO count is bigger than AXI_PREULTRA_THRES, AXI preultra transaction is triggered when AXI_PREULTRA_EN = 1. |

**15106A90**      **ADMA\_INT\_STATUS\_0**      **ADMA interrupt status 0**      **00000000**

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | INT_STATUS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | INT_STATUS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                |
|--------|------------|------------------------------------------------------------|
| 31:0   | INT_STATUS | Interrupt status<br>Bitmap is the same as ADMA_INT_STATUS. |

**15106A94**      **ADMA\_INT\_MASK\_0**      **ADMA interrupt mask 0**      **00000000**

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | INT_MASK |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | INT_MASK |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name     | Description                                            |
|--------|----------|--------------------------------------------------------|
| 31:0   | INT_MASK | Interrupt mask<br>Bitmap is the same as ADMA_INT_MASK. |

**15106A98**      **ADMA\_INT\_STATUS\_1**      **ADMA interrupt status 1**      **00000000**

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | INT_STATUS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | INT_STATUS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                |
|--------|------------|------------------------------------------------------------|
| 31:0   | INT_STATUS | Interrupt status<br>Bitmap is the same as ADMA_INT_STATUS. |

**15106A9C**      **ADMA\_INT\_MASK\_1**      **ADMA interrupt mask 1**      **00000000**

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | INT_MASK |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | INT_MASK |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name     | Description                                            |
|--------|----------|--------------------------------------------------------|
| 31:0   | INT_MASK | Interrupt mask<br>Bitmap is the same as ADMA_INT_MASK. |

**15106AA0**      **ADMA\_INT\_STATUS\_2**      **ADMA interrupt status 2**      **00000000**

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | INT_STATUS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | INT_STATUS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                |
|--------|------------|------------------------------------------------------------|
| 31:0   | INT_STATUS | Interrupt status<br>Bitmap is the same as ADMA_INT_STATUS. |

**15106AA4**      **ADMA\_INT\_MASK\_2**      **ADMA interrupt mask 2**      **00000000**

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | INT_MASK |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | INT_MASK |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name     | Description                                            |
|--------|----------|--------------------------------------------------------|
| 31:0   | INT_MASK | Interrupt mask<br>Bitmap is the same as ADMA_INT_MASK. |



**15106AA8      ADMA\_INT\_STATUS\_3      ADMA interrupt status 3      00000000**

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | INT_STATUS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | INT_STATUS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | W1C        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name       | Description                                                |
|--------|------------|------------------------------------------------------------|
| 31:0   | INT_STATUS | Interrupt status<br>Bitmap is the same as ADMA_INT_STATUS. |

**15106AAC      ADMA\_INT\_MASK\_3      ADMA interrupt mask 3      00000000**

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | INT_MASK |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | INT_MASK |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name     | Description                                            |
|--------|----------|--------------------------------------------------------|
| 31:0   | INT_MASK | Interrupt mask<br>Bitmap is the same as ADMA_INT_MASK. |

**15106AB0 ADMA\_TX\_DELAY\_INT\_CFG\_0** ADMA TX delay interrupt configuration 0 **00000000**

| Bit   | 31                 | 30               | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|------------------|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| Name  | RING1_TXDLY_INT_EN | RING1_TXMAX_PINT |    |    |    |    |    |    | RING1_TXMAX_PTIME |    |    |    |    |    |    |    |
| Type  | RW                 | RW               |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                  | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14               | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RING0_TXDLY_INT_EN | RING0_TXMAX_PINT |    |    |    |    |    |    | RING0_TXMAX_PTIME |    |    |    |    |    |    |    |
| Type  | RW                 | RW               |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                  | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                  |
|--------|--------------------|------------------------------------------------------------------------------------------------------------------------------|
| 31     | RING1_TXDLY_INT_EN | <b>Enables delay interrupt mechanism for TX ring 1</b><br><br>0: Disable<br><br>1: Enable                                    |
| 30:24  | RING1_TXMAX_PINT   | <b>Specified maximum number of pending interrupts</b><br><br>Note: Reset this to 0 to disable pending interrupt count check. |
| 23:16  | RING1_TXMAX_PTIME  | <b>Specified maximum pending time</b><br><br>Note: Reset this to 0 to disable pending interrupt time check.                  |
| 15     | RING0_TXDLY_INT_EN | <b>Enables delay interrupt mechanism for TX ring 0</b><br><br>0: Disable<br><br>1: Enable                                    |
| 14:8   | RING0_TXMAX_PINT   | <b>Specified maximum number of pending interrupts</b><br><br>Note: Reset this to 0 to disable pending interrupt count check. |
| 7:0    | RING0_TXMAX_PTIME  | <b>Specified maximum pending time</b><br><br>Note: Reset this to 0 to disable pending interrupt time check.                  |

15106AB4 ADMA\_TX\_DELAY\_INT\_CFG\_1ADMA TX delay interrupt configuration 1 00000000

| Bit   | 31                 | 30               | 29 | 28 | 27 | 26 | 25 | 24 | 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|------------------|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| Name  | RING3_TXDLY_INT_EN | RING3_TXMAX_PINT |    |    |    |    |    |    | RING3_TXMAX_PTIME |    |    |    |    |    |    |    |
| Type  | RW                 | RW               |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                  | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14               | 13 | 12 | 11 | 10 | 9  | 8  | 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RING2_TXDLY_INT_EN | RING2_TXMAX_PINT |    |    |    |    |    |    | RING2_TXMAX_PTIME |    |    |    |    |    |    |    |
| Type  | RW                 | RW               |    |    |    |    |    |    | RW                |    |    |    |    |    |    |    |
| Reset | 0                  | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                  |
|--------|--------------------|------------------------------------------------------------------------------------------------------------------------------|
| 31     | RING3_TXDLY_INT_EN | <b>Enables delay interrupt mechanism for TX ring 3</b><br><br>0: Disable<br><br>1: Enable                                    |
| 30:24  | RING3_TXMAX_PINT   | <b>Specified maximum number of pending interrupts</b><br><br>Note: Reset this to 0 to disable pending interrupt count check. |
| 23:16  | RING3_TXMAX_PTIME  | <b>Specified maximum pending time</b><br><br>Note: Reset this to 0 to disable pending interrupt time check.                  |
| 15     | RING2_TXDLY_INT_EN | <b>Enables delay interrupt mechanism for TX ring 2</b><br><br>0: Disable<br><br>1: Enable                                    |
| 14:8   | RING2_TXMAX_PINT   | <b>Specified maximum number of pending interrupts</b><br><br>Note: Reset this to 0 to disable pending interrupt count check. |
| 7:0    | RING2_TXMAX_PTIME  | <b>Specified maximum pending time</b><br><br>Note: Reset this to 0 to disable pending interrupt time check.                  |

15106AC0 ADMA\_RX\_DELAY\_INT\_CFG ADMA RX delay interrupt configuration 0

00000000

0

| Bit   | 31                     | 30                  | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22                   | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------------|---------------------|----|----|----|----|----|----|----|----------------------|----|----|----|----|----|----|
| Name  | RING_4_7_RX_DLY_INT_EN | RING_4_7_RXMAX_PINT |    |    |    |    |    |    |    | RING_4_7_RXMAX_PTIME |    |    |    |    |    |    |
| Type  | RW                     | RW                  |    |    |    |    |    |    |    | RW                   |    |    |    |    |    |    |
| Reset | 0                      | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                    | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                     | 14                  | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6                    | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | RING_0_3_RX_DLY_INT_EN | RING_0_3_RXMAX_PINT |    |    |    |    |    |    |    | RING_0_3_RXMAX_PTIME |    |    |    |    |    |    |
| Type  | RW                     | RW                  |    |    |    |    |    |    |    | RW                   |    |    |    |    |    |    |
| Reset | 0                      | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                    | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                  | Description                                                                                                                                  |
|--------|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | RING_4_7_RXDLY_INT_EN | <b>Enables delay interrupt mechanism for RX ring 4~7</b><br><br>0: Disable<br><br>1: Enable                                                  |
| 30:24  | RING_4_7_RXMAX_PINT   | <b>Specified maximum number of pending interrupts for RX ring 4~7</b><br><br>Note: Reset this to 0 to disable pending interrupt count check. |
| 23:16  | RING_4_7_RXMAX_PTIME  | <b>Specified maximum pending time for RX ring 4~7</b><br><br>Note: Reset this to 0 to disable pending interrupt time check.                  |
| 15     | RING_0_3_RXDLY_INT_EN | <b>Enables delay interrupt mechanism for RX ring 0~3</b><br><br>0: Disable<br><br>1: Enable                                                  |
| 14:8   | RING_0_3_RXMAX_PINT   | <b>Specified maximum number of pending interrupts for RX ring 0~3</b><br><br>Note: Reset this to 0 to disable pending interrupt count check. |
| 7:0    | RING_0_3_RXMAX_PTIME  | <b>Specified maximum pending time for RX ring 0~3</b><br><br>Note: Reset this to 0 to disable pending interrupt time check.                  |

## 4.6 LRO

### 4.6.1 Register Definition

Module name: LRO2 Base address: (+0x15106C00)

| Address  | Name                         | Width | Register Function              |
|----------|------------------------------|-------|--------------------------------|
| 15106C08 | <u>LRO2_CTRL_DW0</u>         | 32    | LRO2 control register          |
| 15106C0C | <u>LRO2_CTRL_DW1</u>         | 32    | LRO2 control register          |
| 15106C10 | <u>LRO2_CTRL_DW2</u>         | 32    | LRO2 control register          |
| 15106C14 | <u>LRO2_CTRL_DW3</u>         | 32    | LRO2 control register          |
| 15106C18 | <u>LRO2_CTRL_DW4</u>         | 32    | LRO2 control register          |
| 15106C1C | <u>LRO2_ALT_SCORE_DELTA</u>  | 32    | LRO2 control register          |
| 15106C20 | <u>LRO2_TIMEOUT_FLAG</u>     | 32    | LRO2 timeout flag              |
| 15106C30 | <u>LRO2_RING1_STS</u>        | 32    | LRO2 ring 1 status             |
| 15106C34 | <u>LRO2_RING2_STS</u>        | 32    | LRO2 ring 2 status             |
| 15106C38 | <u>LRO2_RING3_STS</u>        | 32    | LRO2 ring 3 status             |
| 15106C3C | <u>LRO2_RING4_STS</u>        | 32    | LRO2 ring 4 status             |
| 15106C50 | <u>LRO2_RING1_STP_DTP_DW</u> | 32    | Source TCP port number         |
| 15106C54 | <u>LRO2_RING1_DIP_DW0</u>    | 32    | Destination IP address[31:0]   |
| 15106C58 | <u>LRO2_RING1_DIP_DW1</u>    | 32    | Destination IP address[63:32]  |
| 15106C5C | <u>LRO2_RING1_DIP_DW2</u>    | 32    | Destination IP address[95:64]  |
| 15106C60 | <u>LRO2_RING1_DIP_DW3</u>    | 32    | Destination IP address[127:96] |
| 15106C64 | <u>LRO2_RING1_SIP_DW0</u>    | 32    | Source IP address[31:0]        |
| 15106C68 | <u>LRO2_RING1_SIP_DW1</u>    | 32    | Source IP address[63:32]       |
| 15106C6C | <u>LRO2_RING1_SIP_DW2</u>    | 32    | Source IP address[95:64]       |
| 15106C70 | <u>LRO2_RING1_SIP_DW3</u>    | 32    | Source IP address[127:96]      |
| 15106C74 | <u>LRO2_RING1_CTRL_DW0</u>   | 32    | I2_vlan_vid_I2_I               |
| 15106C78 | <u>LRO2_RING1_CTRL_DW1</u>   | 32    | RX ring age time[9:0]          |
| 15106C7C | <u>LRO2_RING1_CTRL_DW2</u>   | 32    | LRO2_MAX_AGGREGATED_CNT_L      |
| 15106C80 | <u>LRO2_RING1_CTRL_DW3</u>   | 32    | Reserved                       |
| 15106C90 | <u>LRO2_RING2_STP_DTP_DW</u> | 32    | Source TCP port number         |
| 15106C94 | <u>LRO2_RING2_DIP_DW0</u>    | 32    | Destination IP address[31:0]   |
| 15106C98 | <u>LRO2_RING2_DIP_DW1</u>    | 32    | Destination IP address[63:32]  |
| 15106C9C | <u>LRO2_RING2_DIP_DW2</u>    | 32    | Destination IP address[95:64]  |
| 15106CA0 | <u>LRO2_RING2_DIP_DW3</u>    | 32    | Destination IP address[127:96] |
| 15106CA4 | <u>LRO2_RING2_SIP_DW0</u>    | 32    | Source IP address[31:0]        |
| 15106CA8 | <u>LRO2_RING2_SIP_DW1</u>    | 32    | Source IP address[63:32]       |
| 15106CAC | <u>LRO2_RING2_SIP_DW2</u>    | 32    | Source IP address[95:64]       |
| 15106CB0 | <u>LRO2_RING2_SIP_DW3</u>    | 32    | Source IP address[127:96]      |
| 15106CB4 | <u>LRO2_RING2_CTRL_DW0</u>   | 32    | I2_vlan_vid_I2_I               |
| 15106CB8 | <u>LRO2_RING2_CTRL_DW1</u>   | 32    | RX ring age time[9:0]          |
| 15106CBC | <u>LRO2_RING2_CTRL_DW2</u>   | 32    | LRO2_MAX_AGGREGATED_CNT_L      |
| 15106CC0 | <u>LRO2_RING2_CTRL_DW3</u>   | 32    | Reserved                       |
| 15106CD0 | <u>LRO2_RING3_STP_DTP_DW</u> | 32    | Source TCP port number         |
| 15106CD4 | <u>LRO2_RING3_DIP_DW0</u>    | 32    | Destination IP address[31:0]   |
| 15106CD8 | <u>LRO2_RING3_DIP_DW1</u>    | 32    | Destination IP address[63:32]  |
| 15106CDC | <u>LRO2_RING3_DIP_DW2</u>    | 32    | Destination IP address[95:64]  |
| 15106CE0 | <u>LRO2_RING3_DIP_DW3</u>    | 32    | Destination IP address[127:96] |
| 15106CE4 | <u>LRO2_RING3_SIP_DW0</u>    | 32    | Source IP address[31:0]        |

| Address  | Name                         | Width | Register Function              |
|----------|------------------------------|-------|--------------------------------|
| 15106CE8 | <u>LRO2_RING3_SIP_DW1</u>    | 32    | Source IP address[63:32]       |
| 15106CEC | <u>LRO2_RING3_SIP_DW2</u>    | 32    | Source IP address[95:64]       |
| 15106CF0 | <u>LRO2_RING3_SIP_DW3</u>    | 32    | Source IP address[127:96]      |
| 15106CF4 | <u>LRO2_RING3_CTRL_DW0</u>   | 32    | I2_vlan_vid_I2_I               |
| 15106CF8 | <u>LRO2_RING3_CTRL_DW1</u>   | 32    | RX ring age time[9:0]          |
| 15106CFC | <u>LRO2_RING3_CTRL_DW2</u>   | 32    | LRO2_MAX_AGGREGATED_CNT_L      |
| 15106D00 | <u>LRO2_RING3_CTRL_DW3</u>   | 32    | Reserved                       |
| 15106D10 | <u>LRO2_RING4_STP_DTP_DW</u> | 32    | Source TCP port number         |
| 15106D14 | <u>LRO2_RING4_DIP_DW0</u>    | 32    | Destination IP address[31:0]   |
| 15106D18 | <u>LRO2_RING4_DIP_DW1</u>    | 32    | Destination IP address[63:32]  |
| 15106D1C | <u>LRO2_RING4_DIP_DW2</u>    | 32    | Destination IP address[95:64]  |
| 15106D20 | <u>LRO2_RING4_DIP_DW3</u>    | 32    | Destination IP address[127:96] |
| 15106D24 | <u>LRO2_RING4_SIP_DW0</u>    | 32    | Source IP address[31:0]        |
| 15106D28 | <u>LRO2_RING4_SIP_DW1</u>    | 32    | Source IP address[63:32]       |
| 15106D2C | <u>LRO2_RING4_SIP_DW2</u>    | 32    | Source IP address[95:64]       |
| 15106D30 | <u>LRO2_RING4_SIP_DW3</u>    | 32    | Source IP address[127:96]      |
| 15106D34 | <u>LRO2_RING4_CTRL_DW0</u>   | 32    | I2_vlan_vid_I2_I               |
| 15106D38 | <u>LRO2_RING4_CTRL_DW1</u>   | 32    | RX ring age time[9:0]          |
| 15106D3C | <u>LRO2_RING4_CTRL_DW2</u>   | 32    | LRO2_MAX_AGGREGATED_CNT_L      |
| 15106D40 | <u>LRO2_RING4_CTRL_DW3</u>   | 32    | Reserved                       |

**15106C08      LRO2\_CTRL\_DW0      LRO2 control register      F0884000**

| Bit   | 31                   | 30 | 29 | 28 | 27                  | 26 | 25 | 24 | 23                | 22           | 21                | 20                                 | 19                   | 18      | 17 | 16 |
|-------|----------------------|----|----|----|---------------------|----|----|----|-------------------|--------------|-------------------|------------------------------------|----------------------|---------|----|----|
| Name  | RING_RELINGUISH_DONE |    |    |    | RING_RELINGUISH_REQ |    |    |    | cr_l4_ctrl_psh_en | lro_crsn_bnw | cr_alt_score_mode | first_ineligible_pkt_redirected_en | L3_CKS_UPD_EN        | SDL     |    |    |
| Type  | RO                   |    |    |    | RW                  |    |    |    | RW                | RW           | RW                | RW                                 | RW                   | RW      |    |    |
| Reset | 1                    | 1  | 1  | 1  | 0                   | 0  | 0  | 0  | 1                 | 0            | 0                 | 0                                  | 1                    | 0       | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11                  | 10 | 9  | 8  | 7                 | 6            | 5                 | 4                                  | 3                    | 2       | 1  | 0  |
| Name  | SDL                  |    |    |    |                     |    |    |    |                   |              |                   |                                    | MULTIPLE_NON_RING_EN | IPv6_EN | EN |    |
| Type  | RW                   |    |    |    |                     |    |    |    |                   |              |                   |                                    | RW                   | RW      | RW |    |
| Reset | 0                    | 1  | 0  | 0  | 0                   | 0  | 0  | 0  | 0                 | 0            | 0                 | 0                                  | 0                    | 0       | 0  | 0  |

| Bit(s) | Name                               | Description                                                                                                                                                                                    |
|--------|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | RING_RELINGUISH_DONE               | Indicates there are relinquished rings                                                                                                                                                         |
| 27:24  | RING_RELINGUISH_REQ                | FW requests to flush aggregated packets by writing 1, and then 0                                                                                                                               |
| 23     | cr_l4_ctrl_psh_en                  | 0: Disable I4 PSH LRO eligibility check<br>1: Push asserted is LRO ineligible                                                                                                                  |
| 22     | lro_crsn_bnw                       | <b>lro_crsn_bnw</b><br>1: Black list<br>0: White list                                                                                                                                          |
| 21     | cr_alt_score_mode                  | 0: Throughput (byte count)<br>1: Packet count                                                                                                                                                  |
| 20     | first_ineligible_pkt_redirected_en | In order to save one LRO RXD with large sdl0 (64KB), it is better to redirect ineligible packet into Normal ring when the hit LRO ring is clean and empty without existing aggregated packets. |
| 19     | L3_CKS_UPD_EN                      | <b>IPv4 checksum update enable</b><br>1: Enable<br>0: Disable                                                                                                                                  |
| 18:3   | SDL                                | <b>Max aggregated packet length</b>                                                                                                                                                            |
| 2      | MULTIPLE_NON_RING_EN               | <b>To enable multiple non-LRO RX rings</b><br>0: Multiple non-LRO RX rings disable<br>1: Multiple non-LRO RX rings enable                                                                      |
| 1      | IPv6_EN                            | <b>Enable bit for IPv6 packet LRO</b><br>0: Disable LRO to IPv6 flow<br>1: Enable LRO to IPv6 flow                                                                                             |
| 0      | EN                                 | <b>Enable bit to activate RX LRO feature</b>                                                                                                                                                   |

| Bit(s) | Name | Description    |
|--------|------|----------------|
|        |      | 0: Disable LRO |
|        |      | 1: Enable LRO  |

**15106C0C**      **LRO2\_CTRL\_DW1**      **LRO2 control register**      **1F1E1F1E**

| Bit          | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | <b>CPU_REASON</b> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 0  |
| Bit          | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | <b>CPU_REASON</b> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                 | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 0  |

| Bit(s) | Name       | Description                          |
|--------|------------|--------------------------------------|
| 31:0   | CPU_REASON | CPU reason code set (5b per reason). |

**15106C10**      **LRO2\_CTRL\_DW2**      **LRO2 control register**      **00000000**

| Bit          | 31                                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|--------------|--------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| <b>Name</b>  | <b>AUTO_LEARN_ELIGIBLE_THRESHOLD</b> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit          | 15                                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| <b>Name</b>  | <b>AUTO_LEARN_ELIGIBLE_THRESHOLD</b> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Type</b>  | RW                                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b> | 0                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                          | Description                                             |
|--------|-------------------------------|---------------------------------------------------------|
| 31:0   | AUTO_LEARN_ELIGIBLE_THRESHOLD | Min threshold to become a candidate for LRO aggregation |



**15106C14**      **LRO2\_CTRL\_DW3**      **LRO2 control register**      **05F20F00**

| Bit   | 31           | 30 | 29                 | 28 | 27      | 26 | 25 | 24 | 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|--------------------|----|---------|----|----|----|-----|----|----|----|----|----|----|----|
| Name  | MIN_RXD_SDLO |    |                    |    |         |    |    |    |     |    |    |    |    |    |    |    |
| Type  | RW           |    |                    |    |         |    |    |    |     |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0                  | 0  | 0       | 1  | 0  | 1  | 1   | 1  | 1  | 1  | 0  | 0  | 1  | 0  |
| Bit   | 15           | 14 | 13                 | 12 | 11      | 10 | 9  | 8  | 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | CAND_WGT_IDX |    | VLAN_VID_CMP_DEPTH |    | VLAN_EN |    |    |    | REV |    |    |    |    |    |    |    |
| Type  | RW           |    | RW                 |    | RW      |    |    |    | RW  |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0                  | 0  | 1       | 1  | 1  | 1  | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                                                                                                                                                                                                                                                                                              |
|--------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16  | MIN_RXD_SDLO       | <b>The least remaining room of SDLO in RXD for LRO aggregation.</b><br><br>It should be greater than the maximum size of packet which RX MAC can accept without dropping. That is, MIN_RXD_SDLO MUST be equal to or greater than MAX_RX_JUMBO/MAC_RX_PKT_LEN fields in CR MAC_P*_MCR(address: 1B11_0100) |
| 15:14  | CAND_WGT_IDX       | <b>Candidate weight index</b><br><br>Estimated candidate weight value = throughput >> {CAND_WGT_IDX,1'b0}                                                                                                                                                                                                |
| 13:12  | VLAN_VID_CMP_DEPTH | <b>Determines the depth of VLAN ID that needs to be compared</b>                                                                                                                                                                                                                                         |
| 11:8   | VLAN_EN            | <b>Supports max 4-depth VLAN for LRO</b>                                                                                                                                                                                                                                                                 |
| 7:0    | REV                | <b>Reserved</b>                                                                                                                                                                                                                                                                                          |

**15106C18**      **LRO2\_CTRL\_DW4**      **LRO2 control register**      **00008100**

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|
| Name  | REV      |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SPC_TAG_EN |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW         |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| Name  | EXT_TPID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |
| Reset | 1        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          |

| Bit(s) | Name       | Description        |
|--------|------------|--------------------|
| 31:17  | REV        | Reserved           |
| 16     | SPC_TAG_EN | Special tag enable |
| 15:0   | EXT_TPID   | User extended TPID |

**15106C1C**      **LRO2\_ALT\_SCORE\_DELTA**      **LRO2 control register**      **00000000**

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | ALT_SCORE_DELTA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | ALT_SCORE_DELTA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                    |
|--------|-----------------|----------------------------------------------------------------|
| 31:0   | ALT_SCORE_DELTA | To add a delta before determining whether to replace it or not |

**15106C20**      **LRO2\_TIMEOUT\_FLAG**      **LRO2 timeout flag**      **00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19          | 18 | 17 | 16   |
|-------|------|----|----|----|----|----|----|----|-------------|----|----|----|-------------|----|----|------|
| Name  | REV0 |    |    |    |    |    |    |    |             |    |    |    |             |    |    |      |
| Type  | RO   |    |    |    |    |    |    |    |             |    |    |    |             |    |    |      |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0    |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7           | 6  | 5  | 4  | 3           | 2  | 1  | 0    |
| Name  | REV0 |    |    |    |    |    |    |    | AGE_TIMEOUT |    |    |    | AGG_TIMEOUT |    |    | BUSY |
| Type  | RO   |    |    |    |    |    |    |    | RC          |    |    |    | RC          |    |    | RC   |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0    |

| Bit(s) | Name        | Description                                                                                   |
|--------|-------------|-----------------------------------------------------------------------------------------------|
| 31:9   | REV0        | Reserved                                                                                      |
| 8:5    | AGE_TIMEOUT | If the ring times out, the related bit will be on. After CR reading, the bit will be cleared. |
| 4:1    | AGG_TIMEOUT | If the ring times out, the related bit will be on. After CR reading, the bit will be cleared. |
| 0      | BUSY        | LRO busy                                                                                      |

**15106C30**      **LRO2\_RING1\_STS**      **LRO2 ring 1 status**      **00000100**

| Bit   | 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23           | 22      | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|----|----|----|----|----|----|----|--------------|---------|----|----|----|----|----|----|
| Name  | REV |    |    |    |    |    |    |    |              |         |    |    |    |    |    |    |
| Type  | RO  |    |    |    |    |    |    |    |              |         |    |    |    |    |    |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0            | 0       | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7            | 6       | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | REV |    |    |    |    |    |    |    | AGG_CNT_ZERO | AGG_CNT |    |    |    |    |    |    |
| Type  | RO  |    |    |    |    |    |    |    | RO           | RO      |    |    |    |    |    |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1            | 0       | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                     |
|--------|--------------|---------------------------------------------------------------------------------|
| 31:9   | REV          | Reserved                                                                        |
| 8      | AGG_CNT_ZERO | 1'b1: There is no aggregated packet<br>1'b0: There is already aggregated packet |
| 7:0    | AGG_CNT      | Current aggregated packet count number                                          |

**15106C34      LRO2\_RING2\_STS      LRO2 ring 2 status      00000100**

| Bit   | 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24                   | 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|----|----|----|----|----|----|----------------------|---------|----|----|----|----|----|----|----|
| Name  | REV |    |    |    |    |    |    |                      |         |    |    |    |    |    |    |    |
| Type  | RO  |    |    |    |    |    |    |                      |         |    |    |    |    |    |    |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0                    | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8                    | 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | REV |    |    |    |    |    |    | AGG_C<br>NT_ZER<br>O | AGG_CNT |    |    |    |    |    |    |    |
| Type  | RO  |    |    |    |    |    |    | RO                   | RO      |    |    |    |    |    |    |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 1                    | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                     |
|--------|--------------|---------------------------------------------------------------------------------|
| 31:9   | REV          | Reserved                                                                        |
| 8      | AGG_CNT_ZERO | 1'b1: There is no aggregated packet<br>1'b0: There is already aggregated packet |
| 7:0    | AGG_CNT      | Current aggregated packet count number                                          |

**15106C38      LRO2\_RING3\_STS      LRO2 ring 3 status      00000100**

| Bit   | 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24                   | 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|----|----|----|----|----|----|----------------------|---------|----|----|----|----|----|----|----|
| Name  | REV |    |    |    |    |    |    |                      |         |    |    |    |    |    |    |    |
| Type  | RO  |    |    |    |    |    |    |                      |         |    |    |    |    |    |    |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0                    | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8                    | 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | REV |    |    |    |    |    |    | AGG_C<br>NT_ZER<br>O | AGG_CNT |    |    |    |    |    |    |    |
| Type  | RO  |    |    |    |    |    |    | RO                   | RO      |    |    |    |    |    |    |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 1                    | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                     |
|--------|--------------|---------------------------------------------------------------------------------|
| 31:9   | REV          | Reserved                                                                        |
| 8      | AGG_CNT_ZERO | 1'b1: There is no aggregated packet<br>1'b0: There is already aggregated packet |
| 7:0    | AGG_CNT      | Current aggregated packet count number                                          |

15106C3C      LRO2\_RING4\_STS      LRO2 ring 4 status      00000100

| Bit   | 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24           | 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|----|----|----|----|----|----|--------------|---------|----|----|----|----|----|----|----|
| Name  | REV |    |    |    |    |    |    |              |         |    |    |    |    |    |    |    |
| Type  | RO  |    |    |    |    |    |    |              |         |    |    |    |    |    |    |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0            | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8            | 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | REV |    |    |    |    |    |    | AGG_CNT_ZERO | AGG_CNT |    |    |    |    |    |    |    |
| Type  | RO  |    |    |    |    |    |    | RO           | RO      |    |    |    |    |    |    |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 1            | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description                                                                     |
|--------|--------------|---------------------------------------------------------------------------------|
| 31:9   | REV          | Reserved                                                                        |
| 8      | AGG_CNT_ZERO | 1'b1: There is no aggregated packet<br>1'b0: There is already aggregated packet |
| 7:0    | AGG_CNT      | Current aggregated packet count number                                          |

15106C50      LRO2\_RING1\_STP\_DTP\_DW      Source TCP port number      00000000

| Bit   | 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | STP |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DTP |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                 |
|--------|------|-----------------------------|
| 31:16  | STP  | Source TCP port number      |
| 15:0   | DTP  | Destination TCP port number |

**15106C54**      **LRO2\_RING1\_DIP\_DW0**      **Destination IP address[31:0]**      **00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                  |
|--------|------|------------------------------|
| 31:0   | DATA | Destination IP address[31:0] |

**15106C58**      **LRO2\_RING1\_DIP\_DW1**      **Destination IP address[63:32]**      **00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                   |
|--------|------|-------------------------------|
| 31:0   | DATA | Destination IP address[63:32] |

**15106C5C**      **LRO2\_RING1\_DIP\_DW2**      **Destination IP address[95:64]**      **00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                   |
|--------|------|-------------------------------|
| 31:0   | DATA | Destination IP address[95:64] |

**15106C60**      **LRO2\_RING1\_DIP\_DW3**      **Destination IP address[127:96]**      **00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                    |
|--------|------|--------------------------------|
| 31:0   | DATA | Destination IP address[127:96] |

**15106C64**      **LRO2\_RING1\_SIP\_DW0**      **Source IP address[31:0]**      **00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description             |
|--------|------|-------------------------|
| 31:0   | DATA | Source IP address[31:0] |

**15106C68**      **LRO2\_RING1\_SIP\_DW1**      **Source IP address[63:32]**      **00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description              |
|--------|------|--------------------------|
| 31:0   | DATA | Source IP address[63:32] |

15106C6C      LRO2\_RING1\_SIP\_DW2      Source IP address[95:64]      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description              |
|--------|------|--------------------------|
| 31:0   | DATA | Source IP address[95:64] |

15106C70      LRO2\_RING1\_SIP\_DW3      Source IP address[127:96]      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description               |
|--------|------|---------------------------|
| 31:0   | DATA | Source IP address[127:96] |



15106C74 LRO2\_RING1\_CTRL\_DW0 l2\_vlan\_vid\_l2\_l 00000002

| Bit   | 31            | 30 | 29          | 28 | 27 | 26 | 25          | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17           | 16           |
|-------|---------------|----|-------------|----|----|----|-------------|----|----|----|----|----|----|----|--------------|--------------|
| Name  | VLAN_VID_L2_L |    |             |    |    |    | VLAN_VID_L1 |    |    |    |    |    |    |    |              |              |
| Type  | RW            |    |             |    |    |    | RW          |    |    |    |    |    |    |    |              |              |
| Reset | 0             | 0  | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0            | 0            |
| Bit   | 15            | 14 | 13          | 12 | 11 | 10 | 9           | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1            | 0            |
| Name  | VLAN_VID_L1   |    | VLAN_VID_L0 |    |    |    |             |    |    |    |    |    |    |    | FRCP_IPV4_EN | FRCP_IPV6_EN |
| Type  | RW            |    | RW          |    |    |    |             |    |    |    |    |    |    |    | RW           | RW           |
| Reset | 0             | 0  | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1            | 0            |

| Bit(s) | Name          | Description                                   |
|--------|---------------|-----------------------------------------------|
| 31:26  | VLAN_VID_L2_L | VLAN VID of four forced port LRO rings        |
| 25:14  | VLAN_VID_L1   | To validate IPv4 flow of forced port LRO ring |
| 13:2   | VLAN_VID_L0   | To validate IPv4 flow of forced port LRO ring |
| 1      | FRCP_IPV4_EN  | To validate IPv4 flow of forced port LRO ring |
| 0      | FRCP_IPV6_EN  | To validate IPv6 flow of forced port LRO ring |

15106C78 LRO2\_RING1\_CTRL\_DW1 RX ring age time[9:0] FFC00000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21            | 20          | 19          | 18          | 17          | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|---------------|-------------|-------------|-------------|-------------|----|
| Name  | AGE_TIME_L  |    |    |    |    |    |    |    |    |    | VLAN_VLD_L3   | VLAN_VLD_L2 | VLAN_VLD_L1 | VLAN_VLD_L0 | VLAN_VID_L3 |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    | RW            | RW          | RW          | RW          | RW          |    |
| Reset | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0             | 0           | 0           | 0           | 0           | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5             | 4           | 3           | 2           | 1           | 0  |
| Name  | VLAN_VID_L3 |    |    |    |    |    |    |    |    |    | VLAN_VID_L2_H |             |             |             |             |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    | RW            |             |             |             |             |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0             | 0           | 0           | 0           | 0           | 0  |

| Bit(s) | Name          | Description                                         |
|--------|---------------|-----------------------------------------------------|
| 31:22  | AGE_TIME_L    | Age time to flush LRO ring                          |
| 21     | VLAN_VLD_L3   | Valid bit of VLAN VID for four forced port LRO ring |
| 20     | VLAN_VLD_L2   | Valid bit of VLAN VID for four forced port LRO ring |
| 19     | VLAN_VLD_L1   | Valid bit of VLAN VID for four forced port LRO ring |
| 18     | VLAN_VLD_L0   | Valid bit of VLAN VID for four forced port LRO ring |
| 17:6   | VLAN_VID_L3   | VLAN VID of four forced port LRO rings              |
| 5:0    | VLAN_VID_L2_H | VLAN VID of four forced port LRO rings              |

15106C7C LRO2\_RING1\_CTRL\_DW2 LRO2\_MAX\_AGGREGATED\_CNT\_L 03FFFCBF

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25           | 24  | 23      | 22         | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|--------------|-----|---------|------------|----|----|----|----|----|----|
| Name  | MAX_AGGREGATED_CNT_L |    |    |    |    |    | MAX_AGG_TIME |     |         |            |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    | RW           |     |         |            |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 1            | 1   | 1       | 1          | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9            | 8   | 7       | 6          | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_AGG_TIME         |    |    |    |    |    | MYIP_VLD     | VLD | OP_MODE | AGE_TIME_H |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    | RW           | RW  | RW      | RW         |    |    |    |    |    |    |
| Reset | 1                    | 1  | 1  | 1  | 1  | 1  | 0            | 0   | 1       | 0          | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name                 | Description                                             |
|--------|----------------------|---------------------------------------------------------|
| 31:26  | MAX_AGGREGATED_CNT_L | To limit max aggregated packets                         |
| 25:10  | MAX_AGG_TIME         | Maximum aggregation time to flush, = 0 to disable flush |
| 9      | MYIP_VLD             | To validate programmed DIP information                  |
| 8      | VLD                  | To validate programmed flow information                 |
| 7:6    | OP_MODE              | 00: Normal, 01: PSE, 10: forced_port, 11: auto_learn    |
| 5:0    | AGE_TIME_H           | Age time to flush LRO ring, = 0 to disable flush        |

15106C80 LRO2\_RING1\_CTRL\_DW3 Reserved 00000001

| Bit   | 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17                   | 16 |
|-------|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------------------|----|
| Name  | REV |    |    |    |    |    |    |    |    |    |    |    |    |    |                      |    |
| Type  | RO  |    |    |    |    |    |    |    |    |    |    |    |    |    |                      |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                    | 0  |
| Bit   | 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1                    | 0  |
| Name  | REV |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_AGGREGATED_CNT_H |    |
| Type  | RO  |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                   |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                    | 1  |

| Bit(s) | Name                 | Description                     |
|--------|----------------------|---------------------------------|
| 31:2   | REV                  | To limit max aggregated packets |
| 1:0    | MAX_AGGREGATED_CNT_H | To limit max aggregated packets |

15106C90      LRO2\_RING2\_STP\_DTP\_DW      Source TCP port number      00000000

| Bit   | 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | STP |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DTP |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                 |
|--------|------|-----------------------------|
| 31:16  | STP  | Source TCP port number      |
| 15:0   | DTP  | Destination TCP port number |

15106C94      LRO2\_RING2\_DIP\_DW0      Destination IP address[31:0]      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                  |
|--------|------|------------------------------|
| 31:0   | DATA | Destination IP address[31:0] |

15106C98      LRO2\_RING2\_DIP\_DW1      Destination IP address[63:32]      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                   |
|--------|------|-------------------------------|
| 31:0   | DATA | Destination IP address[63:32] |

15106C9C      LRO2\_RING2\_DIP\_DW2      Destination IP address[95:64]      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                   |
|--------|------|-------------------------------|
| 31:0   | DATA | Destination IP address[95:64] |

15106CA0      LRO2\_RING2\_DIP\_DW3      Destination IP address[127:96]      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                    |
|--------|------|--------------------------------|
| 31:0   | DATA | Destination IP address[127:96] |

15106CA4      LRO2\_RING2\_SIP\_DW0      Source IP address[31:0]      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description             |
|--------|------|-------------------------|
| 31:0   | DATA | Source IP address[31:0] |

**15106CA8**      **LRO2\_RING2\_SIP\_DW1**      **Source IP address[63:32]**      **00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description              |
|--------|------|--------------------------|
| 31:0   | DATA | Source IP address[63:32] |

**15106CAC**      **LRO2\_RING2\_SIP\_DW2**      **Source IP address[95:64]**      **00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description              |
|--------|------|--------------------------|
| 31:0   | DATA | Source IP address[95:64] |

**15106CB0**      **LRO2\_RING2\_SIP\_DW3**      **Source IP address[127:96]**      **00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description               |
|--------|------|---------------------------|
| 31:0   | DATA | Source IP address[127:96] |

15106CB4 LRO2\_RING2\_CTRL\_DW0 l2\_vlan\_vid\_l2\_l 00000002

| Bit   | 31            | 30 | 29          | 28 | 27 | 26 | 25          | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17           | 16           |
|-------|---------------|----|-------------|----|----|----|-------------|----|----|----|----|----|----|----|--------------|--------------|
| Name  | VLAN_VID_L2_L |    |             |    |    |    | VLAN_VID_L1 |    |    |    |    |    |    |    |              |              |
| Type  | RW            |    |             |    |    |    | RW          |    |    |    |    |    |    |    |              |              |
| Reset | 0             | 0  | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0            | 0            |
| Bit   | 15            | 14 | 13          | 12 | 11 | 10 | 9           | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1            | 0            |
| Name  | VLAN_VID_L1   |    | VLAN_VID_L0 |    |    |    |             |    |    |    |    |    |    |    | FRCP_IPV4_EN | FRCP_IPV6_EN |
| Type  | RW            |    | RW          |    |    |    |             |    |    |    |    |    |    |    | RW           | RW           |
| Reset | 0             | 0  | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1            | 0            |

| Bit(s) | Name          | Description                                   |
|--------|---------------|-----------------------------------------------|
| 31:26  | VLAN_VID_L2_L | VLAN VID of four forced port LRO rings        |
| 25:14  | VLAN_VID_L1   | To validate IPv4 flow of forced port LRO ring |
| 13:2   | VLAN_VID_L0   | To validate IPv4 flow of forced port LRO ring |
| 1      | FRCP_IPV4_EN  | To validate IPv4 flow of forced port LRO ring |
| 0      | FRCP_IPV6_EN  | To validate IPv6 flow of forced port LRO ring |

15106CB8 LRO2\_RING2\_CTRL\_DW1 RX ring age time[9:0] FFC00000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21            | 20          | 19          | 18          | 17          | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|---------------|-------------|-------------|-------------|-------------|----|
| Name  | AGE_TIME_L  |    |    |    |    |    |    |    |    |    | VLAN_VLD_L3   | VLAN_VLD_L2 | VLAN_VLD_L1 | VLAN_VLD_L0 | VLAN_VID_L3 |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    | RW            | RW          | RW          | RW          | RW          |    |
| Reset | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0             | 0           | 0           | 0           | 0           | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5             | 4           | 3           | 2           | 1           | 0  |
| Name  | VLAN_VID_L3 |    |    |    |    |    |    |    |    |    | VLAN_VID_L2_H |             |             |             |             |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    | RW            |             |             |             |             |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0             | 0           | 0           | 0           | 0           | 0  |

| Bit(s) | Name          | Description                                         |
|--------|---------------|-----------------------------------------------------|
| 31:22  | AGE_TIME_L    | Age time to flush LRO ring                          |
| 21     | VLAN_VLD_L3   | Valid bit of VLAN VID for four forced port LRO ring |
| 20     | VLAN_VLD_L2   | Valid bit of VLAN VID for four forced port LRO ring |
| 19     | VLAN_VLD_L1   | Valid bit of VLAN VID for four forced port LRO ring |
| 18     | VLAN_VLD_L0   | Valid bit of VLAN VID for four forced port LRO ring |
| 17:6   | VLAN_VID_L3   | VLAN VID of four forced port LRO rings              |
| 5:0    | VLAN_VID_L2_H | VLAN VID of four forced port LRO rings              |

15106CBC LRO2\_RING2\_CTRL\_DW2 LRO2\_MAX\_AGGREGATED\_CNT\_L 03FFFCBF

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25           | 24  | 23      | 22         | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|--------------|-----|---------|------------|----|----|----|----|----|----|
| Name  | MAX_AGGREGATED_CNT_L |    |    |    |    |    | MAX_AGG_TIME |     |         |            |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    | RW           |     |         |            |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 1            | 1   | 1       | 1          | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9            | 8   | 7       | 6          | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_AGG_TIME         |    |    |    |    |    | MYIP_VLD     | VLD | OP_MODE | AGE_TIME_H |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    | RW           | RW  | RW      | RW         |    |    |    |    |    |    |
| Reset | 1                    | 1  | 1  | 1  | 1  | 1  | 0            | 0   | 1       | 0          | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name                 | Description                                            |
|--------|----------------------|--------------------------------------------------------|
| 31:26  | MAX_AGGREGATED_CNT_L | To limit max aggregated packets                        |
| 25:10  | MAX_AGG_TIME         | Maximum aggregation time to flush, =0 to disable flush |
| 9      | MYIP_VLD             | To validate programmed DIP information                 |
| 8      | VLD                  | To validate programmed flow information                |
| 7:6    | OP_MODE              | 00: Normal, 01: PSE, 10: forced_port, 11: auto_learn   |
| 5:0    | AGE_TIME_H           | Age time to flush LRO ring, = 0 to disable flush       |

15106CC0 LRO2\_RING2\_CTRL\_DW3 Reserved 00000001

| Bit   | 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17                   | 16 |
|-------|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------------------|----|
| Name  | REV |    |    |    |    |    |    |    |    |    |    |    |    |    |                      |    |
| Type  | RO  |    |    |    |    |    |    |    |    |    |    |    |    |    |                      |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                    | 0  |
| Bit   | 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1                    | 0  |
| Name  | REV |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_AGGREGATED_CNT_H |    |
| Type  | RO  |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                   |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                    | 1  |

| Bit(s) | Name                 | Description                     |
|--------|----------------------|---------------------------------|
| 31:2   | REV                  | To limit max aggregated packets |
| 1:0    | MAX_AGGREGATED_CNT_H | To limit max aggregated packets |

15106CD0      LRO2 RING3 STP DTP DW      Source TCP port number      00000000

| Bit   | 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | STP |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DTP |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                 |
|--------|------|-----------------------------|
| 31:16  | STP  | Source TCP port number      |
| 15:0   | DTP  | Destination TCP port number |

15106CD4      LRO2 RING3 DIP DW0      Destination IP address[31:0]      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                  |
|--------|------|------------------------------|
| 31:0   | DATA | Destination IP address[31:0] |

15106CD8      LRO2 RING3 DIP DW1      Destination IP address[63:32]      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                   |
|--------|------|-------------------------------|
| 31:0   | DATA | Destination IP address[63:32] |



15106CDC      LRO2 RING3 DIP DW2      Destination IP address[95:64]      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                   |
|--------|------|-------------------------------|
| 31:0   | DATA | Destination IP address[95:64] |

15106CE0      LRO2 RING3 DIP DW3      Destination IP address[127:96]      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                    |
|--------|------|--------------------------------|
| 31:0   | DATA | Destination IP address[127:96] |

15106CE4      LRO2 RING3 SIP DW0      Source IP address[31:0]      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description             |
|--------|------|-------------------------|
| 31:0   | DATA | Source IP address[31:0] |

15106CE8      LRO2 RING3 SIP DW1      Source IP address[63:32]      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description              |
|--------|------|--------------------------|
| 31:0   | DATA | Source IP address[63:32] |

15106CEC      LRO2 RING3 SIP DW2      Source IP address[95:64]      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description              |
|--------|------|--------------------------|
| 31:0   | DATA | Source IP address[95:64] |

15106CF0      LRO2 RING3 SIP DW3      Source IP address[127:96]      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description               |
|--------|------|---------------------------|
| 31:0   | DATA | Source IP address[127:96] |

15106CF4 LRO2\_RING3\_CTRL\_DW0 l2\_vlan\_vid\_l2\_l 00000002

| Bit   | 31            | 30 | 29          | 28 | 27 | 26 | 25          | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17           | 16           |
|-------|---------------|----|-------------|----|----|----|-------------|----|----|----|----|----|----|----|--------------|--------------|
| Name  | VLAN_VID_L2_L |    |             |    |    |    | VLAN_VID_L1 |    |    |    |    |    |    |    |              |              |
| Type  | RW            |    |             |    |    |    | RW          |    |    |    |    |    |    |    |              |              |
| Reset | 0             | 0  | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0            | 0            |
| Bit   | 15            | 14 | 13          | 12 | 11 | 10 | 9           | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1            | 0            |
| Name  | VLAN_VID_L1   |    | VLAN_VID_L0 |    |    |    |             |    |    |    |    |    |    |    | FRCP_IPV4_EN | FRCP_IPV6_EN |
| Type  | RW            |    | RW          |    |    |    |             |    |    |    |    |    |    |    | RW           | RW           |
| Reset | 0             | 0  | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1            | 0            |

| Bit(s) | Name          | Description                                   |
|--------|---------------|-----------------------------------------------|
| 31:26  | VLAN_VID_L2_L | VLAN VID of four forced port LRO rings        |
| 25:14  | VLAN_VID_L1   | To validate IPv4 flow of forced port LRO ring |
| 13:2   | VLAN_VID_L0   | To validate IPv4 flow of forced port LRO ring |
| 1      | FRCP_IPV4_EN  | To validate IPv4 flow of forced port LRO ring |
| 0      | FRCP_IPV6_EN  | To validate IPv6 flow of forced port LRO ring |

15106CF8 LRO2\_RING3\_CTRL\_DW1 RX ring age time[9:0] FFC00000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21            | 20          | 19          | 18          | 17          | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|---------------|-------------|-------------|-------------|-------------|----|
| Name  | AGE_TIME_L  |    |    |    |    |    |    |    |    |    | VLAN_VLD_L3   | VLAN_VLD_L2 | VLAN_VLD_L1 | VLAN_VLD_L0 | VLAN_VID_L3 |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    | RW            | RW          | RW          | RW          | RW          |    |
| Reset | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0             | 0           | 0           | 0           | 0           | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5             | 4           | 3           | 2           | 1           | 0  |
| Name  | VLAN_VID_L3 |    |    |    |    |    |    |    |    |    | VLAN_VID_L2_H |             |             |             |             |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    | RW            |             |             |             |             |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0             | 0           | 0           | 0           | 0           | 0  |

| Bit(s) | Name          | Description                                         |
|--------|---------------|-----------------------------------------------------|
| 31:22  | AGE_TIME_L    | Age time to flush LRO ring                          |
| 21     | VLAN_VLD_L3   | Valid bit of VLAN VID for four forced port LRO ring |
| 20     | VLAN_VLD_L2   | Valid bit of VLAN VID for four forced port LRO ring |
| 19     | VLAN_VLD_L1   | Valid bit of VLAN VID for four forced port LRO ring |
| 18     | VLAN_VLD_L0   | Valid bit of VLAN VID for four forced port LRO ring |
| 17:6   | VLAN_VID_L3   | VLAN VID of four forced port LRO rings              |
| 5:0    | VLAN_VID_L2_H | VLAN VID of four forced port LRO rings              |

15106CFC LRO2\_RING3\_CTRL\_DW2 LRO2\_MAX\_AGGREGATED\_CNT\_L 03FFFCBF

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25           | 24  | 23      | 22         | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|--------------|-----|---------|------------|----|----|----|----|----|----|
| Name  | MAX_AGGREGATED_CNT_L |    |    |    |    |    | MAX_AGG_TIME |     |         |            |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    | RW           |     |         |            |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 1            | 1   | 1       | 1          | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9            | 8   | 7       | 6          | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_AGG_TIME         |    |    |    |    |    | MYIP_VLD     | VLD | OP_MODE | AGE_TIME_H |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    | RW           | RW  | RW      | RW         |    |    |    |    |    |    |
| Reset | 1                    | 1  | 1  | 1  | 1  | 1  | 0            | 0   | 1       | 0          | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name                 | Description                                             |
|--------|----------------------|---------------------------------------------------------|
| 31:26  | MAX_AGGREGATED_CNT_L | To limit max aggregated packets                         |
| 25:10  | MAX_AGG_TIME         | Maximum aggregation time to flush, = 0 to disable flush |
| 9      | MYIP_VLD             | To validate programmed DIP information                  |
| 8      | VLD                  | To validate programmed flow information                 |
| 7:6    | OP_MODE              | 00: Normal, 01: PSE, 10: forced_port, 11: auto_learn    |
| 5:0    | AGE_TIME_H           | Age time to flush LRO ring, = 0 to disable flush        |

15106D00 LRO2\_RING3\_CTRL\_DW3 Reserved 00000001

| Bit   | 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17                   | 16 |
|-------|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------------------|----|
| Name  | REV |    |    |    |    |    |    |    |    |    |    |    |    |    |                      |    |
| Type  | RO  |    |    |    |    |    |    |    |    |    |    |    |    |    |                      |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                    | 0  |
| Bit   | 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1                    | 0  |
| Name  | REV |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_AGGREGATED_CNT_H |    |
| Type  | RO  |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                   |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                    | 1  |

| Bit(s) | Name                 | Description                     |
|--------|----------------------|---------------------------------|
| 31:2   | REV                  | To limit max aggregated packets |
| 1:0    | MAX_AGGREGATED_CNT_H | To limit max aggregated packets |

**15106D10**      **LRO2\_RING4\_STP\_DTP\_DW**      **Source TCP port number**      **00000000**

| Bit   | 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | STP |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DTP |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                 |
|--------|------|-----------------------------|
| 31:16  | STP  | Source TCP port number      |
| 15:0   | DTP  | Destination TCP port number |

**15106D14**      **LRO2\_RING4\_DIP\_DW0**      **Destination IP address[31:0]**      **00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                  |
|--------|------|------------------------------|
| 31:0   | DATA | Destination IP address[31:0] |

**15106D18**      **LRO2\_RING4\_DIP\_DW1**      **Destination IP address[63:32]**      **00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                   |
|--------|------|-------------------------------|
| 31:0   | DATA | Destination IP address[63:32] |

**15106D1C      LRO2\_RING4\_DIP\_DW2      Destination IP address[95:64]      00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                   |
|--------|------|-------------------------------|
| 31:0   | DATA | Destination IP address[95:64] |

**15106D20      LRO2\_RING4\_DIP\_DW3      Destination IP address[127:96]      00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description                    |
|--------|------|--------------------------------|
| 31:0   | DATA | Destination IP address[127:96] |

**15106D24      LRO2\_RING4\_SIP\_DW0      Source IP address[31:0]      00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description             |
|--------|------|-------------------------|
| 31:0   | DATA | Source IP address[31:0] |

**15106D28**      **LRO2\_RING4\_SIP\_DW1**      **Source IP address[63:32]**      **00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description              |
|--------|------|--------------------------|
| 31:0   | DATA | Source IP address[63:32] |

**15106D2C**      **LRO2\_RING4\_SIP\_DW2**      **Source IP address[95:64]**      **00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description              |
|--------|------|--------------------------|
| 31:0   | DATA | Source IP address[95:64] |

**15106D30**      **LRO2\_RING4\_SIP\_DW3**      **Source IP address[127:96]**      **00000000**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description               |
|--------|------|---------------------------|
| 31:0   | DATA | Source IP address[127:96] |

15106D34 LRO2\_RING4\_CTRL\_DW0 l2\_vlan\_vid\_l2\_l 00000002

| Bit   | 31            | 30 | 29          | 28 | 27 | 26 | 25          | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17           | 16           |
|-------|---------------|----|-------------|----|----|----|-------------|----|----|----|----|----|----|----|--------------|--------------|
| Name  | VLAN_VID_L2_L |    |             |    |    |    | VLAN_VID_L1 |    |    |    |    |    |    |    |              |              |
| Type  | RW            |    |             |    |    |    | RW          |    |    |    |    |    |    |    |              |              |
| Reset | 0             | 0  | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0            | 0            |
| Bit   | 15            | 14 | 13          | 12 | 11 | 10 | 9           | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1            | 0            |
| Name  | VLAN_VID_L1   |    | VLAN_VID_L0 |    |    |    |             |    |    |    |    |    |    |    | FRCP_IPV4_EN | FRCP_IPV6_EN |
| Type  | RW            |    | RW          |    |    |    |             |    |    |    |    |    |    |    | RW           | RW           |
| Reset | 0             | 0  | 0           | 0  | 0  | 0  | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1            | 0            |

| Bit(s) | Name          | Description                                   |
|--------|---------------|-----------------------------------------------|
| 31:26  | VLAN_VID_L2_L | VLAN VID of four forced port LRO rings        |
| 25:14  | VLAN_VID_L1   | To validate IPv4 flow of forced port LRO ring |
| 13:2   | VLAN_VID_L0   | To validate IPv4 flow of forced port LRO ring |
| 1      | FRCP_IPV4_EN  | To validate IPv4 flow of forced port LRO ring |
| 0      | FRCP_IPV6_EN  | To validate IPv6 flow of forced port LRO ring |

15106D38 LRO2\_RING4\_CTRL\_DW1 RX ring age time[9:0] FFC00000

| Bit   | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21            | 20          | 19          | 18          | 17          | 16 |
|-------|-------------|----|----|----|----|----|----|----|----|----|---------------|-------------|-------------|-------------|-------------|----|
| Name  | AGE_TIME_L  |    |    |    |    |    |    |    |    |    | VLAN_VLD_L3   | VLAN_VLD_L2 | VLAN_VLD_L1 | VLAN_VLD_L0 | VLAN_VID_L3 |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    | RW            | RW          | RW          | RW          | RW          |    |
| Reset | 1           | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0             | 0           | 0           | 0           | 0           | 0  |
| Bit   | 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5             | 4           | 3           | 2           | 1           | 0  |
| Name  | VLAN_VID_L3 |    |    |    |    |    |    |    |    |    | VLAN_VID_L2_H |             |             |             |             |    |
| Type  | RW          |    |    |    |    |    |    |    |    |    | RW            |             |             |             |             |    |
| Reset | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0             | 0           | 0           | 0           | 0           | 0  |

| Bit(s) | Name          | Description                                         |
|--------|---------------|-----------------------------------------------------|
| 31:22  | AGE_TIME_L    | Age time to flush LRO ring                          |
| 21     | VLAN_VLD_L3   | Valid bit of VLAN VID for four forced port LRO ring |
| 20     | VLAN_VLD_L2   | Valid bit of VLAN VID for four forced port LRO ring |
| 19     | VLAN_VLD_L1   | Valid bit of VLAN VID for four forced port LRO ring |
| 18     | VLAN_VLD_L0   | Valid bit of VLAN VID for four forced port LRO ring |
| 17:6   | VLAN_VID_L3   | VLAN VID of four forced port LRO rings              |
| 5:0    | VLAN_VID_L2_H | VLAN VID of four forced port LRO rings              |



15106D3C      LRO2\_RING4\_CTRL\_DW2      LRO2\_MAX\_AGGREGATED\_CNT\_L      03FFFCBF

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25           | 24  | 23      | 22         | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|--------------|-----|---------|------------|----|----|----|----|----|----|
| Name  | MAX_AGGREGATED_CNT_L |    |    |    |    |    | MAX_AGG_TIME |     |         |            |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    | RW           |     |         |            |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 1            | 1   | 1       | 1          | 1  | 1  | 1  | 1  | 1  | 1  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9            | 8   | 7       | 6          | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | MAX_AGG_TIME         |    |    |    |    |    | MYIP_VLD     | VLD | OP_MODE | AGE_TIME_H |    |    |    |    |    |    |
| Type  | RW                   |    |    |    |    |    | RW           | RW  | RW      | RW         |    |    |    |    |    |    |
| Reset | 1                    | 1  | 1  | 1  | 1  | 1  | 0            | 0   | 1       | 0          | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit(s) | Name                 | Description                                             |
|--------|----------------------|---------------------------------------------------------|
| 31:26  | MAX_AGGREGATED_CNT_L | To limit max aggregated packets                         |
| 25:10  | MAX_AGG_TIME         | Maximum aggregation time to flush, = 0 to disable flush |
| 9      | MYIP_VLD             | To validate programmed DIP information                  |
| 8      | VLD                  | To validate programmed flow information                 |
| 7:6    | OP_MODE              | 00: Normal, 01: PSE, 10: forced_port, 11: auto_learn    |
| 5:0    | AGE_TIME_H           | Age time to flush LRO ring, = 0 to disable flush        |

15106D40      LRO2\_RING4\_CTRL\_DW3      Reserved      00000001

| Bit   | 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17                   | 16 |
|-------|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------------------|----|
| Name  | REV |    |    |    |    |    |    |    |    |    |    |    |    |    |                      |    |
| Type  | RO  |    |    |    |    |    |    |    |    |    |    |    |    |    |                      |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                    | 0  |
| Bit   | 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1                    | 0  |
| Name  | REV |    |    |    |    |    |    |    |    |    |    |    |    |    | MAX_AGGREGATED_CNT_H |    |
| Type  | RO  |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                   |    |
| Reset | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                    | 1  |

| Bit(s) | Name                 | Description                     |
|--------|----------------------|---------------------------------|
| 31:2   | REV                  | To limit max aggregated packets |
| 1:0    | MAX_AGGREGATED_CNT_H | To limit max aggregated packets |

## 4.7 RSS

### 4.7.1 Register Definition

Module name: RSS2 Base address: (+0x15107000)

| Address  | Name                       | Width | Register Function          |
|----------|----------------------------|-------|----------------------------|
| 15107000 | <u>RSS2_GLO_CFG</u>        | 32    | RSS global configuration   |
| 15107008 | <u>RSS2_GLO_CFG3</u>       | 32    | RSS global configuration 3 |
| 15107020 | <u>RSS2_HASH_KEY_DW0</u>   | 32    | RSS hash key DW0           |
| 15107024 | <u>RSS2_HASH_KEY_DW1</u>   | 32    | RSS hash key DW1           |
| 15107028 | <u>RSS2_HASH_KEY_DW2</u>   | 32    | RSS hash key DW2           |
| 1510702C | <u>RSS2_HASH_KEY_DW3</u>   | 32    | RSS hash key DW3           |
| 15107030 | <u>RSS2_HASH_KEY_DW4</u>   | 32    | RSS hash key DW4           |
| 15107034 | <u>RSS2_HASH_KEY_DW5</u>   | 32    | RSS hash key DW5           |
| 15107038 | <u>RSS2_HASH_KEY_DW6</u>   | 32    | RSS hash key DW6           |
| 1510703C | <u>RSS2_HASH_KEY_DW7</u>   | 32    | RSS hash key DW7           |
| 15107040 | <u>RSS2_HASH_KEY_DW8</u>   | 32    | RSS hash key DW8           |
| 15107044 | <u>RSS2_HASH_KEY_DW9</u>   | 32    | RSS hash key DW9           |
| 15107050 | <u>RSS2_INDR_TABLE_DW0</u> | 32    | RSS indirection table DW0  |
| 15107054 | <u>RSS2_INDR_TABLE_DW1</u> | 32    | RSS indirection table DW1  |
| 15107058 | <u>RSS2_INDR_TABLE_DW2</u> | 32    | RSS indirection table DW2  |
| 1510705C | <u>RSS2_INDR_TABLE_DW3</u> | 32    | RSS indirection table DW3  |
| 15107060 | <u>RSS2_INDR_TABLE_DW4</u> | 32    | RSS indirection table DW4  |
| 15107064 | <u>RSS2_INDR_TABLE_DW5</u> | 32    | RSS indirection table DW5  |
| 15107068 | <u>RSS2_INDR_TABLE_DW6</u> | 32    | RSS indirection table DW6  |
| 1510706C | <u>RSS2_INDR_TABLE_DW7</u> | 32    | RSS indirection table DW7  |

**15107000 RSS2\_GLO\_CFG RSS global configuration 1F1F3370**

| Bit   | 31 | 30        | 29 | 28            | 27 | 26        | 25 | 24 | 23 | 22            | 21 | 20            | 19          | 18          | 17       | 16         |
|-------|----|-----------|----|---------------|----|-----------|----|----|----|---------------|----|---------------|-------------|-------------|----------|------------|
| Name  |    |           |    | IPV4_TUPLE_EN |    |           |    |    |    |               |    | IPV6_TUPLE_EN |             |             |          |            |
| Type  |    |           |    | RW            |    |           |    |    |    |               |    | RW            |             |             |          |            |
| Reset |    |           |    | 1             | 1  | 1         | 1  | 1  |    |               |    | 1             | 1           | 1           | 1        | 1          |
| Bit   | 15 | 14        | 13 | 12            | 11 | 10        | 9  | 8  | 7  | 6             | 5  | 4             | 3           | 2           | 1        | 0          |
| Name  |    | IPV4_TYPE |    |               |    | IPV6_TYPE |    |    |    | INDR_TBL_SIZE |    |               | RSS_CFG_RDY | RSS_CFG_REQ | RSS_BUSY | RSS_ENABLE |
| Type  |    | RW        |    |               |    | RW        |    |    |    | RW            |    |               | RO          | RW          | RO       | RW         |
| Reset |    | 0         | 1  | 1             |    | 0         | 1  | 1  |    | 1             | 1  | 1             | 0           | 0           | 0        | 0          |

| Bit(s) | Name          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 28:24  | IPV4_TUPLE_EN | <p><b>IPv4 Hash Tuple Global Enable</b></p> <p>This field controls which hash tuple is valid for IPv4 hash calculation. The invalid(disabled) tuple can be seem as 0x0 when calculating HASH.</p> <p>For example, when SIP is disabled, 2-tuple and 4-tuple hash will not consider SIP. Another example, when DPORT is disabled, 4-tuple hash will not consider DPORT.</p> <p>Bit Maps: {DPROT,SPORT,DIP,SIP,Reserved}</p> <p>Set the bits to 1 to enable corresponding hash tuple for hash calculation.</p> <p>Set the bits to 0 to disable corresponding hash tuple for hash calculation.</p> <p>5'b00000: Disable All</p> <p>5'b00010: Enable SIP for HASH</p> <p>5'b00100: Enable DIP for HASH</p> <p>5'b01000: Enable SPORT for HASH</p> <p>5'b10000: Enable DPORT for HASH</p> <p>5'b11111: Enable DPORT, SPORT, DIP, SIP for HASH</p> <p>Others: Combinations of the above hash tuple</p> |
| 20:16  | IPV6_TUPLE_EN | <p><b>IPv6 Hash Tuple Global Enable</b></p> <p>This field controls which hash tuple is valid for IPv6 hash calculation.</p> <p>See description of IPV4_TUPLE_EN for more detail.</p> <p>Bit Maps: {DPROT,SPORT,DIP,SIP,Reserved}</p> <p>Set the bits to 1 to enable corresponding hash tuple for hash calculation.</p> <p>Set the bits to 0 to disable corresponding hash tuple for hash calculation.</p> <p>5'b00000: Disable All</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

| Bit(s) | Name      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|--------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |           | 5'b00010: Enable SIP for HASH                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|        |           | 5'b00100: Enable DIP for HASH                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|        |           | 5'b01000: Enable SPORT for HASH                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|        |           | 5'b10000: Enable DPORT for HASH                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|        |           | 5'b11111: Enable DPORT, SPORT, DIP, SIP for HASH                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|        |           | Others: Combinations of the above hash tuple                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 14:12  | IPV4_TYPE | <p><b>IPv4 Hash Type Selection Flag</b></p> <p>This field controls the selection of hash 2-tuple and 4-tuple for different kinds of IPv4 packet.</p> <p>Bit Maps: {UDP 4-tuple,TCP4-tuple,IP 2-tuple}</p> <p>RSS performs the hash calculations as specified for the enabled case.</p> <p>For example, IPV4_TYPE=3'b011, RSS will use 4-tuple hash for IPv4 TCP packets and 2-tuple hash for IPv4 non-TCP packets (such as IPv4 fragment packet).</p> <p>3'b000: Disable IPv4 packets for RSS. RSS does not accept IPv4 packets</p> <p>3'b001: Enable IPv4 2-tuple hash</p> <p>3'b010: Enable TCP 4-tuple hash</p> <p>3'b100: Enable UDP 4-tuple hash</p> <p>3'b011: Enable IPv4 2-tuple hash + TCP 4-tuple hash</p> <p>3'b101: Enable IPv4 2-tuple hash + UDP 4-tuple hash</p> <p>3'b110: TCP 4-tuple hash + UDP 4-tuple hash</p> <p>3'b111: IPv4 2-tuple hash + TCP 4-tuple hash + UDP 4-tuple hash</p> |
| 10:8   | IPV6_TYPE | <p><b>IPv6 Hash Type Selection Flag</b></p> <p>This field controls the selection of hash 2-tuple and 4-tuple for different kinds of IPv6 packet.</p> <p>Bit Maps: {UDP 4-tuple,TCP4-tuple,IP 2-tuple}</p> <p>See description of IPV4_TYPE for more detail.</p> <p>3'b000: Disable IPv6 packets for RSS. RSS does not accept IPv4 packets</p> <p>3'b001: Enable IPv6 2-tuple hash</p> <p>3'b010: Enable TCP 4-tuple hash</p> <p>3'b100: Enable UDP 4-tuple hash</p> <p>3'b011: Enable IPv6 2-tuple hash + TCP 4-tuple hash</p> <p>3'b101: Enable IPv6 2-tuple hash + UDP 4-tuple hash</p>                                                                                                                                                                                                                                                                                                                  |

| Bit(s) | Name          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|--------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |               | 3'b110: TCP 4-tuple hash + UDP 4-tuple hash                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|        |               | 3'b111: IPv6 2-tuple hash + TCP 4-tuple hash + UDP 4-tuple hash                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 6:4    | INDR_TBL_SIZE | <p><b>Change the size of indirection table.</b></p> <p>This register field affects how many bits of hash result will be used as the entry of indirection table.</p> <p>For example, INDR_TBL_SIZE=6 means RSS use only 6 bits of hash result as indirection table entry, which also means that indirection table has <math>2^6=64</math> entries.</p> <p>3'd1: Indirection table size = 2 entries</p> <p>3'd2: Indirection table size = 4 entries</p> <p>3'd3: Indirection table size = 8 entries</p> <p>3'd4: Indirection table size = 16 entries</p> <p>3'd5: Indirection table size = 32 entries</p> <p>3'd6: Indirection table size = 64 entries</p> <p>3'd7: Indirection table size = 128 entries</p> <p>Other: Invalid value</p> |
| 3      | RSS_CFG_RDY   | <p><b>RSS is ready to accept new register configuration.</b></p> <p>This register will be asserted after RSS accepts the request from RSS_CFG_REQ. See description of RSS_CFG_REQ for more details.</p> <p>0: Not Ready</p> <p>1: Ready</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 2      | RSS_CFG_REQ   | <p><b>Request to change RSS register configuration.</b></p> <p>When request is asserted, RSS will be paused after the process of current packet has finished. Note that assert RSS_CFG_REQ is required before enabling RSS or changing other register setting (such as indirection table). Must wait until RSS_CFG_RDY=1 before changing RSS register value (including RSS_ENABLE).</p> <p>0: Request deassert</p> <p>1: Request assert</p>                                                                                                                                                                                                                                                                                            |
| 1      | RSS_BUSY      | <p><b>RSS is working or not</b></p> <p>0: RSS IDLE</p> <p>1: RSS BUSY</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 0      | RSS_ENABLE    | <p><b>Enables or disables RSS</b></p> <p>0: Disable RSS</p> <p>1: Enable RSS</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

| Bit(s) | Name | Description |
|--------|------|-------------|
|--------|------|-------------|

**15107008**      **RSS2\_GLO\_CFG3**      **RSS global configuration 3**      **00008100**

| Bit   | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
|-------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|
| Name  | REV      |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SPC_TAG_EN |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW         |
| Reset | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          |
| Bit   | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| Name  | EXT_TPID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |
| Type  | RW       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |
| Reset | 1        | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          |

| Bit(s) | Name       | Description        |
|--------|------------|--------------------|
| 31:17  | REV        | Reserved           |
| 16     | SPC_TAG_EN | Special tag enable |
| 15:0   | EXT_TPID   | User extended TPID |

**15107020**      **RSS2\_HASH\_KEY\_DW0**      **RSS hash key DW0**      **BEAC01FA**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 0  |

| Bit(s) | Name | Description        |
|--------|------|--------------------|
| 31:0   | DATA | Hash key bits 31~0 |

**15107024**      **RSS2 HASH KEY DW1**      **RSS hash key DW1**      **6A42B73B**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 0  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 0  | 1  | 1  | 1  | 0  | 1  | 1  |

| Bit(s) | Name | Description         |
|--------|------|---------------------|
| 31:0   | DATA | Hash key bits 63~32 |

**15107028**      **RSS2 HASH KEY DW2**      **RSS hash key DW2**      **8030F20C**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 1  | 1  | 1  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  |

| Bit(s) | Name | Description         |
|--------|------|---------------------|
| 31:0   | DATA | Hash key bits 95~64 |

**1510702C**      **RSS2 HASH KEY DW3**      **RSS hash key DW3**      **77CB2DA3**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 0  | 1  | 0  | 1  | 1  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 1  | 0  | 1  | 0  | 0  | 0  | 1  | 1  |

| Bit(s) | Name | Description          |
|--------|------|----------------------|
| 31:0   | DATA | Hash key bits 127~96 |

**15107030**      **RSS2 HASH KEY DW4**      **RSS hash key DW4**      **AE7B30B4**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 0  | 1  | 0  | 1  | 1  | 1  | 0  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 1  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 0  | 0  |

| Bit(s) | Name | Description           |
|--------|------|-----------------------|
| 31:0   | DATA | Hash key bits 159~128 |

**15107034**      **RSS2 HASH KEY DW5**      **RSS hash key DW5**      **D0CA2BCB**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 0  | 1  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 0  | 1  | 0  | 1  | 1  |

| Bit(s) | Name | Description           |
|--------|------|-----------------------|
| 31:0   | DATA | Hash key bits 191~160 |

**15107038**      **RSS2 HASH KEY DW6**      **RSS hash key DW6**      **43A38FB0**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 1  | 0  | 0  | 0  | 1  | 1  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 0  | 0  | 0  | 0  |

| Bit(s) | Name | Description           |
|--------|------|-----------------------|
| 31:0   | DATA | Hash key bits 223~192 |



**1510703C**      **RSS2 HASH KEY DW7**      **RSS hash key DW7**      **4167253D**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 0  | 1  | 1  | 1  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 1  | 1  | 1  | 0  | 1  |

| Bit(s) | Name | Description           |
|--------|------|-----------------------|
| 31:0   | DATA | Hash key bits 255~224 |

**15107040**      **RSS2 HASH KEY DW8**      **RSS hash key DW8**      **255B0EC2**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 1  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 1  | 0  |

| Bit(s) | Name | Description           |
|--------|------|-----------------------|
| 31:0   | DATA | Hash key bits 287~256 |

**15107044**      **RSS2 HASH KEY DW9**      **RSS hash key DW9**      **6D5A56DA**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 1  | 1  | 0  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0    | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 1  | 0  | 1  | 1  | 0  | 1  | 0  |

| Bit(s) | Name | Description           |
|--------|------|-----------------------|
| 31:0   | DATA | Hash key bits 319~288 |

**15107050**      **RSS2\_INDR\_TABLE\_DW0**      **RSS indirection table DW0**      **DEADBEEF**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name | Description                                             |
|--------|------|---------------------------------------------------------|
| 31:0   | DATA | Indirection table entries 15~0<br>Each entry has 2 bits |

**15107054**      **RSS2\_INDR\_TABLE\_DW1**      **RSS indirection table DW1**      **DEADBEEF**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name | Description                                              |
|--------|------|----------------------------------------------------------|
| 31:0   | DATA | Indirection table entries 31~16<br>Each entry has 2 bits |

**15107058**      **RSS2\_INDR\_TABLE\_DW2**      **RSS indirection table DW2**      **DEADBEEF**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name | Description                                              |
|--------|------|----------------------------------------------------------|
| 31:0   | DATA | Indirection table entries 47~32<br>Each entry has 2 bits |

**1510705C**      **RSS2\_INDR\_TABLE\_DW3**      **RSS indirection table DW3**      **DEADBEEF**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name | Description                                              |
|--------|------|----------------------------------------------------------|
| 31:0   | DATA | Indirection table entries 63~48<br>Each entry has 2 bits |

**15107060**      **RSS2\_INDR\_TABLE\_DW4**      **RSS indirection table DW4**      **DEADBEEF**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name | Description                                              |
|--------|------|----------------------------------------------------------|
| 31:0   | DATA | Indirection table entries 79~64<br>Each entry has 2 bits |

**15107064**      **RSS2\_INDR\_TABLE\_DW5**      **RSS indirection table DW5**      **DEADBEEF**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name | Description                                              |
|--------|------|----------------------------------------------------------|
| 31:0   | DATA | Indirection table entries 95~80<br>Each entry has 2 bits |

**15107068**      **RSS2\_INDR\_TABLE\_DW6**      **RSS indirection table DW6**      **DEADBEEF**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name | Description                                               |
|--------|------|-----------------------------------------------------------|
| 31:0   | DATA | Indirection table entries 111~96<br>Each entry has 2 bits |

**1510706C**      **RSS2\_INDR\_TABLE\_DW7**      **RSS indirection table DW7**      **DEADBEEF**

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | DATA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 1    | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

| Bit(s) | Name | Description                                                |
|--------|------|------------------------------------------------------------|
| 31:0   | DATA | Indirection table entries 127~112<br>Each entry has 2 bits |

## 4.8 GMAC

### 4.8.1 Register Definition

Module name: GMAC Base address: (+0x15110000)

| Address  | Name                             | Width | Register Function                                 |
|----------|----------------------------------|-------|---------------------------------------------------|
| 15110000 | <u>MAC_PPSC</u>                  | 32    | PHY polling and SMI master control                |
| 15110004 | <u>MAC_PIAC</u>                  | 32    | PHY indirect access control                       |
| 15110008 | <u>MAC_GPC</u>                   | 32    | GIGA MAC port control                             |
| 1511000C | <u>XGMAC_STS</u>                 | 32    | XGMAC status register                             |
| 15110010 | <u>MAC_MISC</u>                  | 32    | MAC MISC register                                 |
| 15110018 | <u>MAC_GPC1</u>                  | 32    | GIGA MAC port control - P3                        |
| 1511001C | <u>XGMAC_STS1</u>                | 32    | XGMAC status register - P3                        |
| 15110080 | <u>GSW_CFG</u>                   | 32    | GSW bridge registers                              |
| 15110088 | <u>GSW_STS</u>                   | 32    | GSW bridge status                                 |
| 15110100 | <u>MAC_P1_MCR</u>                | 32    | Port 1 MAC control                                |
| 15110104 | <u>MAC_P1_EEE</u>                | 32    | Port 1 EEE control                                |
| 15110108 | <u>MAC_P1_SR</u>                 | 32    | Port 1 MAC status                                 |
| 15110110 | <u>MAC_P1_WOL</u>                | 32    | Port 1 WOL                                        |
| 15110114 | <u>MAC_P1_SGMII</u>              | 32    | Port 1 SGMII                                      |
| 15110118 | <u>MAC_P1_PFC_CTRL</u>           | 32    | Port 1 PFC control                                |
| 1511011C | <u>MAC_P1_PFC_STS</u>            | 32    | Port 1 PFC status                                 |
| 15110120 | <u>MAC_P1_PFC_RX_PSON_CNT_L</u>  | 32    | Port 1 RX PFC pause on counter for low priority   |
| 15110124 | <u>MAC_P1_PFC_RX_PSON_CNT_H</u>  | 32    | Port 1 RX PFC pause on counter for high priority  |
| 15110128 | <u>MAC_P1_PFC_RX_PSOFF_CNT_L</u> | 32    | Port 1 RX PFC pause off counter for low priority  |
| 1511012C | <u>MAC_P1_PFC_RX_PSOFF_CNT_H</u> | 32    | Port 1 RX PFC pause off counter for high priority |
| 15110130 | <u>MAC_P1_PFC_TX_PSON_CNT_L</u>  | 32    | Port 1 TX PFC pause on counter for low priority   |
| 15110134 | <u>MAC_P1_PFC_TX_PSON_CNT_H</u>  | 32    | Port 1 TX PFC pause on counter for high priority  |
| 15110138 | <u>MAC_P1_PFC_TX_PSOFF_CNT_L</u> | 32    | Port 1 TX PFC pause off counter for low priority  |
| 1511013C | <u>MAC_P1_PFC_TX_PSOFF_CNT_H</u> | 32    | Port 1 TX PFC pause off counter for high priority |
| 15110200 | <u>MAC_P2_MCR</u>                | 32    | Port 2 MAC control                                |
| 15110204 | <u>MAC_P2_EEE</u>                | 32    | Port 2 EEE control                                |
| 15110208 | <u>MAC_P2_SR</u>                 | 32    | Port 2 MAC status                                 |
| 15110210 | <u>MAC_P2_WOL</u>                | 32    | Port 2 WOL                                        |
| 15110214 | <u>MAC_P2_SGMII</u>              | 32    | Port 2 SGMII                                      |
| 15110218 | <u>MAC_P2_PFC_CTRL</u>           | 32    | Port 2 PFC control                                |
| 1511021C | <u>MAC_P2_PFC_STS</u>            | 32    | Port 2 PFC status                                 |
| 15110220 | <u>MAC_P2_PFC_RX_PSON_CNT_L</u>  | 32    | Port 2 RX PFC pause on counter for low priority   |
| 15110224 | <u>MAC_P2_PFC_RX_PSON_CNT_H</u>  | 32    | Port 2 RX PFC pause on counter for high priority  |
| 15110228 | <u>MAC_P2_PFC_RX_PSOFF_CNT_L</u> | 32    | Port 2 RX PFC pause off counter for low priority  |

| Address  | Name                                       | Width | Register Function                                 |
|----------|--------------------------------------------|-------|---------------------------------------------------|
| 1511022C | <u>MAC P2 PFC RX PSOFF CNT</u><br><u>H</u> | 32    | Port 2 RX PFC pause off counter for high priority |
| 15110230 | <u>MAC P2 PFC TX PSON CNT</u><br><u>L</u>  | 32    | Port 2 TX PFC pause on counter for low priority   |
| 15110234 | <u>MAC P2 PFC TX PSON CNT</u><br><u>H</u>  | 32    | Port 2 TX PFC pause on counter for high priority  |
| 15110238 | <u>MAC P2 PFC TX PSOFF CNT</u><br><u>L</u> | 32    | Port 2 TX PFC pause off counter for low priority  |
| 1511023C | <u>MAC P2 PFC TX PSOFF CNT</u><br><u>H</u> | 32    | Port 2 TX PFC pause off counter for high priority |
| 15110300 | <u>MAC P3 MCR</u>                          | 32    | Port 3 MAC control                                |
| 15110304 | <u>MAC P3 EEE</u>                          | 32    | Port 3 EEE control                                |
| 15110308 | <u>MAC P3 SR</u>                           | 32    | Port 3 MAC status                                 |
| 15110310 | <u>MAC P3 WOL</u>                          | 32    | Port 3 WOL                                        |
| 15110314 | <u>MAC P3 SGMII</u>                        | 32    | Port 3 SGMII                                      |
| 15110318 | <u>MAC P3 PFC CTRL</u>                     | 32    | Port 3 PFC control                                |
| 1511031C | <u>MAC P3 PFC STS</u>                      | 32    | Port 3 PFC status                                 |
| 15110320 | <u>MAC P3 PFC RX PSON CNT</u><br><u>L</u>  | 32    | Port 3 RX PFC pause on counter for low priority   |
| 15110324 | <u>MAC P3 PFC RX PSON CNT</u><br><u>H</u>  | 32    | Port 3 RX PFC pause on counter for high priority  |
| 15110328 | <u>MAC P3 PFC RX PSOFF CNT</u><br><u>L</u> | 32    | Port 3 RX PFC pause off counter for low priority  |
| 1511032C | <u>MAC P3 PFC RX PSOFF CNT</u><br><u>H</u> | 32    | Port 3 RX PFC pause off counter for high priority |
| 15110330 | <u>MAC P3 PFC TX PSON CNT</u><br><u>L</u>  | 32    | Port 3 TX PFC pause on counter for low priority   |
| 15110334 | <u>MAC P3 PFC TX PSON CNT</u><br><u>H</u>  | 32    | Port 3 TX PFC pause on counter for high priority  |
| 15110338 | <u>MAC P3 PFC TX PSOFF CNT</u><br><u>L</u> | 32    | Port 3 TX PFC pause off counter for low priority  |
| 1511033C | <u>MAC P3 PFC TX PSOFF CNT</u><br><u>H</u> | 32    | Port 3 TX PFC pause off counter for high priority |
| 15110400 | <u>GMAC P1 RX UCST PKTCNTL</u>             | 32    | Port 1 RX unicast packet count low word           |
| 15110404 | <u>GMAC P1 RX UCST PKTCNT</u><br><u>H</u>  | 32    | Port 1 RX unicast packet count high word          |
| 15110408 | <u>GMAC P1 RX UCST BYTECN</u><br><u>TL</u> | 32    | Port 1 RX unicast byte count low word             |
| 1511040C | <u>GMAC P1 RX UCST BYTECN</u><br><u>TH</u> | 32    | Port 1 RX unicast byte count high word            |
| 15110410 | <u>GMAC P1 RX MCST PKTCNT</u><br><u>L</u>  | 32    | Port 1 RX multicast packet count low word         |
| 15110414 | <u>GMAC P1 RX MCST PKTCNT</u><br><u>H</u>  | 32    | Port 1 RX multicast packet count high word        |
| 15110418 | <u>GMAC P1 RX MCST BYTECN</u><br><u>TL</u> | 32    | Port 1 RX multicast byte count low word           |
| 1511041C | <u>GMAC P1 RX MCST BYTECN</u><br><u>TH</u> | 32    | Port 1 RX multicast byte count high word          |
| 15110420 | <u>GMAC P1 RX BCST PKTCNTL</u>             | 32    | Port 1 RX broadcast packet count low word         |
| 15110424 | <u>GMAC P1 RX BCST PKTCNT</u><br><u>H</u>  | 32    | Port 1 RX broadcast packet count high word        |
| 15110428 | <u>GMAC P1 RX BCST BYTECNT</u><br><u>L</u> | 32    | Port 1 RX broadcast byte count low word           |

| Address  | Name                                       | Width | Register Function                          |
|----------|--------------------------------------------|-------|--------------------------------------------|
| 1511042C | <u>GMAC P1 RX BCST BYTECNT</u><br><u>H</u> | 32    | Port 1 RX broadcast byte count high word   |
| 15110430 | <u>GMAC P1 TX UCST PKTCNTL</u>             | 32    | Port 1 TX unicast packet count low word    |
| 15110434 | <u>GMAC P1 TX UCST PKTCNT</u><br><u>H</u>  | 32    | Port 1 TX unicast packet count high word   |
| 15110438 | <u>GMAC P1 TX UCST BYTECNT</u><br><u>L</u> | 32    | Port 1 TX unicast byte count low word      |
| 1511043C | <u>GMAC P1 TX UCST BYTECNT</u><br><u>H</u> | 32    | Port 1 TX unicast byte count high word     |
| 15110440 | <u>GMAC P1 TX MCST PKTCNT</u><br><u>L</u>  | 32    | Port 1 TX multicast packet count low word  |
| 15110444 | <u>GMAC P1 TX MCST PKTCNT</u><br><u>H</u>  | 32    | Port 1 TX multicast packet count high word |
| 15110448 | <u>GMAC P1 TX MCST BYTECN</u><br><u>TL</u> | 32    | Port 1 TX multicast byte count low word    |
| 1511044C | <u>GMAC P1 TX MCST BYTECN</u><br><u>TH</u> | 32    | Port 1 TX multicast byte count high word   |
| 15110450 | <u>GMAC P1 TX BCST PKTCNTL</u>             | 32    | Port 1 TX broadcast packet count low word  |
| 15110454 | <u>GMAC P1 TX BCST PKTCNT</u><br><u>H</u>  | 32    | Port 1 TX broadcast packet count high word |
| 15110458 | <u>GMAC P1 TX BCST BYTECNT</u><br><u>L</u> | 32    | Port 1 TX broadcast byte count low word    |
| 1511045C | <u>GMAC P1 TX BCST BYTECNT</u><br><u>H</u> | 32    | Port 1 TX broadcast byte count high word   |
| 15110460 | <u>GMAC P2 RX UCST PKTCNTL</u>             | 32    | Port 2 RX unicast packet count low word    |
| 15110464 | <u>GMAC P2 RX UCST PKTCNT</u><br><u>H</u>  | 32    | Port 2 RX unicast packet count high word   |
| 15110468 | <u>GMAC P2 RX UCST BYTECN</u><br><u>TL</u> | 32    | Port 2 RX unicast byte count low word      |
| 1511046C | <u>GMAC P2 RX UCST BYTECN</u><br><u>TH</u> | 32    | Port 2 RX unicast byte count high word     |
| 15110470 | <u>GMAC P2 RX MCST PKTCNT</u><br><u>L</u>  | 32    | Port 2 RX multicast packet count low word  |
| 15110474 | <u>GMAC P2 RX MCST PKTCNT</u><br><u>H</u>  | 32    | Port 2 RX multicast packet count high word |
| 15110478 | <u>GMAC P2 RX MCST BYTECN</u><br><u>TL</u> | 32    | Port 2 RX multicast byte count low word    |
| 1511047C | <u>GMAC P2 RX MCST BYTECN</u><br><u>TH</u> | 32    | Port 2 RX multicast byte count high word   |
| 15110480 | <u>GMAC P2 RX BCST PKTCNTL</u>             | 32    | Port 2 RX broadcast packet count low word  |
| 15110484 | <u>GMAC P2 RX BCST PKTCNT</u><br><u>H</u>  | 32    | Port 2 RX broadcast packet count high word |
| 15110488 | <u>GMAC P2 RX BCST BYTECNT</u><br><u>L</u> | 32    | Port 2 RX broadcast byte count low word    |
| 1511048C | <u>GMAC P2 RX BCST BYTECNT</u><br><u>H</u> | 32    | Port 2 RX broadcast byte count high word   |
| 15110490 | <u>GMAC P2 TX UCST PKTCNTL</u>             | 32    | Port 2 TX unicast packet count low word    |
| 15110494 | <u>GMAC P2 TX UCST PKTCNT</u><br><u>H</u>  | 32    | Port 2 TX unicast packet count high word   |
| 15110498 | <u>GMAC P2 TX UCST BYTECNT</u><br><u>L</u> | 32    | Port 2 TX unicast byte count low word      |
| 1511049C | <u>GMAC P2 TX UCST BYTECNT</u><br><u>H</u> | 32    | Port 2 TX unicast byte count high word     |



| Address  | Name                                       | Width | Register Function                          |
|----------|--------------------------------------------|-------|--------------------------------------------|
| 151104A0 | <u>GMAC P2 TX MCST PKTCNT</u><br><u>L</u>  | 32    | Port 2 TX multicast packet count low word  |
| 151104A4 | <u>GMAC P2 TX MCST PKTCNT</u><br><u>H</u>  | 32    | Port 2 TX multicast packet count high word |
| 151104A8 | <u>GMAC P2 TX MCST BYTECN</u><br><u>TL</u> | 32    | Port 2 TX multicast byte count low word    |
| 151104AC | <u>GMAC P2 TX MCST BYTECN</u><br><u>TH</u> | 32    | Port 2 TX multicast byte count high word   |
| 151104B0 | <u>GMAC P2 TX BCST PKTCNT</u><br><u>L</u>  | 32    | Port 2 TX broadcast packet count low word  |
| 151104B4 | <u>GMAC P2 TX BCST PKTCNT</u><br><u>H</u>  | 32    | Port 2 TX broadcast packet count high word |
| 151104B8 | <u>GMAC P2 TX BCST BYTECN</u><br><u>L</u>  | 32    | Port 2 TX broadcast byte count low word    |
| 151104BC | <u>GMAC P2 TX BCST BYTECN</u><br><u>H</u>  | 32    | Port 2 TX broadcast byte count high word   |

**15110000      MAC\_PPSC      PHY polling and SMI master control      45000504**

| Bit   | 31        | 30         | 29          | 28          | 27 | 26 | 25 | 24 | 23    | 22        | 21            | 20          | 19    | 18        | 17            | 16 |
|-------|-----------|------------|-------------|-------------|----|----|----|----|-------|-----------|---------------|-------------|-------|-----------|---------------|----|
| Name  | PHY_AP_EN | PHY_PRE_EN | PHY_MDC_CFG |             |    |    |    |    | RESV0 | P2_EEE_AN | P2_PHY_AN_CFG |             | RESV1 | P1_EEE_AN | P1_PHY_AN_CFG |    |
| Type  | RW        | RW         | RW          |             |    |    |    |    | RW    | RW        | RW            |             | RW    | RW        | RW            |    |
| Reset | 0         | 1          | 0           | 0           | 0  | 1  | 0  | 1  | 0     | 0         | 0             | 0           | 0     | 0         | 0             | 0  |
| Bit   | 15        | 14         | 13          | 12          | 11 | 10 | 9  | 8  | 7     | 6         | 5             | 4           | 3     | 2         | 1             | 0  |
| Name  | RESV2     |            |             | P2_PHY_ADDR |    |    |    |    | RESV3 |           |               | P1_PHY_ADDR |       |           |               |    |
| Type  | RW        |            |             | RW          |    |    |    |    | RW    |           |               | RW          |       |           |               |    |
| Reset | 0         | 0          | 0           | 0           | 0  | 1  | 0  | 1  | 0     | 0         | 0             | 0           | 0     | 1         | 0             | 0  |

| Bit(s) | Name          | Description                                                                                                                                                                                                                                    |
|--------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | PHY_AP_EN     | <b>PHY auto polling enable</b><br><br>Indicates all PHY's status will be updated to PHY's status registers by PHY polling process.                                                                                                             |
| 30     | PHY_PRE_EN    | <b>PHY preamble enable</b><br><br>Indicates SMI master will send preamble bits (32 bits) at each MDIO read/write transaction.<br><br>[note] This bit will affect both PHY polling mode and PHY indirect access mode.                           |
| 29:24  | PHY_MDC_CFG   | <b>PHY MDC clock configuration</b><br><br>Used to configure the divider N for MDC clock frequency. MDC clock is sourced from 12.5MHz system clock and divided by N.<br><br>[note] MDC clock is gated or disabled when PHY_MDC_CFG is set to 0. |
| 23     | RESV0         | <b>Reserved</b>                                                                                                                                                                                                                                |
| 22     | P2_EEE_AN     | <b>Port 2 PHY EEE auto-polling enable</b><br><br>1'b0: EEE Polling Disable<br><br>1'b1: EEE Polling Enable                                                                                                                                     |
| 21:20  | P2_PHY_AN_CFG | <b>Port 2 PHY polling configuration</b><br><br>2'b00: CL22 Giga ETH PHY<br><br>2'b01: CL22 Fast ETH PHY<br><br>2'b10: CL45 10G ETH PHY (Link Resolution Only)<br><br>2'b11: Auto-Polling Disable                                               |
| 19     | RESV1         | <b>Reserved</b>                                                                                                                                                                                                                                |
| 18     | P1_EEE_AN     | <b>Port 1 PHY EEE auto-polling enable</b><br><br>1'b0: EEE Polling Disable<br><br>1'b1: EEE Polling Enable                                                                                                                                     |
| 17:16  | P1_PHY_AN_CFG | <b>Port 1 PHY polling configuration</b><br><br>2'b00: CL22 Giga ETH PHY                                                                                                                                                                        |

| Bit(s) | Name        | Description                                                                                                |
|--------|-------------|------------------------------------------------------------------------------------------------------------|
|        |             | 2'b01: CL22 Fast ETH PHY                                                                                   |
|        |             | 2'b10: CL45 10G ETH PHY (Link Resolution Only)                                                             |
|        |             | 2'b11: Auto-Polling Disable                                                                                |
| 15:13  | RESV2       | <b>Reserved</b>                                                                                            |
| 12:8   | P2_PHY_ADDR | <b>Port 2 PHY polling end address</b><br>Indicates the end of PHY address of PHY auto-polling process.     |
| 7:5    | RESV3       | <b>Reserved</b>                                                                                            |
| 4:0    | P1_PHY_ADDR | <b>Port 1 PHY polling start address</b><br>Indicates the start of PHY address of PHY auto-polling process. |

15110004      **MAC PIAC**      PHY indirect access control      00090000

| Bit   | 31           | 30    | 29            | 28 | 27 | 26 | 25 | 24            | 23 | 22 | 21 | 20 | 19       | 18 | 17       | 16 |
|-------|--------------|-------|---------------|----|----|----|----|---------------|----|----|----|----|----------|----|----------|----|
| Name  | PHY_ACS_ST   | RESV0 | MDIO_REG_ADDR |    |    |    |    | MDIO_PHY_ADDR |    |    |    |    | MDIO_CMD |    | NMDIO_ST |    |
| Type  | W1C          | RW    | RW            |    |    |    |    | RW            |    |    |    |    | RW       |    | RW       |    |
| Reset | 0            | 0     | 0             | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 1        | 0  | 0        | 1  |
| Bit   | 15           | 14    | 13            | 12 | 11 | 10 | 9  | 8             | 7  | 6  | 5  | 4  | 3        | 2  | 1        | 0  |
| Name  | MDIO_RW_DATA |       |               |    |    |    |    |               |    |    |    |    |          |    |          |    |
| Type  | RW           |       |               |    |    |    |    |               |    |    |    |    |          |    |          |    |
| Reset | 0            | 0     | 0             | 0  | 0  | 0  | 0  | 0             | 0  | 0  | 0  | 0  | 0        | 0  | 0        | 0  |

| Bit(s) | Name          | Description                                                                                                                                                                                                                                                                        |
|--------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | PHY_ACS_ST    | <b>PHY access start</b><br><br>Starts indirect access to PHY's register. While PHY's register access is complete, this bit will be self-cleared to 0.<br><br>0: Idle or indirect access complete<br><br>1: Start PHY access                                                        |
| 30     | RESV0         | <b>Reserved</b>                                                                                                                                                                                                                                                                    |
| 29:25  | MDIO_REG_ADDR | <b>Register Address (Clause 22) or Device Address (Clause 45)</b>                                                                                                                                                                                                                  |
| 24:20  | MDIO_PHY_ADDR | <b>PHY Address (Clause 22) or Port Address (Clause 45)</b>                                                                                                                                                                                                                         |
| 19:18  | MDIO_CMD      | <b>MDIO command</b><br><br>2'b00: Address (Clause 45)<br><br>2'b01: MDIO write<br><br>2'b10: MDIO read (Clause 22) / Read inc (Clause 45)<br><br>2'b11: MDIO read (Clause 45)                                                                                                      |
| 17:16  | NMDIO_ST      | <b>MDIO start field</b><br><br>2'b00: Start (Clause 45)<br><br>2'b01: Start (Clause 22)<br><br>Other: Reserved                                                                                                                                                                     |
| 15:0   | MDIO_RW_DATA  | <b>MDIO read/write data</b><br><br>This is used as MDIO data field for read/write data access.<br><br>When MDIO write command is activated, this is used as MDIO write data field. When MDIO read command is activated, this is used as MDIO read data field for read access only. |

15110008      **MAC\_GPC**      **GIGA MAC port control**      400C400C

| Bit   | 31 | 30 | 29 | 28 | 27    | 26 | 25 | 24 | 23           | 22           | 21           | 20           | 19             | 18             | 17         | 16 |
|-------|----|----|----|----|-------|----|----|----|--------------|--------------|--------------|--------------|----------------|----------------|------------|----|
| Name  |    |    |    |    | RESV0 |    |    |    | P2_RMII_CKRX | P2_RMII_CKIN | P2_TMII_FREQ | P2_TMII_MODE | P2_TX_CLK_MODE | P2_RX_CLK_MODE | P2_RX_SKEW |    |
| Type  |    |    |    |    | RW    |    |    |    | RW           | RW           | RW           | RW           | RW             | RW             | RW         |    |
| Reset |    |    |    |    | 0     | 0  | 0  |    | 0            | 0            | 0            | 0            | 1              | 1              | 0          | 0  |
| Bit   | 15 | 14 | 13 | 12 | 11    | 10 | 9  | 8  | 7            | 6            | 5            | 4            | 3              | 2              | 1          | 0  |
| Name  |    |    |    |    |       |    |    |    | RESV2        |              | P1_TMII_FREQ | P1_TMII_MODE | P1_TX_CLK_MODE | P1_RX_CLK_MODE | P1_RX_SKEW |    |
| Type  |    |    |    |    |       |    |    |    | RW           |              | RW           | RW           | RW             | RW             | RW         |    |
| Reset |    |    |    |    |       |    |    |    | 0            | 0            | 0            | 0            | 1              | 1              | 0          | 0  |

| Bit(s) | Name           | Description                                                                                                                              |
|--------|----------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 27:25  | RESV0          | <b>Reserved</b>                                                                                                                          |
| 23     | P2_RMII_CKRX   | <b>RMII reference clock pin selection</b><br><br>0: TXC<br><br>1: RXC                                                                    |
| 22     | P2_RMII_CKIN   | <b>RMII reference clock direction</b><br><br>0: Output<br><br>1: Input                                                                   |
| 21     | P2_TMII_FREQ   | <b>TMII frequency</b>                                                                                                                    |
| 20     | P2_TMII_MODE   | <b>TMII mode</b><br><br>Switch to Turbot MII mode                                                                                        |
| 19     | P2_TX_CLK_MODE | <b>P2 TX clock control</b><br><br>0: HP mode (clock and data are in-phase)<br><br>1: 3Com mode (clock and data is 90 degree offset)      |
| 18     | P2_RX_CLK_MODE | <b>P2 RX clock control</b><br><br>0: Delay 2ns on input rx_clk<br><br>1: No delay                                                        |
| 17:16  | P2_RX_SKEW     | <b>P2 RX clock skew control</b><br><br>2'b00: No delay<br><br>2'b01: Delay 150ps<br><br>2'b10: Delay 300ps<br><br>2'b11: Clock inversion |
| 7:6    | RESV2          | <b>Reserved</b>                                                                                                                          |
| 5      | P1_TMII_FREQ   | <b>TMII frequency</b>                                                                                                                    |

| Bit(s) | Name           | Description                                                                                                                              |
|--------|----------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 4      | P1_TMII_MODE   | <b>TMII mode</b><br><br>Switch to Turbot MII mode                                                                                        |
| 3      | P1_TX_CLK_MODE | <b>P1 TX clock control</b><br><br>0: HP mode (clock and data are in-phase)<br><br>1: 3Com mode (clock and data is 90 degree offset)      |
| 2      | P1_RX_CLK_MODE | <b>P1 RX clock control</b><br><br>0: Delay 2ns on input rx_clk<br><br>1: No delay                                                        |
| 1:0    | P1_RX_SKEW     | <b>P1 RX clock skew control</b><br><br>2'b00: No delay<br><br>2'b01: Delay 150ps<br><br>2'b10: Delay 300ps<br><br>2'b11: Clock inversion |

**1511000C XGMAC\_STS XGMAC status register 08000800**

| Bit   | 31                              | 30    | 29 | 28 | 27                    | 26    | 25                     | 24                             | 23    | 22 | 21                     | 20                     | 19                      | 18 | 17 | 16                            |
|-------|---------------------------------|-------|----|----|-----------------------|-------|------------------------|--------------------------------|-------|----|------------------------|------------------------|-------------------------|----|----|-------------------------------|
| Name  | P2_XG<br>MAC_F<br>ORCE          | RESV6 |    |    | P2_FO<br>RCE_LI<br>NK | RESV5 | P2_EXT<br>PHY_L<br>INK | P2_US<br>XGMII<br>PCS_LI<br>NK | RESV4 |    | P2_XG<br>MAC_R<br>X_FC | P2_XG<br>MAC_T<br>X_FC | P2_USXGMII_PCS_MO<br>DE |    |    | P2_XG<br>MAC_L<br>INK_ST<br>S |
| Type  | RW                              | RW    |    |    | RW                    | RW    | RO                     | RO                             | RO    |    | RO                     | RO                     | RO                      |    |    | RO                            |
| Reset | 0                               | 0     | 0  | 0  | 1                     | 0     | 0                      | 0                              | 0     | 0  | 0                      | 0                      | 0                       | 0  | 0  | 0                             |
| Bit   | 15                              | 14    | 13 | 12 | 11                    | 10    | 9                      | 8                              | 7     | 6  | 5                      | 4                      | 3                       | 2  | 1  | 0                             |
| Name  | P1_XG<br>MAC_F<br>ORCE_<br>LINK | RESV3 |    |    | P1_FO<br>RCE_LI<br>NK | RESV2 | P1_EXT<br>PHY_L<br>INK | P1_US<br>XGMII<br>PCS_LI<br>NK | RESV1 |    | P1_XG<br>MAC_R<br>X_FC | P1_XG<br>MAC_T<br>X_FC | P1_USXGMII_PCS_MO<br>DE |    |    | P1_XG<br>MAC_L<br>INK_ST<br>S |
| Type  | RW                              | RW    |    |    | RW                    | RW    | RO                     | RO                             | RO    |    | RO                     | RO                     | RO                      |    |    | RO                            |
| Reset | 0                               | 0     | 0  | 0  | 1                     | 0     | 0                      | 0                              | 0     | 0  | 0                      | 0                      | 0                       | 0  | 0  | 0                             |

| Bit(s) | Name                | Description                                                                                                                                                                                                                                                                     |
|--------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31     | P2_XGMAC_FORCE      | <b>Port 2 XGMAC Force Mode enable</b><br><br>1'b0: XGMAC Link Status by PCS (P2_USXGMII_PCS_LINK)<br><br>1'b1: XGMAC Link Status by Force Value (P2_FORCE_LINK)                                                                                                                 |
| 30:28  | RESV6               | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 27     | P2_FORCE_LINK       | <b>Port 2 XGMAC Force Link Mode</b><br><br>1'b0: Force XGMAC link down<br><br>1'b1: Force XGMAC link up                                                                                                                                                                         |
| 26     | RESV5               | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 25     | P2_EXT_PHY_LINK     | <b>P1 external PHY link status by auto-polling mechanism</b><br><br>If auto-polling is supported, this PHY link status will be logic-AND with PCS Link status (USXGMII_PCS_LINK) to come out the final link status (XGMAC_LINK_STS)<br><br>1'b0: Link down<br><br>1'b1: Link up |
| 24     | P2_USXGMII_PCS_LINK | <b>Port 2 USXGMII link status</b><br><br>1'b0: Link down<br><br>1'b1: Link up                                                                                                                                                                                                   |
| 23:22  | RESV4               | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 21     | P2_XGMAC_RX_FC      | <b>Port 2 XGMAC RX pause capability</b><br><br>1'b0: Disable<br><br>1'b1: Enable                                                                                                                                                                                                |
| 20     | P2_XGMAC_TX_FC      | <b>Port 2 XGMAC TX pause capability</b><br><br>1'b0: Disable                                                                                                                                                                                                                    |

| Bit(s) | Name                | Description                                                                                                                                                                                                                                                                     |
|--------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                     | 1'b1: Enable                                                                                                                                                                                                                                                                    |
| 19:17  | P2_USXGMII_PCS_MODE | <b>Port 2 USXGMII PCS mode</b><br><br>3'b000: 10G USXGMII<br><br>3'b001: 5G USXGMII<br><br>3'b010: 2.5G USXGMII<br><br>3'b011: 1G USXGMII<br><br>3'b1xx: Reserved                                                                                                               |
| 16     | P2_XGMAC_LINK_STS   | <b>Port 2 XGMAC final link status</b><br><br>1'b0: Link down<br><br>1'b1: Link up                                                                                                                                                                                               |
| 15     | P1_XGMAC_FORCE_LINK | <b>Port 1 XGMAC Force Mode enable</b><br><br>1'b0: XGMAC Link Status by PCS (P1_USXGMII_PCS_LINK)<br><br>1'b1: XGMAC Link Status by Force Value (P1_FORCE_LINK)                                                                                                                 |
| 14:12  | RESV3               | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 11     | P1_FORCE_LINK       | <b>Port 1 XGMAC Force Link Mode</b><br><br>1'b0: Force XGMAC link down<br><br>1'b1: Force XGMAC link up                                                                                                                                                                         |
| 10     | RESV2               | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 9      | P1_EXT_PHY_LINK     | <b>P1 external PHY link status by auto-polling mechanism</b><br><br>If auto-polling is supported, this PHY link status will be logic-AND with PCS Link status (USXGMII_PCS_LINK) to come out the final link status (XGMAC_LINK_STS)<br><br>1'b0: Link down<br><br>1'b1: Link up |
| 8      | P1_USXGMII_PCS_LINK | <b>Port 1 USXGMII link status</b><br><br>1'b0: Link down<br><br>1'b1: Link up                                                                                                                                                                                                   |
| 7:6    | RESV1               | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 5      | P1_XGMAC_RX_FC      | <b>Port 1 XGMAC RX pause capability</b><br><br>1'b0: Disable<br><br>1'b1: Enable                                                                                                                                                                                                |
| 4      | P1_XGMAC_TX_FC      | <b>Port 1 XGMAC TX pause capability</b><br><br>1'b0: Disable                                                                                                                                                                                                                    |



| Bit(s) | Name                | Description                                                                                                                                                       |
|--------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |                     | 1'b1: Enable                                                                                                                                                      |
| 3:1    | P1_USXGMII_PCS_MODE | <b>Port 1 USXGMII PCS mode</b><br><br>3'b000: 10G USXGMII<br><br>3'b001: 5G USXGMII<br><br>3'b010: 2.5G USXGMII<br><br>3'b011: 1G USXGMII<br><br>3'b1xx: Reserved |
| 0      | P1_XGMAC_LINK_STS   | <b>Port 1 XGMAC final link status</b><br><br>1'b0: Link down<br><br>1'b1: Link up                                                                                 |

**15110010      MAC\_MISC      MAC MISC register      00000006**

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21          | 20            | 19    | 18            | 17          | 16    |
|-------|-------|----|----|----|----|----|----|----|----|----|-------------|---------------|-------|---------------|-------------|-------|
| Name  | RESV3 |    |    |    |    |    |    |    |    |    |             |               |       |               |             |       |
| Type  | RW    |    |    |    |    |    |    |    |    |    |             |               |       |               |             |       |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0             | 0     | 0             | 0           | 0     |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5           | 4             | 3     | 2             | 1           | 0     |
| Name  | RESV3 |    |    |    |    |    |    |    |    |    | CHK_T<br>A1 | MDC_T<br>URBO | RESV2 | CNTR_<br>WRAP | CNTR_<br>RC | RESV1 |
| Type  | RW    |    |    |    |    |    |    |    |    |    | RW          | RW            | RW    | RW            | RW          | RW    |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0             | 0     | 1             | 1           | 0     |

| Bit(s) | Name      | Description                                                                                                                                                                                                           |
|--------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6   | RESV3     | <b>Reserved</b>                                                                                                                                                                                                       |
| 5      | CHK_TA1   | <b>Check MDIO Turn Around Bit (TA)</b><br><br>1'b0: Check Pull-High during Turn-Around<br><br>1'b1: Disable                                                                                                           |
| 4      | MDC_TURBO | <b>MDC clock Turbo mode</b><br><br>When this bit is set, MDC clock is sourced from 25MHz system clock and divided by PHY_MDC_CFG.<br><br>1'b0: MDC clock source from 12.5MHz<br><br>1'b0: MDC clock source from 25MHz |
| 3      | RESV2     | <b>Reserved</b>                                                                                                                                                                                                       |
| 2      | CNTR_WRAP | <b>counter wrap control</b><br><br>1'b0: counter wrap disabled<br><br>1'b1: counter wrap enabled                                                                                                                      |
| 1      | CNTR_RC   | <b>counter read clear control</b><br><br>1'b0: counter read clear disabled<br><br>1'b1: counter read clear enabled                                                                                                    |
| 0      | RESV1     | <b>Reserved</b>                                                                                                                                                                                                       |

15110018      MAC\_GPC1      GIGA MAC port control - P3      0000400C

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23    | 22 | 21           | 20           | 19             | 18             | 17         | 16 |
|-------|----|----|----|----|----|----|----|----|-------|----|--------------|--------------|----------------|----------------|------------|----|
| Name  |    |    |    |    |    |    |    |    |       |    |              |              |                |                |            |    |
| Type  |    |    |    |    |    |    |    |    |       |    |              |              |                |                |            |    |
| Reset |    |    |    |    |    |    |    |    |       |    |              |              |                |                |            |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7     | 6  | 5            | 4            | 3              | 2              | 1          | 0  |
| Name  |    |    |    |    |    |    |    |    | RESV2 |    | P3_TMII_FREQ | P3_TMII_MODE | P3_TX_CLK_MODE | P3_RX_CLK_MODE | P3_RX_SKEW |    |
| Type  |    |    |    |    |    |    |    |    | RW    |    | RW           | RW           | RW             | RW             | RW         |    |
| Reset |    |    |    |    |    |    |    |    | 0     | 0  | 0            | 0            | 1              | 1              | 0          | 0  |

| Bit(s) | Name           | Description                                                                                                                              |
|--------|----------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6    | RESV2          | <b>Reserved</b>                                                                                                                          |
| 5      | P3_TMII_FREQ   | <b>TMII frequency</b>                                                                                                                    |
| 4      | P3_TMII_MODE   | <b>TMII mode</b><br><br>Switch to Turbot MII mode                                                                                        |
| 3      | P3_TX_CLK_MODE | <b>P1 TX clock control</b><br><br>0: HP mode (clock and data are in-phase)<br><br>1: 3Com mode (clock and data is 90 degree offset)      |
| 2      | P3_RX_CLK_MODE | <b>P1 RX clock control</b><br><br>0: Delay 2ns on input rx_clk<br><br>1: No delay                                                        |
| 1:0    | P3_RX_SKEW     | <b>P1 RX clock skew control</b><br><br>2'b00: No delay<br><br>2'b01: Delay 150ps<br><br>2'b10: Delay 300ps<br><br>2'b11: Clock inversion |

**1511001C XGMAC\_STS1 XGMAC status register - P3 00000800**

| Bit   | 31                              | 30    | 29 | 28 | 27                    | 26    | 25                     | 24                              | 23    | 22 | 21                     | 20                     | 19                      | 18 | 17 | 16                            |
|-------|---------------------------------|-------|----|----|-----------------------|-------|------------------------|---------------------------------|-------|----|------------------------|------------------------|-------------------------|----|----|-------------------------------|
| Name  |                                 |       |    |    |                       |       |                        |                                 |       |    |                        |                        |                         |    |    |                               |
| Type  |                                 |       |    |    |                       |       |                        |                                 |       |    |                        |                        |                         |    |    |                               |
| Reset |                                 |       |    |    |                       |       |                        |                                 |       |    |                        |                        |                         |    |    |                               |
| Bit   | 15                              | 14    | 13 | 12 | 11                    | 10    | 9                      | 8                               | 7     | 6  | 5                      | 4                      | 3                       | 2  | 1  | 0                             |
| Name  | P3_XG<br>MAC_F<br>ORCE_<br>LINK | RESV3 |    |    | P3_FO<br>RCE_LI<br>NK | RESV2 | P3_EXT<br>PHY_L<br>INK | P3_US<br>XGMII_<br>PCS_LI<br>NK | RESV1 |    | P3_XG<br>MAC_R<br>X_FC | P3_XG<br>MAC_T<br>X_FC | P3_USXGMII_PCS_MO<br>DE |    |    | P3_XG<br>MAC_L<br>INK_ST<br>S |
| Type  | RW                              | RW    |    |    | RW                    | RW    | RO                     | RO                              | RO    |    | RO                     | RO                     | RO                      |    |    | RO                            |
| Reset | 0                               | 0     | 0  | 0  | 1                     | 0     | 0                      | 0                               | 0     | 0  | 0                      | 0                      | 0                       | 0  | 0  | 0                             |

| Bit(s) | Name                | Description                                                                                                                                                                                                                                                                     |
|--------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15     | P3_XGMAC_FORCE_LINK | <b>Port 3 XGMAC Force Mode enable</b><br><br>1'b0: XGMAC Link Status by PCS (P3_USXGMII_PCS_LINK)<br><br>1'b1: XGMAC Link Status by Force Value (P3_FORCE_LINK)                                                                                                                 |
| 14:12  | RESV3               | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 11     | P3_FORCE_LINK       | <b>Port 3 XGMAC Force Link Mode</b><br><br>1'b0: Force XGMAC link down<br><br>1'b1: Force XGMAC link up                                                                                                                                                                         |
| 10     | RESV2               | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 9      | P3_EXT_PHY_LINK     | <b>P3 external PHY link status by auto-polling mechanism</b><br><br>If auto-polling is supported, this PHY link status will be logic-AND with PCS Link status (USXGMII_PCS_LINK) to come out the final link status (XGMAC_LINK_STS)<br><br>1'b0: Link down<br><br>1'b1: Link up |
| 8      | P3_USXGMII_PCS_LINK | <b>Port 3 USXGMII link status</b><br><br>1'b0: Link down<br><br>1'b1: Link up                                                                                                                                                                                                   |
| 7:6    | RESV1               | <b>Reserved</b>                                                                                                                                                                                                                                                                 |
| 5      | P3_XGMAC_RX_FC      | <b>Port 3 XGMAC RX pause capability</b><br><br>1'b0: Disable<br><br>1'b1: Enable                                                                                                                                                                                                |
| 4      | P3_XGMAC_TX_FC      | <b>Port 3 XGMAC TX pause capability</b><br><br>1'b0: Disable<br><br>1'b1: Enable                                                                                                                                                                                                |
| 3:1    | P3_USXGMII_PCS_MODE | <b>Port 3 USXGMII PCS mode</b>                                                                                                                                                                                                                                                  |

| Bit(s) | Name              | Description                           |
|--------|-------------------|---------------------------------------|
|        |                   | 3'b000: 10G USXGMII                   |
|        |                   | 3'b001: 5G USXGMII                    |
|        |                   | 3'b010: 2.5G USXGMII                  |
|        |                   | 3'b011: 1G USXGMII                    |
|        |                   | 3'b1xx: Reserved                      |
| 0      | P3_XGMAC_LINK_STS | <b>Port 3 XGMAC final link status</b> |
|        |                   | 1'b0: Link down                       |
|        |                   | 1'b1: Link up                         |

| 15110080 |           | <u>GSW_CFG</u> |    |    | GSW bridge registers |    |    |    |    |    |    |    | 000C000C  |    |    |    |
|----------|-----------|----------------|----|----|----------------------|----|----|----|----|----|----|----|-----------|----|----|----|
| Bit      | 31        | 30             | 29 | 28 | 27                   | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| Name     | GSWTX_RSV |                |    |    |                      |    |    |    |    |    |    |    | GSWTX_IPG |    |    |    |
| Type     | RW        |                |    |    |                      |    |    |    |    |    |    |    | RW        |    |    |    |
| Reset    | 0         | 0              | 0  | 0  | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1         | 1  | 0  | 0  |
| Bit      | 15        | 14             | 13 | 12 | 11                   | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| Name     | GSWRX_RSV |                |    |    |                      |    |    |    |    |    |    |    | GSWRX_IPG |    |    |    |
| Type     | RW        |                |    |    |                      |    |    |    |    |    |    |    | RW        |    |    |    |
| Reset    | 0         | 0              | 0  | 0  | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1         | 1  | 0  | 0  |

| Bit(s) | Name      | Description                                              |
|--------|-----------|----------------------------------------------------------|
| 31:20  | GSWTX_RSV | Reserved                                                 |
| 19:16  | GSWTX_IPG | GSW bridge TX IPG cycle setting between data of packets. |
| 15:4   | GSWRX_RSV | Reserved                                                 |
| 3:0    | GSWRX_IPG | GSW bridge RX IPG cycle setting between data of packets. |

15110088      GSW\_STS      GSW bridge status      01010101

| Bit   | 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | GSWTX_STS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| Bit   | 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | GSWRX_STS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |

| Bit(s) | Name      | Description   |
|--------|-----------|---------------|
| 31:16  | GSWTX_STS | GSW TX status |
| 15:0   | GSWRX_STS | GSW RX status |

15110100      **MAC P1\_MCR**      Port 1 MAC control      20006300

| Bit   | 31           | 30        | 29        | 28              | 27                          | 26           | 25             | 24         | 23          | 22           | 21          | 20          | 19        | 18 | 17        | 16                |
|-------|--------------|-----------|-----------|-----------------|-----------------------------|--------------|----------------|------------|-------------|--------------|-------------|-------------|-----------|----|-----------|-------------------|
| Name  | MAX_RX_JUMBO |           |           |                 | RESV0                       |              | MAC_RX_PKT_LEN |            | MTCC_LMT    |              |             |             | IPG_CFG   |    | RESV1     | DIFF_RX_FIFO_WCLR |
| Type  | RW           |           |           |                 | RW                          |              | RW             |            | RW          |              |             |             | RW        |    | RW        | RW                |
| Reset | 0            | 0         | 1         | 0               | 0                           | 0            | 0              | 0          | 0           | 0            | 0           | 0           | 0         | 0  | 0         | 0                 |
| Bit   | 15           | 14        | 13        | 12              | 11                          | 10           | 9              | 8          | 7           | 6            | 5           | 4           | 3         | 2  | 1         | 0                 |
| Name  | FORCE_MOD_E  | MAC_TX_EN | MAC_RX_EN | DEL_RX_FIFO_CLR | GMAC_RDMA_HANG_ECO_ROLLBACK | PRMBL_LMT_EN | BKOFF_EN       | BACKP_R_EN | FORCE_EEE1G | FORCE_EEE10G | FORCE_RX_FC | FORCE_TX_FC | FORCE_SPD |    | FORCE_DPX | FORCE_LINK        |
| Type  | RW           | RW        | RW        | RW              | RW                          | RW           | RW             | RW         | RW          | RW           | RW          | RW          | RW        |    | RW        | RW                |
| Reset | 0            | 1         | 1         | 0               | 0                           | 0            | 1              | 1          | 0           | 0            | 0           | 0           | 0         | 0  | 0         | 0                 |

| Bit(s) | Name           | Description                                                                                                                                                                                                                                                                                                               |
|--------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | MAX_RX_JUMBO   | <b>Maximum received jumbo packet length</b><br><br>4'h0, 4'h1: Reserved<br><br>4'h2: 2 Kbytes (maxi. length on FE/GDM)<br><br>4'h3 ... 4'hF: Reserved                                                                                                                                                                     |
| 27:26  | RESV0          | <b>Reserved</b>                                                                                                                                                                                                                                                                                                           |
| 25:24  | MAC_RX_PKT_LEN | <b>Maximum received packet length</b><br><br>Sets the maximum length of ingress packets including CRC that can be received by MAC.<br><br>2'b00: 1518 bytes for untagged frames; 1522 bytes for tagged frames<br><br>2'b01: 1536 bytes<br><br>2'b10: 1552 bytes<br><br>2'b11: MAX_RX_JUMBO                                |
| 23:20  | MTCC_LMT       | <b>MTCC limit</b><br><br>Maximum transmit collision count limitation.<br><br>0: Disable TX collision abort function, and send packet until success<br><br>1 ~ 15: Maximum transmit collision count                                                                                                                        |
| 19:18  | IPG_CFG        | <b>Inter-frame gap shrink</b><br><br>2'b00: Normal 96-bit IFG<br><br>2'b01: Transmit 96-bit IFG with short IFG in random behavior.<br><br>2'b10: Shrink 64-bit IFG<br><br>2'b11: When any output queue inside the port is congested, shrink 64-bit IFG will be enabled; otherwise, normal 96-bit IFG will be the default. |
| 17     | RESV1          | <b>Reserved</b>                                                                                                                                                                                                                                                                                                           |

| Bit(s) | Name                        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--------|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16     | DIFF_RXFIFO_WCLR            | <b>Change RX FIFO wclear function</b><br>0: Remain RX FIFO wclear function<br>1: Change RX FIFO wclear function                                                                                                                                                                                                                                                                                                                             |
| 15     | FORCE_MODE                  | <b>Force MAC mode</b><br>0: Force mode off (MAC status is decided by PHY auto-polling)<br>1: Force mode on (MAC status is determined by FORCE_XXX register)                                                                                                                                                                                                                                                                                 |
| 14     | MAC_TX_EN                   | <b>TX MAC enable</b><br>0: TX MAC function is disabled<br>1: TX MAC function is enabled                                                                                                                                                                                                                                                                                                                                                     |
| 13     | MAC_RX_EN                   | <b>RX MAC enable</b><br>0: RX MAC function is disabled<br>1: RX MAC function is enabled                                                                                                                                                                                                                                                                                                                                                     |
| 12     | DEL_RXFIFO_CLR              | <b>Disables RX FIFO clear function</b><br>0: Remain RX FIFO clear function<br>1: Broke RX FIFO clear function                                                                                                                                                                                                                                                                                                                               |
| 11     | GMAC_RDMA_HANG_ECO_ROLLBACK | <b>Rollback ECO for GMAC RDMA hang issue</b><br>0: ECO is enabled<br>1: Rollback ECO                                                                                                                                                                                                                                                                                                                                                        |
| 10     | PRMBL_LMT_EN                | <b>Preamble limit enable</b><br>0: RXMAC can recognize the Start Frame Delimiter (SFD), without needing to receive a byte with the value of 55 in the preamble.<br>1: RXMAC will recognize the SFD before the next new frame when it receives the 7 consecutive bytes with the value of 55 within the 8-byte Preamble. If SFD (8'hd5) shows up after the 8-byte Preamble, RXMAC will not recognize it and treat it as if there were no SFD. |
| 9      | BKOFF_EN                    | <b>Back-off enable</b><br>0: Disabled<br>1: Let MAC follow the back-off mechanism when collision happens                                                                                                                                                                                                                                                                                                                                    |
| 8      | BACKPR_EN                   | <b>Back-Pressure enable</b><br>0: Disabled<br>1: Enable back-pressure mechanism when operating in half-duplex mode and flow-control is on                                                                                                                                                                                                                                                                                                   |
| 7      | FORCE_EEE1G                 | <b>Force LPI mode for 1000m link speed</b><br>When (FORCE_MODE= 1), these bits are used to control MAC EEE mode                                                                                                                                                                                                                                                                                                                             |



| Bit(s) | Name         | Description                                                                                                                                                                                                                                                     |
|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 0: Do not have the ability of entering EEE low power idle mode for 1000m link speed<br>1: Have the ability of entering EEE low power idle mode                                                                                                                  |
| 6      | FORCE_EEE100 | <b>Force LPI mode for 100m link speed</b><br>When (FORCE_MODE= 1), these bits are used to control MAC EEE mode<br>0: Do not have the ability of entering EEE low power idle mode for 100m link speed<br>1: Have the ability of entering EEE low power idle mode |
| 5      | FORCE_RX_FC  | <b>Force RX flow control</b><br>When (FORCE_MODE= 1), these bits are used to control MAC RX flow control<br>0: Disable<br>1: Let MAC accept the pause frame when operating in full-duplex mode and flow-control is on                                           |
| 4      | FORCE_TX_FC  | <b>Force TX flow control</b><br>When (FORCE_MODE= 1), these bits are used to control MAC TX flow control<br>0: Disable<br>1: Let MAC transmit the pause frame when operating in full-duplex mode and flow-control is on                                         |
| 3:2    | FORCE_SPD    | <b>Force link speed</b><br>When (FORCE_MODE= 1), these bits are used to control MAC link speed<br>2'b00: 10 Mbps<br>2'b01: 100 Mbps<br>2'b10: 1000 Mbps<br>2'b11: reserved                                                                                      |
| 1      | FORCE_DPX    | <b>Force duplex</b><br>When (FORCE_MODE= 1), these bits are used to control MAC link duplex<br>0: Half-duplex<br>1: Full-duplex                                                                                                                                 |
| 0      | FORCE_LINK   | <b>Force link state</b><br>When (FORCE_MODE= 1), these bits are used to control MAC link state<br>0: Link down<br>1: Link up                                                                                                                                    |

15110104      MAC P1\_EEE      Port 1 EEE control      00000002

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19         | 18        | 17 | 16       |
|-------|------------------|----|----|----|----|----|----|----|-----------------|----|----|----|------------|-----------|----|----------|
| Name  | WAKEUP_TIME_1000 |    |    |    |    |    |    |    | WAKEUP_TIME_100 |    |    |    |            |           |    |          |
| Type  | RW               |    |    |    |    |    |    |    | RW              |    |    |    |            |           |    |          |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0          | 0         | 0  | 0        |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3          | 2         | 1  | 0        |
| Name  | LPI_TXIDLE_THD   |    |    |    |    |    |    |    | RESV0           |    |    |    | CKG_TXIDLE | CKG_RXLPI |    | LPI_MODE |
| Type  | RW               |    |    |    |    |    |    |    | RW              |    |    |    | RW         | RW        |    | RW       |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0          | 0         |    | 0        |

| Bit(s) | Name             | Description                                                                                                                                                                                                                                        |
|--------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | WAKEUP_TIME_1000 | <b>Wake up time for 1000-Mbps LPI mode</b><br><br>The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packet after wake-up<br><br>Time unit: 1us                                                         |
| 23:16  | WAKEUP_TIME_100  | <b>Wake up time for 100-Mbps LPI mode</b><br><br>The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packet after wake-up<br><br>Time unit: 1us                                                          |
| 15:8   | LPI_TXIDLE_THD   | <b>TX IDLE timer to enter LPI mode</b><br><br>When there is no packet to be transmitted and LPI_TXIDLE_THD is exceeded, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI signal to link partner<br><br>Time unit: 1ms |
| 7:4    | RESV0            | <b>Reserved</b>                                                                                                                                                                                                                                    |
| 3      | CKG_TXIDLE       | <b>TX clock power down</b><br><br>0: Disable<br><br>1: Stop TX clock when the corresponding port has no traffic to send and has entered IDLE state for <LPI_TXIDLE_THD> ms.                                                                        |
| 2      | CKG_RXLPI        | <b>RX clock power down</b><br><br>0: Disable<br><br>1: Stop RX clock ticking when the corresponding port entering the LPI mode and IDLE state.                                                                                                     |
| 0      | LPI_MODE         | <b>LPI mode activated</b><br><br>0: Disable<br><br>1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner                                                                                                         |

15110108      **MAC P1\_SR**      Port 1 MAC status      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23           | 22            | 21           | 20           | 19         | 18 | 17         | 16          |
|-------|-------|----|----|----|----|----|----|----|--------------|---------------|--------------|--------------|------------|----|------------|-------------|
| Name  | RESV0 |    |    |    |    |    |    |    |              |               |              |              |            |    |            |             |
| Type  | RO    |    |    |    |    |    |    |    |              |               |              |              |            |    |            |             |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0            | 0             | 0            | 0            | 0          | 0  | 0          | 0           |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7            | 6             | 5            | 4            | 3          | 2  | 1          | 0           |
| Name  | RESV0 |    |    |    |    |    |    |    | EEE1G_STATUS | EEE100_STATUS | RX_FC_STATUS | TX_FC_STATUS | SPD_STATUS |    | DPX_STATUS | LINK_STATUS |
| Type  | RO    |    |    |    |    |    |    |    | RO           | RO            | RO           | RO           | RO         |    | RO         | RO          |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0            | 0             | 0            | 0            | 0          | 0  | 0          | 0           |

| Bit(s) | Name          | Description                                                                                                                                                                                    |
|--------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8   | RESV0         | <b>Reserved</b>                                                                                                                                                                                |
| 7      | EEE1G_STATUS  | <b>LPI mode for 1000m link speed</b><br><br>0: Do not have the ability of entering EEE low power idle mode for 1000m link speed<br><br>1: Have the ability of entering EEE low power idle mode |
| 6      | EEE100_STATUS | <b>LPI mode for 100m link speed</b><br><br>0: Do not have the ability of entering EEE low power idle mode for 100m link speed<br><br>1: Have the ability of entering EEE low power idle mode   |
| 5      | RX_FC_STATUS  | <b>RX flow control status</b><br><br>0: Disable<br><br>1: Let MAC accept the pause frame when operating in full-duplex mode and flow-control is on                                             |
| 4      | TX_FC_STATUS  | <b>TX flow control status</b><br><br>0: Disable<br><br>1: Let MAC transmit the pause frame when operating in full-duplex mode and flow-control is on                                           |
| 3:2    | SPD_STATUS    | <b>Link speed status</b><br><br>2'b00: 10 Mbps<br><br>2'b01: 100 Mbps<br><br>2'b10: 1000 Mbps<br><br>2'b11: reserved                                                                           |
| 1      | DPX_STATUS    | <b>Duplex status</b><br><br>0: Half-duplex<br><br>1: Full-duplex                                                                                                                               |
| 0      | LINK_STATUS   | <b>Link state</b>                                                                                                                                                                              |

| Bit(s) | Name | Description  |
|--------|------|--------------|
|        |      | 0: Link down |
|        |      | 1: Link up   |

**15110110      MAC P1 WOL      Port 1 WOL      00000000**

| Bit          | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19             | 18             | 17                 | 16             |
|--------------|----------------|----|----|----|----|----|----|----|----|----|----|----|----------------|----------------|--------------------|----------------|
| <b>Name</b>  | <b>WOL_DBG</b> |    |    |    |    |    |    |    |    |    |    |    |                |                | <b>WOL_INT_STS</b> | <b>WOL_STS</b> |
| <b>Type</b>  | <b>RO</b>      |    |    |    |    |    |    |    |    |    |    |    |                |                | <b>W1C</b>         | <b>RO</b>      |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0              | 0                  | 0              |
| Bit          | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3              | 2              | 1                  | 0              |
| <b>Name</b>  | <b>RESV0</b>   |    |    |    |    |    |    |    |    |    |    |    | <b>SNP_PKT</b> | <b>CRC_DIS</b> | <b>WOL_INT_EN</b>  | <b>WOL_EN</b>  |
| <b>Type</b>  | <b>RW</b>      |    |    |    |    |    |    |    |    |    |    |    | <b>RW</b>      | <b>RW</b>      | <b>RW</b>          | <b>RW</b>      |
| <b>Reset</b> | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0              | 0                  | 0              |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                  |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:18  | WOL_DBG     | <b>GMAC1 Wake-on-LAN debug signals</b>                                                                                                                                                                                                                                       |
| 17     | WOL_INT_STS | <b>GMAC1 Wake-on-LAN interrupt status</b>                                                                                                                                                                                                                                    |
| 16     | WOL_STS     | <b>GMAC1 Wake-on-LAN status</b><br><br>If WOL is enabled, this bit will change from 0 to 1 when GMAC RX state machine enters IDLE state. It indicates GMAC will drop all packets and detect magic packet.<br><br>0: Normal state<br><br>1: Listen state. Detect magic packet |
| 15:4   | RESV0       | <b>Reserved</b>                                                                                                                                                                                                                                                              |
| 3      | SNP_PKT     | <b>GMAC1 Wake-on-LAN with snoopy packet</b>                                                                                                                                                                                                                                  |
| 2      | CRC_DIS     | <b>GMAC1 Wake-on-LAN with CRC Check disable</b>                                                                                                                                                                                                                              |
| 1      | WOL_INT_EN  | <b>GMAC1 Wake-on-LAN Interrupt enable</b>                                                                                                                                                                                                                                    |
| 0      | WOL_EN      | <b>GMAC1 Wake-on-LAN Function enable</b>                                                                                                                                                                                                                                     |

15110114      **MAC P1 SGMII**      Port 1 SGMII      050B0001

| Bit   | 31                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16            |
|-------|-----------------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|---------------|
| Name  | LOADPSTMR_EXTEND_TIME |    |    |    |    |    |    |    | SYNCDONE_TIME |    |    |    |    |    |    |               |
| Type  | RW                    |    |    |    |    |    |    |    | RW            |    |    |    |    |    |    |               |
| Reset | 0                     | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0             | 0  | 0  | 0  | 1  | 0  | 1  | 1             |
| Bit   | 15                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0             |
| Name  |                       |    |    |    |    |    |    |    |               |    |    |    |    |    |    | DIS_TXCLK_ENA |
| Type  |                       |    |    |    |    |    |    |    |               |    |    |    |    |    |    | RW            |
| Reset |                       |    |    |    |    |    |    |    |               |    |    |    |    |    |    | 1             |

| Bit(s) | Name                  | Description                                                                                                        |
|--------|-----------------------|--------------------------------------------------------------------------------------------------------------------|
| 31:24  | LOADPSTMR_EXTEND_TIME | <b>rx_loadpstmr extend time in SGMII mode</b>                                                                      |
| 23:16  | SYNCDONE_TIME         | <b>Sync done time for RX flow control in SGMII mode</b>                                                            |
| 0      | DIS_TXCLK_ENA         | <b>Disables txclk_ena in SGMII mode</b><br><br>0: SGMII txclk_ena is enabled<br><br>1: SGMII txclk_ena is disabled |

15110118      **MAC P1\_PFC\_CTRL**      Port 1 PFC control      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19                | 18          | 17         | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|-------------------|-------------|------------|----|
| Name  | RESV |    |    |    |    |    |    |    |    |    |    |    |                   |             |            |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |                   |             |            |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0           | 0          | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3                 | 2           | 1          | 0  |
| Name  | RESV |    |    |    |    |    |    |    |    |    |    |    | PFC_AUTO_SYNC_DLY | PFC_SYNC_EN | PFC_ENABLE |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    | RW                | RW          | RW         |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0           | 0          | 0  |

| Bit(s) | Name              | Description                                                                                                                            |
|--------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:4   | RESV              | Reserved                                                                                                                               |
| 3:2    | PFC_AUTO_SYNC_DLY | <b>Selects the delay of sending PFC auto sync packet</b><br><br>0: Delay 0s<br><br>1: Delay 0.5s<br><br>2: Delay 1s<br><br>3: Delay 2s |
| 1      | PFC_SYNC_EN       | <b>Enables PFC auto-sync ability</b><br><br>0: Disable<br><br>1: Enable                                                                |
| 0      | PFC_EN            | <b>Enables PFC ability</b><br><br>0: Disable<br><br>1: Enable                                                                          |

**1511011C      MAC\_P1\_PFC\_STS      Port 1 PFC status      00000000**

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16          |
|-------|------------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|-------------|
| Name  | RESV       |    |    |    |    |    |    |    |            |    |    |    |    |    |    | PFC_AUTO_EN |
| Type  | RO         |    |    |    |    |    |    |    |            |    |    |    |    |    |    | RO          |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0           |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0           |
| Name  | TX_PFC_STS |    |    |    |    |    |    |    | RX_PFC_STS |    |    |    |    |    |    |             |
| Type  | RO         |    |    |    |    |    |    |    | RO         |    |    |    |    |    |    |             |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0           |

| Bit(s) | Name        | Description                                               |
|--------|-------------|-----------------------------------------------------------|
| 31:17  | RESV        | Reserved                                                  |
| 16     | PFC_AUTO_EN | PFC auto enable status<br><br>0: Disable<br><br>1: Enable |
| 15:8   | TX_PFC_STS  | TX PFC status                                             |
| 7:0    | RX_PFC_STS  | RX PFC status                                             |

**15110120      MAC\_P1\_PFC\_RX\_PSON\_CNT      Port 1 RX PFC pause on counter for low priority      00000000**
L

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  | Q3_RX_PSON_CNT |    |    |    |    |    |    |    | Q2_RX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q1_RX_PSON_CNT |    |    |    |    |    |    |    | Q0_RX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                 |
|--------|----------------|---------------------------------------------|
| 31:24  | Q3_RX_PSON_CNT | PFC RX pause on count for port 1 priority 3 |
| 23:16  | Q2_RX_PSON_CNT | PFC RX pause on count for port 1 priority 2 |
| 15:8   | Q1_RX_PSON_CNT | PFC RX pause on count for port 1 priority 1 |
| 7:0    | Q0_RX_PSON_CNT | PFC RX pause on count for port 1 priority 0 |

15110124 MAC P1 PFC RX PSON\_CNT Port 1 RX PFC pause on counter for high priority

00000000

H

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  | Q7_RX_PSON_CNT |    |    |    |    |    |    |    | Q6_RX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_RX_PSON_CNT |    |    |    |    |    |    |    | Q4_RX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                 |
|--------|----------------|---------------------------------------------|
| 31:24  | Q7_RX_PSON_CNT | PFC RX pause on count for port 1 priority 7 |
| 23:16  | Q6_RX_PSON_CNT | PFC RX pause on count for port 1 priority 6 |
| 15:8   | Q5_RX_PSON_CNT | PFC RX pause on count for port 1 priority 5 |
| 7:0    | Q4_RX_PSON_CNT | PFC RX pause on count for port 1 priority 4 |

15110128 MAC P1 PFC RX PSOFF\_CNTPort 1 RX PFC pause off counter for low priority

00000000

L

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | Q3_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q2_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q1_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q0_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                  |
|--------|-----------------|----------------------------------------------|
| 31:24  | Q3_RX_PSOFF_CNT | PFC RX pause off count for port 1 priority 3 |
| 23:16  | Q2_RX_PSOFF_CNT | PFC RX pause off count for port 1 priority 2 |
| 15:8   | Q1_RX_PSOFF_CNT | PFC RX pause off count for port 1 priority 1 |
| 7:0    | Q0_RX_PSOFF_CNT | PFC RX pause off count for port 1 priority 0 |



1511012C **MAC P1 PFC RX PSOFF\_CNT** Port 1 RX PFC pause off counter for high priority 00000000

H

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | Q7_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q6_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q4_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                  |
|--------|-----------------|----------------------------------------------|
| 31:24  | Q7_RX_PSOFF_CNT | PFC RX pause off count for port 1 priority 7 |
| 23:16  | Q6_RX_PSOFF_CNT | PFC RX pause off count for port 1 priority 6 |
| 15:8   | Q5_RX_PSOFF_CNT | PFC RX pause off count for port 1 priority 5 |
| 7:0    | Q4_RX_PSOFF_CNT | PFC RX pause off count for port 1 priority 4 |

15110130 **MAC P1 PFC TX PSON\_CNT** Port 1 TX PFC pause on counter for low priority 00000000

L

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  | Q3_TX_PSON_CNT |    |    |    |    |    |    |    | Q2_TX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q1_TX_PSON_CNT |    |    |    |    |    |    |    | Q0_TX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                 |
|--------|----------------|---------------------------------------------|
| 31:24  | Q3_TX_PSON_CNT | PFC TX pause on count for port 1 priority 3 |
| 23:16  | Q2_TX_PSON_CNT | PFC TX pause on count for port 1 priority 2 |
| 15:8   | Q1_TX_PSON_CNT | PFC TX pause on count for port 1 priority 1 |
| 7:0    | Q0_TX_PSON_CNT | PFC TX pause on count for port 1 priority 0 |

15110134 MAC P1\_PFC\_TX\_PSON\_CNT Port 1 TX PFC pause on counter for high priority

00000000

H

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  | Q7_TX_PSON_CNT |    |    |    |    |    |    |    | Q6_TX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_TX_PSON_CNT |    |    |    |    |    |    |    | Q4_TX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                 |
|--------|----------------|---------------------------------------------|
| 31:24  | Q7_TX_PSON_CNT | PFC TX pause on count for port 1 priority 7 |
| 23:16  | Q6_TX_PSON_CNT | PFC TX pause on count for port 1 priority 6 |
| 15:8   | Q5_TX_PSON_CNT | PFC TX pause on count for port 1 priority 5 |
| 7:0    | Q4_TX_PSON_CNT | PFC TX pause on count for port 1 priority 4 |

15110138 MAC P1\_PFC\_TX\_PSOFF\_CNT Port 1 TX PFC pause off counter for low priority

00000000

L

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | Q3_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q2_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q1_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q0_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                  |
|--------|-----------------|----------------------------------------------|
| 31:24  | Q3_TX_PSOFF_CNT | PFC TX pause off count for port 1 priority 3 |
| 23:16  | Q2_TX_PSOFF_CNT | PFC TX pause off count for port 1 priority 2 |
| 15:8   | Q1_TX_PSOFF_CNT | PFC TX pause off count for port 1 priority 1 |
| 7:0    | Q0_TX_PSOFF_CNT | PFC TX pause off count for port 1 priority 0 |

1511013C **MAC\_P1\_PFC\_TX\_PSOFF\_CNT** Port 1 TX PFC pause off counter for high priority 00000000  
H

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | Q7_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q6_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q4_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                  |
|--------|-----------------|----------------------------------------------|
| 31:24  | Q7_TX_PSOFF_CNT | PFC TX pause off count for port 1 priority 7 |
| 23:16  | Q6_TX_PSOFF_CNT | PFC TX pause off count for port 1 priority 6 |
| 15:8   | Q5_TX_PSOFF_CNT | PFC TX pause off count for port 1 priority 5 |
| 7:0    | Q4_TX_PSOFF_CNT | PFC TX pause off count for port 1 priority 4 |

**15110200      MAC\_P2\_MCR      Port 2 MAC control      20006300**

| Bit   | 31           | 30        | 29        | 28              | 27                          | 26           | 25             | 24         | 23          | 22           | 21          | 20          | 19        | 18 | 17        | 16                |
|-------|--------------|-----------|-----------|-----------------|-----------------------------|--------------|----------------|------------|-------------|--------------|-------------|-------------|-----------|----|-----------|-------------------|
| Name  | MAX_RX_JUMBO |           |           |                 | RESV0                       |              | MAC_RX_PKT_LEN |            | MTCC_LMT    |              |             |             | IPG_CFG   |    | RESV1     | DIFF_RX_FIFO_WCLR |
| Type  | RW           |           |           |                 | RW                          |              | RW             |            | RW          |              |             |             | RW        |    | RW        | RW                |
| Reset | 0            | 0         | 1         | 0               | 0                           | 0            | 0              | 0          | 0           | 0            | 0           | 0           | 0         | 0  | 0         | 0                 |
| Bit   | 15           | 14        | 13        | 12              | 11                          | 10           | 9              | 8          | 7           | 6            | 5           | 4           | 3         | 2  | 1         | 0                 |
| Name  | FORCE_MOD_E  | MAC_TX_EN | MAC_RX_EN | DEL_RX_FIFO_CLR | GMAC_RDMA_HANG_ECO_ROLLBACK | PRMBL_LMT_EN | BKOFF_EN       | BACKP_R_EN | FORCE_EEE1G | FORCE_EEE100 | FORCE_RX_FC | FORCE_TX_FC | FORCE_SPD |    | FORCE_DPX | FORCE_LINK        |
| Type  | RW           | RW        | RW        | RW              | RW                          | RW           | RW             | RW         | RW          | RW           | RW          | RW          | RW        |    | RW        | RW                |
| Reset | 0            | 1         | 1         | 0               | 0                           | 0            | 1              | 1          | 0           | 0            | 0           | 0           | 0         | 0  | 0         | 0                 |

| Bit(s) | Name           | Description                                                                                                                                                                                                                                                                                                               |
|--------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | MAX_RX_JUMBO   | <b>Maximum received jumbo packet length</b><br><br>4'h0, 4'h1: Reserved<br><br>4'h2: 2 Kbytes (maxi. length on FE/GDM)<br><br>4'h3 ... 4'hF: Reserved                                                                                                                                                                     |
| 27:26  | RESV0          | <b>Reserved</b>                                                                                                                                                                                                                                                                                                           |
| 25:24  | MAC_RX_PKT_LEN | <b>Maximum received packet length</b><br><br>Sets the maximum length of ingress packets including CRC that can be received by MAC.<br><br>2'b00: 1518 bytes for untagged frames;1522 bytes for tagged frames<br><br>2'b01: 1536 bytes<br><br>2'b10: 1552 bytes<br><br>2'b11: MAX_RX_JUMBO                                 |
| 23:20  | MTCC_LMT       | <b>MTCC limit</b><br><br>Maximum transmit collision count limitation.<br><br>0: Disable TX collision abort function, and send packet until success<br><br>1 ~ 15: Maximum transmit collision count                                                                                                                        |
| 19:18  | IPG_CFG        | <b>Inter-frame gap shrink</b><br><br>2'b00: Normal 96-bit IFG<br><br>2'b01: Transmit 96-bit IFG with short IFG in random behavior.<br><br>2'b10: Shrink 64-bit IFG<br><br>2'b11: When any output queue inside the port is congested, shrink 64-bit IFG will be enabled; otherwise, normal 96-bit IFG will be the default. |
| 17     | RESV1          | <b>Reserved</b>                                                                                                                                                                                                                                                                                                           |

| Bit(s) | Name                        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--------|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16     | DIFF_RXFIFO_WCLR            | <b>Change RX FIFO wclear function</b><br>0: Remain RX FIFO wclear function<br>1: Change RX FIFO wclear function                                                                                                                                                                                                                                                                                                                             |
| 15     | FORCE_MODE                  | <b>Force MAC mode</b><br>0: Force mode off (MAC status is decided by PHY auto-polling)<br>1: Force mode on (MAC status is determined by FORCE_XXX register)                                                                                                                                                                                                                                                                                 |
| 14     | MAC_TX_EN                   | <b>TX MAC enable</b><br>0: TX MAC function is disabled<br>1: TX MAC function is enabled                                                                                                                                                                                                                                                                                                                                                     |
| 13     | MAC_RX_EN                   | <b>RX MAC enable</b><br>0: RX MAC function is disabled<br>1: RX MAC function is enabled                                                                                                                                                                                                                                                                                                                                                     |
| 12     | DEL_RXFIFO_CLR              | <b>Disables RX FIFO clear function</b><br>0: Remain RX FIFO clear function<br>1: Broke RX FIFO clear function                                                                                                                                                                                                                                                                                                                               |
| 11     | GMAC_RDMA_HANG_ECO_ROLLBACK | <b>Rollback ECO for GMAC RDMA hang issue</b><br>0: ECO is enabled<br>1: Rollback ECO                                                                                                                                                                                                                                                                                                                                                        |
| 10     | PRMBL_LMT_EN                | <b>Preamble limit enable</b><br>0: RXMAC can recognize the Start Frame Delimiter (SFD), without needing to receive a byte with the value of 55 in the preamble.<br>1: RXMAC will recognize the SFD before the next new frame when it receives the 7 consecutive bytes with the value of 55 within the 8-byte Preamble. If SFD (8'hd5) shows up after the 8-byte Preamble, RXMAC will not recognize it and treat it as if there were no SFD. |
| 9      | BKOFF_EN                    | <b>Back-off enable</b><br>0: Disabled<br>1: Let MAC follow the back-off mechanism when collision happens                                                                                                                                                                                                                                                                                                                                    |
| 8      | BACKPR_EN                   | <b>Back-Pressure enable</b><br>0: Disabled<br>1: Enable back-pressure mechanism when operating in half-duplex mode and flow-control is on                                                                                                                                                                                                                                                                                                   |
| 7      | FORCE_EEE1G                 | <b>Force LPI mode for 1000m link speed</b><br>When (FORCE_MODE= 1), these bits are used to control MAC EEE mode                                                                                                                                                                                                                                                                                                                             |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                     |
|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 0: Do not have the ability of entering EEE low power idle mode for 1000m link speed<br>1: Have the ability of entering EEE low power idle mode                                                                                                                  |
| 6      | FORCE_EEE100 | <b>Force LPI mode for 100m link speed</b><br>When (FORCE_MODE= 1), these bits are used to control MAC EEE mode<br>0: Do not have the ability of entering EEE low power idle mode for 100m link speed<br>1: Have the ability of entering EEE low power idle mode |
| 5      | FORCE_RX_FC  | <b>Force RX flow control</b><br>When (FORCE_MODE= 1), these bits are used to control MAC RX flow control<br>0: Disable<br>1: Let MAC accept the pause frame when operating in full-duplex mode and flow-control is on                                           |
| 4      | FORCE_TX_FC  | <b>Force TX flow control</b><br>When (FORCE_MODE= 1), these bits are used to control MAC TX flow control<br>0: Disable<br>1: Let MAC transmit the pause frame when operating in full-duplex mode and flow-control is on                                         |
| 3:2    | FORCE_SPD    | <b>Force link speed</b><br>When (FORCE_MODE= 1), these bits are used to control MAC link speed<br>2'b00: 10 Mbps<br>2'b01: 100 Mbps<br>2'b10: 1000 Mbps<br>2'b11: reserved                                                                                      |
| 1      | FORCE_DPX    | <b>Force duplex</b><br>When (FORCE_MODE= 1), these bits are used to control MAC link duplex<br>0: Half-duplex<br>1: Full-duplex                                                                                                                                 |
| 0      | FORCE_LINK   | <b>Force link state</b><br>When (FORCE_MODE= 1), these bits are used to control MAC link state<br>0: Link down<br>1: Link up                                                                                                                                    |

15110204      **MAC\_P2\_EEE**      Port 2 EEE control      00000002

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19         | 18        | 17 | 16       |
|-------|------------------|----|----|----|----|----|----|----|-----------------|----|----|----|------------|-----------|----|----------|
| Name  | WAKEUP_TIME_1000 |    |    |    |    |    |    |    | WAKEUP_TIME_100 |    |    |    |            |           |    |          |
| Type  | RW               |    |    |    |    |    |    |    | RW              |    |    |    |            |           |    |          |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0          | 0         | 0  | 0        |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3          | 2         | 1  | 0        |
| Name  | LPI_TXIDLE_THD   |    |    |    |    |    |    |    | RESV0           |    |    |    | CKG_TXIDLE | CKG_RXLPI |    | LPI_MODE |
| Type  | RW               |    |    |    |    |    |    |    | RW              |    |    |    | RW         | RW        |    | RW       |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0          | 0         |    | 0        |

| Bit(s) | Name             | Description                                                                                                                                                                                                                                        |
|--------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | WAKEUP_TIME_1000 | <b>Wake up time for 1000-Mbps LPI mode</b><br><br>The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packet after wake-up<br><br>Time unit: 1us                                                         |
| 23:16  | WAKEUP_TIME_100  | <b>Wake up time for 100-Mbps LPI mode</b><br><br>The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packet after wake-up<br><br>Time unit: 1us                                                          |
| 15:8   | LPI_TXIDLE_THD   | <b>TX IDLE timer to enter LPI mode</b><br><br>When there is no packet to be transmitted and LPI_TXIDLE_THD is exceeded, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI signal to link partner<br><br>Time unit: 1ms |
| 7:4    | RESV0            | <b>Reserved</b>                                                                                                                                                                                                                                    |
| 3      | CKG_TXIDLE       | <b>TX clock power down</b><br><br>0: Disable<br><br>1: Stop TX clock when the corresponding port has no traffic to send and has entered IDLE state for <LPI_TXIDLE_THD> ms.                                                                        |
| 2      | CKG_RXLPI        | <b>RX clock power down</b><br><br>0: Disable<br><br>1: Stop RX clock ticking when the corresponding port entering the LPI mode and IDLE state.                                                                                                     |
| 0      | LPI_MODE         | <b>LPI mode activated</b><br><br>0: Disable<br><br>1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner                                                                                                         |

15110208      **MAC P2\_SR**      Port 2 MAC status      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23           | 22            | 21           | 20           | 19         | 18 | 17         | 16          |
|-------|-------|----|----|----|----|----|----|----|--------------|---------------|--------------|--------------|------------|----|------------|-------------|
| Name  | RESV0 |    |    |    |    |    |    |    |              |               |              |              |            |    |            |             |
| Type  | RO    |    |    |    |    |    |    |    |              |               |              |              |            |    |            |             |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0            | 0             | 0            | 0            | 0          | 0  | 0          | 0           |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7            | 6             | 5            | 4            | 3          | 2  | 1          | 0           |
| Name  | RESV0 |    |    |    |    |    |    |    | EEE1G_STATUS | EEE100_STATUS | RX_FC_STATUS | TX_FC_STATUS | SPD_STATUS |    | DPX_STATUS | LINK_STATUS |
| Type  | RO    |    |    |    |    |    |    |    | RO           | RO            | RO           | RO           | RO         |    | RO         | RO          |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0            | 0             | 0            | 0            | 0          | 0  | 0          | 0           |

| Bit(s) | Name          | Description                                                                                                                                                                                    |
|--------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8   | RESV0         | <b>Reserved</b>                                                                                                                                                                                |
| 7      | EEE1G_STATUS  | <b>LPI mode for 1000m link speed</b><br><br>0: Do not have the ability of entering EEE low power idle mode for 1000m link speed<br><br>1: Have the ability of entering EEE low power idle mode |
| 6      | EEE100_STATUS | <b>LPI mode for 100m link speed</b><br><br>0: Do not have the ability of entering EEE low power idle mode for 100m link speed<br><br>1: Have the ability of entering EEE low power idle mode   |
| 5      | RX_FC_STATUS  | <b>RX flow control status</b><br><br>0: Disable<br><br>1: Let MAC accept the pause frame when operating in full-duplex mode and flow-control is on                                             |
| 4      | TX_FC_STATUS  | <b>TX flow control status</b><br><br>0: Disable<br><br>1: Let MAC transmit the pause frame when operating in full-duplex mode and flow-control is on                                           |
| 3:2    | SPD_STATUS    | <b>Link speed status</b><br><br>2'b00: 10 Mbps<br><br>2'b01: 100 Mbps<br><br>2'b10: 1000 Mbps<br><br>2'b11: reserved                                                                           |
| 1      | DPX_STATUS    | <b>Duplex status</b><br><br>0: Half-duplex<br><br>1: Full-duplex                                                                                                                               |
| 0      | LINK_STATUS   | <b>Link state</b>                                                                                                                                                                              |



| Bit(s) | Name | Description  |
|--------|------|--------------|
|        |      | 0: Link down |
|        |      | 1: Link up   |

15110210      **MAC P2\_WOL**      **Port 2 WOL**      00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19      | 18      | 17          | 16      |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|---------|---------|-------------|---------|
| Name  | WOL_DBG |    |    |    |    |    |    |    |    |    |    |    |         |         | WOL_INT_STS | WOL_STS |
| Type  | RO      |    |    |    |    |    |    |    |    |    |    |    |         |         | W1C         | RO      |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       | 0       | 0           | 0       |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3       | 2       | 1           | 0       |
| Name  | RESV0   |    |    |    |    |    |    |    |    |    |    |    | SNP_PKT | CRC_DIS | WOL_INT_EN  | WOL_EN  |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    | RW      | RW      | RW          | RW      |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0       | 0       | 0           | 0       |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                  |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:18  | WOL_DBG     | <b>GMAC2 Wake-on-LAN debug signals</b>                                                                                                                                                                                                                                       |
| 17     | WOL_INT_STS | <b>GMAC2 Wake-on-LAN interrupt status</b>                                                                                                                                                                                                                                    |
| 16     | WOL_STS     | <b>GMAC2 Wake-on-LAN status</b><br><br>If WOL is enabled, this bit will change from 0 to 1 when GMAC RX state machine enters IDLE state. It indicates GMAC will drop all packets and detect magic packet.<br><br>0: Normal state<br><br>1: Listen state. Detect magic packet |
| 15:4   | RESV0       | <b>Reserved</b>                                                                                                                                                                                                                                                              |
| 3      | SNP_PKT     | <b>GMAC2 Wake-on-LAN with snoopy packet</b>                                                                                                                                                                                                                                  |
| 2      | CRC_DIS     | <b>GMAC2 Wake-on-LAN with CRC Check disable</b>                                                                                                                                                                                                                              |
| 1      | WOL_INT_EN  | <b>GMAC2 Wake-on-LAN Interrupt enable</b>                                                                                                                                                                                                                                    |
| 0      | WOL_EN      | <b>GMAC2 Wake-on-LAN Function enable</b>                                                                                                                                                                                                                                     |

15110214      **MAC P2 SGMII**      Port 2 SGMII      050B0001

| Bit   | 31                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16            |
|-------|-----------------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|---------------|
| Name  | LOADPSTMR_EXTEND_TIME |    |    |    |    |    |    |    | SYNCDONE_TIME |    |    |    |    |    |    |               |
| Type  | RW                    |    |    |    |    |    |    |    | RW            |    |    |    |    |    |    |               |
| Reset | 0                     | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0             | 0  | 0  | 0  | 1  | 0  | 1  | 1             |
| Bit   | 15                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0             |
| Name  |                       |    |    |    |    |    |    |    |               |    |    |    |    |    |    | DIS_TXCLK_ENA |
| Type  |                       |    |    |    |    |    |    |    |               |    |    |    |    |    |    | RW            |
| Reset |                       |    |    |    |    |    |    |    |               |    |    |    |    |    |    | 1             |

| Bit(s) | Name                  | Description                                                                                                        |
|--------|-----------------------|--------------------------------------------------------------------------------------------------------------------|
| 31:24  | LOADPSTMR_EXTEND_TIME | <b>rx_loadpstmr extend time in SGMII mode</b>                                                                      |
| 23:16  | SYNCDONE_TIME         | <b>Sync done time for RX flow control in SGMII mode</b>                                                            |
| 0      | DIS_TXCLK_ENA         | <b>Disables txclk_ena in SGMII mode</b><br><br>0: SGMII txclk_ena is enabled<br><br>1: SGMII txclk_ena is disabled |

15110218      **MAC P2\_PFC\_CTRL**      Port 2 PFC control      00000000

| Bit          | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19                | 18          | 17         | 16 |
|--------------|------|----|----|----|----|----|----|----|----|----|----|----|-------------------|-------------|------------|----|
| <b>Name</b>  | RESV |    |    |    |    |    |    |    |    |    |    |    |                   |             |            |    |
| <b>Type</b>  | RW   |    |    |    |    |    |    |    |    |    |    |    |                   |             |            |    |
| <b>Reset</b> | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0           | 0          | 0  |
| Bit          | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3                 | 2           | 1          | 0  |
| <b>Name</b>  | RESV |    |    |    |    |    |    |    |    |    |    |    | PFC_AUTO_SYNC_DLY | PFC_SYNC_EN | PFC_ENABLE |    |
| <b>Type</b>  | RW   |    |    |    |    |    |    |    |    |    |    |    | RW                | RW          | RW         |    |
| <b>Reset</b> | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0           | 0          | 0  |

| Bit(s) | Name              | Description                                                                                                                            |
|--------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:4   | RESV              | <b>Reserved</b>                                                                                                                        |
| 3:2    | PFC_AUTO_SYNC_DLY | <b>Selects the delay of sending PFC auto sync packet</b><br><br>0: Delay 0s<br><br>1: Delay 0.5s<br><br>2: Delay 1s<br><br>3: Delay 2s |
| 1      | PFC_SYNC_EN       | <b>Enables PFC auto-sync ability</b><br><br>0: Disable<br><br>1: Enable                                                                |
| 0      | PFC_EN            | <b>Enables PFC ability</b><br><br>0: Disable<br><br>1: Enable                                                                          |

**1511021C      MAC\_P2\_PFC\_STS      Port 2 PFC status      00000000**

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16          |
|-------|------------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|-------------|
| Name  | RESV       |    |    |    |    |    |    |    |            |    |    |    |    |    |    | PFC_AUTO_EN |
| Type  | RO         |    |    |    |    |    |    |    |            |    |    |    |    |    |    | RO          |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0           |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0           |
| Name  | TX_PFC_STS |    |    |    |    |    |    |    | RX_PFC_STS |    |    |    |    |    |    |             |
| Type  | RO         |    |    |    |    |    |    |    | RO         |    |    |    |    |    |    |             |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0           |

| Bit(s) | Name        | Description                                       |
|--------|-------------|---------------------------------------------------|
| 31:17  | RESV        | Reserved                                          |
| 16     | PFC_AUTO_EN | PFC auto enable status<br>0: Disable<br>1: Enable |
| 15:8   | TX_PFC_STS  | TX PFC status                                     |
| 7:0    | RX_PFC_STS  | RX PFC status                                     |

**15110220      MAC\_P2\_PFC\_RX\_PSON\_CNT      Port 2 RX PFC pause on counter for low priority      00000000**
L

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  | Q3_RX_PSON_CNT |    |    |    |    |    |    |    | Q2_RX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q1_RX_PSON_CNT |    |    |    |    |    |    |    | Q0_RX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                 |
|--------|----------------|---------------------------------------------|
| 31:24  | Q3_RX_PSON_CNT | PFC RX pause on count for port 2 priority 3 |
| 23:16  | Q2_RX_PSON_CNT | PFC RX pause on count for port 2 priority 2 |
| 15:8   | Q1_RX_PSON_CNT | PFC RX pause on count for port 2 priority 1 |
| 7:0    | Q0_RX_PSON_CNT | PFC RX pause on count for port 2 priority 0 |

15110224 MAC P2\_PFC\_RX\_PSON\_CNT Port 2 RX PFC pause on counter for high priority

00000000

H

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  | Q7_RX_PSON_CNT |    |    |    |    |    |    |    | Q6_RX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_RX_PSON_CNT |    |    |    |    |    |    |    | Q4_RX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                 |
|--------|----------------|---------------------------------------------|
| 31:24  | Q7_RX_PSON_CNT | PFC RX pause on count for port 2 priority 7 |
| 23:16  | Q6_RX_PSON_CNT | PFC RX pause on count for port 2 priority 6 |
| 15:8   | Q5_RX_PSON_CNT | PFC RX pause on count for port 2 priority 5 |
| 7:0    | Q4_RX_PSON_CNT | PFC RX pause on count for port 2 priority 4 |

15110228 MAC P2\_PFC\_RX\_PSOFF\_CNT Port 2 RX PFC pause off counter for low priority

00000000

L

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | Q3_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q2_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q1_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q0_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                  |
|--------|-----------------|----------------------------------------------|
| 31:24  | Q3_RX_PSOFF_CNT | PFC RX pause off count for port 2 priority 3 |
| 23:16  | Q2_RX_PSOFF_CNT | PFC RX pause off count for port 2 priority 2 |
| 15:8   | Q1_RX_PSOFF_CNT | PFC RX pause off count for port 2 priority 1 |
| 7:0    | Q0_RX_PSOFF_CNT | PFC RX pause off count for port 2 priority 0 |

1511022C **MAC P2\_PFC\_RX\_PSOFF\_CNT** Port 2 RX PFC pause off counter for high priority 00000000H

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | Q7_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q6_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q4_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                  |
|--------|-----------------|----------------------------------------------|
| 31:24  | Q7_RX_PSOFF_CNT | PFC RX pause off count for port 2 priority 7 |
| 23:16  | Q6_RX_PSOFF_CNT | PFC RX pause off count for port 2 priority 6 |
| 15:8   | Q5_RX_PSOFF_CNT | PFC RX pause off count for port 2 priority 5 |
| 7:0    | Q4_RX_PSOFF_CNT | PFC RX pause off count for port 2 priority 4 |

15110230 **MAC P2\_PFC\_TX\_PSON\_CNT** Port 2 TX PFC pause on counter for low priority 00000000L

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  | Q3_TX_PSON_CNT |    |    |    |    |    |    |    | Q2_TX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q1_TX_PSON_CNT |    |    |    |    |    |    |    | Q0_TX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                 |
|--------|----------------|---------------------------------------------|
| 31:24  | Q3_TX_PSON_CNT | PFC TX pause on count for port 2 priority 3 |
| 23:16  | Q2_TX_PSON_CNT | PFC TX pause on count for port 2 priority 2 |
| 15:8   | Q1_TX_PSON_CNT | PFC TX pause on count for port 2 priority 1 |
| 7:0    | Q0_TX_PSON_CNT | PFC TX pause on count for port 2 priority 0 |

15110234 MAC P2\_PFC\_TX\_PSON\_CNT Port 2 TX PFC pause on counter for high priority

00000000

H

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  | Q7_TX_PSON_CNT |    |    |    |    |    |    |    | Q6_TX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_TX_PSON_CNT |    |    |    |    |    |    |    | Q4_TX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                 |
|--------|----------------|---------------------------------------------|
| 31:24  | Q7_TX_PSON_CNT | PFC TX pause on count for port 2 priority 7 |
| 23:16  | Q6_TX_PSON_CNT | PFC TX pause on count for port 2 priority 6 |
| 15:8   | Q5_TX_PSON_CNT | PFC TX pause on count for port 2 priority 5 |
| 7:0    | Q4_TX_PSON_CNT | PFC TX pause on count for port 2 priority 4 |

15110238 MAC P2\_PFC\_TX\_PSOFF\_CNT Port 2 TX PFC pause off counter for low priority

00000000

L

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | Q3_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q2_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q1_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q0_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                  |
|--------|-----------------|----------------------------------------------|
| 31:24  | Q3_TX_PSOFF_CNT | PFC TX pause off count for port 2 priority 3 |
| 23:16  | Q2_TX_PSOFF_CNT | PFC TX pause off count for port 2 priority 2 |
| 15:8   | Q1_TX_PSOFF_CNT | PFC TX pause off count for port 2 priority 1 |
| 7:0    | Q0_TX_PSOFF_CNT | PFC TX pause off count for port 2 priority 0 |

1511023C **MAC\_P2\_PFC\_TX\_PSOFF\_CNT** Port 2 TX PFC pause off counter for high priority 00000000H

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | Q7_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q6_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q4_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                  |
|--------|-----------------|----------------------------------------------|
| 31:24  | Q7_TX_PSOFF_CNT | PFC TX pause off count for port 2 priority 7 |
| 23:16  | Q6_TX_PSOFF_CNT | PFC TX pause off count for port 2 priority 6 |
| 15:8   | Q5_TX_PSOFF_CNT | PFC TX pause off count for port 2 priority 5 |
| 7:0    | Q4_TX_PSOFF_CNT | PFC TX pause off count for port 2 priority 4 |



15110300      **MAC\_P3\_MCR**      Port 3 MAC control      20006300

| Bit   | 31           | 30        | 29        | 28              | 27                          | 26           | 25             | 24         | 23          | 22           | 21          | 20          | 19        | 18 | 17        | 16                |
|-------|--------------|-----------|-----------|-----------------|-----------------------------|--------------|----------------|------------|-------------|--------------|-------------|-------------|-----------|----|-----------|-------------------|
| Name  | MAX_RX_JUMBO |           |           |                 | RESV0                       |              | MAC_RX_PKT_LEN |            | MTCC_LMT    |              |             |             | IPG_CFG   |    | RESV1     | DIFF_RX_FIFO_WCLR |
| Type  | RW           |           |           |                 | RW                          |              | RW             |            | RW          |              |             |             | RW        |    | RW        | RW                |
| Reset | 0            | 0         | 1         | 0               | 0                           | 0            | 0              | 0          | 0           | 0            | 0           | 0           | 0         | 0  | 0         | 0                 |
| Bit   | 15           | 14        | 13        | 12              | 11                          | 10           | 9              | 8          | 7           | 6            | 5           | 4           | 3         | 2  | 1         | 0                 |
| Name  | FORCE_MOD_E  | MAC_TX_EN | MAC_RX_EN | DEL_RX_FIFO_CLR | GMAC_RDMA_HANG_ECO_ROLLBACK | PRMBL_LMT_EN | BKOFF_EN       | BACKP_R_EN | FORCE_EEE1G | FORCE_EEE100 | FORCE_RX_FC | FORCE_TX_FC | FORCE_SPD |    | FORCE_DPX | FORCE_LINK        |
| Type  | RW           | RW        | RW        | RW              | RW                          | RW           | RW             | RW         | RW          | RW           | RW          | RW          | RW        |    | RW        | RW                |
| Reset | 0            | 1         | 1         | 0               | 0                           | 0            | 1              | 1          | 0           | 0            | 0           | 0           | 0         | 0  | 0         | 0                 |

| Bit(s) | Name           | Description                                                                                                                                                                                                                                                                                                               |
|--------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28  | MAX_RX_JUMBO   | <b>Maximum received jumbo packet length</b><br><br>4'h0, 4'h1: Reserved<br><br>4'h2: 2 Kbytes (maxi. length on FE/GDM)<br><br>4'h3 ... 4'hF: Reserved                                                                                                                                                                     |
| 27:26  | RESV0          | <b>Reserved</b>                                                                                                                                                                                                                                                                                                           |
| 25:24  | MAC_RX_PKT_LEN | <b>Maximum received packet length</b><br><br>Sets the maximum length of ingress packets including CRC that can be received by MAC.<br><br>2'b00: 1518 bytes for untagged frames; 1522 bytes for tagged frames<br><br>2'b01: 1536 bytes<br><br>2'b10: 1552 bytes<br><br>2'b11: MAX_RX_JUMBO                                |
| 23:20  | MTCC_LMT       | <b>MTCC limit</b><br><br>Maximum transmit collision count limitation.<br><br>0: Disable TX collision abort function, and send packet until success<br><br>1 ~ 15: Maximum transmit collision count                                                                                                                        |
| 19:18  | IPG_CFG        | <b>Inter-frame gap shrink</b><br><br>2'b00: Normal 96-bit IFG<br><br>2'b01: Transmit 96-bit IFG with short IFG in random behavior.<br><br>2'b10: Shrink 64-bit IFG<br><br>2'b11: When any output queue inside the port is congested, shrink 64-bit IFG will be enabled; otherwise, normal 96-bit IFG will be the default. |
| 17     | RESV1          | <b>Reserved</b>                                                                                                                                                                                                                                                                                                           |

| Bit(s) | Name                        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--------|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16     | DIFF_RXFIFO_WCLR            | <b>Change RX FIFO wclear function</b><br>0: Remain RX FIFO wclear function<br>1: Change RX FIFO wclear function                                                                                                                                                                                                                                                                                                                             |
| 15     | FORCE_MODE                  | <b>Force MAC mode</b><br>0: Force mode off (MAC status is decided by PHY auto-polling)<br>1: Force mode on (MAC status is determined by FORCE_XXX register)                                                                                                                                                                                                                                                                                 |
| 14     | MAC_TX_EN                   | <b>TX MAC enable</b><br>0: TX MAC function is disabled<br>1: TX MAC function is enabled                                                                                                                                                                                                                                                                                                                                                     |
| 13     | MAC_RX_EN                   | <b>RX MAC enable</b><br>0: RX MAC function is disabled<br>1: RX MAC function is enabled                                                                                                                                                                                                                                                                                                                                                     |
| 12     | DEL_RXFIFO_CLR              | <b>Disables RX FIFO clear function</b><br>0: Remain RX FIFO clear function<br>1: Broke RX FIFO clear function                                                                                                                                                                                                                                                                                                                               |
| 11     | GMAC_RDMA_HANG_ECO_ROLLBACK | <b>Rollback ECO for GMAC RDMA hang issue</b><br>0: ECO is enabled<br>1: Rollback ECO                                                                                                                                                                                                                                                                                                                                                        |
| 10     | PRMBL_LMT_EN                | <b>Preamble limit enable</b><br>0: RXMAC can recognize the Start Frame Delimiter (SFD), without needing to receive a byte with the value of 55 in the preamble.<br>1: RXMAC will recognize the SFD before the next new frame when it receives the 7 consecutive bytes with the value of 55 within the 8-byte Preamble. If SFD (8'hd5) shows up after the 8-byte Preamble, RXMAC will not recognize it and treat it as if there were no SFD. |
| 9      | BKOFF_EN                    | <b>Back-off enable</b><br>0: Disabled<br>1: Let MAC follow the back-off mechanism when collision happens                                                                                                                                                                                                                                                                                                                                    |
| 8      | BACKPR_EN                   | <b>Back-Pressure enable</b><br>0: Disabled<br>1: Enable back-pressure mechanism when operating in half-duplex mode and flow-control is on                                                                                                                                                                                                                                                                                                   |
| 7      | FORCE_EEE1G                 | <b>Force LPI mode for 1000m link speed</b><br>When (FORCE_MODE= 1), these bits are used to control MAC EEE mode                                                                                                                                                                                                                                                                                                                             |

| Bit(s) | Name         | Description                                                                                                                                                                                                                                                     |
|--------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|        |              | 0: Do not have the ability of entering EEE low power idle mode for 1000m link speed<br>1: Have the ability of entering EEE low power idle mode                                                                                                                  |
| 6      | FORCE_EEE100 | <b>Force LPI mode for 100m link speed</b><br>When (FORCE_MODE= 1), these bits are used to control MAC EEE mode<br>0: Do not have the ability of entering EEE low power idle mode for 100m link speed<br>1: Have the ability of entering EEE low power idle mode |
| 5      | FORCE_RX_FC  | <b>Force RX flow control</b><br>When (FORCE_MODE= 1), these bits are used to control MAC RX flow control<br>0: Disable<br>1: Let MAC accept the pause frame when operating in full-duplex mode and flow-control is on                                           |
| 4      | FORCE_TX_FC  | <b>Force TX flow control</b><br>When (FORCE_MODE= 1), these bits are used to control MAC TX flow control<br>0: Disable<br>1: Let MAC transmit the pause frame when operating in full-duplex mode and flow-control is on                                         |
| 3:2    | FORCE_SPD    | <b>Force link speed</b><br>When (FORCE_MODE= 1), these bits are used to control MAC link speed<br>2'b00: 10 Mbps<br>2'b01: 100 Mbps<br>2'b10: 1000 Mbps<br>2'b11: reserved                                                                                      |
| 1      | FORCE_DPX    | <b>Force duplex</b><br>When (FORCE_MODE= 1), these bits are used to control MAC link duplex<br>0: Half-duplex<br>1: Full-duplex                                                                                                                                 |
| 0      | FORCE_LINK   | <b>Force link state</b><br>When (FORCE_MODE= 1), these bits are used to control MAC link state<br>0: Link down<br>1: Link up                                                                                                                                    |

15110304      **MAC\_P3\_EEE**      Port 3 EEE control      00000002

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19         | 18        | 17 | 16       |
|-------|------------------|----|----|----|----|----|----|----|-----------------|----|----|----|------------|-----------|----|----------|
| Name  | WAKEUP_TIME_1000 |    |    |    |    |    |    |    | WAKEUP_TIME_100 |    |    |    |            |           |    |          |
| Type  | RW               |    |    |    |    |    |    |    | RW              |    |    |    |            |           |    |          |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0          | 0         | 0  | 0        |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3          | 2         | 1  | 0        |
| Name  | LPI_TXIDLE_THD   |    |    |    |    |    |    |    | RESV0           |    |    |    | CKG_TXIDLE | CKG_RXLPI |    | LPI_MODE |
| Type  | RW               |    |    |    |    |    |    |    | RW              |    |    |    | RW         | RW        |    | RW       |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0          | 0         |    | 0        |

| Bit(s) | Name             | Description                                                                                                                                                                                                                                        |
|--------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24  | WAKEUP_TIME_1000 | <b>Wake up time for 1000-Mbps LPI mode</b><br><br>The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packet after wake-up<br><br>Time unit: 1us                                                         |
| 23:16  | WAKEUP_TIME_100  | <b>Wake up time for 100-Mbps LPI mode</b><br><br>The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packet after wake-up<br><br>Time unit: 1us                                                          |
| 15:8   | LPI_TXIDLE_THD   | <b>TX IDLE timer to enter LPI mode</b><br><br>When there is no packet to be transmitted and LPI_TXIDLE_THD is exceeded, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI signal to link partner<br><br>Time unit: 1ms |
| 7:4    | RESV0            | <b>Reserved</b>                                                                                                                                                                                                                                    |
| 3      | CKG_TXIDLE       | <b>TX clock power down</b><br><br>0: Disable<br><br>1: Stop TX clock when the corresponding port has no traffic to send and has entered IDLE state for <LPI_TXIDLE_THD> ms.                                                                        |
| 2      | CKG_RXLPI        | <b>RX clock power down</b><br><br>0: Disable<br><br>1: Stop RX clock ticking when the corresponding port entering the LPI mode and IDLE state.                                                                                                     |
| 0      | LPI_MODE         | <b>LPI mode activated</b><br><br>0: Disable<br><br>1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner                                                                                                         |

15110308      **MAC\_P3\_SR**      Port 3 MAC status      00000000

| Bit   | 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23           | 22            | 21           | 20           | 19         | 18 | 17         | 16          |
|-------|-------|----|----|----|----|----|----|----|--------------|---------------|--------------|--------------|------------|----|------------|-------------|
| Name  | RESV0 |    |    |    |    |    |    |    |              |               |              |              |            |    |            |             |
| Type  | RO    |    |    |    |    |    |    |    |              |               |              |              |            |    |            |             |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0            | 0             | 0            | 0            | 0          | 0  | 0          | 0           |
| Bit   | 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7            | 6             | 5            | 4            | 3          | 2  | 1          | 0           |
| Name  | RESV0 |    |    |    |    |    |    |    | EEE1G_STATUS | EEE100_STATUS | RX_FC_STATUS | TX_FC_STATUS | SPD_STATUS |    | DPX_STATUS | LINK_STATUS |
| Type  | RO    |    |    |    |    |    |    |    | RO           | RO            | RO           | RO           | RO         |    | RO         | RO          |
| Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0            | 0             | 0            | 0            | 0          | 0  | 0          | 0           |

| Bit(s) | Name          | Description                                                                                                                                                                                    |
|--------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8   | RESV0         | <b>Reserved</b>                                                                                                                                                                                |
| 7      | EEE1G_STATUS  | <b>LPI mode for 1000m link speed</b><br><br>0: Do not have the ability of entering EEE low power idle mode for 1000m link speed<br><br>1: Have the ability of entering EEE low power idle mode |
| 6      | EEE100_STATUS | <b>LPI mode for 100m link speed</b><br><br>0: Do not have the ability of entering EEE low power idle mode for 100m link speed<br><br>1: Have the ability of entering EEE low power idle mode   |
| 5      | RX_FC_STATUS  | <b>RX flow control status</b><br><br>0: Disable<br><br>1: Let MAC accept the pause frame when operating in full-duplex mode and flow-control is on                                             |
| 4      | TX_FC_STATUS  | <b>TX flow control status</b><br><br>0: Disable<br><br>1: Let MAC transmit the pause frame when operating in full-duplex mode and flow-control is on                                           |
| 3:2    | SPD_STATUS    | <b>Link speed status</b><br><br>2'b00: 10 Mbps<br><br>2'b01: 100 Mbps<br><br>2'b10: 1000 Mbps<br><br>2'b11: reserved                                                                           |
| 1      | DPX_STATUS    | <b>Duplex status</b><br><br>0: Half-duplex<br><br>1: Full-duplex                                                                                                                               |
| 0      | LINK_STATUS   | <b>Link state</b>                                                                                                                                                                              |

| Bit(s) | Name | Description  |
|--------|------|--------------|
|        |      | 0: Link down |
|        |      | 1: Link up   |

15110310 **MAC P3 WOL** Port 3 WOL 00000000

| Bit   | 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19          | 18          | 17              | 16          |
|-------|---------|----|----|----|----|----|----|----|----|----|----|----|-------------|-------------|-----------------|-------------|
| Name  | WOL_DBG |    |    |    |    |    |    |    |    |    |    |    |             |             | WOL_I<br>NT_STS | WOL_S<br>TS |
| Type  | RO      |    |    |    |    |    |    |    |    |    |    |    |             |             | W1C             | RO          |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0           | 0               | 0           |
| Bit   | 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3           | 2           | 1               | 0           |
| Name  | RESV0   |    |    |    |    |    |    |    |    |    |    |    | SNP_P<br>KT | CRC_DI<br>S | WOL_I<br>NT_EN  | WOL_E<br>N  |
| Type  | RW      |    |    |    |    |    |    |    |    |    |    |    | RW          | RW          | RW              | RW          |
| Reset | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0           | 0               | 0           |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                  |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:18  | WOL_DBG     | <b>GMAC1 Wake-on-LAN debug signals</b>                                                                                                                                                                                                                                       |
| 17     | WOL_INT_STS | <b>GMAC1 Wake-on-LAN interrupt status</b>                                                                                                                                                                                                                                    |
| 16     | WOL_STS     | <b>GMAC1 Wake-on-LAN status</b><br><br>If WOL is enabled, this bit will change from 0 to 1 when GMAC RX state machine enters IDLE state. It indicates GMAC will drop all packets and detect magic packet.<br><br>0: Normal state<br><br>1: Listen state. Detect magic packet |
| 15:4   | RESV0       | <b>Reserved</b>                                                                                                                                                                                                                                                              |
| 3      | SNP_PKT     | <b>GMAC1 Wake-on-LAN with snoopy packet</b>                                                                                                                                                                                                                                  |
| 2      | CRC_DIS     | <b>GMAC1 Wake-on-LAN with CRC Check disable</b>                                                                                                                                                                                                                              |
| 1      | WOL_INT_EN  | <b>GMAC1 Wake-on-LAN Interrupt enable</b>                                                                                                                                                                                                                                    |
| 0      | WOL_EN      | <b>GMAC1 Wake-on-LAN Function enable</b>                                                                                                                                                                                                                                     |

15110314      MAC P3 SGMII      Port 3 SGMII      050B0001

| Bit   | 31                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16            |
|-------|-----------------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|---------------|
| Name  | LOADPSTMR_EXTEND_TIME |    |    |    |    |    |    |    | SYNCDONE_TIME |    |    |    |    |    |    |               |
| Type  | RW                    |    |    |    |    |    |    |    | RW            |    |    |    |    |    |    |               |
| Reset | 0                     | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0             | 0  | 0  | 0  | 1  | 0  | 1  | 1             |
| Bit   | 15                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0             |
| Name  |                       |    |    |    |    |    |    |    |               |    |    |    |    |    |    | DIS_TXCLK_ENA |
| Type  |                       |    |    |    |    |    |    |    |               |    |    |    |    |    |    | RW            |
| Reset |                       |    |    |    |    |    |    |    |               |    |    |    |    |    |    | 1             |

| Bit(s) | Name                  | Description                                                                                                        |
|--------|-----------------------|--------------------------------------------------------------------------------------------------------------------|
| 31:24  | LOADPSTMR_EXTEND_TIME | <b>rx_loadpstmr extend time in SGMII mode</b>                                                                      |
| 23:16  | SYNCDONE_TIME         | <b>Sync done time for RX flow control in SGMII mode</b>                                                            |
| 0      | DIS_TXCLK_ENA         | <b>Disables txclk_ena in SGMII mode</b><br><br>0: SGMII txclk_ena is enabled<br><br>1: SGMII txclk_ena is disabled |

15110318      **MAC P3 PFC\_CTRL**      Port 3 PFC control      00000000

| Bit   | 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19                | 18          | 17         | 16 |
|-------|------|----|----|----|----|----|----|----|----|----|----|----|-------------------|-------------|------------|----|
| Name  | RESV |    |    |    |    |    |    |    |    |    |    |    |                   |             |            |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    |                   |             |            |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0           | 0          | 0  |
| Bit   | 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3                 | 2           | 1          | 0  |
| Name  | RESV |    |    |    |    |    |    |    |    |    |    |    | PFC_AUTO_SYNC_DLY | PFC_SYNC_EN | PFC_ENABLE |    |
| Type  | RW   |    |    |    |    |    |    |    |    |    |    |    | RW                | RW          | RW         |    |
| Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | 0           | 0          | 0  |

| Bit(s) | Name              | Description                                                                                                                            |
|--------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:4   | RESV              | Reserved                                                                                                                               |
| 3:2    | PFC_AUTO_SYNC_DLY | <b>Selects the delay of sending PFC auto sync packet</b><br><br>0: Delay 0s<br><br>1: Delay 0.5s<br><br>2: Delay 1s<br><br>3: Delay 2s |
| 1      | PFC_SYNC_EN       | <b>Enables PFC auto-sync ability</b><br><br>0: Disable<br><br>1: Enable                                                                |
| 0      | PFC_EN            | <b>Enables PFC ability</b><br><br>0: Disable<br><br>1: Enable                                                                          |



**1511031C      MAC\_P3\_PFC\_STS      Port 3 PFC status      00000000**

| Bit   | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16          |
|-------|------------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|-------------|
| Name  | RESV       |    |    |    |    |    |    |    |            |    |    |    |    |    |    | PFC_AUTO_EN |
| Type  | RO         |    |    |    |    |    |    |    |            |    |    |    |    |    |    | RO          |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0           |
| Bit   | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0           |
| Name  | TX_PFC_STS |    |    |    |    |    |    |    | RX_PFC_STS |    |    |    |    |    |    |             |
| Type  | RO         |    |    |    |    |    |    |    | RO         |    |    |    |    |    |    |             |
| Reset | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0           |

| Bit(s) | Name        | Description                                               |
|--------|-------------|-----------------------------------------------------------|
| 31:17  | RESV        | Reserved                                                  |
| 16     | PFC_AUTO_EN | PFC auto enable status<br><br>0: Disable<br><br>1: Enable |
| 15:8   | TX_PFC_STS  | TX PFC status                                             |
| 7:0    | RX_PFC_STS  | RX PFC status                                             |

**15110320      MAC\_P3\_PFC\_RX\_PSON\_CNT      Port 3 RX PFC pause on counter for low priority      00000000**
L

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  | Q3_RX_PSON_CNT |    |    |    |    |    |    |    | Q2_RX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q1_RX_PSON_CNT |    |    |    |    |    |    |    | Q0_RX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                 |
|--------|----------------|---------------------------------------------|
| 31:24  | Q3_RX_PSON_CNT | PFC RX pause on count for port 1 priority 3 |
| 23:16  | Q2_RX_PSON_CNT | PFC RX pause on count for port 1 priority 2 |
| 15:8   | Q1_RX_PSON_CNT | PFC RX pause on count for port 1 priority 1 |
| 7:0    | Q0_RX_PSON_CNT | PFC RX pause on count for port 1 priority 0 |

15110324 MAC\_P3\_PFC\_RX\_PSON\_CNT Port 3 RX PFC pause on counter for high priority

00000000

H

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  | Q7_RX_PSON_CNT |    |    |    |    |    |    |    | Q6_RX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_RX_PSON_CNT |    |    |    |    |    |    |    | Q4_RX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                 |
|--------|----------------|---------------------------------------------|
| 31:24  | Q7_RX_PSON_CNT | PFC RX pause on count for port 1 priority 7 |
| 23:16  | Q6_RX_PSON_CNT | PFC RX pause on count for port 1 priority 6 |
| 15:8   | Q5_RX_PSON_CNT | PFC RX pause on count for port 1 priority 5 |
| 7:0    | Q4_RX_PSON_CNT | PFC RX pause on count for port 1 priority 4 |

15110328 MAC\_P3\_PFC\_RX\_PSOFF\_CNT Port 3 RX PFC pause off counter for low priority

00000000

L

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | Q3_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q2_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q1_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q0_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                  |
|--------|-----------------|----------------------------------------------|
| 31:24  | Q3_RX_PSOFF_CNT | PFC RX pause off count for port 1 priority 3 |
| 23:16  | Q2_RX_PSOFF_CNT | PFC RX pause off count for port 1 priority 2 |
| 15:8   | Q1_RX_PSOFF_CNT | PFC RX pause off count for port 1 priority 1 |
| 7:0    | Q0_RX_PSOFF_CNT | PFC RX pause off count for port 1 priority 0 |

1511032C **MAC\_P3\_PFC\_RX\_PSOFF\_CNT** Port 3 RX PFC pause off counter for high priority 00000000H

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | Q7_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q6_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_RX_PSOFF_CNT |    |    |    |    |    |    |    | Q4_RX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                  |
|--------|-----------------|----------------------------------------------|
| 31:24  | Q7_RX_PSOFF_CNT | PFC RX pause off count for port 1 priority 7 |
| 23:16  | Q6_RX_PSOFF_CNT | PFC RX pause off count for port 1 priority 6 |
| 15:8   | Q5_RX_PSOFF_CNT | PFC RX pause off count for port 1 priority 5 |
| 7:0    | Q4_RX_PSOFF_CNT | PFC RX pause off count for port 1 priority 4 |

15110330 **MAC\_P3\_PFC\_TX\_PSON\_CNT** Port 3 TX PFC pause on counter for low priority 00000000L

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  | Q3_TX_PSON_CNT |    |    |    |    |    |    |    | Q2_TX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q1_TX_PSON_CNT |    |    |    |    |    |    |    | Q0_TX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                 |
|--------|----------------|---------------------------------------------|
| 31:24  | Q3_TX_PSON_CNT | PFC TX pause on count for port 1 priority 3 |
| 23:16  | Q2_TX_PSON_CNT | PFC TX pause on count for port 1 priority 2 |
| 15:8   | Q1_TX_PSON_CNT | PFC TX pause on count for port 1 priority 1 |
| 7:0    | Q0_TX_PSON_CNT | PFC TX pause on count for port 1 priority 0 |

15110334 MAC\_P3\_PFC\_TX\_PSON\_CNT Port 3 TX PFC pause on counter for high priority

00000000

H

| Bit   | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| Name  | Q7_TX_PSON_CNT |    |    |    |    |    |    |    | Q6_TX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_TX_PSON_CNT |    |    |    |    |    |    |    | Q4_TX_PSON_CNT |    |    |    |    |    |    |    |
| Type  | RC             |    |    |    |    |    |    |    | RC             |    |    |    |    |    |    |    |
| Reset | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name           | Description                                 |
|--------|----------------|---------------------------------------------|
| 31:24  | Q7_TX_PSON_CNT | PFC TX pause on count for port 1 priority 7 |
| 23:16  | Q6_TX_PSON_CNT | PFC TX pause on count for port 1 priority 6 |
| 15:8   | Q5_TX_PSON_CNT | PFC TX pause on count for port 1 priority 5 |
| 7:0    | Q4_TX_PSON_CNT | PFC TX pause on count for port 1 priority 4 |

15110338 MAC\_P3\_PFC\_TX\_PSOFF\_CNT Port 3 TX PFC pause off counter for low priority

00000000

L

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | Q3_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q2_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q1_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q0_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                  |
|--------|-----------------|----------------------------------------------|
| 31:24  | Q3_TX_PSOFF_CNT | PFC TX pause off count for port 1 priority 3 |
| 23:16  | Q2_TX_PSOFF_CNT | PFC TX pause off count for port 1 priority 2 |
| 15:8   | Q1_TX_PSOFF_CNT | PFC TX pause off count for port 1 priority 1 |
| 7:0    | Q0_TX_PSOFF_CNT | PFC TX pause off count for port 1 priority 0 |

1511033C MAC\_P3\_PFC\_TX\_PSOFF\_CNT Port 3 TX PFC pause off counter for high priority

00000000

H

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| Name  | Q7_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q6_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | Q5_TX_PSOFF_CNT |    |    |    |    |    |    |    | Q4_TX_PSOFF_CNT |    |    |    |    |    |    |    |
| Type  | RC              |    |    |    |    |    |    |    | RC              |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                  |
|--------|-----------------|----------------------------------------------|
| 31:24  | Q7_TX_PSOFF_CNT | PFC TX pause off count for port 1 priority 7 |
| 23:16  | Q6_TX_PSOFF_CNT | PFC TX pause off count for port 1 priority 6 |
| 15:8   | Q5_TX_PSOFF_CNT | PFC TX pause off count for port 1 priority 5 |
| 7:0    | Q4_TX_PSOFF_CNT | PFC TX pause off count for port 1 priority 4 |

15110400 GMAC\_P1\_RX\_UCST\_PKTCTL Port 1 RX unicast packet count low word

00000000

L

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_RX_UCST_PKTCTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_RX_UCST_PKTCTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                      |
|--------|-------------------|----------------------------------|
| 31:0   | P1_RX_UCST_PKTCTL | RX unicast packet count low word |

15110404 **GMAC P1\_RX\_UCST\_PKT CNT** Port 1 RX unicast packet count high word

00000000

H

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_RX_UCST_PKT CNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_RX_UCST_PKT CNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                       |
|--------|---------------------|-----------------------------------|
| 31:0   | P1_RX_UCST_PKT CNTH | RX unicast packet count high word |

15110408 **GMAC P1\_RX\_UCST\_BYTE CNT** Port 1 RX unicast byte count low word

00000000

TL

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_RX_UCST_BYTE CNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_RX_UCST_BYTE CNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                    |
|--------|----------------------|--------------------------------|
| 31:0   | P1_RX_UCST_BYTE CNTL | RX unicast byte count low word |

1511040C **GMAC P1\_RX\_UCST\_BYTECN** Port 1 RX unicast byte count high word

00000000

TH

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_RX_UCST_BYTECNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_RX_UCST_BYTECNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                     |
|--------|---------------------|---------------------------------|
| 31:0   | P1_RX_UCST_BYTECNTH | RX unicast byte count high word |

15110410 **GMAC P1\_RX\_MCST\_PKT CNT** Port 1 RX multicast packet count low word

00000000

L

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_RX_MCST_PKT CNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_RX_MCST_PKT CNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                        |
|--------|---------------------|------------------------------------|
| 31:0   | P1_RX_MCST_PKT CNTL | RX multicast packet count low word |

15110414 GMAC P1\_RX\_MCST\_PKT CNT Port 1 RX multicast packet count high word

00000000

H

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_RX_MCST_PKT CNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_RX_MCST_PKT CNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                         |
|--------|---------------------|-------------------------------------|
| 31:0   | P1_RX_MCST_PKT CNTH | RX multicast packet count high word |

15110418 GMAC P1\_RX\_MCST\_BYTE CNT Port 1 RX multicast byte count low word

00000000

TL

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_RX_MCST_BYTE CNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_RX_MCST_BYTE CNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                      |
|--------|----------------------|----------------------------------|
| 31:0   | P1_RX_MCST_BYTE CNTL | RX multicast byte count low word |



1511041C GMAC P1\_RX\_MCST\_BYTECNTH Port 1 RX multicast byte count high word

00000000

TH

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_RX_MCST_BYTECNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_RX_MCST_BYTECNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                       |
|--------|---------------------|-----------------------------------|
| 31:0   | P1_RX_MCST_BYTECNTH | RX multicast byte count high word |

15110420 GMAC P1\_RX\_BCST\_PKTCTL Port 1 RX broadcast packet count low word

00000000

L

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_RX_BCST_PKTCTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_RX_BCST_PKTCTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                        |
|--------|-------------------|------------------------------------|
| 31:0   | P1_RX_BCST_PKTCTL | RX broadcast packet count low word |

15110424 GMAC P1\_RX\_BCST\_PKT CNT Port 1 RX broadcast packet count high word

00000000

H

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_RX_BCST_PKT CNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_RX_BCST_PKT CNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                         |
|--------|---------------------|-------------------------------------|
| 31:0   | P1_RX_BCST_PKT CNTH | RX broadcast packet count high word |

15110428 GMAC P1\_RX\_BCST\_BYTE CNT Port 1 RX broadcast byte count low word

00000000

TL

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_RX_BCST_BYTE CNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_RX_BCST_BYTE CNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                      |
|--------|----------------------|----------------------------------|
| 31:0   | P1_RX_BCST_BYTE CNTL | RX broadcast byte count low word |

1511042C GMAC P1\_RX\_BCST\_BYTECNTH Port 1 RX broadcast byte count high word  
TH

00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_RX_BCST_BYTECNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_RX_BCST_BYTECNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                       |
|--------|---------------------|-----------------------------------|
| 31:0   | P1_RX_BCST_BYTECNTH | RX broadcast byte count high word |

15110430 GMAC P1\_TX\_UCST\_PKTCNTL Port 1 TX unicast packet count low word  
L

00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_TX_UCST_PKTCNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_TX_UCST_PKTCNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                      |
|--------|--------------------|----------------------------------|
| 31:0   | P1_TX_UCST_PKTCNTL | TX unicast packet count low word |

15110434 GMAC P1\_TX\_UCST\_PKT CNT Port 1 TX unicast packet count high word

00000000

H

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_TX_UCST_PKT CNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_TX_UCST_PKT CNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                       |
|--------|---------------------|-----------------------------------|
| 31:0   | P1_TX_UCST_PKT CNTH | TX unicast packet count high word |

15110438 GMAC P1\_TX\_UCST\_BYTECNTL Port 1 TX unicast byte count low word

00000000

TL

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_TX_UCST_BYTECNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_TX_UCST_BYTECNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                    |
|--------|---------------------|--------------------------------|
| 31:0   | P1_TX_UCST_BYTECNTL | TX unicast byte count low word |

1511043C GMAC P1\_TX\_UCST\_BYTECN Port 1 TX unicast byte count high word

00000000

TH

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_TX_UCST_BYTECNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_TX_UCST_BYTECNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                     |
|--------|---------------------|---------------------------------|
| 31:0   | P1_TX_UCST_BYTECNTH | TX unicast byte count high word |

15110440 GMAC P1\_TX\_MCST\_PKT CNT Port 1 TX multicast packet count low word

00000000

L

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_TX_MCST_PKT CNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_TX_MCST_PKT CNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                        |
|--------|---------------------|------------------------------------|
| 31:0   | P1_TX_MCST_PKT CNTL | TX multicast packet count low word |

15110444 GMAC P1\_TX\_MCST\_PKT CNT Port 1 TX multicast packet count high word

00000000

H

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_TX_MCST_PKT CNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_TX_MCST_PKT CNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                         |
|--------|---------------------|-------------------------------------|
| 31:0   | P1_TX_MCST_PKT CNTH | TX multicast packet count high word |

15110448 GMAC P1\_TX\_MCST\_BYTE CNT Port 1 TX multicast byte count low word

00000000

TL

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_TX_MCST_BYTE CNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_TX_MCST_BYTE CNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                      |
|--------|----------------------|----------------------------------|
| 31:0   | P1_TX_MCST_BYTE CNTL | TX multicast byte count low word |

1511044C **GMAC P1\_TX\_MCST\_BYTECN** Port 1 TX multicast byte count high word 00000000TH

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_TX_MCST_BYTECNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_TX_MCST_BYTECNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                       |
|--------|---------------------|-----------------------------------|
| 31:0   | P1_TX_MCST_BYTECNTH | TX multicast byte count high word |

15110450 **GMAC P1\_TX\_BCST\_PKTCTL** Port 1 TX broadcast packet count low word 00000000

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_TX_BCST_PKTCTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_TX_BCST_PKTCTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                        |
|--------|-------------------|------------------------------------|
| 31:0   | P1_TX_BCST_PKTCTL | TX broadcast packet count low word |

15110454 **GMAC P1\_TX\_BCST\_PKTCTL** Port 1 TX broadcast packet count high word 00000000H

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_TX_BCST_PKTCNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_TX_BCST_PKTCNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                         |
|--------|--------------------|-------------------------------------|
| 31:0   | P1_TX_BCST_PKTCNTH | TX broadcast packet count high word |

15110458 **GMAC P1\_TX\_BCST\_BYTECN** Port 1 TX broadcast byte count low word

00000000

TL

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_TX_BCST_BYTECN TL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_TX_BCST_BYTECN TL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                      |
|--------|----------------------|----------------------------------|
| 31:0   | P1_TX_BCST_BYTECN TL | TX broadcast byte count low word |

1511045C **GMAC P1\_TX\_BCST\_BYTECN** Port 1 TX broadcast byte count high word

00000000

TH

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P1_TX_BCST_BYTECN TH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P1_TX_BCST_BYTECN TH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                       |
|--------|----------------------|-----------------------------------|
| 31:0   | P1_TX_BCST_BYTECN TH | TX broadcast byte count high word |



15110460 GMAC P2\_RX\_UCST\_PKTCTL Port 2 RX unicast packet count low word

00000000

L

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_RX_UCST_PKTCTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_RX_UCST_PKTCTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                      |
|--------|-------------------|----------------------------------|
| 31:0   | P2_RX_UCST_PKTCTL | RX unicast packet count low word |

15110464 GMAC P2\_RX\_UCST\_PKTCH Port 2 RX unicast packet count high word

00000000

H

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_RX_UCST_PKTCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_RX_UCST_PKTCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                       |
|--------|------------------|-----------------------------------|
| 31:0   | P2_RX_UCST_PKTCH | RX unicast packet count high word |

15110468 **GMAC P2\_RX\_UCST\_BYTECN** Port 2 RX unicast byte count low word

00000000

TL

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_RX_UCST_BYTECN TL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_RX_UCST_BYTECN TL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                    |
|--------|----------------------|--------------------------------|
| 31:0   | P2_RX_UCST_BYTECN TL | RX unicast byte count low word |

1511046C **GMAC P2\_RX\_UCST\_BYTECN** Port 2 RX unicast byte count high word

00000000

TH

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_RX_UCST_BYTECN TH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_RX_UCST_BYTECN TH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                     |
|--------|----------------------|---------------------------------|
| 31:0   | P2_RX_UCST_BYTECN TH | RX unicast byte count high word |

15110470 GMAC P2\_RX\_MCST\_PKTCTL Port 2 RX multicast packet count low word

00000000

L

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_RX_MCST_PKTCTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_RX_MCST_PKTCTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                        |
|--------|-------------------|------------------------------------|
| 31:0   | P2_RX_MCST_PKTCTL | RX multicast packet count low word |

15110474 GMAC P2\_RX\_MCST\_PKTCH Port 2 RX multicast packet count high word

00000000

H

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_RX_MCST_PKTCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_RX_MCST_PKTCH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                         |
|--------|------------------|-------------------------------------|
| 31:0   | P2_RX_MCST_PKTCH | RX multicast packet count high word |

15110478 **GMAC P2\_RX\_MCST\_BYTECN**Port 2 RX multicast byte count low word 00000000  
TL

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_RX_MCST_BYTECN TL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_RX_MCST_BYTECN TL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                      |
|--------|----------------------|----------------------------------|
| 31:0   | P2_RX_MCST_BYTECN TL | RX multicast byte count low word |

1511047C **GMAC P2\_RX\_MCST\_BYTECN**Port 2 RX multicast byte count high word 00000000  
TH

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_RX_MCST_BYTECN TH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_RX_MCST_BYTECN TH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                       |
|--------|----------------------|-----------------------------------|
| 31:0   | P2_RX_MCST_BYTECN TH | RX multicast byte count high word |

15110480 GMAC P2\_RX\_BCST\_PKT CNT Port 2 RX broadcast packet count low word

00000000

L

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_RX_BCST_PKT CNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_RX_BCST_PKT CNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                        |
|--------|---------------------|------------------------------------|
| 31:0   | P2_RX_BCST_PKT CNTL | RX broadcast packet count low word |

15110484 GMAC P2\_RX\_BCST\_PKT CNT Port 2 RX broadcast packet count high word

00000000

H

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_RX_BCST_PKT CNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_RX_BCST_PKT CNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                         |
|--------|---------------------|-------------------------------------|
| 31:0   | P2_RX_BCST_PKT CNTH | RX broadcast packet count high word |

15110488 GMAC P2\_RX\_BCST\_BYTECN Port 2 RX broadcast byte count low word

00000000

TL

| Bit   | 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_RX_BCST_BYTECN <sub>TL</sub> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_RX_BCST_BYTECN <sub>TL</sub> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                            | Description                      |
|--------|---------------------------------|----------------------------------|
| 31:0   | P2_RX_BCST_BYTECN <sub>TL</sub> | RX broadcast byte count low word |

1511048C GMAC P2\_RX\_BCST\_BYTECN Port 2 RX broadcast byte count high word

00000000

TH

| Bit   | 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_RX_BCST_BYTECN <sub>TH</sub> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_RX_BCST_BYTECN <sub>TH</sub> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                            | Description                       |
|--------|---------------------------------|-----------------------------------|
| 31:0   | P2_RX_BCST_BYTECN <sub>TH</sub> | RX broadcast byte count high word |

15110490 GMAC P2\_TX\_UCST\_PKT CNT Port 2 TX unicast packet count low word

00000000

L

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_TX_UCST_PKT CNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_TX_UCST_PKT CNTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                      |
|--------|---------------------|----------------------------------|
| 31:0   | P2_TX_UCST_PKT CNTL | TX unicast packet count low word |

15110494 GMAC P2\_TX\_UCST\_PKT CNT Port 2 TX unicast packet count high word

00000000

H

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_TX_UCST_PKT CNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_TX_UCST_PKT CNTH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                       |
|--------|---------------------|-----------------------------------|
| 31:0   | P2_TX_UCST_PKT CNTH | TX unicast packet count high word |

15110498 GMAC P2\_TX\_UCST\_BYTECN Port 2 TX unicast byte count low word

00000000

TL

| Bit   | 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_TX_UCST_BYTECN <sub>TL</sub> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_TX_UCST_BYTECN <sub>TL</sub> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                            | Description                    |
|--------|---------------------------------|--------------------------------|
| 31:0   | P2_TX_UCST_BYTECN <sub>TL</sub> | TX unicast byte count low word |

1511049C GMAC P2\_TX\_UCST\_BYTECN Port 2 TX unicast byte count high word

00000000

TH

| Bit   | 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_TX_UCST_BYTECN <sub>TH</sub> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_TX_UCST_BYTECN <sub>TH</sub> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                            | Description                     |
|--------|---------------------------------|---------------------------------|
| 31:0   | P2_TX_UCST_BYTECN <sub>TH</sub> | TX unicast byte count high word |



151104A0 GMAC P2\_TX\_MCST\_PKTCTL Port 2 TX multicast packet count low word

00000000

L

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_TX_MCST_PKTCTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_TX_MCST_PKTCTL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                        |
|--------|-------------------|------------------------------------|
| 31:0   | P2_TX_MCST_PKTCTL | TX multicast packet count low word |

151104A4 GMAC P2\_TX\_MCST\_PKTCTL Port 2 TX multicast packet count high word

00000000

H

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_TX_MCST_PKTCTLH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_TX_MCST_PKTCTLH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                         |
|--------|--------------------|-------------------------------------|
| 31:0   | P2_TX_MCST_PKTCTLH | TX multicast packet count high word |

151104A8 GMAC P2\_TX\_MCST\_BYTECN Port 2 TX multicast byte count low word

00000000

TL

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_TX_MCST_BYTECN TL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_TX_MCST_BYTECN TL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                      |
|--------|----------------------|----------------------------------|
| 31:0   | P2_TX_MCST_BYTECN TL | TX multicast byte count low word |

151104AC GMAC P2\_TX\_MCST\_BYTECN Port 2 TX multicast byte count high word

00000000

TH

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_TX_MCST_BYTECN TH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_TX_MCST_BYTECN TH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                       |
|--------|----------------------|-----------------------------------|
| 31:0   | P2_TX_MCST_BYTECN TH | TX multicast byte count high word |

151104B0 **GMAC P2\_TX\_BCST\_PKTCTRL** Port 2 TX broadcast packet count low word 00000000

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_TX_BCST_PKTCTRL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_TX_BCST_PKTCTRL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                        |
|--------|--------------------|------------------------------------|
| 31:0   | P2_TX_BCST_PKTCTRL | TX broadcast packet count low word |

151104B4 **GMAC P2\_TX\_BCST\_PKTCTRL** Port 2 TX broadcast packet count high word 00000000

H

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_TX_BCST_PKTCTRLH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_TX_BCST_PKTCTRLH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                         |
|--------|---------------------|-------------------------------------|
| 31:0   | P2_TX_BCST_PKTCTRLH | TX broadcast packet count high word |

151104B8 GMAC P2\_TX\_BCST\_BYTECN Port 2 TX broadcast byte count low word

00000000

TL

| Bit   | 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_TX_BCST_BYTECN |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_TX_BCST_BYTECN |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name              | Description                      |
|--------|-------------------|----------------------------------|
| 31:0   | P2_TX_BCST_BYTECN | TX broadcast byte count low word |

151104BC GMAC P2\_TX\_BCST\_BYTECN Port 2 TX broadcast byte count high word

00000000

TH

| Bit   | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | P2_TX_BCST_BYTECNH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | P2_TX_BCST_BYTECNH |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RC                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name               | Description                       |
|--------|--------------------|-----------------------------------|
| 31:0   | P2_TX_BCST_BYTECNH | TX broadcast byte count high word |

## 4.9 XFI MAC

### 4.9.1 Register Definition

Module name: xfimac Base address: (+0x1511\_3000)

| Address  | Name                        | Width | Register Function                             |
|----------|-----------------------------|-------|-----------------------------------------------|
| 15113000 | <u>xfi_glb_cfg</u>          | 32    | XFI global MAC control                        |
| 15113004 | <u>xfi_int_sts</u>          | 32    | XFI interrupt status                          |
| 15113008 | <u>xfi_int_en</u>           | 32    | XFI interrupt enable                          |
| 15113020 | <u>xfi_fc_sts</u>           | 32    | XFI global status                             |
| 15113060 | <u>xfi_macaddrh</u>         | 32    | XFI MAC address high                          |
| 15113064 | <u>xfi_macaddrl</u>         | 32    | XFI MAC address low                           |
| 151130CC | <u>xfi_if_sts</u>           | 32    | XFI interface status                          |
| 151130D0 | <u>xfi_rx_cfg_2</u>         | 32    | XFI RX configuration 2                        |
| 151130D4 | <u>xfi_tx_cfg_2</u>         | 32    | XFI TX configuration 2                        |
| 151130E0 | <u>xfi_rx_sts_2</u>         | 32    | XFI USXGMII channel information               |
| 15113100 | <u>xfi_cnt_ctrl</u>         | 32    | XFI count global control                      |
| 15113104 | <u>xfi_tx_octets_cnt</u>    | 32    | XFI transmit octets counter                   |
| 15113108 | <u>xfi_tx_pkt_cnt</u>       | 32    | XFI transmit packet counter                   |
| 15113150 | <u>xfi_tx_uc_pkt_cnt_l</u>  | 32    | XFI transmit unicast packet counter [31:0]    |
| 15113154 | <u>xfi_tx_uc_pkt_cnt_h</u>  | 32    | XFI transmit unicast packet counter [63:32]   |
| 15113158 | <u>xfi_tx_uc_byte_cnt_l</u> | 32    | XFI transmit unicast byte counter [31:0]      |
| 1511315C | <u>xfi_tx_uc_byte_cnt_h</u> | 32    | XFI transmit unicast byte counter [63:32]     |
| 15113160 | <u>xfi_tx_mc_pkt_cnt_l</u>  | 32    | XFI transmit multicast packet counter [31:0]  |
| 15113164 | <u>xfi_tx_mc_pkt_cnt_h</u>  | 32    | XFI transmit multicast packet counter [63:32] |
| 15113168 | <u>xfi_tx_mc_byte_cnt_l</u> | 32    | XFI transmit multicast byte counter [31:0]    |
| 1511316C | <u>xfi_tx_mc_byte_cnt_h</u> | 32    | XFI transmit multicast byte counter [63:32]   |
| 15113170 | <u>xfi_tx_bc_pkt_cnt_l</u>  | 32    | XFI transmit broadcast packet counter [31:0]  |
| 15113174 | <u>xfi_tx_bc_pkt_cnt_h</u>  | 32    | XFI transmit broadcast packet counter [63:32] |
| 15113178 | <u>xfi_tx_bc_byte_cnt_l</u> | 32    | XFI transmit broadcast byte counter [31:0]    |
| 1511317C | <u>xfi_tx_bc_byte_cnt_h</u> | 32    | XFI transmit broadcast byte counter [63:32]   |
| 15113184 | <u>xfi_rx_octets_cnt</u>    | 32    | XFI receive octets counter                    |
| 15113188 | <u>xfi_rx_pkt_cnt</u>       | 32    | XFI receive packet counter                    |
| 15113190 | <u>xfi_rx_pause_cnt</u>     | 32    | XFI receive pause packet counter              |
| 151131C0 | <u>xfi_rx_uc_pkt_cnt_l</u>  | 32    | XFI receive unicast packet counter [31:0]     |
| 151131C4 | <u>xfi_rx_uc_pkt_cnt_h</u>  | 32    | XFI receive unicast packet counter [63:32]    |
| 151131C8 | <u>xfi_rx_uc_byte_cnt_l</u> | 32    | XFI receive unicast byte counter [31:0]       |
| 151131CC | <u>xfi_rx_uc_byte_cnt_h</u> | 32    | XFI receive unicast byte counter [63:32]      |
| 151131D0 | <u>xfi_rx_mc_pkt_cnt_l</u>  | 32    | XFI receive multicast packet counter [31:0]   |
| 151131D4 | <u>xfi_rx_mc_pkt_cnt_h</u>  | 32    | XFI receive multicast packet counter [63:32]  |
| 151131D8 | <u>xfi_rx_mc_byte_cnt_l</u> | 32    | XFI receive multicast byte counter [31:0]     |
| 151131DC | <u>xfi_rx_mc_byte_cnt_h</u> | 32    | XFI receive multicast byte counter [63:32]    |
| 151131E0 | <u>xfi_rx_bc_pkt_cnt_l</u>  | 32    | XFI receive broadcast packet counter [31:0]   |
| 151131E4 | <u>xfi_rx_bc_pkt_cnt_h</u>  | 32    | XFI receive broadcast packet counter [63:32]  |
| 151131E8 | <u>xfi_rx_bc_byte_cnt_l</u> | 32    | XFI receive broadcast byte counter [31:0]     |
| 151131EC | <u>xfi_rx_bc_byte_cnt_h</u> | 32    | XFI receive broadcast byte counter [63:32]    |

**15113000**      **xfi\_glb\_cfg**      **XFI global MAC control**      **77FE2C00**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26          | 25 | 24 | 23 | 22 | 21          | 20       | 19         | 18         | 17         | 16         |
|-------|----|----|----|----|----|-------------|----|----|----|----|-------------|----------|------------|------------|------------|------------|
| Name  |    |    |    |    |    | rx_frag_len |    |    |    |    | tx_frag_len |          |            |            |            |            |
| Type  |    |    |    |    |    | RW          |    |    |    |    | RW          |          |            |            |            |            |
| Reset |    |    |    |    |    | 1           | 1  | 1  | 1  | 1  | 1           | 1        | 1          | 1          | 1          |            |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10          | 9  | 8  | 7  | 6  | 5           | 4        | 3          | 2          | 1          | 0          |
| Name  |    |    |    |    |    |             |    |    |    |    | tx_fc_en    | rx_fc_en | rxmpi_stop | rxmbi_stop | txmpi_stop | txmbi_stop |
| Type  |    |    |    |    |    |             |    |    |    |    | RW          | RW       | RW         | RW         | RW         | RW         |
| Reset |    |    |    |    |    |             |    |    |    |    | 0           | 0        | 0          | 0          | 0          | 0          |

| Bit(s) | Name        | Description                                                                                                                                                                                                                                                                                                                                                                                                  |
|--------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:22  | rx_frag_len | <b>Fragment length when transferred from xfi_mac to FE, rx_frag_len[4:0]:</b><br><br>0-2: 64 bytes<br><br>3-30: rx_frag_len * 32 (bytes)<br><br>31: rx_frag_len = 0, no fragment                                                                                                                                                                                                                             |
| 21:17  | tx_frag_len | <b>Fragment length when transferred from FE to xfi_mac, tx_frag_len[4:0]:</b><br><br>0-2: 64 bytes<br><br>3-30: tx_frag_len * 32 (bytes)<br><br>31: tx_frag_len = 0, no fragment;<br><br>Recommended value: 4 to 26<br><br>This register should be used with register xfi_txdfifo_thr.<br>txdfifo_aempty_thr should satisfy:<br><br>$2 * tx\_frag\_len + txdfifo\_aempty\_thr \leq 60 \text{ (fifo\_depth)}$ |
| 5      | tx_fc_en    | <b>Enable TX Flow control</b>                                                                                                                                                                                                                                                                                                                                                                                |
| 4      | rx_fc_en    | <b>Enable RX Flow control</b>                                                                                                                                                                                                                                                                                                                                                                                |
| 3      | rxmpi_stop  | <b>RXMPI_STOP</b><br><br>0: Normal RX<br><br>1: MAC stop receiving data from PHY                                                                                                                                                                                                                                                                                                                             |
| 2      | rxmbi_stop  | <b>RXMBI_STOP</b><br><br>0: Normal RX<br><br>1: MAC stop sending data to RXMBI                                                                                                                                                                                                                                                                                                                               |
| 1      | txmpi_stop  | <b>TXMPI_STOP</b><br><br>0: Normal TX<br><br>1: MAC stop sending data to PHY                                                                                                                                                                                                                                                                                                                                 |
| 0      | txmbi_stop  | <b>TXMBI_STOP</b><br><br>0: Normal TX<br><br>1: MAC stop requesting data from TXMBI                                                                                                                                                                                                                                                                                                                          |

| Bit(s) | Name | Description |
|--------|------|-------------|
|--------|------|-------------|

15113004      xfi\_int\_sts      XFI interrupt status      00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26                          | 25                        | 24                        | 23                       | 22                         | 21                       | 20                      | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|-----------------------------|---------------------------|---------------------------|--------------------------|----------------------------|--------------------------|-------------------------|----|----|----|----|
| Name  |    |    |    |    |    |                             |                           |                           |                          |                            |                          |                         |    |    |    |    |
| Type  |    |    |    |    |    |                             |                           |                           |                          |                            |                          |                         |    |    |    |    |
| Reset |    |    |    |    |    |                             |                           |                           |                          |                            |                          |                         |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10                          | 9                         | 8                         | 7                        | 6                          | 5                        | 4                       | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | rx_codi<br>ng_err<br>or_int | rx_leng<br>_error<br>_int | rx_frag<br>_error<br>_int | rx_crc_<br>error_i<br>nt | rx_pau<br>se_fra<br>me_int | remote<br>_fault_i<br>nt | local_f<br>ault_in<br>t |    |    |    |    |
| Type  |    |    |    |    |    | W1C                         | W1C                       | W1C                       | W1C                      | W1C                        | W1C                      | W1C                     |    |    |    |    |
| Reset |    |    |    |    |    | 0                           | 0                         | 0                         | 0                        | 0                          | 0                        | 0                       |    |    |    |    |

| Bit(s) | Name                | Description                                                                                                                                                                                            |
|--------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10     | rx_coding_error_int | When se, indicates that a coding error was detected.                                                                                                                                                   |
| 9      | rx_leng_error_int   | When set, indicates that a packet was received with length over 16000 bytes.                                                                                                                           |
| 8      | rx_frag_error_int   | When set, indicates that a fragment was received.<br><br>A fragment is a frame that has a start of frame delimiter but no end of frame. Typically, it is immediately followed by a new start of frame. |
| 7      | rx_crc_error_int    | When set, indicates that a frame was received with<br><br>invalid CRC.                                                                                                                                 |
| 6      | rx_pause_frame_int  | When set, indicates that a pause frame was received.<br><br>Pause frames are discarded.                                                                                                                |
| 5      | remote_fault_int    | When set, indicates that the fault state-machine has transitioned in or out of remote fault condition.                                                                                                 |
| 4      | local_fault_int     | When set, indicates that the fault state-machine has transitioned in or out of local fault condition.                                                                                                  |



15113008      xfi\_int\_en      XFI interrupt enable      00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26                         | 25                       | 24                       | 23                      | 22                        | 21                      | 20                 | 19 | 18 | 17 | 16 |
|-------|----|----|----|----|----|----------------------------|--------------------------|--------------------------|-------------------------|---------------------------|-------------------------|--------------------|----|----|----|----|
| Name  |    |    |    |    |    |                            |                          |                          |                         |                           |                         |                    |    |    |    |    |
| Type  |    |    |    |    |    |                            |                          |                          |                         |                           |                         |                    |    |    |    |    |
| Reset |    |    |    |    |    |                            |                          |                          |                         |                           |                         |                    |    |    |    |    |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10                         | 9                        | 8                        | 7                       | 6                         | 5                       | 4                  | 3  | 2  | 1  | 0  |
| Name  |    |    |    |    |    | rx_codi<br>ng_err<br>or_en | rx_leng<br>_error<br>_en | rx_frag<br>_error<br>_en | rx_crc<br>_error_e<br>n | rx_pau<br>se_fra<br>me_en | remote<br>_fault_<br>en | local_f<br>ault_en |    |    |    |    |
| Type  |    |    |    |    |    | RW                         | RW                       | RW                       | RW                      | RW                        | RW                      | RW                 |    |    |    |    |
| Reset |    |    |    |    |    | 0                          | 0                        | 0                        | 0                       | 0                         | 0                       | 0                  |    |    |    |    |

| Bit(s) | Name               | Description                                    |
|--------|--------------------|------------------------------------------------|
| 10     | rx_coding_error_en | Set 1 to enable RX_CODING_ERROR_INT interrupt. |
| 9      | rx_leng_error_en   | Set 1 to enable RX LENG_ERROR_INT interrupt.   |
| 8      | rx_frag_error_en   | Set 1 to enable RX_FRAG_ERROR_INT interrupt.   |
| 7      | rx_crc_error_en    | Set 1 to enable RX_CRC_ERROR_INT interrupt.    |
| 6      | rx_pause_frame_en  | Set 1 to enable RX_PAUSE_FRAME_INT interrupt.  |
| 5      | remote_fault_en    | Set 1 to enable REMOTE_FAULT_INT interrupt.    |
| 4      | local_fault_en     | Set 1 to enable LOCAL_FAULT_INT interrupt.     |

**15113020**      **xfi\_fc\_sts**      **XFI global status**      **00000000**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20                       | 19                | 18               | 17            | 16            |
|-------|----|----|----|----|----|----|----|----|----|----|----|--------------------------|-------------------|------------------|---------------|---------------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |                          |                   |                  |               |               |
| Type  |    |    |    |    |    |    |    |    |    |    |    |                          |                   |                  |               |               |
| Reset |    |    |    |    |    |    |    |    |    |    |    |                          |                   |                  |               |               |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4                        | 3                 | 2                | 1             | 0             |
| Name  |    |    |    |    |    |    |    |    |    |    |    | tx_pau<br>se_pkt<br>type | fe_q_f<br>ull_sts | rx_pau<br>se_sts | tx_fc_s<br>ts | rx_fc_s<br>ts |
| Type  |    |    |    |    |    |    |    |    |    |    |    | RO                       | RO                | RO               | RO            | RO            |
| Reset |    |    |    |    |    |    |    |    |    |    |    | 0                        | 0                 | 0                | 0             | 0             |

| Bit(s) | Name             | Description                                                                                                                                                            |
|--------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4      | tx_pause_pkttype | <b>Last TX pause packet type</b><br><br>1'b1: Pause on<br><br>1'b0: Pause off                                                                                          |
| 3      | fe_q_full_sts    | <b>Indicates FE -- XFI port RX buffer usage status is nearly full</b>                                                                                                  |
| 2      | rx_pause_sts     | <b>RX pause frame is OK and on pause RX status</b>                                                                                                                     |
| 1      | tx_fc_sts        | <b>Pause on frame is sent when tx_fc_sts is set;</b><br><br>Pause off frame is sent when tx_fc_sts is not set.<br><br>tx_fc_sts is set when tx_fc_en & fe_q_full_sts   |
| 0      | rx_fc_sts        | <b>TX frame will be paused when rx_fc_sts is 1</b><br><br>This bit is set when rx_fc_en and RX pause on frame and unset when pause timer expires or RX pause off frame |

**15113060**      **xfi\_macaddrh**      **XFI MAC address high**      **00000000**

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_macaddrh |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description           |
|--------|--------------|-----------------------|
| 15:0   | xfi_macaddrh | <b>XFIMAC address</b> |

15113064 xfi\_macaddr1 XFI MAC address low 00000000

| Bit   | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_macaddr1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_macaddr1 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name         | Description    |
|--------|--------------|----------------|
| 31:0   | xfi_macaddr1 | XFIMAC address |

151130CC xfi\_if\_sts XFI interface status 00000000

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|------------------------|------------------------|------------------------|------------------------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |                        |                        |                        |                        |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |                        |                        |                        |                        |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |                        |                        |                        |                        |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    | rxmpi_<br>stop_st<br>s | rxmbi_<br>stop_st<br>s | txmpi_<br>stop_st<br>s | txmbi_<br>stop_st<br>s |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    | RO                     | RO                     | RO                     | RO                     |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    | 0                      | 0                      | 0                      | 0                      |

| Bit(s) | Name           | Description                 |
|--------|----------------|-----------------------------|
| 3      | rxmpi_stop_sts | Status of rxmpi stop or not |
| 2      | rxmbi_stop_sts | Status of rxmbi stop or not |
| 1      | txmpi_stop_sts | Status of txmpi stop or not |
| 0      | txmbi_stop_sts | Status of txmbi stop or not |

**151130D0      xfi\_rx\_cfg\_2      XFI RX configuration 2      00000800**

| Bit   | 31 | 30 | 29             | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
|-------|----|----|----------------|----|----|----|----|----|----|----|----|----|----|-----------------|----|----|
| Name  |    |    |                |    |    |    |    |    |    |    |    |    |    | rx_crc_strip_en |    |    |
| Type  |    |    |                |    |    |    |    |    |    |    |    |    |    | RW              |    |    |
| Reset |    |    |                |    |    |    |    |    |    |    |    |    |    | 0               |    |    |
| Bit   | 15 | 14 | 13             | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| Name  |    |    | rx_max_len_cfg |    |    |    |    |    |    |    |    |    |    |                 |    |    |
| Type  |    |    | RW             |    |    |    |    |    |    |    |    |    |    |                 |    |    |
| Reset |    |    | 0              | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0  |

| Bit(s) | Name            | Description                                                                                      |
|--------|-----------------|--------------------------------------------------------------------------------------------------|
| 18     | rx_crc_strip_en | <b>Strip RX CRC</b><br><br>1'b0: No effect<br><br>1'b1: Strip 4-byte CRC at the end of RX packet |
| 13:0   | rx_max_len_cfg  | <b>The maximum RX packet size (unit is byte)</b>                                                 |

**151130D4      xfi\_tx\_cfg\_2      XFI TX configuration 2      00000000**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                     |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                        |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                      |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | tx_padding_8byte_align |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                     |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                      |

| Bit(s) | Name                   | Description                                                                                                                                                     |
|--------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0      | tx_padding_8byte_align | <b>TX padding is 8-byte aligned</b><br><br>1'b0: TX padding is added from 1-byte aligned byte_cnt<br><br>1'b1: TX padding is added from 8-byte aligned byte_cnt |

**151130E0**      **xfi\_rx\_sts\_2**      **XFI USXGMII channel information**      **00000000**

| Bit   | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  |                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  |                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset |                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit   | 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | usxgmii_chn_info |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name             | Description                        |
|--------|------------------|------------------------------------|
| 15:0   | usxgmii_chn_info | USXGMII channel information status |

**15113100**      **xfi\_cnt\_ctrl**      **XFI count global control**      **00000006**

| Bit   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18              | 17                  | 16         |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------------|---------------------|------------|
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |                     |            |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |                     |            |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |                     |            |
| Bit   | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2               | 1                   | 0          |
| Name  |    |    |    |    |    |    |    |    |    |    |    |    |    | glb_cnt64b_wrap | glb_cnt64b_read_clr | glb_cntclr |
| Type  |    |    |    |    |    |    |    |    |    |    |    |    |    | RW              | RW                  | A0         |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    | 1               | 1                   | 0          |

| Bit(s) | Name                | Description                                                                                                                                                                  |
|--------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2      | glb_cnt64b_wrap     | <b>64-bit counter (0x150~0x17c, 0x1c0~0x1ec) wrap around control</b><br><br>1'b0: Counter keeps in maximux value when saturated<br>1'b1: Counter wraps around when saturated |
| 1      | glb_cnt64b_read_clr | <b>64-bit counter (0x150~0x17c, 0x1c0~0x1ec) read clear control</b><br><br>1'b0: Counter is not read clear<br>1'b1: Counter is read clear                                    |
| 0      | glb_cntclr          | <b>Global counter clear</b>                                                                                                                                                  |

15113104      xfi\_tx\_octets\_cnt      XFI transmit octets counter      00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | tx_octets_cnt |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | tx_octets_cnt |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                     |
|--------|---------------|---------------------------------------------------------------------------------|
| 31:0   | tx_octets_cnt | Counter for all transmitted octets.<br>Counter will wrap when limit is reached. |

15113108      xfi\_tx\_pkt\_cnt      XFI transmit packet counter      00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | tx_packet_cnt |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | tx_packet_cnt |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                     |
|--------|---------------|---------------------------------------------------------------------------------|
| 31:0   | tx_packet_cnt | Counter for all transmitted packet.<br>Counter will wrap when limit is reached. |

15113150 xfi\_tx\_uc\_pkt\_cnt\_l XFI transmit unicast packet counter [31:0] 00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_tx_uc_pkt_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_tx_uc_pkt_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                       |
|--------|---------------------|---------------------------------------------------|
| 31:0   | xfi_tx_uc_pkt_cnt_l | Counter for all transmitted unicast packet[31:0]. |

15113154 xfi\_tx\_uc\_pkt\_cnt\_h XFI transmit unicast packet counter [63:32] 00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_tx_uc_pkt_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_tx_uc_pkt_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                        |
|--------|---------------------|----------------------------------------------------|
| 31:0   | xfi_tx_uc_pkt_cnt_h | Counter for all transmitted unicast packet[63:32]. |

15113158 xfi\_tx\_uc\_byte\_cnt\_l XFI transmit unicast byte counter [31:0] 00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_tx_uc_byte_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_tx_uc_byte_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                     |
|--------|----------------------|-------------------------------------------------|
| 31:0   | xfi_tx_uc_byte_cnt_l | Counter for all transmitted unicast byte[31:0]. |

**1511315C      xfi\_tx\_uc\_byte\_cnt\_h      XFI transmit unicast byte counter [63:32]      00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_tx_uc_byte_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_tx_uc_byte_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                      |
|--------|----------------------|--------------------------------------------------|
| 31:0   | xfi_tx_uc_byte_cnt_h | Counter for all transmitted unicast byte[63:32]. |

**15113160      xfi\_tx\_mc\_pkt\_cnt\_l      XFI transmit multicast packet counter [31:0]      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_tx_mc_pkt_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_tx_mc_pkt_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                         |
|--------|---------------------|-----------------------------------------------------|
| 31:0   | xfi_tx_mc_pkt_cnt_l | Counter for all transmitted multicast packet[31:0]. |

**15113164      xfi\_tx\_mc\_pkt\_cnt\_h      XFI transmit multicast packet counter [63:32]      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_tx_mc_pkt_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_tx_mc_pkt_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                          |
|--------|---------------------|------------------------------------------------------|
| 31:0   | xfi_tx_mc_pkt_cnt_h | Counter for all transmitted multicast packet[63:32]. |



**15113168**      **xfi\_tx\_mc\_byte\_cnt\_l**      **XFI transmit multicast byte counter [31:0]**      **00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_tx_mc_byte_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_tx_mc_byte_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                       |
|--------|----------------------|---------------------------------------------------|
| 31:0   | xfi_tx_mc_byte_cnt_l | Counter for all transmitted multicast byte[31:0]. |

**1511316C**      **xfi\_tx\_mc\_byte\_cnt\_h**      **XFI transmit multicast byte counter [63:32]**      **00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_tx_mc_byte_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_tx_mc_byte_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                        |
|--------|----------------------|----------------------------------------------------|
| 31:0   | xfi_tx_mc_byte_cnt_h | Counter for all transmitted multicast byte[63:32]. |

**15113170**      **xfi\_tx\_bc\_pkt\_cnt\_l**      **XFI transmit broadcast packet counter [31:0]**      **00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_tx_bc_pkt_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_tx_bc_pkt_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                         |
|--------|---------------------|-----------------------------------------------------|
| 31:0   | xfi_tx_bc_pkt_cnt_l | Counter for all transmitted broadcast packet[31:0]. |

**15113174**      **xfi\_tx\_bc\_pkt\_cnt\_h**      **XFI transmit broadcast packet counter [63:32]**      **00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_tx_bc_pkt_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_tx_bc_pkt_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                          |
|--------|---------------------|------------------------------------------------------|
| 31:0   | xfi_tx_bc_pkt_cnt_h | Counter for all transmitted broadcast packet[63:32]. |

**15113178**      **xfi\_tx\_bc\_byte\_cnt\_l**      **XFI transmit broadcast byte counter [31:0]**      **00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_tx_bc_byte_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_tx_bc_byte_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                       |
|--------|----------------------|---------------------------------------------------|
| 31:0   | xfi_tx_bc_byte_cnt_l | Counter for all transmitted broadcast byte[31:0]. |

**1511317C**      **xfi\_tx\_bc\_byte\_cnt\_h**      **XFI transmit broadcast byte counter [63:32]**      **00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_tx_bc_byte_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_tx_bc_byte_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                        |
|--------|----------------------|----------------------------------------------------|
| 31:0   | xfi_tx_bc_byte_cnt_h | Counter for all transmitted broadcast byte[63:32]. |

15113184      xfi\_rx\_octets\_cnt      XFI receive octets counter      00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | rx_octets_cnt |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | rx_octets_cnt |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                  |
|--------|---------------|------------------------------------------------------------------------------|
| 31:0   | rx_octets_cnt | Counter for all received octets.<br>Counter will wrap when limit is reached. |

15113188      xfi\_rx\_pkt\_cnt      XFI receive packet counter      00000000

| Bit   | 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | rx_packet_cnt |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | rx_packet_cnt |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name          | Description                                                                  |
|--------|---------------|------------------------------------------------------------------------------|
| 31:0   | rx_packet_cnt | Counter for all received packet.<br>Counter will wrap when limit is reached. |

15113190      xfi\_rx\_pause\_cnt      XFI receive pause packet counter      00000000

| Bit   | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | rx_pauseoff_cnt |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | rx_pauseon_cnt  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name            | Description                                                                            |
|--------|-----------------|----------------------------------------------------------------------------------------|
| 31:16  | rx_pauseoff_cnt | Counter for all received pause off packet.<br>Counter will wrap when limit is reached. |
| 15:0   | rx_pauseon_cnt  | Counter for all received pause on packet.<br>Counter will wrap when limit is reached.  |

151131C0      xfi\_rx\_uc\_pkt\_cnt\_l      XFI receive unicast packet counter [31:0]      00000000

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_rx_uc_pkt_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_rx_uc_pkt_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                    |
|--------|---------------------|------------------------------------------------|
| 31:0   | xfi_rx_uc_pkt_cnt_l | Counter for all received unicast packet[31:0]. |

**151131C4**      **xfi\_rx\_uc\_pkt\_cnt\_h**      **XFI receive unicast packet counter [63:32]**      **00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_rx_uc_pkt_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_rx_uc_pkt_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                     |
|--------|---------------------|-------------------------------------------------|
| 31:0   | xfi_rx_uc_pkt_cnt_h | Counter for all received unicast packet[63:32]. |

**151131C8**      **xfi\_rx\_uc\_byte\_cnt\_l**      **XFI receive unicast byte counter [31:0]**      **00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_rx_uc_byte_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_rx_uc_byte_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                  |
|--------|----------------------|----------------------------------------------|
| 31:0   | xfi_rx_uc_byte_cnt_l | Counter for all received unicast byte[31:0]. |

**151131CC**      **xfi\_rx\_uc\_byte\_cnt\_h**      **XFI receive unicast byte counter [63:32]**      **00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_rx_uc_byte_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_rx_uc_byte_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                   |
|--------|----------------------|-----------------------------------------------|
| 31:0   | xfi_rx_uc_byte_cnt_h | Counter for all received unicast byte[63:32]. |

**151131D0**      **xfi\_rx\_mc\_pkt\_cnt\_l**      **XFI receive multicast packet counter [31:0]**      **00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_rx_mc_pkt_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_rx_mc_pkt_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                      |
|--------|---------------------|--------------------------------------------------|
| 31:0   | xfi_rx_mc_pkt_cnt_l | Counter for all received multicast packet[31:0]. |

**151131D4**      **xfi\_rx\_mc\_pkt\_cnt\_h**      **XFI receive multicast packet counter [63:32]**      **00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_rx_mc_pkt_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_rx_mc_pkt_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                       |
|--------|---------------------|---------------------------------------------------|
| 31:0   | xfi_rx_mc_pkt_cnt_h | Counter for all received multicast packet[63:32]. |

**151131D8**      **xfi\_rx\_mc\_byte\_cnt\_l**      **XFI receive multicast byte counter [31:0]**      **00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_rx_mc_byte_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_rx_mc_byte_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                    |
|--------|----------------------|------------------------------------------------|
| 31:0   | xfi_rx_mc_byte_cnt_l | Counter for all received multicast byte[31:0]. |

**151131DC      xfi\_rx\_mc\_byte\_cnt\_h      XFI receive multicast byte counter [63:32]      00000000**

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_rx_mc_byte_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_rx_mc_byte_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                     |
|--------|----------------------|-------------------------------------------------|
| 31:0   | xfi_rx_mc_byte_cnt_h | Counter for all received multicast byte[63:32]. |

**151131E0      xfi\_rx\_bc\_pkt\_cnt\_l      XFI receive broadcast packet counter [31:0]      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_rx_bc_pkt_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_rx_bc_pkt_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                      |
|--------|---------------------|--------------------------------------------------|
| 31:0   | xfi_rx_bc_pkt_cnt_l | Counter for all received broadcast packet[31:0]. |

**151131E4      xfi\_rx\_bc\_pkt\_cnt\_h      XFI receive broadcast packet counter [63:32]      00000000**

| Bit   | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_rx_bc_pkt_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_rx_bc_pkt_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                | Description                                       |
|--------|---------------------|---------------------------------------------------|
| 31:0   | xfi_rx_bc_pkt_cnt_h | Counter for all received broadcast packet[63:32]. |

151131E8      xfi\_rx\_bc\_byte\_cnt\_l      XFI receive broadcast byte counter [31:0]      00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_rx_bc_byte_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_rx_bc_byte_cnt_l |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                    |
|--------|----------------------|------------------------------------------------|
| 31:0   | xfi_rx_bc_byte_cnt_l | Counter for all received broadcast byte[31:0]. |

151131EC      xfi\_rx\_bc\_byte\_cnt\_h      XFI receive broadcast byte counter [63:32]      00000000

| Bit   | 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|-------|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Name  | xfi_rx_bc_byte_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| Bit   | 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Name  | xfi_rx_bc_byte_cnt_h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Type  | RO                   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit(s) | Name                 | Description                                     |
|--------|----------------------|-------------------------------------------------|
| 31:0   | xfi_rx_bc_byte_cnt_h | Counter for all received broadcast byte[63:32]. |



## Exhibit 1 Terms and Conditions

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