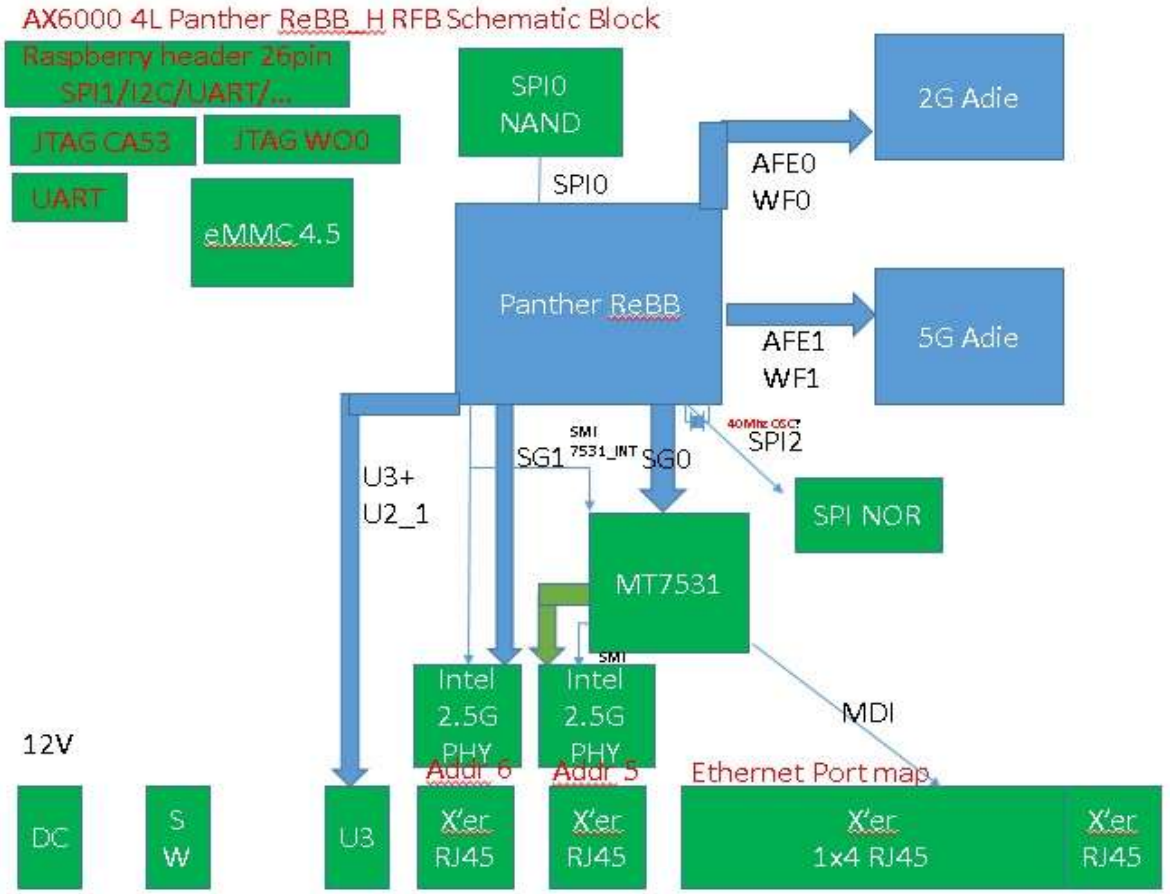

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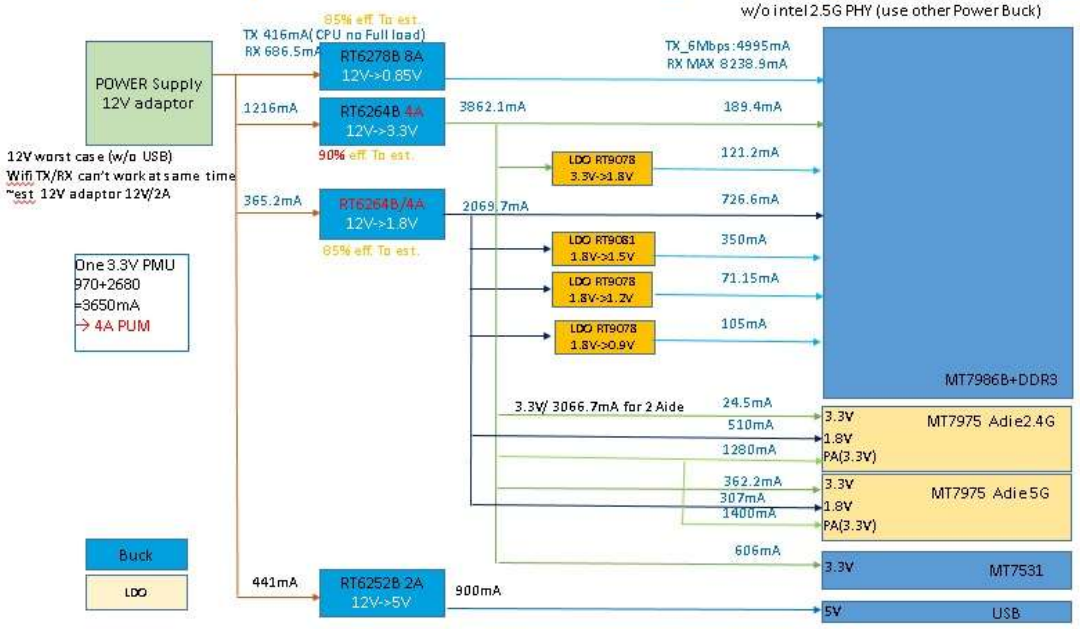
MEDIATEK	Title: Block Diagram & Power on sequence		
Size: B	Document Number: MT7629 RFB	Drawn:	Rev: V01
Date: Monday, August 09, 2021	Sheet 1 of 15		

Power Tree (MT7986B+MT7975x2_AX6000)

2021/04/15 update



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Title: Power Tree			
Size: B	Document Number: MTMT7986B RFB	Drawn:	Rev: V10
Date: Monday, August 09, 2021		Sheet 2 of 16	

20210329 V10
1. Draft Revision for MT7975
2. RSTB rename PAD_PMU_POR_B for page 07 and 08
3. Remove multi-rail power

20210506 V11
1. Pull high Bootstrap pin "PWM0"
2. Pull high DIG_RESETB and reserve HB9/HB10 connection.
3. Update 2G matching

20210527 V12
1. Reserve MT7986 SG1 wire to MT7531 P5.
2. MT7531 2.5G PHY change control path to MT7986 MDC/MDIO

20210806 BOM update
1. update Power on sequence LOD 1.5VD should delay than AVDD18 at least 3 ms

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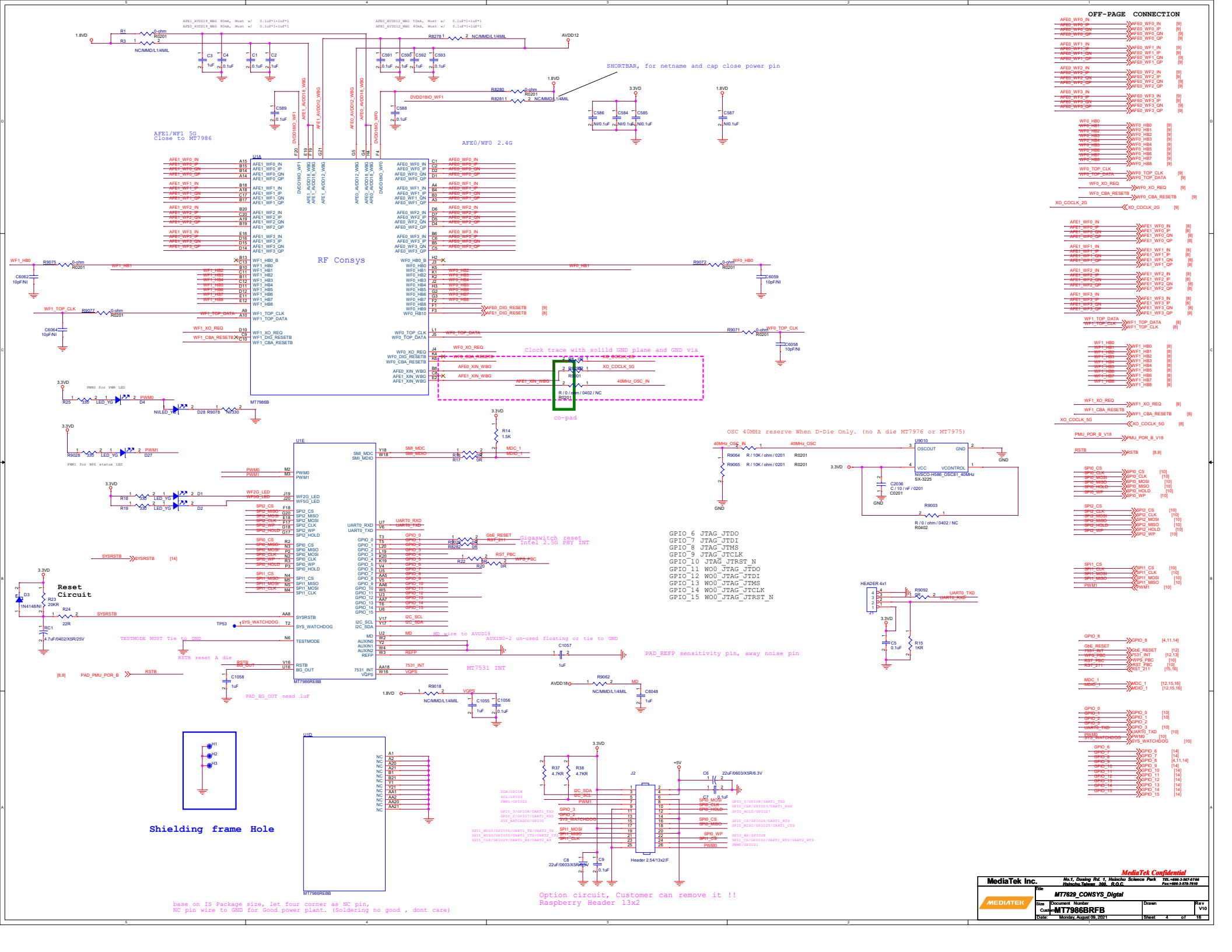
Title: Change History

Size	Document Number	Drawn	Rev
B	MT7986B RFB		V10
Date: Monday, August 09, 2021		Sheet 3 of 16	


OFF-PAGE CONNECTION
SHORTBAR, for netname and cap close power pin
AFE1/WF1 5G
Close to MT7986
AFE0/WF0 2.4G
RF Consys
Clock trace with solild GND plane and GND via
co-pad
OSC 40MHz reserve When D-Die Only. (no A die MT7976 or MT7975)
Reset Circuit
Gigaswitch reset
Intel 2.5G PHY INT
MT7531 INT
PAD_REFP sensitivity pin, away noise pin
PAD_BG_OUT need 1uF
TESTMODE MUST Tie to GND
RSTB reset A die
MD wire to AVDD18
AUXIN0-2 un-used floating or tie to GND
GPIO_6 JTAG_JTDO
GPIO_7 JTAG_JTDI
GPIO_8 JTAG_JTMS
GPIO_9 JTAG_JTCLK
GPIO_10 JTAG_JTRST_N
GPIO_11 WO0_JTAG_JTDO
GPIO_12 WO0_JTAG_JTDI
GPIO_13 WO0_JTAG_JTMS
GPIO_14 WO0_JTAG_JTCLK
GPIO_15 WO0_JTAG_JTRST_N
Shielding frame Hole
base on IS Package size, let four corner as NC pin,
NC pin wire to GND for Good power plant. (Soldering no good , dont care)
Option circuit, Customer can remove it !!
Raspberry Header 13x2
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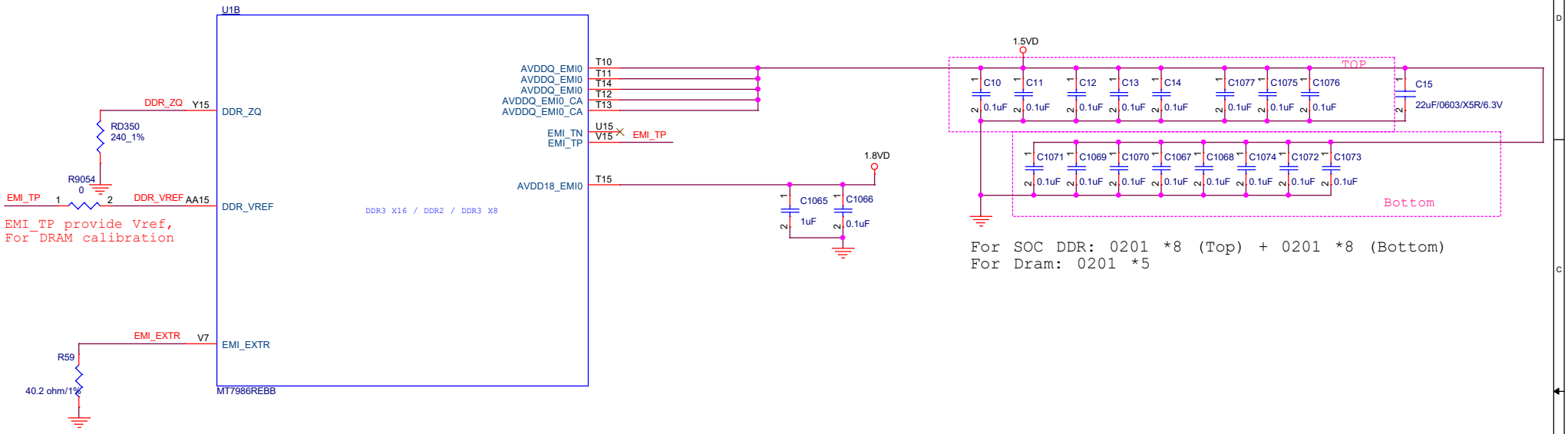
MT7629_CONSYS_Digtal
MT7986BRFB
Monday, August 09, 2021

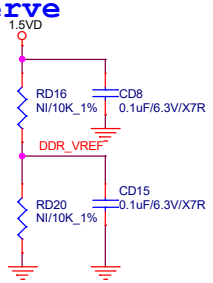
OFF-PAGE CONNECTION



For SOC DDR: 0201 *8 (Top) + 0201 *8 (Bottom)
For Dram: 0201 *5

DDR3 EXTR 40.2 ohm

External DDR3 Ref Volt. Reserve



Near MT7986 DRAM SIDE

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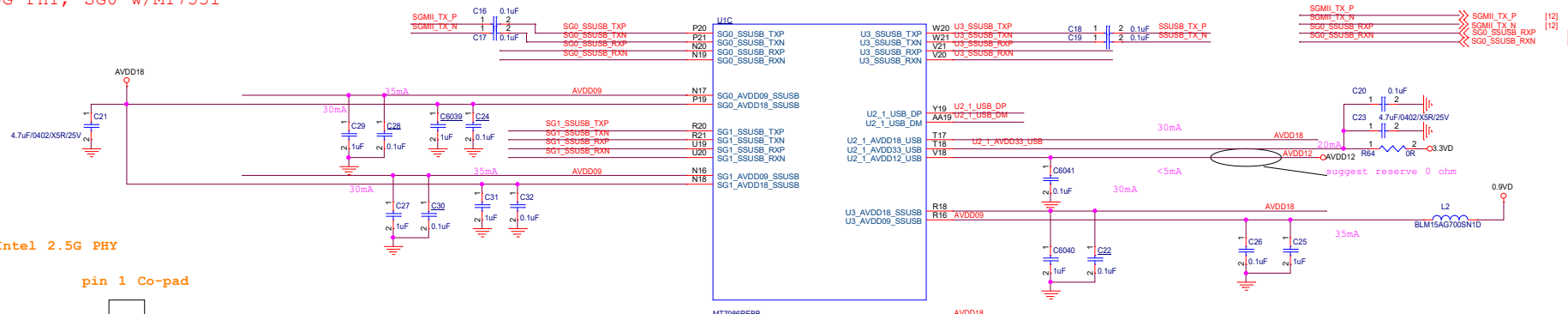
Title: MT7986B_DRAM			
Size: B	Document Number: MT7986B RFB	Drawn:	Rev: V10
Date: Monday, August 09, 2021		Sheet 5 of 16	

1. U2_1 w/ U3
2. SG1 w/ 2.5G PHY, SG0 w/MT7531

OFF-PAGE CONNECTION

USB differential impedance: 90 ohm



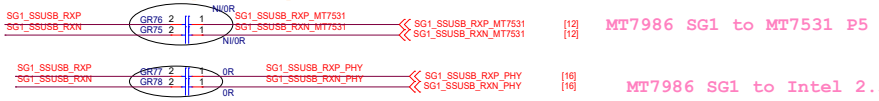
Default BOM SG1 to Intel 2.5G PHY

pin 1 Co-pad

MT7986 SG1 to Intel 2.5G PHY

MT7986 SG1 to MT7531 P5

pin 1 Co-pad

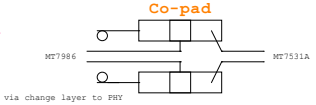


MT7986 SG1 to MT7531 P5

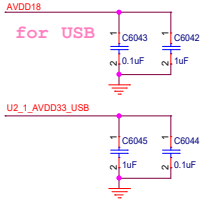
MT7986 SG1 to Intel 2.5G PHY

GR76/G77 copad, GR75/GR78 copad
C7065/C7063 copad, C7066/C7064 copad

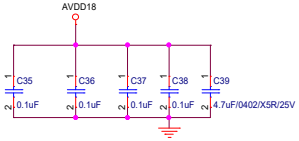
Co-pad



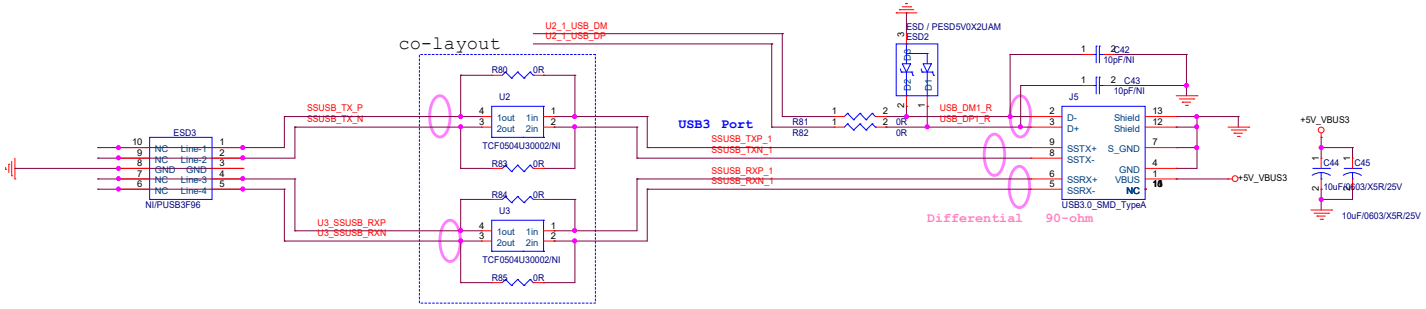
for USB



SGMII-P6 to MT7986



co-layout



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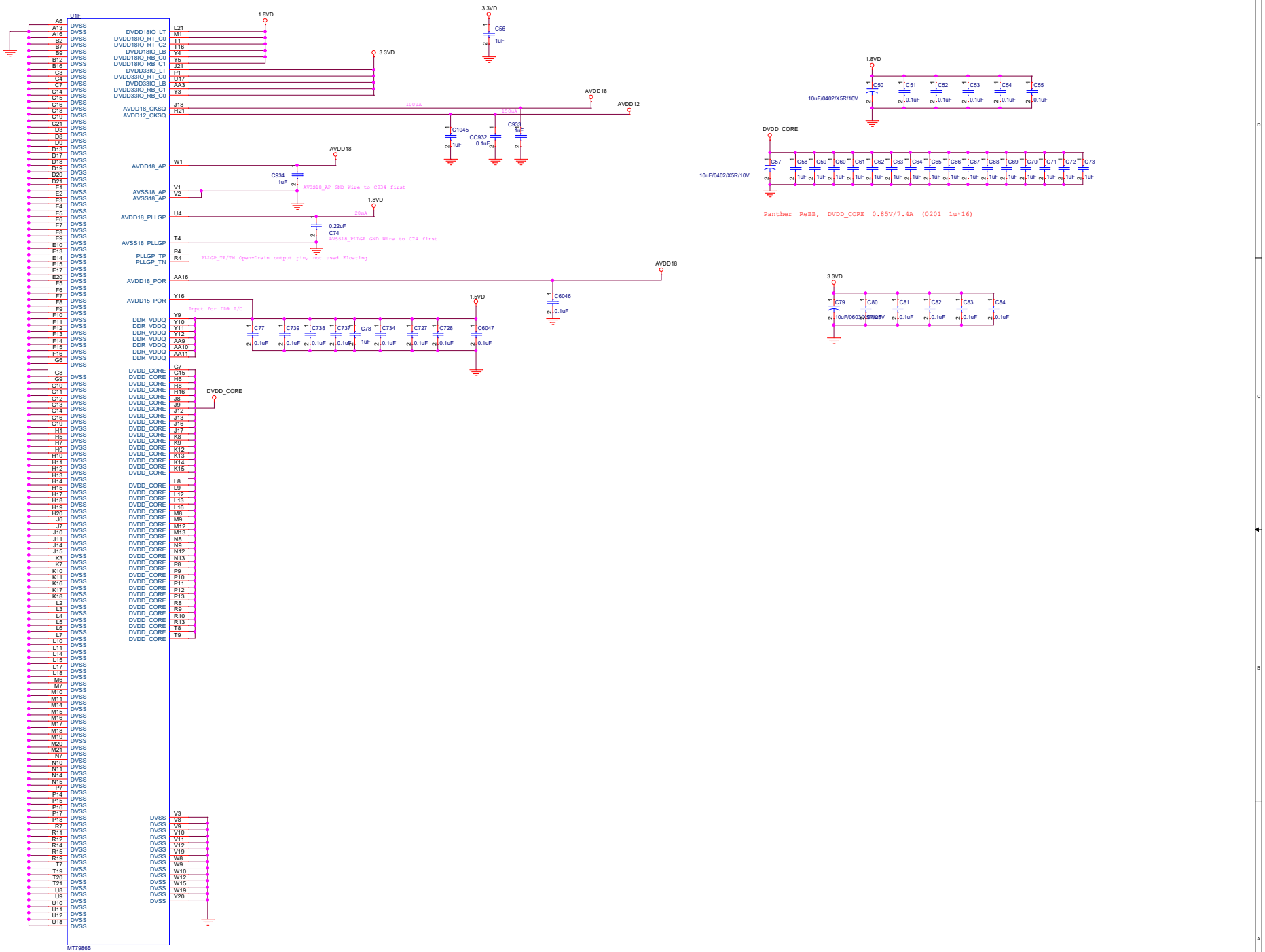
Title: MT79B6B_PCIe_USB_SGMII			
Size: Custom	Document Number: MT7986B RFB	Drawn	Rev: V10
Date: Monday, August 09, 2021		Sheet 6 of 16	



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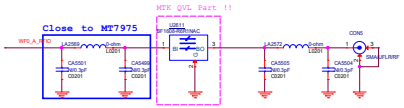
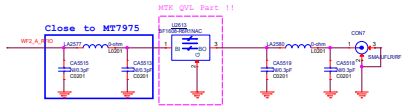
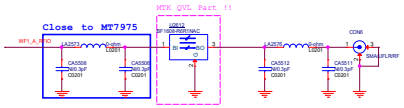
MEDIATEK	Title: MT7986_PWRGND		
	Size: Custom	Document Number: MT7986B RFB	Drawn / Rev: 10
	Date: Monday, August 09, 2021	Sheet 7 of 16	



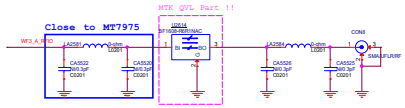
WF0_5G_iPAiLNA TX Out Circuit



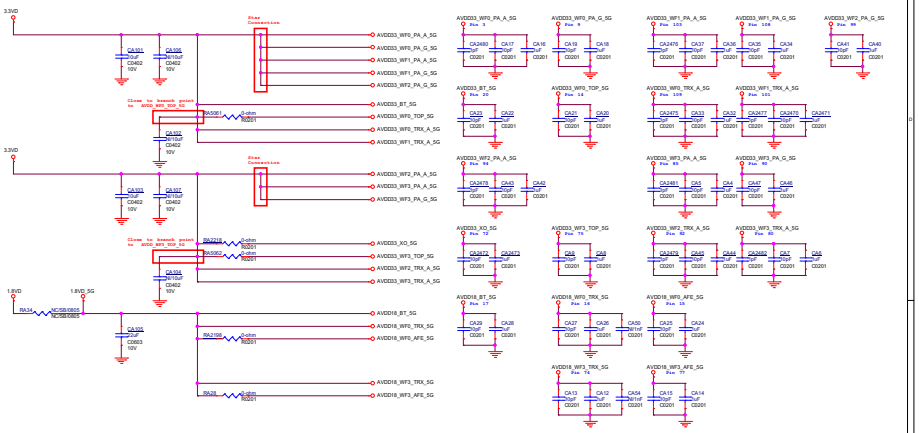
WF2_5G_iPAiLNA TX Out Circuit

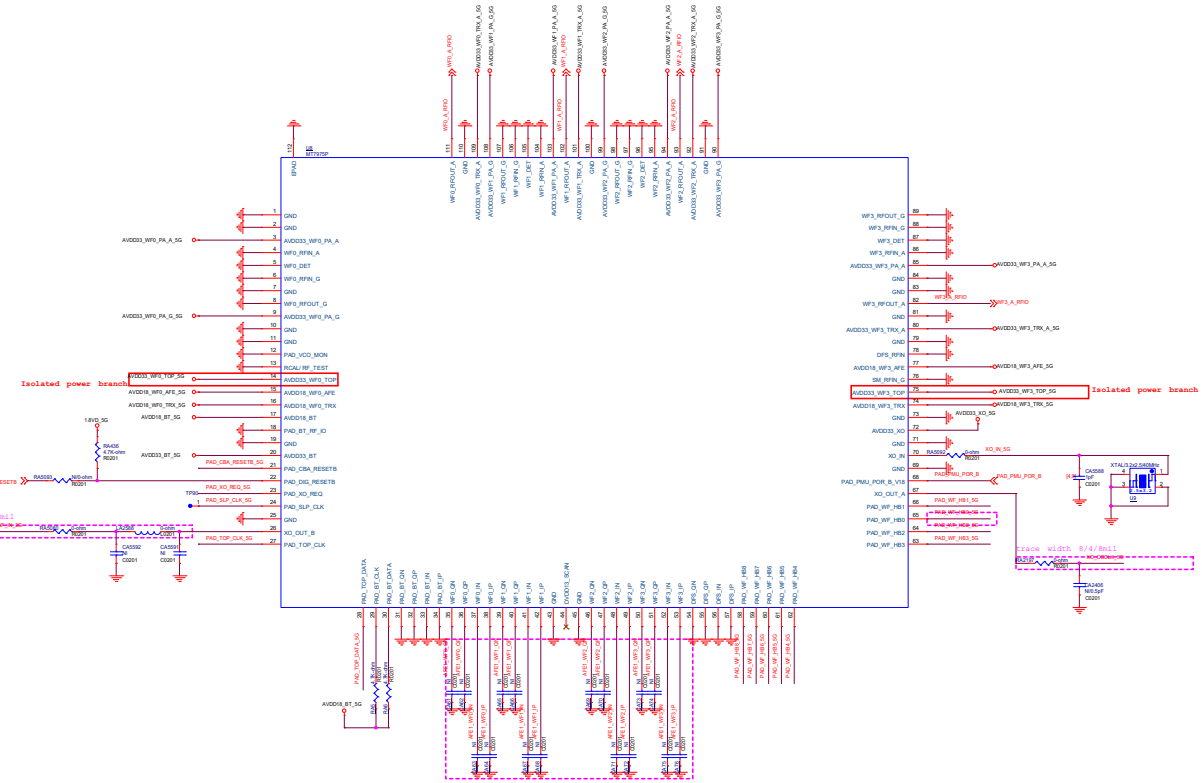


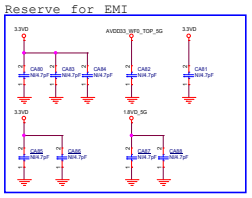
WF1_5G_iPAiLNA TX Out Circuit

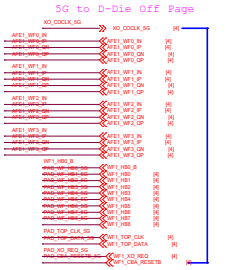


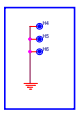
WF3_5G_iPAiLNA TX Out Circuit



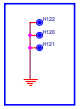








Shielding frame Hole (TOP)



Shielding frame Hole (BOT)

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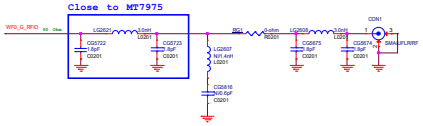
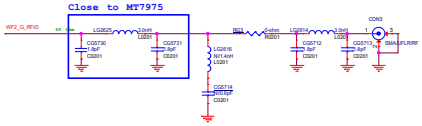
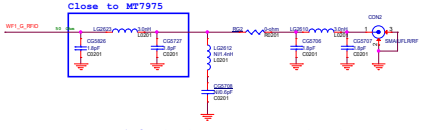
Title	MT7975_5G-AX_A		
Size: A1	Document Number: MT7986B RFB	Drawn:	Rev: 1.0
Date: Monday, August 09, 2021	Sheet 8 of 31		



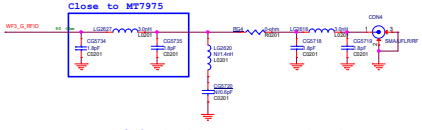
WF0_2G_iPAiLNA TRX Out Circuit



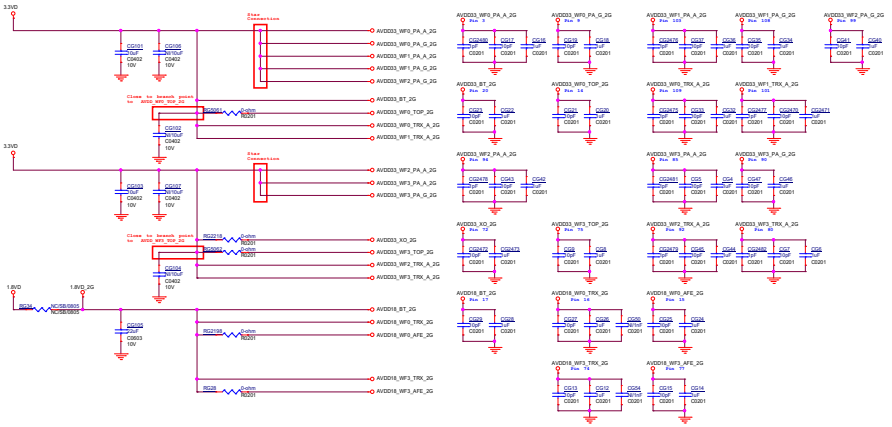
WF2_2G_iPAiLNA TRX Out Circuit

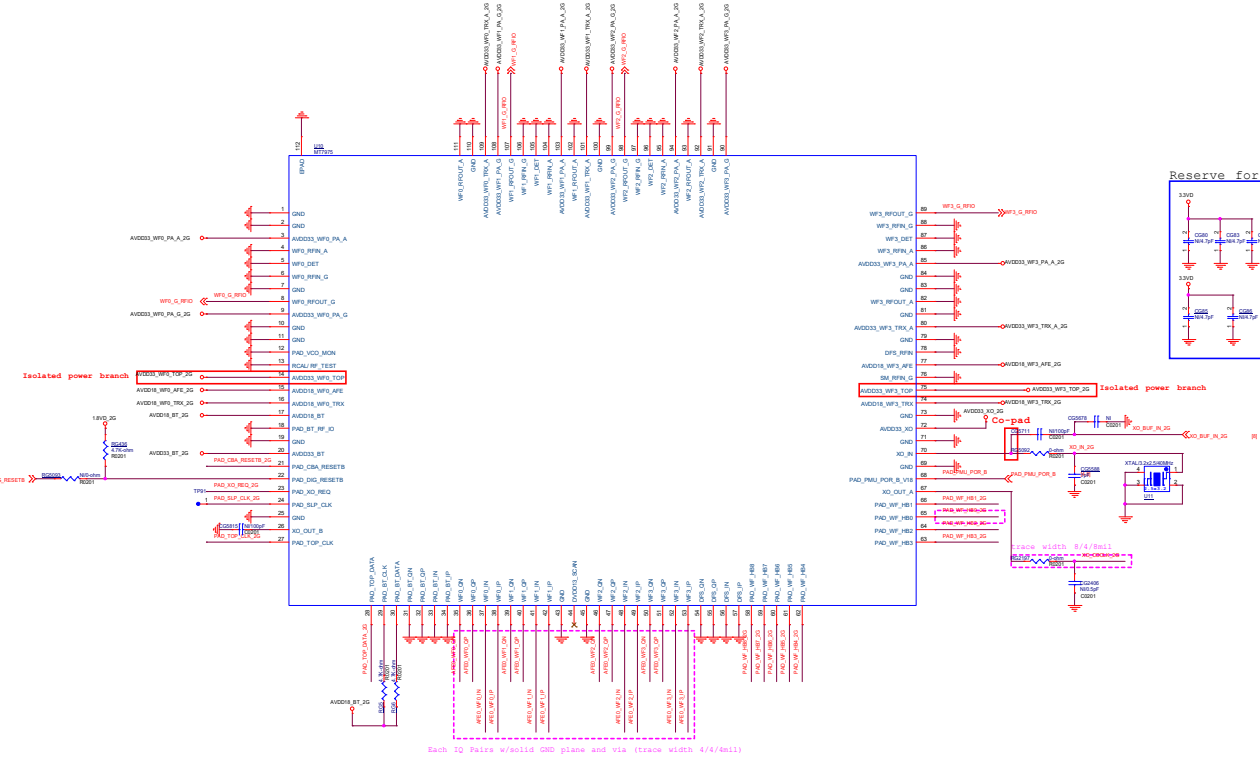


WF1_2G_iPAiLNA TRX Out Circuit



WF3_2G_iPAiLNA TRX Out Circuit





MediaTek Inc.			
Title: MT7975_2.4G			
Size: A1	Document Number: MT7986B RFB	Drawn:	Rev: 1.0
Date: Monday, August 02, 2021		Sheet: 9 of 31	

Heat SINK FIX HOLD

H21 TOOLING_HOLE/4MM/NI
H16 TOOLING_HOLE/4MM/NI
H18 TOOLING_HOLE/4MM/NI

OFF-PAGE CONNECTION

SPI0_CS, SPI0_CLK, SPI0_MOSI, SPI0_MISO, SPI0_HOLD, SPI0_WP
SPI0_CS [4], SPI0_CLK [4], SPI0_MOSI [4], SPI0_MISO [4], SPI0_HOLD [4], SPI0_WP [4]

SPI2_CS, SPI2_CLK, SPI2_MOSI, SPI2_MISO, SPI2_HOLD, SPI2_WP
SPI2_CS [4], SPI2_CLK [4], SPI2_MOSI [4], SPI2_MISO [4], SPI2_HOLD [4], SPI2_WP [4]

WPS_PBC, RST_PBC
WPS_PBC [4,10], RST_PBC [4,10]

GPIO_0, GPIO_1, GPIO_3, UART0_TXD, PWM0, SYS_WATCHDOG
GPIO_0 [4], GPIO_1 [4], GPIO_3 [4], UART0_TXD [4], PWM0 [4], SYS_WATCHDOG [4]

System/Power LED

D5 LED, POWERLED, R154 330R, 3.3VD

WPS Button

R9089 4.7K/NC, R9090 4.7K/NC, S1 TS02-CN-S1PF, WPS_PBC, GND1–GND4

Reset/ Factory Default Button

S2 TS02-CN-S1PF, RST_PBC, H15 NI/HOLE/GND

Jumper5

J611, SPI1_CS, eMMC_CLK, J / DIP3 / P2.54

CLK work >40Mhz suggest add damping for Flash CLK
SPI2 to SPIM-NOR/SPIM-NAND Flash

eMMC IO 3.3V

eMMC is share pin w/ SPI (3.3V)
if eMMC data 1.8V, SPI 3.3V current leakage?

U46 eMMC, THGBMBG5D1LBAIL
eMMC_CLK, eMMC_CMD, eMMC_DAT0, eMMC_DAT1, eMMC_DAT2, eMMC_DAT3, eMMC_DAT4, eMMC_DAT5, eMMC_DAT6, eMMC_DAT7, eMMC_RSTB
C758, C2, 1uF
eMMC_VCC, eMMC_VCCQ
eMMC VCC: 3.3V
eMMC VCCQ: 3.3V
C751 1uF, C750 1uF, C752 0.1uF, C753 0.1uF, C754 0.1uF
C755 1uF, C756 1uF, C757 0.1uF, C749 0.1uF
L85 0R, L91 0R, C747 2.2uF, C748 0.1uF

PWM1 EMMC_RSTB
SPI0_CLK EMMC_DATA_0
SPI0_MOSI EMMC_DATA_1
SPI0_MISO EMMC_DATA_2
SPI0_CS EMMC_DATA_3
SPI0_HOLD EMMC_DATA_4
SPI0_WP EMMC_DATA_5
SPI1_CLK EMMC_DATA_6
SPI1_MOSI EMMC_DATA_7
SPI1_MISO EMMC_CMD
SPI1_CS EMMC_CK

Jumper4

J610, SPI0_CS, eMMC_DAT3, R9080 NI/0R, SPI0_CS_SNFI
C231 0.1uF, C232 0.1uF
Near SPI Flash VCC

SPI Nor/NAND Flash

R156 4.7K, R158 4.7K, R159 4.7K
U12 MX25L12833FM2I-10G
SPI2_CS_NOR, SPI2_MISO, SPI2_WP, SPI2_HOLD, SPI2_CLK, SPI2_MOSI
SPIM-NOR SOP-8

keep layout trace short
R9085 4.7K, U9011 MX35LF1GE4AB
SPIM-NAND
for ECC Free

U13 SPI FLASH NI/MX25L25635F
SPIM-NOR SOP-16

SPI0 to NAND FLASH

keep layout trace short
R9087 4.7K, R9086 4.7K
U14 W25N01GVZEIG
SNFI-NAND
for ECC 1bit/4bit/8bit, rhe image need ECC

Boot Strapping

Pin Name	Description	Boot Sequence
{GPIO_1,GPIO_0}	Boot mode	00: SPIM-NOR 01: SPIM-NAND (MTK suggest SPIM_NAND) 10: eMMC 11: SNFI-NAND (Don't suggest customer use)
{GPIO_3}	A-Die Mode	0: 2 A-Die keelp low
UART_TX0	Second A Die Xtal mode	0 : XTAL mode 1 : Buffer mode
PWM0	XTAL frequency select	1 : 40MHz
SYS_WATCHDOG (for IAP only)	CPU 1.023V/ 0.85V select	MT7986B don't care

x: Don't care

JP setting	JP1	JP2	JP3	JP4	JP5
SPIM-NOR	2-3	2-3	1-2	1-2	1-2
SPIM-NAND	2-3	1-2	2-3	1-2	1-2
eMMC	1-2	2-3	x	1-2	1-2
SNFI-NAND	1-2	1-2	NC	2-3	2-3

GPIO_0, GPIO_1 Internal PD

R9004 NI/1K R0402, R9005 NI/1K R0402
R9007 NI/1K R0402, R9006 NI/1K R0402

A die MT7975

PWM0, R9052 1K R0402, R9053 NI/1K R0402

MT7986B, CPU Only 0.85V, this bootstrap don't care

R9051 NI/1K R0402, SYS_WATCHDOG

2nd A die XTAL mode: XTAL Mode

GPIO_3, R9025 1K R0402
UART0_TXD, R9037 NI/1K R0402, R9088 1K R0402

Boot mode Jumper/Layout TXT indicate table

Jumper1: J607, GPIO_1, R9033 1K R0402, R9035 1K R0402
Jumper2: J606, GPIO_0, R9034 1K R0402, R9036 1K R0402
J / DIP3 / P2.54

Jumper3: J609, SPI2_CS, SPI2_CS_NOR, SPI2_CS_NAND, R5047 NI/0R, R5048 NI/0R

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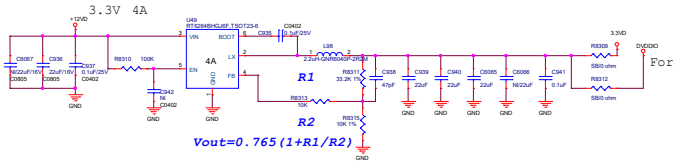
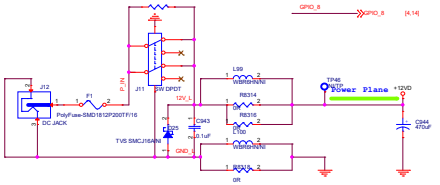
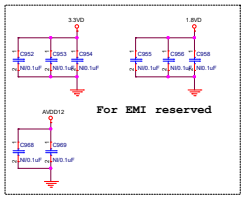
Title: Flash & LEDs
Size: C
Document Number: MT7986B RFB
Drawn:
Rev: V10
Date: Monday, August 09, 2021
Sheet 10 of 16

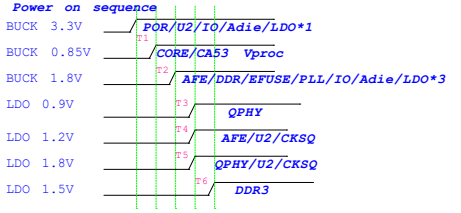






T1=0.95ms T2=1.7ms T3=3.13ms T4=3.13ms T5=3.57ms T5=4.5ms

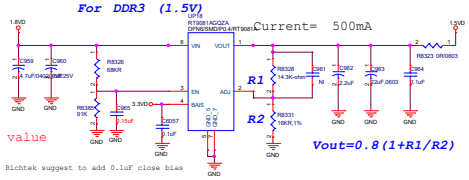
Power on sequence



2021/0806 LDO 1.5V delay at leat 3ms than LDO1.8V

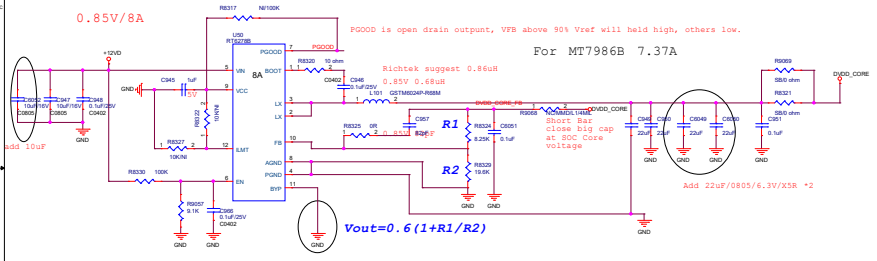
For DDR3 (1.5V)

Current= 500mA



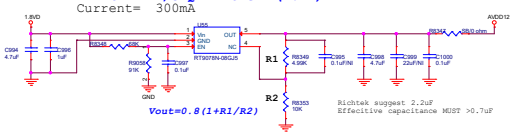
2021/08/06 modify C965 value

0.85V/8A



For AFE/CKQ12 Power (1.2V)

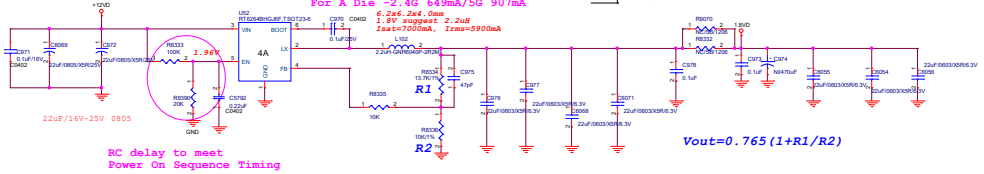
Current= 300mA



1.8V/4A

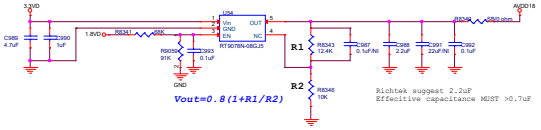
For D Die -Rebb_H 726mA
LDO 1.5V/350mA, 1.2V/71mA, 0.9V/105mA
For A Die -2.4G 649mA/5G 907mA

1.8V/2.8A



For CKSQ18/SGMII/USB/PCIE Power (1.8V)

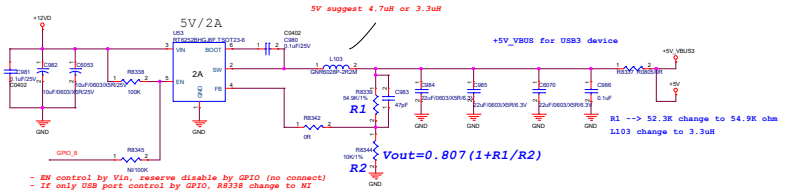
Current= 300mA



5V/2A

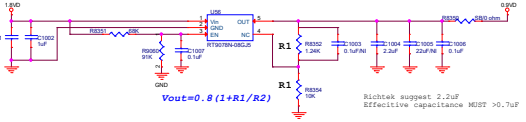
5V suggest 4.7uH or 3.3uH

+5V_VBUS for USB3 device



For SGMII/USB3/PCIe Power (0.9V)

Current= 300mA



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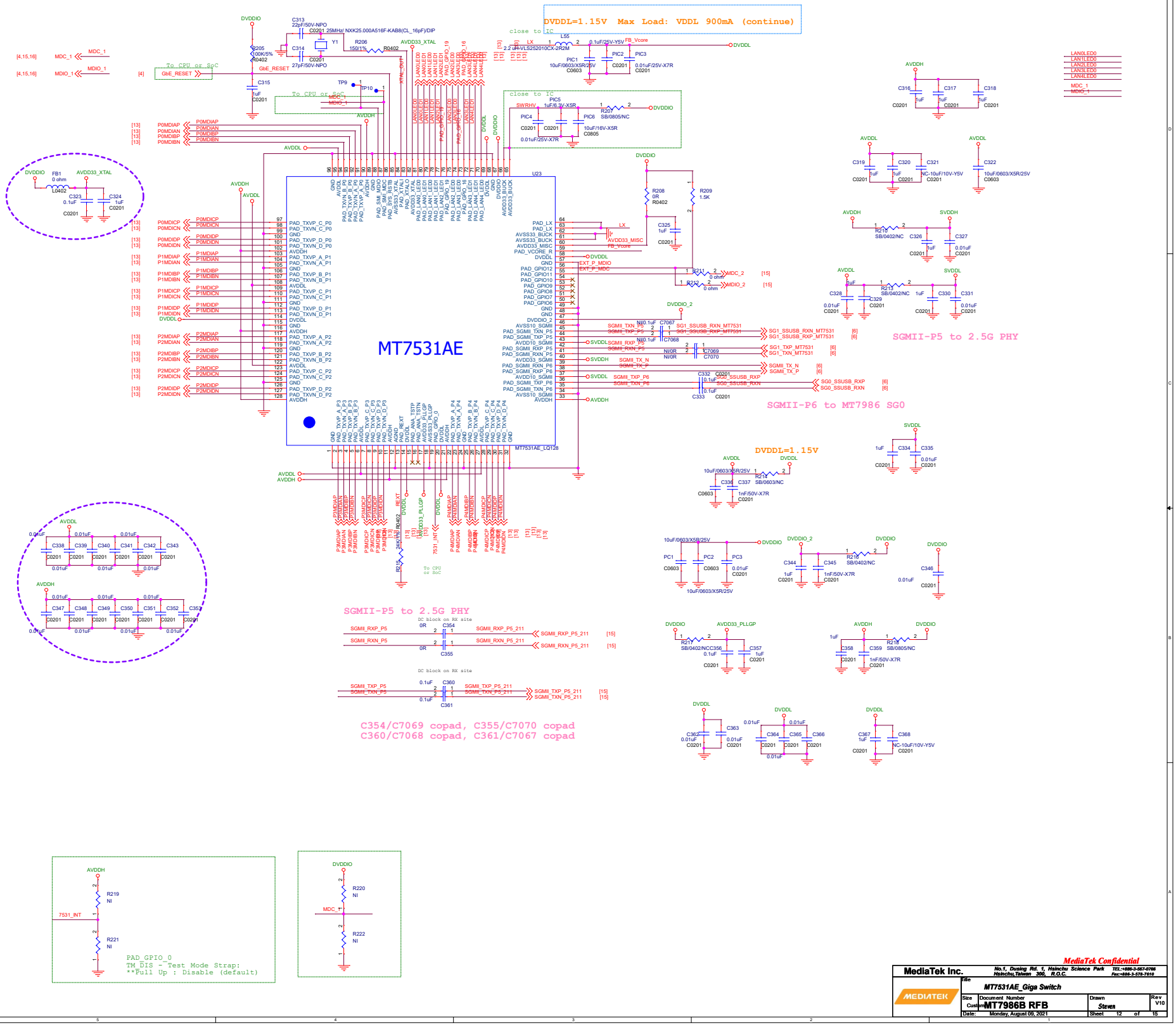
Title: Power_External Buck_LDO

Size: D | Document Number: MT7986B RFB | Rev: V10 | Drawn | Date: Monday, August 09, 2021 | Sheet 11 of 16


DVDDL=1.15V Max Load: VDDL 900mA (continue)
MT7531AE
MT7531AE_LQT128
SGMII-P5 to 2.5G PHY
SGMII-P6 to MT7986 SG0
SGMII-P5 to 2.5G PHY
DVDDL=1.15V
C354/C7069 copad, C355/C7070 copad
C360/C7068 copad, C361/C7067 copad
PAD_GPIO_0
TM_DIS - Test Mode Strap:
**Pull Up : Disable (default)
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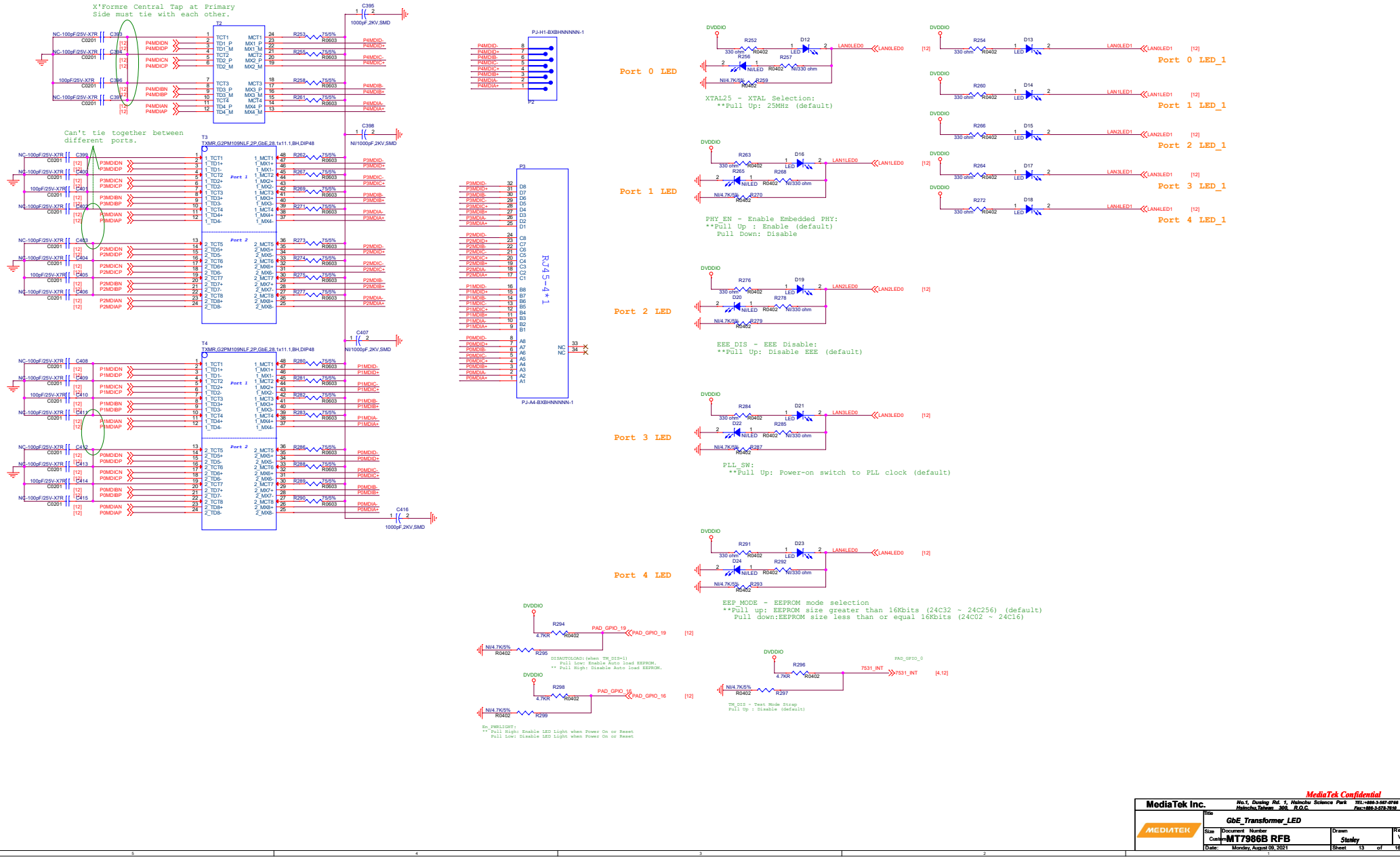
Hsinchu,Taiwan 300, R.O.C.
MT7531AE_Giga Switch
MT7986B RFB
Steven
Monday, August 09, 2021
Sheet 12 of 15



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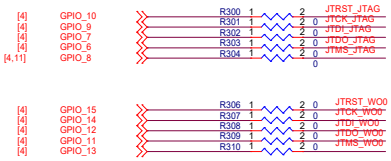
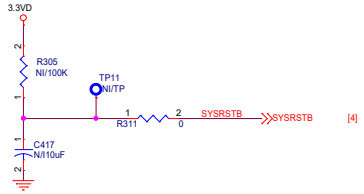
Title: GbE_Transformer_LED			
Size: Custom	Document Number: MT7986B RFB	Drawn: Stanley	Rev: V10
Date: Monday, August 09, 2021		Sheet 13 of 16	

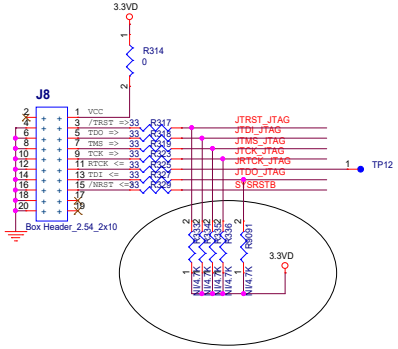
JTAG



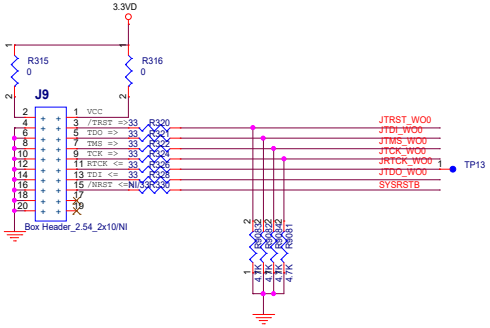

```
GPIO_6 JTAG_JTDO
GPIO_7 JTAG_JTDI
GPIO_8 JTAG_JTMS
GPIO_9 JTAG_JTCLK
GPIO_10 JTAG_JTRST_N
GPIO_11 WO0_JTAG_JTDO
GPIO_12 WO0_JTAG_JTDI
GPIO_13 WO0_JTAG_JTMS
GPIO_14 WO0_JTAG_JTCLK
GPIO_15 WO0_JTAG_JTRST_N
```



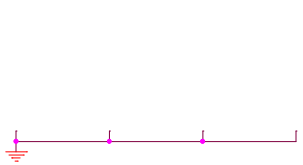
default- JTAG_CA53
sw confiig for WM0

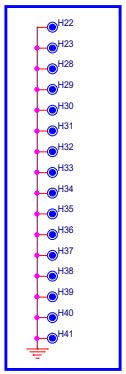


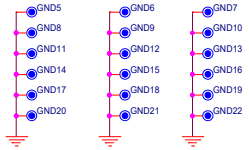
default- JTAG_WO0
swconfiig for WM1/WO1



Reserved for debug







Shielding frame Hole

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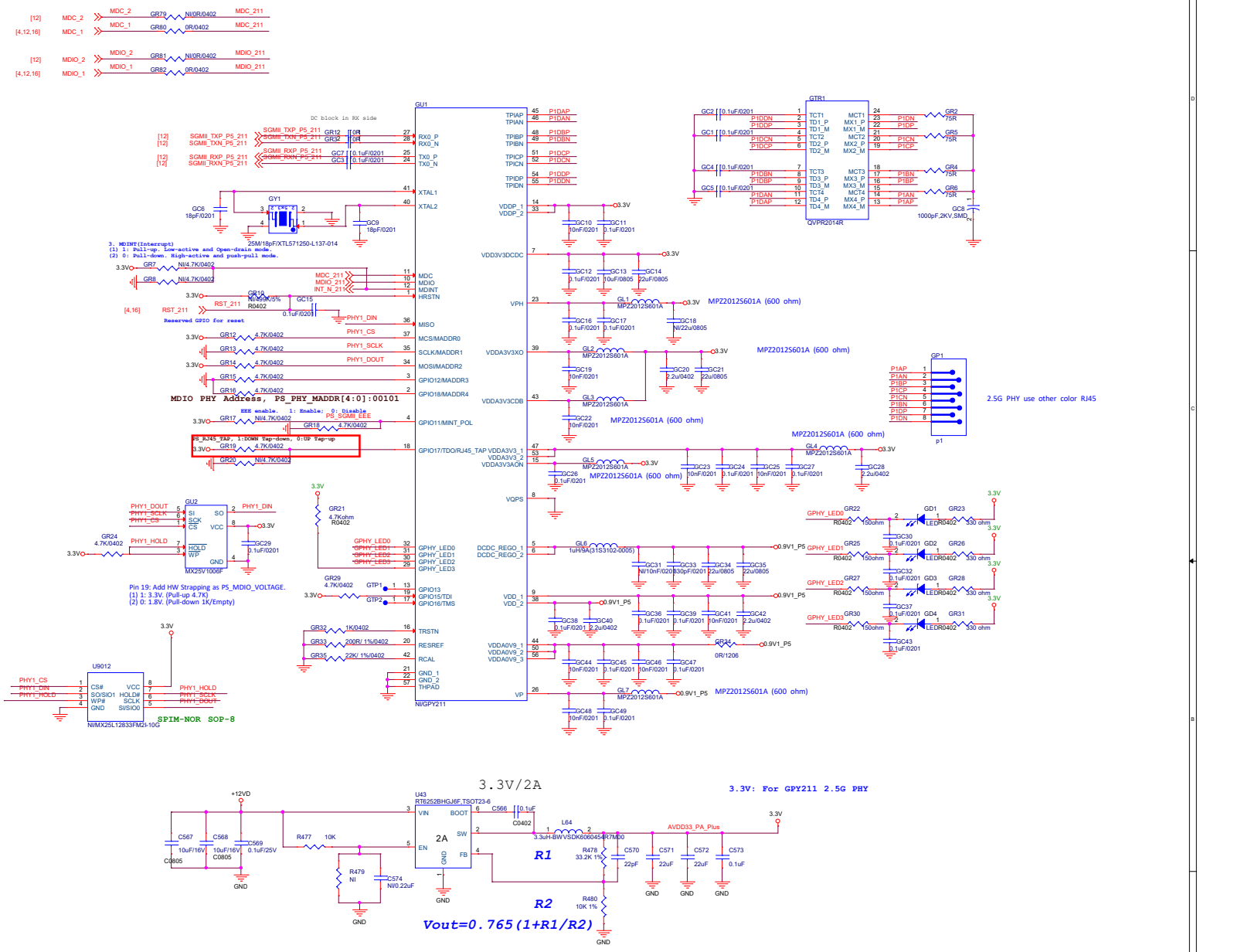
Title: JTAG			
Size: C	Document Number: MT7986B RFB	Drawn: Steven	Rev: V10
Date: Monday, August 09, 2021		Sheet 14 of 16	


MDC_2
MDC_1
MDIO_2
MDIO_1
GU1
XTAL1
XTAL2
MDIO PHY Address, PS_PHY_MADDR[4:0]:00101
Reserved GPIO for reset
MISO
MCS/MADDR0
SCLK/MADDR1
MOSI/MADDR2
GPIO12/MADDR3
GPIO18/MADDR4
GPIO11/MINT_POL
GPIO17/TDO/RJ45_TAP
TRSTN
RESREF
RCAL
NI/GPY211
GTR1
QVPR2014R
GP1
2.5G PHY use other color RJ45
MPZ2012S601A (600 ohm)
GU2
MX25V1006F
SPIM-NOR SOP-8
U9012
NI/MX25L12833FM2I-10G
3.3V/2A
3.3V: For GPY211 2.5G PHY
U43
RT8252BHGJ6F,TSOT23-6
R1
R2
Vout=0.765(1+R1/R2)
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MediaTek Inc.
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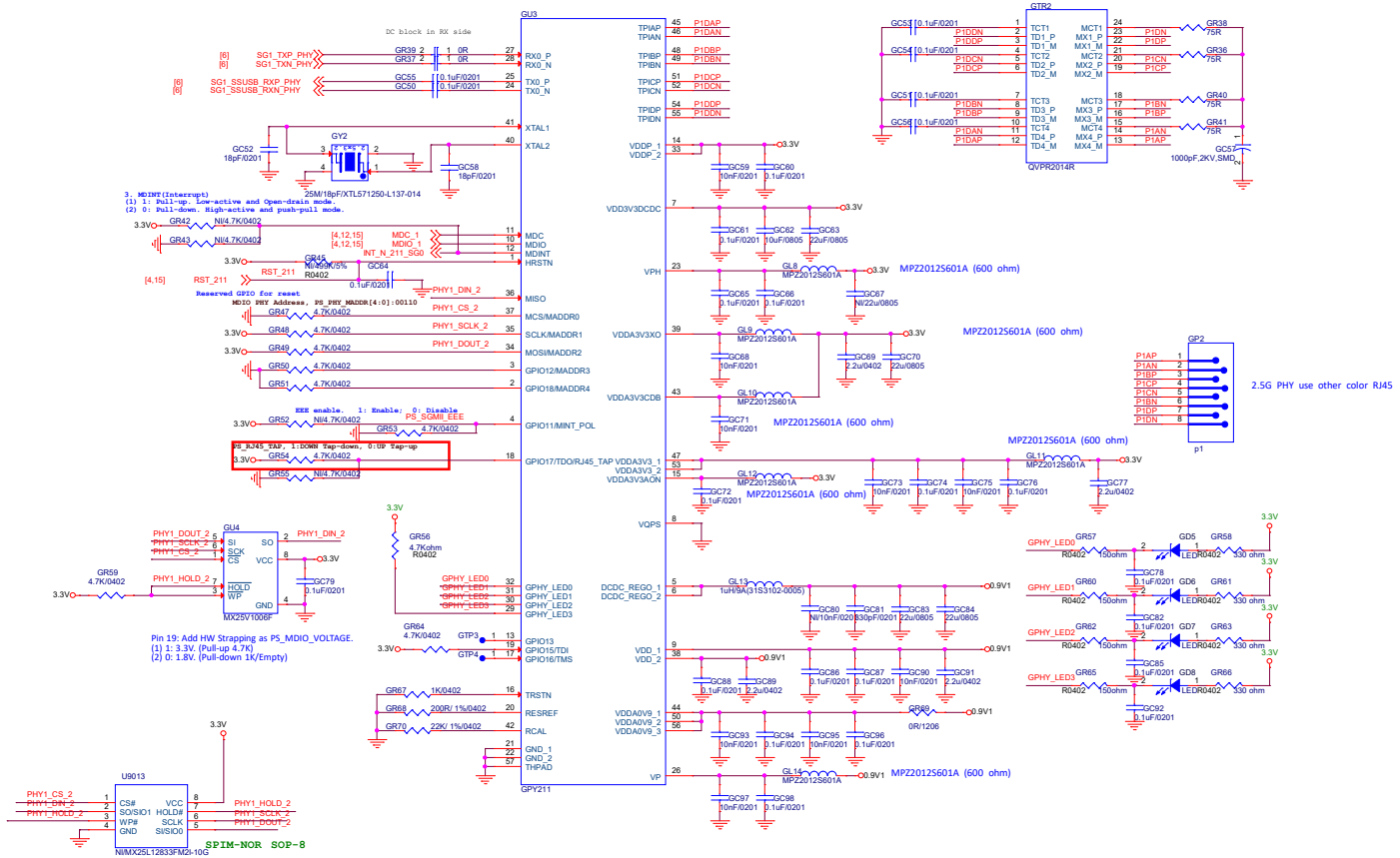
TEL:+886-3-567-0766
Fax:+886-3-578-7610
Intel GPY211 2.5GPHY
MT7986B RFB
Steven
Monday, August 09, 2021



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MEDIATEK	Title: Intel GPY211 2.5GPHY		
	Size: Custom	Document Number: MT7986 RFB	Drawn: Steven
	Date: Monday, August 09, 2021	Sheet 16 of 16	Rev V10