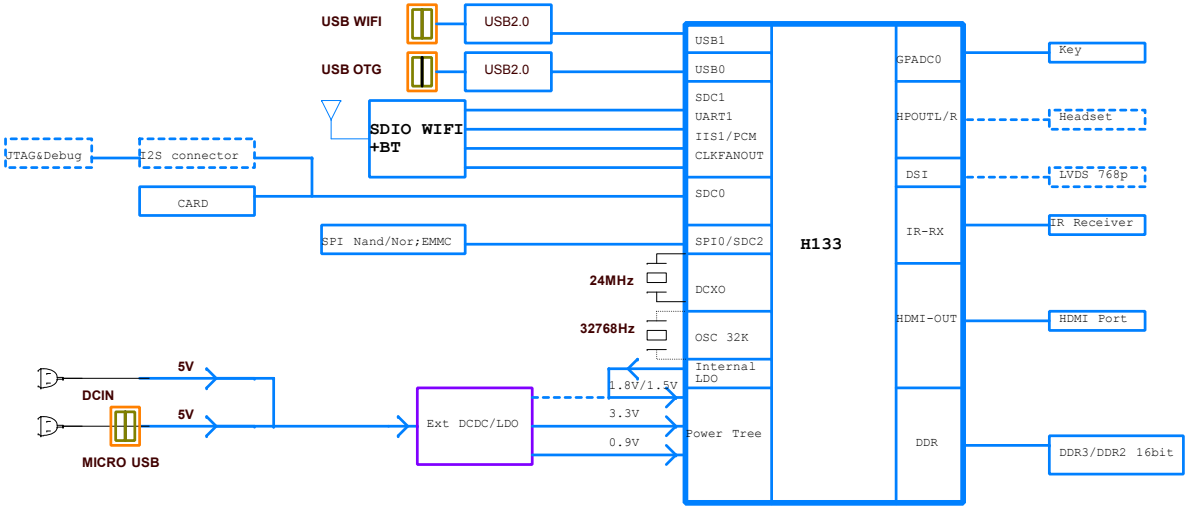
VERSION HISTORY

Index:

Revision	Description	Date	Drawn	Checked	Approved
Ver 0.1	Releas version	2020-12-31			
Ver 1.0	AddAW859 Add UART2 /5 and SPI test point	2021-04-07	YJY	JIAYONG	YINWEI
Ver 1.1	ADD DDR2 ADD FALE FEL KEY ADD USB WIFI ADD DCDC4 for dram	2021-11-21	WJH	YJY	YINWEI
Ver 1.2	Merge VDD-CPU and vdd-SYS VCC-DRAM change to ext DCDC	2022-01-05	WJH	YJY	YINWEI
Ver 1.3	Change the DCDC-EN for power -sequency in Merge VDD-CPU AND VDD-SYS.	2022-02-25	WJH	YJY	YINWEI
Ver 1.4	DELETE SPDIF IN Fuction Delete SGM809	2022-04-12	WJH	YJY	YINWEI

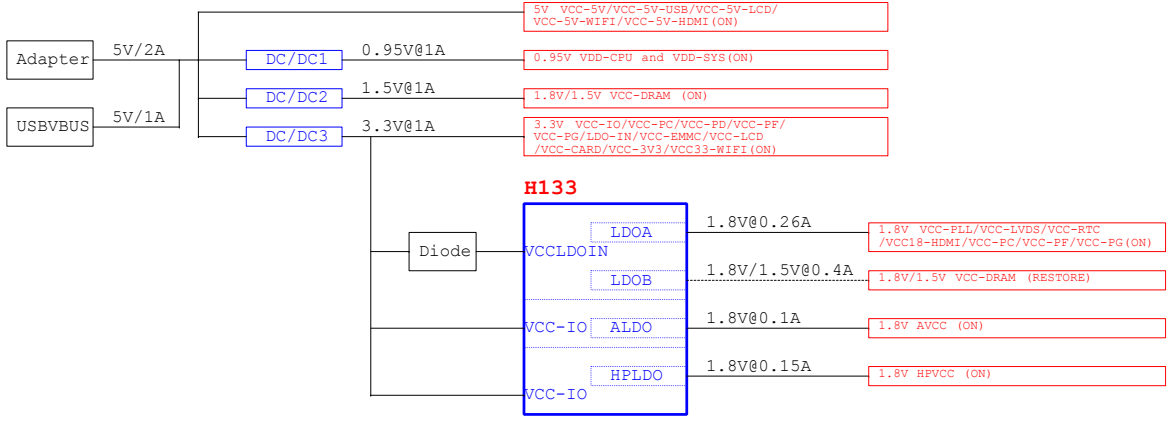
BLOCK



AllWinner Technology Co.,Ltd		
Design Name: H133_DONGLE_STD		
Size: A3	Page Name: 02 BLOCK DIAGRAM	Rev
Date: Friday, April 15, 2022	Sheet 2 of 12	

DEFAULT POWER ON

DEFAULT POWER OFF



AllWinner Technology Co.,Ltd		
Design Name: H133_DONGLE_STD		
Size: A3	Page Name: 03 POWER TREE	Rev
Date: Friday, April 15, 2022	Sheet 3 of 12	

GPIO ASSIGNMENT

Ball Number	Ball Name	GPIO Multiplex Function
D15	PB0	PWM3/IR_TX/TWI2_SCK/SPI1_WP/DBI_TE/UART0_TX/UART2_TX/SPDIF_OUT/PB_EINT0
D14	PB1	PWM4/I2S2_DOUT3/TWI2_SDA/I2S2_DIN3/UART0_RX/UART2_RX/IR_RX/PB_EINT1
D13	PB8	DMIC_DATA3/PWM5/TWI2_SCK/SPI1_HOLD/DBI_DCX/DBI_WRX/ UART0_TX/UART1_TX/PB_EINT8
C14	PB9	DMIC_DATA2/PWM6/TWI2_SDA/SPI1_MISO/DBI_SDI/DBI_TE/DBI_DCX/ UART0_RX/UART1_RX/PB_EINT9
C13	PB10	DMIC_DATA1/PWM7/TWI0_SCK/SPI1_MOSI/DBI_SDO/CLK_FANOUT0/ UART1_RTS/PB_EINT10
B15	PB11	DMIC_DATA0/PWM2/TWI0_SDA/SPI1_CLK/DBI_SCLK/CLK_FANOUT1/ UART1_CTS/PB_EINT11
B14	PB12	DMIC_CLK/PWM0/SPDIF_IN/SPI1_CS/DBI_CSX/CLK_FANOUT2/IR_RX/PB_EINT12

Ball Number	Ball Name	GPIO Multiplex Function
F3	PC2	SPI0_CLK/SDC2_CLK/PC_EINT2
F2	PC3	SPI0_CS0/SDC2_CMD/PC_EINT3
F1	PC4	SPI0_MOSI/SDC2_D2/BOOT_SEL0/PC_EINT4
G3	PC5	SPI0_MISO/SDC2_D1/BOOT_SEL1/PC_EINT5
G2	PC6	SPI0_WP/SDC2_D0/UART3_TX/TWI3_SCK/DBG_CLK/PC_EINT6
H3	PC7	SPI0_HOLD/SDC2_D3/UART3_RX/TWI3_SDA/TCON_TRIG/PC_EINT7

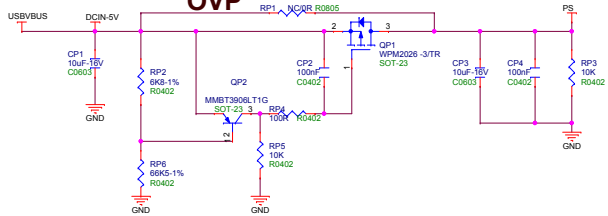
Ball Number	Ball Name	GPIO Multiplex Function
N15	PD0	LCD0_D2/LVDS0_V0P/DSI_D0P/TWI0_SCK/PD_EINT0
N14	PD1	LCD0_D3/LVDS0_V0N/DSI_D0N/UART2_TX/PD_EINT1
M15	PD2	LCD0_D4/LVDS0_V1P/DSI_D1P/UART2_RX/PD_EINT2
M14	PD3	LCD0_D5/LVDS0_V1N/DSI_D1N/UART2_RTS/PD_EINT3
L15	PD4	LCD0_D6/LVDS0_V2P/DSI_CKP/UART2_CTS/PD_EINT4
L14	PD5	LCD0_D7/LVDS0_V2N/DSI_CKN/UART5_TX/PD_EINT5
K15	PD6	LCD0_D10/LVDS0_CKP/DSI_D2P/UART5_RX/PD_EINT6
K14	PD7	LCD0_D11/LVDS0_CKN/DSI_D2N/UART4_TX/PD_EINT7
J15	PD8	LCD0_D12/LVDS0_V3P/DSI_D3P/UART4_RX/PD_EINT8
J14	PD9	LCD0_D13/LVDS0_V3N/DSI_D3N/PWM6/PD_EINT9

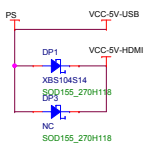
Ball Number	Ball Name	GPIO Multiplex Function
B8	PG0	SDC1_CLK/UART3_TX/RGMII_RXCTRL/RMII_CRS_DV/PWM7/PG_EINT0
C9	PG1	SDC1_CMD/UART3_RX/RGMII_RXD0/RMII_RXD0/PWM6/PG_EINT1
A8	PG2	SDC1_D0/UART3_RTS/RGMII_RXD1/RMII_RXD1/UART4_TX/PG_EINT2
B7	PG3	SDC1_D1/UART3_CTS/RGMII_TXCK/RMII_TXCK/UART4_RX/PG_EINT3
A6	PG4	SDC1_D2/UART5_TX/RGMII_TXD0/RMII_TXD0/PWM5/PG_EINT4
C7	PG5	SDC1_D3/UART5_RX/RGMII_TXD1/RMII_TXD1/PWM4/PG_EINT5
B4	PG6	UART1_TX/TWI2_SCK/RGMII_TXD2/PWM1/PG_EINT6
A3	PG7	UART1_RX/TWI2_SDA/RGMII_TXD3/SPDIF_IN/PG_EINT7
B3	PG8	UART1_RTS/TWI1_SCK/RGMII_RXD2/UART3_TX/PG_EINT8
A2	PG9	UART1_CTS/TWI1_SDA/RGMII_RXD3/UART3_RX/PG_EINT9
C4	PG10	PWM3/TWI3_SCK/RGMII_RXCK/CLK_FANOUT0/IR_RX/PG_EINT10
B6	PG11	I2S1_MCLK/TWI3_SDA/EPHY_25M/CLK_FANOUT1/TCON_TRIG/PG_EINT11
C6	PG12	I2S1_LRCK/TWI0_SCK/RGMII_TXCTRL/RMII_TXEN/CLK_FANOUT2/PWM0/UART1_TX/PG_EINT12
B5	PG13	I2S1_BCLK/TWI0_SDA/RGMII_CLKIN/RMII_RXER/PWM2/LEDC_DO/UART1_RX/PG_EINT13
C5	PG14	I2S1_DIN0/TWI2_SCK/MDC/I2S1_DOUT1/SPI0_WP/UART1_RTS/PG_EINT14
A4	PG15	I2S1_DOUT0/TWI2_SDA/MDIO/I2S1_DIN1/SPI0_HOLD/UART1_CTS/PG_EINT15
B2	PG16	IR_RX/TCON_TRIG/PWM5/CLK_FANOUT2/SPDIF_IN/LEDC_DO/PG_EINT16
C10	PG17	UART2_TX/TWI3_SCK/PWM7/CLK_FANOUT0/IR_TX/UART0_TX/PG_EINT17
B9	PG18	UART2_RX/TWI3_SDA/PWM6/CLK_FANOUT1/SPDIF_OUT/UART0_RX/PG_EINT18

Ball Number	Ball Name	GPIO Multiplex Function
B1	PF0	SDC0_D1/JTAG_MS/R_JTAG_MS/I2S2_DOUT1/I2S2_DIN0/PF_EINT0
C3	PF1	SDC0_D0/JTAG_DI/R_JTAG_DI/I2S2_DOUT0/I2S2_DIN1/PF_EINT1
C2	PF2	SDC0_CLK/UART0_TX/TWI0_SCK/LEDC_DO/SPDIF_IN/PF_EINT2
D3	PF3	SDC0_CMD/JTAG_DO/R_JTAG_DO/I2S2_BCLK/PF_EINT3
D2	PF4	SDC0_D3/UART0_RX/TWI0_SDA/PWM6/IR_TX/PF_EINT4
D1	PF5	SDC0_D2/JTAG_CK/R_JTAG_CK/I2S2_LRCK/PF_EINT5
E2	PF6	SPDIF_OUT/IR_RX/I2S2_MCLK/PWM5/PF_EINT6

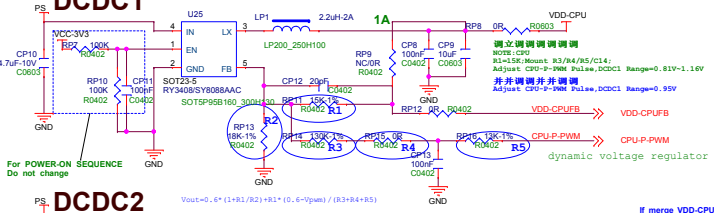
POWER

5V DCIN TO PS OVP

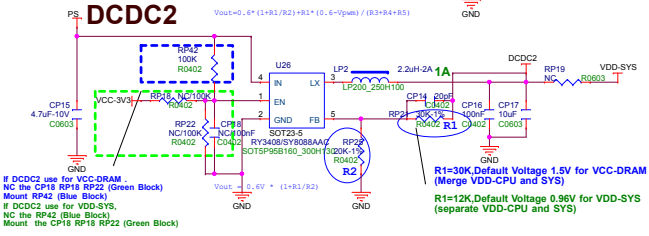


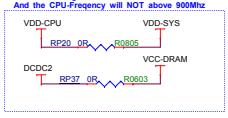


DCDC1

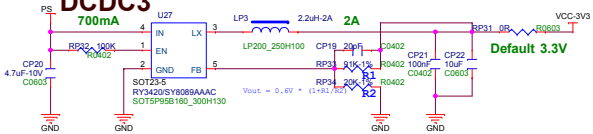


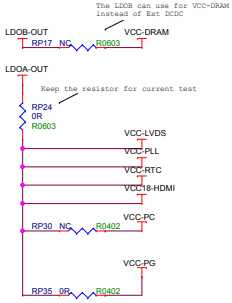
DCDC2

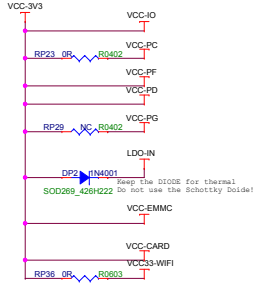




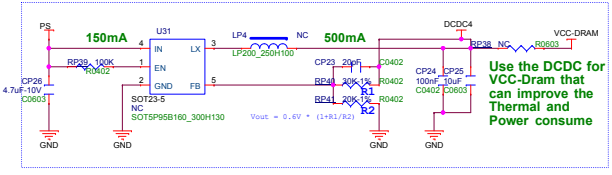
DCDC3







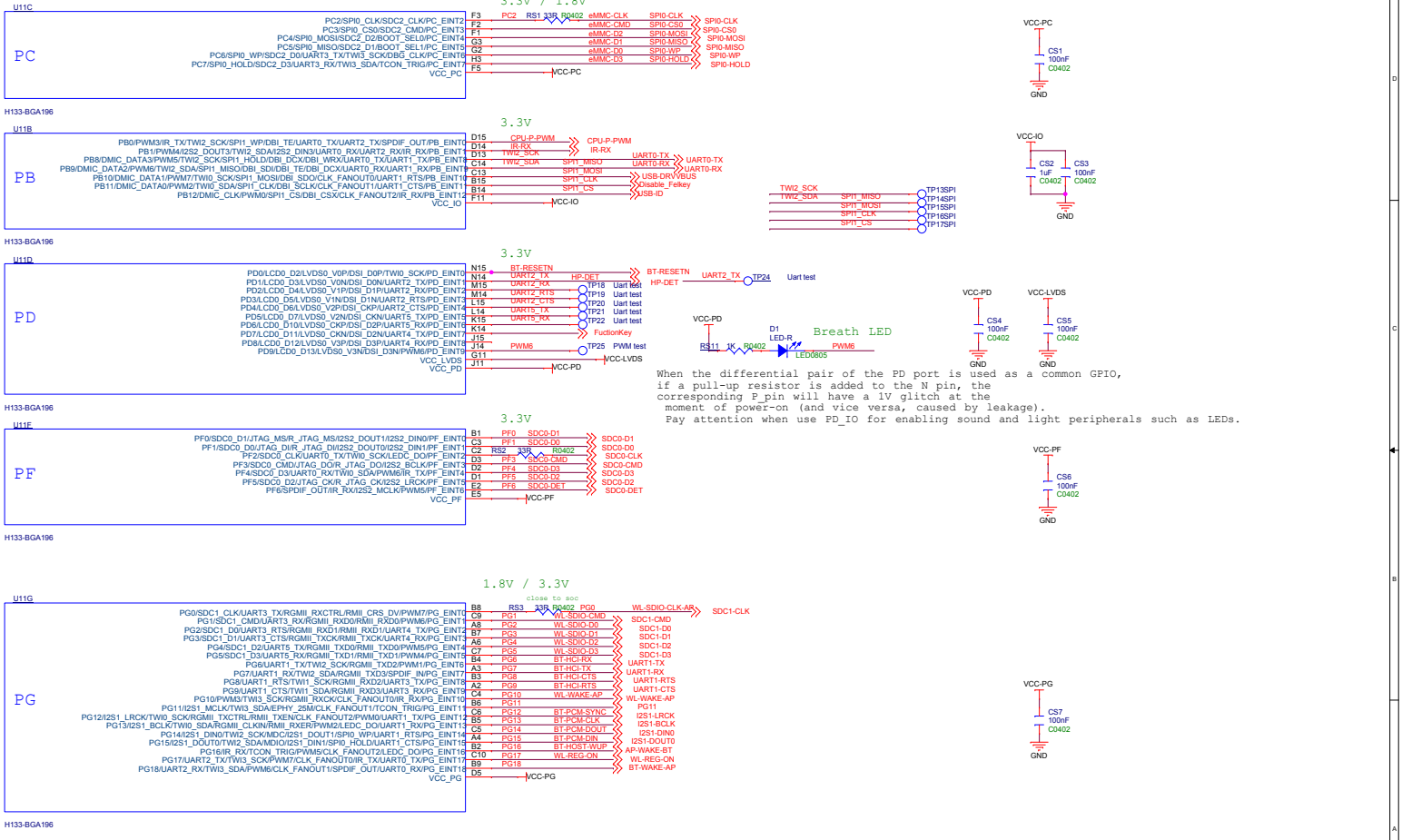
DCDC4



	DCDC1 (EXT)	DCDC2 (EXT)	DCDC3 (EXT)	DCDC4 (EXT)	LDOB (IN)	LDOA (IN)	REMARK
Default PLAN	VDD-CPU VDD-SYS (0.95V)	VCC-DRAM 1.5/1.8V	VCC-WIFI VCC-3V3 LDOIN	NC	NC	VCC-PLL VCC-RTC VCC-1V8	Merge VDD-CPU and VDD-SYS ,that Cpu-fregency below 900Mhz.The Power comsume is below2.5W@4K30,And the thermal will be very low.
Performance PLAN	VDD-CPU (0.8~ 1.16V)	VDD-SYS 0.9V	VCC-WIFI VCC-3V3 LDOIN	VCC-DRAM 1.5/1.8V	NC	VCC-PLL VCC-RTC VCC-1V8	Separate VDD-CPU and VDD-SYS ,The Cpu-fregency upon to 1.2Ghz .The Power comsume is below2.5W@4K30, And the thermal will be very low.
Econormy PLAN	VDD-CPU VDD-SYS (0.95V)	NC	VCC-WIFI VCC-3V3 LDOIN	NC	VCC-DRAM 1.5/1.8V	VCC-PLL VCC-RTC VCC-1V8	Merge VDD-CPU and VDD-SYS ,that Cpu-fregency below 900Mhz.VCC-Dram be supplied by internal LDOB,instead of Ext DCDC.

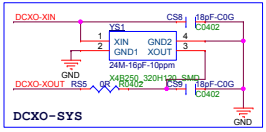
AllWinner Technology Co.,Ltd
Design Name: H133_DONGLE_STD
Size: Custom
Page Name: 05 POWER
Rev:
Date: Friday, April 15, 2022
Sheet 5 of 12

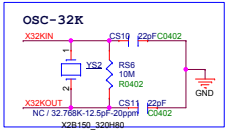
SOC1

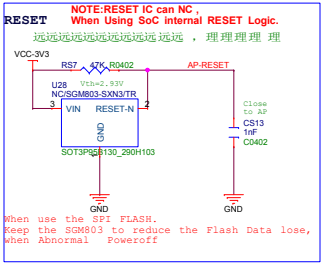


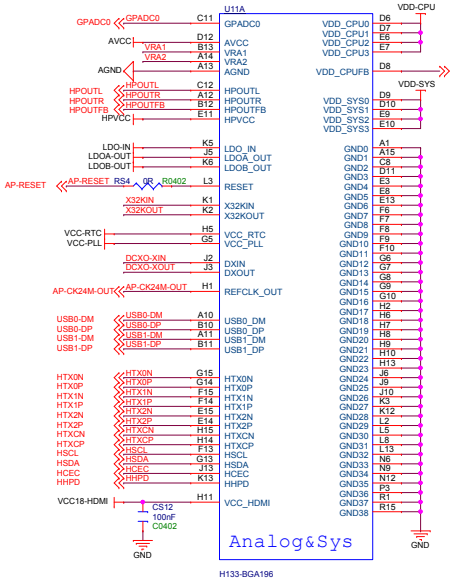
AllWinner Technology Co.,Ltd			
Design Name: H133_DONGLE_STD			
Size: A3	Page Name: 07 SOC1		Rev
Date: Wednesday, April 20, 2022	Sheet 6 of 12		

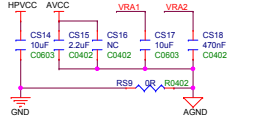
SOC2

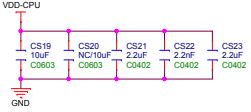


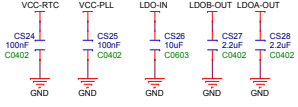


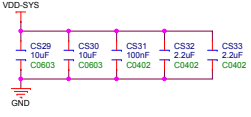






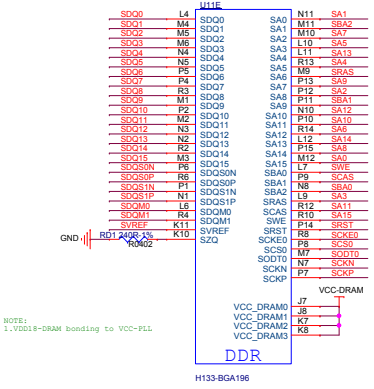


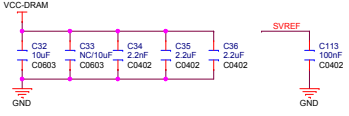


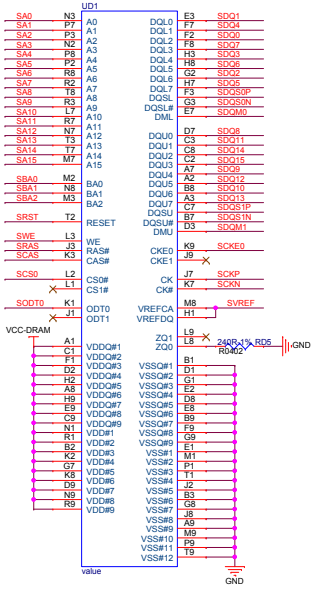


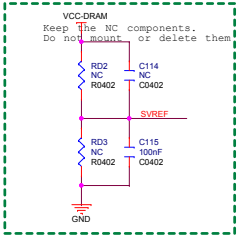
AllWinner Technology Co.,Ltd		
Design Name: H133_DONGLE_STD		
Size: A3	Page Name: 08 SOC2	Rev
Date: Friday, April 15, 2022	Sheet 7 of 12	

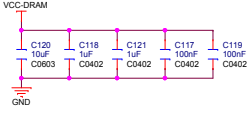
DDR3





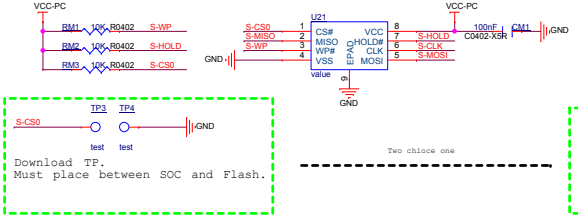




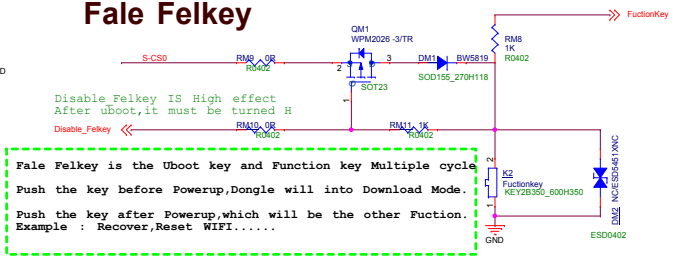


AllWinner Technology Co.,Ltd			
Design Name: H133_DONGLE_STD			
Size: A3	Page Name: 09 DDR3		Rev
Date: Friday, April 15, 2022	Sheet 8 of 12		

SPI



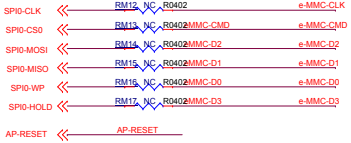
Fale Felkey

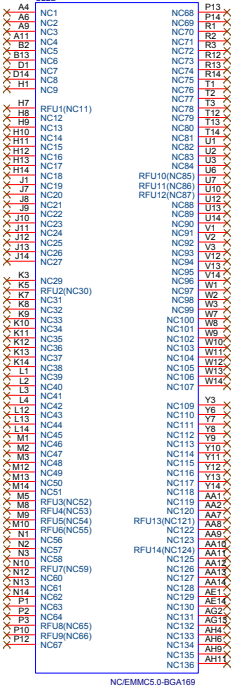


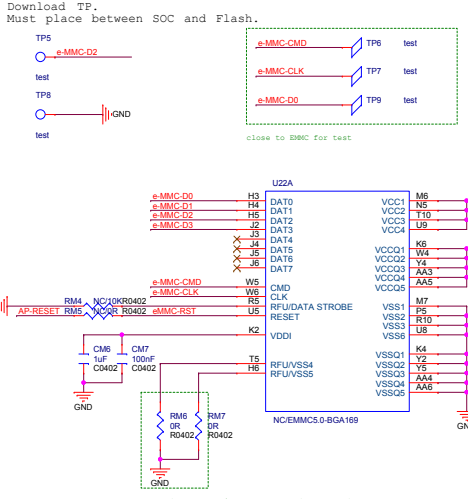
EMMC

SPI FLASH and EMMC only can chioce one of them.

Both Layout in PCB will effect the SI

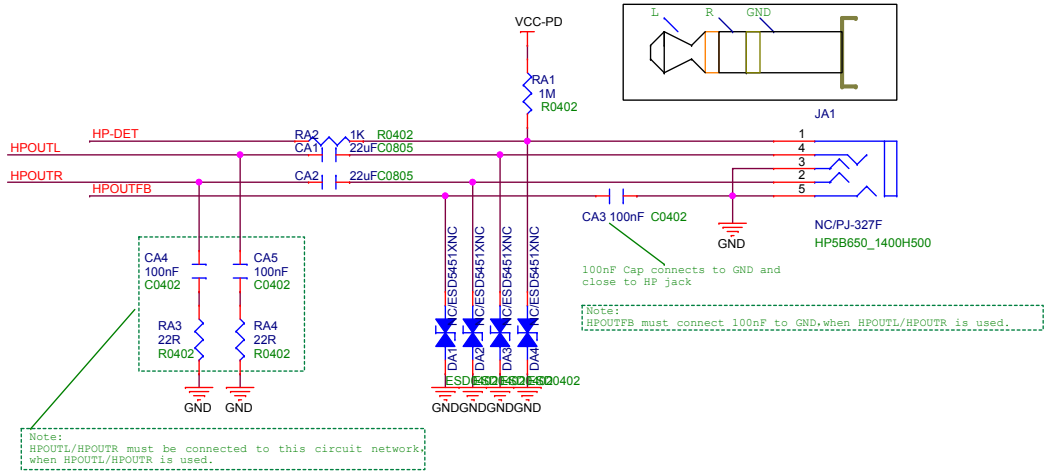






AllWinner Technology Co.,Ltd		
Design Name: H133_DONGLE_STD		
Size: A3	Page Name: 10 FLASH	Rev
Date: Friday, April 15, 2022	Sheet 9 of 12	

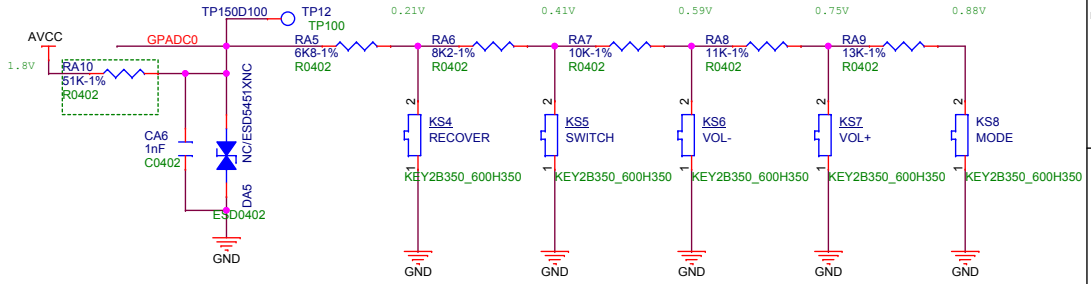
Audio



HP-DET

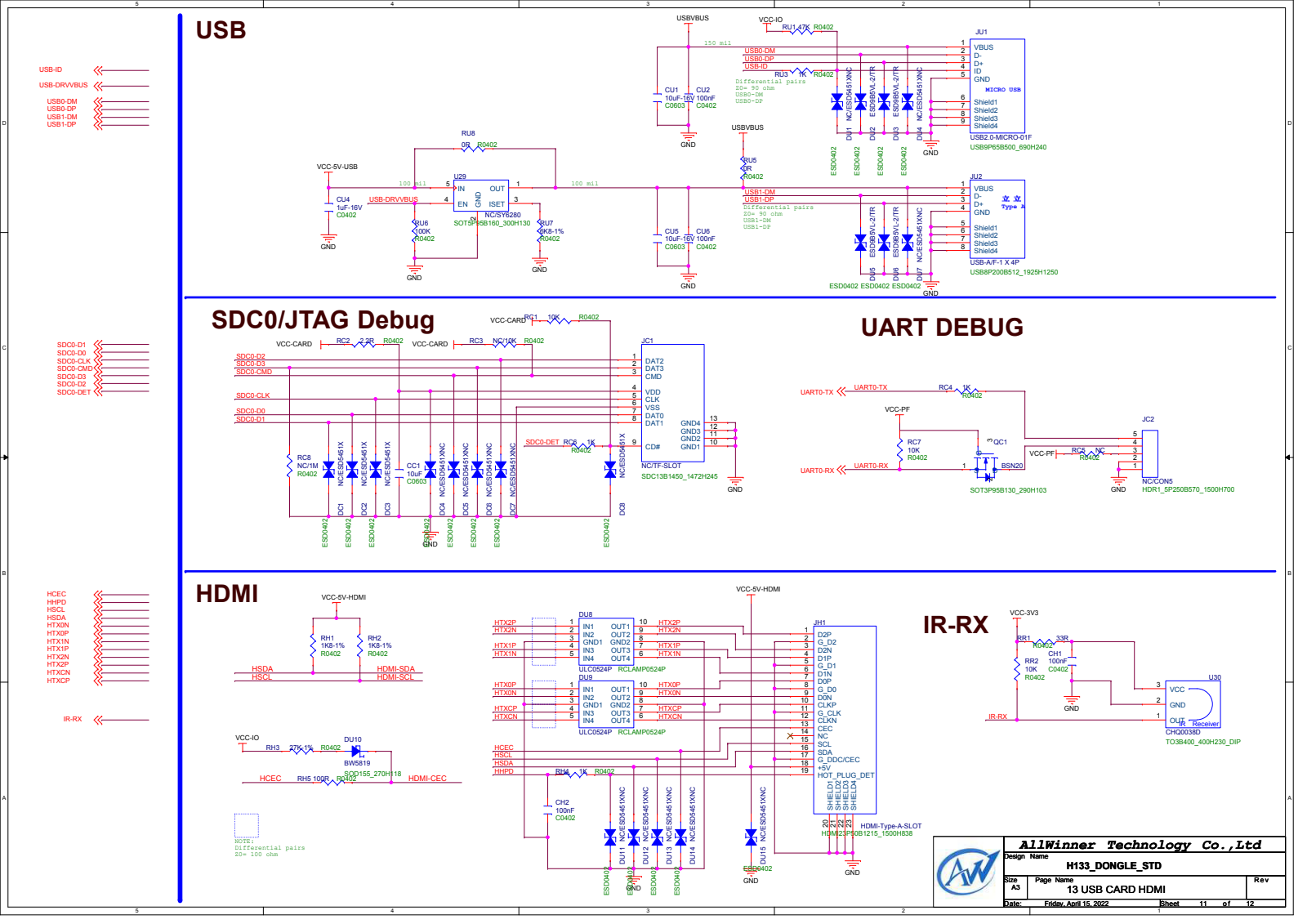
HPOUTFB
HPOUTL
HPOUTR

KEY ADC



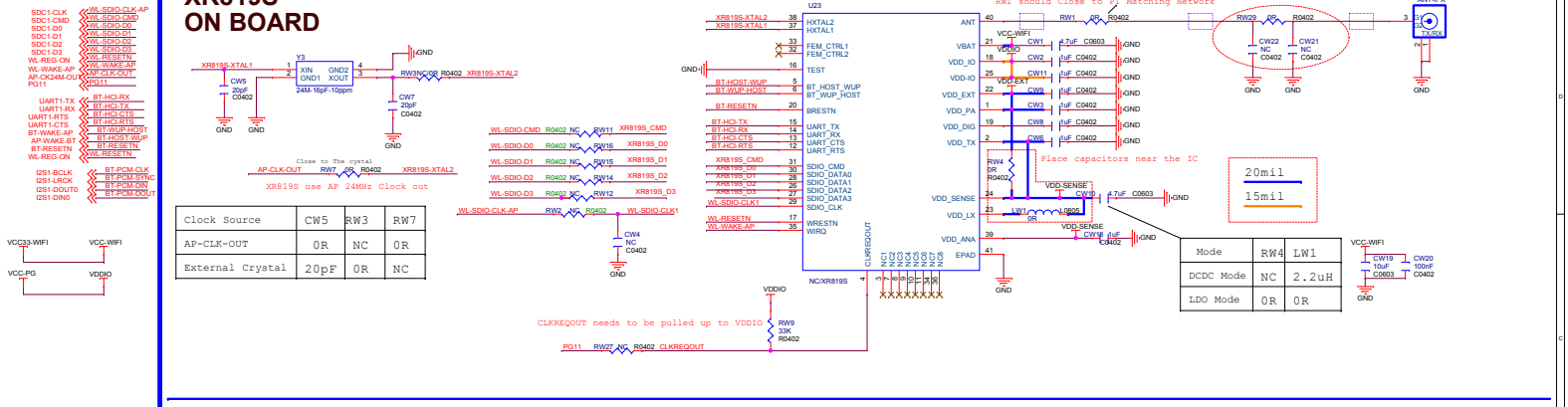
GPADC0

AllWinner Technology Co.,Ltd		
Design Name: H133_DONGLE_STD		
Size: A4	Page Name: 12 AUDIO & KEY	Rev
Date: Friday, April 15, 2022	Sheet 10 of 12	



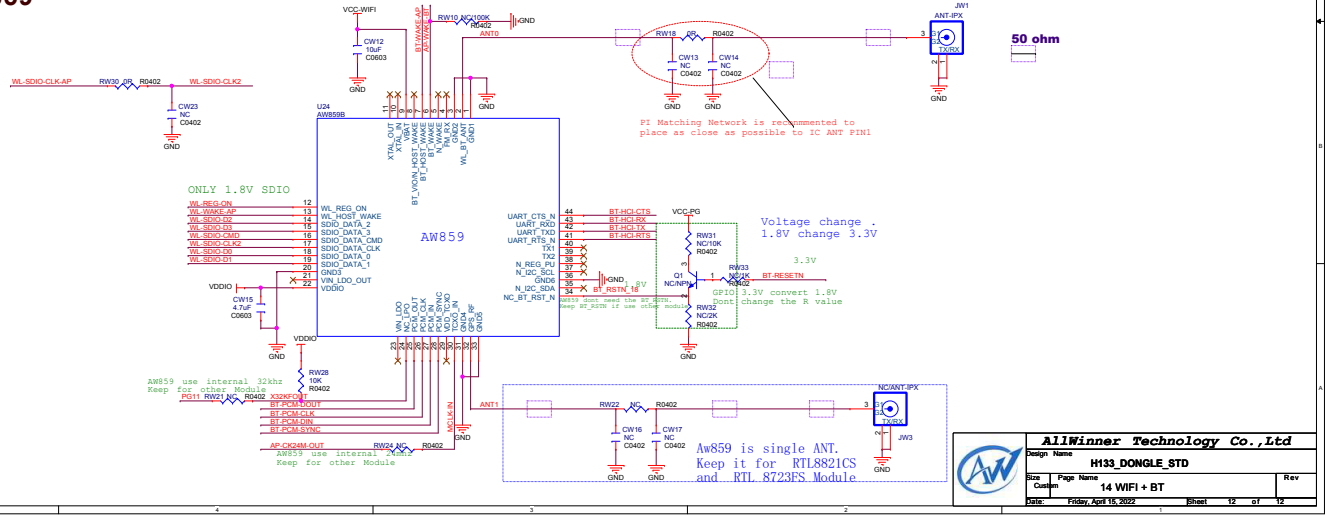
AllWinner Technology Co.,Ltd			
Design Name	H133_DONGLE_STD		
Size A3	Page Name 13 USB CARD HDMI		Rev
Date: Friday, April 15, 2022	Sheet 11 of 12		

XR819S ON BOARD



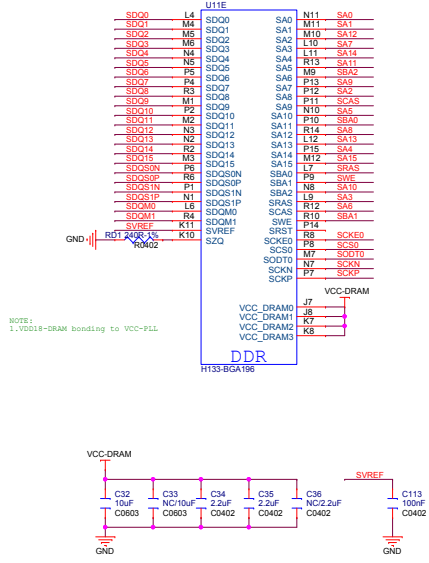
Clock Source	CW5	RW3	RW7
AP-CLK-OUT	0R	NC	0R
External Crystal	20pF	0R	NC

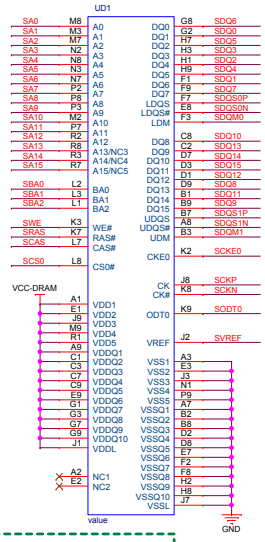
AW859

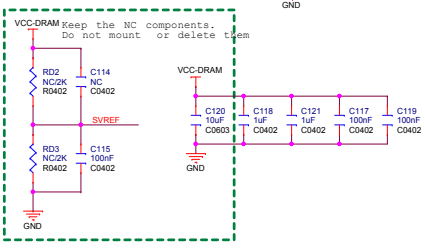


AllWinner Technology Co.,Ltd		
Design Name: H133_DONGLE_STD		
Size: Custom	Page Name: 14 WIFI + BT	Rev
Date: Friday, April 15, 2022	Sheet 12 of 12	

DDR2







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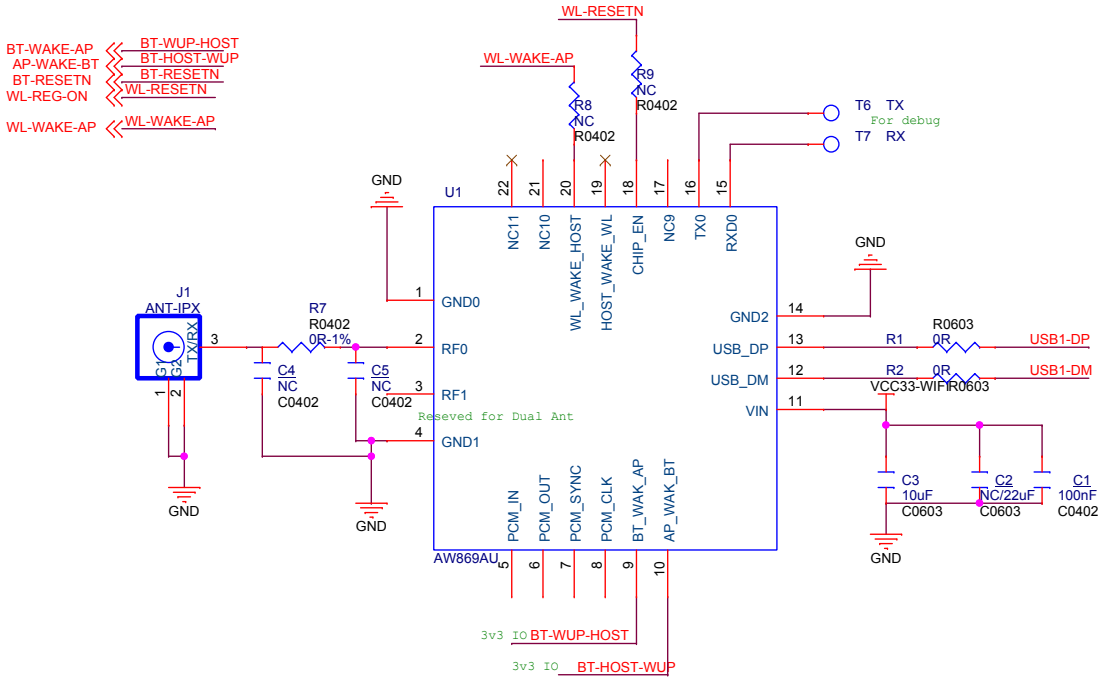
Design Name: H133_DONGLE_STD		
Size: A3	Page Name: 13 DDR2	Rev
Date: Friday, April 15, 2022	Sheet 13 of 14	

USB WIFI



AllWinner Technology Co.,Ltd		
Design Name: H133_DONGLE_STD		
Size: A	Page Name: 14 USB_WIFI_AW869au	Rev:
Date: Friday, April 15, 2022	Sheet 14 of 14	