

UIS8910DM Device Specification

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Revision History

Version	Date	Owner	Note
0.1	7/26/2018	JM Gao	First draft.
0.2	12/07/2018	Jackie Li	Update for UIS8910DM.

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1 System Overview

1.1 General Description

UIS8910DM is an advanced system-on-chip solution integrated CAT1bis/GSM/GPRS modems. Building on the success of UNISOC's current solutions, the UIS8910DM integrates RF transceiver and Bluetooth RF for low cost.

UIS8910DM supports plenty of peripherals such as SDIO, UART, I2C, SPI, I2S, MIPI CSI, and GPIOs. Full custom power management chip provides power to SOC and all peripherals.

To meet the increasing popular power-saving requirements without the use of additional hardware, UIS8910DM has an ultra-low power standby solution that an embedded power-FSM can perform standby events and wake up the system as required.

UIS8910DM 8.9X8.9mm TFBGA package and 301 balls.

1.2 Features

1.2.1 Platform Features

Microcontroller Subsystem

- 500MHz Cortex A5 Application processor with 32KB ICache and 32KB DCache, NEON/FPU
- Three(3) Boot modes
 - Normal : Boot from Nor-flash
 - Boot from SD card
 - Force download(UART2 or USB)
- Twelve general DMA channels for peripherals and one dedicated channel for debug host
- Multiple SoC low power modes with rich wakeup sources

Memory

- Integrated SPI Nor Flash(64Mb) and PSRAM(128Mb)
- 4K-bit E-fuse

WCN Subsystem

- Support Bluetooth 4.2 true dual mode(BR/EDR and BLE)
- Support WIFI 802.11b Rx only(RSSI and MAC Address for Location)
- Support FM
- Integrated balun for RF

User Interface

- 1 Pulse Width Modulator
- Up to 32 GPIOs with interrupt function
- 3 UART interface
- 2 SDIO interface
- 3 I2C interface
- 2 I2S(slave) interface

- 2 SPI(master) interface
- Up to 6 column x 6 row keypad
- GPIO0-5 can be used to extend external flash
- USB2.0

Power Management

- External DC-DC and LDOs solution(PMIC UIP8910M) deriving from VBAT
- Flexible I/O voltage
- External pin reset

Clock Source

- 26MHz VC-TCXO or TSX
- 32KHz crystal oscillator or 32K-less

1.2.2 Modem Features

CAT1bis Communication

- 3GPP Release 13
- Supports FDD, TDD
- Supports 1.4/3/5/10/15/20MHz bandwidth in downlink and uplink
- Up to UL/DL 5Mbps/10Mbps respectively
- Support VoLTE

GSM/GPRS

- Dual differential LNAs support quad band receiver
- Fully integrated channel filter
- High dynamic range ADC
- Transmitter support quad band
- Programmable fractional-N synthesizer
- On die wide range VCO and integrated loop filter
- Fast settling time suitable for multi-slot GPRS applications
- Low power mode support 32KHz crystal removal
- GPRS Class 12
- Support HR/FR/EFR voice codec

1.2.3 Multi-media Features

Audio Processor

- ZSP900m processor
- L1 cache(32KB ICache and 32KB DCache)

Audio Interface

- Support AUD interface
- Support I2S(slave) interface

Camera

- Support serial port up to 2 data-line VGA@15fps
- Support MIPI CSI port up to 1 lane VGA@30fps
- 0.3M ISP integrated

Display

- Support 4 wire 8 bit I / II type LCD
- Support 3 wire 9 bit I / II type LCD
- Support 3 wire 9 bit 2 data-line LCD
- Support SPI 3 or 4 wires mode up to QVGA@30fps
- Support 1 lane MIPI DSI Interface up to VGA@30fps

Video Codec

- Support MJPEG QVGA@15fps encoder
- Support H.264, H.263, MPEG4, MJPG HVGA@25fps decoder

1.3 Chip Architecture

The following figure shows UIS8910DM chip architecture.

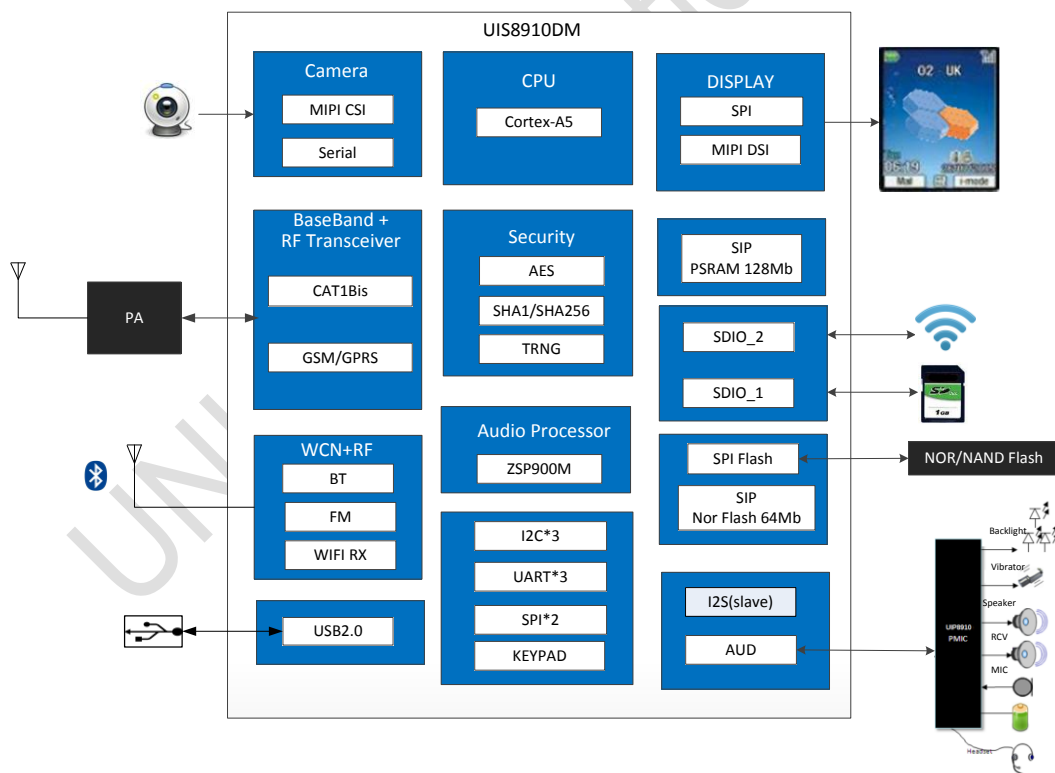


Figure 1-1 Chip Architecture

2 Package Information

2.1 Top Marketing Definition

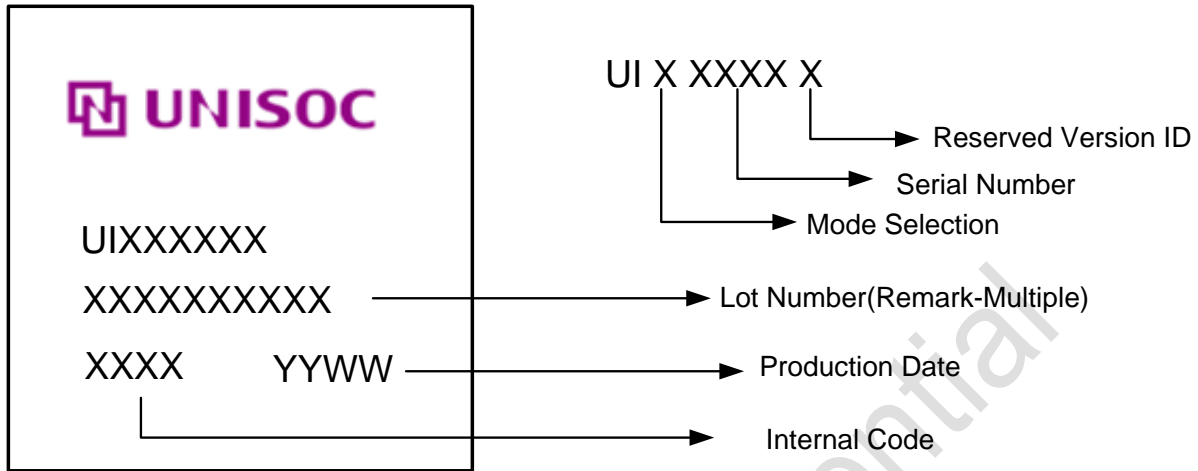


Figure 2-1 Top Marketing Definition

2.2 BGA Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22			
A	AI_NC	RF_VIP_L TE_LB	RF_VIP_L TE_LB	RF_VIN_L TE_MB	RF_VIP_L TE_HB	RF_VIP_L TE_MB	RFOUT_GS MH	RFOUT_LB 1	RFOUT_LB 2	RFOUT_HB 1	AVSS_RF	RFDIG_GP 10_0	RFDIG_GP 10_1	RFDIG_GP 10_2	RFDIG_GP 10_3	RFDIG_GP 10_4	RFDIG_GP 10_5	RFDIG_GP 10_6	RFDIG_GP 10_7	AVDD15_R X_WCN	AVSS_WCN	FM_RFIP	WB_RFIP	AVDD15_T XRF_WCN	A22_NC
B	RF_VIP_G SM_HB	RF_VIN_L TE_LB	RF_VIP_L TE_LB	RF_VIN_L TE_LB	RF_VIN_L TE_HB	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVDD15_C LK_WCN	KEYIN_0
C	RF_VIN_G SM_HB	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	KEYIN_1
D	RF_VIP_G SM_LB	RF_VIN_G SM_LB	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	KEYIN_4
E		AVDD15_R X	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	KEYIN_5
F	RAMP_OUT	TSEN_IN	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	KEYOUT_1
G	TSEN_VRE FP	TSEN_VRE FN	VI_AUXAD C	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	KEYOUT_2
H	XTAL1	AVSS_RF	APC_OUT	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	KEYOUT_3
J	XTAL2	AVDD18_D CXO	CLK26M_A UX1	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	KEYIN_2
K		CLK26M_P MTC	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	KEYIN_3
L	OSC_32K	GP10_6	CHIP_PD	UART_1_R XD	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	KEYOUT_0
M	AD1_SDA	AD1_SCL	AUD_SCLK	UART_1_T XD	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	KEYIN_0
N					V_SIM1	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	V_PAD_1V 8_RTC	KEYIN_1
P	AD1_SIN0																								KEYIN_2
R	RESETB	AUD_DA_0 S_VNC	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	V_PAD_1V 8_1	KEYIN_3
T	AUD_DA_0 S_VNC	AUD_DA_0 S_VNC																							KEYIN_4
U	AUD_AD_0 S_VNC	SIM_1_D1 0																							KEYIN_5
V	AUD_AD_0 S_VNC	TST_H	SIM_1_C1 K	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	KEYOUT_0
W		GP0_4	AP_JTAG TMS	AP_JTAG TCK	SIM_1_RS T	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	KEYOUT_1
Y	GP0_1	GP0_3	AP_JTAG TDI	AP_JTAG TDO	SIM_2_RS T	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	KEYOUT_2
AA	GP10_7	GP0_0	AP_JTAG TDI	SIM_2_D1 0	USB_DP	USB_DM	USB_VBUS	USB_ID	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	KEYOUT_3
AB	AB1_NC	GP0_2	SIM_2_CL K	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	AVSS_RF	KEYOUT_4

Figure 2-2 BGA Pinout

2.3 Mechanical Dimensions

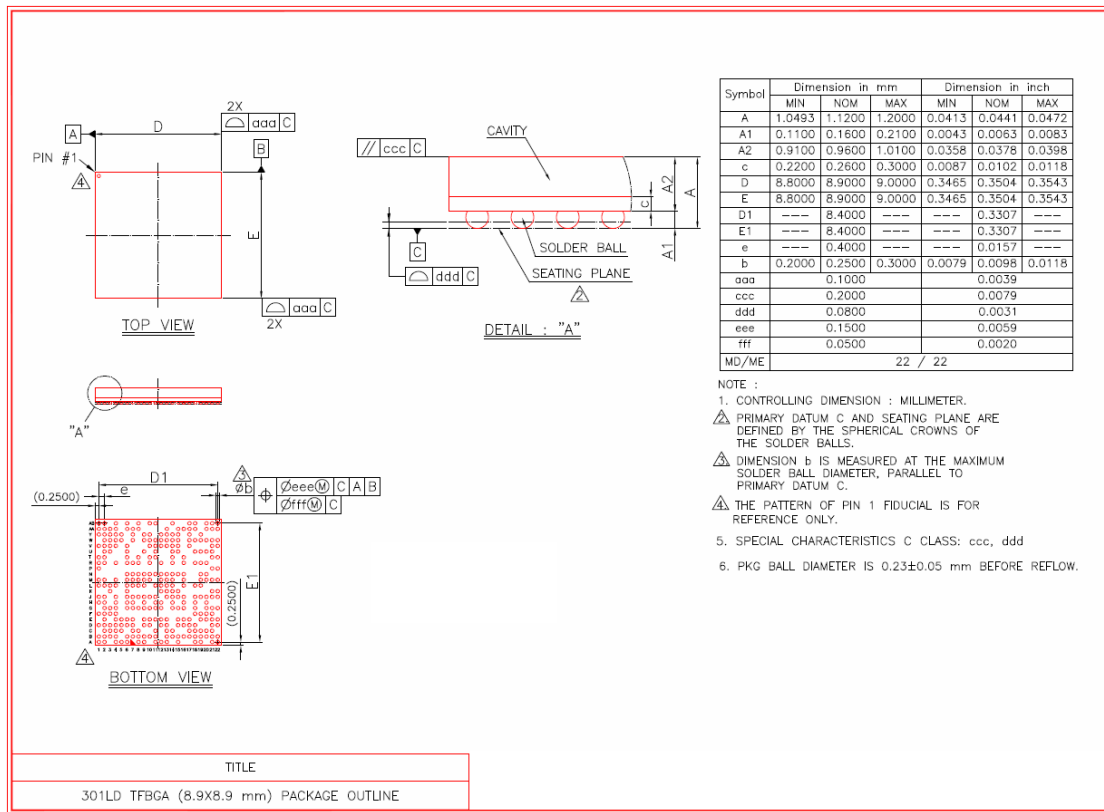


Figure 2-3 Mechanical Dimensions

2.4 Reflow Profile

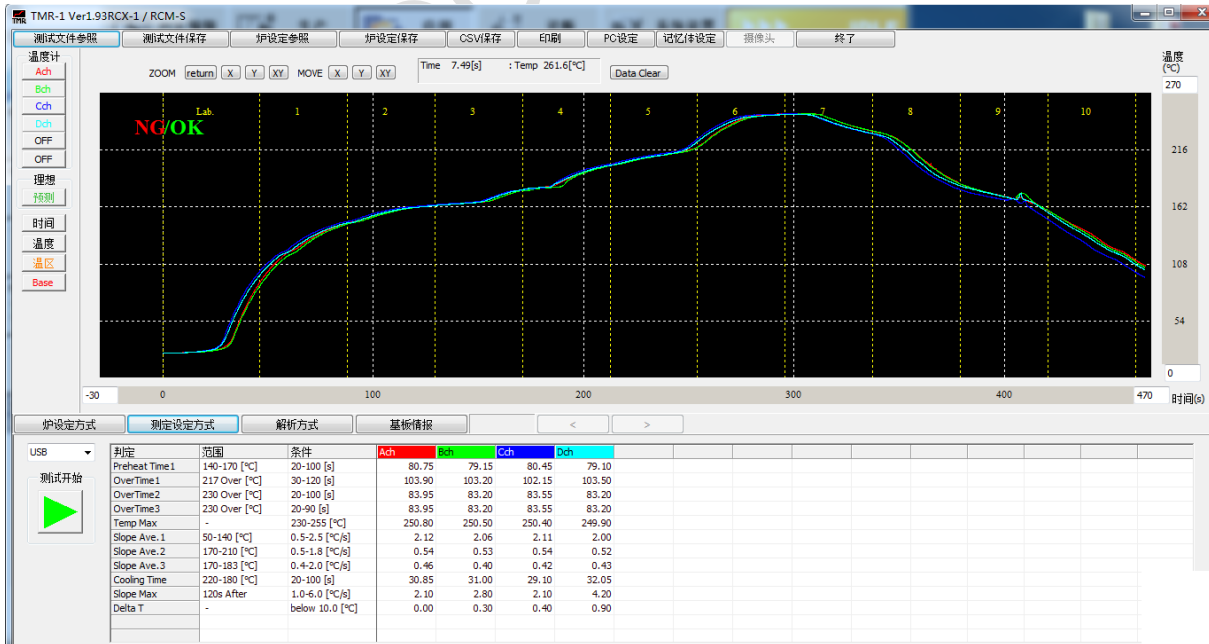


Figure 2-4 Recommended reflow profile

3 Pin Information

3.1 Pin Symbol Descriptions

Table 3-1 Pin Symbol

Field	Symbol	Type Description
Pin Type	I	Digital input
	O	Digital output
	O/T	Digital output with tri-state option
	I/O	Digital bi-directional pin
	I/O/T	Digital bi-directional pin with tri-state option
	PI	Power pin, input from external power supply
	PIO	Power pin, input from external or floating to use internal LDO power supply
	PO	Power pin, output for external devices
	G	Ground pin
	AI	Analog input pin
	AO	Analog output pin
	AIO	Analog bi-directional pin
Pin Value	IPU	Input with pull-up
	IPD	Input with pull-down
	OH	Output "1"
	OL	Output "0"
	Z	Tri-state
Power	VBAT	Battery power supply input
	VDDCORE	Power supply for core, the internal power source are DCDC CORE
	VDDARM	Power supply for ARM, the internal power source are DCDC ARM

3.2 Pin List

3.2.1 SDMMC INTERFACE

Pin Name	Type	Voltage	Function	Location
SDMMC1_CLK	I/O	1.8V/3.0V	Configurable I/O Function0: SD card clock(default) Function2: SPI camera reference clock Function7: SPI master 2 CS	V22
SDMMC1_CMD	I/O	1.8V/3.0V	Configurable I/O Function0: SD card command line(default) Function1: gpio 24 Function2: SPI camera reset, low active Function3: I2C master3 SCL	W22
SDMMC1_DATA_0	I/O	1.8V/3.0V	Configurable I/O Function0: SD card data0 line(default) Function1: gpio 25 Function2: SPI camera power dow control Function3: I2C master3 SDA Function5: uart2 rx data Function6: uart3 CTS	AA22
SDMMC1_DATA_1	I/O	1.8V/3.0V	Configurable I/O Function0: SD card data1 line(default) Function1: gpio 26 Function2: SPI camera serial data0 input Function3: SPI camera serial data1 input Function5: uart2 tx data Function6: uart3 RTS Function7: SPI master 2 clock	W21
SDMMC1_DATA_2	I/O	1.8V/3.0V	Configurable I/O Function0: SD card data2 line(default) Function1: gpio 27 Function2: SPI camera serial data1 input Function3: SPI camera serial data0 input Function4: SPI camera ssn Function5: uart2 CTS Function6: uart3 rx data Function7: SPI master 2 dio	W20
SDMMC1_DATA_3	I/O	1.8V/3.0V	Configurable I/O Function0: SD card data3 line(default) Function1: gpio 28 Function2: SPI camera serial clock Function5: uart2 RTS Function6: uart3 tx data Function7: SPI master 2 di	V21

3.2.2 LCD INTERFACE

Pin Name	Type	Voltage	Function	Location
SPI_LCD_SIO	I/O	1.8V/3.0V	Configurable I/O Function0: SPI LCD serial data I/O(default) Function1: gpio 0 Function2: SPI flash 1 clock	AB21

SPI_LCD_SDC	I/O	1.8V/3.0V	Configurable I/O Function0: SPI LCD SDC(default) Function1: gpio 1 Function2: SPI flash 1 CS Function3: I2C master 3 SDA	AA20
SPI_LCD_CLK	I/O	1.8V/3.0V	Configurable I/O Function0: SPI LCD serial clock(default) Function1: gpio 2 Function2: SPI flash 1 serial data0 I/O	AA21
SPI_LCD_CS	I/O	1.8V/3.0V	Configurable I/O Function0: SPI LCD CS(default) Function1: gpio 3 Function2: SPI flash 1 serial data1 I/O	AB20
SPI_LCD_SELECT	I/O	1.8V/3.0V	Configurable I/O Function0: SPI LCD select signal(default) Function1: gpio 4 Function2: SPI flash 1 serial data2 I/O	AB18
LCD_FMARK	I/O	1.8V/3.0V	Configurable I/O Function0: SPI LCD frame mark(default) Function1: gpio 5 Function2: SPI flash 1 serial data3 I/O Function4: UART2 tx data	AA18
LCD_RSTB	I/O	1.8V/3.0V	Configurable I/O Function0: SPI LCD reset signal (default) Function1: gpio 6 Function3: I2C master 3 SCL Function4: UART2 rx data	Y19

3.2.3 CAMERA INTERFACE

Pin Name	Type	Voltage	Function	Location
I2C_M1_SCL	I/O	1.8V	Configurable I/O Function0: I2C master 1 SCL (default) Function4: gpio 16	L18
I2C_M1_SDA	I/O	1.8V	Configurable I/O Function0: I2C master 1 SDA (default) Function4: gpio 17	L19
CAMERA_RST_L	I/O	1.8V	Configurable I/O Function0: SPI camera reset signal (default) Function1: I2C master 1 SCI Function4: gpio 18	M19
CAMERA_PWDN	I/O	1.8V	Configurable I/O Function0: SPI camera power down (default) Function1: I2C master 1 SDA Function4: gpio 19	K21
CAMERA_REF_CLK	I/O	1.8V	Configurable I/O Function0: SPI camera reference clock(default) Function4: gpio 20	K22
SPI_CAMERA_SI_0	I/O	1.8V	Configurable I/O Function0: SPI camera serial input data 0(default) Function1: SPI camera serial input data 1 Function4: gpio21	M20

SPI_CAMERA_SI_1	I/O	1.8V	Configurable I/O Function0: SPI camera serial input data 1 (default) Function1: SPI camera serial input data 0 Function2: SPI camera ssn Function4: gpio22	M21
SPI_CAMERA_SCK	I/O	1.8V	Configurable I/O Function0: SPI camera serial clock (default) Function4: gpio 23	M22

3.2.4 GPIO INTERFACE

Pin Name	Type	Voltage	Function	Location
PWM_LPG_OUT	O	1.8V	Configurable I/O Function0: gpio 13 (default) Function1: PWM LPG out	D13
GPIO_0	O	1.8V	Configurable I/O Function0: gpio 0 (default) Function1: SPI flash 1 serial clock Function2: SPI master 2 clock Function3: I2S 2 bit clock	R19
GPIO_1	I/O	1.8V	Configurable I/O Function0: gpio 1 (default) Function1: SPI flash 1 chip select output, low active. Function2: SPI 2 CS0 Function3: I2S 2 strobe clock	R20
GPIO_2	I/O	1.8V	Configurable I/O Function0: gpio 2 (default) Function1: SPI flash 1 serial input/output 0 Function2: SPI 2 data I/O Function3: I2S 2 data in	P21
GPIO_3	I/O	1.8V	Configurable I/O Function0: gpio 3 (default) Function1: SPI flash 1 serial input/output 1 Function2: SPI 2 data input Function3: I2S 2 data out	P22
GPIO_4	I/O	1.8V	Configurable I/O Function0: gpio 4 (default) Function1: SPI flash 1 serial input/output 2 Function2: SPI 2 CS1 Function3: PWL out Function6: I2C M3 SCL	T21
GPIO_5	I/O	1.8V	Configurable I/O Function0: gpio 5 (default) Function1: SPI flash 1 serial input/output 3 Function2: PWT out Function3: LCD frame mark Function6: I2C M3 SDA	T22
GPIO_6	I/O	1.8V	Dedicated for PMIC external interrupter	L2
GPIO_7	I/O	1.8V	Configurable I/O Function0: gpio 7 (default) Function1: SD MMC 2 clock Function2: SPI master 1 clock	AA1

			Function3: PWL out	
I2C_M2_SCL	I/O	1.8V	Configurable I/O Function0: gpio 14(default) Function1: I2C master 2 SCL	J18
I2C_M2_SDA	I/O	1.8V	Configurable I/O Function0: gpio 15(default) Function1: I2C master 2 SDA	J19
UART_1_CTS	I/O	1.8V	Configurable I/O Function0: gpio 18(default) Function1: UART 1 CTS	G21
UART_1_RTS	I/O	1.8V	Configurable I/O Function0: gpio 19(default) Function1: UART 1 RTS	G22
UART_1_RXD	I/O	1.8V	UART 1 rx data	L4
UART_1_TXD	I/O	1.8V	UART 1 tx data	L6
UART_2_RXD	I/O	1.8V	Configurable I/O Function0: gpio 20(default) Function1: UART 2 rx data Function2: UART 3 rx data Function4: UART 3 cts	J21
UART_2_TXD	I/O	1.8V	Configurable I/O Function0: gpio 21(default) Function1: UART 2 tx data Function2: UART 3 tx data Function4: UART 3 rts	J22
UART_2_CTS	I/O	1.8V	Configurable I/O Function0: gpio 22(default) Function1: UART 2 cts Function2: UART 3 cts Function4: UART 3 rxd	N20
UART_2_RTS	I/O	1.8V	Configurable I/O Function0: gpio 23(default) Function1: UART 2 rts Function2: UART 3 rts Function4: UART 3 txd	N19
GPO_0	I/O	1.8V	Configurable I/O Function0: gpio 8(default) Function1: SPI master 1 CS1	AA2
GPO_1	I/O	1.8V	Configurable I/O Function0: gpio 9(default) Function1: SPI master 1 clock	Y1
GPO_2	I/O	1.8V	Configurable I/O Function0: gpio 10(default) Function1: SPI master 1 CS0	AB2
GPO_3	I/O	1.8V	Configurable I/O Function0: gpio 11(default) Function1: SPI master 1 data I/O	Y2
GPO_4	I/O	1.8V	Configurable I/O Function0: gpio 12(default) Function1: SPI master 1 data in	W2

3.2.5 KEYPAD INTERFACE

Pin Name	Type	Voltage	Function	Location
KEYIN_0	I/O	1.8V	Key pad input 0 Pull high into Force download mode	B22
KEYIN_1	I/O	1.8V	Key pad input 1 Pull high :Boot from SD card	C21
KEYIN_2	I/O	1.8V	Key pad input 2	E19
KEYIN_3	I/O	1.8V	Key pad input 3	E20
KEYIN_4	I/O	1.8V	Configurable I/O Function0: Key pad input 4 (default) Function3: UART 2 rx data Function4: UART 3 CTS	D21
KEYIN_5	I/O	1.8V	Configurable I/O Function0: Key pad input 5 (default) Function3: UART 2 tx data Function4: UART 3 RTS	D22
KEYOUT_0	I/O	1.8V	Key pad output 0	E21
KEYOUT_1	I/O	1.8V	Key pad output 0	E22
KEYOUT_2	I/O	1.8V	Key pad output 0	F20
KEYOUT_3	I/O	1.8V	Key pad output 0	G20
KEYOUT_4	I/O	1.8V	Configurable I/O Function0: Key pad output 4 (default) Function3: UART 2 CTS Function4: UART 3 rx data	F21
KEYOUT_5	I/O	1.8V	Configurable I/O Function0: Key pad output 5 (default) Function3: UART 2 RTS Function4: UART 3 tx data	F19

3.2.6 SIM INTERFACE

Pin Name	Type	Voltage	Function	Location
SIM_1_CLK	I/O	1.8V/3.0V	SIM card 1 clock	V3
SIM_1_DIO	O	1.8V/3.0V	SIM card 1 data I/O	U3
SIM_1_RST	I/O	1.8V/3.0V	SIM card 1 reset	W5
SIM_2_CLK	I/O	1.8V/3.0V	Configurable I/O Function0: SIM card 2 clock (default) Function1: gpo 5 Function2: gpio 29	AB4
SIM_2_DIO	I/O	1.8V/3.0V	Configurable I/O Function0: SIM card 2 data I/O (default) Function1: gpo 6 Function2: gpio 30 Function3: UART 1 CTS	AA4
SIM_2_RST	I/O	1.8V/3.0V	Configurable I/O Function0: SIM card 2 reset (default) Function1: gpo 7 Function2: gpio 31 Function3: UART 1 RTS	Y5

3.2.7 DEBUGHOST INTERFACE

Pin Name	Type	Voltage	Function	Location
DEBUG_HOST_RX	I/O	1.8V	Configurable I/O Function0: debug host rx data (default) Function1: gpio 16	J20
DEBUG_HOST_TX	I/O	1.8V	Debug host tx data (default)	H18
DEBUG_HOST_CLK	I/O	1.8V	Configurable I/O Function0: debug host external clock(default) Function1: gpio 17	H20

3.2.8 PMIC INTERFACE

Pin Name	Type	Voltage	Function	Location
AUD_DA_SYNC	O	1.8V	Audio DAC sync	T2
AUD_DA_D1	O	1.8V	Audio DAC data 1	R2
AUD_DA_D0	O	1.8V	Audio DAC data 0	T1
AUD_AD_SYNC	I	1.8V	Audio ADC sync	U2
AUD_AD_D0	I	1.8V	Audio ADC data 0	V1
AUD_SCLK	O	1.8V	Audio serial clock	M4
ADI_SDA	I/O	1.8V	Analog/digital interface SDA	M1
ADI_SYNC	O	1.8V	Analog/digital interface SYNC	P1
ADI_SCL	O	1.8V	Analog/digital interface SCL	M2
CHIP_PD	O	1.8V	Chip deep sleep control to PMIC 0:normal 1:sleep	L3
OSC_32K	I	1.8V	32K clock from PMIC	L1
RESETB	I	1.8V	reset from PMIC 0:reset chip 1:realse reset chip	R1
CLK26M_PMIC	O	1.8V	Audio 26MHz clock to PMIC	K3

3.2.9 USB INTERFACE

Pin Name	Type	Voltage	Function	Location
USB_DP	Analog I/O	-	USB high speed data+	AA6
USB_DM	Analog I/O	-	USB high speed data-	AA7
USB_ID	Analog I	-	USB otg ID(default 98K ohm pullup)	AB8

3.2.10 RF INTERFACE

Pin Name	Type	Voltage	Function	Location
RFOUT_LB2	Analog O	1.5V	TX LTE LB output	B9
RFOUT_LB1	Analog O	1.5V	TX LTE LB output	A9
RFOUT_HB2	Analog O	1.5V	TX LTE HB output	B10
RFOUT_HB1	Analog O	1.5V	TX LTE HB output	B11
RFOUT_GSML	Analog O	1.5V	TX GSM LB output	B8

RFOUT_GSMH	Analog O	1.5V	TX GSM HB output	A8
RAMP_OUT	Analog O	1.5V	GSM PA ramp signal output to PA	F1
APC_OUT	Analog O	1.5V	LTE PA VCC control signal output to PA	H4
TSEN_VREFP	Analog O	1.5V	TSEN ADC reference voltage output	G2
TSEN_VREFN	Analog O	1.5V	TSEN ADC reference voltage output	G3
XTAL2	Analog I	1.5V	Crystal port for XTAL	J1
XTAL1	Analog O	1.5V	Crystal port for XTAL	H1
PSM_CAL_EN	Analog I	1.5V	PSM mode calibration enable	J6
TSEN_IN	Analog I	1.5V	TSEN ADC current voltage value	F2
RF_VIP_LTE_ULB	Analog I	1.5V	RX LTE ultra LB input	A2
RF_VIP_LTE_MB	Analog I	1.5V	RX LTE MB input	A5
RF_VIP_LTE_LB	Analog I	1.5V	RX LTE LB input	B3
RF_VIP_LTE_HB	Analog I	1.5V	RX LTE HB input	A6
RF_VIP_GSM_LB	Analog I	1.5V	RX GSM LB input	D1
RF_VIP_GSM_HB	Analog I	1.5V	RX GSM HB input	B1
RF_VIN_LTE_ULB	Analog I	1.5V	RX LTE ultra LB input	B2
RF_VIN_LTE_MB	Analog I	1.5V	RX LTE MB input	A4
RF_VIN_LTE_LB	Analog I	1.5V	RX LTE LB input	B4
RF_VIN_LTE_HB	Analog I	1.5V	RX LTE HB input	B6
RF_VIN_GSM_LB	Analog I	1.5V	RX GSM LB input	D2
RF_VIN_GSM_HB	Analog I	1.5V	RX GSM HB input	C2
PDET_GND	Analog I	1.5V	External power detector analog input	E12
PDET	Analog I	1.5V	External power detector analog GND input	D12

4 Electrical Specification

4.1 Recommended Operating Conditions

Table 4-1 Recommended Operating Power Range

Parameter	Min	Typical	Max	Units
VDD	0.8	0.9	1.0	V
VDDQ	1.62	1.8	1.98	V
AVDD15_WCN	1.35	1.5	1.65	V
V_PAD_1V8	1.7	1.8	1.9	V
V_PAD_1V8_RTC	1.62	1.85	1.98	V
AVDD15_RF	1.35	1.5	1.65	V
VSIM1/VSIM2	1.62	1.8	1.98	V
	2.9	3.0	3.3	V
AVDD18_DCXO	1.7	1.8	1.9	V
AVDD18	1.62	1.8	1.98	V
V_LCD	1.62	1.8	1.98	V
	2.7	3.0	3.3	V
AVDD33_USB	3.1	3.3	3.5	V
V_SPIMEM	1.62	1.8	1.98	V
	3.15	3.3	3.45	V
V_MMC	1.62	1.8	1.98	V
	2.8	3.0	3.3	V

Table 4-2 DC Parameters (1.8V Digital IO)

Parameter	Min	Typical	Max	Units
High Input Voltage VIH	0.7Vcc	-	-	V
Low Input Voltage VIL	-	-	0.3Vcc	V
Input Leakage IL	-	-	20	uA
Tri-State Output Leakage	-	2.8	20	uA
High Output Voltage VOL	-	-	0.2Vcc	V
High Output Voltage VOH	0.8Vcc	-	-	V
Pullup Resistance RPU	0.54	1.8	3.06	KΩ
	2.35	4.7	7.05	KΩ
	6	20	34	KΩ
Pulldown Resistance VPD	20	50	80	KΩ
High Input Voltage VIH	0.7Vcc	-	-	V
Low Input Voltage VIL	-	-	0.3Vcc	V

Table 4-3 DC Parameters (3.3V Digital IO)

Parameter	Min	Typical	Max	Units
High Input Voltage VIH	0.7Vcc	-	-	V
Low Input Voltage VIL	-	-	0.15Vcc	V
Input Leakage IL	-	-	20	uA
Tri-State Output Leakage	-	2.8	20	uA
High Output Voltage VOL	-	-	0.15Vcc	V
High Output Voltage VOH	0.7Vcc	-	-	V
Pullup Resistance RPU	0.54	1.8	3.06	KΩ
	2.35	4.7	7.05	KΩ
	6	20	34	KΩ
Pulldown Resistance VPD	20	50	80	KΩ
High Input Voltage VIH	0.7Vcc	-	-	V
Low Input Voltage VIL	-	-	0.15Vcc	V

4.2 Thermal Characteristics

Table 4-4 Thermal Characteristics

Parameter	Min	Typical	Max	Units
Operating Temperature	-40	25	85	°C
Storage Temperature	-55	-	150	°C