

VERSION HISTORY

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1

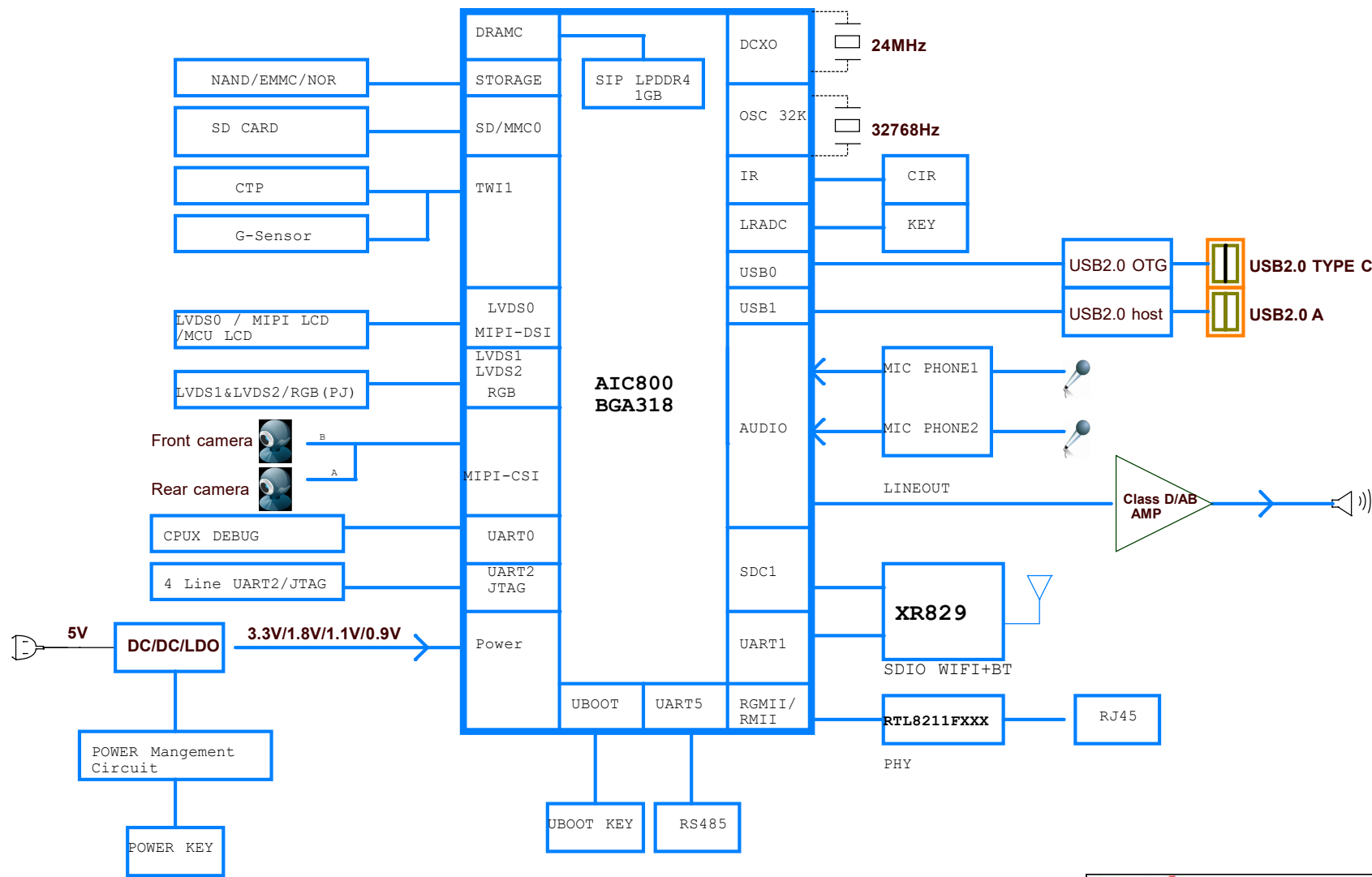
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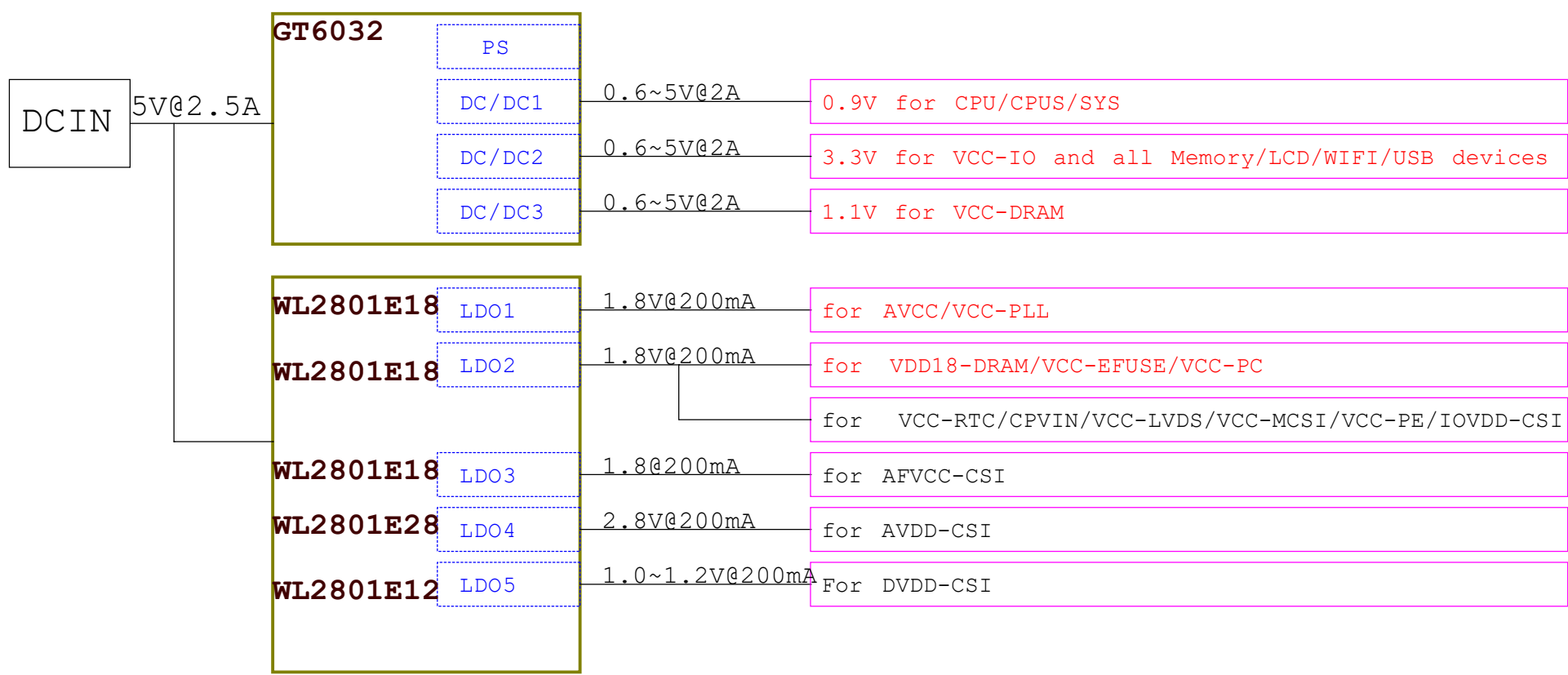
Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Initial Edition	2020/10/13	ZSC		

 Sochip 深圳市索智科技股份有限公司 ShenZhen Sochip Technology Co.,LTD		
Design name	SC3904Q	
Size	Document Number	Rev
A3	VERSION HISTORY	V00
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BLOCK DIAGRAM



POWER TREE



GPIO ASSIGNMENT

PIN	Define	CFG	Function
PB0	JTAG-TMS/TX2		
PB1	JTAG-TCK/RX2	JTAG	
PB2	JTAG-TDO/RTS2	UART2	4L
PB3	JTAG-TDI/CTS2		
PB4	TWI1-SCK		CTP
PB5	TWI1-SDA		G-Sensor
PB6	USB-ID		
PB7	USB0-BUSDET		USB OTG
PB8	USB0-DRVBUS		
PB9	UAR0-TX		UART0
PB10	UART0-RX		DEBUG

PIN	Define	CFG	Function
PD0	LCD0-D2/DP0		
PD1	LCD0-D3/DN0		
PD2	LCD0-D4/DP1		
PD3	LCD0-D5/DN1		MCU LCD
PD4	LCD0-D6/CKP		LVDS0 LCD
PD5	LCD0-D7/CKN		MIPI LCD
PD6	LCD0-D10/DP2		
PD7	LCD0-D11/DM2		
PD8	LCD0-D12/DP3		
PD9	LCD0-D13/DN3		

PIN	Define	CFG	Function
PG0	WL-SDIO-CLK		
PG1	WL-SDIO-CMD		
PG2	WL-SDIO-D0		
PG3	WL-SDIO-D1		WIFI+BT
PG4	WL-SDIO-D2		
PG5	WL-SDIO-D3		
PG6	UART1-TX		
PG7	UART1-RX		
PG8	UART1-RTS		
PG9	UART1-CTS		

PIN	Define	CFG	Function
PJ0	LCD1-D0/2D0P		
PJ1	LCD1-D1/2D0N		
PJ2	LCD1-D2/2D1P		
PJ3	LCD1-D3/2D1N		
PJ4	LCD1-D4/2D2P		
PJ5	LCD1-D5/2D2N		
PJ6	LCD1-D6/2CKP		
PJ7	LCD1-D7/2CKN		
PJ8	LCD1-D8/2D3P		
PJ9	LCD1-D9/2D3N		
PJ10	LCD1-D10/3D0P		
PJ11	LCD1-D11/3D0N		
PJ12	LCD1-D12/3D1P		RGB LCD
PJ13	LCD1-D13/3D1N		LVDS LCD
PJ14	LCD1-D14/3D2P		
PJ15	LCD1-D15/3D2N		
PJ16	LCD1-D16/3CKP		
PJ17	LCD1-D17/3CKN		
PJ18	LCD1-D18/3D3P		
PJ19	LCD1-D19/3D3N		
PJ20	LCD1-D20		
PJ21	LCD1-D21		
PJ22	LCD1-D22		
PJ23	LCD1-D23		
PJ24	LCD1-CLK		
PJ25	LCD1-DE		
PJ26	LCD1-HSYNC		
PJ27	LCD1-VSYNC		

PIN	Define	CFG	Function
PC0	NAND-WE/DS		NAND
PC1	NAND-ALE/RST		eMMC
PC2	NAND-CLE/MOSI		
PC3	NAND-CE1/CS0		NAND
PC4	NAND-CE0/MISO		SPI
PC5	NAND-RE/CLK		
PC6	NAND-RB0/CMD		NAND
PC8	NAND-DQ7/D3		eMMC
PC9	NAND-DQ6/D4		
PC10	NAND-DQ5/D0		
PC11	NAND-DQ4/D5		
PC12	NAND-DQS/CLK		NAND/SPI
PC13	NAND-DQ3/D1		NAND
PC14	NAND-DQ2/D6		eMMC
PC15	NAND-DQ1/D2		NAND /eMMC
PC16	NAND-DQ0/D7		SPI

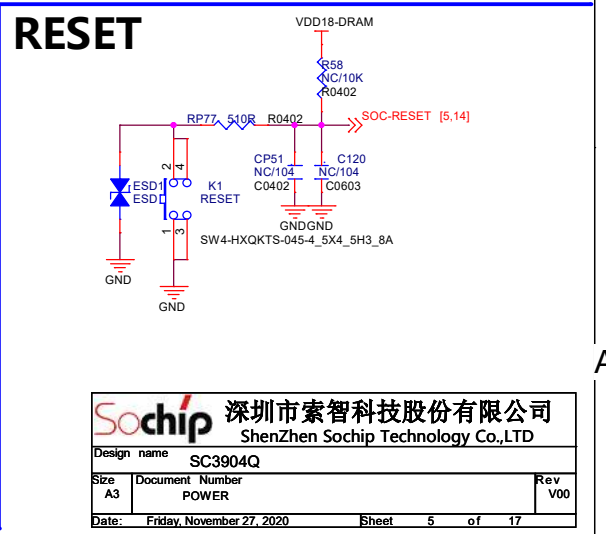
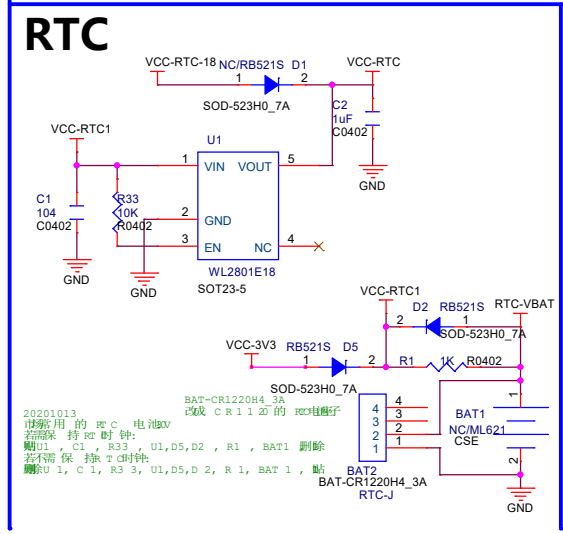
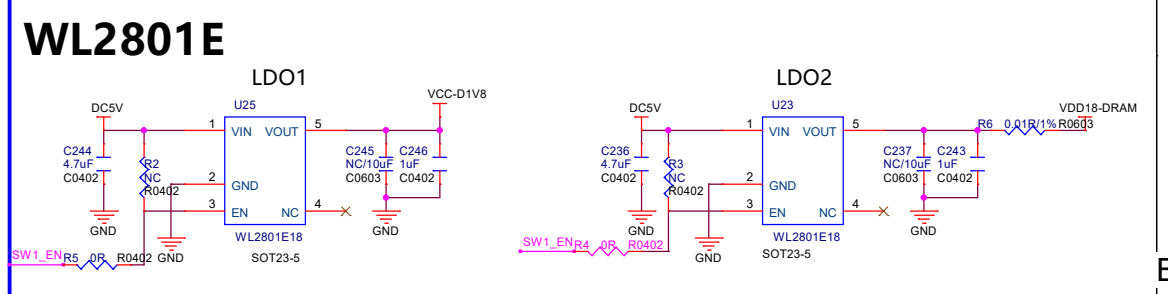
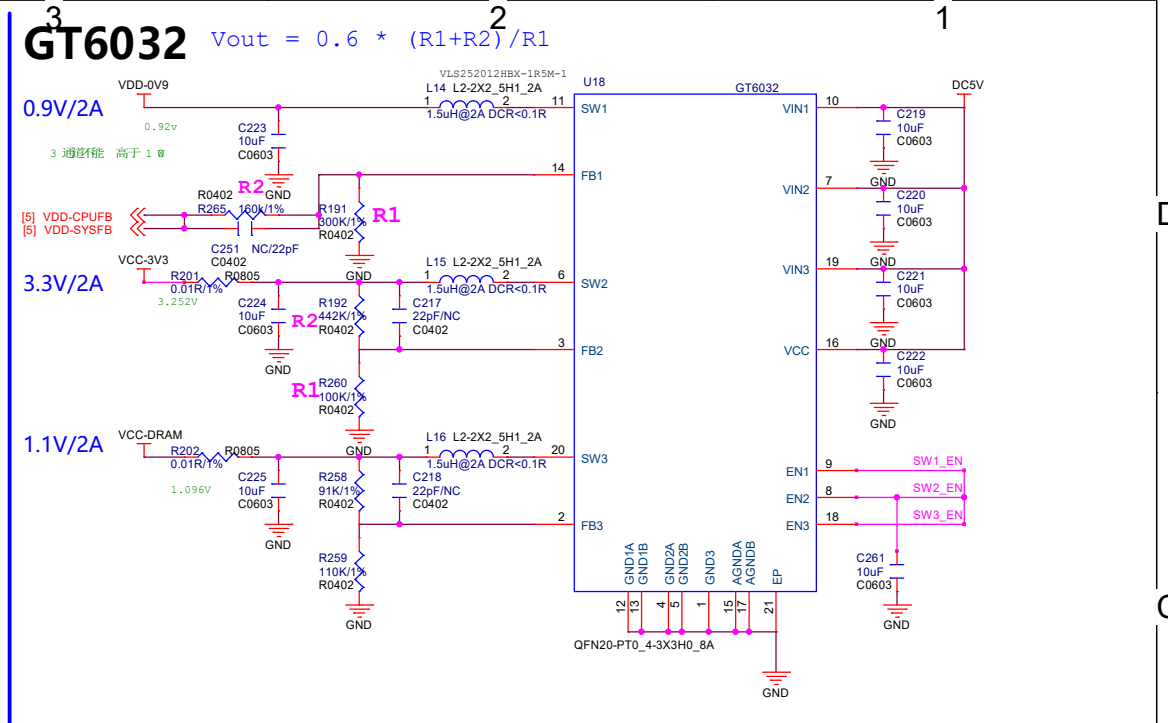
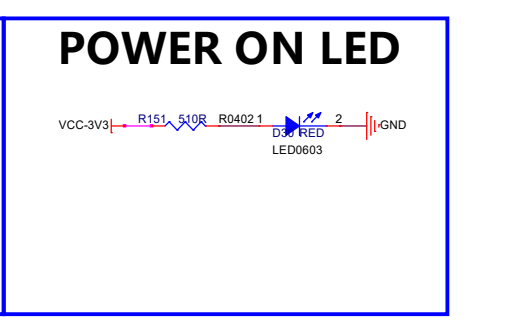
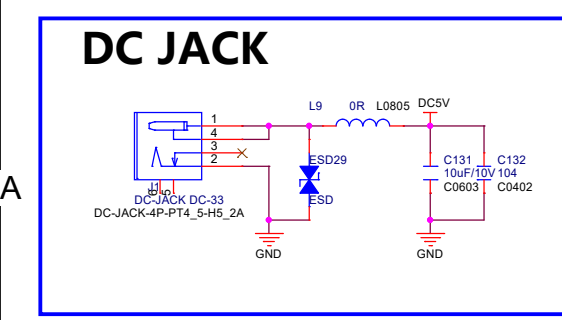
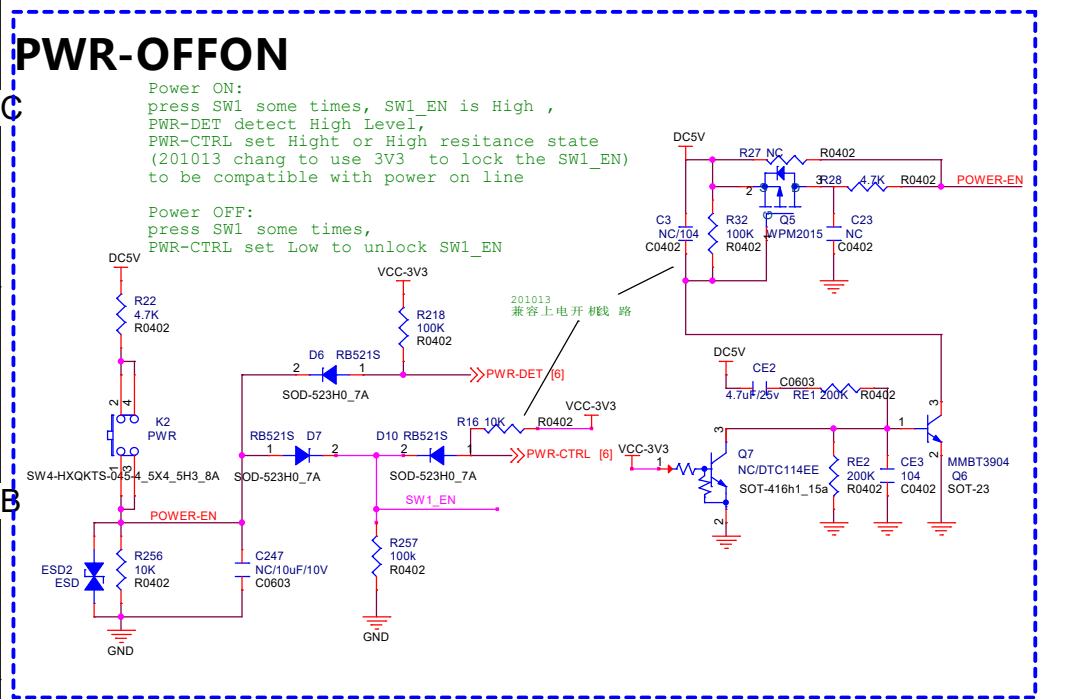
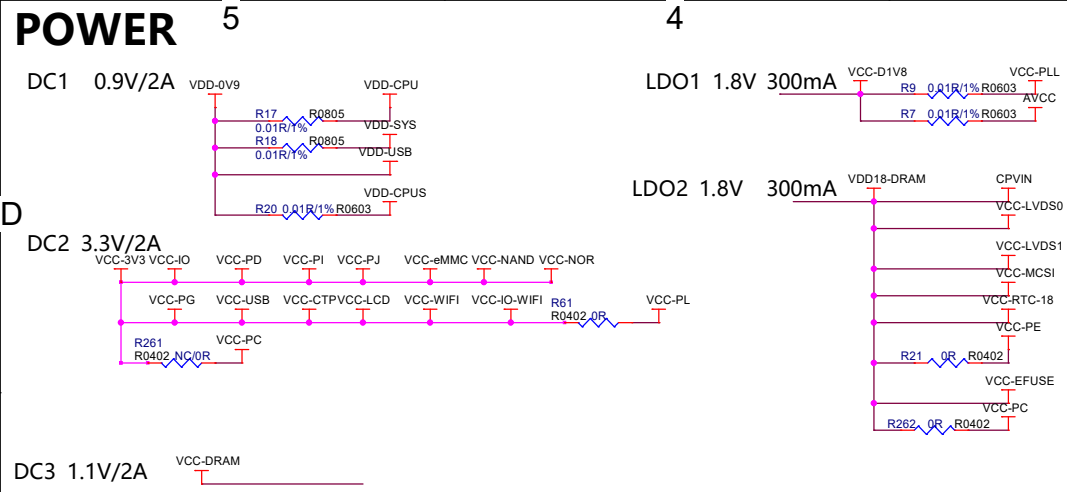
PIN	Define	CFG	Function
PI0	CTP-INT		CTP
PI1	CTP-RST		
PI2	UART5-TX		
PI3	UART5-TX		RS485
PI4	UART5-RTS		
PI5	UART5-CTS		RESERVE
PI6	LCD-RST		
PI7	LCD-PWM		LCD
PI8	LCD-PWR-EN		
PI9	PA-SHDN		SPK

PIN	Define	CFG	Function
PH0	RGMII0-RXD1	1	
PH1	RGMII0-RXD0		
PH2	RGMII0-RXCTL1		
PH3	RGMII0-CLKIN1		
PH4	RGMII0-TXD1		
PH5	RGMII0-TXD0		
PH6	RGMII0-TXCK		
PH7	RGMII0-TXCTL		
PH9	MDC0		
PH10	MDIO0		
PH13	EPHY0-25M		
PH14	RGMII0-RXD3		
PH15	RGMII0-RXD2		
PH16	RGMII0-RXCK		
PH17	RGMII0-TXD3		
PH18	RGMII0-TXD2		
PH19	RGMII0-RST		

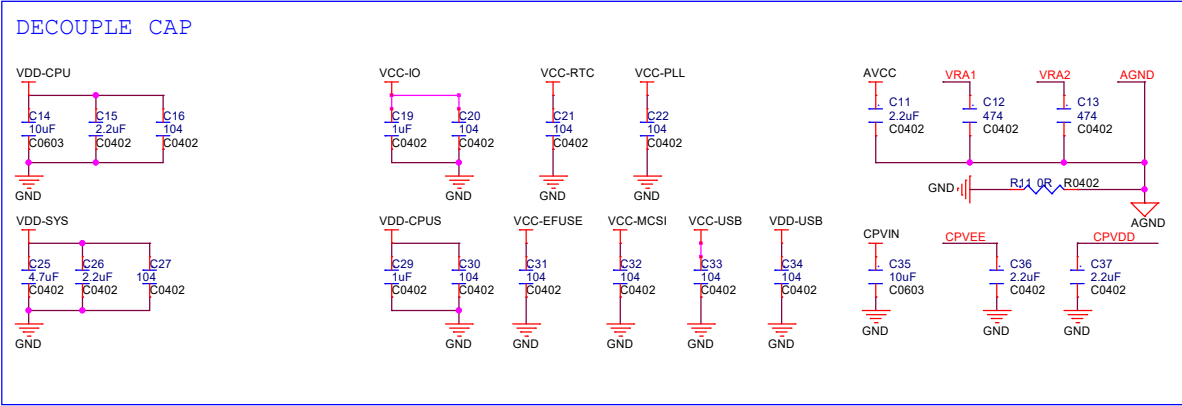
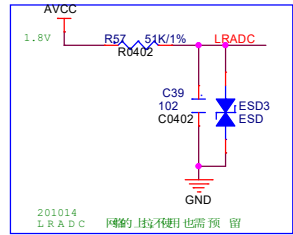
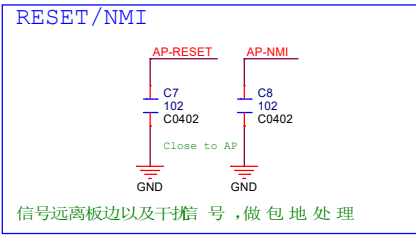
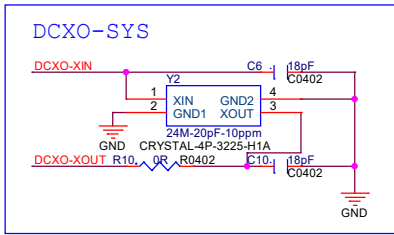
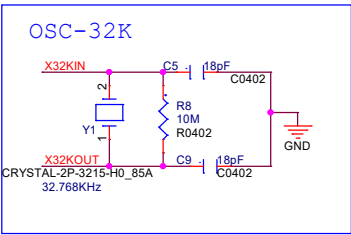
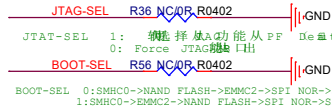
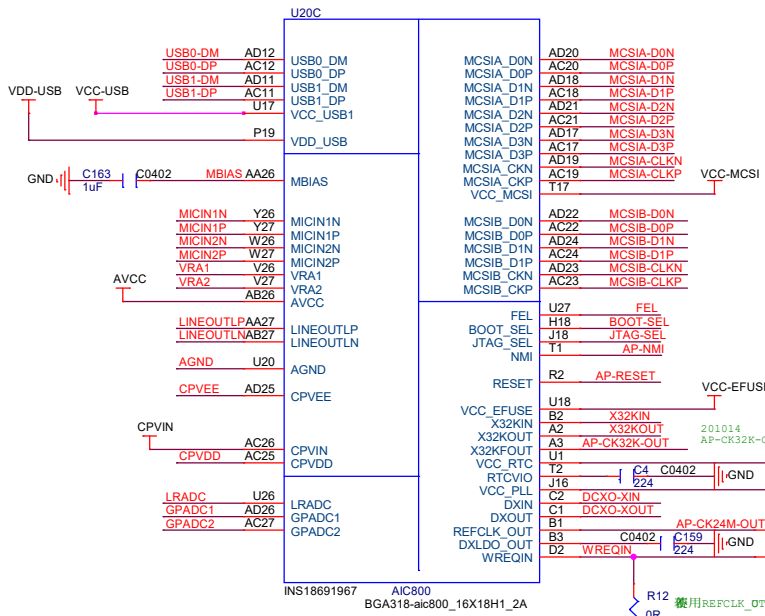
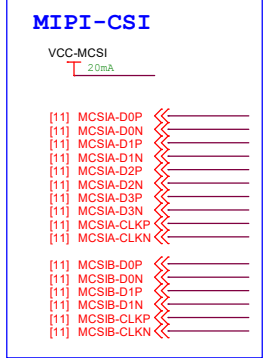
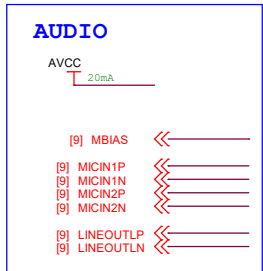
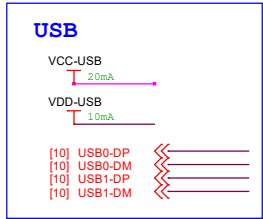
PIN	Define	CFG	Function
PE0	MIPI-MCLK0		MIPI-CSIA
PE1	TWI2-SCK		
PE2	TWI2-SDA		
PE3	TWI3-SCK		
PE4	TWI3-SDA		MIPI-CSIB
PE5	MIPI-MCLK1		
PE6	MCSIA-RESET		MIPI-CSIA
PE7	MCSIA-PWDN		

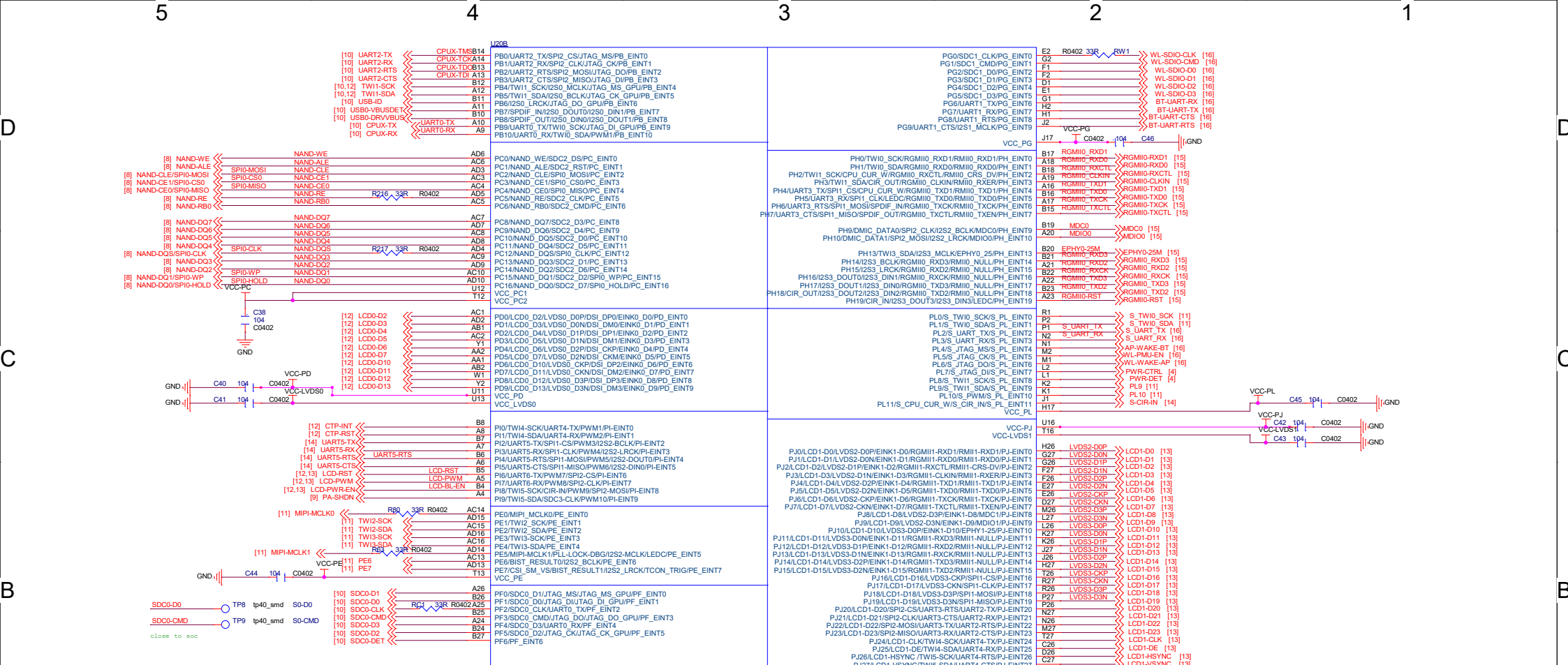
PIN	Define	CFG	Function
PL0	MIPI-CSI-B		MIPI-CSIB
PL1	MIPI-CSIB-PWD		
PL2	BT-RST-N		WIFI+BT
PL3	BT-WAKE-AP		
PL4	AP-WAKE-BT		
PL5	WL-PMU-EN		
PL6	WL-WAKE-AP		
PL7	PWR-CTRL		POWER CONTROL
PL8	PWR-DET		
PL9	CSI-PWREN-A		MIPI-CSIA
PL10	CSI-PWREN-B		MIPI-CSIB
PL11	S-CIR-IN		CIR

PIN	Define	CFG	Function
PF0	SDC0-D1		MIPI-CSIA
PF1	SDC0-D0		
PF2	SDC0-CLK		
PF3	SDC0-CMD		
PF4	SDC0-D3		MIPI-CSIB
PF5	SDC0-D2		
PF6	SDC0-DET		



20201013
 新增用的 3V3 电池
 新增保持时钟
 删除 C1, R33, U1,D5,D2, R1, BAT1 删除
 不需要保持时钟
 删除 U1, C1, R33, U1,D5,D2, R1, BAT1, 点
 BAT-CR1220H4_3A 改成 C R11220 的 锂电池
 BAT1 删除
 BAT2
 RTC-J





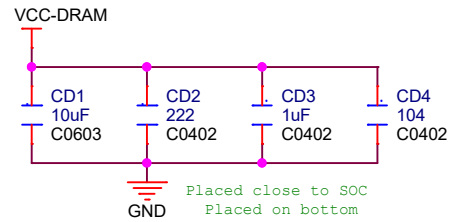
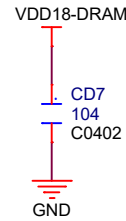
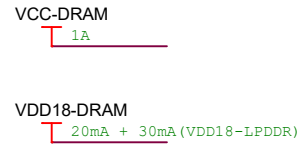
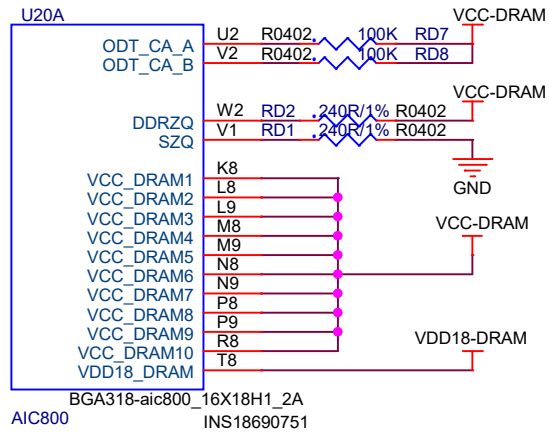
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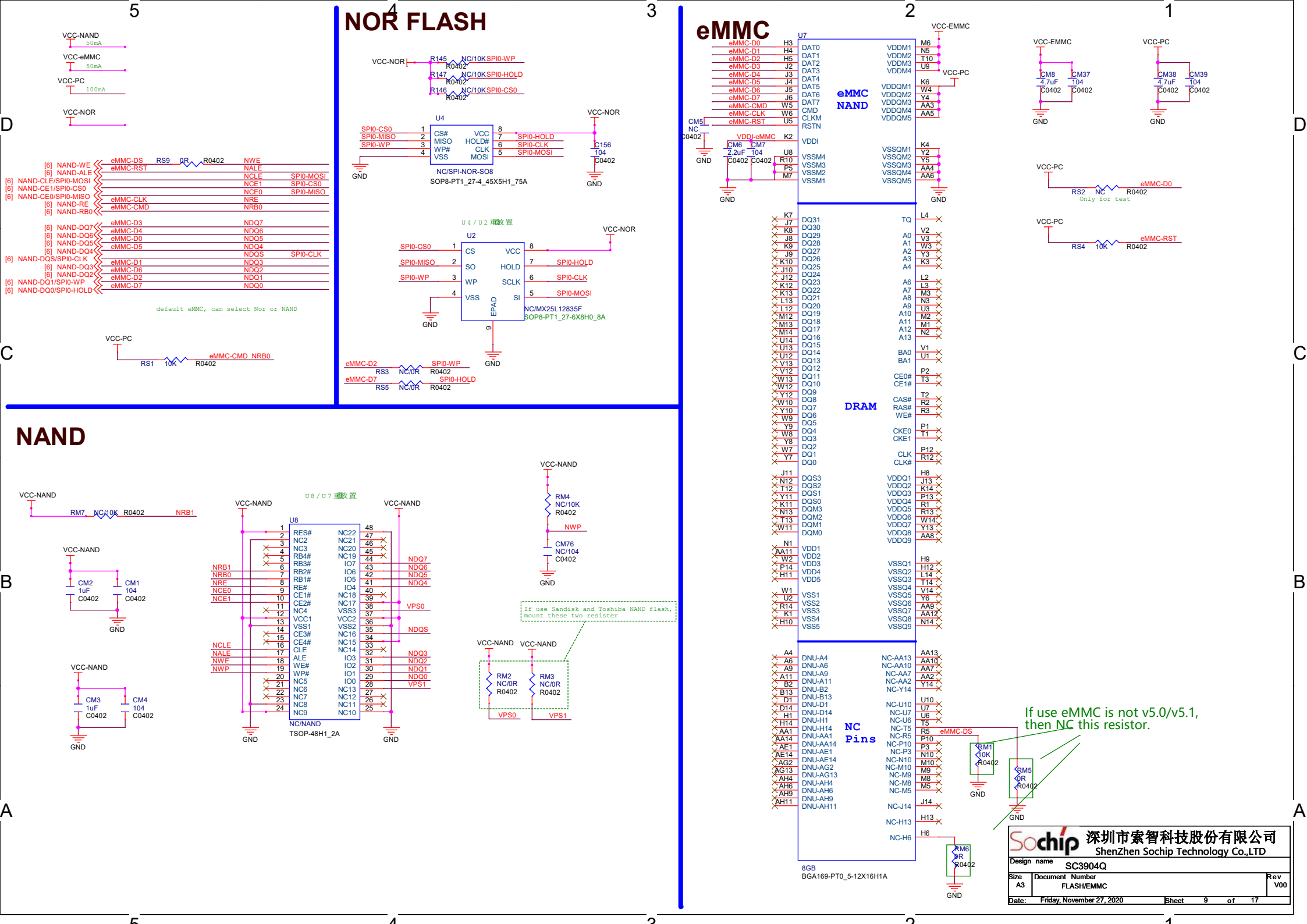
GPIO 说明
 1、注意 S @端与接的D电平匹配
 2、I @端电压选择对按钮所属电源域电压

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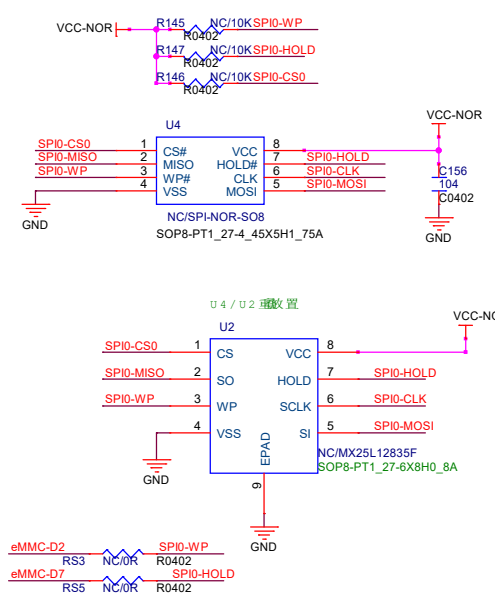
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Size	Custom
Document	Number
Custm	CPU GPIO
Date:	Friday, November 27, 2020
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Rev	000

LPDDR4

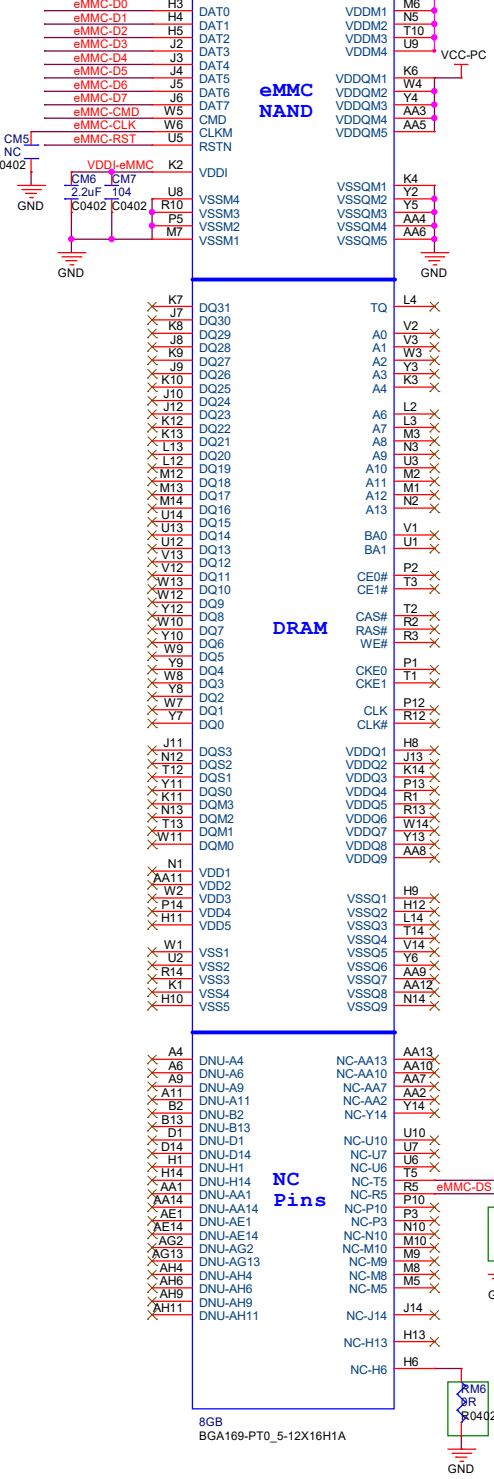




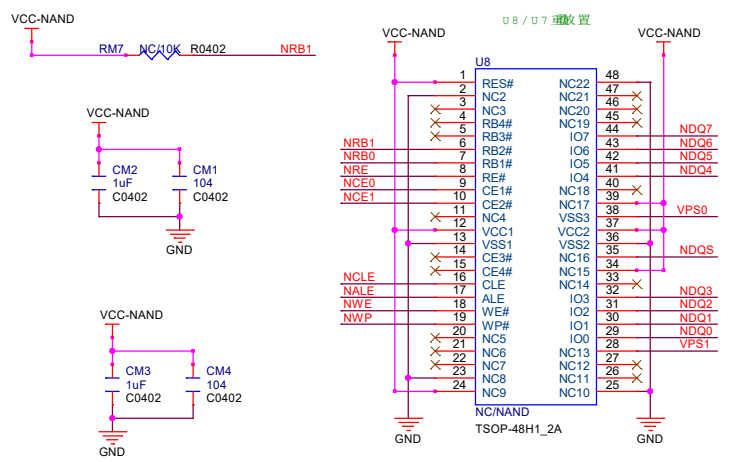
NOR FLASH



eMMC



NAND



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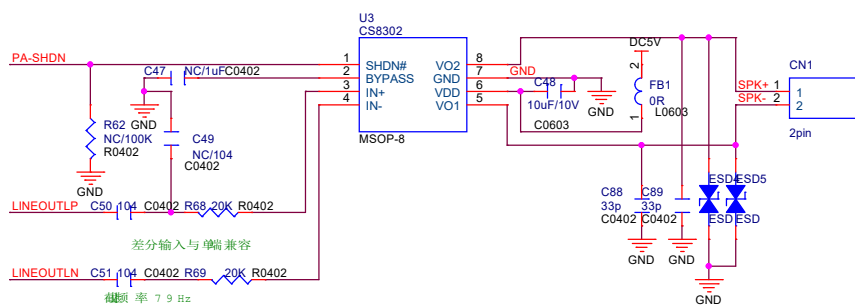
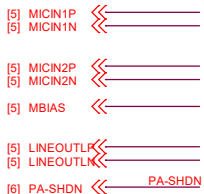
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Size	Document Number	Rev
A3	FLASH/eMMC	V00

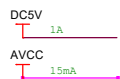
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SPK

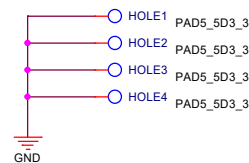
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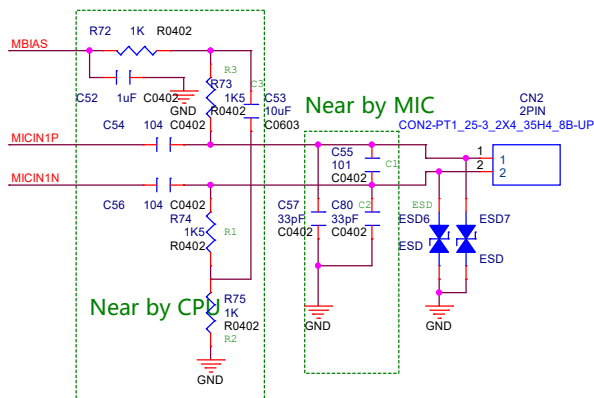
差分输入与单端兼容
 音频率 7.9 Hz



SCREW HOLD



MIC1

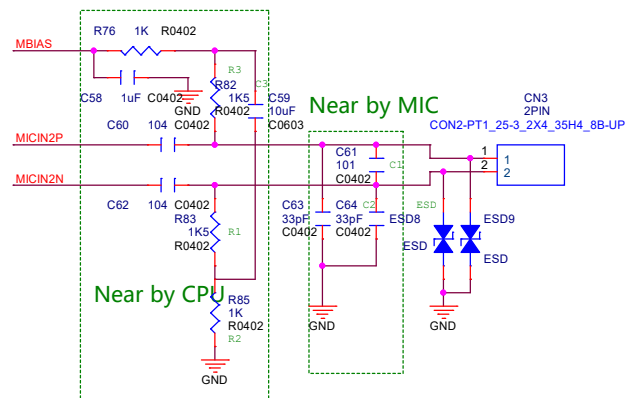


Near by CPU

Near by MIC

Component	Diferential	single-ended
R1 R2 C1 C3 D1 ESD	USE	NC
C2	33pF	0R
R3	1.5K	1K

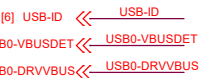
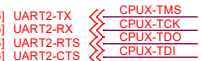
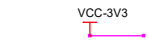
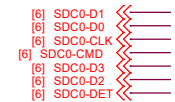
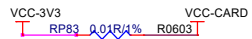
MIC2



Near by CPU

Near by MIC

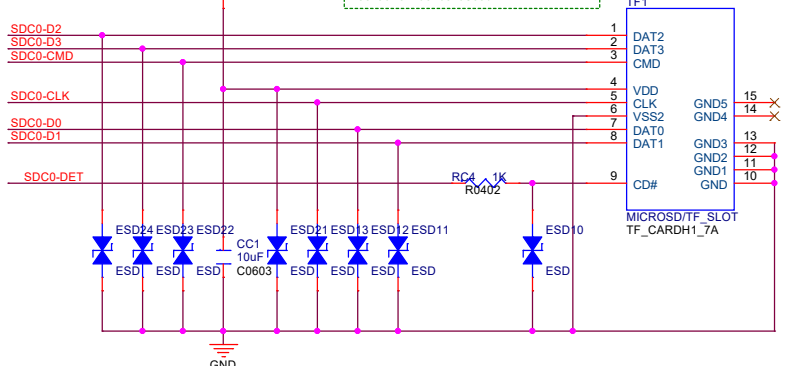
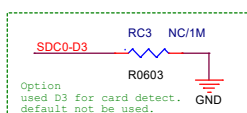
CARD0



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VCC-CARD

RC2 2R2 R0603

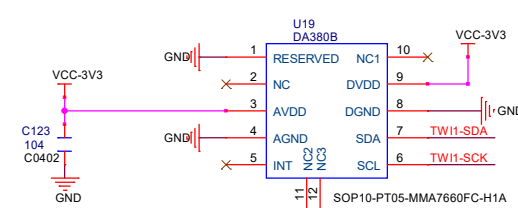


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G-Sensor

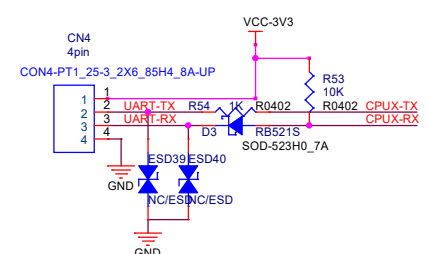


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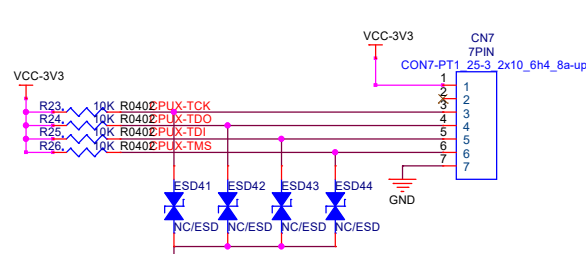


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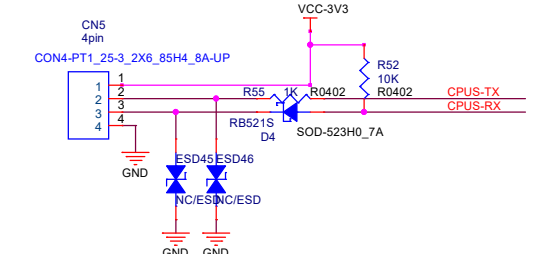
CPUX DEBUG



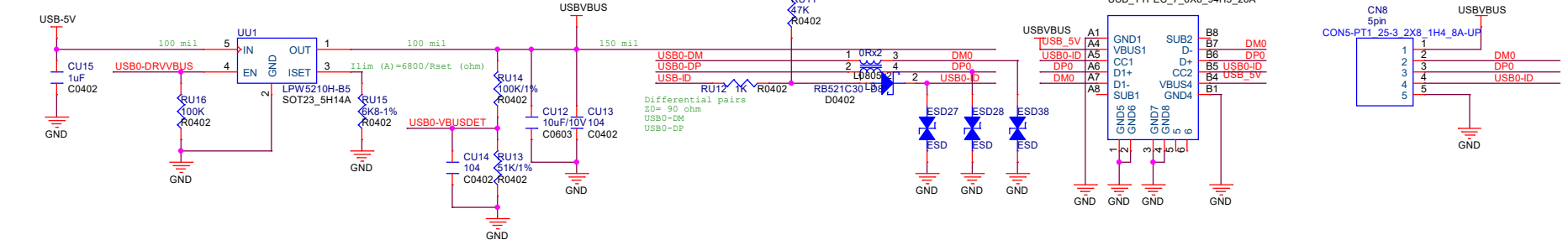
4 UART2 CON & JTAG CON



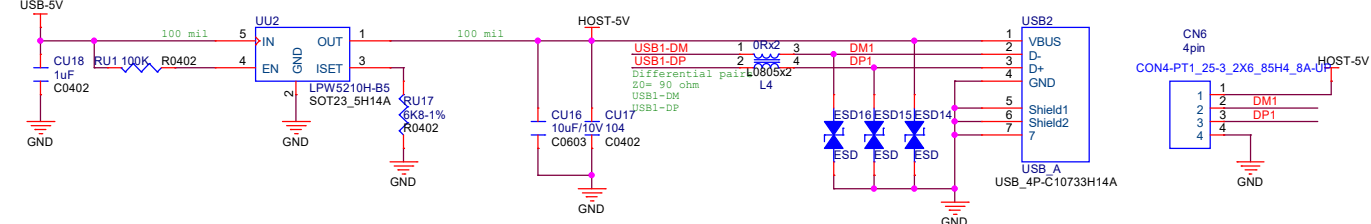
CPUS DEBUG



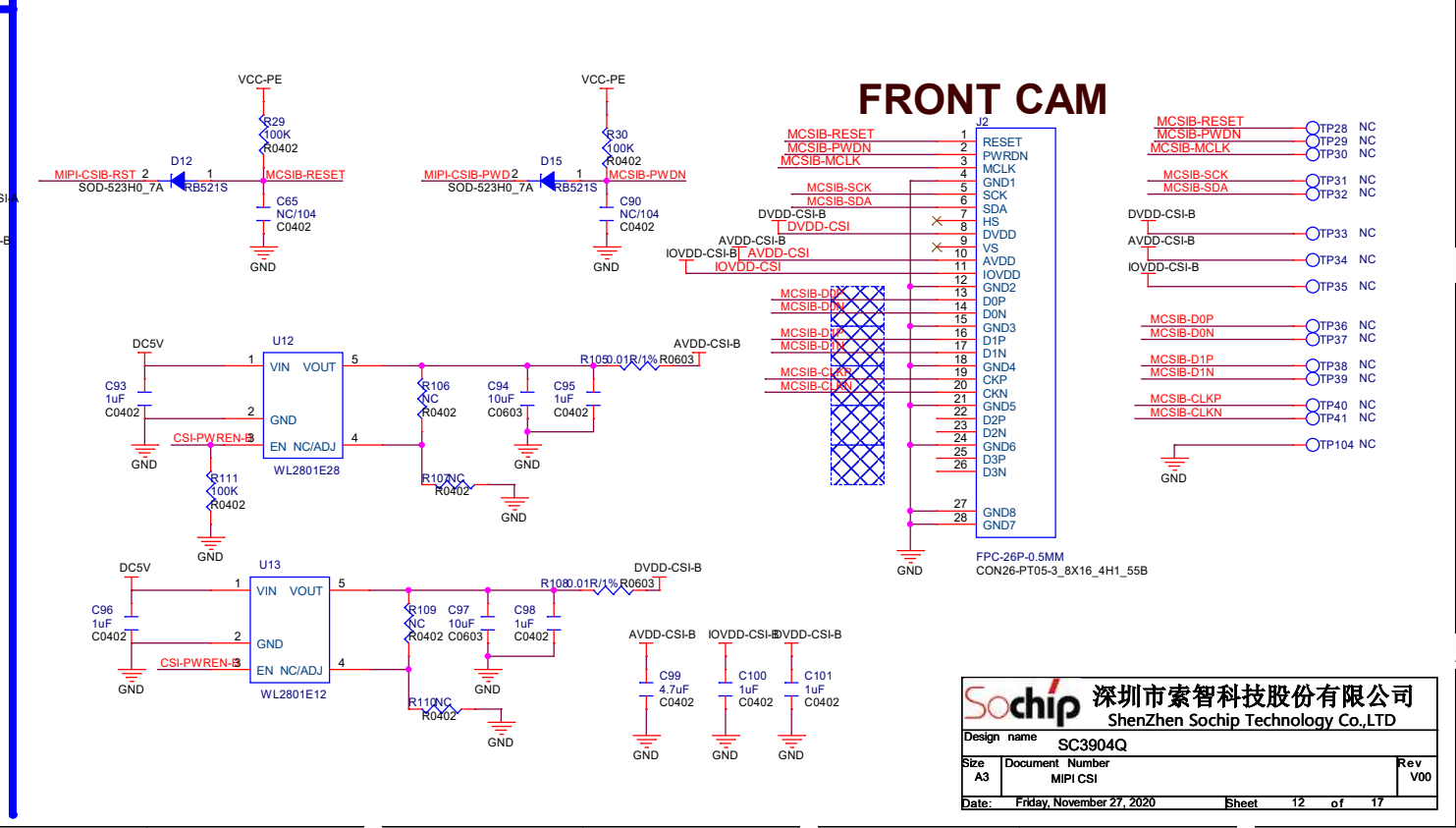
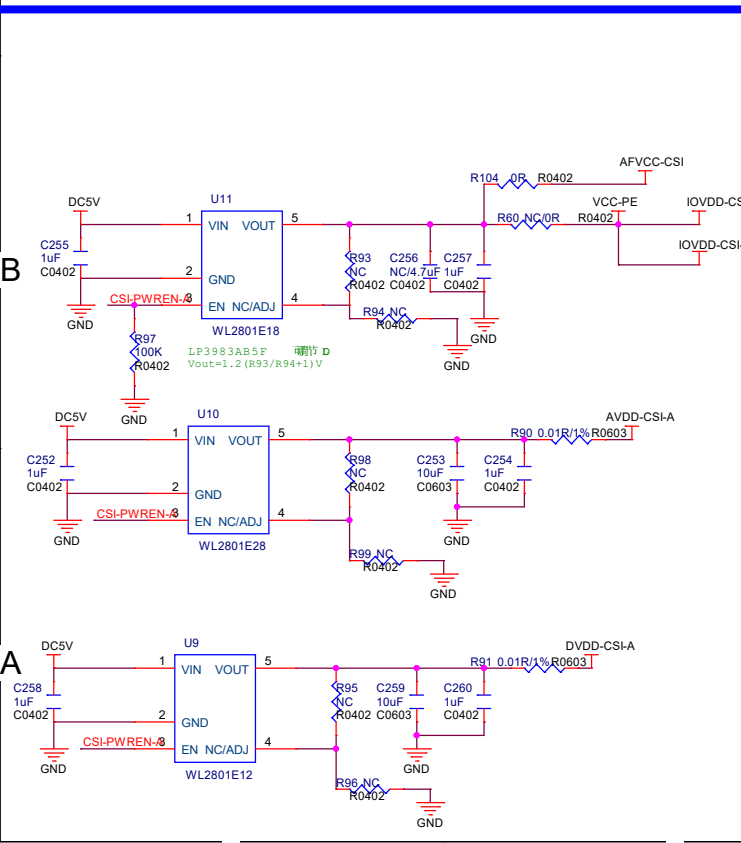
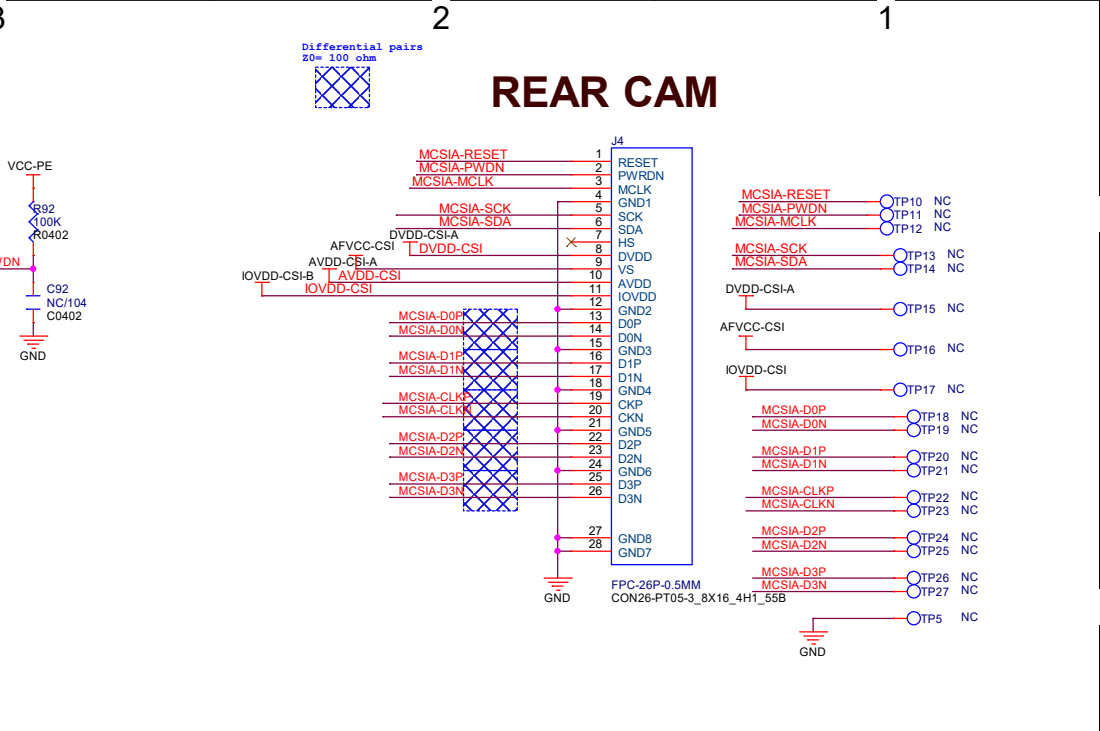
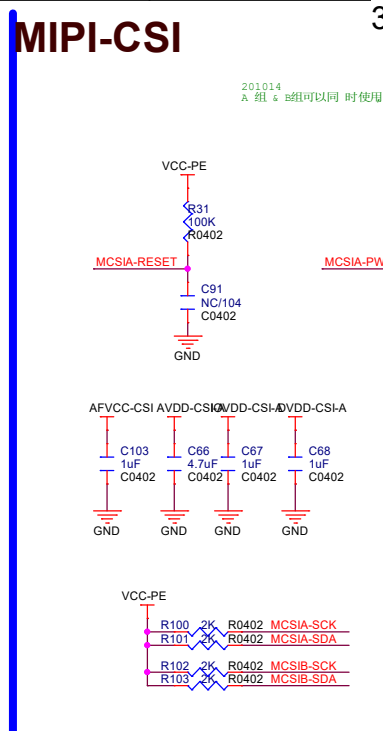
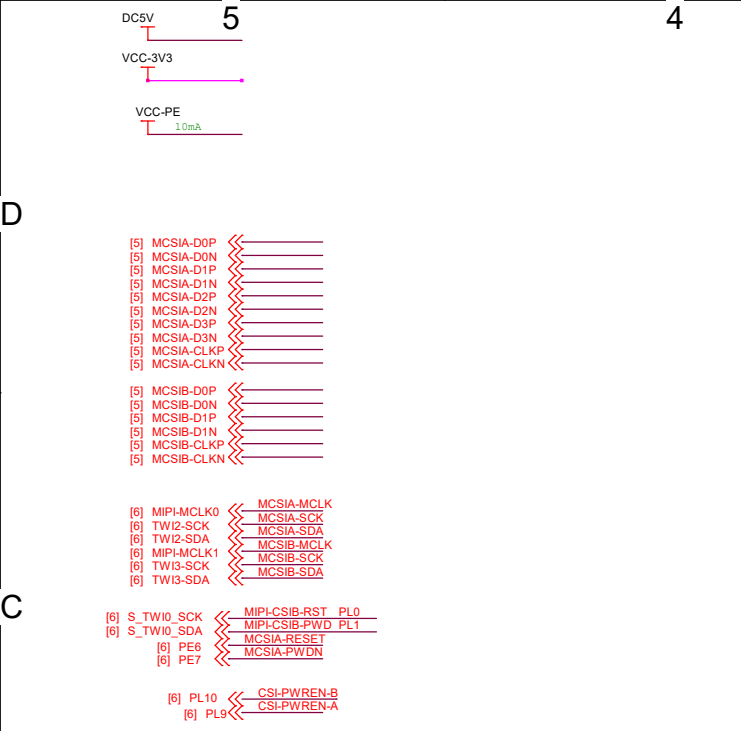
USB0 OTG



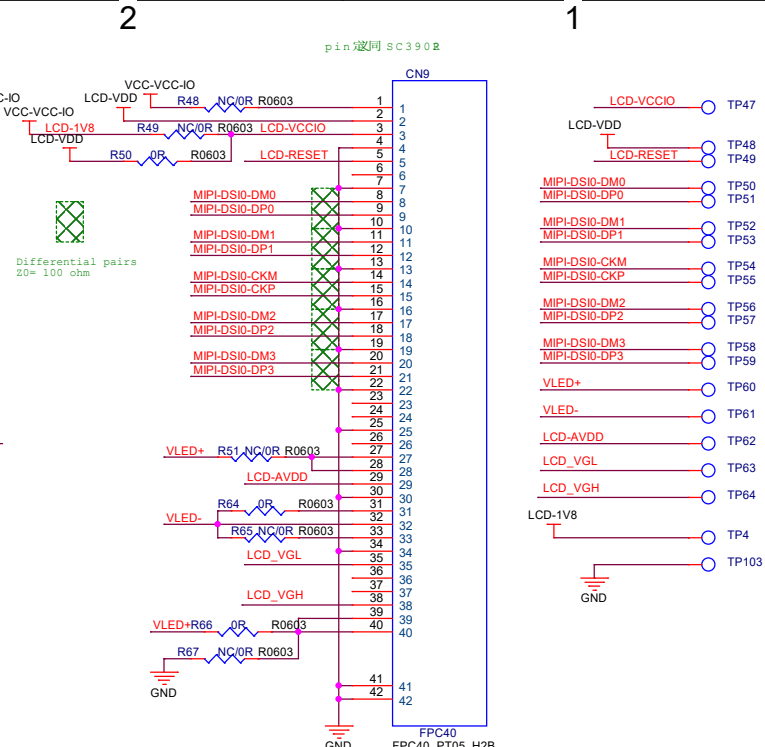
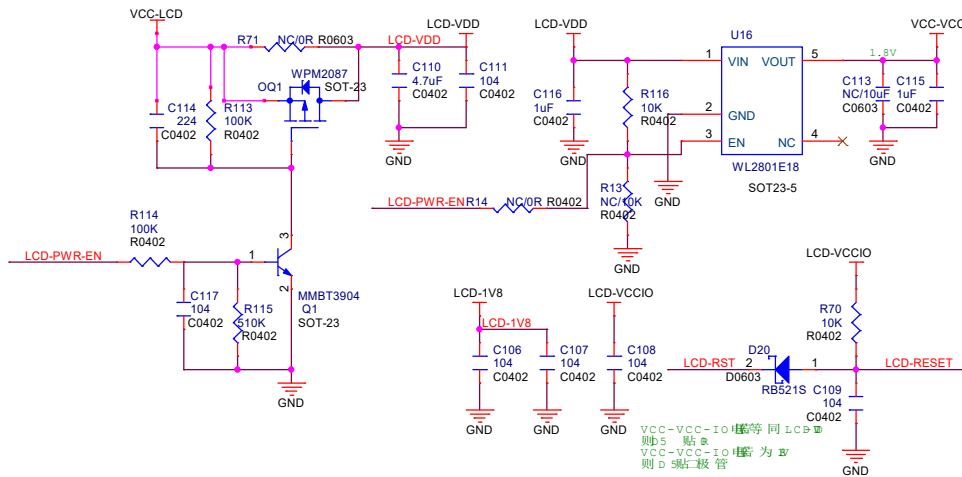
USB1 HOST



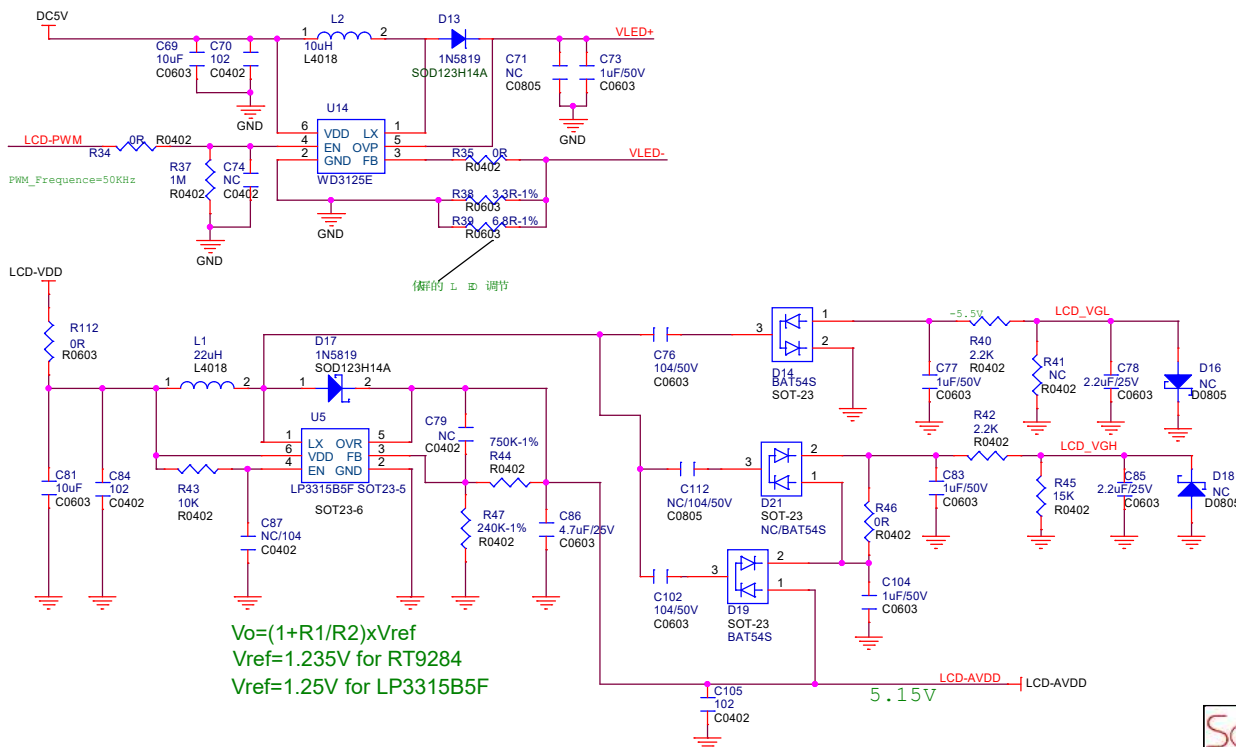
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 ShenZhen Sochip Technology Co.,LTD
 Design name SC3904Q
 Size A3 Document Number USB/DEBUG/TF card Rev V00
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MIPI/LVDS0/MCU LCD



BACKLIGHT



$$V_o = (1 + R_1/R_2) \times V_{ref}$$

$V_{ref} = 1.235V$ for RT9284
 $V_{ref} = 1.25V$ for LP3315B5F

- [6] LCD0-D2 MIPI-DSIO-DP0 LVDS0-D0P
- [6] LCD0-D3 MIPI-DSIO-DM0 LVDS0-D0N
- [6] LCD0-D4 MIPI-DSIO-DP1 LVDS0-D1P
- [6] LCD0-D5 MIPI-DSIO-DM1 LVDS0-D1N
- [6] LCD0-D6 MIPI-DSIO-CKP LVDS0-D2P
- [6] LCD0-D7 MIPI-DSIO-CKM LVDS0-D2N
- [6] LCD0-D8 MIPI-DSIO-DP2 LVDS0-D2P
- [6] LCD0-D9 MIPI-DSIO-DM2 LVDS0-D2N
- [6] LCD0-D10 MIPI-DSIO-CKM LVDS0-D3P
- [6] LCD0-D11 MIPI-DSIO-CKP LVDS0-D3N
- [6] LCD0-D12 MIPI-DSIO-DM3 LVDS0-D3P
- [6] LCD0-D13 MIPI-DSIO-DM3 LVDS0-D3N
- [6.13] LCD-RST LCD-RST
- [6.13] LCD-PWM LCD-PWM
- [6.13] LCD-PWR-EN LCD-PWR-EN

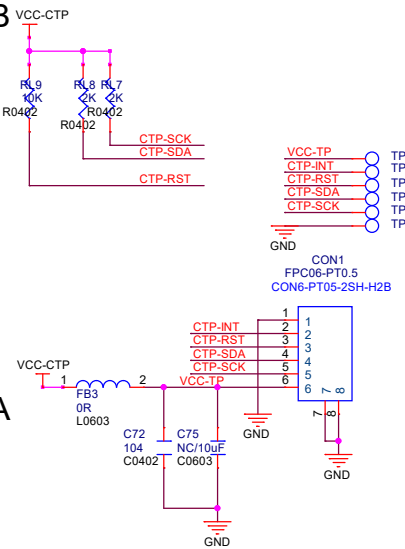
- [6.10] TWI1-SCK CTP-SCK
- [6.10] TWI1-SDA CTP-SDA
- [6] CTP-INT CTP-INT
- [6] CTP-RST CTP-RST

VCC-CTP
I_{MAX}=50mA

VCC-LCD
I_{MAX}=0.2A

DC5V
I_{MAX}=0.5A

CTP



Sochip 深圳市索智科技股份有限公司
ShenZhen Sochip Technology Co.,LTD

Design name: SC3904Q

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RGB LCD & Double LVDS

- [6] LCD1-D0 << LVDS2-D0P
- [6] LCD1-D1 << LVDS2-D0N
- [6] LCD1-D2 << LVDS2-D1P
- [6] LCD1-D3 << LVDS2-D1N
- [6] LCD1-D4 << LVDS2-D2P
- [6] LCD1-D5 << LVDS2-D2N
- [6] LCD1-D6 << LVDS2-CKP
- [6] LCD1-D7 << LVDS2-CKN
- [6] LCD1-D8 << LVDS2-D3P
- [6] LCD1-D9 << LVDS2-D3N
- [6] LCD1-D10 << LVDS3-D0P
- [6] LCD1-D11 << LVDS3-D0N
- [6] LCD1-D12 << LVDS3-D1P
- [6] LCD1-D13 << LVDS3-D1N
- [6] LCD1-D14 << LVDS3-D2P
- [6] LCD1-D15 << LVDS3-D2N
- [6] LCD1-D16 << LVDS3-CKP
- [6] LCD1-D17 << LVDS3-CKN
- [6] LCD1-D18 << LVDS3-D3P
- [6] LCD1-D19 << LVDS3-D3N
- [6] LCD1-D20 << LCD1-D20
- [6] LCD1-D21 << LCD1-D21
- [6] LCD1-D22 << LCD1-D22
- [6] LCD1-D23 << LCD1-D23
- [6] LCD1-CLK << LCD1-CLK
- [6] LCD1-DE << LCD1-DE
- [6] LCD1-HSYNC << LCD1-HSYNC
- [6] LCD1-VSYNC << LCD1-VSYNC

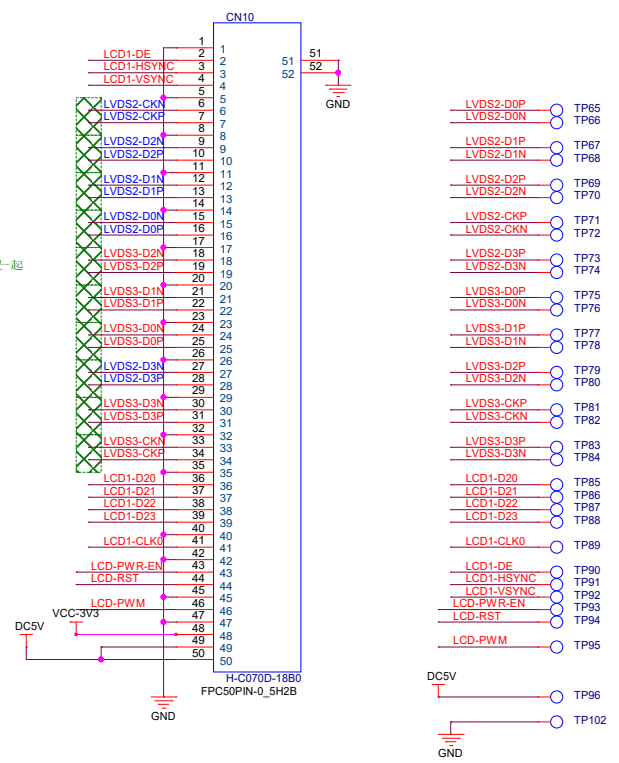
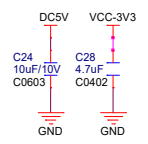
- [6,12] LCD-RST << LCD-RST
- [6,12] LCD-PWM << LCD-PWM
- [6,12] LCD-PWR-EN << LCD-PWR-EN

LCD1-CLK0 33R RW9 LCD1-CLK0
RW9 close to CPU

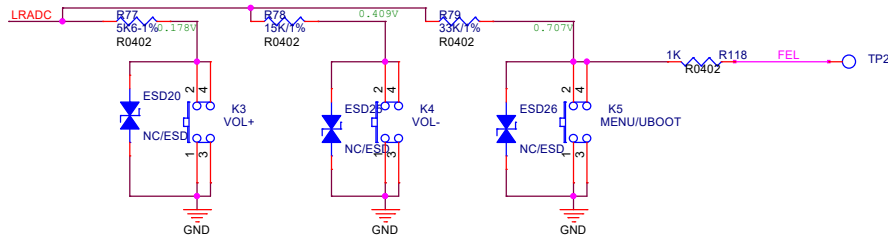
屏资源不 确定 预备
外接 寸板



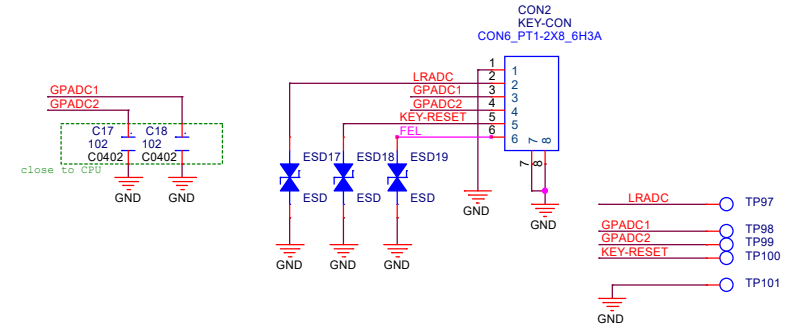
注意：LVDS组与LVDS组连线因错开段放在一起



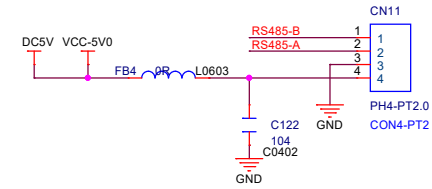
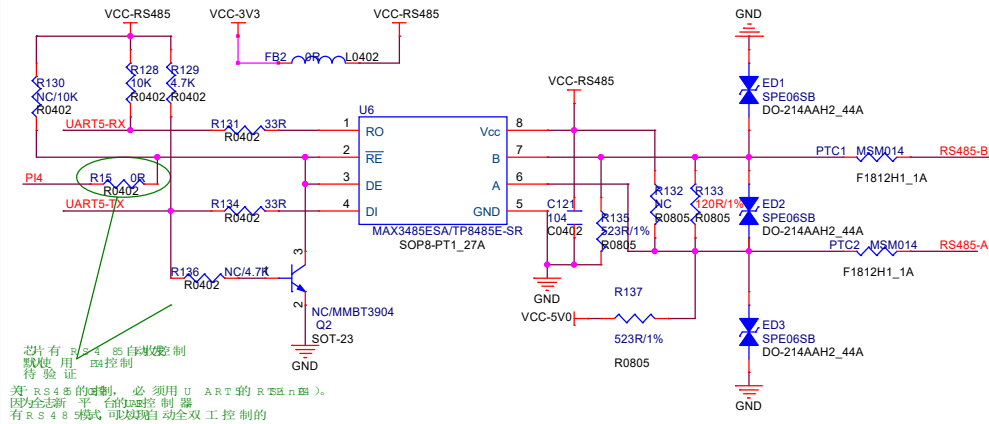
KEY



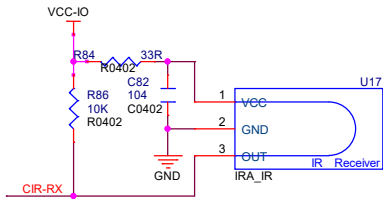
KEY ENTEND&ADC CON

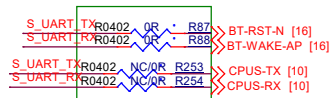
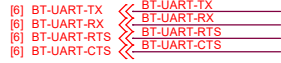


RS485

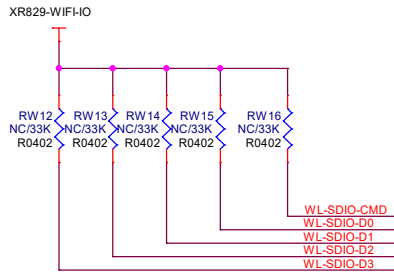


CIR

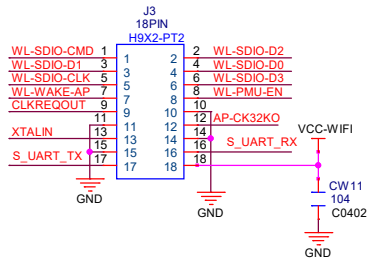




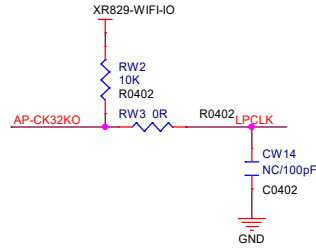
WIFI用WIFI
需用CPUS-TX/CPUS-RX Deb g
脚253,R254 0R; R87,R88 NC



SD EXTENSION

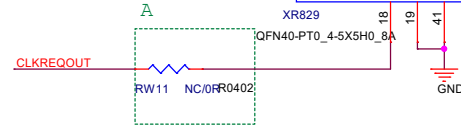
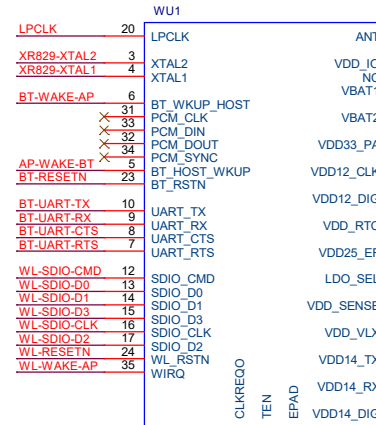
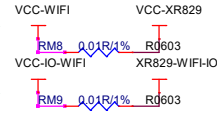


XR829

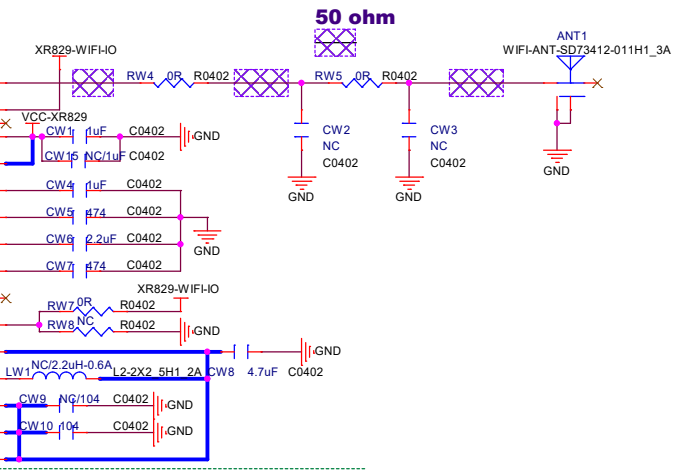


2.7-5.5V 400mA

3.3/1.8V 10mA



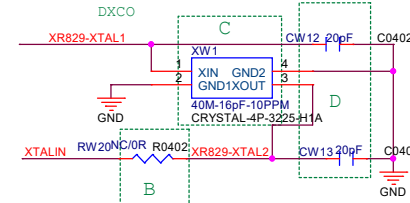
NOTE: Place capacitors near the IC



NOTE:

若24MHz 频率精度,可 选贴 40MHz 晶体

24M/40MHz Crystal source	A	B	C	D
Crystal	NC	NC	24M-16pF-10PPM 40M-15pF-10PPM	CW12=20pF, CW13=20pF
DCXO-RFCLK	0R	0R	NC	CW12=0R, CW13=NC



XR829 must be used in conjunction with this crystal :
E33840B043015, Ct=20pF

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