1/3” D1 CMOS Image Sensor

GC0403

DataSheet

Released V1.0

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GalaxyCore Inc.

Content

1. Sensor Overview

1.1 General Description

The GC0403 features 768V x 576H resolution with 1/3-inch optical format, and 4-transistor pixel structure for low light image quality and low noise variations.

The full scale integration of high-performance and low-power functions makes the GC0403 best fit the design, and reduce implementation process. The superior image quality in both low light and high dynamic range scene makes it the perfect choice for a wide range of applications, including surveillance, automobile and D1 video.

It provides RAW10 and RAW8 data formats with MIPI interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/3 inch
- Output formats: Raw Bayer 10bit/8bit
- Power supply requirement: AVDD: 3.0~3.6V
  DVDD: 1.7~1.9V
  IOVDD: 1.7~3.6V
- PLL support
- Full size @ 60fps
- Windowing support
- MIPI interface support
- Horizontal/Vertical mirror
- Image processing module
- High sensitivity for low-light operation

- Package: CSP

1.3 Application

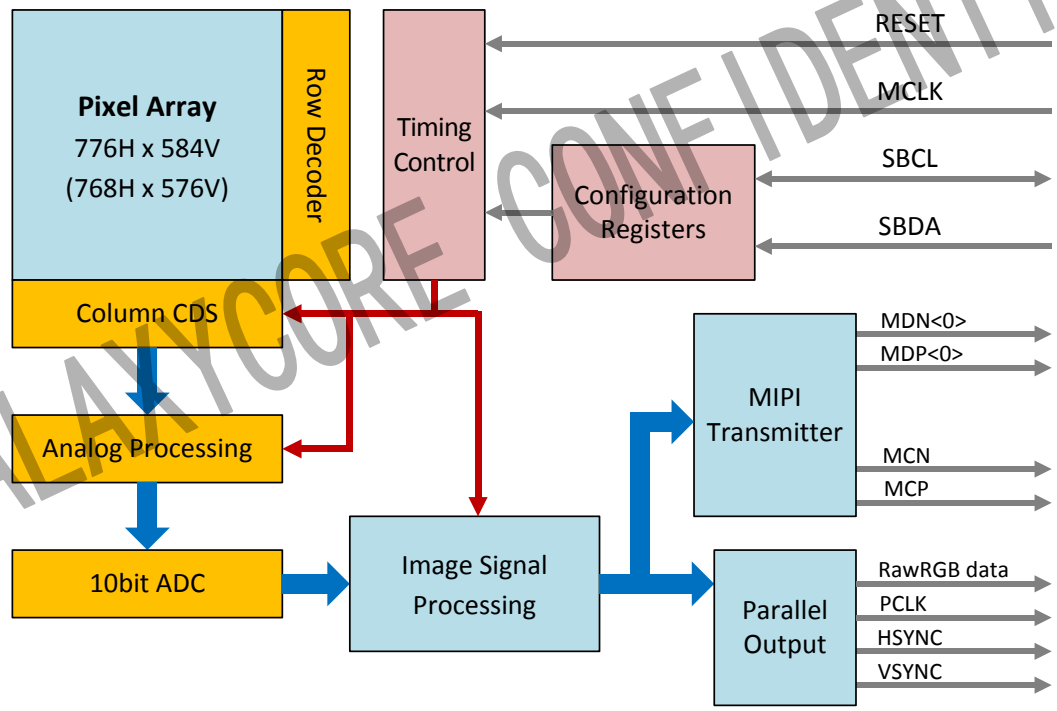
- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipments
- Security systems
- Industrial and environmental systems
- Automobile video recorder

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/3 inch
Pixel Size	6.25um x 6.25um
Active pixel array	776 x 584
ADC resolution	10 bit ADC
Max Frame rate	Full size@60fps
Power Supply	AVDD: 3.0~3.6V DVDD: 1.7~1.9V IOVDD: 1.7~3.6V
Power Consumption	TBD
SNR	76db
Dark Current	50mV/s@60C
Sensitivity	TBD
Operating temperature:	-30~70℃
Stable Image temperature	0~50℃
Optimal lens chief ray angle(CRA)	12° (non-linear)
Package type	CSP

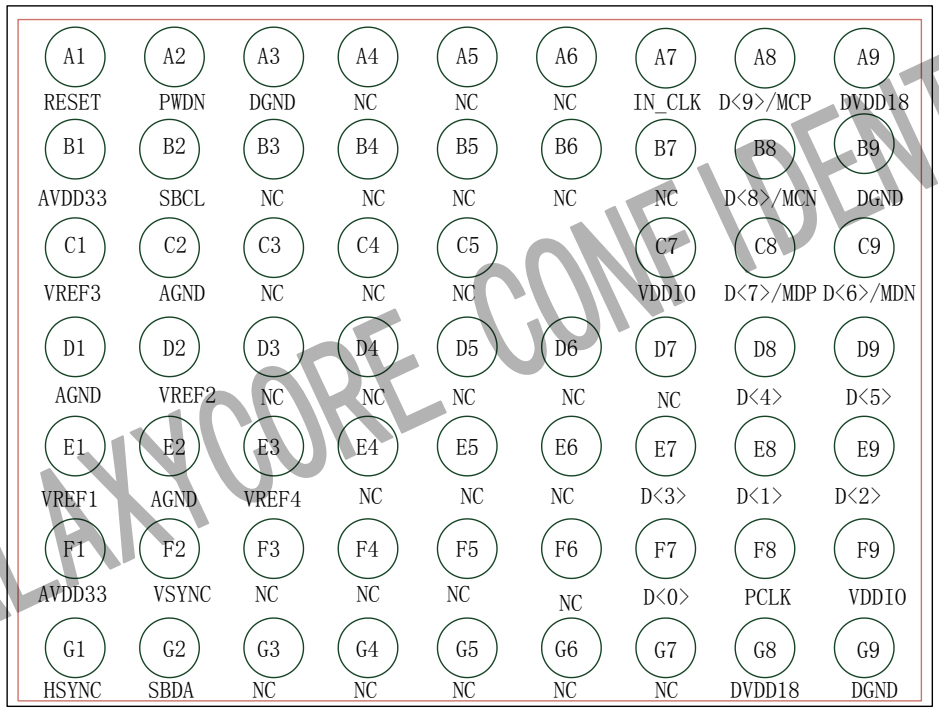
2. Block Diagram

2.1 Block Diagram



GC0403 has an active image array of 776x584 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bit A/D converter. The digital signals are processed in the ISP Block. Users can easily control these functions via two-wire serial interface bus.

2.2 Pin Diagram



Top View

2.3 Signal Descriptions

	Name	Pin Type	Function
A1	**RESETB**	Input	Chip reset control: 0: chip reset 1: normal work
A2	**PWDN**	Input	Sensor power down control: 0: normal work 1: standby
A3	**DGND**	Ground	DGND
A7	**INCLK**	Input	Input clock
A8	**D<9>**	Output	Raw RGB data output bit[9]
	MCP	Output	MIPI clock (+)
A9	**DVDD**	Power	Power for digital core: 1.7~1.9V, please connect capacity to ground.
B1	**AVDD33**	Power	Analog power: 3.0~3.6V, please connect capacity to ground.
B2	**SBCL**	Input	Two-wire serial bus, clock
B8	**D<8>**	Output	Raw RGB data output bit[8]
	MCN	Output	MIPI clock (-)

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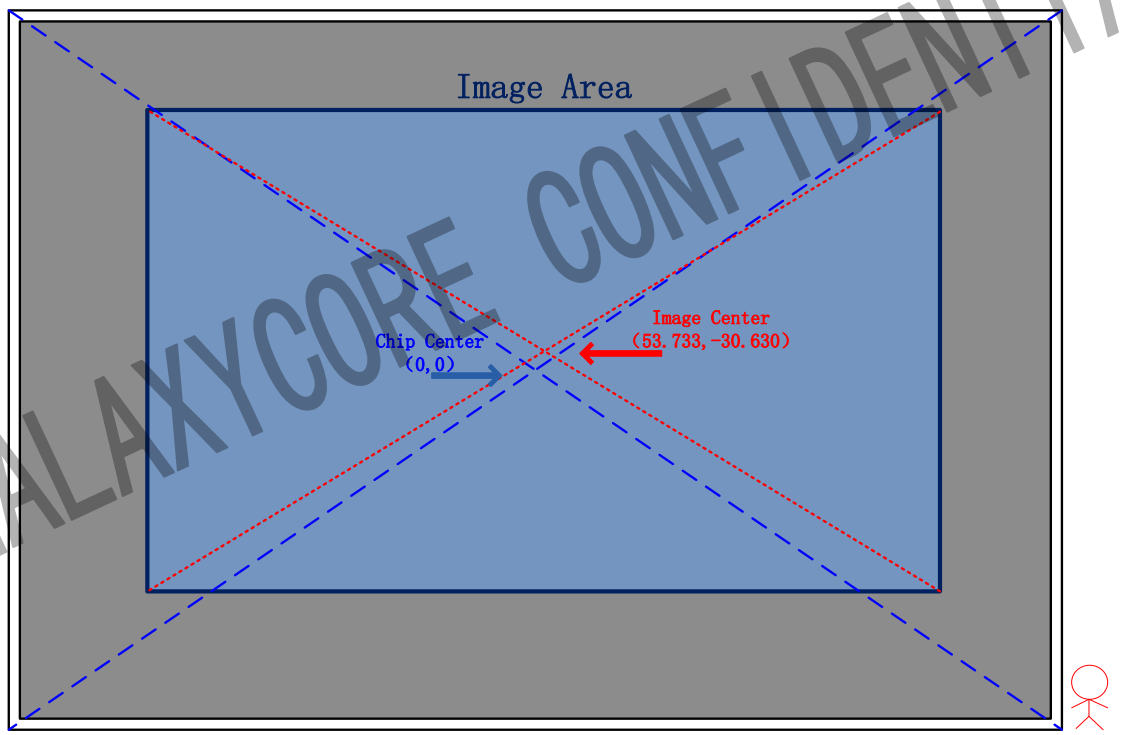
B9	**DGND**	Ground	DGND
C1	**VREF3**	Reference	Reference voltage, please connect capacity to ground.
C2	**AGND**	Ground	AGND
C7	**IOVDD**	Power	Power supply for I/O circuits: 1.7~3.6V, please connect capacity to ground.
C8	**D<7>**	Output	Raw RGB data output bit[7]
	MDP	Output	MIPI data<0> (+)
C9	**D<6>**	Output	Raw RGB data output bit[6]
	MDN	Output	MIPI data<0> (-)
D1	**AGND**	Ground	AGND
D2	**VREF2**	Reference	Reference voltage, please connect capacity to ground.
D8	**D<4>**	Output	Raw RGB data output bit[4]
D9	**D<5>**	Output	Raw RGB data output bit[5]
E1	**VREF1**	Reference	Reference voltage, please connect capacity to ground.
E2	**AGND**	Ground	AGND
E3	**VREF4**	Reference	Reference voltage, please connect capacity to ground.
E7	**D<3>**	Output	Raw RGB data output bit[3]
E8	**D<1>**	Output	Raw RGB data output bit[1]
E9	**D<2>**	Output	Raw RGB data output bit[2]
F1	**AVDD33**	Power	Analog power: 3.0~3.6V, please connect capacity to ground.
F2	**VSYNC**	Output	VSYNC output
F7	**D<0>**	Output	Raw RGB data output bit[0]
F8	**PCLK**	Output	Pixel clock output
F9	**VDDIO**	Power	Power supply for I/O circuits: 1.7~3.6V, please connect capacity to ground.
G1	**HSYNC**	Output	HSYNC output
G2	**SBDA**	I/O	Two-wire serial bus, data
G8	**DVDD18**	Power	Power for digital core: 1.7~1.9V, please connect capacity to ground.
G9	**DGND**	Ground	DGND

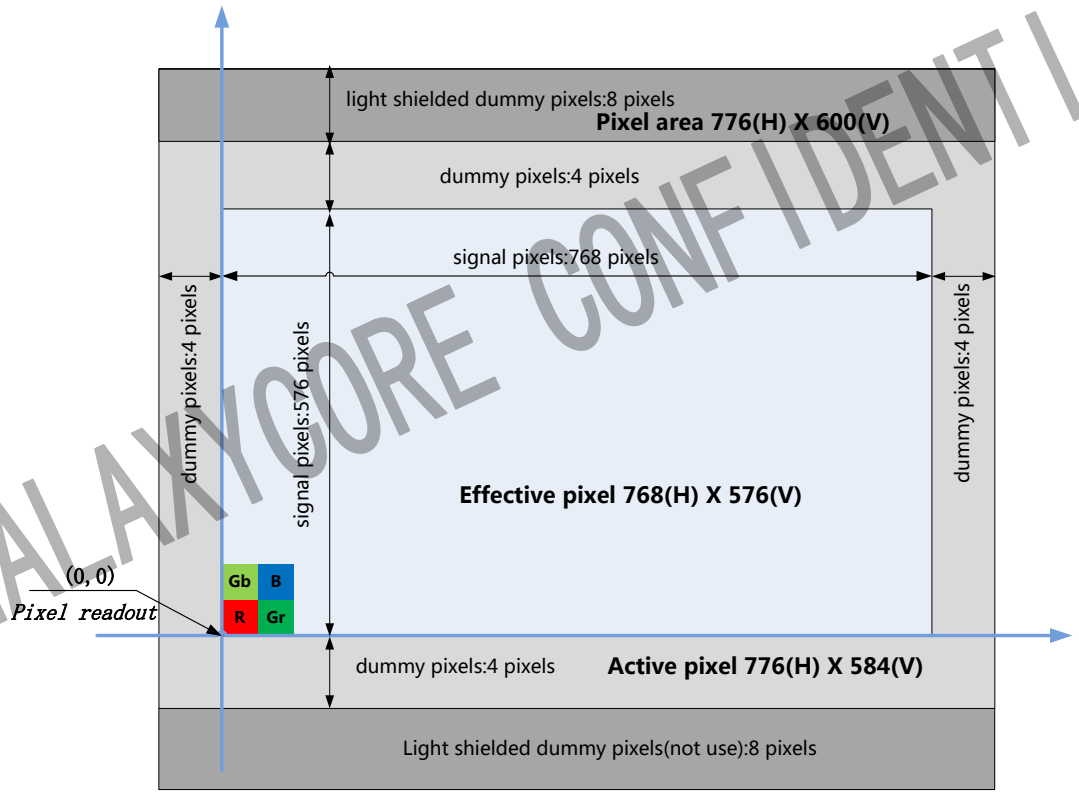
- **10-bit output (RAW): D<9>~D<0>.**
- **8-bit output (RAW): D<9>~D<2>.**

3. Optical Specifications

3.1 Sensor Array Center



3.2 Pixel Array

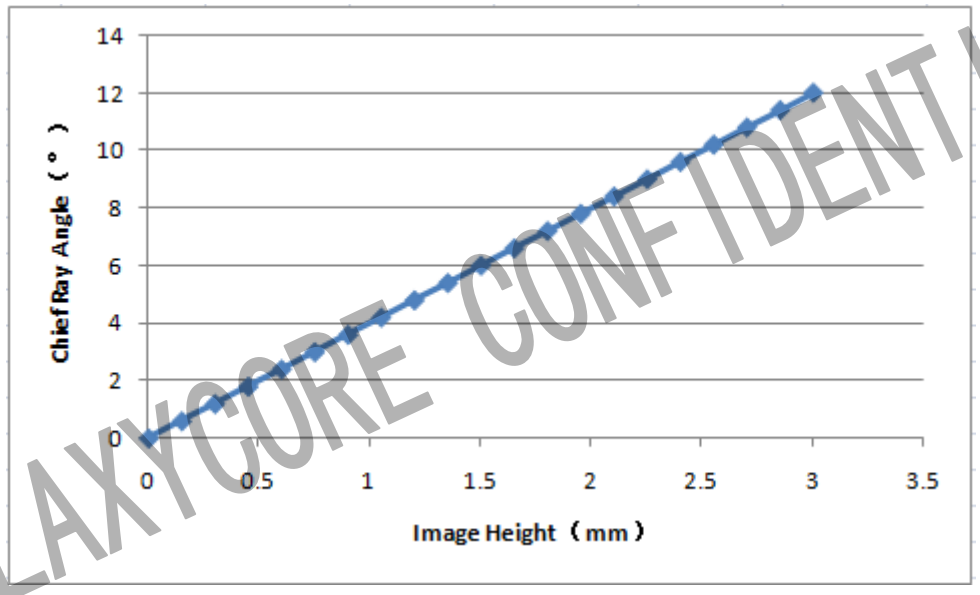


Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 775. If flip in column, column is read out from 775 to 0.

If no flip in row, row is read out from 0 to 583.If flip in row, row is read out from 583 to 0.

3.3 Lens Chief Ray Angle (CRA)

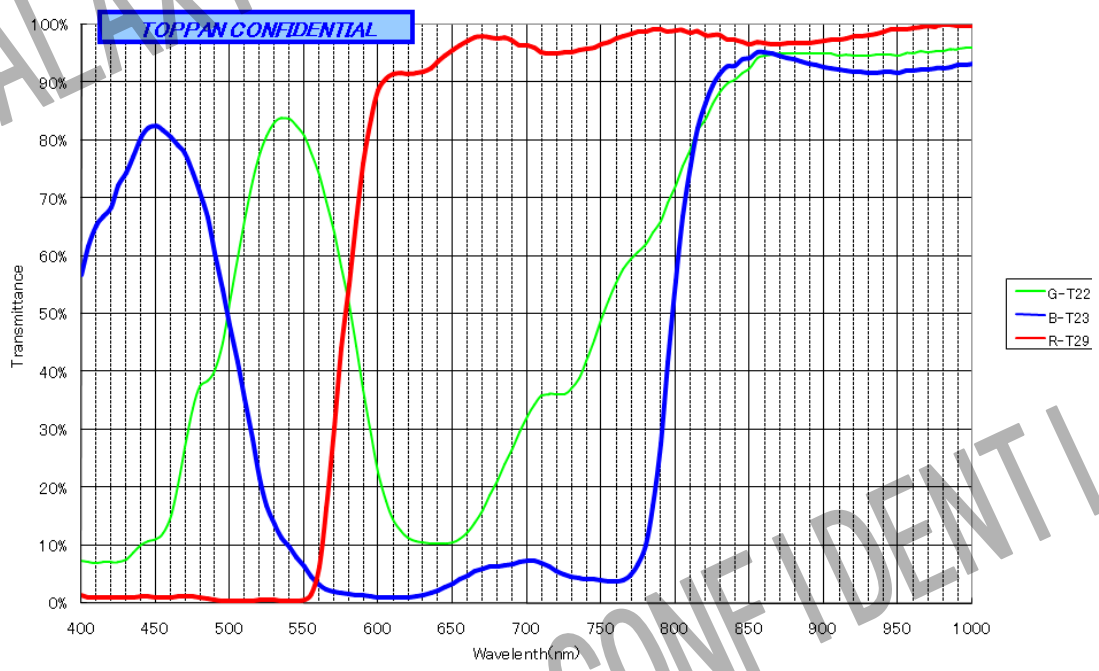


Field(%)	Image Height(mm)	CRA(degrees)
0	0	0
5	0.150144	0.6
10	0.300288	1.2
15	0.450432	1.8
20	0.600576	2.4
25	0.75072	3
30	0.900864	3.6
35	1.051008	4.2
40	1.201152	4.8
45	1.351296	5.4
50	1.50144	6
55	1.651584	6.6
60	1.801728	7.2
65	1.951872	7.8
70	2.102016	8.4
75	2.25216	9

80	**2.402304**	**9.6**
85	**2.552448**	**10.2**
90	**2.702592**	**10.8**
95	**2.852736**	**11.4**
100	**3.00288**	**12**

3.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below



4. Two-wire Serial Bus Communication

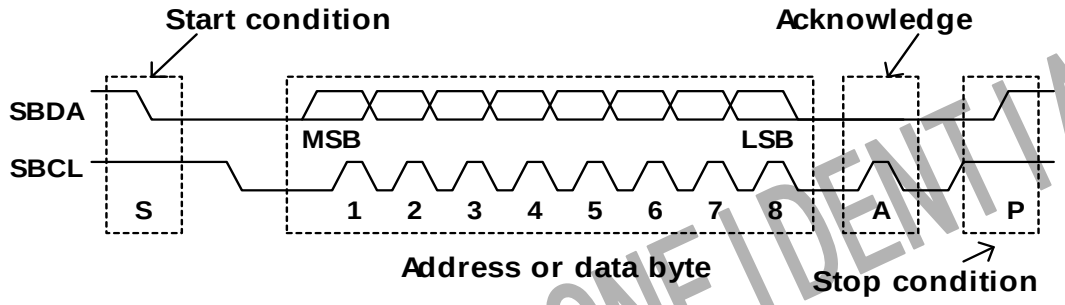
GC0403 Device Address:

serial bus write address = 0x78, serial bus read address = 0x79

4.1 Protocol

The host must perform the role of a communications master and GC0403 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**.



Single Register Writing:

S	78H	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	78H	A	Register Address	A	Data(1)	A	.....	Data(N)	A	P

Single Register Reading:

S	79H	A	Register Address	A	S	79H	A	Data	NA	P

Notes:

From master to slave

From slave to master

S: Start condition

P: Stop condition

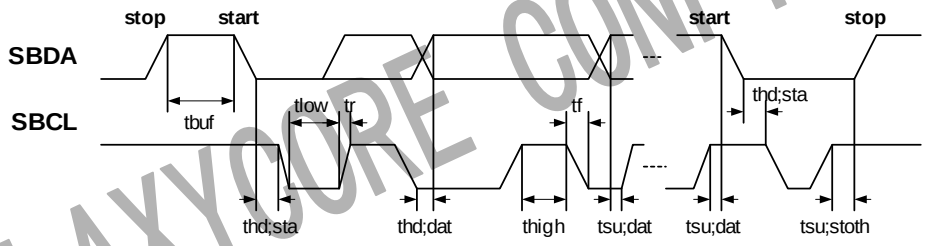
A: Acknowledge bit

NA: No acknowledge

Register Address: Sensor register address

Data: Sensor register value

4.2 Serial Bus Timing



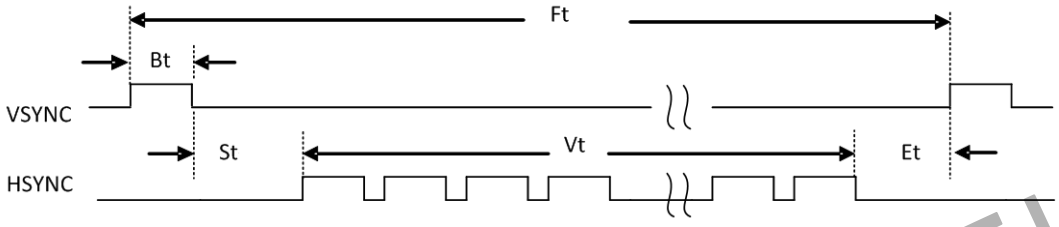
Parameter	Symbol	Min.	Max.	Unit
SBCL clock frequency	fscl	0	--	400
Bus free time between a stop and a start	tbuf	1.3	--	--
Hold time for a repeated start	thd;sta	0.6	--	--
LOW period of SBCL	tlow	1.3	--	--
HIGH period of SBCL	thigh	0.6	--	--

Set-up time for a repeated start	tsu;sta	0.6	--	--
Data hold time	thd;dat	0	--	0.9
Data Set-up time	tsu;dat	100	--	--
Rise time of SBCL, SBDA	tr	--	--	300
Fall time of SBCL, SBDA	tf	--	--	300
Set-up time for a stop	tsu;sto	0.6	--	--
Capacitive load of bus line (SBCL, SBDA)	Cb	--	--	--

5. Applications

5.1 DVP Timing

Suppose Vsync is low active and Hsync is high active, and output format is RAW Bayer 10bit/8bit, then the timing of Vsync and Hsync is bellowing (take capture mode for example, preview mode is the same):



Ft =VB+ Vt +8(darkrow_line) (unit is row_time)

VB+8= Bt + St + Et, Vblank/Dummy line, setting by register P0:0x07 and P0:0x08.

Ft -> Frame time, one frame time.

Bt -> Blank time, Vsync no active time.

St -> Start time, setting by register P0:0x13.

Et –> End time, setting by register P0:0x14.

Vt -> valid line time. Vt = win_height, win_height is setting by register P0:0x0d and P0:0x0e.

When exp_time ≤ win_height+VB+8, Bt = VB+8 – St - Et. Frame rate is controlled by window_height + VB+8.

When exp_time > win_height + VB, Bt = exp_time - win_height – St - Et.

Frame rate is controlled by exp_time.

The following is row_time calculate:

row_time = (Hb + Sh_delay + win_width /2+ 4)/HPCLK.

Hb –> HBlank or dummy pixel，Setting by register P0:0x05 and P0:0x06.

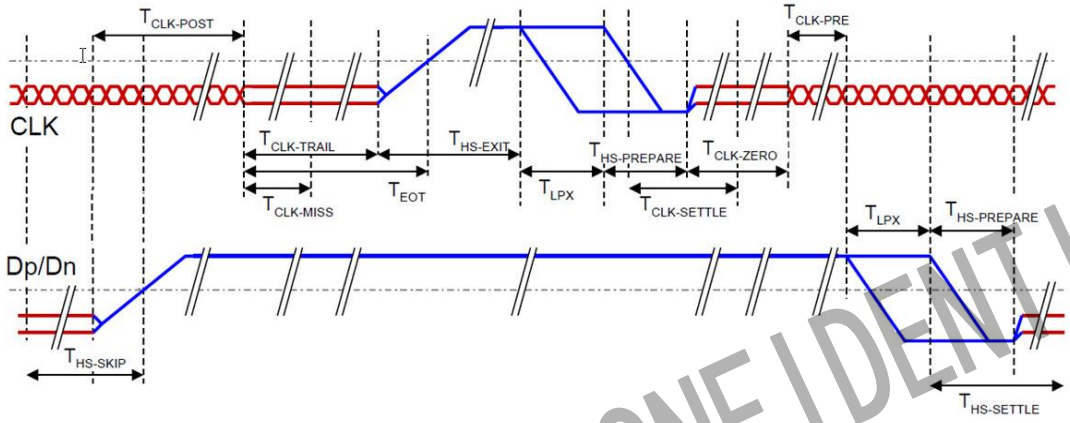
Sh_delay -> Setting by register P0:0x12.

win_width -> Setting by register P0:0x0f and P0:0x10, win_width = final_output_width + 8. So for D1, we should set win_width as 776.

HPCLK -> half PCLK.

5.2 MIPI

5.2.1 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

T_{CLK_PRE}: setting by Register P3: 0x24

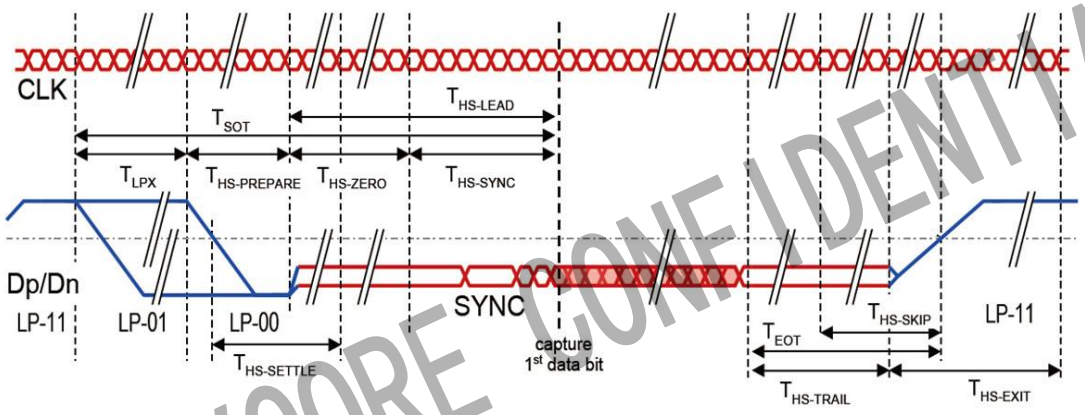
$T_{CLK\_HS\_PRE}$: setting by Register P3: 0x22

T_{CLK_POST} : setting by Register P3: 0x25

T_{CLK_ZERO}: setting by Register P3: 0x23

T_{CLK_TRAIL}: setting by Register P3: 0x26 s

5.2.2 Data Burst



Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

  T_{LPX}: setting by Register P3:0x21

  $T_{HS\_PREPARE}$: setting by Register P3: 0x29

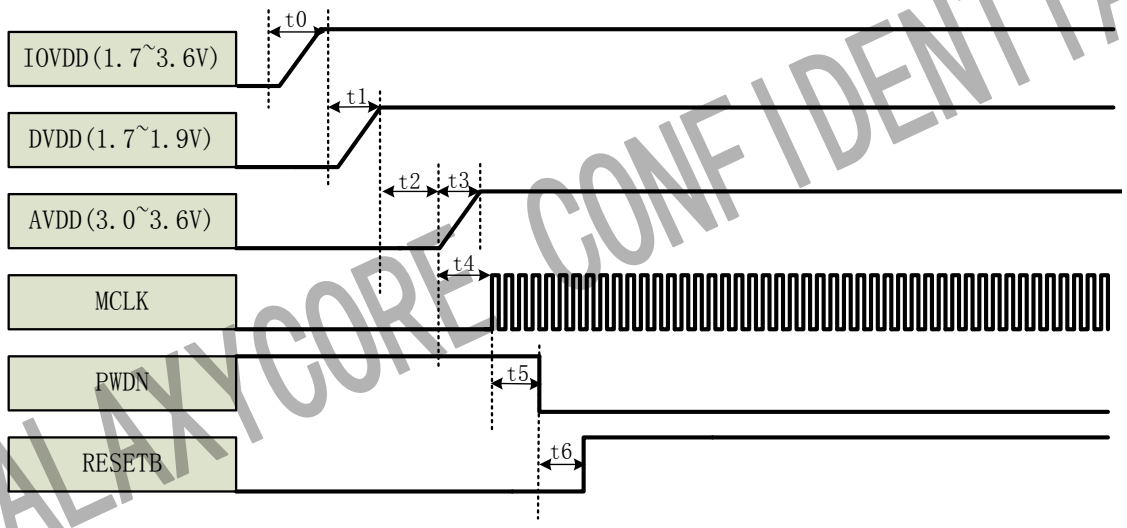
  T_{HS_ZERO}: setting by Register P3: 0x2a

  T_{HS_TRAIL}: setting by Register P3: 0x2b

  T_{HS_EXIT}: setting by Register P3: 0x27

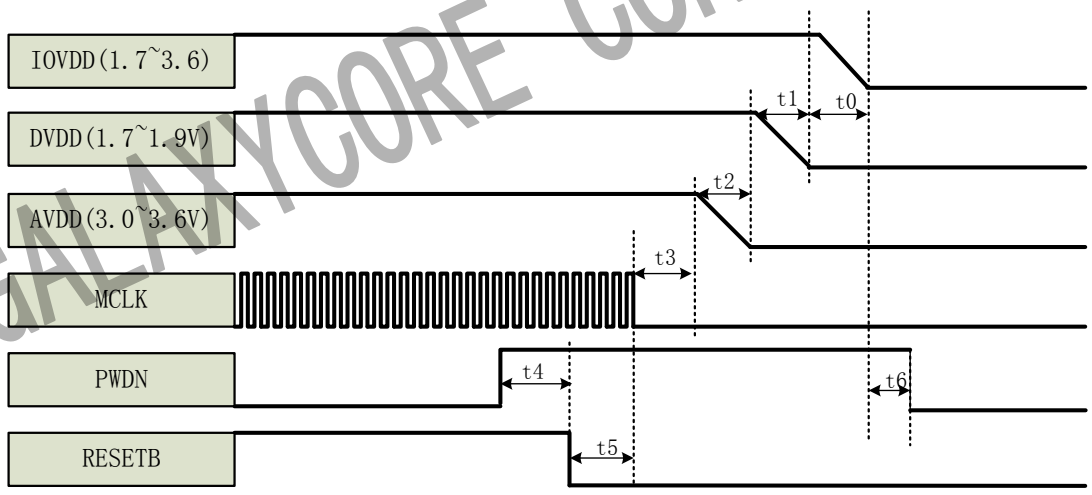
5.3 Power On/Off Sequence

5.3.1 Power On Sequence



Parameter	Description	Min.	Max.	Unit
t0	IOVDD rising time	50		us
t1	From IOVDD to DVDD	0		us
t2	From DVDD to AVDD	50		us
t3	AVDD rising time	50		
t4	From AVDD to MCLK applied	0		us
t5	From MCLK applied to Sensor enable	0		us
t6	From PWDN pull low to RESET pull high	0		us

5.3.2 Power Off Sequence



Parameter	Description	Min.	Max.	Unit

t0	From DVDD to IOVDD falling time	0		us
t1	From AVDD to DVDD falling time	0		us
t2	AVDD falling time	0		us
t3	From MCLK disable to sensor AVDD power down	0		us
t4	From sensor disable to RESET pull low	0		us
t5	From sensor RESET pull low to MCLK disable	0		us
t6	From power Off to PWDN pull low	0		us

- **Recommended power on/off sequence is above.**
- **If you have special requirements in application, please contact with us to confirm.**

5.4 DC Parameters

Supply					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_{AVDD}	Power supply	3.0	3.3	3.6	V
V_{DVDD}	Supply voltage(digital core)	1.7	1.8	1.9	V
V_{IOVDD}	Supply voltage(digital I/O)	1.7	3.3	3.6	V

DVP	**Symbol**		**Parameter**	**Min**	**Typ**	**Max**	**Unit**
	I_{AVDD}		Active(operating) current	-	28	35	mA
	I_{DVDD18}			-	15	20	mA
	I_{IOVDD}	1.8V		-	8	10	mA
		3.3V		-	18	25	mA
	I_{DDS_PWD}		Standby Current	TBD	TBD	TBD	uA

MIPI	**Symbol**		**Parameter**	**Min**	**Typ**	**Max**	**Unit**
	I_{AVDD}		Active(operating) current	-	28	35	mA
	I_{DVDD18}			-	25	35	mA
	I_{IOVDD}	1.8V		-	0.1	5	mA
		3.3V		-	0.2	5	mA
	I_{DDS_PWD}		Standby Current	TBD	TBD	TBD	uA

Digital Input(Typical conditions: AVDD=3.3V，DVDD=1.8V，IOVDD=3.3V)					
V_{IH}	Input voltage HIGH	2.4			V
V_{IL}	Input voltage LOW			0.6	V
Digital Output(AVDD=3.3V，standard Loading 25PF，IOVDD=3.3V)					
V_{OH}	Output voltage HIGH	3.0			V
V_{OL}	Output voltage LOW			0.2	V

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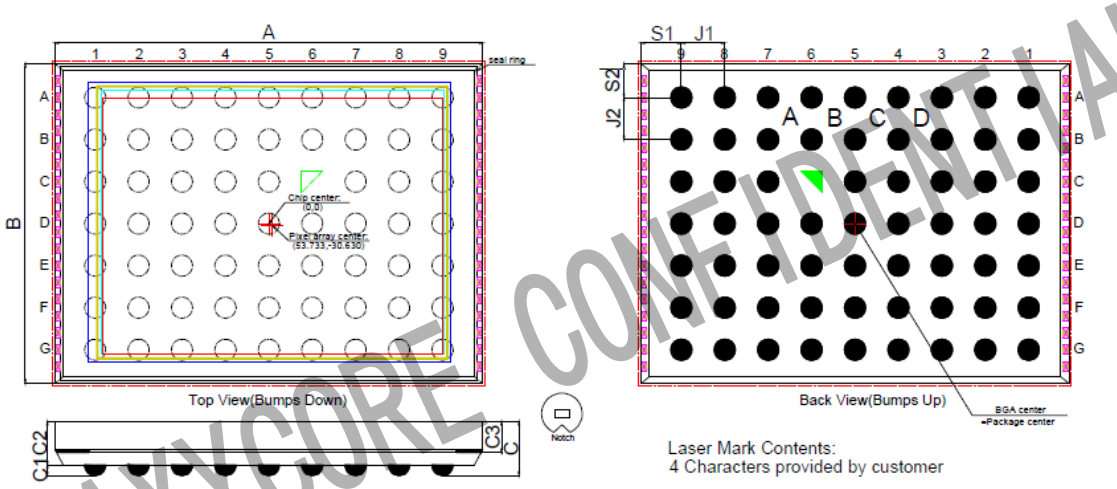
6. Package Specification



Parameter	Symbol	Nominal	Min.	Max.
		μm		
Package Body Dimension X	A	6110	6085	6135
Package Body Dimension Y	B	4560	4535	4585
Package Height	C	780	720	840
Ball Height	C1	160	130	190
Package Body Thickness	C2	620	585	655
Glass Thickness	C3	445	425	465
Ball Diameter	D	300	270	330
Total Pin Count	N	62		
Pins Count X axis	N1	9		
Pins Count Y axis	N2	7		
Pins Pitch X axis	J1	620		
Pins Pitch Y axis	J2	600		
Edge to Pin Center Distance along X	S1	575	545	605
Edge to Pin Center Distance along Y	S2	480	450	510

7. Register List

System Register

Address	Name	Width	Default Value	R/W	Description
0xf0	**Sensor_ID_high**	**8**	**0x04**	**RO**	**Sensor_ID**
0xf1	**Sensor_ID_low**	**8**	**0x03**	**RO**	**Sensor_ID**
0xf2	pad_buf_mode pad_vb_hiz_mode, data_pad_io sync_pad_io	6	0x20	RW	[5] pad_buf_mode [4] pad_vb_hiz_mode [3] data_pad_io [2:0] sync_pad_io 0: input 1: output
0xf3	I2C_open_ena	1	0x00	RW	[7:1] NA [0] I2C_open_en
0xf6	up_dn pwd_dn	6	0x00	RW	[7:6] NA [5:4] up_dn 00: not pull 01: pull down 10: pull up 11: illegal [3:1] NA [0] PWD dn 0: pull down 1: not pull
0xf7	PLL_mode1	8	0x10	RW	[7]dvpmode [6:4]serial clk div [3]clk_double [2]auto_div2en [1] div2en [0] pll_en
0xf8	PLL_mode2	8	0x00	RW	[7]div2 enable [6]div2_frame [5:0] divx4 eg:mclk 24 divx4=8 so pllclk_nodiv=24*8*4=768 for mipi pllclk=pllclk_nodiv/4=768/4=192
0xf9	Cm_mode	8	0x00	RW	[7]regf clk enable [6] use internal clk [5] NA

					[4] sync_use_pll_mode [3]isp all clock enable [2] NA [1]re_lock_pll [0]not_use_pll
0xfa	clk_div_mode	8	0x00	RW	[7:4] +1 represent the frequency division number / divide_by [3:0] represent the high level in one pulse after frequency division /clock duty MCLK by Div duty 0x11 2 1:1 0x21 3 1:2 0x22 3 2:1 0x31 4 1:3 0x32 4 2:2 0x33 4 3:1 …
0xfb	i2c_device_id	7		RO	[7:1] I2C device ID, can write once [0] NA
0xfc	analog_pwc	8	0x01	RW	[7:6]NA [5:4]vpll_r [3]vpll_en [2]vpix_en [1]NA [0] apwd --- Not wether which will cause suicide
0xfd	clk_div2_mode	8	0x11	RW	[7:4]divide_by [3:0]clock duty eg:pllclk=192
0xfe	Reset related page_select	8	0x00	RW	[7]soft_reset [6]cm_reset [5]mipi_reset [4]CISCTL_restart_n [3]spi_reset [2:0]page_select 00:REGF 01:REGF1 10:REGF2 11:BCR 111:is fpga

Analog & CISCTL

Address	Name	Width	Default Value	R/W	Description

P0:0x01	CISCTL_buf_exp2[12:8]	5	0x00	RW	[7:5] NA [4:0] exposure[12:8], use line processing time as the unit.
P0:0x02	CISCTL_buf_exp2[7:0]	8	0x04	RW	Exposure[7:0]
P0:0x03	CISCTL_buf_exp[12:8]	5	0x00	RW	[7:5] NA [4:0] exposure[12:8], use line processing time as the unit.
P0:0x04	CISCTL_buf_ex[7:0	8	0x10	RW	Exposure[7:0]
P0:0x05	HB[11:8]	4	0x00	RW	H Blanking [3:0] HB[11:8] [7:0] HB[7:0]
P0:0x06	HB[7:0]	8	0xa4	RW	
P0:0x07	VB[12:8]	5	0x00	RW	Vertical blanking, if current exposure < (Vb + window Height) , frame rate will be (Vb + window Height); otherwise frame rate will be determined by exposure
P0:0x08	VB[7:0]	8	0x10	RW	
P0:0x09	Row_start[9:8]	2	0x00	RW	Row Start
P0:0x0a	Row_start[7:0]	8	0x00	RW	
P0:0x0b	Col_start[9:8]	3	0x03	RW	Col start
P0:0x0c	Col_start[7:1]	8	0x00	RW	
P0:0x0d	win_height[9:8]	2	0x02	RW	[7:2] NA [1:0] Window height[9:8]
P0:0x0e	win_height[7:0]	8	0x40	RW	Window height[7:0]
P0:0x0f	win_width[9:8]	3	0x03	RW	[7:3] NA [2:0] Window width[10:8]
P0:0x10	win_width[7:1]	8	0x04	RW	window width[7:0]
P0:0x11	Reserved	8	0x44	RW	Reserved
P0:0x12	Reserved	8	0x18	RW	Reserved
P0:0x13	Reserved	8	0x11	RW	Reserved
P0:0x14	Reserved	8	0x01	RW	Reserved
P0:0x15	Reserved	8	0x00	RW	Reserved
P0:0x16	Reserved	8	0xc1	RW	Reserved
P0:0x17	Mirror & Flip	8	0X00	RW	[7:2]Reserved [1] updown [0] mirror
P0:0x18	Reserved	8	0x0a	RW	Reserved
P0:0x19	CISCTL_mode3	8	0x05	RW	[7:6]space width [5]capture_ad0_data_edge

					[4]capture_ad1_data_edge [3:0] AD_pipe_number
P0:0x1a	CISCTL_mode4	8	0x10	RW	[7:6]tx_mode [5]hsync_always [4]fix_fps [3]evenskip [2]switch sdark ndark addr [1:0]AD manual swtich mode [1]pixel
P0:0x1b	Rsh_width	8	0x33	RW	[7:4] tx_shs_width, [3:0] shs_width , X4
P0:0x1c	Tsp_width	8	0x09	RW	[7:2] tx_width [1:0] SFdown width
P0:0x1d	buf_CISCTL_reset_mode	8	0x20	RW	[7:5]hstart width [4] double reset [3]double reset tx [2] reset once more [1] rowse 0 mode [0] vsync_comb
P0:0x1e	Analog_mode1	8	0x90	RW	[7]txhigh_en [6:4]coln_r [3]rowclk_mode [2]rsthigh_en [1:0] coltest
P0:0x1f	Analog_mode2	8	0x08	RW	[7:6] rsgl_s_mode [5:4] vpix_s_mode [3] txlow_en [2:0] txlow_r3 000:-1.544 001:-1.399 010:-1.254 011:-1.108 100:-0.936 101:-0.818 110:-0.672 111:-0.527
P0:0x20	Analog_mode3	8	0x00	RW	[7:6] ref_r [5:4] sun_r [3:1] comv_r [0] adclk_mode
P0:0x21	Analog_Hrst_rsg	8	0x40	RW	[7] hrst, [6:4] da_rsg

					000:0.287 001:0.433 010:0.578 011:0.723 100:0.867 101:1.012 110:1.157 111:1.301 [3:2] rsvd [1:0] rsvu
P0:0x22	Analog_Vref_V25	8	0xb5	RW	[7] vref_en [6:4] da25_vref 000:2.986 001:3.134 010:3.281 011:3.428 100:3.574 101:3.72 110:3.866 111:4.012 [3]reset_one_more_row [2:0]vpix_r 000:2.187 001:2.287 010:2.387 011:2.487 100:2.587 101:2.687 110:2.787 111:2.887
P0:0x23	Analog_ADC_r	8	0x01	RW	[7:3] opa_r 00:IREF(default) 01:1.5*IREF 10:2*IREF 11:2.5*IREF [2] gate_AD_clk [1:0] sRef 00:1.5 01:1.6 10:1.7(default) 11:1.8
P0:0x24	ANALOG_PAD_	8	0x55	RW	[7:6] data_low_drv

	drv				[5:4] sync_drv [3:2] data_high_drv [1:0] pclk_drv
P0:0x25	ANALOG_ADC_TEST_mode	8	0x00	RW	[7:6] txl_s_mode [5] T2 allow tail [4] isp_quiet_mode [3:2] sth_s_mode [1:0] ad0test_en
P0:0x26	buf_CISCTL_shs_10	2	0x00		buf_CISCTL_shs_10
P0:0x27	CISCTL_rowsg_tx_mode	8	0x01	RW	[7] bypass exp2 [6] hdr all output [5:4] txl_drv_mode [3] shs_from_shr_mode [2] ndark_actually_sdark [1:0]ifast
P0:0x28	CISCTL_dummy_width	8	0x10	RW	[7:0] CISCTL_dummy_width
P0:0x29	buf_CISCTL_mode5	8	0x80	RW	[7]CISCTL_ndark_tx_off_mode [6]rowskip_new_mode [5]capture_sun0_edge [4]capture_sun1_edge [3:2]restg_mode [1:0] vpix_bs
P0:0x2a	Analog_mode6	8	0x00	RW	[7:6]sr_s_mode [5:4]sv_s_mode [3:2]srh_s_mode [1:0]stl_s_mode
P0:0x2b	Analog_mode4	8	0xe0	RW	[7:6]pxd_s_mode [5:4]sf_s_mode [3:2]pb1sw_mode [1:0]NBD_s_mode
P0:0x2c	Analog_mode7	8	0x58	RW	[7] vrefrh_en [6:4] rsgh_r 000:2.675 001:2.822 010:2.968 011:3.114 100:3.26 101:3.406 110:3.551 111:3.697

					[3:2] ispg [1] pwd_rc [0] rst_rc
P0:0x2d	NBD_s_width	8	0x14	RW	[7:4] pre_NBD_s_width [3:0] NBD s width
P0:0x2e	Analog_mode8	8	0x02	RW	[7:6]dcgl_s_mode [5:4]dcgh_s_mode [3]txlow_sw [2:0]txhigh_r 000:0.144 001:0.289 010:0.433 011:0.578 100:0.723 101:0.867 110:1.012 111:1.157
P0:0x2f	CISCTL_reset_tx_width	8	0x12	RW	[7:0] CISCTL_reset_tx_width
P0:0x30	ANALOG_PGA_gain0	6	0x20	RW	int+pga 1*1
P0:0x31	ANALOG_PGA_gain1	6	0x21	RW	1*sqrt(2)
P0:0x32	ANALOG_PGA_gain2	6	0x22	RW	1*2
P0:0x33	ANALOG_PGA_gain3	6	0x01	RW	1*2*sqrt(2)
P0:0x34	ANALOG_PGA_gain4	6	0x02	RW	2*2
P0:0x35	ANALOG_PGA_gain5	6	0x03	RW	2*2*sqrt(2)
P0:0x36	ANALOG_PGA_gain6	6	0x04	RW	2*2*2
P0:0x37	ANALOG_PGA_gain7	6	0x5	RW	2*2*2*sqrt(2)
P0:0x38	ANALOG_PGA_gain8	6	0x06	RW	2*2*2*2
P0:0x39	ANALOG_PGA_gain9	6	0x07	RW	2*2*2*2*sqrt(2)
P0:0x3a	ANALOG_PGA_gaina	6	0x0f	RW	2*2*2*2*2 //max 32
P0:0x3b	ANALOG_PGA_	6	0x17	RW	2*2*2*2*2 //max 32

	gainb				
P0:0x3c	ANALOG_PGA_gainc	6	0x1f	RW	
P0:0x3d	CISCTL_DCG	8	0x00	RW	[7]dcgh_en [6:4]dcgh_r 000:2.986 001:3.134 010:3.281 011:3.428 100:3.574 101:3.72 110:3.866 111:4.012 [3]dcgl_en [2:0]dcgl_r 000:-1.544 001:-1.399 010:-1.254 011:-1.108 100:-0.963 101:-0.818 110:-0.672 111:-0.527
P0:0x3e	ANALOG_mode9	8	0x45	RW	[7:6] dcg_adv [5:4] dcg_delay [3:2] SFdown_first_delay [1:0] SFdown_second_delay
P0:0x3f	ANALOG_mode5	8	0x04	RW	[7:6]NA [5]pgsf_bypass [4]EQ_SEL [3:2]pgclamp [1:0]pgsf_sw_mode
P0:0x4d	Reserved	7	0x00	RW	Reserved

CSI/PHY1.0

Address	Name	Width	Default Value	R/W	Description
P3:0x01	DPHY_analog_mode1	8	0x00	RW	[7]clklane_p2s_sel [6] CTD_lane1 [5] CTD_lane0 [4] CTD_clk

					[2] PHY_lane1_en [1] PHY_lane0_en [0] PHY_clk_en
P3:0x02	DPHY_analog_mode2	8	0x00	RW	[6:4] lane0_diff [2:0] clk_diff
P3:0x03	DPHY_analog_mode3	8	0x00	RW	[5] lane0_delay [4] clk_delay [3] NA [2]lpldo_en [1:0]lpldo_r
P3:0x04	FIFO_prog_full_level[7:0]	8	0x01	RW	FIFO_prog_full_level[7:0]
P3:0x05	FIFO_prog_full_level[11:8]	4	0x00	RW	[7:4] NA [3:0] FIFO_prog_full_level[11:8]
P3:0x06	FIFO_mode	8	0x04	RW	[7] MIPI_CLK_MODULE [6] manual CSI2_up mode [5]no flop mode [4]fifo_rst_mode [3:2]FIFO write read gate mode [1] NA [0] mipi_write_gate mode
P3:0x10	buf_CSI2_mode	8	0x00	RW	[7] lane_ena [6] NA [5] ULP_mode [4] MIPI_ena [3] bit10_swicth [2] RAW8 [1] line_sync_mode [0] double_lane
P3:0x11	LDI_set	8	0x2b	RW	RAW10
P3:0x12	LWC_set[7:0]	8	0xc0	RW	768x5/4 RAW10
P3:0x13	LWC_set[15:8]	8	0x03	RW	768x5/4 RAW10
P3:0x14	SYNC_set	8	0xb8	RW	SYNC_set
P3:0x15	DPHY_mode	8	0x00	RW	[7]DATA gate mode [6]quiet or lien rise [5]delay cnt [4] 1 adv trigger 0 prog [3]lane0_switch_msb [2]clk_switch_msb [1:0] clklane_mode
P3:0x16	LP_set	8	0x09	RW	[7:6] hi-z [3:2] 1

					[1:0] 0
P3:0x20	T_init_set	8	0x80	RW	Timing of initial setting, more than 100 us
P3:0x21	T_LPX_set	8	0x10	RW	Timing of LP setting, more than 50ns
P3:0x22	T_CLK_HS_PREPARE_set	8	0x05	RW	Timing of COCLK HS PREPARE setting, 38ns ~95ns LP00
P3:0x23	T_CLK_zero_set	8	0x30	RW	Timing of COCLK HS zero setting, more than 300ns
P3:0x24	T_CLK_PRE_set	8	0x02	RW	Timing of COCLK HS PRE of Data setting, more than 8UI
P3:0x25	T_CLK_POST_set	8	0x10	RW	Timing of COCLK HS Post of Data setting, 60ns +52UI
P3:0x26	T_CLK_TRAIL_set	8	0x08	RW	Timing of COCLK tail setting, 60ns
P3:0x27	T_HS_exit_set	8	0x10	RW	Timing of HS exit setting, more than 100ns
P3:0x28	T_wakeup_set	8	0xa0	RW	Timing of wakeup setting, 1ms
P3:0x29	T_HS_PREPARE_set	8	0x06	RW	Timing of data HS PREPARE setting, 45+4UI~85+5UI
P3:0x2a	T_HS_Zero_set	8	0x0a	RW	Timing of data HS zero setting, 140ns
P3:0x2b	T_HS_TRAIL_set	8	0x08	RW	Timing of data HS trail setting, 60ns
P3:0x30	MIPI_test	2	0x00	RW	[7:2] NA [1:0] MIPI_test
P3:0x31	MIPI_test_data0	8	0x96	RW	MIPI_test_data0
P3:0x32	MIPI_test_data1	8	0x3a	RW	MIPI_test_data1
P3:0x33	MIPI_test_data2	8	0x87	RW	MIPI_test_data2
P3:0x34	MIPI_test_data3	8	0xb5	RW	MIPI_test_data3
P3:0x35	hsync_in_start_4_5_cnt_num[7:0]	8	0x08	RW	hsync_in_start_4_5_cnt_num[7:0]
P3:0x36	hsync_in_start_4_5_cnt_num[9:8]	2	0x00	RW	[7:2] NA [1:0] hsync_in_start_4_5_cnt_num[9:8]
P3:0x3f	fifo_error log	2		RO	fifo_error log
P3:0x40	output_buf_m	8	0x00	RW	[7:4] start_mode

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	ode1				[3] dummy mode [2:1]delay_half [0] buf enable
P3:0x41	output_buf_mode2	8	0x00	RW	[4] buf 8 bit mode [3] dummy pclk mode [2] clk gating [1] pclk_polarity [0] hsync_polarity
P3:0x42	buf_win_width[7:0]	8	0x20	RW	[7:0] buf_win_width[7:0]
P3:0x43	buf_win_width[10:8]	3	0x00	RW	[7:3] NA [2:0] buf_win_width[10:8]

ISP Related

Address	Name	Width	Default Value	R/W	Description
P0:0x7b	Reserved	8	0x00	RW	Reserved
P0:0x7c	Reserved	8	0x00	RW	Reserved
P0:0x7d	Reserved	8	0x00	RW	Reserved
P0:0x86	Reserved	8	0x00	RW	Reserved
P0:0x87	debug_mode4	8	0x00	RW	[7] clear frame_start_num =0 [6] AEC_delay_mode [5:4] fix_odd_even [3] OUT for SOC mode [2] protect_exp_mode [1:0] CISCTL_exp2_ratio
P0:0x88	Reserved	8	0x53	RW	Reserved
P0:0x89	Reserved	8	0x03	RW	Reserved
P0:0x8a	Reserved	8	0xbf	RW	Reserved
P0:0x8b	debug_mode1	8	0xa2	RW	[7:5]Reserved [4]test image in output [3:0]Reserved
P0:0x8c	debug_mode2	8	0x07	RW	[7]data_delay_half_2pclk [6]hsync_delay_half_2pclk [5]test_image when in VGA or UXGA,1:UXGA 0:VGA [4]input_test_image [3]cur_exp change => total gain swith [2]pclk_out_polarity [1]hsync_polarity [0]vsync_polarity
P0:0x8d	debug_mode3	8	0x03	RW	[7:4] test image fix value,

					[3] test image fix value mode [2:0] Reserved
P0:0x8e	Reserved	3	0x00	RW	Reserved
P0:0x8f	Reserved	7	0x12	RW	Reserved
P0:0x90	Crop_win_mode	2	0x01	RW	[7:1]NA [0] Crop out win mode
P0:0x91	out_win_y1[9:8]	2	0x00	RW	[7:2] NA [1:0] Crop _win_y1[9:8]
P0:0x92	out_win_y1[7:0]	8	0x00	RW	Crop _win_y1[7:0]
P0:0x93	out_win_x1[10:8]	3	0x00	RW	[7:3] NA [2:0] Crop _win_x1[10:8]
P0:0x94	out_win_x1[7:0]	8	0x00	RW	Crop _win_x1[7:0]
P0:0x95	out_win_height[9:8]	2	0x02	RW	[7:2] NA [1:0] Out window height[9:8]
P0:0x96	out_win_height[7:0]	8	0x40	RW	Out window height[7:0]
P0:0x97	out_win_width[10:8]	3	0x03	RW	[7:3] NA [2:0] Out window width[10:8]
P0:0x98	out_win_width[7:0]	8	0x00	RW	Out window width[7:0]
P0:0xef	Reserved	8		RO	Reserved

BLK

Address	Name	Width	Default Value	R/W	Description
P0:0x40	Blk_mode1	8	0x23	RW	[7:2]Reserved [1]dark_current_en [0]offset_en
P0:0x41	BLK_mode2	7	0x05	RW	Reserved
P0:0x42	Reserved	8	0xff	RW	Reserved
P0:0x5e	offset_ratio_G1_odd	6	0x18	RW	offset_ratio
P0:0x6a	manual_G1_odd_offset	6	0x00	RW	manual_G1_odd_offset S5, low align to 11
P0:0x6b	manual_G1_even_offset	6	0x00	RW	manual_G1_even_offset S5, low align to 11
P0:0x6c	manual_R1_odd_offset	6	0x00	RW	manual_R1_odd_offset S5, low align to 11
P0:0x6d	manual_R1_even_offset	6	0x00	RW	manual_R1_even_offset S5, low align to 11

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P0:0x6e	manual_B2_odd_offset	6	0x00	RW	manual_B2_odd_offset S5, low align to 11
P0:0x6f	manual_B2_even_offset	6	0x00	RW	manual_B2_even_offset S5, low align to 11
P0:0x70	manual_G2_odd_offset	6	0x00	RW	manual_G2_odd_offset S5, low align to 11
P0:0x71	manual_G2_even_offset	6	0x00	RW	manual_G2_even_offset S5, low align to 11

GLOBAL/PRE/POSTGAIN

Address	Name	Width	Default Value	R/W	Description
P0:0xa8	channel_gain_G1_odd	8	0x80	RW	G1 odd Channel gain
P0:0xa9	channel_gain_G1_even	8	0x80	RW	G1 even Channel gain
P0:0xaa	channel_gain_R1_odd	8	0x80	RW	R1 odd Channel gain
P0:0xab	channel_gain_R1_even	8	0x80	RW	R1 even Channel gain
P0:0xac	channel_gain_B2_odd	8	0x80	RW	B2 odd channel gain
P0:0xad	channel_gain_B2_even	8	0x80	RW	B2 even channel gain
P0:0xae	channel_gain_G2_odd	8	0x80	RW	G2 odd channel gain
P0:0xaf	channel_gain_G2_even	8	0x80	RW	G2 even channel gain
P0:0xb0	global_gain	8	0x40	RW	Global gain
P0:0xb1	auto_pregain_[9:6]	4	0x01	RW	[7:4] NA [3:0] Auto_pregain[9:6]
P0:0xb2	auto_pregain[5:0]	6	0x00	RW	[7:2] Auto_pregain[5:0] [1:0] NA
P0:0xb3	AWB_R_gain	8	0x40	RW	AWB_R_gain
P0:0xb4	AWB_G_gain	8	0x40	RW	AWB_G_gain
P0:0xb5	AWB_B_gain	8	0x40	RW	AWB_B_gain
P0:0xb6	Col_code	8	0x00	RW	[7:4] ANALOG_GAIN_for_exp2 [3:0] ANALOG_GAIN_for normal
P0:0xb7	buf_freq_div2	1	0x00	RW	[7:1] NA [0] freq_div2
P0:0xb8~	col_gain0	8	0x10	RW	col_gain

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0xbf					
P0:0x80~ 0x85	col_gain	8	0x00	RW	col_gain
P0:0xa5~ 0xa7	col_gain]	8	0x00	RW	col_gain

DARK SUN CORRECTION

Address	Name	Width	Default Value	R/W	Description
P0:0xe9	dark_sun_en	7	0x27	RW	[7:6]NA [5] darksun enable [4:0]NA
P0:0xea	Reserved	8	0xf0	RW	Reserved
P0:0xeb	Reserved	6	0x03	RW	Reserved
P0:0xec	Reserved	8	0xff	RW	Reserved
P0:0xed	Reserved	6	0x00	RW	Reserved
P0:0xee	Reserved	8	0x14	RW	Reserved
P0:0xc0	Reserved	8	0x80	RW	Reserved
P0:0xc1	Reserved	8	0x00	RW	Reserved
P0:0xc2	Reserved	8	0x20	RW	Reserved
P0:0xc3	Reserved	8	0x00	RW	Reserved
P0:0xcc	Reserved	8	0x10	RW	Reserved
P0:0xcd	Reserved	8	0x20	RW	Reserved
P0:0xdc	Reserved	8		RO	Reserved
P0:0xde	Reserved	7		RO	Reserved

Revision History

Version TBD 2014.12.04

- Document Release