X2000

IoT Application Processor

Programming Manual

Release Date: Jan 17, 2020



北京君正集成电路股份有限公司

Ingenic Semiconductor Co.,Ltd.

X2000/E IoT Application Processor

Programming Manual

Copyright © 2005-2020 Ingenic Semiconductor Co. Ltd. All rights reserved.

Disclaimer

This documentation is provided for use with Ingenic products. No license to Ingenic property rights is granted. Ingenic assumes no liability, provides no warranty either expressed or implied relating to the usage, or intellectual property right infringement except as provided for by Ingenic Terms and Conditions of Sale.

Ingenic products are not designed for and should not be used in any medical or life sustaining or supporting equipment.

All information in this document should be treated as preliminary. Ingenic may make changes to this document without notice. Anyone relying on this documentation should contact Ingenic for the current documentation and errata.

Ingenic Semiconductor Co., Ltd.

Ingenic Headquarters, East Bldg. 14, Courtyard #10,
XIbeiwang East Road, Haidian District, Beijing 100193, China,
Tel: 86-10-56345000
Fax: 86-10-56345001
Http: //www.ingenic.com

CONTENTS

CONTENTS i

TABLES i

FIGURES i

OVERVIEW 1

1 Overview 2

1.1 Block Diagram 2
1.2 Features 2
1.2.1 CPU Core 2
1.2.2 Video Process Unit(VPU) ..... 错误!未定义书签。
1.2.3 Image Signal Processor(ISPx2) ..... 错误!未定义书签。
1.2.4 Memory Interface ..... 错误!未定义书签。
1.2.5 Audio ..... 错误!未定义书签。
1.2.6 MIPI-CSI ..... 错误!未定义书签。
1.2.7 Camera ..... 错误!未定义书签。
1.2.8 Display ..... 错误!未定义书签。
1.2.9 System Functions ..... 错误!未定义书签。
1.2.10 Peripherals ..... 错误!未定义书签。
1.2.11 Bootrom ..... 错误!未定义书签。

CORE FUNCTIONS 10

2 CPU 11

2.1 Overview 11
2.2 Features of XBurst®2 CPU 11
2.3 Operating Modes 12

3 Multiple Channel Scaler (MScaler) 13

3.1 Overview 13
3.2 Features 13
3.3 Block Diagram 13
3.4 Functional Description 14
3.4.1 Input 14
3.4.2 Resize Function 15
3.4.3 Frame rate control function 15
3.4.4 Crop Function 15
3.4.5 Cover(Mask) Function 16

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.4.6 FLIP and MIRROR Function 16
3.4.7 Scaler resize coefficient configure 16
3.4.8 Reset 17
3.4.9 Enable 、Disable and the Status of each channel 17
3.4.10 Work-flow 17
3.4.11 Interrupt 17
3.4.12 DMAOUT working mechanism 18
3.4.13 Frame number 18
3.4.14 Output resolution reconfigure 18
3.5 Pins Description 18
3.6 Register Description 18
3.6.1 Register Memory Map 19
3.6.2 Register and Fields Description 23
3.7 Index 99
4 Video Interface Control (VIC) 100
4.1 Overview 100
4.2 Features 100
4.2.1 VIC features 100
4.3 Interface Timing 101
4.3.1 DVP 101
4.3.2 BT 102
4.4 Data Format 103
4.4.1 Input data 103
4.4.2 Internal data 104
4.4.3 Output data 104
4.5 Register Description 105
4.5.1 Register Memory Map 106
4.5.2 VIC Registers 106
4.5.3 DMA registers 133
4.6 Operation Flow 140
4.6.1 Overview 140
4.6.2 Configure VIC 141
4.7 Index 143
IMAGE CORE 144
5 Felix 145
5.1 Overview 145
5.1.1 Block Diagram 145
5.1.2 Features of FELIX 145
5.1.3 Data Format 146
5.1.4 Internal physical address base definition 148

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

5.2 VDMA 148
5.2.1 Overview 148
5.2.2 Task trigger (TRIG) 150
5.2.3 VDMA status (STAT) 150
5.3 Global 151
5.3.1 Global control 151
5.3.2 Interrupt state 151
5.4 FELIX RESET 152
5.4.1 reset process 152
5.5 Interrupt 152
5.5.1 Interrupt state 152
5.5.2 Interrupt processing 152
5.5.3 Interrupt clear 153
5.6 Operational process 153
6 Helix 154
6.1 Overview 154
6.1.1 Block Diagram 154
6.1.2 Features 154
6.1.3 Data Format 155
6.2 VDMA 155
6.3 Register Definition 156
6.3.1 VDMA status (STAT) 156
6.3.2 LIX Task trigger 156
6.3.3 HELIX Global control 157
6.3.4 HELIX Interrupt state 157
6.3.5 H264 Encode Slice bs len 158
6.3.6 H264 Encode Y SAD 158
6.3.7 H264 Encode C SAD 158
6.3.8 JPGC trigger 159
6.3.9 JPGC Status 159
6.3.10 JPEG Bitstream buffer address 160
6.3.11 JPEG Component 0 plane buffer address 160
6.3.12 JPEG Component 1 plane buffer address 161
6.3.13 JPEG Component 2 plane buffer address 161
6.3.14 JPEG Component 3 plane buffer address 161
6.3.15 JPEG MCU number 162
6.3.16 JPEG Re-Sync-Marker gap number 162
6.3.17 JPEG Component configure information 163
6.3.18 JPEG EFE control 163
6.3.19 JPEG Encode slice geometry information 164
6.3.20 JPEG RAW plane source buffer address 164
6.3.21 JPEG RAW destination buffer basement address 164

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

6.3.22 JPEG RAW plane stride....165
6.4 JPEG Table definition....165
6.4.1 Huffman Base Table....165
6.4.2 Huffman MIN Table....165
6.4.3 Quantization Table....166
6.4.4 Huffman Symbol Table....166
6.5 HELIX RESET....166
6.5.1 Helix reset process....167
6.6 H264 encoder Interrupt....167
6.6.1 Interrupt state....167
6.6.2 Interrupt processing....167
6.6.3 Interrupt clear....167
6.7 H264 encoder Operational process....167
DISPLAY/CAMERA/AUDIO....168
7 Display Controller specification....169
7.1 Features....169
7.1.1 Layer feature....169
7.1.2 Composition feature....169
7.1.3 Display feature....169
7.2 Architecture map....169
7.3 Data Format Description....170
7.3.1 Source data define (the format of source data in DDR memory)....170
7.3.2 SLCD output pin define....170
7.3.3 GPIO Pads relation....171
7.4 Descriptor definition....172
7.5 Registers Description....178
7.5.1 Instructions....178
7.5.2 Map....178
7.5.3 Composer configure....181
7.5.4 Display interfaces configure....202
7.6 Operation guide....213
7.6.1 Composer operation....213
7.6.2 TFT operation....213
7.6.3 SLCD operation....213
7.6.4 Data channel switch....214
7.6.5 Insert new descriptor into current chain....214
7.6.6 Simple Rdma/Composer switch....215
7.6.7 interrupt control....215
7.7 Software Notes....215
8 Rotator....216

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

8.1 Features 216
8.1.1 Frame feature 216
8.1.2 Rotate feature 216
8.2 Architecture map 216
8.3 Descriptor definition 216
8.4 Registers Description 219
8.4.1 Instructions 219
8.4.2 Map 219
8.4.3 Common config registers 220
8.5 Operation guide 226
8.5.1 Composer operation 226
9 MIPI DSI Controller 227
9.1 Overview 227
9.2 Registers 227
9.2.1 Registers Memory Map 228
9.2.2 Registers and Fields Description 230
9.2.3 VERSION 230
9.2.4 PWR_UP 230
9.2.5 CLKMGR_CFG 231
9.2.6 DPI_VCID 231
9.2.7 DPI_COLOR_CODING 232
9.2.8 DPI_CFG_POL 232
9.2.9 DPI_LP_CMD_TIM 233
9.2.10 PCKHDL_CFG 233
9.2.11 GEN_VCID 234
9.2.12 MODE_CFG 234
9.2.13 VID_MODE_CFG 234
9.2.14 VID_PKT_SIZE 236
9.2.15 VID_NUM_CHUNKS 236
9.2.16 VID_NULL_SIZE 236
9.2.17 VID_HSA_TIME 237
9.2.18 VID_HBP_TIME 237
9.2.19 VID_HLINE_TIME 237
9.2.20 VID_HSA_LINES 238
9.2.21 VID_VBP_HLINES 238
9.2.22 VID_VFP_LINES 239
9.2.23 VID_VACTIVE_LINES 239
9.2.24 EDPI_CMD_SIZE 239
9.2.25 CMD_MODE_CFG 240
9.2.26 GEN_HDR 241
9.2.27 GEN_PLD_DATA 242
9.2.28 CMD_PKT_STATUS 242

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.2.29 TO_CNT_CFG 243
9.2.30 HS_RD_TO_CNT 244
9.2.31 LP_RD_TO_CNT 244
9.2.32 HS_WR_TO_CNT 244
9.2.33 LP_WR_TO_CNT 245
9.2.34 BTA_TO_CNT 246
9.2.35 SOF_3D 246
9.2.36 LPCLK_CTRL 247
9.2.37 PHY_TMR_LPCLK_CFG 247
9.2.38 PHY_TMR_CFG 248
9.2.39 PHY_RSTZ 248
9.2.40 PHY_IF_CFG 249
9.2.41 PHY_ULPS_CTRL 249
9.2.42 PHY_TX_TRIGGERS 250
9.2.43 PHY_STATUS 250
9.2.44 PHY_TST_CTRL0 251
9.2.45 PHY_TST_CTRL1 251
9.2.46 INT_ST0 252
9.2.47 INT_ST1 253
9.2.48 INT_MSK0 254
9.2.49 INT_MSK1 255
9.2.50 INT_FORCE0 256
9.2.51 INT_FORCE1 257
9.2.52 VID_SHADOW_CTRL 258
9.2.53 DPI_VCID_ACT 259
9.2.54 Static and Dynamic Registers 259
9.3 MIPI DSI Host Controller Guide 260
9.3.1 Initializing MIPI DSI Host Controller and D-PHY 260
9.3.2 Configuring the DPI Resolution for Transmission 260
9.3.3 Initializing D-PHY 263
9.3.4 Video Mode Pattern Generator 263
9.3.5 ULPM Flow 263
9.3.6 Process Flow to Enter the ULPM 263
9.3.7 Process Flow to Exit the ULPM 264
10 MIPI_CSI Interface 265
10.1 Overview 265
10.1.1 Features 265
10.2 Register Descriptions 265
10.2.1 Register Mapping 265
10.2.2 VERSION 266
10.2.3 N_LANES 267
10.2.4 PHY_SHUTDOWNZ 267

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

10.2.5 DPHY_RSTZ 268
10.2.6 CSI2_RESETN 268
10.2.7 PHY_STATE 269
10.2.8 DATA_IDS_1 269
10.2.9 DATA_IDS_2 270
10.2.10 ERR1 271
10.2.11 ERR2 272
10.2.12 MASK1 273
10.2.13 MASK2 275
10.2.14 PHY_TST_CRTL0 276
10.2.15 PHY_TST_CRTL1 276
10.3 Operation 277

11 Camera Interface Module(CIM) 278

11.1 Overview 278
11.2 Features 278
11.3 Function Description 278
11.3.1 Mode 278
11.4 Data Format Description 279
11.4.1 Input Data(DVP Interface) 279
11.4.2 Output Data(memory) 279
11.4.3 Timing 280
11.4.4 Others 280
11.5 Pins Description 281
11.6 Architecture map 281
11.7 Descriptors define 281
11.8 Registers Description 284
11.8.1 Instructions 284
11.8.2 Map 285
11.8.3 Registers 286
11.9 Operation guide 296
11.9.1 Configure flow 296
11.9.2 Interlace scan mode 297

12 Audio Interface Controller 298

12.1 Overview 298
12.1.1 Features 298
12.1.2 Architecture Map 300
12.2 SubModule 301
12.2.1 DMA 301
12.2.2 Format Converter 310
12.2.3 Internal CBUS 312
12.2.4 nternal DBUS 314

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.5 BAIC 326
12.2.6 DMIC 347
12.2.7 SPDIF OUT 360
12.2.8 SPDIF IN 365
12.2.9 MIXER 372

13 Internal CODEC 374

13.1 DESCRIPTOR 374
13.2 BLOCK DIAGRAM 374
13.3 Electrical Characteristics 374
13.4 I2S MASTER AND SLAVER OPERATION 375
13.5 Register descriptor 377
13.5.1 Reset register(0x00) 377
13.5.2 ADC-DAC Configure1 Register(0x02) 377
13.5.3 ADC-DAC Configure2 Register(0x03) 378
13.5.4 ADC-DAC Configure3 Register(0x04) 378
13.5.5 ADC-DAC Configure4 Register(0x05) 379
13.5.6 Choose ALC Gain register(0x0a) 380
13.5.7 Select Pre-charge / Dis-charge Register(0x21) 380
13.5.8 Control1 Register(0x22) 381
13.5.9 Control2 Register(0x23) 381
13.5.10 Control3 Register(0x24) 382
13.5.11 Control4 Register(0x25) 382
13.5.12 Control5 Register(0x26) 383
13.5.13 Control6 Register(0x27) 384
13.5.14 Control7 Register(0x28) 384
13.5.15 ALG CONFIG1(0x44) 385
13.5.16 ALG MAXL(0x45) 385
13.5.17 ALGMAXH(0x46) 386
13.5.18 ALG MINL(0x47) 386
13.5.19 ALG MINH(0x48) 386
13.5.20 ALG CONFIG2(0x49) 386
13.6 FREQUENCY AMPLITUDE RESPONSE 387
13.7 PCB LAYOUT GUIDE 388
13.8 APPLICATION REFERENCE 389
13.8.1 POWER UP 389
13.8.2 POWER OFF 389
13.8.3 ENABLE ADC 389
13.8.4 DISABLE ADC 390
13.8.5 ENABLE DAC 390
13.8.6 DISABLE DAC 391
13.8.7 ENABLE ALC 391
13.8.8 DISABLE ALC 392

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

MEMORY INTERFACE 393

14 DDR Controller 394

14.1 Overview 394
14.1.1 Block Diagram 394
14.2 DDR Controller Register Description 395
14.2.1 DSTS 398
14.2.2 DCFG 398
14.2.3 DCTRL 400
14.2.4 DLMR 402
14.2.5 DDLP 404
14.2.6 DASR_EN 405
14.2.7 DASR_CNT 405
14.2.8 DREFCNT 406
14.2.9 DTIMING1 407
14.2.10 DTIMING2 408
14.2.11 DTIMING3 408
14.2.12 DTIMING4 409
14.2.13 DTIMING5 409
14.2.14 DMMAP0/1 410
14.2.15 DBWCFG 411
14.2.16 DBWSTP 411
14.2.17 DBWP0W/R 412
14.2.18 DBWP1W/R 413
14.2.19 DBWP2W/R 413
14.2.20 DBWP3W/R 414
14.2.21 HREGPRO 414
14.2.22 DBGEN 415
14.2.23 DBGINFO 416
14.2.24 DWCFG 416
14.2.25 DWSTATUS 417
14.2.26 DREMAP1/2/3/4/5 418
14.2.27 CPAC 419
14.2.28 CCHC0/1/2/3/4/5/6/7 420
14.2.29 CSCHC0 421
14.2.30 CSCHC1 422
14.2.31 CSCHC2 422
14.2.32 CSCHC3 423
14.2.33 CMONC0 424
14.2.34 CMONC1 424
14.2.35 CMONC2 425
14.2.36 CMONC3 425

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.2.37 CMONC4 426
14.2.38 CCGUC0 426
14.2.39 CCGUC1 427
14.2.40 PREGPRO 429
14.2.41 BUFCFG 429
14.3 DDR PHY Register Description 430
14.3.1 DDR PHY RST 431
14.3.2 DDR PHY MEM_CFG 431
14.3.3 DDR PHY TRAINING_CTRL 432
14.3.4 DDR PHY WL_MODE1 432
14.3.5 DDR PHY WL_MODE2 433
14.3.6 DDR PHY CL 433
14.3.7 DDR PHY AL 433
14.3.8 DDR PHY CWL 434
14.3.9 DDR CMD NRCOMP 434
14.3.10 DDR CMD PRCOMP 434
14.3.11 DDR CK/CKB NRCOMP 435
14.3.12 DDR CK/CKB PRCOMP 435
14.3.13 DDR Weak Pull Up/Down 435
14.3.14 DDR CMD DLL 436
14.3.15 DDR CK DLL 436
14.3.16 DDR DFI LP Response Timing 437
14.3.17 DDR DQ Width 437
14.3.18 DDR PLL Feedbackdive 437
14.3.19 DDR PLL PowerDown Enable 438
14.3.20 DDR PLL Post Divide 438
14.3.21 DDR Write Leveling Complete 439
14.3.22 DDR PHY PLL_LOCK 439
14.3.23 DDR PHY CALIB_DONE 439
14.3.24 DDR PHY INIT_COMP 440
14.3.25 DDR PHY Bist 440
14.4 Power-up and Initialize Sequence 441
14.4.1 Main initialize flow 441
14.4.2 RESET flow 442
15 External Memory Controller 444
15.1 Overview 444
15.2 Pin Description 444
15.3 Physical Address Space Map 445
15.4 Static Memory Interface 447
15.4.1 Register Description 447
15.4.2 Example of Connection 452
15.4.3 Basic Interface 452

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

15.4.4 Burst ROM Interface 456

16 SPI Flash Controller(SFC) 457

16.1 Overview 457
16.2 Features 457
16.3 Block Diagram 458
16.4 Functional Description 458
16.4.1 Bus function 458
16.4.2 Configurable Timing parameter 459
16.5 Pin Description 459
16.6 Data Format Description 460
16.6.1 1Transfer format 460
16.6.2 Endian Description 465
16.7 Registers Description 465
16.7.1 Instructions 465
16.7.2 Map 466
16.7.3 Registers 467
16.8 Software Guideline 481
16.8.1 CDT Description 481
16.8.2 DMA Descriptor 482
16.8.3 Phase Description 483
16.8.4 Multi phases flow 483
16.8.5 One phase flow 484
16.8.6 Meters of DMA operation need attention 484
16.8.7 Meters of slave mode operation need attention 484
16.8.8 Example (NAND flash write with multi phases in DMA mode) 485
16.8.9 Example (NAND flash write with multi phases in DMA descriptor mode) 486
16.8.10 Example (NAND flash write with multi phases in CDT mode) 487
16.8.11 Example (NAND flash write with single phase in REG mode) 487
16.9 Index 488

SYSTEM FUNCTIONS 490

17 Clock Reset and Power Controller 491

17.1 Overview 491
17.1.1 CGU Block Diagram 492
17.1.2 CGU Registers 493
17.1.3 PLL Operation 528
17.1.4 Main Clock Division Change Sequence 529
17.2 Power Manager 530
17.2.1 Low-Power Modes and Function 530
17.2.2 Register Description 531
17.2.3 IDLE Mode 542

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

17.2.4 SLEEP Mode 542
17.3 Reset Control Module 543
17.3.1 Register Description 543
17.3.2 Power On Reset 544
17.3.3 WDT Reset 544
18 Timer/Counter Unit 545
18.1 Overview 545
18.2 Features 545
18.3 Pin Description 545
18.4 Register Description 545
18.4.1 Register Memory Map 546
18.4.2 Register and Fields Description 548
18.5 Operation 592
18.5.1 Operation in TCU1 Mode 592
19 Operating System Timer For Time Slice 597
19.1 Overview 597
19.2 Convention 597
19.3 Registers Mapping 598
19.3.1 Register and Fields Description 598
19.4 Operation 601
19.4.1 Basic Operation 601
19.4.2 Stop Operation 601
19.4.3 Modify The PRE-SCALE 602
20 Operating System Timer For Time Elapsed 603
20.1 overview 603
20.2 Convention 603
20.3 Registers Mapping 604
20.3.1 Register and Fields Description 604
20.4 Operation 607
20.4.1 Basic Operation 607
20.4.2 Stop Operation 607
20.4.3 Modify The PRE-SCALE 607
21 Interrupt Controller 608
21.1 Overview 608
21.2 Register Description 608
21.2.1 Interrupt Controller Source Register (ICSR0) 609
21.2.2 Interrupt Controller Source Register (ICSR1) 610
21.2.3 Interrupt Controller Mask Register (ICMR0) 610
21.2.4 Interrupt Controller Mask Register (ICMR1) 611

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

21.2.5 Interrupt Controller Mask Set Register (ICMSR0) 611
21.2.6 Interrupt Controller Mask Set Register (ICMSR1) 611
21.2.7 Interrupt Controller Mask Clear Register (ICMCR0) 612
21.2.8 Interrupt Controller Mask Clear Register (ICMCR1) 612
21.2.9 Interrupt Controller Pending Register (ICPR0) 612
21.2.10 Interrupt Controller Pending Register (ICPR1) 613
21.2.11 Interrupt Source Register0 for PDMA (DSR0) 613
21.2.12 Interrupt Mask Register0 for PDMA (DMR0) 614
21.2.13 Interrupt Pending Register0 for PDMA (DPR0) 614
21.2.14 Interrupt Source Register1 to PDMA (DSR1) 614
21.2.15 Interrupt Mask Register1 for PDMA (DMR1) 615
21.2.16 Interrupt Pending Register1 for PDMA (DPR1) 615
21.3 Software Considerations 616

22 Watchdog Timer 617

22.1 Overview 617
22.2 Features 617
22.3 Register Description 617
22.3.1 Register Memory Map 618
22.3.2 Register and Fields Description 618
22.3.3 Watchdog Timer Data Register (WDT_FULL,0x00) 618
22.3.4 Watchdog Enable Register (WDT_ENABLE,0x04) 618
22.3.5 Watchdog Timer Counter (WDT_COUNT,0x08) 619
22.3.6 Watchdog Control Register(WDT_CONTROL,0x0C) 619
22.4 Watchdog Timer Function 620

23 PDMA Controller 621

23.1 Overview 621
23.2 Features 621
23.3 Block Diagram 621
23.4 Memory Mapped Register Descriptions 622
23.4.1 DMA Channel Registers 622
23.4.2 Global Control Registers 623
23.5 DMA Channel Register Definition 623
23.5.1 DMA Source Address (DSAn, n = 0 ~ 31) 623
23.5.2 DMA Target Address (DTAn, n = 0 ~ 31) 624
23.5.3 DMA Transfer Count (DTCn, n = 0 ~ 31) 624
23.5.4 DMA Request Types (DRTn, n = 0 ~ 31) 624
23.5.5 DMA Channel Control/Status (DCSn, n = 0 ~ 31) 626
23.5.6 DMA Channel Command (DCMn, n = 0 ~ 31) 627
23.5.7 DMA Descriptor Address (DDAn, n = 0 ~ 31) 631
23.5.8 DMA Stride Difference (DSDn, n = 0 ~ 31) 632
23.6 DMA Global Register Definition 632

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

23.6.1 DMA Control....632
23.6.2 DMA Interrupt Pending (DIRQP)....633
23.6.3 DMA Doorbell (DDB)....634
23.6.4 DMA Doorbell Set (DDS)....634
23.6.5 Descriptor Interrupt Pending (DIP)....634
23.6.6 Descriptor Interrupt Clear (DIC)....635
23.6.7 DMA Channel Programmable (DMACP)....635
23.6.8 DMA Soft IRQ Pending (DSIRQP)....635
23.6.9 DMA Soft IRQ Mask (DSIRQM)....636
23.6.10 DMA Channel IRQ Pending to MCU (DCIRQP)....636
23.6.11 DMA Channel IRQ to MCU Mask (DCIRQM)....637
23.6.12 Programmable Channel Bound With INTC_IRQ....637
23.6.13 Special Channel 0 and Channel 1....637
23.7 MCU....638
23.7.1 MCU Control & Status....638
23.7.2 MCU Normal MailBox....639
23.7.3 MCU Security MailBox....639
23.7.4 MCU Interrupt....639
23.7.5 Multiple Bank Tightly Coupled Sharing Memory....640
23.7.6 CP0 Registers of MCU....640
23.7.7 Normal Exceptions Accepted by MCU....641
23.7.8 How to Boot MCU Up....641
23.7.9 Security features....642
23.8 DMA manipulation....642
23.8.1 Descriptor Transfer Mode....642
23.8.2 No-Descriptor Transfer Mode....645
23.8.3 Descriptor Transfer Interrupt/Stop control....645
23.9 DMA Requests....647
23.9.1 Auto Request....647
23.9.2 On-Chip Peripheral Request....647
23.10 How to Use Programmable DMA Channel....647
24 SAR A/D Controller....648
24.1 Overview....648
24.2 Features....648
24.3 Block Diagram....648
24.4 Pins Description....649
24.5 Register Description....649
24.5.1 Register Memory Map....649
24.5.2 Register and Fields Description....650
24.6 SAR A/D Controller Guide....655
24.6.1 Power Down Mode....656
24.6.2 AUX Sample Operation....656

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

25 Real Time Clock 657
25.1 Overview 657
25.2 Features 657
25.3 Block Diagram 657
25.4 Pins Description 658
25.5 Registers Description 658
25.5.1 RTC Control Register (RTCCR) 660
25.5.2 RTC Second Register (RTCSR) 661
25.5.3 RTC Second Alarm Register (RTCSAR) 662
25.5.4 RTC Regulator Register (RTCGR) 662
25.5.5 Hibernate Control Register (HCR) 663
25.5.6 HIBERNATE mode Wakeup Filter Counter Register (HWFCR) 664
25.5.7 Hibernate Reset Counter Register (HRCR) 664
25.5.8 HIBERNATE Wakeup Control Register (HWCR) 665
25.5.9 HIBERNATE Wakeup Status Register (HWRSR) 665
25.5.10 Hibernate Scratch Pattern Register (HSPR) 666
25.5.11 Write Enable Pattern Register (WENR) 667
25.5.12 WKUP_PIN_RST control register (WKUPPINCR) 668
25.6 Operation Flow 668
25.6.1 Registers Access 668
25.6.2 Registers Read 668
25.6.3 Registers Write 669
25.6.4 Normal Mode 669
25.6.5 Power Detect 669
25.6.6 Power On Timing Diagram 669
25.6.7 HIBERNATE Mode 669
25.6.8 Procedure to Enter HIBERNATE mode 670
25.6.9 Procedure to Wake-up from HIBERNATE mode 670
25.6.10 Time Regulation 670
25.6.11 Clock select 671
26 EFUSE Slave Interface (EFUSE) 673
26.1 Overview 673
26.2 Registers 673
26.2.1 Registers Memory Map 674
26.2.2 Registers and Fields Description 674
26.3 Operation Mode 679
26.4 Flow 680
26.4.1 Program EFUSE Flow 680
26.4.2 Program Security Key Flow 680
26.4.3 Read EFUSE Flow 681
26.4.4 Read Security Key Flow 681

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

PERIPHERALS.....682

27 General-Purpose I/O Ports.....683

27.1 Overview.....683
27.2 Features.....683
27.3 About GPIO Port Summary Table.....683
27.3.1 GPIO Port A Summary.....686
27.3.2 GPIO Port B Summary.....687
27.3.3 GPIO Port C Summary.....688
27.3.4 GPIO Port D Summary.....689
27.3.5 GPIO Port E Summary.....690
27.3.6 GPIO Port Z - Shadow Group.....692
27.4 Registers Description.....692
27.4.1 Register Memory Map.....692
27.4.2 Register and Fields Description.....698
27.4.3 PORT PIN Level Registers (PxPINL,0x0000).....698
27.4.4 PORT Interrupt Registers (PxINT,0x0010).....699
27.4.5 PORT Interrupt Set Registers (PxINTS,0x0014).....699
27.4.6 PORT Interrupt Clear Registers (PxINTC,0x0018).....699
27.4.7 PORT Mask Registers (PxMSK,0x0020).....700
27.4.8 PORT Mask Set Registers (PxMSKS,0x0024).....700
27.4.9 PORT Mask Clear Registers (PxMSKC,0x0028).....701
27.4.10 PORT PAT1/Direction Registers (PxPAT1,0x0030).....701
27.4.11 PORT PAT1/Direction Set Registers (PxPAT1S,0x0034).....702
27.4.12 PORT PAT1/Direction Clear Registers (PxPAT1C,0x0038).....702
27.4.13 PORT PAT0/Data Registers (PxPAT0,0x0040).....703
27.4.14 PORT PAT0/Data Set Registers (PxPAT0S,0x0044).....703
27.4.15 PORT PAT0/Data Clear Registers (PxPAT0C,0x0048).....704
27.4.16 PORT FLAG Registers (PxFLG,0x0050).....704
27.4.17 PORT FLAG Clear Registers (PxFLGC,0x0058).....705
27.4.18 PORT Dual-Edge Interrupt Register (PxEDG,0x70).....705
27.4.19 PORT Dual-Edge Interrupt Set Register (PxEDGS,0x74).....706
27.4.20 PORT Dual-Edge Interrupt Clear Register (PxEDGC,0x78).....706
27.4.21 PORT PULL-UP State Register (PxPU,0x80).....706
27.4.22 PORT PULL-UP State Set Register (PxPUS,0x84).....708
27.4.23 PORT PULL-UP State Clear Register (PxPUC,0x88).....709
27.4.24 PORT PULL-DOWN State Register (PxPD,0x90).....709
27.4.25 PORT PULL-DOWN State Set Register (PxPDS,0x94).....711
27.4.26 PORT PULL-DOWN State Clear Register (PxPDC,0x98).....711
27.4.27 PORT Drive Strength State Register0 (PxDS0,0xA0).....711
27.4.28 PORT Drive Strength State Set Register0 (PxDS0S,0xA4).....712
27.4.29 PORT Drive Strength State Clear Register0 (PxDS0C,0xA8).....712

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.4.30 PORT Drive Strength State Register1 (PxDS1,0xB0) 713
27.4.31 PORT Drive Strength State Set Register1 (PxDS1S,0xB4) 713
27.4.32 PORT Drive Strength State Clear Register1 (PxDS1C,0xB8) 713
27.4.33 PORT Drive Strength State Register2 (PxDS2,0xC0) 714
27.4.34 PORT Drive Strength State Set Register2 (PxDS2S,0xC4) 714
27.4.35 PORT Drive Strength State Clear Register2 (PxDS2C,0xC8) 715
27.4.36 PORT Slew Rate Register (PxSR,0xD0) 715
27.4.37 PORT Slew Rate Set Register (PxSRS,0xD4) 715
27.4.38 PORT Slew Rate Clear Register (PxSRC,0xD8) 716
27.4.39 PORT Schmitt Trigger Register (PxSMT,0xE0) 716
27.4.40 PORT Schmitt Trigger Set Register (PxSMTS,0xE4) 716
27.4.41 PORT Schmitt Trigger Clear Register (PxSMTC,0xE8) 717
27.4.42 PORT Z Shadow Register Group 717
27.4.43 GPIOZ Group ID to Load Register (PzGID2LD,0x00F0) 719
27.5 Program Guide 720
27.5.1 Port Function Guide 720
27.5.2 Configure without 3rd-unexpected state 720
27.5.3 Dual-edge Interrupt Configure Guide 721
28 SMB Controller 722
28.1 Overview 722
28.1.1 Features 722
28.1.2 Pin Description 722
28.2 Registers 723
28.2.1 Registers Memory Map 723
28.2.2 Registers and Fields Description 724
28.2.3 SMB_CON (SMB Control Register) 724
28.2.4 SMB_TAR (SMB Target Address Register) 725
28.2.5 SMB_SAR (SMB Slave Address Register) 727
28.2.6 SMB_HS_MADDR (SMB High Speed Master Mode Code Address Register) 727
28.2.7 SMB_DC (SMB Rx/Tx Data Buffer and Command Register) 728
28.2.8 SMB_SHCNT (SMB Standard Speed SCL High Count Register) 729
28.2.9 SMB_SLCNT (SMB Standard Speed SCL Low Count Register) 730
28.2.10 SMB_FHCNT (SMB Fast Speed SCL High Count Register) 730
28.2.11 SMB_FLCNT (SMB Fast Speed SCL Low Count Register) 731
28.2.12 SMB_HHCNT (SMB High Speed SCL High Count Register) 731
28.2.13 SMB_HLCNT (SMB High Speed SCL Low Count Register) 732
28.2.14 SMB_INTST (SMB Interrupt Status Register) 732
28.2.15 SMB_INTM (SMB Interrupt Mask Register) 734
28.2.16 SMB_RAW_INTR_STAT 735
28.2.17 SMB_RXTL (SMB Receive FIFO Threshold Register) 737
28.2.18 SMB_TXTL (SMB Transmit FIFO Threshold Register) 737
28.2.19 SMB_CINT (SMB Clear Combined and Individual Interrupt Register) 737

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

28.2.20 SMB_CRXUF (SMB Clear RXUF Interrupt Register) 738
28.2.21 SMB_CRXOF (SMB Clear RXOF Interrupt Register) 738
28.2.22 SMB_CTXOF (SMB Clear TX_OVER Interrupt Register) 739
28.2.23 SMB_CRXREQ (SMB Clear RDREQ Interrupt Register) 739
28.2.24 SMB_CTXABT (SMB Clear TX_ABRT Interrupt Register) 739
28.2.25 SMB_CRXDN (SMB Clear RX_DONE Interrupt Register) 740
28.2.26 SMB_CACT (SMB Clear ACTIVITY Interrupt Register) 740
28.2.27 SMB_CSTP (SMB Clear STOP Interrupt Register) 741
28.2.28 SMB_CSTT (SMB Clear START Interrupt Register) 741
28.2.29 SMB_CGC (SMB Clear GEN_CALL Interrupt Register) 741
28.2.30 SMB_ENABLE (SMB Enable Register) 742
28.2.31 SMB_ST(SMB Status Register) 742
28.2.32 SMB_TXFLR(SMB Transmit FIFO Level Register) 744
28.2.33 SMB_RXFLR(SMB Receive FIFO Level Register) 744
28.2.34 SMB_SDAHD (SMB SDA Hold Time Register) 744
28.2.35 SMB_ABTSRC (SMB Transmit Abort Source Register) 745
28.2.36 SMB_SLV_DATA_NACK_ONLY (SMB Generate Slave Data NACK Register) 747
28.2.37 SMB_DMACR (SMB DMA Control Register) 748
28.2.38 SMB_DMATDLR (SMB DMA Transmit Data Level Register) 749
28.2.39 SMB_DMARDLR (SMB DMA Transmit Data Level Register) 749
28.2.40 SMB_SDASU (SMB SDA Setup Register) 749
28.2.41 SMB_ACKGC (SMB ACK General Call Register) 750
28.2.42 SMB_ENBST (SMB Enable Status) 751
28.2.43 SMB_FS_SPKLEN (SMB SS and FS Spike Suppression Limit Register) 752
28.2.44 SMB_HS_SPKLEN (SMB HS Spike Suppression Limit Register) 753
28.3 Operating Flow 753
28.3.1 SMB Behavior 753
28.3.2 Master Mode Operation 754
28.3.3 Configuration 754
28.3.4 Dynamic SMBTAR or SMB10BITADDR_MASTER Update 755
28.3.5 Master Transmit and Master Receive 755
28.3.6 Slave Mode Operation 756
28.3.7 Initial Configuration 756
28.3.8 Slave-Transmitter Operation for a Single Byte 756
28.3.9 Slave-Receiver Operation for a Single Byte 758
28.3.10 Slave-Transfer Operation For Bulk Transfers 758
28.3.11 Disabling SMB 759
28.3.12 Procedure 759
28.3.13 Summary the condition could flush TX FIFO 759
28.3.14 The condition could generate START, STOP and RESTART 760
29 Smart Card Controller 763
29.1 Overview 763

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

29.2 Pin Description 764
29.3 Register Description 764
29.3.1 Transmit/Receive FIFO Data Register (SCCDR) 765
29.3.2 FIFO Data Count Register (SCCFDR) 765
29.3.3 Control Register (SCCCR) 765
29.3.4 Status Register (SCCSR) 767
29.3.5 Transmission Factor Register (SCCTFR) 767
29.3.6 Extra Guard Timer Register (SCCEGTR) 768
29.3.7 ETU Counter Value Register (SCCECR) 768
29.3.8 Reception Timeout Register (SCCRTOR) 768
30 Synchronous Serial Interface(SSI) 769
30.1 Overview 769
30.2 Features: 769
30.3 Block Diagram 770
30.4 Functional Description 770
30.5 Pin Description 771
30.6 Data Formats 771
30.6.1 Motorola's SPI Format Details 772
30.6.2 TI's SSP Format Details 775
30.6.3 National Microwire Format Details 776
30.7 Register Description 778
30.7.1 Register Mapping 778
30.7.2 SSI Data Register (SSIDR) 779
30.7.3 SSI Control Register0 (SSICR0) 780
30.7.4 SSI Control Register1 (SSICR1) 782
30.7.5 SSI Status Register (SSISR) 784
30.7.6 SSI Interval Time Control Register (SSIITR) 785
30.7.7 SSI Interval Character-per-frame Control Register (SSIICR) 786
30.7.8 SSI Clock Generator Register (SSIGR) 787
30.7.9 SSI Receive Counter Register (SSIRCNT) 787
30.8 Software Guideline 788
30.8.1 Common flow 788
30.8.2 Interrupt Operation 788
30.9 Index 788
31 UART Interface 790
31.1 Overview 790
31.1.1 Features 790
31.1.2 Pin Description 790
31.2 Register Descriptions 791
31.2.1 Register Mapping 791
31.2.2 UART Receive Buffer Register (URBR) 792

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

31.2.3 UART Transmit Hold Register (UTHR) 792
31.2.4 UART Divisor Latch Low/High Register (UDLLR / UDLHR) 792
31.2.5 UART Interrupt Enable Register (UIER) 793
31.2.6 UART Interrupt Identification Register (UIIR) 794
31.2.7 UART FIFO Control Register (UFCR) 795
31.2.8 UART Line Control Register (ULCR) 796
31.2.9 UART Line Status Register (ULSR) 797
31.2.10 UART Modem Control Register (UMCR) 799
31.2.11 UART Modem Status Register (UMSR) 800
31.2.12 UART Scratchpad Register 801
31.2.13 Infrared Selection Register (ISR) 801
31.2.14 UART M Register (UMR) 802
31.2.15 UART Add Cycle Register (UACR) 802
31.2.16 UART RXFIFO Counter Register (URCR) 803
31.2.17 UART TXFIFO Counter Register (UTCR) 803
31.2.18 UART Separate RX/TX DMA Register (URTDCR) 803
31.3 Operation 804
31.3.1 UART Configuration 804
31.3.2 Data Transmission 804
31.3.3 Data Reception 804
31.3.4 Receive Error Handling 805
31.3.5 Modem Transfer 805
31.3.6 DMA Transfer 805
31.3.7 Slow IrDA Asynchronous Interface 806
31.3.8 For any frequency clock to use the UART 806

32 eMMC/SD Controller（MSC） 809

32.1 Overview 809
32.2 Features 809
32.3 Block Diagram 810
32.4 Data Format Description 810
32.5 Register Description 811
32.5.1 Register Memory Map 814
32.5.2 Register and Fields Description 817
32.6 Data Flow 886
32.6.1 ADMA2 Operation 888
32.6.2 ADMA3 Operation 889
32.6.3 Command Queueing Task Descriptor 892
32.6.4 eMMC Data Structures 893
32.7 SDIO Read Wait 897
32.8 SDIO Card Interrupt 897
32.9 Operation Flow 898
32.9.1 Overview 898

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.9.2 Host Controller Setup Sequence 899
32.9.3 Clock Control 901
32.9.4 Card Interface Setup Sequence 902
32.9.5 Timeout Setting 903
32.9.6 Abort Transaction 903
32.9.7 SD/SDIO Transaction Mode 906
32.9.8 eMMC Transaction Mode 919
32.9.9 Error Recovery 923

33 ON-THE-GO Controller(OTG) 927

33.1 Overview 927
33.2 Features 927
33.3 Functional Description 927
33.4 Pins Description 927
33.5 Data Format Description 927
33.6 Register Description 928
33.6.1 Register Memory Map 928
33.6.2 Register and Fields Description 930

34 Gigabit Ethernet Media Access Controller (GMAC) 1015

34.1 Overview 1015
34.2 Features 1015
34.3 Block Diagram 1016
34.4 Functional Description 1016
34.5 Pins Description 1016
34.6 Data Format Description 1017
34.7 Register Description 1017
34.7.1 Register Memory Map 1018
34.7.2 Register and Fields Description 1019
34.8 Operation Flow 1073

35 AES 1074

35.1 Overview 1074
35.2 AES engine 1074
35.3 Registers 1076
35.3.1 Register Memory Map 1076
35.3.2 AES Control Register (ASCR) 1077
35.3.3 AES Status Register (ASSR) 1078
35.3.4 AES Interrupt Mask Register (ASINTM) 1078
35.3.5 AES DMA Source Address (ASSA) 1079
35.3.6 AES DMA Destination Address (ASDA) 1079
35.3.7 AES Transfer Count (ASTC) 1079
35.3.8 AES Data Input Register (ASDI) 1080

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

35.3.9 AES Data Output Register (ASDO) 1080
35.3.10 AES KEY FIFO (ASKY) 1081
35.3.11 AES IV FIFO (ASIV) 1081
35.4 Software User Guide 1082
36 SC_RSA 1084
36.1 Overview 1084
36.2 Feature 1084
36.3 Registers 1084
36.3.1 Register Memory Map 1085
36.3.2 RSA Ctrl Register (RSAC) 1085
36.3.3 RSA E-key Register (RSAE) 1086
36.3.4 RSA N-key Register (RSAN) 1086
36.3.5 RSA M-message Register (RSAM) 1087
36.3.6 RSA P-output Register (RSAP) 1087
36.4 Software User Guide 1088
37 SC_HASH HDL 1089
37.1 Overview 1089
37.2 Feature 1089
37.3 Registers 1089
37.3.1 Register Memory Map 1090
37.3.2 Hash Ctrl Register (HSCR) 1090
37.3.3 Hash Status Register (HSSR) 1091
37.3.4 Hash Interrupt Mask Register (HSINTM) 1092
37.3.5 Hash DMA Source Address (HSSA) 1092
37.3.6 Hash Transfer Count (HSTC) 1093
37.3.7 Hash Data Input Register (HSDI) 1093
37.3.8 Hash Data Output Register (HSDO) 1093
37.4 Software User Guide 1094
37.4.1 HASH running flow: 1094
37.4.2 Example of MD5 1095
37.4.3 Example of SHA1 1096
37.4.4 Test Vectors 1096
37.5 AHB Interface 1096
37.5.1 AHB Slave Interface 1096
37.5.2 AHB Master Interface 1097
38 Pulse Modulator Module 1100
38.1 overview 1100
38.2 Features 1100
38.3 Block Diagram 1100
38.4 register description 1101

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

38.4.1 PWM Counter Clock Configure Register (PWMCFG0,1) 1102
38.4.2 PWM Counter Enable Register (PWMEN, PWMENS, PWMENC) 1103
38.4.3 PWM Update Register (PWMUPDATE) 1104
38.4.4 PWM Update Process Busy Status Register (PWMBUSYR) 1105
38.4.5 PWM LEVEL Register (PWMLVL) 1105
38.4.6 PWM Waveform Configuration(PWMWCFGn) 1105
38.4.7 PWM DMA Enable Register (PWMDE, PWMDES, PWMDEC) 1106
38.4.8 PWM DMA Control Register0(PWMDCR0) 1107
38.4.9 WM DMA Control Register1(PWMDCR1) 1108
38.4.10 PWM DMA Transfer Trigger Register(PWMDTRIG) 1108
38.4.11 PWM DMA Fifo Empty Status Register(PWMDFER) 1109
38.4.12 PWM DMA FSM Register(PWMDFSM) 1109
38.4.13 PWM DMA Status Register(PWMDSR) 1109
38.4.14 PWM DMA Status Clear Register(PWMDSCR) 1110
38.4.15 PWM DMA INTERRUPT Control Register(PWMDINTC) 1110
38.4.16 PWM n DMA Memory Address Register (PWMnDMADDR) 1110
38.4.17 PWM n DMA Transfer Length Register (PWMnDTLR) 1111
38.4.18 PWM n Output Enable Register (PWMOEN) 1111
38.5 Basic Operation 1112
38.5.1 Register update mode 1112
38.5.2 DMA update mode 1113

39 Digital True Random Number Generator（DTRNG） 1115

39.1 Overview 1115
39.2 Features 1115
39.3 Block Diagram 1115
39.4 Register Description 1115
39.4.1 Register Memory Map 1116
39.4.2 Register and Fields Description 1116
39.5 Operation Flow 1119

BOOT 1120

40 XBurst Boot ROM Specification 1121

40.1 Boot Select 1121
40.2 Boot Procedure 1121
40.3 SPL Structure 1123
40.4 SPL Paramaters 1123
40.5 MSC Boot Specification 1126
40.6 SFC boot Specification 1127
40.7 USB Boot Specification 1129

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

TABLES

Table 2-1 the conditions of operating mode 12
Table 3-1 MScaler Main Function Points 14
Table 3-2 Registers Memory Map Base Address 19
Table 3-3 MScaler Registers Map 19
Table 3-4 Description of Proprietary Vocabulary 99
Table 4-1 DMA Registers Map 133
Table 4-2 Description of Proprietary Vocabulary 143
Table 5-1 FELIX Features 145
Table 5-2 FELIX Internal physical address base definition 148
Table 7-1 DC Registers Map 179
Table 8-1 DC Registers Map 219
Table 9-1 Registers Memory Map-Address Base 228
Table 9-2 MIPI DSI Register Description 228
Table 10-1 MIPI_CSI Registers Description 266
Table 11-1 DC Registers Map 285
Table 12-1 DMIC Controller Registers Description 347
Table 13-1 Supported Data Formats in Different Modes 375
Table 14-1 DDRC Register 395
Table 14-2 PHY Registers Address Mapping 430
Table 15-1 EMC Pin Description 444
Table 15-2 Physical Address Space Map 446
Table 15-3 Default Configuration of EMC Chip Select Signals 446
Table 15-4 Static Memory Interface Registers 447
Table 16-1 I/O Pin Description 459
Table 16-2 SFC Registers Map 466
Table 16-3 Terms and Abbreviations 488
Table 17-1 Registers Memory Map-Address Base 493
Table 17-2 CGU Registers Configuration 494
Table 17-3 Power/Reset Management Controller Registers Configuration 531
Table 18-1 PWM Pins Description 545
Table 18-2 Registers Memory Map Base Address 546
Table 18-3 TCU Registers Map 546
Table 19-1 Registers Memory Map-Address Base 598
Table 19-2 Registers Configuration 598
Table 20-1 Registers Memory Map-Address Base 604
Table 20-2 Registers Configuration 604
Table 21-1 Registers Memory Map-Address Base 608
Table 21-2 INTC Register 609
Table 22-1 Registers Memory Map Base Address 618
Table 22-2 WDT Registers Map 618
Table 23-1 Registers Memory Map-Address Base 622

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Table 23-2 DMA Channel Registers (n=0~31) 622
Table 23-3 Registers Memory Map-Address Base 623
Table 23-4 Global Control Registers 623
Table 23-5 Transfer Request Types 625
Table 23-6 Available RDIL 628
Table 23-7 TCSM space 640
Table 23-8 Descriptor Structure 643
Table 24-1 SADC Analog Pin 649
Table 24-2 Registers Memory Map Base Address 649
Table 24-3 SADC Registers Map 650
Table 25-1 Registers Memory Map-Address Base 659
Table 25-2 Registers for real time clock 659
Table 25-3 Registers for hibernating mode 659
Table 25-4 Clock select registers 671
Table 26-1 Registers Memory Map-Address Base 674
Table 26-2 EFUSE Register Description 674
Table 27-1 GPIO port summary table illustration 683
Table 27-2 GPIO Port A summary 686
Table 27-3 GPIO Port B summary 687
Table 27-4 GPIO Port C summary 688
Table 27-5 GPIO Port D summary 689
Table 27-6 GPIO Port E summary 690
Table 27-7 Registers Memory Map Base Address 692
Table 27-8 GPIO Registers Group Map 693
Table 28-1 SMB Pin Description 722
Table 28-2 Registers Memory Map-Address Base 723
Table 28-3 Registers Memory Map-Address Offset 723
Table 29-1 Smart Card Controller Pins Description 764
Table 29-2 Smart Card Controller Registers Description 764
Table 30-1 SSI Controller Pins Description 771
Table 30-2 SSI Serial Port Registers 779
Table 30-3 SSI Interrupts 788
Table 31-1 UART Pins Description 790
Table 31-2 UART Registers Description 791
Table 31-3 UART Interrupt Identification Register Description 795
Table 32-1 Card Interfaces Supported for Different Register Types 812
Table 32-2 Registers Memory Map Base Address 814
Table 32-3 MSC Registers Map 814
Table 32-4 Task Descriptor Structure; Lower 64 bits (Data Transfer tasks) 893
Table 32-5 Task Descriptor Fields 894
Table 32-6 Transfer Descriptor Structure (32-Bit Addressing) 895
Table 32-7 Transfer Descriptor Fields 895
Table 32-8 Task Descriptor Structure: Lower 64 bits (for Direct-Command (DCMD) tasks) 896

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Table 32-9 Transfer Descriptor Fields 896
Table 32-10 Card Initialization Sequence for Different Cards 899
Table 32-11 Command Sequence for Different Cards 899
Table 33-1 Registers Memory Map Base Address 928
Table 33-2 On-The-Go（OTG） Registers Map 928
Table 33-3 Minimum Duration for Soft Disconnect 989
Table 34-1 GMAC pin description 1016
Table 34-2 Registers Memory Map Base Address 1018
Table 34-3 GMAC Registers Map 1018
Table 35-1 Registers Memory Map-Address Base 1076
Table 35-2 AES registers description 1076
Table 36-1 Registers Memory Map-Address Base 1085
Table 36-2 RSA registers description 1085
Table 37-1 Registers Memory Map-Address Base 1090
Table 37-2 HASH registers description 1090
Table 38-1 Registers Memory Map-Address Base 1101
Table 38-2 SYS_OST Registers Configuration 1101
Table 39-1 Registers Memory Map Base Address 1116
Table 39-2 DTRNG Registers Map 1116
Table 40-1 Boot Configuration of X2000 1121
Table 40-2 SPL parameters structure 1123
Table 40-3 SPI NOR flash boot flag informations（in spl signature） 1128
Table 40-4 SPI NAND flash boot flag informations（in spl signature） 1128
Table 40-5 Transfer Types Used by the Boot Program 1129
Table 40-6 Vendor Request 0 Setup Command Data Structure 1132
Table 40-7 Vendor Request 1 Setup Command Data Structure 1132
Table 40-8 Vendor Request 2 Setup Command Data Structure 1132
Table 40-9 Vendor Request 3 Setup Command Data Structure 1132
Table 40-10 Vendor Request 4 Setup Command Data Structure 1133
Table 40-11 Vendor Request 5 Setup Command Data Structure 1133

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

FIGURES

Figure 1-1 X2000 Diagram 2
Figure 7-1 Top architecture 169
Figure 7-2 7 layers OSD 214
Figure 12-1 BAIC system structure 327
Figure 12-2 PCM mode A format（8bit，falling edge，sync length one cycle） 343
Figure 12-3 PCM mode B format（8bit，falling edge，sync length one cycle） 343
Figure 12-4 DSP mode A format（8bit，falling edge，sync length one cycle） 343
Figure 12-5 DSP mode B format（8bit，falling edge，sync length one cycle） 344
Figure 12-6 I2S normal format（falling edge） 344
Figure 12-7 I2S LEFT-Justied format（falling edge） 344
Figure 12-8 I2S RIGHT-Justied format（falling edge） 345
Figure 12-9 I2S Mulit-channel-normal- format（8channel,falling edge） 345
Figure 12-10 TDM1- format（8channel,falling edge） 346
Figure 12-11 TDM2- format（8channel,falling edge） 346
Figure 13-1 Codec Overview 374
Figure 13-2 Left Justified Mode 376
Figure 13-3 I2S Mode 376
Figure 14-1 DDR system block diagram 394
Figure 15-1 Physical Address Space Map 445
Figure 15-2 Example of 16-Bit Data Width SRAM Connection 452
Figure 15-3 Example of 8-Bit Data Width SRAM Connection 452
Figure 15-4 Basic Timing of Normal Memory Read 453
Figure 15-5 Basic Timing of Normal Memory Write 454
Figure 15-6 Normal Memory Read Timing With Wait (Software Wait Only) 454
Figure 15-7 Normal Memory Write Timing With Wait (Software Wait Only) 455
Figure 15-8 Normal Memory Read Timing With Wait (Wait Cycle Insertion by WAIT# pin) 455
Figure 15-9 Burst ROM Read Timing (Software Wait Only) 456
Figure 16-1 SFC Block Diagram 458
Figure 16-2 Sample point(no delay) 459
Figure 16-3 Sample point(delay) 459
Figure 16-4 AC timing 459
Figure 16-5 Data Format(Standard SPI) 460
Figure 16-6 Data Format(Dual SPI) 460
Figure 16-7 Data Format(Quad SPI) 461
Figure 16-8 Data Format(Octal@CHIP_SEL=0) 462
Figure 16-9 Data Format(Quad@CHIP_SEL=2) 463
Figure 16-10 Data Format(Dual@CHIP_SEL=2) 464
Figure 16-11 Data Format(Standard SPI@CHIP_SEL=2) 465
Figure 16-12 Multi phases flow 483
Figure 16-13 One phase flow 484
Figure 17-1 Block Diagram of PLL 528

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 23-1 Block Diagram of PDMA 621
Figure 23-2 Descriptor Transfer Flow 644
Figure 23-3 Example for Stride Transfer Mode 645
Figure 24-1 Block Diagram of SADC 648
Figure 25-1 Core Power On 669
Figure 25-2 RTC clock selection path 671
Figure 28-1 Master Transmitter — Tx FIFO Empties/STOP Generation 760
Figure 28-2 Master Receiver — Tx FIFO Empties/STOP Generation 760
Figure 28-3 Master Transmitter — Restart bit of SMB_DC is set 761
Figure 28-4 Master Receiver — Restart bit of SMB_DC is set 761
Figure 28-5 Master Transmitter — Stop Bit of SMB_DC Set/Tx FIFO Not Empty 761
Figure 28-6 Master Transmitter — First Byte Loaded Into Tx FIFO Allowed to Empty, Restart Bit Set 762
Figure 28-7 Master Receiver — Stop Bit of IC_DATA_CMD Set/Tx FIFO Not Empty 762
Figure 28-8 Master Receiver — First Command Loaded After Tx FIFO Allowed to Empty/Restart Bit Set 762
Figure 30-1 SSI Block Diagram 770
Figure 30-2 SPI Single Character Transfer Format (PHA = 0) 772
Figure 30-3 SPI Single Character Transfer Format (PHA = 1) 772
Figure 30-4 SPI Back-to-Back Transfer Format 773
Figure 30-5 SPI Frame Interval Mode Transfer Format (ITFRM = 0, LFST = 0) 774
Figure 30-6 SPI Frame Interval Mode Transfer Format (ITFRM = 1, LFST = 1) 775
Figure 30-7 TI's SSP Single Transfer Format 775
Figure 30-8 TI's SSP Back-to-back Transfer Format 776
Figure 30-9 National Microwire Format 1 Single Transfer 777
Figure 30-10 National Microwire Format 1 Back-to-back Transfer 777
Figure 30-11 National Microwire Format 2 Read Timing 777
Figure 30-12 National Microwire Format 2 Write Timing 778
Figure 32-1 msc data format 811
Figure 32-2 Host Controller Data Flow 887
Figure 32-3 ADMA2 Block Diagram 888
Figure 32-4 ADMA2 Descriptor Table 889
Figure 32-5 ADMA3 Integrated Descriptor Pair(Command Descriptor + ADMA2 Descriptor) 890
Figure 32-6 ADMA3 Command Descriptor Format 891
Figure 32-7 ADMA3 Integrated Descriptor Format 891
Figure 32-8 Command Queuing Host Controller Interface (HCI) Structure 893
Figure 32-9 Host Controller Setup Sequence for SD 900
Figure 32-10 Host Controller Setup Sequence for eMMC Interface 901
Figure 32-11 Host Controller Clock Supply Sequence 902
Figure 32-12 Card Clock Supply and Stop Sequence 902
Figure 32-13 Card Interface Setup Sequence 902
Figure 32-14 SD/eMMC Bus Timeout Setting 903

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 32-15 Abort Command Sequence 904
Figure 32-16 Asynchronous Abort Sequence 905
Figure 32-17 Synchronous Abort Sequence 905
Figure 32-18 SD Card Initialization and Identification 907
Figure 32-19 SD Card Initialization and Identification (contd) 908
Figure 32-20 Change Bus Width Sequence 909
Figure 32-21 Tuning Sequence 910
Figure 32-22 SD Command Issue and Complete 911
Figure 32-23 Transaction Not Using DMA for Data Transfer 912
Figure 32-24 Transaction Control with Data Transfer Using DAT Line (Not Using DMA) 913
Figure 32-25 Transaction Using SDMA for Data Transfer 914
Figure 32-26 Transaction Control with Data Transfer Using DAT Line (Using ADMA2) 915
Figure 32-27 Transaction Control with Data Transfer Using DAT Line (Using ADMA) (Contd) 916
Figure 32-28 Transaction Control with Data Transfer Using DAT Line (Using ADMA3) 917
Figure 32-29 SD Changing Bus Speed Mode 918
Figure 32-30 Card Initialization and Identification Programming Sequence 920
Figure 32-31 Programming Sequence to Switch to Various Speed Modes in an eMMC Device 921
Figure 32-32 Programming Sequence to Change Data Bus Width for an eMMC Device 922
Figure 32-33 Initializing the Command Queuing Engine 922
Figure 32-34 Submitting and Completing a Task 923
Figure 32-35 Error Recovery in SD/eMMC Mode 925
Figure 34-1 GMAC Block Diagram 1016
Figure 34-2 GMAC configure flow 1073
Figure 35-1 ECB mode encoding 1074
Figure 35-2 ECB mode decoding 1075
Figure 35-3 CBC mode encoding 1075
Figure 35-4 CBC mode decoding 1075
Figure 38-1 PWM Block Diagram 1100
Figure 38-2 Register update mode 1112
Figure 38-3 DMA update mode 1113
Figure 39-1 DTRNG Block Diagram 1115
Figure 40-1 Boot sequence diagram of X2000 1122
Figure 40-2 The basic SPL structure 1123
Figure 40-3 SPL configuration change Procedure 1125
Figure 40-4 Typical Procedure of MSC0/MSC1/MSC2 boot 1126
Figure 40-5 SFC Boot Procedure 1127
Figure 40-6 USB Communication Flow 1129
Figure 40-7 Typical Procedure of USB Boot 1131

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Section 1

OVERVIEW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

1 Overview

X2000 is a low power consumption, high performance and high integrated application processor, the application is focus on IoT devices. And it can match the requirements of many other embedded products.

1.1 Block Diagram

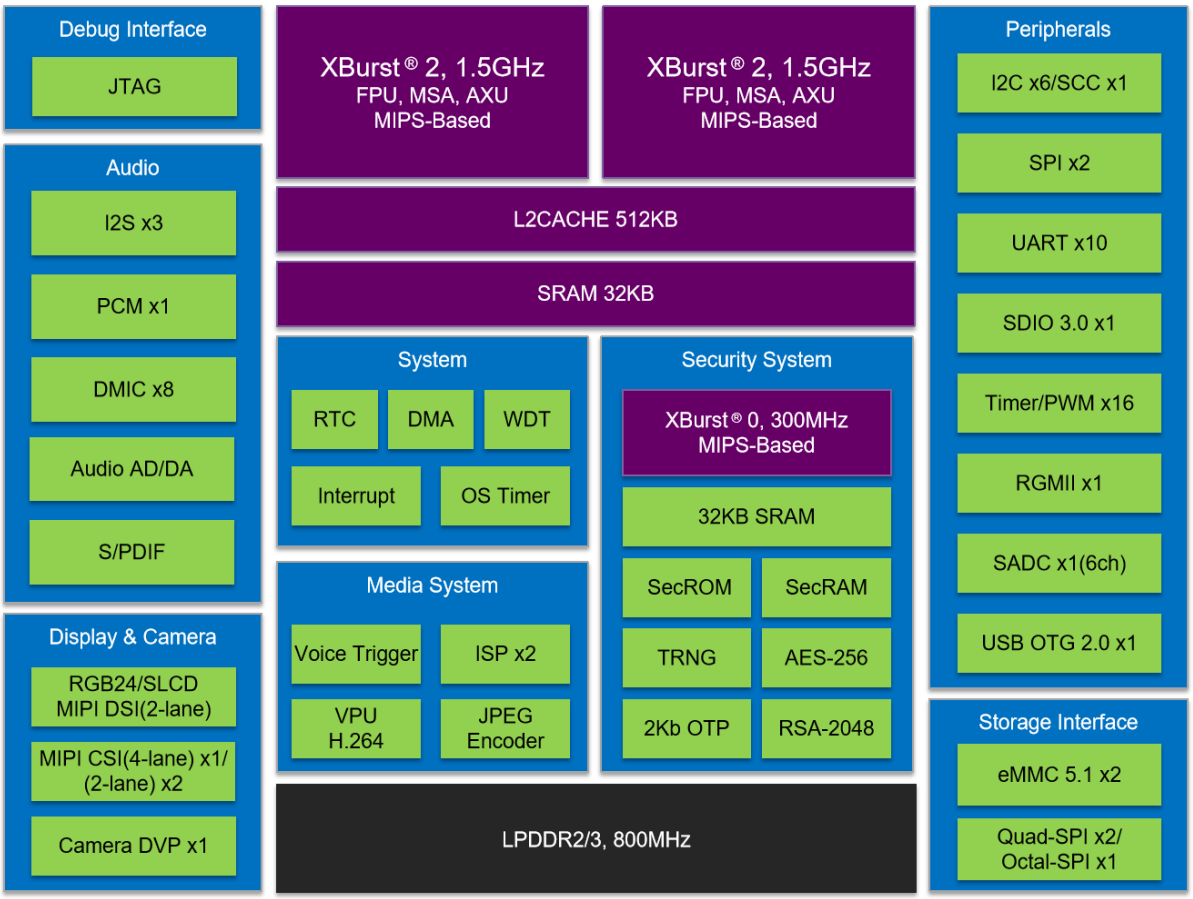


Figure 1-1 X2000 Diagram

1.2 Features

1.2.1 CPU Core

- XBurst® 2, up to 1.5GHz, Dual Core, Dual-issue， MIPS-Based
- 32KB L1，512 KB L2，32KB SRAM
- High-performance Floating-point Unit and 128-bit SIMD Unit
  - 32 x 128-bit register set, 128-bit loads/stores to/from SIMD unit
  - support data types: 8/16/32 bits integer, x16/32/64 bits floating point

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

- IEEE-754 2008 compliant
- Programmable Memory Management Unit (MMU)
  - 1st level mini-TLBs (MTLBs) – 8 x 2 entry instruction TLB, 16 x 2 entry data TLB
  - 2nd level TLBs: 32 × 2 entry VTLB, 256 × 2 entry 4-way set associative FTLB
- The XBurst® processor system supports little endian only

1.2.2 Video Process Unit(VPU)

- H.264 Encoder
  - Input data format NV12/NV21
  - Encoding resolution and frame rate up to 1920x1080@30fps
  - Support hardware RBSP bytes insertion
  - Support auto-read of slice header
  - Support reference frame lossless compression
- H.264 Decoder
  - Output data format NV12/NV21
  - Decoding resolution and frame rate up to 1920x1080@30fps
  - Support hardware RBSP bytes eliminate
- JPEG Codec
  - JPEG compressing/decompressing up to 70Mega-pixels per second
  - Baseline ISO/IEC 10918-1 JPEG compliant
  - 8-bit pixel depth support
  - Up to four programmable Quantization tables
  - Fully programmable Huffman tables

1.2.3 Image Signal Processor(ISPx2)

- Data stream feature
  - DVP： raw8 / 10 / 12 / YUV422 input
  - MIPI： up to 1080P@60fps
  - Support dual-camera sync
  - Frame data check, make up for lost data and drop redundant data
- Advanced feature
  - 2A(Auto Exposure/Auto White Balance) supported
  - Advanced demosaic, color processing, lens shading, sharpen, static/dynamic defect pixel and other modules provide high image quality
  - 2-D noise reduction filter

1.2.4 Memory Interface

- DDR Controller
  - Support LPDDR2, LPDDR3, 16Bit bus width, clock up to 800MHz
  - 128MB/256MB memory in package,
    - X2000: 128MB SIP LPDDR3
    - X2000E: 256MB SIP LPDDR2

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

- SFC Controller
  - 1 group clock and CE pad
  - Two Quad SPI, one Octal SPI (SFC0/1)
  - Support Standard, Dual, Quad SPI and Octal DDR protocol
  - Clock frequency up to 80MHz in SDR mode
  - Support multiple transfer modes, standard SPI, dual-output/dual-Input SPI, Quad-Output/Quad-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI, and Octal-I/O

1.2.5 Audio

- Digital Microphone Array Controller
  - Support 8 channels digital MIC
  - 24/16bit precision internal controller, sample rate support 8K, 16K, 32K, 48K and 96K
  - SNR: 90dB, THD: -90dB @ FS -20dB
  - Linear high pass filter include. Attenuation: -2.9dB@100Hz, -22dB@27Hz. -36dB@10Hz
  - Low power voice trigger when waiting to start talking.
  - Support voice data pre-fetch when trigger enable and the data interface disable, but do not increase the power dissipation.
  - Support low power voice trigger enable
- I2S(1~3) / I2S0
  - DMA transfer mode supported
  - Support share clock mode and split clock mode.
  - I2S0: Internal I2S CODEC supported
  - Support master mode and slave mode
  - Support number of data pin from 1 to 4
  - Support six modes of operation for TDM protocol
- PCM interface
  - Support master mode and slave mode
  - Support four modes of operation for PCM
    - DSP NORMAL \ LEFT MODE
    - PCM NORMAL \ LEFT MOD
- S/PDIF(IN and OUT)
  - Support IEC 60958-3 compliant, up to 2 channels
  - Sample bit support 20-bit and 24-bit two mode
  - Sample rate support, all of IEC60958-3 sample rate(44.1k up to 192k)
- Internal Audio Codec (**DAC and ADC working together**)
  - 24 bits DAC / ADC
  - Sample rate supported: 8k, 12k, 16k, 24k, 32k, 44.1k,48k,96k
  - **Mono Differential input/output**
  - DAC : SNR: 90dB A-Weighted, THD: -80dB @FS，-1dB ; ADC: SNR 90dB

1.2.6 MIPI-CSI

- MIPI-CSI2(v1.0) interface, resolution up to 1080P@120fps

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

– Support dual 2-lane mode and single 4-lane mode
– Support 1-lane, 2-lane and 4-lane mode

1.2.7 Camera

- Camera interface module(CIM)
  - Support DVP 8bit / MIPI input ,resolution up to 1280x720@30fps
  - Support snapshot control
  - Supported data format: RGB888, RGB565, YCbCr 4:2:2
  - Supports ITU656 (YCbCr 4:2:2) input
  - Support histogram output and global binarization

1.2.8 Display

- MIPI-DSI2(v1.0) interface
  Display size up to 1920x1080@40Hz
- SLCD controller
  - Display size up to 640x480@60Hz, 24BPP
  - Supports different size of display panel
- RGB controller
  - Display size up to 1280x720@60Hz, 24BPP
  - Support input format, ARGB8888, ARGB1555, RGB888, RGB565, RGB555, YUV422, YUV420
  - Support 4 modes parallel interface, 24-bit, 18-bit, 16-bit and 8-bit(third times)
  - Support frame buffer crop and dither

1.2.9 System Functions

- Clock generation and power management
  - On-chip oscillator circuit (support 24MHz)
  - Two phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK frequency can be changed separately for software by setting registers
  - Functional-unit clock gating
  - Supply block power shut down
- TCU
  - 8 channels each channel has two pins
  - Support posedge / negedge / dualedge clock counting
  - Support gate counting(only count for gating signal)
  - Support quadrature counting
  - Support direction counting(add / sub because of input signal)
  - Support counting after posedge / negedge signal
  - Support capture counting, output signal high-level time and total cycle time
  - Support exclk / pclk two clock source
- PWM
  - 16 channels, output signal ~50MHz, signal precision ~500MHz

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

- Cpu / dma mode to update config

- OS timer
  - One event timer for one logic core
  - One global timer for system time

- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled

- Watchdog timer
  - A 16-bit Data register and a 16-bit counter
  - Programmable interrupt generation prior to timeout
  - Counter clock uses the input clock selected by software
    - EXTAL / RTCCLK can be used as the clock for counter
    - The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software

- PDMA Controller
  - Support up to 32 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: 1 ~ 2^{24} - 1
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest

- SAR A/D Controller
  - 6 Channels
  - Resolution: 10-bit

- RTC (Real Time Clock)
  - Need external 32768Hz oscillator for 32KHz clock generation.
  - 32-bits second counter
  - Programmable and adjustable counter to generate accurate 1 Hz clock
  - Alarm interrupt, 1Hz interrupt
  - Stand alone power supply, work in hibernating mode
  - Power down controller
  - Alarm wakeup
  - External pin wakeup with up to 2s glitch filter
  - Power Detect to Shut down PMU (find Core without voltage then shut PMU other voltage)

1.2.10 Peripherals

- General-Purpose I/O ports

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

- Input / output / function port configurable
- Low/high, rising/falling edge triggering. Every interrupt source can be masked independent

- Six I2C Controller (I2C0~5)
  - Two-wire I2C serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
  - Three speeds mode
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
    - High speed mode (3.4Mb/s)
  - Programmable SCL generator
  - Master or slave I2C operation
  - 7-bit addressing/10-bit addressing
  - The number of devices that you can connect to the same I2C-bus is limited only by the maximum bus capacitance of 400pF

- One Smart Card Controller (SCC)
  - Supports normal card and UIM card.
  - Supports asynchronous character (T=0) communication modes.
  - Supports asynchronous block (T=1) communication modes.
  - Supports setting of clock-rate conversion factor F (372, 512, 558, etc.), and bit-rate adjustment factor D (1, 2, 4, 8, 16, 32, 12, 20, etc.).
  - Supports extra guard time waiting.
  - Auto-error detection in T=0 receive mode.
  - Auto-character repeat in T=0 transmit mode.
  - Transforms inverted format to regular format and vice versa.
  - Support stop clock function in some power consuming sensitive applications.

- Two Synchronous serial interfaces (SSI0~1)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
  - Configurable normal transfer mode or Interval transfer mode
  - Programmable clock phase and polarity for Motorola's SSI format
  - Two slave select signal (SSI0_CE0_ / SSI1_CE0_) supporting up to 2 slave devices
  - Back-to-back character transmission/reception mode
  - Loop back mode for testing
  - Data transfer up to 30Mbits/s

- Ten UARTs (UART0~9)
  - Full-duplex operation
  - Baud rate supports 4800, 9600, 19200, 38400, 43000, 56000, 57600, 115200, 230400, 460800, 576000, 921600, 1000000, 1152000, 1500000, 2000000, 2500000, 3000000,

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3500000, 4000000, 6000000, 8000000, 12000000
- 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
- Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
- Separate DMA requests for transmit and receive data services in FIFO mode
- Supports modem flow control by software or hardware

- Three MMC/SD/SDIO controllers (MSC0,MSC1,SDIO)
  - All support eMMC 5.1 (command queueing)
  - Support SD Specification 3.0
  - Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
  - Maximum clock speed is 104MHz
  - Both support MMC data width 1bit ,4bit, only MSC0 support 8bit
  - Single or multi block access to the card including erase operation
  - The maximum block length is 4096bytes

- USB 2.0 OTG interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
  - Support operating as USB peripheral, as USB host
  - Support split transmission
  - Support hub
  - Support remote-wakeup

- One GMAC controller
  - 10/100 Mbps and 1000Mbps operation
  - Supports RMII and RGMII PHY interfaces
  - Support IEEE 1588-2002

- Security System
  - XBurst®, 300MHz
  - Secret ROM and RAM
  - Up to 32KB SRAM
  - True Random Number Generator
  - Encryption Engine
    - MD5, SHA, SHA2
    - AES, support 256-bit, 192-bit, 128-bit key size Algorithm
    - RSA, support 1024/2048-bit key size
  - Support secure boot

- OTP Slave Interface

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

- Total 2Kb.

1.2.11 Bootrom

16KB Boot ROM memory and 16KB Security Boot ROM

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Section 2

CORE FUNCTIONS

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

2 CPU

2.1 Overview

XBurst®2 CPU is a high performance and low power implementation of MIPS32 ISA r5 + MSA128 + XBurst® MXA128 instruction set architecture.

2.2 Features of XBurst®2 CPU

- 32-bit MIPS32 ISA R5 plus MIPS SIMD instruction set architecture:MSA128
- Ingenic SIMD instruction set architecture: MXA128
- dual-issue, superscalar, super pipeline with Simultaneous Multi-Threading (SMT)
  - 2 hardware threads per physical core
  - Quad instruction fetch per cycle
  - Dual-issue instruction per cycle
  - Smart branch prediction scheme with Instruction trace buffer (ITB), Branch Target Buffer (BTB), Pattern History Table (PHT), Return Address Stack (RAS) and Jump Target Buffer (RTB)
- L1 cache size for Instruction and Data up to 32KB for each, 8-way set associative
- high-performance dual-issue Floating-point and 128-bit SIMD Unit
  - 32 x 128-bit registers, 128-bit loads/stores to/from SIMD unit
  - data types: 8/16/32 bits integer, Q15/Q31 fixed point and 32/64 bits floating point
  - IEEE-754 2008 compliance
- Programmable Memory Management Unit (MMU)
  - 1st level mini-TLB (MTLB): 8-entry instruction MTLB, 16-entry data MTLB
  - 2nd level joint TLBs: 32-entry VTLB, 256-entry 4-way set associative FTLB
- Integrated Cache Crossbar (CCX) and L2 cache
  - Configurable size up to 1MB
  - Hardware prefetcher for streaming performance
- Advanced power management
  - Hardware automatic clock gating for idle subsystems
- XBurst2 CPU implements SMT technology - a physical core contains 2 simultaneous threads. For convenience of description, a thread can be regarded as a logic core. Therefore, except explicitly claim, a core means a logic core in later chapters.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

2.3 Operating Modes

XBurst®2 CPU core supports three operating modes:

- Debug Mode
- Kernel Mode
- User Mode

Table 2-1 the conditions of operating mode

Debug.DM	Status.UM	Status.EXL	Status.ERL	Operating Mode
1	X	X	X	Debug Mode
0	0	X	X	Kernel Mode
0	X	1	X	
0	X	X	1	
0	1	0	0	User Mode

X denotes don't care.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3 Multiple Channel Scaler (MScaler)

3.1 Overview

Multiple Channel Scaler, which takes MScaler as abbreviation, is used for image post processing including down scale ,crop ,mask ,flip and mirror.

3.2 Features

- Input Mode : Tiziano
- Input data format:
  - Tiziano：YUV420
- Output Mode :DMAOUT using AXI bus
- Output channel number:
  - 3 scaler channel
- Output data format:
  - NV12/NV21
- Minimum input image size (pixel): 8x8
- Maximum input image size (pixel): 2048x2048
- Minimum output image size (pixel): 8x8
- Maximum output image size (pixel): 2048x2048
  - Channel 0 ：2048*2048
  - Channel 1 ：1280*1280
  - Channel 2 ：640*640
- Minimum scale rate down to 1/32
- Each output channel enable can be configured independently
- Each output channel frame rate can be configured independently
- Each output channel can cover(mask) 4 areas with configured value independently
- Each output channel can support a crop function independently
- Each output channel can support a flip and mirror function independently

3.3 Block Diagram

Figure 3-1 shows the block diagram of MScaler data flow. One Online data channel. A frame rate control process should be done to get different frame rate videos before the resize process .Using 2 scale process channels to resize the same source image to 1 different resolution images,and source image. Image after resize process can do cover ,crop ,flip and mirror process before DMAOUT to DDR for each channel.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

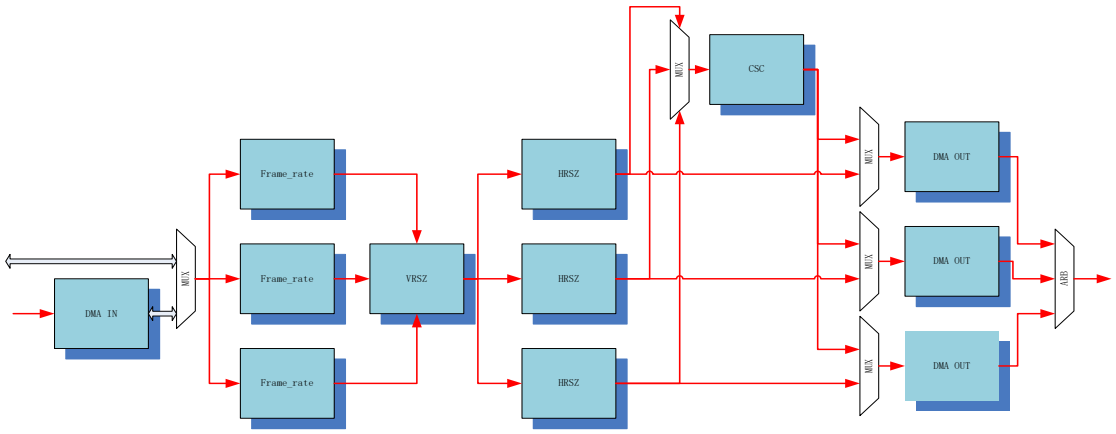


Figure 3-1 Block Diagram of MScaler data flow

3.4 Functional Description

MScaler is the module which can support resize function in high performance. At most output 2 re-sized images at the same time. Table 3-1 shows the main function points of MScaler.

Table 3-1 MScaler Main Function Points

Main Function	Input Format Support	Output Format Support	Output Destination
Resize	NV12/NV21/YUV422	NV12/NV21	DDR

3.4.1 Input

Input source and format register which is used to configure the source and format of MScaler input source data .

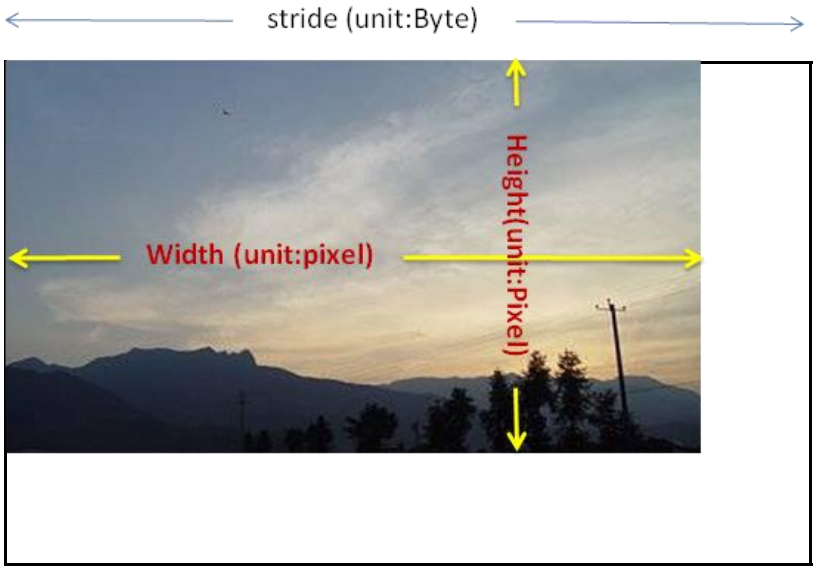


Figure 3-2 Picture Parameters

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

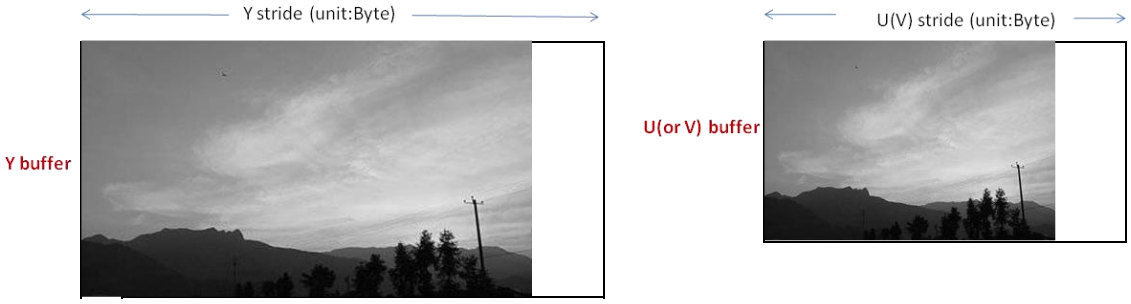


Figure 3-3 NV Picture Parameters

3.4.2 Resize Function

3 independent resize channels are used to do resize process, each channel can be configured with different output resolution .

Channel 0 Maximum output resolution :2048x2048

Channel 1 Maximum output resolution :1280x1280

Channel 2 Maximum output resolution :640x640

Each channel writes the re-sized image to DDR by DMAOUT . User should configure the output address and line stride for both Y data and UV data for each one of the 3 channels independently .

3.4.3 Frame rate control function

Each one of the 3 channels has its own frame rate control unit , user should configure these registers to get the right frame rate that you want :

1. FR_CTRL_LOOP register, it is used to control the loop length .The Maximum is 31 and the Minimum is 0.

2. FR_CTRL_MASK register , each one of the available bits that cut by FR_CTRL_LOOP register from bit 0 to bit "FR_CTRL_LOOP" of FR_CTRL_MASK is used to tell MScaler which frames should be kept and which frames should be dropped. High means being kept and low means being dropped .

3.4.4 Crop Function

Each channel provides a crop function after resize in MScaler, user should tell MScaler the upper left point coordinate and the size of the crop image that you want. The values of the coordinate 、 width and height are all should be even number .

MScaler DMAOUT the cropped image rather than the re-sized image .

Crop function has no bypass mode, if user do not want to do any crop , the upper left point coordinate should be set as (0,0) and the size should be set as the re-sized size .

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.4.5 Cover(Mask) Function

Each channel provides a mask function after resize in MScaler, which user can get 4 mask areas with the independent value .User should tell MScaler the upper left point coordinate 、mask size and values of the 4 mask areas .MScaler provides a MASK ENABLE for each channel ,set 0 will disable all the 4 mask areas . IF user do not want to mask all the 4 areas ,just set the MASK ENABLE high and set the size as 0 for the area that you do not want to mask .

3.4.6 FLIP and MIRROR Function

Each channel provides a flip and mirror function ,Flip means the hole image output upside down and mirror means left and right mirror .These two functions can configure at any time and don't need to stop the channel .

3.4.7 Scaler resize coefficient configure

All resize coefficients are stored in a single port RAM , which is 256 in depth and 44 bits in width. MScaler has 3 image channels ,every channel has Y and UV data channel , every data channel has to do vertical and horizontal resize , so there are 12 RAMs in total . Each one of these RAMs has its own register, through which CPU can configure the coefficient independently . The RAM width is 44 bits , but each time CPU write can only configure 22 bits ,so every one of the 256 stored cells must be wrote twice in series. The twice write operations must have the same WADDR but different HIGH_BIT.

There is the other way to configure these RAMs together by writing the global resize coefficient register.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WR_FINISH	HIGH_BIT	WADDR								WDATA																					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	WR_FINISH	All the 256 coefficients write finish	RW
30	HIGH_BIT	1:Write the high 22 bits of the address 0:Write the low 22 bits of the address	RW
29:22	WADDR	RAM address of this write	RW
21:0	WDATA	Value of this write	RW

Each RAM has its own register to read the value in RAM:

First of all , write this register with the address in RAM and high or low 22 bits that you want to read in the right order, then read this register. If the RDATA_VALID bit is high, means the RDATA is valid. Whenever the MScaler read these RAMs for inside logic, user can't get the valid RDATA.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDATA_VALID	HIGH_BIT	RADDR								RDATA																					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	RDATA_VALID	Whether the read data valid or not: 1:valid 0:not valid	R
30	HIGH_BIT	1：Read the high 22 bits of this RAM address 0：Read the low 22 bits of this RAM address	RW
29:22	RADDR	Read RAM address	RW
21:0	RDATA	Read data	RW

3.4.8 Reset

1.Write 1 to the bit 0 of MSCA_CTRL (0x000) as the soft reset of MScaler. The MScaler will be reset after all the current transfers on the AXI bus are finished .

3.4.9 Enable 、Disable and the Status of each channel

Enable：User can enable one channel by writing 1 to corresponding bit of MSCA_CH_EN(0x0004),it will work when the frame start signal comes.

Disable: User can disable one channel by writing 0 to corresponding bit of MSCA_CH_EN(0x0004),it will work whenever the frame start or the frame end signal comes .

Status(0x008):Each one of the 3 channels has its corresponding status bit in MSCA_CH_STAT(0x008) register , high means the channel is active and low means stopped . MSCA_CH_STAT is a read only register.

3.4.10 Work-flow

1.Set the function registers such as output image size , resize step ,address and stride, resize coefficient, crop position and size , mask position and size, frame rate control ,flip and mirror or not;

2.Set channel enable

3. Wait for frame start signal ;

3.4.11 Interrupt

Mscaler has an interrupt output , low active.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Inside the MScaler, there are 7 interrupt source , they are 3 frame end interrupts , 3 crop size error interrupts , 1 frame start error interrupt .

3.4.12 DMAOUT working mechanism

Each frame DMAOUT buffer address is stored in a 5 depth address FIFO, whenever the FIFO is not full ,CPU could write a new DMAOUT buffer address by write a given register .
The address FIFO has several status :
FIFO Full：FIFO is full，CPU can read but not write;
FIFO Empty：FIFO is empty，CPU can write but no buffer to DMAOUT;
FIFO Entry : The number of available address for DMAOUT in FIFO;
FIFO Rd_ptr ：Current read pointer ;
FIFO Wr_ptr ：Current write pointer ;
All the FIFOs have a clean function.

3.4.13 Frame number

NCU will give a 32 bits frame number , which is used for VPU encode. It is sent together with frame start signal to MScaler. MScaler will store this information together with the used buffer address in a LAST_ADDR_FIFO at the frame end pulse for each channel . CPU can read this FIFO to get the last address and frame number . User should first read DMA_LAST_ADDR register and then read the LAST_STATS_NUM register .Each time user read DMA_LAST_ADDR register , the frame number will change at the same time .

3.4.14 Output resolution reconfigure

First ,configure the corresponding bit in MSCA_CH_EN(0x004) to stop the channel ;
Second ,check the MSCA_CH_STAT to make sure that the channel is stopped ;
Third, set the new configuration and enable the channel .
The channel will work again when the next frame start comes.

3.5 Pins Description

MScaler has no IO pins.

3.6 Register Description

Following chapter will describe the functions of all software accessible registers.
Conventions:
1. Register Address = Base + Address offset
2. Register read/write attribute
   R- Read only
   W- Write only

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

RW- Read and Write
RCW- Read and Write, but Clear to 0 by Read
RSW- Read and Write, but Set to 1 by Read
RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
RC- Read only, and Clear to 0 by read
RS- Read only, and Set to 1 by read

3. Reset Value
1 - reset to 1
0 - reset to 0
? - value unknown after reset

3.6.1 Register Memory Map

Table 3-2 Registers Memory Map Base Address

Name	Base	Description
MScaler	0x13703500	Address base of ISP0 MScaler.
MScaler	0x13803500	Address base of ISP1 MScaler

The MScaler is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 3-3 MScaler Registers Map

Name	RW	Reset Value	Address Offset	Access Size
MSCA_CTRL	RW	0x0000_0000	0x0000	32
MSCA_CH_EN	RW	0x0000_0000	0x0004	32
MSCA_CH_STAT	RW	0x0000_0000	0x0008	32
DMA_OUY_ARB	RW	0x0000_0000	0x0018	32
CLK_GATE_EN	RW	0x0000_0000	0x001C	32
CLK_DIS	RW	0x0000_0000	0x0020	32
SRC_IN	RW	0x0000_0000	0x0030	32
GLO_RSZ_COEF_WR	RW	0x0000_0000	0x0040	32
SYS_PRO_CLK_EN	RW	0x0000_0000	0x0050	32
CH0_CLK_NUM	RW	0x0000_0000	0x0054	32
CH1_CLK_NUM	RW	0x0000_0000	0x0058	32
CH2_CLK_NUM	RW	0x0000_0000	0x005C	32
CH0_RSZ_OSIZE	RW	0x0000_0000	0x0100	32
CH0_RSZ_STEP	RW	0x0000_0000	0x0104	32
CH0_COE	RW	0x0000_0000	0x0108	32
CH0_COE_WIRE	RW	0x0000_0000	0x010C	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

CH0_CROP_OPOS	RW	0x0000_0000	0x0128	32
CH0_CROP_OSIZE	RW	0x0000_0000	0x012C	32
CH0_FR_CTRL_LOOP	RW	0x0000_0000	0x0130	32
CH0_FR_CTRL_MASK	RW	0x0000_0001	0x0134	32
CH0_MS0_POS	RW	0x0000_0000	0x0138	32
CH0_MS0_SIZE	RW	0x0000_0000	0x013C	32
CH0_MS0_VALUE	RW	0x0000_0000	0x0140	32
CH0_MS1_POS	RW	0x0000_0000	0x0144	32
CH0_MS1_SIZE	RW	0x0000_0000	0x0148	32
CH0_MS1_VALUE	RW	0x0000_0000	0x014C	32
CH0_MS2_POS	RW	0x0000_0000	0x0150	32
CH0_MS2_SIZE	RW	0x0000_0000	0x0154	32
CH0_MS2_VALUE	RW	0x0000_0000	0x0158	32
CH0_MS3_POS	RW	0x0000_0000	0x015C	32
CH0_MS3_SIZE	RW	0x0000_0000	0x0160	32
CH0_MS3_VALUE	RW	0x0000_0000	0x0164	32
CH0_OUT_FMT	RW	0x0000_0000	0x0168	32
CH0_DMAOUT_Y_ADDR	RW	0x0000_0000	0x016C	32
CH0_Y_ADDR_FIFO_STA	RW	0x0000_0000	0x0170	32
CH0_DMAOUT_Y_LAST_ADDR	RW	0x0000_0000	0x0174	32
CH0_DMAOUT_Y_LAST_STATS_NUM	RW	0x0000_0000	0x0178	32
CH0_Y_LAST_ADDR_FIFO_STA	RW	0x0000_0000	0x017C	32
CH0_DMAOUT_Y_STRI	RW	0x0000_0000	0x0180	32
CH0_DMAOUT_UV_ADDR	RW	0x0000_0000	0x0184	32
CH0_UV_ADDR_FIFO_STA	RW	0x0000_0000	0x0188	32
CH0_DMAOUT_UV_LAST_ADDR	RW	0x0000_0000	0x018C	32
CH0_DMAOUT_UV_LAST_STATS_NUM	RW	0x0000_0000	0x0190	32
CH0_UV_LAST_ADDR_FIFO_STA	RW	0x0000_0000	0x0194	32
CH0_DMAOUT_UV_STRI	RW	0x0000_0000	0x0198	32
CH0_DMAOUT_Y_ADDR_CLR	RW	0x0000_0000	0x019C	32
CH0_DMAOUT_UV_ADDR_CLR	RW	0x0000_0000	0x01A0	32
CH0_DMAOUT_Y_LAST_ADDR_CLR	RW	0x0000_0000	0x01A4	32
CH0_DMAOUT_UV_LAST_ADDR_CLR	RW	0x0000_0000	0x01A8	32
CH0_DMAOUT_Y_ADDR_SEL	RW	0x0000_0000	0x01AC	32
CH0_DMAOUT_UV_ADDR_SEL	RW	0x0000_0000	0x01B0	32
CH0_COE_ZERO_VRSZ_H	RW	0x0000_0000	0x01C0	32
CH0_COE_ZERO_VRSZ_L	RW	0x0000_0000	0x01C4	32
CH0_COE_ZERO_HRSZ_H	RW	0x0000_0000	0x01C8	32
CH0_COE_ZERO_HRSZ_L	RW	0x0000_0000	0x01CC	32
CH0_COE_OFT	RW	0x0000_0000	0x01D0	32
CH1_RSZ_OSIZE	RW	0x0000_0000	0x0200	32
CH1_RSZ_STEP	RW	0x0000_0000	0x0204	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

CH1_Y_HRSZ_COEF_WR	RW	0x0000_0000	0x0208	32
CH1_Y_HRSZ_COEF_RD	RW	0x0000_0000	0x020C	32
CH1_Y_VRSZ_COEF_WR	RW	0x0000_0000	0x0210	32
CH1_Y_VRSZ_COEF_RD	RW	0x0000_0000	0x0214	32
CH1_UV_HRSZ_COEF_WR	RW	0x0000_0000	0x0218	32
CH1_UV_HRSZ_COEF_RD	RW	0x0000_0000	0x021C	32
CH1_UV_VRSZ_COEF_WR	RW	0x0000_0000	0x0220	32
CH1_UV_VRSZ_COEF_RD	RW	0x0000_0000	0x0224	32
CH1_CROP_OPOS	RW	0x0000_0000	0x0228	32
CH1_CROP_OSIZE	RW	0x0000_0000	0x022C	32
CH1_FR_CTRL_LOOP	RW	0x0000_0000	0x0230	32
CH1_FR_CTRL_MASK	RW	0x0000_0001	0x0234	32
CH1_MS0_POS	RW	0x0000_0000	0x0238	32
CH1_MS0_SIZE	RW	0x0000_0000	0x023C	32
CH1_MS0_VALUE	RW	0x0000_0000	0x0240	32
CH1_MS1_POS	RW	0x0000_0000	0x0244	32
CH1_MS1_SIZE	RW	0x0000_0000	0x0248	32
CH1_MS1_VALUE	RW	0x0000_0000	0x024C	32
CH1_MS2_POS	RW	0x0000_0000	0x0250	32
CH1_MS2_SIZE	RW	0x0000_0000	0x0254	32
CH1_MS2_VALUE	RW	0x0000_0000	0x0258	32
CH1_MS3_POS	RW	0x0000_0000	0x025C	32
CH1_MS3_SIZE	RW	0x0000_0000	0x0260	32
CH1_MS3_VALUE	RW	0x0000_0000	0x0264	32
CH1_OUT_FMT	RW	0x0000_0000	0x0268	32
CH1_DMAOUT_Y_ADDR	RW	0x0000_0000	0x026C	32
CH1_Y_ADDR_FIFO_STA	RW	0x0000_0000	0x0270	32
CH1_DMAOUT_Y_LAST_ADDR	RW	0x0000_0000	0x0274	32
CH1_DMAOUT_Y_LAST_STATS_NUM	RW	0x0000_0000	0x0278	32
CH1_Y_LAST_ADDR_FIFO_STA	RW	0x0000_0000	0x027C	32
CH1_DMAOUT_Y_STRI	RW	0x0000_0000	0x0280	32
CH1_DMAOUT_UV_ADDR	RW	0x0000_0000	0x0284	32
CH1_UV_ADDR_FIFO_STA	RW	0x0000_0000	0x0288	32
CH1_DMAOUT_UV_LAST_ADDR	RW	0x0000_0000	0x028C	32
CH1_DMAOUT_UV_LAST_STATS_NUM	RW	0x0000_0000	0x0290	32
CH1_UV_LAST_ADDR_FIFO_STA	RW	0x0000_0000	0x0294	32
CH1_DMAOUT_UV_STRI	RW	0x0000_0000	0x0298	32
CH1_DMAOUT_Y_ADDR_CLR	RW	0x0000_0000	0x029C	32
CH1_DMAOUT_UV_ADDR_CLR	RW	0x0000_0000	0x02A0	32
CH1_DMAOUT_Y_LAST_ADDR_CLR	RW	0x0000_0000	0x02A4	32
CH1_DMAOUT_UV_LAST_ADDR_CLR	RW	0x0000_0000	0x02A8	32
CH1_DMAOUT_Y_ADDR_SEL	RW	0x0000_0000	0x02AC	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

CH1_DMAOUT_UV_ADDR_SEL	RW	0x0000_0000	0x02B0	32
CH1_COE_ZERO_VRSZ_H	RW	0x0000_0000	0x02C0	32
CH1_COE_ZERO_VRSZ_L	RW	0x0000_0000	0x02C4	32
CH1_COE_ZERO_HRSZ_H	RW	0x0000_0000	0x02C8	32
CH1_COE_ZERO_HRSZ_L	RW	0x0000_0000	0x02CC	32
CH1_COE_OFT	RW	0x0000_0000	0x02D0	32
CH2_RSZ_OSIZE	RW	0x0000_0000	0x0300	32
CH2_RSZ_STEP	RW	0x0000_0000	0x0304	32
CH2_Y_HRSZ_COEF_WR	RW	0x0000_0000	0x0308	32
CH2_Y_HRSZ_COEF_RD	RW	0x0000_0000	0x030C	32
CH2_Y_VRSZ_COEF_WR	RW	0x0000_0000	0x0310	32
CH2_Y_VRSZ_COEF_RD	RW	0x0000_0000	0x0314	32
CH2_UV_HRSZ_COEF_WR	RW	0x0000_0000	0x0318	32
CH2_UV_HRSZ_COEF_RD	RW	0x0000_0000	0x031C	32
CH2_UV_VRSZ_COEF_WR	RW	0x0000_0000	0x0320	32
CH2_UV_VRSZ_COEF_RD	RW	0x0000_0000	0x0324	32
CH2_CROP_OPOS	RW	0x0000_0000	0x0328	32
CH2_CROP_OSIZE	RW	0x0000_0000	0x032C	32
CH2_FR_CTRL_LOOP	RW	0x0000_0000	0x0330	32
CH2_FR_CTRL_MASK	RW	0x0000_0001	0x0334	32
CH2_MS0_POS	RW	0x0000_0000	0x0338	32
CH2_MS0_SIZE	RW	0x0000_0000	0x033C	32
CH2_MS0_VALUE	RW	0x0000_0000	0x0340	32
CH2_MS1_POS	RW	0x0000_0000	0x0344	32
CH2_MS1_SIZE	RW	0x0000_0000	0x0348	32
CH2_MS1_VALUE	RW	0x0000_0000	0x034C	32
CH2_MS2_POS	RW	0x0000_0000	0x0350	32
CH2_MS2_SIZE	RW	0x0000_0000	0x0354	32
CH2_MS2_VALUE	RW	0x0000_0000	0x0358	32
CH2_MS3_POS	RW	0x0000_0000	0x035C	32
CH2_MS3_SIZE	RW	0x0000_0000	0x0360	32
CH2_MS3_VALUE	RW	0x0000_0000	0x0364	32
CH2_OUT_FMT	RW	0x0000_0000	0x0368	32
CH2_DMAOUT_Y_ADDR	RW	0x0000_0000	0x036C	32
CH2_Y_ADDR_FIFO_STA	RW	0x0000_0000	0x0370	32
CH2_DMAOUT_Y_LAST_ADDR	RW	0x0000_0000	0x0374	32
CH2_DMAOUT_Y_LAST_STATS_NUM	RW	0x0000_0000	0x0378	32
CH2_Y_LAST_ADDR_FIFO_STA	RW	0x0000_0000	0x037C	32
CH2_DMAOUT_Y_STRI	RW	0x0000_0000	0x0380	32
CH2_DMAOUT_UV_ADDR	RW	0x0000_0000	0x0384	32
CH2_UV_ADDR_FIFO_STA	RW	0x0000_0000	0x0388	32
CH2_DMAOUT_UV_LAST_ADDR	RW	0x0000_0000	0x038C	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

CH2_DMAOUT_UV_LAST_STATS_NUM	RW	0x0000_0000	0x0390	32
CH2_UV_LAST_ADDR_FIFO_STA	RW	0x0000_0000	0x0394	32
CH2_DMAOUT_UV_STRI	RW	0x0000_0000	0x0398	32
CH2_DMAOUT_Y_ADDR_CLR	RW	0x0000_0000	0x039C	32
CH2_DMAOUT_UV_ADDR_CLR	RW	0x0000_0000	0x03A0	32
CH2_DMAOUT_Y_LAST_ADDR_CLR	RW	0x0000_0000	0x03A4	32
CH2_DMAOUT_UV_LAST_ADDR_CLR	RW	0x0000_0000	0x03A8	32
CH2_DMAOUT_Y_ADDR_SEL	RW	0x0000_0000	0x03AC	32
CH2_DMAOUT_UV_ADDR_SEL	RW	0x0000_0000	0x03B0	32
CH2_COE_ZERO_VRSZ_H	RW	0x0000_0000	0x03C0	32
CH2_COE_ZERO_VRSZ_L	RW	0x0000_0000	0x03C4	32
CH2_COE_ZERO_HRSZ_H	RW	0x0000_0000	0x03C8	32
CH2_COE_ZERO_HRSZ_L	RW	0x0000_0000	0x03CC	32
CH2_COE_OFT	RW	0x0000_0000	0x03D0	32

3.6.2 Register and Fields Description

3.6.2.1 MScaler Control Register（MSCA_CTRL, 0x0000）

The MSCA_CTRL is to start or stop the MScaler .

	MSCA_CTRL																BASE + 0x0000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															Mode
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	Mode	1=safe stop(MScaler will stop when AXI bus safe)	RW

3.6.2.2 MScaler Ch Enable Register（MSCA_CH_EN, 0x0004）

The MSCA_CH_ENABLE register is used to enable or stop the resize channel and mask function.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	MSCA_CH_EN																		BASE + 0x0004																	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		ds2_coef_fix_hrsz_en	ds1_coef_fix_hrsz_en	ds0_coef_fix_hrsz_en	ds2_coef_fix_vrsz_en	ds1_coef_fix_vrsz_en	ds0_coef_fix_vrsz_en	Reserved		CH2_MS_EN	CH1_MS_EN	CH0_MS_EN	CH2_RSZ_EN	CH1_RSZ_EN	CH0_RSZ_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:14	Reserved	Writing has no effect. Read as zero.	R
13	ds2_coef_fix_hrsz_en	channel 2 hrsz all coef fix zero value enable	RW
12	ds1_coef_fix_hrsz_en	channel 1 hrsz all coef fix zero value enable	RW
11	ds0_coef_fix_hrsz_en	channel 0 hrsz all coef fix zero value enable	RW
10	ds2_coef_fix_vrsz_en	channel 2 vrsz all coef fix zero value enable	RW
9	ds1_coef_fix_vrsz_en	channel 1 vrsz all coef fix zero value enable	RW
8	ds0_coef_fix_vrsz_en	channel 0 vrsz all coef fix zero value enable	RW
7:6	Reserved	Writing has no effect. Read as zero.	R
5	CH2_MS_EN	CH2 mask enable	RW
4	CH1_MS_EN	CH1 mask enable	RW
3	CH0_MS_EN	CH0 mask enable	RW
2	CH2_RSZ_EN	CH2 Resize Enable	RW
1	CH1_RSZ_EN	CH1 Resize Enable	RW
0	CH0_RSZ_EN	CH0 Resize Enable	RW

3.6.2.3 MScaler Ch Status Register（MSCA_CH_STAT, 0x0008）

The MSCA_CH_STAT is used to indicate that whether the channel is enabled.

	MSCA_CH_STAT																										BASE + 0x0008					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										CH2_MASK_STAT	CH1_MASK_STAT	CH0_MASK_STAT	CH2_WROK_STAT	CH1_WROK_STAT	CH0_WROK_STAT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:6	Reserved	Writing has no effect. Read as zero.	R
5	CH2_MASK_STAT	1:active 0: No Mask	R
4	CH1_MASK_STAT	1:active 0: No Mask	R
3	CH0_MASK_STAT	1:active 0: No Mask	R
2	CH2_WORK_STAT	1:active 0：stop	R
1	CH1_WORK_STAT	1:active 0：stop	R
0	CH0_WORK_STAT	1:active 0：stop	R

3.6.2.4 DMA Out Arbiter Control Register（DMA_OUT_ARB, 0x0018）

The DMA_OUT_ARB register is used to indicate the DMA out mode of 3 DMA channels.

	DMA_OUT_ARB																BASE + 0x0018											
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																						CH2_MIRROR	CH1_MIRROR	CH0_MIRROR	CH2_FLIP	CH1_FLIP	CH0_FLIP	CH2_UV_RSMP	CH1_UV_RSMP	CH0_UV_RSMP	DMA_DONE_MODE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:10	Reserved	Writing has no effect. Read as zero.	R
9	CH2_MIRROR	DMAOUT image mirror or not 1= Mirror the image 0=don't mirror the image	RW
8	CH1_MIRROR	DMAOUT image mirror or not 1= Mirror the image 0=don't mirror the image	RW
7	CH0_MIRROR	DMAOUT image mirror or not 1= Mirror the image 0=don't mirror the image	RW
6	CH2_FLIP	DMAOUT image flip or not	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1= Flip the image 0=don't flip the image	
5	CH1_FLIP	DMAOUT image flip or not 1= Flip the image 0=don't flip the image	RW
4	CH0_FLIP	DMAOUT image flip or not 1= Flip the image 0=don't flip the image	RW
3	CH2_UV_RSMP	UV pixel re-sample mode for DMAOUT 0= re-sample each two line and two column(total 4 pixel) (by average) one UV; 1=don't re-sample, just keep each odd line and column UV	RW
2	CH1_UV_RSMP	UV pixel re-sample mode for DMAOUT 0= re-sample each two line and two column(total 4 pixel) (by average) one UV; 1=don't re-sample, just keep each odd line and column UV	RW
1	CH0_UV_RSMP	UV pixel re-sample mode for DMAOUT 0= re-sample each two line and two column(total 4 pixel) (by average) one UV; 1=don't re-sample, just keep each odd line and column UV	RW
0	DMA_DONE_MODE	DMA DONE whether depend on the bvalid(AXI bus) or not. 1=depend on 0=not depend on	RW

3.6.2.5 Clock Gate Enable Register（CLK_GATE_EN,0x001C）

The CLK_GATE_EN register is used to indicate the clock gate enable for every sub module.

	CLK_GATE_EN																BASE + 0x001C																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											HRSZ2_CLK_GATE	HRSZ1_CLK_GATE	HRSZ0_CLK_GATE	VRSZ_CLK_GATE	DMA_CLK_GATE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect. Read as zero.	R
4	HRSZ2_CLK_GATE	HRSZ2 CLK GATE Enable 0：No gate，1：gate	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3	HRSZ1_CLK_GATE	HRSZ1 CLK GATE Enable 0：No gate，1：gate	RW
2	HRSZ0_CLK_GATE	HRSZ0 CLK GATE Enable 0：No gate，1：gate	RW
1	VRSZ_CLK_GATE	VRSZ CLK GATE Enable 0：No gate，1：gate	RW
0	DMA_CLK_GATE	DMAIN/DMAOUT CLK GATE Enable 0：No gate，1：gate	RW

3.6.2.6 Clock Disable Register（CLK_DIS,0x0020）

Whole MScaler clock gate register .

CLK_DIS																		BASE + 0x0020													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CLK_DIS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect.Read as zero.	R
0	CLK_DIS	Module clock disable ,0:clock enable 1:MScaler clock disable	RW

3.6.2.7 Source Image In Register（SRC_IN, 0x0030）

The SRC_IN register is used to tell MScaler the source image format and UV replenish mode.

SRC_IN																		BASE + 0x0030													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													SRC_SAMPLE_CH2	SRC_SAMPLE_CH1	SRC_SAMPLE_CH0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect. Read as zero.	R
3	SRC_SAMPLE_CH2	Two mode to replenish Channel 2 input image NV12/NV21 to YUV444, 0=copy the closest UV data 1=take mean value of the two closest UV data	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

2	SRC_SAMPLE_CH1	Two mode to replenish Channel 1 input image NV12/NV21 to YUV444, 0=copy the closest UV data 1=take mean value of the two closest UV data	RW
1	SRC_SAMPLE_CH0	Two mode to replenish Channel 0 input image NV12/NV21 to YUV444, 0=copy the closest UV data 1=take mean value of the two closest UV data	RW

3.6.2.8 Global Resize Coefficient Write（GLO_RSZ_COEF_WR, 0x0040)

The GLO_RSZ_COEF_WR register is used to indicate the interpolation coefficient for all data channel .

	GLO_RSZ_COEF_WR																BASE + 0x0040															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WR_FINISH	HIGH_BIT	WADDR														WDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	WR_FINISH	RAM write finish	RW
30	HIGH_BIT	1：Write to the high 22 bits of RAM address 0：Write to the low 22 bits of RAM address	RW
29:22	WADDR	Write RAM address	RW
21:0	WDATA	Write RAM value	RW

3.6.2.9 MScaler Process cost System Clock Cycle Number Enable （SYS_PRO_CLK_EN, 0x0050）

The SYS_PRO_CLK_EN register is used to Enable the system clock cycle number it cost when MScaler process one frame .

	SYS_PRO_CLK_EN																BASE + 0x0050															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													CH2_CLK_NUM_EN	CH1_CLK_NUM_EN	CH0_CLK_NUM_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect. Read as zero.	R
2	CH2_CLK_NUM_EN	CH2 CLOCK CNT ENABLE	RW
1	CH1_CLK_NUM_EN	CH1 CLOCK CNT ENABLE	RW
0	CH0_CLK_NUM_EN	CH0 CLOCK CNT ENABLE	RW

3.6.2.10 CH0 Clock Cycle Number（CH0_CLK_NUM, 0x0054）

The CH0_CLK_NUM register is used to indicate the system clock cycle number it cost when MScaler process one frame on CH0 .

	CH0_CLK_NUM																BASE + 0x0054															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_CLK_NUM																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH0_CLK_NUM	Frame start valid ,the count register inside MScaler clean to 0, when do scale and SYS_PRO_CLK_EN [0] is high , every clock cycle the count register add by 1,till the frame finished .MScaler will write the count register value to CH0_CLK_NUM.	R

3.6.2.11 CH1 Clock Cycle Number（CH1_CLK_NUM, 0x0058）

The CH1_CLK_NUM register is used to indicate the system clock cycle number it cost when MScaler process one frame on CH1.

	CH1_CLK_NUM																BASE + 0x0058															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_CLK_NUM																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH1_CLK_NUM	Frame start valid ,the count register inside MScaler clean to 0, when do scale and SYS_PRO_CLK_EN [1] is high , every clock cycle the count register add by 1,till the frame finished .MScaler will write the count register value to CH1_CLK_NUM.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.12 CH2 Clock Cycle Number（CH2_CLK_NUM, 0x005C）

The CH2_CLK_NUM register is used to indicate the system clock cycle number it cost when MScaler process one frame on CH2 .

	CH2_CLK_NUM																BASE + 0x005C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_CLK_NUM																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH2_CLK_NUM	Frame start valid ,the count register inside MScaler clean to 0, when do scale and SYS_PRO_CLK_EN [2] is high , every clock cycle the count register add by 1,till the frame finished .MScaler will write the count register value to CH2_CLK_NUM.	R

3.6.2.13 Ch 0 Resize Out Image Size（CH0_RSZ_OSIZE, 0x0100）

Channel 0 scale output image size, both the width and the height should be even number. This is not the DMAOUT image size.

	CH0_RSZ_OSIZE																BASE + 0x00100													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_RSZ_OW																CH0_RSZ_OH															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH0_RSZ_OW	The width of the channel 0 resize out frame (unit: pixel)	RW
15:0	CH0_RSZ_OH	The height of the channel 0 resize out frame (unit: pixel)	RW

3.6.2.14 Ch 0 Resize Step Register（CH0_RSZ_STEP, 0x0104）

The CH0_RSZ_STEP is used to indicate the scale step of Channel 0, the CH0_STEP_W value equals floor(SRC_W/CH0_RSZ_OW * 512), the CH0_STEP_H value equals floor(SRC_H/CH0_RSZ_OH * 512).

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	CH0_RSZ_STEP																BASE + 0x0104															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_STEP_W																CH0_STEP_H															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH0_STEP_W	The width resize scale step of channel 0	RW
15:0	CH0_STEP_H	The height resize scale step of channel 0	RW

3.6.2.15 Ch 0 Coe Register（CH0_COE, 0x0108）

The CH0_COE Register is select coef value mux.

	CH0_COEF																												BASE + 0x0108	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														CH0_COE_SEL	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect. Read as zero.	R
1:0	CH0_COE_SEL	channel 0 coe value select	RW

3.6.2.16 Ch 0 Coe Wire Register（CH0_COE, 0x0108）

The CH0_COE_WIRE Register is wire value enable and slope.

	CH0_RSZ_STEP																BASE + 0x010C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ch0_coe_hrsz_wire_en	Reserved							ch0_coe_hrsz_wire_slope								ch0_coe_vrsz_wire_en	Reserved							ch0_coe_vrsz_wire_slope							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31	ch0_coe_hrsz_wire_en	ch0 reszie coe hrsz value use wire enable	RW
30:24	Reserved	Writing has no effect. Read as zero.	R
23:16	ch0_coe_hrsz_wire_slope	ch0 reszie coe hrsz wire slope	RW
15	ch0_coe_vrsz_wire_en	ch0 resize coe vrsz value use wire enable	RW
14:8	Reserved	Writing has no effect. Read as zero.	R
7:0	ch0_coe_vrsz_wire_slope	ch0 resize coe vrsz wire slope	RW

3.6.2.17 Ch 0 Crop Out Image Position（CH0_CROP_OPOS, 0x0128）

The CH0_CROP_OPOS is used to indicate the crop start point after scale, both the X-axis and the Y-axis should be even number .

	CH0_CROP_OPOS																BASE + 0x0128															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_CROP_OX																CH0_CROP_OY															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH0_CROP_OX	Crop upper-left point X-axis position of channel 0 crop output image .	RW
15:0	CH0_CROP_OY	Crop upper-left point Y-axis position of channel 0 crop output image .	RW

3.6.2.18 Ch 0 Crop Out Image Size（CH0_CROP_OSIZE, 0x012C）

The CH0_CROP_OSIZE is used to indicate the Channel 0 Crop output image size, both the width and the height should be even number . This size is the channel 0 final output size.

	CH0_CROP_OSIZE																BASE + 0x012C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_CROP_OW																CH0_CROP_OH															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:16	CH0_CROP_OW	The width of channel 0 crop output image , unit pixel	RW
15:0	CH0_CROP_OH	The height of channel 0 crop output image , unit pixel	RW

3.6.2.19 Ch 0 Frame Rate Ctrl Loop(CH0_FR_CTRL_LOOP, 0x0130)

The CH0_FR_CTRL_LOOP is used to indicate the maximum value of frame rate control loop number. For example the number is N, it means that it will take the bit 0 to bit N(N+1 in total) from CH0_FR_CTRL_MASK to do frame rate control . Maximum number is 31.

	CH0_FR_CTRL_LOOP																															
																												BASE + 0x0130				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											CH0_FR_CTRL_LOOP				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect. Read as zero.	R
4:0	CH0_FR_CTRL_LOOP	Maximum: 31, Minimum:0	RW

3.6.2.20 Ch 0 Frame Rate Ctrl Mask(CH0_FR_CTRL_MASK, 0x0134)

The CH0_FR_CTRL_MASK is used to indicate which frames should be kept and which frames should be dropped .The corresponding bit is 1 means kept , 0 means dropped .The valid bits of this register is from bit 0 to bit CH0_FR_CTRL_LOOP.

	CH0_FR_CRTL_MASK																															
																												BASE + 0x0134				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_FR_CTRL_MASK																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	CH0_FR_CTRL_MASK	the valid bits of CH0_FR_CTRL_MASK is [CH0_FR_CTRL_LOOP:0]	RW

Note： The CH0_FR_CTRL_MASK should be better configured after CH0_FR_CTRL_LOOP .

3.6.2.21 Ch 0 Mask0 Pos Register（CH0_MS0_POS, 0x0138）

The CH0_MS0_POS is used to indicate the mask start point of the area 0 of channel 0 after scale, both the X-axis and the Y-axis should be even number .

	CH0_MS0_POS																BASE + 0x0138															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_MS0_POS_X																CH0_MS0_POS_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH0_MS0_POS_X	The X-axis of channel 0 mask area 0	RW
15:0	CH0_MS0_POS_Y	The Y-axis of channel 0 mask area 0	RW

3.6.2.22 Ch 0 Mask0 Size Register（CH0_MS0_SIZE, 0x013C）

The CH0_MS0_SIZE is used to indicate the mask size of the area 0 of channel 0 after scale, both the width and the height should be even number .

	CH0_MS0_SIZE																BASE + 0x013C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_MS0_SIZE_X																CH0_MS0_SIZE_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH0_MS0_SIZE_X	The Width of channel 0 mask area 0	RW
15:0	CH0_MS0_SIZE_Y	The Height of channel 0 mask area 0	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.23 Ch 0 Mask0 Value Register（CH0_MS0_VALUE, 0x0140）

The CH0_MS0_VALUE is used to indicate the value of the mask area 0 of channel 0.

	CH0_MS0_VALUE																BASE + 0x0140															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_MS0_VALUE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH0_MS0_VALUE	When CH0_MASK_EN =1, if the pixel located in Mask0 ,channel 0 will output this ARGB values for Mask function. If output picture format is ARGB/RGB, this data sequence of this register is also ARGB. If background picture format is NV12/NV21, then the data sequence of this register is AYVU/AYUV	RW

Note:

1. Mask function has a priority to decide what value should output when the pixel located in overlapping mask area. Mask0 has the highest priority .
2.When output type is ARGB/RGB, the 32 bits mask value should set with the same order as output type ,for example ,if output is RBGA, the mask value is also should be RBGA .
3.When output type is RGB565, the 32 bits mask value should set as RGBRGB.

3.6.2.24 Ch 0 Mask1 Pos Register（CH0_MS1_POS, 0x0144）

The CH0_MS1_POS is used to indicate the mask start point of the area 1 of channel 0 after scale, both the X-axis and the Y-axis should be even number.

	CH0_MS1_POS																BASE + 0x0144															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_MS1_POS_X																CH0_MS1_POS_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH0_MS1_POS_X	The X-axis of channel 0 mask area 1	RW
15:0	CH0_MS1_POS_Y	The Y-axis of channel 0 mask area 1	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.25 Ch 0 Mask1 Size Register（CH0_MS1_SIZE, 0x0148）

The CH0_MS1_SIZE is used to indicate the mask size of the area 1 of channel 0 after scale, both the width and the height should be even number.

	CH0_MS1_SIZE																BASE + 0x0148															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_MS1_SIZE_X																CH0_MS1_SIZE_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH0_MS1_SIZE_X	The Width of channel 0 mask area 1	RW
15:0	CH0_MS1_SIZE_Y	The Height of channel 0 mask area 1	RW

3.6.2.26 Ch 0 Mask1 Value Register（CH0_MS1_VALUE, 0x014C）

The CH0_MS1_VALUE is used to indicate the value of the mask area 1 of channel 0.

	CH0_MS1_VALUE																BASE + 0x014C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_MS1_VALUE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH0_MS1_VALUE	When CH0_MASK_EN =1, if the pixel located in Mask0 ,channel 0 will output this ARGB values for Mask function. If output picture format is ARGB/RGB, this data sequence of this register is also ARGB. If background picture format is NV12/NV21, then the data sequence of this register is AYVU/AYUV	RW

Note:

1. Mask function has a priority to decide what value should output when the pixel located in over;
2.When output type is ARGB/RGB, the 32 bits mask value should set with the same order as output type ,for example ,if output is RBGA, the mask value is also should be RBGA .
3.When output type is RGB565, the 32 bits mask value should set as RGBRGB.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.27 Ch 0 Mask2 Pos Register（CH0_MS2_POS, 0x0150）

The CH0_MS2_POS is used to indicate the mask start point of the area 2 of channel 0 after scale, both the X-axis and the Y-axis should be even number.

	CH0_MS2_POS																BASE + 0x0150															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_MS2_POS_X																CH0_MS2_POS_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH0_MS2_POS_X	The X-axis of channel 0 mask area 2	RW
15:0	CH0_MS2_POS_Y	The Y-axis of channel 0 mask area 2	RW

3.6.2.28 Ch 0 Mask2 Size Register（CH0_MS2_SIZE, 0x0154）

The CH0_MS2_SIZE is used to indicate the mask size of the area 2 of channel 0 after scale, both the width and the height should be even number.

	CH0_MS2_SIZE																BASE + 0x0154															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_MS2_SIZE_X																CH0_MS2_SIZE_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH0_MS2_SIZE_X	The Width of channel 0 mask area 2	RW
15:0	CH0_MS2_SIZE_Y	The Height of channel 0 mask area 2	RW

3.6.2.29 Ch 0 Mask2 Value Register（CH0_MS2_VALUE, 0x0158）

The CH0_MS2_VALUE is used to indicate the value of the mask area 2 of channel 0.

	CH0_MS2_VALUE																BASE + 0x0158															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_MS2_VALUE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	CH0_MS2_VALUE	When CH0_MASK_EN =1, if the pixel located in Mask0 ,channel 0 will output this ARGB values for Mask function. If output picture format is ARGB/RGB, this data sequence of this register is also ARGB. If background picture format is NV12/NV21, then the data sequence of this register is AYVU/AYUV	RW

Note:

1. Mask function has a priority to decide what value should output when the pixel located in over
2.When output type is ARGB/RGB, the 32 bits mask value should set with the same order as output type ,for example ,if output is RBGA, the mask value is also should be RBGA .
3.When output type is RGB565, the 32 bits mask value should set as RGBRGB.

3.6.2.30 Ch 0 Mask3 Pos Register（CH0_MS3_POS, 0x015C）

The CH0_MS3_POS is used to indicate the mask start point of the area 3 of channel 0 after scale, both the X-axis and the Y-axis should be even number.

	CH0_MS3_POS																BASE + 0x015C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_MS3_POS_X																CH0_MS3_POS_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH0_MS3_POS_X	The X-axis of channel 0 mask area 3	RW
15:0	CH0_MS3_POS_Y	The Y-axis of channel 0 mask area 3	RW

3.6.2.31 Ch 0 Mask3 Size Register（CH0_MS3_SIZE, 0x0160）

The CH0_MS3_SIZE is used to indicate the mask size of the area 3 of channel 0 after scale, both the width and the height should be even number.

	CH0_MS3_SIZE																BASE + 0x0160															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_MS3_SIZE_X																CH0_MS3_SIZE_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:16	CH0_MS3_SIZE_X	The Width of channel 0 mask area 3	RW
15:0	CH0_MS3_SIZE_Y	The Height of channel 0 mask area 3	RW

3.6.2.32 Ch 0 Mask3 Value Register（CH0_MS3_VALUE, 0x0164）

The CH0_MS3_VALUE is used to indicate the value of the mask area 3 of channel 0.

	CH0_MS3_VALUE																BASE + 0x0164															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_MS3_VALUE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH0_MS3_VALUE	When CH0_MASK_EN =1, if the pixel located in Mask0 ,channel 0 will output this ARGB values for Mask function. If output picture format is ARGB/RGB, this data sequence of this register is also ARGB. If background picture format is NV12/NV21, then the data sequence of this register is AYVU/AYUV	RW

Note:

1. Mask function has a priority to decide what value should output when the pixel located in over
2.When output type is ARGB/RGB, the 32 bits mask value should set with the same order as output type ,for example ,if output is RBGA, the mask value is also should be RBGA .
3.When output type is RGB565, the 32 bits mask value should set as RGBRGB.

3.6.2.33 Ch 0 Out Data Format Register（CH0_OUT_FMT, 0x0168）

The CH0_OUT_FMT is used to indicate the Channel 0 output format . There is only one channel can do CSC transfer , so there is only one channel can set ARGB/RGB type output , the other two channels should be set as NV12/NV21.If there are more than one channel set as ARGB/RGB output, the MScaler will get a highest priority for channel 0 and the lowest priority for channel 2 to output ARGB/RGB. The lower priority channels will has an error occurred . So make sure less than two channels are set as ARGB/RGB output format .

	CH0_OUT_FMT																BASE + 0x0168															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									Y_OUT_ONLY	RGB_ORDER				OUT_FMT	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect. Read as zero.	R
6	Y_OUT_ONLY	1:DMAOUT Y DATA ONLY 0:BOTH Y AND UV DATA DMAOUT	RW
5:2	RGB_ORDER	ARGB order. 4'b0000: BGRA 4'b0001: GBRA 4'b0010: RBGA 4'b0011: BRGA 4'b0100: GRBA 4'b0101: RGBA 4'b1000: ABGR 4'b1001: AGBR 4'b1010: ARBG 4'b1011: ABRG 4'b1100: AGRB 4'b1101: ARGB RGB565 0:BGR 1:GBR 2:RBG 3:BRG 4:GRB 5:RGB	RW
1:0	OUT_FMT	00:NV12 01:NV21 02:ARGB888 03: RGB565	RW

3.6.2.34 Ch 0 DMAOUT Y Buff Address（CH0_DMAOUT_Y_ADDR, 0x016C）

The CH0_DMAOUT_Y_ADDR is used to indicate the channel 0 Y data DMAOUT buffer address .8 bytes align .Write this register , MScaler will store the address in a 5 depth FIFO .(if the FIFO is full , CPU should not write anymore, user can check its status by read CH0_Y_ADDR_FIFO_STA register).

DMAOUT will read the FIFO when frame start comes .CPU read data is the current address that DMAOUT is using .

	CH0_DMAOUT_Y_ADDR																BASE + 0x016C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_DMAOUT_Y_ADDR[31:3]																													Reserved		ADDR_STATU
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	CH0_DMAOUT_Y_ADDR[31:3]	The DMAOUT address that MScaler is being used . 8 byte align	RW
2:1	Reserved	Writing has no effect.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Read as zero.	
0	ADDR_STATU	0:current frame DMAOUT finished 1:current frame is DMAOUT	R

3.6.2.35 Ch 0 Y Buff Address FIFO Status（CH0_Y_ADDR_FIFO_STA, 0x0170）

The CH0_Y_ADDR_FIFO_STA is used to indicate the status of Y address FIFO of channel 0 .

	CH0_Y_ADDR_FIFO_STA																														
																	BASE + 0x0170														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					Wr_ptr			Rd_ptr			Entry			Full	Empty
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect. Read as zero.	R
10:8	Wr_ptr	write point of FIFO,0~4	R
7:5	Rd_ptr	read point of FIFO,0~4	R
4:2	Entry	valid address number,0~5	R
1	Full	FIFO Full , high valid	R
0	Empty	FIFO Empty, high valid	R

3.6.2.36 Ch 0 Y Buff Last Address（CH0_DMAOUT_Y_LAST_ADDR, 0x0174）

The CH0_DMAOUT_Y_LAST_ADDR is used to indicate the last DMAOUT address of channel 0 .8 bytes align .Read only .User should read the FIFO status before read this register , if it is not empty ,user can get the last DMAOUT address of channel 0 Y data . If the FIFO is full , MScaler can't write anymore, the address information will lose .

	CH0_DMAOUT_Y_LAST_ADDR																														
																	BASE + 0x0174														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_DMAOUT_Y_LAST_ADDR																														
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH0_DMAOUT_Y_ LAST_ADDR	Last DMAOUT address of channel 0 Y data	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.37 Ch 0 Y Buff Last Stats Num（CH0_DMAOUT_Y_LAST_STATS_NUM, 0x0178）

The CH0_DMAOUT_Y_LAST_STATS_NUM is used to indicate the corresponding NCU frame number to last Y DMAOUT address .This is dependent on 0x174 register, every time user read the 0x174 register, then should read this register. If user read 0x174 twice without no this register read in middle, User will lose one frame number information .

	CH0_DMAOUT_Y_LAST_STATS_NUM																BASE + 0x0178															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_DMAOUT_Y_LAST_STATS_NUM																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH0_DMAOUT_Y_LAST_STATS_NUM	Corresponding Frame number with last Y address of channel 0	R

3.6.2.38 Ch 0 Y Buff Last Address FIFO Status（CH0_Y_LAST_ADDR_FIFO_STA, 0x017C）

The CH0_Y_LAST_ADDR_FIFO_STA is used to indicate the status of Y last address FIFO of channel 0 .Read only

	CH0_Y_LAST_ADDR_FIFO_STA																BASE + 0x017C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					Wr_ptr			Rd_ptr			Entry			Full	Empty
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect. Read as zero.	R
10:8	Wr_ptr	write point of FIFO,0~4	R
7:5	Rd_ptr	read point of FIFO,0~4	R
4:2	Entry	valid address number,0~5	R
1	Full	FIFO Full , high valid	R
0	Empty	FIFO Empty, high valid	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.39 Ch 0 DMAOUT Y Line Stride（CH0_DMAOUT_Y_STRI, 0x0180）

The CH0_DMAOUT_Y_STRI is used to indicate the line stride of channel 0 Y data . IF output format is RGB888 , it's four times as the output width and if the output format is RGB565 , it's two times as the output width .

	CH0_DMAOUT_Y_STRI																BASE + 0x0180															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CH0_Y_STRI															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect. Read as zero.	R
15:0	CH0_Y_STRI	the line stride of channel 0 Y data, unit byte	RW

3.6.2.40 Ch 0 DMAOUT UV Buff Address（CH0_DMAOUT_UV_ADDR, 0x0184）

The CH0_DMAOUT_UV_ADDR is used to indicate the channel 0 UV data DMAOUT buffer address .8 bytes align .Write this register , MScaler will store the address in a 5 depth FIFO .(if the FIFO is full , CPU should not write anymore, user can check is status by read CH0_UV_ADDR_FIFO_STA register).DMAOUT will read the FIFO when frame start comes .CPU read data is the current address that DMAOUT is using .

	CH0_DMAOUT_UV_ADDR																BASE + 0x0184															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_DMAOUT_UV_ADDR[31:3]																													Reserved		ADDR_STATU
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	CH0_DMAOUT_UV_ADDR[31:1]	The DMAOUT address that MScaler is being used . 8 byte align	RW
2:1	Reserved	Writing has no effect. Read as zero.	R
0	ADDR_STATU	0:current frame DMAOUT finished 1:current frame is DMAOUT	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.41 Ch 0 UV Buff Address FIFO Status（CH0_UV_ADDR_FIFO_STA, 0x0188）

The CH0_UV_ADDR_FIFO_STA is used to indicate the status of UV address FIFO of channel 0.

	CH0_UV_ADDR_FIFO_STA																BASE + 0x0188															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					Wr_ptr			Rd_ptr			Entry			Full	Empty
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect. Read as zero.	R
10:8	Wr_ptr	write point of FIFO,0~4	R
7:5	Rd_ptr	read point of FIFO,0~4	R
4:2	Entry	valid address number,0~5	R
1	Full	FIFO Full , high valid	R
0	Empty	FIFO Empty, high valid	R

3.6.2.42 Ch 0 UV Buff Last Address（CH0_DMAOUT_UV_LAST_ADDR, 0x018C）

The CH0_DMAOUT_UV_LAST_ADDR is used to indicate the last DMAOUT address of channel 0 .8 byte align .Read only .User should read the FIFO status before read this register , if it is not empty ,user can get the last DMAOUT address of channel 0 UV data . If the FIFO is full , MScaler can't write anymore, the address information will lose .

	CH0_DMAOUT_UV_LAST_ADDR																BASE + 0x018C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_DMAOUT_UV_LAST_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH0_DMAOUT_UV_LAST_ADDR	Last DMAOUT address of channel 0 UV data	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.43 Ch 0 UV Buff Last Stats num（CH0_DMAOUT_UV_LAST_STATS_NUM, 0x0190）

The CH0_DMAOUT_UV_LAST_STATS_NUM is used to indicate the corresponding NCU frame number to last UV DMAOUT address .This is dependent on 0x18C register, every time user read the 0x18C register, then should read this register. If user read 0x18C twice without no this register read in middle, User will lose one frame number information .

	CH0_DMAOUT_UV_LAST_STATS_NUM																BASE + 0x0190															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH0_DMAOUT_UV_LAST_STATS_NUM																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH0_DMAOUT_UV_LAST_STATS_NUM	Corresponding Frame number with last UV address of channel 0	R

3.6.2.44 Ch 0 UV Buff Last Address FIFO Status（CH0_UV_LAST_ADDR_FIFO_STA, 0x0194）

The CH0_UV_LAST_ADDR_FIFO_STA is used to indicate the status of UV last address FIFO of channel 0 .Read only

	CH0_UV_LAST_ADDR_FIFO_STA																BASE + 0x0194															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					Wr_ptr			Rd_ptr			Entry			Full	Empty
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect. Read as zero.	R
10:8	Wr_ptr	write point of FIFO,0~4	R
7:5	Rd_ptr	read point of FIFO,0~4	R
4:2	Entry	valid address number,0~5	R
1	Full	FIFO Full , high valid	R
0	Empty	FIFO Empty, high valid	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.45 Ch 0 DMAOUT UV Line Stride（CH0_DMAOUT_UV_STRI, 0x0198）

The CH0_DMAOUT_UV_STRI is used to indicate the line stride of channel 0 UV data .8 bytes align .

	CH0_DMAOUT_UV_STRI																BASE + 0x0198															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CH0_UV_STRI															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect. Read as zero.	R
15:0	CH0_UV_STRI	the line stride of channel 0 UV data, unit pixel	RW

3.6.2.46 Ch 0 DMAOUT Y Address Buff Clear (CH0_DMAOUT_Y_ADDR_CLR,0x019C)

The CH0_DMAOUT_Y_ADDR_CLR is used to set to clear channel 0 DMAOUT Y address FIFO .

	CH0_DMAOUT_Y_ADDR_CLR																BASE + 0x019C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CH0_Y_ADDR_CLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CH0_Y_ADDR_CLR	CH0 DMAOUT Y Address FIFO clear ,write 1 clear	RW

3.6.2.47 Ch 0 DMAOUT UV Address Buff Clear (CH0_DMAOUT_UV_ADDR_CLR,0x01A0)

The CH0_DMAOUT_UV_ADDR_CLR is used to set to clear channel 0 DMAOUT UV address FIFO

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	CH0_DMAOUT_UV_ADDR_CLR																BASE + 0x01A0														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CH0_UV_ADDR_CLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CH0_UV_ADDR_CLR	CH0 DMAOUT UV Address FIFO clear ,write 1 clear	RW

3.6.2.48 Ch 0 DMAOUT Y Last Address Buff Clear (CH0_DMAOUT_Y_LAST_ADDR_CLR,0x01A4)

The CH0_DMAOUT_Y_LAST_ADDR_CLR is used to set to clear channel 0 DMAOUT Y last address FIFO

	CH0_DMAOUT_Y_LAST_ADDR_CLR																BASE + 0x01A4														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CH0_Y_LAST_ADDR_CLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CH0_Y_LAST_ADDR_CLR	CH0 DMAOUT Y Last Address FIFO clear ,write 1 clear	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.49 Ch 0 DMAOUT UV LAST Address Buff Clear (CH0_DMAOUT_UV_LAST_ADDR_CLR,0x01A8)

The CH0_DMAOUT_UV_LAST_ADDR_CLR is used to set to clear channel 0 DMAOUT UV last address FIFO

	CH0_DMAOUT_UV_LAST_ADDR_CLR																BASE + 0x01A8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CH0_UV_LAST_ADDR_CLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CH0_UV_LAST_ADDR_CLR	CH0 DMAOUT UV Last Address FIFO clear ,write 1 clear	RW

3.6.2.50 Ch 0 DMAOUT Y Address Buff Select (CH0_DMAOUT_Y_ADDR_SEL,0x01AC)

The CH0_DMAOUT_Y_ADDR_SEL is used to set to select channel 0 DMAOUT Y address from Y address FIFO or Y address register when Tiziano overflow happened . Address register is a buffer to store address read from address FIFO .

	CH0_DMAOUT_Y_ADDR_SEL																BASE + 0x01AC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CH0_Y_ADDR_SEL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	CH0_Y_ADDR_SEL	0: From address register 1: From address FIFO	RW

3.6.2.51 Ch 0 DMAOUT UV Address Buff Select (CH0_DMAOUT_UV_ADDR_SEL,0x01B0)

The CH0_DMAOUT_UV_ADDR_SEL is used to set to select channel 0 DMAOUT UV address from UV address FIFO or UV address register when Tiziano overflow happened . Address register is a buffer to store address read from address FIFO .

	CH0_DMAOUT_UV_ADDR_SEL																BASE + 0x01B0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CH0_UV_ADDR_SEL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CH0_UV_ADDR_SEL	0: From address register 1: From address FIFO	RW

3.6.2.52 Ch 0 Coe Zero Vrsz H（CH0_COE_ZERO_VRSZ_H, 0x0200）

Channel 0 vresize coe zero value.

	CH0_COE_ZERO_VRSZ_H																BASE + 0x001C0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											ch0_vrsz_zero_h																				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect. Read as zero.	R
21:0	ch0_vrsz_zero_h	channel 0 vresize zero coef hight	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.53 Ch 0 Coe Zero Vrsz L（CH0_COE_ZERO_VRSZ_L, 0x0200）

Channel 0 vresize coe zero value.

	CH0_COE_ZERO_VRSZ_L																BASE + 0x001C4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																ch0_vrsz_zero_l															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect. Read as zero.	R
21:0	ch0_vrsz_zero_l	channel 0 vresize zero coef low	RW

3.6.2.54 Ch 0 Coe Zero Hrsz H（CH0_COE_ZERO_VRSZ_H, 0x0200）

Channel 0 hresize coe zero value.

	CH0_COE_ZERO_HRSZ_H																BASE + 0x001C8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																ch0_hrsz_zero_h															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect. Read as zero.	R
21:0	ch0_hrsz_zero_h	channel 0 hresize zero coef hight	RW

3.6.2.55 Ch 0 Coe Zero Hrsz L（CH0_COE_ZERO_HRSZ_L, 0x0200）

Channel 0 hresize coe zero value.

	CH0_COE_ZERO_HRSZ_L																BASE + 0x001CC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																ch0_hrsz_zero_l															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect. Read as zero.	R
21:0	ch0_hrsz_zero_l	channel 0 hresize zero coef low	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.56 Ch 0 Coe Oft（CH0_COE_OFT, 0x0200）

Channel 0 resize coe oft.

	CH0_COE_OFT																BASE + 0x001D0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								ch0_coe_oft_hrsz								Reserved								ch0_coe_oft_vrsz							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect. Read as zero.	R
24:16	ch0_coe_oft_hrsz	channel 0 coe oft for hresize	RW
15:9	Reserved	Writing has no effect. Read as zero.	R
8:0	ch0_coe_oft_vrsz	channel 0 coe oft for vresize	RW

3.6.2.57 Ch 1 Resize Out Image Size（CH1_RSZ_OSIZE, 0x0200）

Channel 1 scale output image size, both the width and the height should be even number. This is not the DMAOUT image size.

	CH1_RSZ_OSIZE																BASE + 0x00200															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_RSZ_OW																CH1_RSZ_OH															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH1_RSZ_OW	The width resize scale step of channel 1	RW
15:0	CH1_RSZ_OH	The height resize scale step of channel 1	RW

3.6.2.58 Ch 1 Resize Step Register（CH1_RSZ_STEP, 0x0204）

The CH1_RSZ_STEP is used to indicate the scale step of Channel 1, the CH1_STEP_W value equals floor(SRC_W/CH1_RSZ_OW * 512), the CH1_STEP_H value equals floor(SRC_H/CH1_RSZ_OH * 512).

	CH1_RSZ_STEP																BASE + 0x0204															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_STEP_W																CH1_STEP_H															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:16	CH1_STEP_W	The width resize scale step of channel 1	RW
15:0	CH1_STEP_H	The height resize scale step of channel 1	RW

3.6.2.59 Ch 1 Y HResize Coef Write（CH1_Y_HRSZ_COEF_WR, 0x0208）

The CH1_Y_HRSZ_COEF_WR register is used to indicate the interpolation coefficient for channel 1 Y horizontal resize.

	CH1_Y_HRSZ_COEF_WR																															BASE + 0x0208
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WR_FINISH	HIGH_BIT	WADDR														WDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	WR_FINISH	RAM write finish	RW
30	HIGH_BIT	1：Write to the high 22 bits of RAM address 0：Write to the low 22 bits of RAM address	RW
29:22	WADDR	Write RAM address	RW
21:0	WDATA	Write RAM value	RW

3.6.2.60 Ch 1 Y HResize Coef Read（CH1_Y_HRSZ_COEF_RD, 0x020C）

The CH1_Y_HRSZ_COEF_RD register is used to read the interpolation coefficient for channel 1 Y horizontal resize.

	CH1_Y_HRSZ_COEF_RD																															BASE + 0x020C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDATA_VALID	HIGH_BIT	RADDR														RDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	RDATA_VALID	RDATA valid 1:valid 0 :invalid	R
30	HIGH_BIT	1：read high 22 bits of the RAM address 0：read low 22 bits of the RAM address	RW
29:22	RADDR	The read RAM address	RW
21:0	RDATA	The read data	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.61 Ch 1 Y VResize Coef Write（CH1_Y_VRSZ_COEF_WR, 0x0210）

The CH1_Y_VRSZ_COEF_WR register is used to indicate the interpolation coefficient for channel 1 Y vertical resize.

	CH1_Y_VRSZ_COEF_WR																BASE + 0x0210															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WR_FINISH	HIGH_BIT	WADDR														WDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	WR_FINISH	RAM write finish	RW
30	HIGH_BIT	1：Write to the high 22 bits of RAM address 0：Write to the low 22 bits of RAM address	RW
29:22	WADDR	Write RAM address	RW
21:0	WDATA	Write RAM value	RW

3.6.2.62 Ch 1 Y VResize Coef Read（CH1_Y_VRSZ_COEF_RD, 0x0214）

The CH1_Y_VRSZ_COEF_RD register is used to read the interpolation coefficient for channel 1 Y vertical resize.

	CH1_Y_VRSZ_COEF_RD																BASE + 0x0214															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDATA_VALID	HIGH_BIT	RADDR														RDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	RDATA_VALID	RDATA valid 1:valid 0 :invalid	R
30	HIGH_BIT	1：read high 22 bits of the RAM address 0：read low 22 bits of the RAM address	RW
29:22	RADDR	The read RAM address	RW
21:0	RDATA	The read data	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.63 Ch 1 UV HResize Coef Write（CH1_UV_HRSZ_COEF_WR, 0x0218）

The CH1_UV_HRSZ_COEF_WR register is used to indicate the interpolation coefficient for channel 1 UV horizontal resize.

	CH1_UV_HRSZ_COEF_WR																BASE + 0x0218															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WR_FINISH	HIGH_BIT	WADDR														WDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	WR_FINISH	RAM write finish	RW
30	HIGH_BIT	1：Write to the high 22 bits of RAM address 0：Write to the low 22 bits of RAM address	RW
29:22	WADDR	Write RAM address	RW
21:0	WDATA	Write RAM value	RW

3.6.2.64 Ch 1 UV HResize Coef Read（CH1_UV_HRSZ_COEF_RD, 0x021C）

The CH1_UV_HRSZ_COEF_RD register is used to read the interpolation coefficient for channel 1 UV horizontal resize.

	CH1_UV_HRSZ_COEF_RD																BASE + 0x021C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDATA_VALID	HIGH_BIT	RADDR														RDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	RDATA_VALID	RDATA valid 1:valid 0 :invalid	R
30	HIGH_BIT	1：read high 22 bits of the RAM address 0：read low 22 bits of the RAM address	RW
29:22	RADDR	The read RAM address	RW
21:0	RDATA	The read data	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.65 Ch 1 UV VResize Coef Write（CH1_UV_VRSZ_COEF_WR, 0x0220）

The CH1_UV_VRSZ_COEF_WR register is used to indicate the interpolation coefficient for channel 1 UV vertical resize.

	CH1_UV_VRSZ_COEF_WR																BASE + 0x0220															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WR_FINISH	HIGH_BIT	WADDR														WDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	WR_FINISH	RAM write finish	RW
30	HIGH_BIT	1：Write to the high 22 bits of RAM address 0：Write to the low 22 bits of RAM address	RW
29:22	WADDR	Write RAM address	RW
21:0	WDATA	Write RAM value	RW

3.6.2.66 Ch 1 UV VResize Coef Read（CH1_UV_VRSZ_COEF_RD, 0x0224）

The CH1_UV_VRSZ_COEF_RD register is used to read the interpolation coefficient for channel 1 UV vertical resize.

	CH1_UV_VRSZ_COEF_RD																BASE + 0x0224															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDATA_VALID	HIGH_BIT	RADDR														RDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	RDATA_VALID	RDATA valid 1:valid 0 :invalid	R
30	HIGH_BIT	1：read high 22 bits of the RAM address 0：read low 22 bits of the RAM address	RW
29:22	RADDR	The read RAM address	RW
21:0	RDATA	The read data	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.67 Ch 1 Crop Out Image Position（CH1_CROP_OPOS, 0x0228）

The CH1_CROP_OPOS is used to indicate the crop start point after scale, both the X-axis and the Y-axis should be even number .

	CH1_CROP_OPOS																BASE + 0x0228															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_CROP_OX																CH1_CROP_OY															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH1_CROP_OX	Crop upper-left point X-axis position of channel 1 crop output image .	RW
15:0	CH1_CROP_OY	Crop upper-left point Y-axis position of channel 1 crop output image .	RW

3.6.2.68 Ch 1 Crop Out Image Size（CH1_CROP_OSIZE, 0x022C）

The CH1_CROP_OSIZE is used to indicate the Channel 1 Crop output image size, both the width and the height should be even number . This size is the channel 1 final output size.

	CH1_CROP_OSIZE																BASE + 0x022C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_CROP_OW																CH1_CROP_OH															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH1_CROP_OW	The width of channel 1 crop output image , unit pixel	RW
15:0	CH1_CROP_OH	The height of channel 1 crop output image , unit pixel	RW

3.6.2.69 Ch 1 Frame Rate Ctrl Loop(CH1_FR_CTRL_LOOP, 0x0230)

The CH1_FR_CTRL_LOOP is used to indicate the maximum number of frame rate control loop number. For example the number is N, it means that it will take the bit 0 to bit N(N+1 in total) from CH1_FR_CTRL_MASK to do frame rate control . Maximum number is 31.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	CH1_FR_CTRL_LOOP																BASE + 0x0230																	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											CH1_FR_CTRL_LOOP				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect. Read as zero.	R
4:0	CH1_FR_CTRL_LOOP	Maximum: 31, Minimum:0	RW

3.6.2.70 Ch 1 Frame Rate Ctrl Mask(CH1_FR_CTRL_MASK, 0x0234)

The CH1_FR_CTRL_MASK is used to indicate which frames should be kept and which frames should be dropped .The corresponding bit is 1 means kept , 0 means dropped .The valid bits of this register is from bit 0 to bit CH1_FR_CTRL_LOOP.

	CH1_FR_CTRL_MASK																BASE + 0x0234																	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_FR_CTRL_MASK																																	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:0	CH1_FR_CTRL_MASK	the valid bits of CH1_FR_CTRL_MASK is [CH1_FR_CTRL_LOOP:0]	RW

Note： The CH1_FR_CTRL_MASK should be better configured after CH1_FR_CTRL_LOOP .

3.6.2.71 Ch 1 Mask0 Pos Register（CH1_MS0_POS, 0x0238）

The CH1_MS0_POS is used to indicate the mask start point of the area 0 of channel 1 after scale, both the X-axis and the Y-axis should be even number .

	CH1_MS0_POS																BASE + 0x0238																	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_MS0_POS_X																CH1_MS0_POS_Y																	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:16	CH1_MS0_POS_X	The X-axis of channel 1 mask area 0	RW
15:0	CH1_MS0_POS_Y	The Y-axis of channel 1 mask area 0	RW

3.6.2.72 Ch 1 Mask0 Size Register（CH1_MS0_SIZE, 0x023C）

The CH1_MS0_SIZE is used to indicate the mask size of the area 0 of channel 1 after scale, both the width and the height should be even number.

	CH1_MS0_SIZE																BASE + 0x023C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_MS0_SIZE_X																CH1_MS0_SIZE_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH1_MS0_SIZE_X	The Width of channel 1 mask area 0	RW
15:0	CH1_MS0_SIZE_Y	The Height of channel 1 mask area 0	RW

3.6.2.73 Ch 1 Mask0 Value Register（CH1_MS0_VALUE, 0x0240）

The CH1_MS0_VALUE is used to indicate the value of the mask area 0 of channel 1.

	CH1_MS0_VALUE																BASE + 0x0240															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_MS0_VALUE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH1_MS0_VALUE	When CH1_MASK_EN =1, if the pixel located in Mask0 ,channel 0 will output this ARGB values for Mask function. If output picture format is ARGB/RGB, this data sequence of this register is also ARGB/RGB. If background picture format is NV12/NV21, then the data sequence of this register is AYVU/AYUV	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Note:

1. Mask function has a priority to decide what value should output when the pixel located in overlapping mask area. Mask0 has the highest priority .
2.When output type is ARGB/RGB, the 32 bits mask value should set with the same order as output type ,for example ,if output is RBGA, the mask value is also should be RBGA .
3.When output type is RGB565, the 32 bits mask value should set as RGBRGB.

3.6.2.74 Ch 1 Mask1 Pos Register（CH1_MS1_POS, 0x0244）

The CH1_MS1_POS is used to indicate the mask start point of the area 1 of channel 1 after scale, both the X-axis and the Y-axis should be even number.

	CH1_MS1_POS																BASE + 0x0244															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_MS1_POS_X																CH1_MS1_POS_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH1_MS1_POS_X	The X-axis of channel 1 mask area 1	RW
15:0	CH1_MS1_POS_Y	The Y-axis of channel 1 mask area 1	RW

3.6.2.75 Ch 1 Mask1 Size Register（CH1_MS1_SIZE, 0x0248）

The CH1_MS1_SIZE is used to indicate the mask size of the area 1 of channel 1 after scale, both the width and the height should be even number.

	CH1_MS1_SIZE																BASE + 0x0248															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_MS1_SIZE_X																CH1_MS1_SIZE_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH1_MS1_SIZE_X	The Width of channel 1 mask area 1	RW
15:0	CH1_MS1_SIZE_Y	The Height of channel 1 mask area 1	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.76 Ch 1 Mask1 Value Register（CH1_MS1_VALUE, 0x024C）

The CH1_MS1_VALUE is used to indicate the value of the mask area 1 of channel 1.

	CH1_MS1_VALUE																BASE + 0x024C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_MS1_VALUE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH1_MS1_VALUE	When CH1_MASK_EN =1, if the pixel located in Mask0 ,channel 0 will output this ARGB values for Mask function. If output picture format is ARGB/RGB, this data sequence of this register is also ARGB/RGB. If background picture format is NV12/NV21, then the data sequence of this register is AYVU/AYUV	RW

Note:

1. Mask function has a priority to decide what value should output when the pixel located in over
2.When output type is ARGB/RGB, the 32 bits mask value should set with the same order as output type ,for example ,if output is RBGA, the mask value is also should be RBGA .
3.When output type is RGB565, the 32 bits mask value should set as RGBRGB.

3.6.2.77 Ch 1 Mask2 Pos Register（CH1_MS2_POS, 0x0250）

The CH1_MS2_POS is used to indicate the mask start point of the area 2 of channel 1 after scale, both the X-axis and the Y-axis should be even number.

	CH1_MS2_POS																BASE + 0x0250															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_MS2_POS_X																CH1_MS2_POS_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH1_MS2_POS_X	The X-axis of channel 1 mask area 2	RW
15:0	CH1_MS2_POS_Y	The Y-axis of channel 1 mask area 2	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.78 Ch 1 Mask2 Size Register（CH1_MS2_SIZE, 0x0254）

The CH1_MS2_SIZE is used to indicate the mask size of the area 2 of channel 1 after scale, both the width and the height should be even number.

	CH1_MS2_SIZE																BASE + 0x0254															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_MS2_SIZE_X																CH1_MS2_SIZE_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH1_MS2_SIZE_X	The Width of channel 1 mask area 2	RW
15:0	CH1_MS2_SIZE_Y	The Height of channel 1 mask area 2	RW

3.6.2.79 Ch 1 Mask2 Value Register（CH1_MS2_VALUE, 0x0258）

The CH1_MS2_VALUE is used to indicate the value of the mask area 2 of channel 1.

	CH1_MS2_VALUE																BASE + 0x0258															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_MS2_VALUE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH1_MS2_VALUE	When CH1_MASK_EN =1, if the pixel located in Mask0 ,channel 0 will output this ARGB values for Mask function. If output picture format is ARGB/RGB, this data sequence of this register is also ARGB/RGB. If background picture format is NV12/NV21, then the data sequence of this register is AYVU/AYUV	RW

Note:

1. Mask function has a priority to decide what value should output when the pixel located in over
2.When output type is ARGB/RGB, the 32 bits mask value should set with the same order as output type ,for example ,if output is RBGA, the mask value is also should be RBGA .
3.When output type is RGB565, the 32 bits mask value should set as RGBRGB.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.80 Ch 1 Mask3 Pos Register（CH1_MS3_POS, 0x025C）

The CH1_MS3_POS is used to indicate the mask start point of the area 3 of channel 1 after scale, both the X-axis and the Y-axis should be even number.

	CH1_MS3_POS																BASE + 0x025C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_MS3_POS_X																CH1_MS3_POS_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH1_MS3_POS_X	The X-axis of channel 1 mask area 3	RW
15:0	CH1_MS3_POS_Y	The Y-axis of channel 1 mask area 3	RW

3.6.2.81 Ch 1 Mask3 Size Register（CH1_MS3_SIZE, 0x0260）

The CH1_MS3_SIZE is used to indicate the mask size of the area 3 of channel 1 after scale, both the width and the height should be even number.

	CH1_MS3_SIZE																BASE + 0x0260															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_MS3_SIZE_X																CH1_MS3_SIZE_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH1_MS3_SIZE_X	The Width of channel 1 mask area 3	RW
15:0	CH1_MS3_SIZE_Y	The Height of channel 1 mask area 3	RW

3.6.2.82 Ch 1 Mask3 Value Register（CH1_MS3_VALUE, 0x0264）

The CH1_MS3_VALUE is used to indicate the value of the mask area 3 of channel 1.

	CH1_MS3_VALUE																BASE + 0x0264															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_MS3_VALUE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	CH1_MS3_VALUE	When CH1_MASK_EN =1, if the pixel located in Mask0 ,channel 0 will output this ARGB values for Mask function. If output picture format is ARGB/RGB, this data sequence of this register is also ARGB/RGB. If background picture format is NV12/NV21, then the data sequence of this register is AYVU/AYUV	RW

Note: 1. Mask function has a priority to decide what value should output when the pixel located in over

2.When output type is ARGB/RGB, the 32 bits mask value should set with the same order as output type ,for example ,if output is RBGA, the mask value is also should be RBGA .

3.When output type is RGB565, the 32 bits mask value should set as RGBRGB.

3.6.2.83 Ch 1 Out Data Format Register（CH1_OUT_FMT, 0x0268）

The CH1_OUT_FMT is used to indicate the Channel 1 output format . There is only one channel can do CSC transfer , so there is only one channel can set ARGB/RGB type output , the other two channels should configure as NV12/NV21.If there are more than one channel set as ARGB/RGB output, the MScaler will get a highest priority for channel 0 and the lowest priority for channel 2 to output ARGB/RGB. The lower priority channels will has a error occurred . So make sure less than two channels are set as ARGB/RGB output format .

	CH1_OUT_FMT																BASE + 0x0268													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									Y_OUT_ONLY	RGB_ORDER				OUT_FMT	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect. Read as zero.	R
6	Y_OUT_ONLY	1:DMAOUT Y DATA ONLY 0:BOTH Y AND UV DATA DMAOUT	RW
5:2	RGB_ORDER	ARGB order. 4'b0000: BGRA 4'b0001: GBRA 4'b0010: RBGA 4'b0011: BRGA 4'b0100: GRBA 4'b0101: RGBA 4'b1000: ABGR 4'b1001: AGBR 4'b1010: ARBG 4'b1011: ABRG 4'b1100: AGRB 4'b1101: ARGB RGB565 0:BGR 1:GBR 2:RBG 3:BRG 4:GRB 5:RGB	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

1:0	OUT_FMT	00:NV12 01:NV21 02:ARGB888 03: RGB565	RW

3.6.2.84 Ch 1 DMAOUT Y Buff Address（CH1_DMAOUT_Y_ADDR, 0x026C）

The CH1_DMAOUT_Y_ADDR is used to indicate the channel 1 Y data DMAOUT buffer address .8 bytes align .Write this register , MScaler will store the address in a 5 depth FIFO .(if the FIFO is full , CPU should not write anymore, user can check is status by read CH1_Y_ADDR_FIFO_STA register).

DMAOUT will read the FIFO when frame start comes .CPU read data is the current address that DMAOUT is using .

	CH1_DMAOUT_Y_ADDR																BASE + 0x026C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_DMAOUT_Y_ADDR[31:3]																													Reserved		ADDR_STATU
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	CH1_DMAOUT_Y_ADDR[31:3]	The DMAOUT address that MScaler is being used . 8 byte align	RW
2:1	Reserved	Writing has no effect. Read as zero.	R
0	ADDR_STATU	0:current frame DMAOUT finished 1:current frame is DMAOUT	R

3.6.2.85 Ch 1 Y Buff Address FIFO Status（CH1_Y_ADDR_FIFO_STA, 0x0270）

The CH1_Y_ADDR_FIFO_STA is used to indicate the status of Y address FIFO of channel 1 .

	CH1_Y_ADDR_FIFO_STA																BASE + 0x0270															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					Wr_ptr			Rd_ptr			Entry			Full	Empty
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect. Read as zero.	R
10:8	Wr_ptr	write point of FIFO,0~4	R
7:5	Rd_ptr	read point of FIFO,0~4	R
4:2	Entry	valid address number,0~5	R
1	Full	FIFO Full , high valid	R
0	Empty	FIFO Empty, high valid	R

3.6.2.86 Ch 1 Y Buff Last Address（CH1_DMAOUT_Y_LAST_ADDR, 0x0274）

The CH1_DMAOUT_Y_LAST_ADDR is used to indicate the last DMAOUT address of channel 0 .8 byte align .Read only .User should read the FIFO status before read this register , if it is not empty ,user can get the last DMAOUT address of channel 1 Y data . If the FIFO is full , MScaler can't write anymore, the address information will lose .

	CH1_DMAOUT_Y_LAST_ADDR																BASE + 0x0274															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_DMAOUT_Y_LAST_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH0_DMAOUT_Y_LAST_ADDR	Last DMAOUT address of channel 1 Y data	R

3.6.2.87 Ch 1 Y Buff Last Stats Num（CH1_DMAOUT_Y_LAST_STATS_NUM, 0x0278）

The CH1_DMAOUT_Y_LAST_STATS_NUM is used to indicate the corresponding NCU frame number to last Y DMAOUT address .This is dependent on 0x274 register, every time user read the 0x274 register, then should read this register. If user read 0x274 twice without no this register read in middle, User will lose one frame number information .

	CH1_DMAOUT_Y_LAST_STATS_NUM																BASE + 0x0278															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_DMAOUT_Y_LAST_STATS_NUM																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	CH1_DMAOUT_Y_LAST_STATS_NUM	Corresponding Frame number with last Y address of channel 1	R

3.6.2.88 Ch 1 Y Buff Last Address FIFO Status（CH1_Y_LAST_ADDR_FIFO_STA, 0x027C）

The CH1_Y_LAST_ADDR_FIFO_STA is used to indicate the status of Y last address FIFO of channel 1.Read only

	CH1_Y_LAST_ADDR_FIFO_STA																														
																	BASE + 0x027C														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					Wr_ptr			Rd_ptr			Entry			Full	Empty
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect. Read as zero.	R
10:8	Wr_ptr	write point of FIFO,0~4	R
7:5	Rd_ptr	read point of FIFO,0~4	R
4:2	Entry	valid address number,0~5	R
1	Full	FIFO Full , high valid	R
0	Empty	FIFO Empty, high valid	R

3.6.2.89 Ch 1 DMAOUT Y Line Stride（CH1_DMAOUT_Y_STRI, 0x0280）

The CH1_DMAOUT_Y_STRI is used to indicate the line stride of channel 1 Y data . IF output format is RGB888 , it's four times as the output width and if the output format is RGB565 , it's two times as the output width .

	CH1_DMAOUT_Y_STRI																														
																	BASE + 0x0280														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CH1_Y_STRI															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect. Read as zero.	R
15:0	CH1_Y_STRI	the line stride of channel 1 Y data, unit byte	RW

3.6.2.90 Ch 1 DMAOUT UV Buff Address（CH1_DMAOUT_UV_ADDR, 0x0284）

The CH1_DMAOUT_UV_ADDR is used to indicate the channel 1 UV data DMAOUT buffer address .8 byte align .Write this register , MScaler will store the address in a 5 depth FIFO .(if the FIFO is full , CPU should not write anymore, user can check is status by read CH1_UV_ADDR_FIFO_STA register).DMAOUT will read the FIFO when frame start comes .CPU read data is the current address that DMAOUT is used .

	CH1_DMAOUT_UV_ADDR																BASE + 0x0284															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_DMAOUT_UV_ADDR[31:3]																													Reserved		ADDR_STATU
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	CH1_DMAOUT_UV_ADDR[31:1]	The DMAOUT address that MScaler is being used . 8 byte align	RW
2:1	Reserved	Writing has no effect. Read as zero.	R
0	ADDR_STATU	0:current frame DMAOUT finished 1:current frame is DMAOUT	R

3.6.2.91 Ch 1 UV Buff Address FIFO Status（CH1_UV_ADDR_FIFO_STA, 0x0288）

The CH1_UV_ADDR_FIFO_STA is used to indicate the status of UV address FIFO of channel 1.

	CH1_UV_ADDR_FIFO_STA																BASE + 0x0288															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					Wr_ptr			Rd_ptr			Entry			Full	Empty
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect. Read as zero.	R
10:8	Wr_ptr	write point of FIFO,0~4	R
7:5	Rd_ptr	read point of FIFO,0~4	R
4:2	Entry	valid address number,0~5	R
1	Full	FIFO Full , high valid	R
0	Empty	FIFO Empty, high valid	R

3.6.2.92 Ch 1 UV Buff Last Address（CH1_DMAOUT_UV_LAST_ADDR, 0x028C）

The CH1_DMAOUT_UV_LAST_ADDR is used to indicate the last DMAOUT address of channel 1 .8 byte align .Read only .User should read the FIFO status before read this register , if it is not empty ,user can get the last DMAOUT address of channel 1 UV data . If the FIFO is full , MScaler can't write anymore, the address information will lose .

	CH1_DMAOUT_UV_LAST_ADDR																BASE + 0x028C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_DMAOUT_UV_LAST_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH1_DMAOUT_UV_LAST_ADDR	Last DMAOUT address of channel 1 UV data	R

3.6.2.93 Ch 1 UV Buff Last Stats num（CH1_DMAOUT_UV_LAST_STATS_NUM, 0x0290）

The CH1_DMAOUT_UV_LAST_STATS_NUM is used to indicate the corresponding NCU frame number to last UV DMAOUT address .This is dependent on 0x28C register, every time user read the 0x28C register, then should read this register. If user read 0x28C twice without no this register read in middle, User will lose one frame number information .

	CH1_DMAOUT_UV_LAST_STATS_NUM																BASE + 0x0290															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH1_DMAOUT_UV_LAST_STATS_NUM																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	CH1_DMAOUT_UV_LAST_STATS_NUM	Corresponding Frame number with last UV address of channel 1	R

3.6.2.94 Ch 1 UV Buff Last Address FIFO Status（CH1_UV_LAST_ADDR_FIFO_STA, 0x0294）

The CH1_UV_LAST_ADDR_FIFO_STA is used to indicate the status of UV last address FIFO of channel 0 .Read only

	CH1_UV_LAST_ADDR_FIFO_STA																														
																	BASE + 0x0294														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					Wr_ptr			Rd_ptr			Entry			Full	Empty
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect. Read as zero.	R
10:8	Wr_ptr	write point of FIFO,0~4	R
7:5	Rd_ptr	read point of FIFO,0~4	R
4:2	Entry	valid address number,0~5	R
1	Full	FIFO Full , high valid	R
0	Empty	FIFO Empty, high valid	R

3.6.2.95 Ch 1 DMAOUT UV Line Stride（CH1_DMAOUT_UV_STRI, 0x0298）

The CH1_DMAOUT_UV_STRI is used to indicate the line stride of channel 1 UV data .8 bytes align .

	CH1_DMAOUT_UV_STRI																														
																	BASE + 0x0298														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CH1_UV_STRI															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect. Read as zero.	R
15:0	CH1_UV_STRI	the line stride of channel 1 UV data, unit pixel	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.96 Ch 1 DMAOUT Y Address Buff Clear (CH1_DMAOUT_Y_ADDR_CLR,0x029C)

The CH1_DMAOUT_Y_ADDR_CLR is used to set to clear channel 1 DMAOUT Y address FIFO .

	CH1_DMAOUT_Y_ADDR_CLR																BASE + 0x029C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CH1_Y_ADDR_CLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CH1_Y_ADDR_CLR	CH1 DMAOUT Y Address FIFO clear ,write 1 clear	RW

3.6.2.97 Ch 1 DMAOUT UV Address Buff Clear (CH1_DMAOUT_UV_ADDR_CLR,0x02A0)

The CH1_DMAOUT_UV_ADDR_CLR is used to set to clear channel 1 DMAOUT UV address FIFO

	CH1_DMAOUT_UV_ADDR_CLR																BASE + 0x02A0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CH1_UV_ADDR_CLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CH1_UV_ADDR_CLR	CH1 DMAOUT UV Address FIFO clear ,write 1 clear	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.98 Ch 1 DMAOUT Y Last Address Buff Clear (CH1_DMAOUT_Y_LAST_ADDR_CLR,0x02A4)

The CH1_DMAOUT_Y_LAST_ADDR_CLR is used to set to clear channel 1 DMAOUT Y last address FIFO

	CH1_DMAOUT_Y_LAST_ADDR_CLR																															BASE + 0x02A4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CH1_Y_LAST_ADDR_CLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CH1_Y_LAST_ADDR_CLR	CH1 DMAOUT Y Last Address FIFO clear ,write 1 clear	RW

3.6.2.99 Ch 1 DMAOUT UV LAST Address Buff Clear (CH1_DMAOUT_UV_LAST_ADDR_CLR,0x02A8)

The CH1_DMAOUT_UV_LAST_ADDR_CLR is used to set to clear channel 1 DMAOUT UV last address FIFO

	CH1_DMAOUT_Y_LAST_ADDR_CLR																															BASE + 0x02A8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CH1_UV_LAST_ADDR_CLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	CH1_UV_LAST_ADDR_CLR	CH1 DMAOUT UV Last Address FIFO clear ,write 1 clear	RW

3.6.2.100 Ch 1 DMAOUT Y Address Buff Select (CH1_DMAOUT_Y_ADDR_SEL,0x02AC)

The CH1_DMAOUT_Y_ADDR_SEL is used to set to select channel 1 DMAOUT Y address from Y address FIFO or Y address register when Tiziano overflow happened . Address register is a buffer to store address read from address FIFO .

	CH1_DMAOUT_Y_ADDR_SEL																BASE + 0x02AC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2		0
	Reserved																															CH1_Y_ADDR_SEL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CH1_Y_ADDR_SEL	0: From address register 1: From address FIFO	RW

3.6.2.101 Ch 1 DMAOUT UV Address Buff Select (CH1_DMAOUT_UV_ADDR_SEL,0x02B0)

The CH1_DMAOUT_UV_ADDR_SEL is used to set to select channel 1 DMAOUT UV address from UV address FIFO or UV address register when Tiziano overflow happened . Address register is a buffer to store address read from address FIFO .

	CH1_DMAOUT_UV_ADDR_SEL																BASE + 0x02B0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2		0
	Reserved																															CH1_UV_ADDR_SEL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CH1_UV_ADDR_SEL	0: From address register 1: From address FIFO	RW

3.6.2.102 Ch 1 Coe Zero Vrsz H（CH1_COE_ZERO_VRSZ_H, 0x01C0）

Channel 1 vresize coe zero value.

	CH1_COE_ZERO_VRSZ_H																BASE + 0x001C0														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																ch1_vrsz_zero_h															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect. Read as zero.	R
21:0	ch1_vrsz_zero_h	channel 1 vresize zero coef hight	RW

3.6.2.103 Ch 1 Coe Zero Vrsz L（CH1_COE_ZERO_VRSZ_L, 0x01C4）

Channel 1 vresize coe zero value.

	CH1_COE_ZERO_VRSZ_L																BASE + 0x001C4														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																ch1_vrsz_zero_l															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect. Read as zero.	R
21:0	ch1_vrsz_zero_l	channel 1 vresize zero coef low	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.104 Ch 1 Coe Zero Hrsz H（CH1_COE_ZERO_VRSZ_H, 0x01C8）

Channel 1 hresize coe zero value.

	CH1_COE_ZERO_HRSZ_H																BASE + 0x001C8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																ch1_hrsz_zero_h															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect. Read as zero.	R
21:0	ch1_hrsz_zero_h	channel 1 hresize zero coef hight	RW

3.6.2.105 Ch 1 Coe Zero Hrsz L（CH1_COE_ZERO_HRSZ_L, 0x01CC）

Channel 1 hresize coe zero value.

	CH1_COE_ZERO_HRSZ_L																BASE + 0x001CC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																ch1_hrsz_zero_l															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect. Read as zero.	R
21:0	ch1_hrsz_zero_l	channel 1 hresize zero coef low	RW

3.6.2.106 Ch 1 Coe Oft（CH1_COE_OFT, 0x01D0）

Channel 1 resize coe oft.

	CH1_COE_OFT																BASE + 0x001D0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												ch1_coe_oft_hrsz				Reserved								ch1_coe_oft_vrsz							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect. Read as zero.	R
24:16	ch1_coe_oft_hrsz	channel 1 coe oft for hresize	RW
15:9	Reserved	Writing has no effect. Read as zero.	R
8:0	ch1_coe_oft_vrsz	channel 1 coe oft for vresize	RW

3.6.2.107 Ch 2 Resize Out Image Size（CH2_RSZ_OSIZE, 0x0300）

Channel 2 scale output image size, both the width and the height should be even number. This is not the DMAOUT image size.

	CH2_RSZ_OSIZE																BASE + 0x0300															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_RSZ_OW																CH2_RSZ_OH															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH2_RSZ_OW	The width of the channel 2 resize out frame (unit: pixel)	RW
15:0	CH2_RSZ_OH	The height of the channel 2 resize out frame (unit: pixel)	RW

3.6.2.108 Ch 2 Resize Step Register（CH2_RSZ_STEP, 0x0304）

The CH2_RSZ_STEP is used to indicate the scale step of Channel 2, the CH2_STEP_W value equals floor(SRC_W/CH2_RSZ_OW * 512), the CH2_STEP_H value equals floor(SRC_H/CH2_RSZ_OH * 512).

	CH2_RSZ_STEP																BASE + 0x0304															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_STEP_W																CH2_STEP_H															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH2_STEP_W	The width resize scale step of channel 2	RW
15:0	CH2_STEP_H	The height resize scale step of channel 2	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.109 Ch 2 Y HResize Coef Write（CH2_Y_HRSZ_COEF_WR, 0x0308）

The CH2_Y_HRSZ_COEF_WR register is used to indicate the interpolation coefficient for channel 2 Y horizontal resize .

	CH2_Y_HRSZ_COEF_WR																															BASE + 0x0308
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WR_FINISH	HIGH_BIT	WADDR								WDATA																					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	WR_FINISH	RAM write finish	RW
30	HIGH_BIT	1：Write to the high 22 bits of RAM address 0：Write to the low 22 bits of RAM address	RW
29:22	WADDR	Write RAM address	RW
21:0	WDATA	Write RAM value	RW

3.6.2.110 Ch 2 Y HResize Coef Read（CH2_Y_HRSZ_COEF_RD, 0x030C）

The CH2_Y_HRSZ_COEF_RD register is used to read the interpolation coefficient for channel 2 Y horizontal resize .

	CH2_Y_HRSZ_COEF_RD																															BASE + 0x030C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDATA_VALID	HIGH_BIT	RADDR								RDATA																					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	RDATA_VALID	RDATA valid 1:valid 0 :invalid	R
30	HIGH_BIT	1：read high 22 bits of the RAM address 0：read low 22 bits of the RAM address	RW
29:22	RADDR	The read RAM address	RW
21:0	RDATA	The read data	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.111 Ch 2 Y VResize Coef Write（CH2_Y_VRSZ_COEF_WR, 0x0310）

The CH2_Y_VRSZ_COEF_WR register is used to indicate the interpolation coefficient for channel 2 Y vertical resize .

	CH2_Y_VRSZ_COEF_WR																BASE + 0x0310															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WR_FINISH	HIGH_BIT	WADDR														WDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	WR_FINISH	RAM write finish	RW
30	HIGH_BIT	1：Write to the high 22 bits of RAM address 0：Write to the low 22 bits of RAM address	RW
29:22	WADDR	Write RAM address	RW
21:0	WDATA	Write RAM value	RW

3.6.2.112 Ch 2 Y VResize Coef Read（CH2_Y_VRSZ_COEF_RD, 0x0314）

The CH2_Y_VRSZ_COEF_RD register is used to read the interpolation coefficient for channel 2 Y vertical resize .

	CH2_Y_VRSZ_COEF_RD																BASE + 0x0314															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDATA_VALID	HIGH_BIT	RADDR														RDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	RDATA_VALID	RDATA valid 1:valid 0 :invalid	R
30	HIGH_BIT	1：read high 22 bits of the RAM address 0：read low 22 bits of the RAM address	RW
29:22	RADDR	The read RAM address	RW
21:0	RDATA	The read data	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.113 Ch 2 UV HResize Coef Write（CH2_UV_HRSZ_COEF_WR, 0x0318）

The CH2_UV_HRSZ_COEF_WR register is used to indicate the interpolation coefficient for channel 2 UV horizontal resize .

	CH2_UV_HRSZ_COEF_WR																BASE + 0x0318															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WR_FINISH	HIGH_BIT	WADDR														WDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	WR_FINISH	RAM write finish	RW
30	HIGH_BIT	1：Write to the high 22 bits of RAM address 0：Write to the low 22 bits of RAM address	RW
29:22	WADDR	Write RAM address	RW
21:0	WDATA	Write RAM value	RW

3.6.2.114 Ch 2 UV HResize Coef Read（CH2_UV_HRSZ_COEF_RD, 0x031C）

The CH2_UV_HRSZ_COEF_RD register is used to read the interpolation coefficient for channel 2 UV horizontal resize .

	CH2_UV_HRSZ_COEF_RD																BASE + 0x031C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDATA_VALID	HIGH_BIT	RADDR														RDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	RDATA_VALID	RDATA valid 1:valid 0 :invalid	R
30	HIGH_BIT	1：read high 22 bits of the RAM address 0：read low 22 bits of the RAM address	RW
29:22	RADDR	The read RAM address	RW
21:0	RDATA	The read data	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.115 Ch 2 UV VResize Coef Write（CH2_UV_VRSZ_COEF_WR, 0x0320）

The CH2_UV_VRSZ_COEF_WR register is used to indicate the interpolation coefficient for channel 2 UV vertical resize .

	CH2_UV_VRSZ_COEF_WR																BASE + 0x0320															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WR_FINISH	HIGH_BIT	WADDR														WDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	WR_FINISH	RAM write finish	RW
30	HIGH_BIT	1：Write to the high 22 bits of RAM address 0：Write to the low 22 bits of RAM address	RW
29:22	WADDR	Write RAM address	RW
21:0	WDATA	Write RAM value	RW

3.6.2.116 Ch 2 UV VResize Coef Read（CH2_UV_VRSZ_COEF_RD, 0x0324）

The CH2_UV_VRSZ_COEF_RD register is used to read the interpolation coefficient for channel 2 UV vertical resize .

	CH2_UV_VRSZ_COEF_RD																BASE + 0x0324															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDATA_VALID	HIGH_BIT	RADDR														RDATA															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	RDATA_VALID	RDATA valid 1:valid 0 :invalid	R
30	HIGH_BIT	1：read high 22 bits of the RAM address 0：read low 22 bits of the RAM address	RW
29:22	RADDR	The read RAM address	RW
21:0	RDATA	The read data	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.117 Ch 2 Crop Out Image Position（CH2_CROP_OPOS, 0x0328）

The CH2_CROP_OPOS is used to indicate the crop start point after scale, both the X-axis and the Y-axis should be even number .

	CH2_CROP_OPOS																BASE + 0x0328															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_CROP_OX																CH2_CROP_OY															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH2_CROP_OX	Crop upper-left point X-axis position of channel 2 crop output image .	RW
15:0	CH2_CROP_OY	Crop upper-left point Y-axis position of channel 2 crop output image .	RW

3.6.2.118 Ch 2 Crop Out Image Size（CH2_CROP_OSIZE, 0x032C）

The CH2_CROP_OSIZE is used to indicate the Channel 2 Crop output image size, both the width and the height should be even number . This size is the channel 2 final output size.

	CH2_CROP_OSIZE																BASE + 0x032C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_CROP_OW																CH2_CROP_OH															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH2_CROP_OW	The width of channel 2 crop output image , unit pixel	RW
15:0	CH2_CROP_OH	The height of channel 2 crop output image , unit pixel	RW

3.6.2.119 Ch 2 Frame Rate Ctrl Loop(CH2_FR_CTRL_LOOP, 0x0330)

The CH2_FR_CTRL_LOOP is used to indicate the maximum number of frame rate control loop number. For example the number is N, it means that it will take the bit 0 to bit N(N+1 in total) from CH2_FR_CTRL_MASK to do frame rate control . Maximum number is 31.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	CH2_FR_CTRL_LOOP																BASE + 0x0330																	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											CH2_FR_CTRL_LOOP				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect. Read as zero.	R
4:0	CH2_FR_CTRL_LOOP	Maximum: 31, Minimum:0	RW

3.6.2.120 Ch 2 Frame Rate Ctrl Mask(CH2_FR_CTRL_MASK, 0x0334)

The CH2_FR_CTRL_MASK is used to indicate which frames should be kept and which frames should be dropped .The corresponding bit is 1 means kept , 0 means dropped .The valid bits of this register is from bit 0 to bit CH2_FR_CTRL_LOOP.

	CH2_FR_CRTL_MASK																												BASE + 0x0334					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_FR_CTRL_MASK																																	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:0	CH2_FR_CTRL_MASK	the valid bits of CH2_FR_CTRL_MASK is [CH2_FR_CTRL_LOOP:0]	RW

Note： The CH2_FR_CTRL_MASK should be better configured after CH2_FR_CTRL_LOOP .

3.6.2.121 Ch 2 Mask0 Pos Register（CH2_MS0_POS, 0x0338）

The CH2_MS0_POS is used to indicate the mask start point of the area 0 of channel 2 after scale, both the X-axis and the Y-axis should be even number .

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	CH2_MS0_POS																BASE + 0x0338															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_MS0_POS_X																CH2_MS0_POS_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH2_MS0_POS_X	The X-axis of channel 2 mask area 0	RW
15:0	CH2_MS0_POS_Y	The Y-axis of channel 2 mask area 0	RW

3.6.2.122 Ch 2 Mask0 Size Register（CH2_MS0_SIZE, 0x033C）

The CH2_MS0_SIZE is used to indicate the mask size of the area 0 of channel 2 after scale, both the width and the height should be even number.

	CH2_MS0_SIZE																BASE + 0x033C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_MS0_SIZE_X																CH2_MS0_SIZE_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH2_MS0_SIZE_X	The Width of channel 2 mask area 0	RW
15:0	CH2_MS0_SIZE_Y	The Height of channel 2 mask area 0	RW

3.6.2.123 Ch 2 Mask0 Value Register（CH2_MS0_VALUE, 0x0340）

The CH2_MS0_VALUE is used to indicate the value of the mask area 0 of channel 2.

	CH2_MS0_VALUE																BASE + 0x0340															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_MS0_VALUE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	CH2_MS0_VALUE	When CH2_MASK_EN =1, if the pixel located in Mask0 ,channel 2 will output this ARGB values for Mask function. If output picture format is ARGB/RGB, this data sequence of this register is also ARGB/RGB. If background picture format is NV12/NV21, then the data sequence of this register is AYVU/AYUV	RW

Note: 1. Mask function has a priority to decide what value should output when the pixel located in overlapping mask area. Mask0 has the highest priority .

2.When output type is ARGB/RGB, the 32 bits mask value should set with the same order as output type ,for example ,if output is RBGA, the mask value is also should be RBGA .

3.When output type is RGB565, the 32 bits mask value should set as RGBRGB.

3.6.2.124 Ch 2 Mask1 Pos Register（CH2_MS1_POS, 0x0344）

The CH2_MS1_POS is used to indicate the mask start point of the area 1 of channel 2 after scale, both the X-axis and the Y-axis should be even number.

	CH2_MS1_POS																BASE + 0x0344															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_MS1_POS_X																CH2_MS1_POS_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH2_MS1_POS_X	The X-axis of channel 2 mask area 1	RW
15:0	CH2_MS1_POS_Y	The Y-axis of channel 2 mask area 1	RW

3.6.2.125 Ch 2 Mask1 Size Register（CH2_MS1_SIZE, 0x0348）

The CH2_MS1_SIZE is used to indicate the mask size of the area 1 of channel 2 after scale, both the width and the height should be even number.

	CH2_MS1_SIZE																BASE + 0x0348															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_MS1_SIZE_X																CH2_MS1_SIZE_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:16	CH2_MS1_SIZE_X	The Width of channel 2 mask area 1	RW
15:0	CH2_MS1_SIZE_Y	The Height of channel 2 mask area 1	RW

3.6.2.126 Ch 2 Mask1 Value Register（CH2_MS1_VALUE, 0x034C）

The CH2_MS1_VALUE is used to indicate the value of the mask area 1 of channel 2.

	CH2_MS1_VALUE																BASE + 0x034C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_MS1_VALUE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH2_MS1_VALUE	When CH2_MASK_EN =1, if the pixel located in Mask0 ,channel 2 will output this ARGB values for Mask function. If output picture format is ARGB/RGB, this data sequence of this register is also ARGB/RGB. If background picture format is NV12/NV21, then the data sequence of this register is AYVU/AYUV	RW

Note:

1. Mask function has a priority to decide what value should output when the pixel located in over

2.When output type is ARGB/RGB, the 32 bits mask value should set with the same order as output type ,for example ,if output is RBGA, the mask value is also should be RBGA .

3.When output type is RGB565, the 32 bits mask value should set as RGBRGB.

3.6.2.127 Ch 2 Mask2 Pos Register（CH2_MS2_POS, 0x0350）

The CH2_MS2_POS is used to indicate the mask start point of the area 2 of channel 2 after scale, both the X-axis and the Y-axis should be even number.

	CH2_MS2_POS																BASE + 0x0350															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_MS2_POS_X																CH2_MS2_POS_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:16	CH2_MS2_POS_X	The X-axis of channel 2 mask area 2	RW
15:0	CH2_MS2_POS_Y	The Y-axis of channel 2 mask area 2	RW

3.6.2.128 Ch 2 Mask2 Size Register（CH2_MS2_SIZE, 0x0354）

The CH2_MS2_SIZE is used to indicate the mask size of the area 2 of channel 2 after scale, both the width and the height should be even number.

	CH2_MS2_SIZE																BASE + 0x0354															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_MS2_SIZE_X																CH2_MS2_SIZE_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH2_MS2_SIZE_X	The Width of channel 2 mask area 2	RW
15:0	CH2_MS2_SIZE_Y	The Height of channel 2 mask area 2	RW

3.6.2.129 Ch 2 Mask2 Value Register（CH2_MS2_VALUE, 0x0358）

The CH2_MS2_VALUE is used to indicate the value of the mask area 2 of channel 2.

	CH2_MS2_VALUE																BASE + 0x0358															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_MS2_VALUE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH2_MS2_VALUE	When CH2_MASK_EN =1, if the pixel located in Mask0 ,channel 2 will output this ARGB values for Mask function. If output picture format is ARGB/RGB, this data sequence of this register is also ARGB/RGB. If background picture format is NV12/NV21, then the data sequence of this register is AYVU/AYUV	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Note:

1. Mask function has a priority to decide what value should output when the pixel located in over
2.When output type is ARGB/RGB, the 32 bits mask value should set with the same order as output type ,for example ,if output is RBGA, the mask value is also should be RBGA .
3.When output type is RGB565, the 32 bits mask value should set as RGBRGB.

3.6.2.130 Ch 2 Mask3 Pos Register（CH2_MS3_POS, 0x035C）

The CH2_MS3_POS is used to indicate the mask start point of the area 3 of channel 2 after scale, both the X-axis and the Y-axis should be even number.

	CH2_MS3_POS																BASE + 0x035C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_MS3_POS_X																CH2_MS3_POS_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH2_MS3_POS_X	The X-axis of channel 2 mask area 3	RW
15:0	CH2_MS3_POS_Y	The Y-axis of channel 2 mask area 3	RW

3.6.2.131 Ch 2 Mask3 Size Register（CH2_MS3_SIZE, 0x0360）

The CH2_MS3_SIZE is used to indicate the mask size of the area 3 of channel 2 after scale, both the width and the height should be even number.

	CH2_MS3_SIZE																BASE + 0x0360															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_MS3_SIZE_X																CH2_MS3_SIZE_Y															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CH2_MS3_SIZE_X	The Width of channel 2 mask area 3	RW
15:0	CH2_MS3_SIZE_Y	The Height of channel 2 mask area 3	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.132 Ch 2 Mask3 Value Register（CH2_MS3_VALUE, 0x0364）

The CH2_MS3_VALUE is used to indicate the value of the mask area 3 of channel 2.

	CH2_MS3_VALUE																BASE + 0x0364															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_MS3_VALUE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH2_MS3_VALUE	When CH2_MASK_EN =1, if the pixel located in Mask0 ,channel 2 will output this ARGB values for Mask function. If output picture format is ARGB/RGB, this data sequence of this register is also ARGB/RGB. If background picture format is NV12/NV21, then the data sequence of this register is AYVU/AYUV	RW

Note:

1. Mask function has a priority to decide what value should output when the pixel located in over
2.When output type is ARGB/RGB, the 32 bits mask value should set with the same order as output type ,for example ,if output is RBGA, the mask value is also should be RBGA .
3.When output type is RGB565, the 32 bits mask value should set as RGBRGB.

3.6.2.133 Ch 2 Out Data Format Register（CH2_OUT_FMT, 0x0368）

The CH2_OUT_FMT is used to indicate the Channel 2 output format . There is only one channel can do CSC transfer , so there is only one channel can set ARGB/RGB type output , the other two channels should configure as NV12/NV21.If there are more than one channel set as ARGB/RGB output, the MScaler will get a highest priority for channel 0 and the lowest priority for channel 2 to output ARGB/RGB. The lower priority channels will has a error occurred . So make sure less than two channels are set as ARGB/RGB output format .

	CH2_OUT_FMT																									BASE + 0x0368						
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									Y_OUT_ONLY	RGB_ORDER				OUT_FMT	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect. Read as zero.	R
6	Y_OUT_ONLY	1:DMAOUT Y DATA ONLY 0:BOTH Y AND UV DATA DMAOUT	RW
5:2	RGB_ORDER	ARGB order. 4'b0000: BGRA 4'b0001: GBRA 4'b0010: RBGA 4'b0011: BRGA 4'b0100: GRBA 4'b0101: RGBA 4'b1000: ABGR 4'b1001: AGBR 4'b1010: ARBG 4'b1011: ABRG 4'b1100: AGRB 4'b1101: ARGB RGB565 0:BGR 1:GBR 2:RBG 3:BRG 4:GRB 5:RGB	RW
1:0	OUT_FMT	00:NV12 01:NV21 02:ARGB888 03: RGB565	RW

3.6.2.134 Ch 2 DMAOUT Y Buff Address（CH2_DMAOUT_Y_ADDR, 0x036C）

The CH2_DMAOUT_Y_ADDR is used to indicate the channel 2 Y data DMAOUT buffer address .8 bytes align .Write this register , MScaler will store the address in a 5 depth FIFO .(if the FIFO is full , CPU should not write anymore, user can check is status by read CH2_Y_ADDR_FIFO_STA register).

DMAOUT will read the FIFO when frame start comes .CPU read data is the current address that DMAOUT is used .

	CH2_DMAOUT_Y_ADDR																BASE + 0x036C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_DMAOUT_Y_ADDR[31:3]																													Reserved		ADDR_STATU
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	CH2_DMAOUT_Y_ADDR[31:3]	The DMAOUT address that MScaler is being used . 8 bytes align	RW
2:1	Reserved	Writing has no effect. Read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	ADDR_STATU	0:current frame DMAOUT finished 1:current frame is DMAOUT	R

3.6.2.135 Ch 2 Y Buff Address FIFO Status（CH2_Y_ADDR_FIFO_STA, 0x0370）

The CH2_Y_ADDR_FIFO_STA is used to indicate the status of Y address FIFO of channel 2 .

	CH2_Y_ADDR_FIFO_STA																														
	BASE + 0x0370																														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					Wr_ptr			Rd_ptr			Entry			Full	Empty
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect. Read as zero.	R
10:8	Wr_ptr	write point of FIFO,0~4	R
7:5	Rd_ptr	read point of FIFO,0~4	R
4:2	Entry	valid address number,0~5	R
1	Full	FIFO Full , high valid	R
0	Empty	FIFO Empty, high valid	R

3.6.2.136 Ch 2 Y Buff Last Address（CH2_DMAOUT_Y_LAST_ADDR, 0x0374）

The CH2_DMAOUT_Y_LAST_ADDR is used to indicate the last DMAOUT address of channel 2 .8 byte align .Read only .User should read the FIFO status before read this register , if it is not empty ,user can get the last DMAOUT address of channel 2 Y data . If the FIFO is full , MScaler can't write anymore, the address information will lose .

	CH2_DMAOUT_Y_LAST_ADDR																														
	BASE + 0x0374																														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_DMAOUT_Y_LAST_ADDR																														
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH2_DMAOUT_Y_ LAST_ADDR	Last DMAOUT address of channel 2 Y data	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.137 Ch 2 Y Buff Last Stats Num（CH2_DMAOUT_Y_LAST_STATS_NUM, 0x0378）

The CH2_DMAOUT_Y_LAST_STATS_NUM is used to indicate the corresponding NCU frame number to last Y DMAOUT address .This is dependent on 0x374 register, every time user read the 0x374 register, then should read this register. If user read 0x374 twice without no this register read in middle, User will lose one frame number information .

	CH2_DMAOUT_Y_LAST_STATS_NUM																BASE + 0x0378															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_DMAOUT_Y_LAST_STATS_NUM																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH2_DMAOUT_Y_LAST_STATS_NUM	Corresponding Frame number with last Y address of channel 2	R

3.6.2.138 Ch 2 Y Buff Last Address FIFO Status（CH2_Y_LAST_ADDR_FIFO_STA, 0x037C）

The CH2_Y_LAST_ADDR_FIFO_STA is used to indicate the status of Y last address FIFO of channel 2 .Read only

	CH2_Y_LAST_ADDR_FIFO_STA																BASE + 0x037C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					Wr_ptr			Rd_ptr			Entry			Full	Empty
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect. Read as zero.	R
10:8	Wr_ptr	write point of FIFO,0~4	R
7:5	Rd_ptr	read point of FIFO,0~4	R
4:2	Entry	valid address number,0~5	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	Full	FIFO Full , high valid	R
0	Empty	FIFO Empty, high valid	R

3.6.2.139 Ch 2 DMAOUT Y Line Stride（CH2_DMAOUT_Y_STRI, 0x0380）

The CH2_DMAOUT_Y_STRI is used to indicate the line stride of channel 2 Y data . IF output format is RGB888 , it's four tines as the output width and if the output format is RGB565 , it's two times as the output width .

	CH2_DMAOUT_Y_STRI																BASE + 0x0380															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CH2_Y_STRI															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect. Read as zero.	R
15:0	CH2_Y_STRI	the line stride of channel 2 Y data, unit pixel	RW

3.6.2.140 Ch 2 DMAOUT UV Buff Address（CH2_DMAOUT_UV_ADDR, 0x0384）

The CH2_DMAOUT_UV_ADDR is used to indicate the channel 2 UV data DMAOUT buffer address .8 byte align .Write this register , MScaler will store the address in a 5 depth FIFO .(if the FIFO is full , CPU should not write anymore, user can check is status by read CH2_UV_ADDR_FIFO_STA register).DMAOUT will read the FIFO when frame start comes .CPU read data is the current address that DMAOUT is used .

	CH2_DMAOUT_UV_ADDR																BASE + 0x0384															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_DMAOUT_UV_ADDR[31:3]																													Reserved		ADDR_STATU
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	CH2_DMAOUT_UV_ADDR[31:1]	The DMAOUT address that MScaler is being used . 8 bytes align	RW
2:1	Reserved	Writing has no effect. Read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	ADDR_STATU	0:current frame DMAOUT finished 1:current frame is DMAOUT	R

3.6.2.141 Ch 2 UV Buff Address FIFO Status（CH2_UV_ADDR_FIFO_STA, 0x0388）

The CH2_UV_ADDR_FIFO_STA is used to indicate the status of UV address FIFO of channel 2.

	CH2_UV_ADDR_FIFO_STA																														
	BASE + 0x0388																														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					Wr_ptr			Rd_ptr			Entry			Full	Empty
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect. Read as zero.	R
10:8	Wr_ptr	write point of FIFO,0~4	R
7:5	Rd_ptr	read point of FIFO,0~4	R
4:2	Entry	valid address number,0~5	R
1	Full	FIFO Full , high valid	R
0	Empty	FIFO Empty, high valid	R

3.6.2.142 Ch 2 UV Buff Last Address（CH2_DMAOUT_UV_LAST_ADDR, 0x038C）

The CH2_DMAOUT_UV_LAST_ADDR is used to indicate the last DMAOUT address of channel 2 .8 byte align .Read only .User should read the FIFO status before read this register, if it is not empty ,user can get the last DMAOUT address of channel 2 UV data . If the FIFO is full , MScaler can't write anymore, the address information will lose .

	CH2_DMAOUT_UV_LAST_ADDR																														
	BASE + 0x038C																														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_DMAOUT_UV_LAST_ADDR																														
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH2_DMAOUT_UV_LAST_ADDR	Last DMAOUT address of channel 2 UV data	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.143 Ch 2 UV Buff Last Stats num（CH2_DMAOUT_UV_LAST_STATS_NUM, 0x0390）

The CH2_DMAOUT_UV_LAST_STATS_NUM is used to indicate the corresponding NCU frame number to last UV DMAOUT address .This is dependent on 0x38C register, every time user read the 0x38C register, then should read this register. If user read 0x38C twice without no this register read in middle, User will lose one frame number information .

	CH2_DMAOUT_UV_LAST_STATS_NUM																BASE + 0x0390															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH2_DMAOUT_UV_LAST_STATS_NUM																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CH2_DMAOUT_UV_LAST_STATS_NUM	Corresponding Frame number with last UV address of channel 2	R

3.6.2.144 Ch 2 UV Buff Last Address FIFO Status （CH2_UV_LAST_ADDR_FIFO_STA, 0x0394）

The CH2_UV_LAST_ADDR_FIFO_STA is used to indicate the status of UV last address FIFO of channel 2 .Read only

	CH2_UV_LAST_ADDR_FIFO_STA																BASE + 0x0394															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					Wr_ptr			Rd_ptr			Entry			Full	Empty
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect. Read as zero.	R
10:8	Wr_ptr	write point of FIFO,0~4	R
7:5	Rd_ptr	read point of FIFO,0~4	R
4:2	Entry	valid address number,0~5	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	Full	FIFO Full , high valid	R
0	Empty	FIFO Empty, high valid	R

3.6.2.145 Ch 2 DMAOUT UV Line Stride（CH2_DMAOUT_UV_STRI, 0x0398）

The CH2_DMAOUT_UV_STRI is used to indicate the line stride of channel 2 UV data .8 byte align .

	CH2_DMAOUT_UV_STRI																BASE + 0x0398															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CH2_UV_STRI															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect. Read as zero.	R
15:0	CH2_UV_STRI	the line stride of channel 2 UV data, unit pixel	RW

3.6.2.146 Ch 2 DMAOUT Y Address Buff Clear (CH2_DMAOUT_Y_ADDR_CLR,0x039C)

The CH2_DMAOUT_Y_ADDR_CLR is used to set to clear channel 2 DMAOUT Y address FIFO .

	CH2_DMAOUT_Y_ADDR_CLR																BASE + 0x039C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CH2_Y_ADDR_CLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CH2_Y_ADDR_CLR	CH2 DMAOUT Y Address FIFO clear ,write 1 clear	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.147 Ch 2 DMAOUT UV Address Buff Clear (CH2_DMAOUT_UV_ADDR_CLR,0x03A0)

The CH2_DMAOUT_UV_ADDR_CLR is used to set to clear channel 2 DMAOUT UV address FIFO

	CH2_DMAOUT_UV_ADDR_CLR																BASE + 0x03A0														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CH2_UV_ADDR_CLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CH2_UV_ADDR_CLR	CH2 DMAOUT UV Address FIFO clear ,write 1 clear	RW

3.6.2.148 Ch 2 DMAOUT Y Last Address Buff Clear (CH2_DMAOUT_Y_LAST_ADDR_CLR,0x03A4)

The CH2_DMAOUT_Y_LAST_ADDR_CLR is used to set to clear channel 2 DMAOUT Y last address FIFO

	CH2_DMAOUT_Y_LAST_ADDR_CLR																BASE + 0x03A4														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CH2_Y_LAST_ADDR_CLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CH2_Y_LAST_ADDR_CLR	CH2 DMAOUT Y Last Address FIFO clear ,write 1 clear	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.149 Ch 2 DMAOUT UV LAST Address Buff Clear (CH2_DMAOUT_UV_LAST_ADDR_CLR,0x03A8)

The CH2_DMAOUT_UV_LAST_ADDR_CLR is used to set to clear channel 2 DMAOUT UV last address FIFO

	CH2_DMAOUT_Y_LAST_ADDR_CLR																BASE + 0x03A8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CH2_UV_LAST_ADDR_CLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CH2_UV_LAST_ADDR_CLR	CH2 DMAOUT UV Last Address FIFO clear ,write 1 clear	RW

3.6.2.150 Ch 2 DMAOUT Y Address Buff Select (CH2_DMAOUT_Y_ADDR_SEL,0x03AC)

The CH2_DMAOUT_Y_ADDR_SEL is used to set to select channel 2 DMAOUT Y address from Y address FIFO or Y address register when Tiziano overflow happened . Address register is a buffer to store address read from address FIFO .

	CH2_DMAOUT_Y_ADDR_SEL																BASE + 0x03AC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CH2_Y_ADDR_SEL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CH2_Y_ADDR_SEL	0: From address register 1: From address FIFO	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3.6.2.151 Ch 2 DMAOUT UV Address Buff Select (CH2_DMAOUT_UV_ADDR_SEL,0x03B0)

The CH2_DMAOUT_UV_ADDR_SEL is used to set to select channel 2 DMAOUT UV address from UV address FIFO or UV address register when Tiziano overflow happened . Address register is a buffer to store address read from address FIFO .

	CH2_DMAOUT_UV_ADDR_SEL																BASE + 0x03B0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															CH2_UV_ADDR_SEL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	CH2_UV_ADDR_SEL	0: From address register 1: From address FIFO	RW

3.6.2.152 Ch 2 Coe Zero Vrsz H（CH2_COE_ZERO_VRSZ_H, 0x01C0）

Channel 2 vresize coe zero value.

	CH2_COE_ZERO_VRSZ_H																BASE + 0x001C0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																ch2_vrsz_zero_h																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect. Read as zero.	R
21:0	ch2_vrsz_zero_h	channel 2 vresize zero coef hight	RW

3.6.2.153 Ch 2 Coe Zero Vrsz L（CH2_COE_ZERO_VRSZ_L, 0x01C4）

Channel 2 vresize coe zero value.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	CH2_COE_ZERO_VRSZ_L																BASE + 0x001C4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																ch2_vrsz_zero_l															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect. Read as zero.	R
21:0	ch2_vrsz_zero_l	channel 2 vresize zero coef low	RW

3.6.2.154 Ch 2 Coe Zero Hrsz H（CH2_COE_ZERO_VRSZ_H, 0x01C8）

Channel 2 hresize coe zero value.

	CH0_COE_ZERO_HRSZ_H																BASE + 0x001C8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																ch2_hrsz_zero_h															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect. Read as zero.	R
21:0	ch2_hrsz_zero_h	channel 2 hresize zero coef hight	RW

3.6.2.155 Ch 2 Coe Zero Hrsz L（CH2_COE_ZERO_HRSZ_L, 0x01CC）

Channel 2 hresize coe zero value.

	CH2_COE_ZERO_HRSZ_L																BASE + 0x001CC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																ch2_hrsz_zero_l															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect. Read as zero.	R
21:0	ch2_hrsz_zero_l	channel 2 hresize zero coef low	RW

3.6.2.156 Ch 2 Coe Oft（CH2_COE_OFT, 0x03D0）

Channel 2 resize coe oft.

	CH2_COE_OFT																BASE + 0x003D0														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																ch2_coe_oft_hrsz								Reserved							
																																ch2_coe_oft_vrsz
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect. Read as zero.	R
24:16	ch2_coe_oft_hrsz	channel 2 coe oft for hresize	RW
15:9	Reserved	Writing has no effect. Read as zero.	R
8:0	ch2_coe_oft_vrsz	channel 2 coe oft for vresize	RW

3.7 Index

Table 3-4 Description of Proprietary Vocabulary

Name	Description
MScaler/MSCA	Multiple Channel Scaler
CSC	Color Space Conversion
DMA	Direct Memory Access

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4 Video Interface Control (VIC)

4.1 Overview

The VIC module is a video input image preprocessing module to reorder the different kinds of input images to a uniform type then output to TIZIANOor write to DDR.

4.2 Features

4.2.1 VIC features

- Work mode: image mode
- Maximum working freq: 350Mhz

Image mode:

- input interface: BT、DVP、MIPI
- Maximum input image size:
  - MIPI: 8M@30fps、6M@30fps、1080p@60fps
  - BT/DVP: 1080p@30fps、720p@60fps
- Minimum input image size: 128*128
- Image format
  - sensor port support

    DVP: RAW8、RAW10、RAW12、YUV422 (Serial 8bit)

    BT601: YUV422 (Parallel 16bit)、YUV422 (Serial 8bit)

    BT656: YUV422 (Serial 8bit)

    BT1120: YUV422 (Parallel 16bit)、YUV422 (Serial 8bit)

    MIPI: RAW8、RAW10、RAW12
  - VIC output port format

    Tiziano: RAW8、RAW10、RAW12

    Scaler: YUV422 (8bit)

    DMA: RAW8、RAW10、RAW12、YUV422 (8bit)

    MIPI: RAW8、RAW10、RAW12
- Fault tolerance
  - DVP、BT601: frame start reset、every line of data within a fixed
  - BT656、BT1120: error reset、every line of data within a fixed
- Support DVP8bit port flexible connection
- VIC DMA output format : RAW16、NV12、NV21

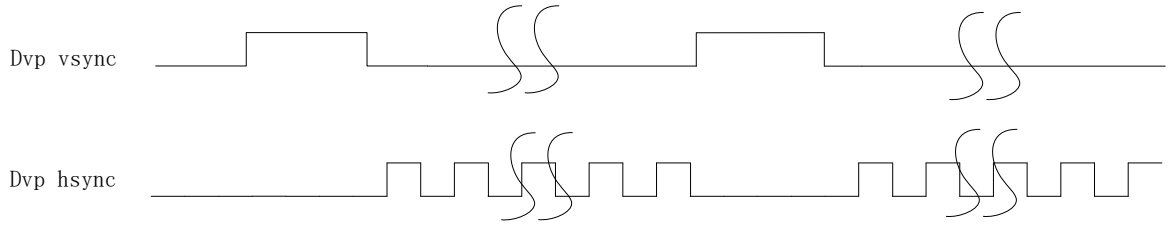
Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4.3 Interface Timing

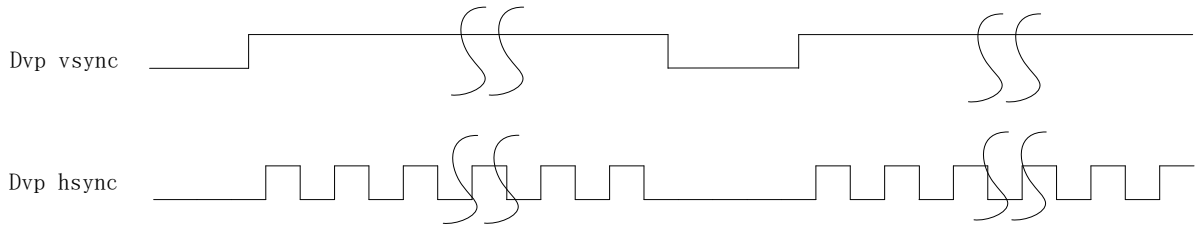
4.3.1 DVP

The DVP interface is a parallel video port which input video data from the sensor in raster-scan order, left-to-right, top-to-bottom, one pixel at a time, at the pixel clock rate.

In the VIC, DVP input interface supports 4 timing modes which are listed as following figures. The vsync and hsync polarity can be configured in VIC.



a) pulse sync



b) line valid

Figure 4-1 DVP mode0

As Figure 4-1 a) b) described, the mode0 is called pulse sync or line valid mode. For pulse sync, one vsync pulse indicate the frame start, and after the vsync pulse, the data is valid if hsync valid. For line valid, one vsync pulse indicate the frame start, and when the vsync pulse and hsync are valid, the data is valid.

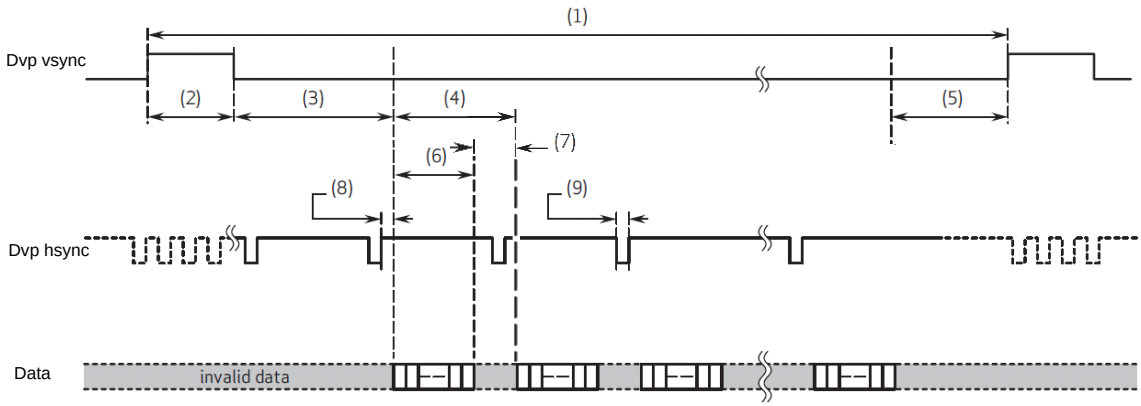


Figure 4-2 DVP mode1

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

As Figure 4-2 described, the mode1 is called vsync mode which one vsync pulse indicate the frame start. For the vsync and hsync there are a front porch and a back porch and the data is invalid when vsync and hsync is front and back porch.

4.3.2 BT

BT video input image format as flow Figure 4-3, the line number is not stationary.

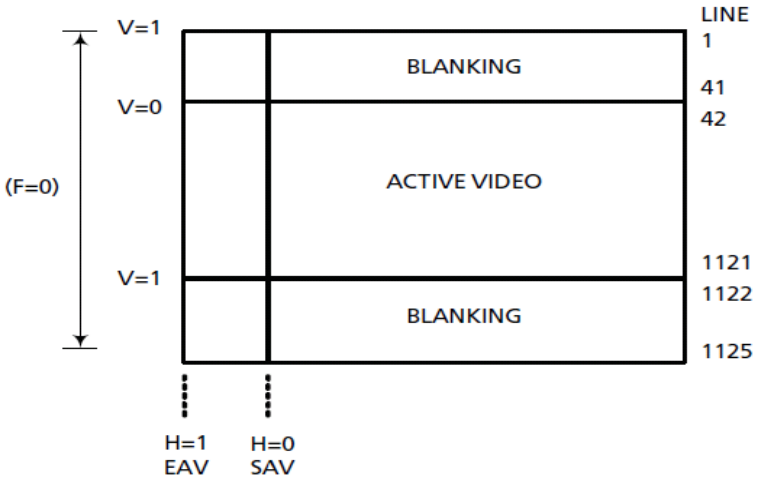


Figure 4-3 BT input format

Composition of interface data line stream as Figure 4-4,image width is not stationary .

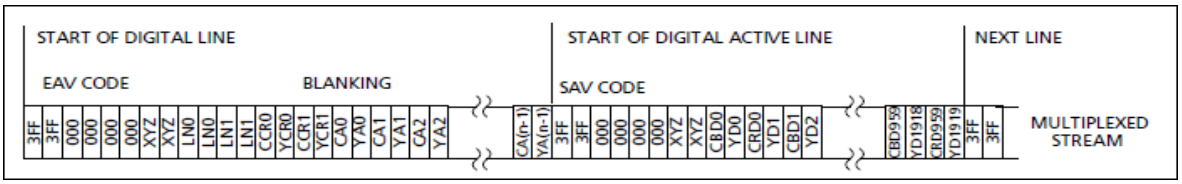


Figure 4-4 BT input line format

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Video timing reference codes as Figure 4-5, take 10 bits data as example.

Data bit number	First word (3FF)	Second word (000)	Third word (000)	Fourth word (XYZ)
9 (MSB)	1	0	0	1
8	1	0	0	F
7	1	0	0	V
6	1	0	0	H
5	1	0	0	P_3
4	1	0	0	P_2
3	1	0	0	P_1
2	1	0	0	P_0
1 (Note 2)	1	0	0	0
0	1	0	0	0

NOTE 1 – The values shown are those recommended for 10-bit interfaces.

NOTE 2 – For compatibility with existing 8-bit interfaces, the values of bits D_1 and D_0 are not defined.

F = 0 during field 1 / 1 during field 2

V = 0 elsewhere / 1 during field blanking

H = 0 in SAV / 1 in EAV

P_0, P_1, P_2, P_3: protection bits (see Table 3)

MSB: most significant bit

Figure 4-5 BT timing reference codes

BT601 uses external sync signal to replace sync codes .

4.4 Data Format

4.4.1 Input data

The width of input data from DVP or BT interface can be 8bit or 12bit, and the data is uncompressed.

a) RAW

The RAW data sequence follows the generic dvp rule. It is described in Table 4-1

Table 4-1 RAW Data sequence

Sequence mode	First clock	Second clock	Third clock	Fourth clock
dvp_msb=0	dvp_data [n-1:0]	dvp_data [n-1:0]	dvp_data [n-1:0]	dvp_data [n-1:0]
dvp_msb=1	dvp_data [15:15-n+1]	dvp_data [15:15-n+1]	dvp_data [15:15-n+1]	dvp_data [15:15-n+1]

b) YUV422 8-bit

The YUV422 8-bit data sequence follows the generic DVP or BT rule. It is described in Table 4-2.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Table 4-2 YUV422 8-bit Data sequence

Sequence mode	First clock	Second clock	Third clock	Fourth clock
YUV_data_order=0	V1[7:0]	Y1[7:0]	U2[7:0]	Y2[7:0]
YUV_data_order=1	U1[7:0]	Y1[7:0]	V2[7:0]	Y2[7:0]
YUV_data_order=2	Y1[7:0]	V1[7:0]	Y2[7:0]	U2[7:0]
YUV_data_order=3	Y1[7:0]	U1[7:0]	Y2[7:0]	V2[7:0]

NOTES:

1. If input is YCbCr, U is replaced by Cb, V is replaced by Cr.

4.4.2 Internal data

Table 4-3 Internal data sequence

S	data_in[23:12]	data_in[11:0]
RAW6	12'b0	RAW[5:0],6'b0
RAW7	12'b0	RAW[6:0],5'b0
RAW8	12'b0	RAW[7:0],4'b0
RAW10	12'b0	RAW[9:0],2'b0
RAW12	12'b0	RAW[11:0]

For the YCbCr 4:2:2,the internal data sequence is as below.

Table 4-4 YUV422 internal sequence

Pixel	data_in[23:12]	data_in[11:0]
0	Y0[7:0], Cb0[7:4]	Cb0[3:0], 8'b0
1	Y1[7:0], Cr0[7:4]	Cr0[3:0], 8'b0
2	Y2[7:0], Cb2[7:4]	Cb2[3:0], 8'b0
3	Y3[7:0], Cr2[7:4]	Cr2[3:0], 8'b0
4	Y4[7:0], Cb4[7:4]	Cb4[3:0], 8'b0
5	Y5[7:0], Cr4[7:4]	Cr4[3:0], 8'b0

4.4.3 Output data

VIC output image data to system DDR SRAM. There are multiple options of packing video data depending on the selected output format. Output format and data packing options are selected using the base mode & plane select parameters(configured in each DMA writer control register), A table of available formats are shown below.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Table 4-5 DMA Output Formats and Packing

Baseplane select		Colour Format	Packing Bit Number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0	0	DMA disabled	
1	0	RGB32(also used for RGB666)	0 0 0 0 0 0 0 0 Red (7:0) Green(7:0) Blue(7:0)
2	0	A2R10G10B10	0 0 Red (9:0) Green(9:0) Blue(9:0)
3	0	RGB 565	Red (4:0) Green(5:0) Blue(4:0) Red (4:0) Green(5:0) Blue(4:0)
5	0	GEN32	Generic Data(31:0)
6	0	RAW16	RAW1(11:0) 0 0 0 0 RAW0(11:0) 0 0 0 0
7	0	RAW12	RAW2(7:0) RAW1(11:0) RAW0(11:0)
			RAW5(3:0) RAW4(11:0) RAW3(11:0) RAW2(11:8
			RAW7(11:0) RAW6(11:0) RAW5(11:4)
8	0	AYUV, 8 bit	0 0 0 0 0 0 0 0 Y(7:0) U(7:0) V(7:0)
10	0	YUY2, 8 bit	V0(7:0) Y1(7:0) U0(7:0) Y0(7:0)
11	0	UYVY, 8 bit	Y1(7:0) V0(7:0) Y0(7:0) U0(7:0)
13	0	NV12/21 Y	Y3(7:0) Y2(7:0) Y1(7:0) Y0(7:0)
	1	NV12 U/V	V1(7:0) U1(7:0) V0(7:0) U0(7:0)
	2	NV21 U/V	U1(7:0) V0(7:0) U0(7:0) V0(7:0)
Notes		In Base mode1, to support RGB666 the bottom2 bits of each colour can be masked in 'Colour space conv ' block. Base mode 5 is for Temper Frame buffer only. In Base mode6 & 7 to support10&8 bit RAW the LSB's of ISP input need to be set to zero	



4.5 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute

   R - Read only

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

W - Write only
RW - read and write
RCW - read and write, but clear to 0 by read
RSW - read and write, but set to 1 by read
RWC - read and write, clear to 0 by write 1, write 0 has no effect
RWS - read and write, set to 1 by write 1, write 0 has no effect
RC - read only, and clear to 0 by read
RS - read only, and set to 1 by read
SPEC - special access method, relate to its description

3. Reset Value
1 - reset to 1
0 - reset to 0
? - value unknown after reset

4.5.1 Register Memory Map

The VIC registers can be divided to 4 groups, such as registers of VIC, registers of VIC DMA. These register groups' base addresses be listed as Table 4-6.

Table 4-6 Registers Memory Map Base Address

Name	Base	Description
VIC_BA	0x13710000	Address base of ISP0 VIC
VIC_BA	0x13810000	Address base of ISP1 VIC

4.5.2 VIC Registers

Table 4-7 VIC Registers Map

Name	RW	Reset Value	Address Offset	Access Size
VIC_CTRL	RW	0x0000_0000	0x000	32
VIC_RES	RW	0x0000_0000	0x004	32
VIC_FRM_ECC	RW	0x0000_0000	0x008	32
VIC_IN_INTF	RW	0x0000_0000	0x00C	32
VIC_IN_DVP	RW	0x0000_0000	0x010	32
VIC_IN_CSI_FMT	RW	0x0000_0000	0x014	32
VIC_IN_HOR_PARA0	RW	0x0000_0000	0x018	32
VIC_IN_HOR_PARA1	RW	0x0000_0000	0x01C	32
VIC_BK_CB_CTRL	RW	0x0000_0000	0x028	32
VIC_BK_CB_BLK	RW	0x0000_0000	0x02C	32
VIC_IN_VER_PARA0	RW	0x0000_0000	0x030	32
VIC_IN_VER_PARA1	RW	0x0000_0000	0x034	32
VIC_IN_VER_PARA2	RW	0x0000_0000	0x038	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

VIC_IN_VER_PARA3	RW	0x0000_0000	0x03C	32
VIC_VLD_LINE_SAV	RW	0x0080_0800	0x060	32
VIC_VLD_LINE_EAV	RW	0x009D_09D0	0x064	32
VIC_VLD_FRM_SAV	RW	0x0000_6002	0x070	32
VIC_VLD_FRM_EAV	RW	0x0000_7003	0x074	32
VIC_VC_CONTROL	R	0x0000_0000	0x08C	32
VIC_VC_CONTROL_CH0_PIX	R	0x0000_0000	0x090	32
VIC_VC_CONTROL_CH1_PIX	R	0x0000_0000	0x094	32
VIC_VC_CONTROL_CH2_PIX	R	0x0000_0000	0x098	32
VIC_VC_CONTROL_CH3_PIX	R	0x0000_0000	0x09C	32
VIC_VC_CONTROL_CH0_LINE	R	0x0000_0000	0x0A0	32
VIC_VC_CONTROL_CH1_LINE	R	0x0000_0000	0x0A4	32
VIC_VC_CONTROL_CH2_LINE	R	0x0000_0000	0x0A8	32
VIC_VC_CONTROL_CH3_LINE	R	0x0000_0000	0x0AC	32
VIC_VC_CONTROL_FIFO_USE	R	0x0000_0000	0x0B0	32
VIC_CB_1ST	RW	0x00EB_8080	0x0C0	32
VIC_CB_2ND	RW	0x0010_8080	0x0C4	32
VIC_CB_3RD	RW	0x0029_F06E	0x0C8	32
VIC_CB_4TH	RW	0x0091_3622	0x0CC	32
VIC_CB_5TH	RW	0x0051_5AF0	0x0D0	32
VIC_CB_6TH	RW	0x00AA_A610	0x0D4	32
VIC_CB_7TH	RW	0x00D2_1092	0x0D8	32
VIC_CB_8TH	RW	0x006A_CADE	0x0DC	32
VIC_CB2_1ST	RW	0x00EB_8080	0x0E0	32
VIC_CB2_2ND	RW	0x0010_8080	0x0E4	32
VIC_CB2_3RD	RW	0x0029_F06E	0x0E8	32
VIC_CB2_4TH	RW	0x0091_3622	0x0EC	32
VIC_CB2_5TH	RW	0x0051_5AF0	0x0F0	32
VIC_CB2_6TH	RW	0x00AA_A610	0x0F4	32
VIC_CB2_7TH	RW	0x00D2_1092	0x0F8	32
VIC_CB2_8TH	RW	0x006A_CADE	0x0FC	32
MIPI_ALL_WIDTH_4BYTE	RW	0x0000_0000	0x100	32
MIPI_VCROP_DEL01	RW	0x0000_0000	0x104	32
MIPI_SENSOR_CONTROL	RW	0x0000_0000	0x10C	32
MIPI_HCROP_CH0	RW	0x0000_0000	0x110	32
MIPI_VCROP_SHADOW_CFG	RW	0x0000_0000	0x120	32
VC_CONTROL_LIMIT	RW	0x0000_0000	0x1A0	32
VC_CONTROL_DELEY	RW	0x0000_0000	0x1A4	32
VC_CONTROL_TIZIANO_ROUTE	RW	0x0000_3210	0x1A8	32
VC_CONTROL_DMA_ROUTE	RW	0x0000_0000	0x1B0	32
VIC_INT_STA	R	0x0000_0000	0x1E0	32
VIC_INT_MASK	RW	0x0000_0000	0x1E8	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

VIC_INT_CLR	W	0x0000_0000	0x1F0	32

4.5.2.1 VIC_CTRL Register (VIC_CTRL,0x000)

The VIC_CTRL register is used to start VIC, reset VIC .

	VIC_CTRL																VIC_BA+0x000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved																													GLB_RST	REG_EN	VIC_START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:3	Reserved	Writing has no effect, read as zero. As default, please setting these bits 0.	R
2	GLB_RST	When this bit is set to 1，the VIC will be reset when the AXI bus has transited the current burst data.	RW
1	REG_EN	When this bit is set to 1, the VIC will start initializing. When the VIC is already initialized, this bit will be set to 0 automatically.	RW
0	VIC_START	Start VIC, When this bit is 1 set to, the VIC will start working. This bit will be set to 0 automatically when the working space has been started.	RW

4.5.2.2 VIC_RES Register (VIC_RES,0x004)

The VIC_RES register is used to configure the resolution of image.

	VIC_RES																VIC_BA+0x004															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	hor_res																ver_res															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	hor_res	Horizontal Size of resolution. Maximum horizontal size of a frame is 2048, because of the maximum horizontal of TIZIANO is 2048.	RW
15:0	ver_res	Vertical Size of resolution Maximum vertical size of a frame is 2048.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4.5.2.3 VIC_FRM_ECC Register (VIC_FRM_ECC,0x008)

The VIC_FRM_ECC register is used to enable VIC frame ecc function

	VIC_FRM_ECC																VIC_BA+0x008															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved																														frame_ecc_mode	frame_ecc_en
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
1	frame_ecc_mode	0=frame will be ecc either VIC enable or disable 1=frame will be ecc only when VIC enable	RW
0	frame_ecc_en	0=Disable frame ecc function 1=Enable frame ecc function	RW

4.5.2.4 VIC_IN_INTF Register (VIC_IN_INTF,0x00C)

The VIC_IN_INTF register is used to select the input interface of VIC.

	VIC_IN_INTF																VIC_BA+0x00c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved																														INPUT_INTF	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:3	Reserved	Writing has no effect, read as zero.	R
2:0	INPUT_INTF	VIC input interface type. 3'b000: BT 656 3'b001: BT 601 3'b010: MIPI_CSI 3'b011: DVP 3'b100: BT 1120 3'b101: reserved 3'b110: reserved **Note:** the interface timing protocol has been described in 1.7 section.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4.5.2.5 VIC_IN_DVP Register (VIC_IN_DVP,0x010)

The VIC_IN_DVP register is used to configure the DVP interface of VIC.

	VIC_IN_DVP																VIC_BA+0x010													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	dvp_hcomp	Reserved		dvp_img_chk	dvp_bus_selec t				dvp_rgb_order			dvp_raw_align	dvp_data_form at			dvp_mode	Reserved				bt_intf_wide	bt_lsav_eav	bt601_mode	Reserved			yuv_order		Reserved		hsync_porlar	vsync_polar
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	dvp_hcomp	DVP/BT Interception and completion function can mark. Open automatically after the completion of the number of lines, remove most of the line.	RW
30:29	Reserved	Writing has no effect, read as zero. As default, please setting these bits 0.	R
28	dvp_img_chk	1=check all vertical and horizon resolution When =1，0x70，0x74 should be configured as ver and hor res. 0=check valid vertical and horizon resolution	RW
27:24	dvp_bus_select	YUV422 or RGB565 or RGB555 pixel's data position in dvp_data[15:0]. (only dvp_data_type=6 or 7, this field is available.) 0000: dvp[7:0] 0001: dvp[8:1] 0010: dvp[9:2] 0011: dvp[10:3] 0100: dvp[11:4] 0101: dvp[12:5] 0110: dvp[13:6] 0111: dvp[14:7] 1000: dvp[15:8]	RW
23:21	dvp_rgb_order	RGB565/555 input sequence from dvp interface. (only dvp_data_type=7, this field is available.) 000: {b[4:0],g[5:3]},{g[2:0],r[4:0]} 001: {r[4:0],g[5:3]},{g[2:0],b[4:0]} 010: {g[5:0],r[4:2]},{r[1:0],b[4:0]} 011: {b[4:0],r[4:2]},{r[1:0],g[5:0]} 100: {g[5:0],b[4:3]},{b[2:0],r[4:0]} 101: {r[4:0],b[4:2]},{b[1:0],g[5:0]}	RW
20	dvp_raw_align	The alignment of raw data for dvp interface 0: low align [7:0]、[9:0]、[11:0]	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1:high align [11:4]、[11:2]、[11:0]	
19:17	dvp_data_format	data type of pixel input from dvp interface. 000: RAW8 001: RAW10 010: RAW12 011: YUV422 100: reserved 101: reserved 110: YUV422(8bit IO) 111: reserved	RW
16:15	dvp_timing_mode	dvp interface timing mode 00: href mode 01: hsync mode (There is internal synchronous signal similar to BT in data line) 10: sony mode 11: reserved **Note**: the dvp interface timing mode has been described in 4.5.1 section.	RW
14:12	Reserved	Writing has no effect, read as zero. As default, please setting these bits 0.	RW
11	bt_intf_wide	bt 601/656/1120 interface width. 0:8bit 1:16bit	RW
10	bt_sav_eav	line mode indicates the position of EAV and SAV 0:EAV before SAV 1:SAV before EAV	RW
9	bt601_ mode	bt601 interface vertical timing mode 0: toggle mode 1:pulse mode	RW
8: 6	Reserved	Writing has no effect, read as zero. As default, please setting these bits 0.	R
5:4	yuv_data_order	The YUV422 sequence, it is available when input interface is bt656/1120 bt601 or dvp_mode For 8bit interface width, the input yuv order(clock4<-clock0): 00: Y1, V0,Y0,U0 01: Y1, U0,Y0,V0 10: V0, Y1,U0,Y0 11: U0, Y1,V0,Y0 For 16bit interface width, the input yuv order(clock1<-clock0): 00: {Y1, V0}, {Y0,U0} 01: {Y1, U0}, {Y0,V0}	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		10: {V0, Y1}, {U0,Y0} 11: {U0, Y1}, {V0,Y0} **Note:** when data format is YCbCr, U replaced by Cb, V replaced by Cr	
3	start_field	When input interlace image, the first field type. 0:first field is odd. 1:first field is even	RW
2	interlace_en	input image is progress or interlace 0:progress 1:interlace	RW
1	hsync_polar	external hsync polarity. 0:high active(hsync's posedge indicate one line start) 1:low active (hsync's negedge indicate one line start)	RW
0	vsync_polar	external vsync polarity. 0:high active (vsync's posedge indicate one frame start) 1:low active (vsync's negedge indicate one frame start)	RW

4.5.2.6 VIC_IN_CSI_ FMT Register (VIC_IN_CSI_LVDS_FMT,0x014)

The VIC_IN_CSI_ FMT register is used to configure MIPI-CSI interface of VIC.

	VIC_IN_CSI_ FMT																VIC_BA+0x014													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved																										pixel_format					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:6	Reserved	Writing has no effect. Read as zero.	R
5:0	pixel_format	Configure the data type for MIPI_CSI and LVDS input. 0:RAW8 1:RAW10 2:RAW12	RW

4.5.2.7 VIC_IN_HOR_PARA0 Register (VIC_IN_HOR_PARA0,0x018)

The VIC_IN_HOR_PARA0 register is used to configure horizon parameters for dvp mode.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	VIC_IN_HOR_PARA0																VIC_BA+0x018															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	hfb_num																hact_num															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	hfb_num	Horizon front blanking time (unit is pixel clock) **Note**:This bit field be used for bt601、dvp hsync mode、dvp sony mode.	RW
15:0	hact_num	Horizon active time (unit is pixel clock) **Note**:This bit field be used for bt601、dvp hsync mode、dvp sony mode.	RW

4.5.2.8 VIC_IN_HOR_PARA1 Register (VIC_IN_HOR_PARA1,0x01C)

The VIC_IN_HOR_PARA1 register is used to configure horizon parameters .

	VIC_IN_HOR_PARA1																VIC_BA+0x01C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserve																hbb_num															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	Reserve	Writing has no effect. Read as zero.	RW
15:0	hbb_num	Horizon back blanking time (unit is pixel clock) **Note:**This bit field used for bt601 interface only	RW

4.5.2.9 VIC_BK_CB_CTRL Register (VIC_BK_CB_CTRL, 0x028)

The VIC_BK_CB_CTRL register is used to configure the VIC' back color bar.

	VIC_BK_CB_CTRL																VIC_BA+0x028															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	enable	incremenal_mode	direction	pixel_format	Reserved	color_bar_dir	frame_num
RST	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	enable	Color bar mode0 enable	RW
30	incremetal_mode	Increase or constant value 1: increase in each line 0: each color bar is constant value (8 bars, each bar's value can be configure)	RW
29	direction	0: horizon color bar 1: vertical color bar(only available when bit30=0、bit26=0)	RW
28:27	pixel_format	0: raw format 1: yuv422 format 2: rgb format (only available when bit30=0)	RW
26	color_bar_dir	0: invalid 1: horizon color bar and vertical color bar each frame switch	RW
25:16	Reserved	Writing has no effect, read as zero.	RW
16	free_bar_blk	0: horizon blank and vertical blank according to 0x0B4 1: free horizon blank and vertical blank	
15:0	frame_num	When frame_num=16'h8000, frame number is infinite, When frame_num[15]=0, frame number is frame_num[14:0]	RW

4.5.2.10 VIC_BK_CB_BLK Register (VIC_BK_CB_BLK, 0x02C)

The VIC_BK_CB_BLK register is used to configure the VIC's front color bar blanking number.

	VIC_BK_CB_BLK																VIC_BA+0x02C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	hor_ blank																ver_blank															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	hor_blank	horizon blank number(unit is work clock)	RW
15:0	ver_blank	vertical blank number(unit is line)	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4.5.2.11 VIC_IN_VER_PARA0 Register (VIC_IN_VER_PARA0,0x030)

The VIC_IN_VER_PARA0 register is used to configure odd frame VFB and VACT.

	VIC_IN_VER_PARA0																VIC_BA+0x030															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	odd_vfb																odd_vact															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	odd_vfb	Odd frame vertical front porch blanking. Unit is line **Note:** This bit field only be used for bt601.	RW
15:0	odd_vact	Odd frame vertical active line **Note:**This bit field only be used for bt601.	RW

4.5.2.12 VIC_IN_VER_PARA1 Register (VIC_IN_VER_PARA1,0x034)

The VIC_IN_VER_PARA1 register is used to configure odd frame VBB and even frame VFB

	VIC_IN_VER_PARA1																VIC_BA+0x034															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	odd_vbb																even_vfb															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	odd_vbb	Odd frame vertical back porch blanking. Unit is line **Note**: This bit field only be used for bt601.	RW
15:0	even_vfb	Even frame vertical front porch blanking. Unit is line **Note**: This bit field only be used for bt601.	RW

4.5.2.13 VIC_IN_VER_PARA2 Register (VIC_IN_VER_PARA2,0x038)

The VIC_IN_VER_PARA2 register is used to configure vertical parameters.

	VIC_IN_VER_PARA2																VIC_BA+0x038															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	even_vact															even_vbb															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	even_vact	Even frame vertical active line **Note**: This bit field only be used for bt601.	RW
15:0	even_vbb	Even frame vertical back porch blanking. Unit is line **Note**: This bit field only be used for bt601.	RW

4.5.2.14 VIC_IN_VER_PARA3 Register (VIC_IN_VER_PARA3,0x03C)

The VIC_IN_VER_PARA3 register is used to configure dvp vertical front blanking for dvp hsync mode.

	VIC_IN_VER_PARA3																VIC_BA+0x03C														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN_VPARA3																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	IN_VER_PARA 3	DVP vertical sync front porch blanking. Unit is pixel clock. **Note**: This bit field be used for dvp hsync and sony mode.	RW

4.5.2.15 VIC_VLD_LINE_SAV Register (VIC_VLD_LINE_SAV,0x060)

The VIC_VLD_LINE_SAV register is used to configure the valid line sav for dvp sony mode .

	VIC_VLD_LINE_SAV																VIC_BA+0x060														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								vic_vld_line_sav																							
RST	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	vic_vld_line_sav	The valid line sav for dvp sony mode , default 0x800800	R

4.5.2.16 VIC_VLD_LINE_EAV Register (VIC_VLD_LINE_EAV,0x064)

The VIC_VLD_LINE_EAV register is used to configure the valid line eav for dvp sony mode .

	VIC_VLD_LINE_EAV																VIC_BA+0x064															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								vic_vld_line_eav																							
RST	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	1	0	0	0	0	1	0	0	1	1	1	0	1	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	vic_vld_line_eav	The valid line eav for dvp sony mode , default 0x9D09D0	R

4.5.2.17 VIC_VLD_FRM_SAV Register (VIC_VLD_FRM_SAV,0x070)

The VIC_VLD_FRM_SAV register is used to configure valid vertical resolution for dvp mode .

	VIC_VLD_FRM_SAV																VIC_BA+0x070															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								vic_vld_frm_sav																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	vic_vld_frm_sav	Now just use dvp_img_chk == 1. Check whether the valid and invalid lines of an image are set values	RW

4.5.2.18 VIC_VLD_FRM_EAV Register (VIC_VLD_FRM_EAV,0x074)

The VIC_VLD_FRM_EAV register is used to configure valid horizon resolution for dvp mode .

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	VIC_VLD_FRM_EAV																VIC_BA+0x074															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								vic_vld_frm_eav																								
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:0	vic_vld_frm_eav	Now just use dvp_img_chk == 1. Check whether the valid and invalid pixel an line are set values	RW

4.5.2.19 VIC_VC_CONTROL Register (VIC_VC_CONTROL_FSM,0x08C)

View the current vic working condition.

	VIC_VC_CONTROL_FSM																VIC_BA+0x08C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								vc_control_fsm							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:6	Reserved	Writing has no effect, read as zero.	R
6:0	vc_control_fsm	Vic output FSM. If is value 0, VIC is not en. If is value same 1, is not have data or fid. 0x00: IDLE 0x01: CHECK 0x02: VSYNC POS 0x04: VSYNC DELAY 0x08: HSYNC VALID 0x0C: HSYNC DELAY 0x10: VSYNC NEG 0x20: VSYNC DELAY	R

4.5.2.20 VIC_VC_CONTROL_CH0_PIX Register (VIC_VC_CH0_PIXEL,0x090)

View the current channel 0 send which one pixel

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	VIC_VC_CH0_PIXEL																VIC_BA+0x090														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																vc_ch0_pixel														
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	vc_ch0_pixel	View the current channel 0 send which one pixel	R

4.5.2.21 VIC_VC_CONTROL_CH0_LINE Register (VIC_VC_CH0_LINE,0x0A0)

View the current channel 0 send which one line

	VIC_VC_CH0_LINE																VIC_BA+0x0A0														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																vc_ch0_line														
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	vc_ch0_line	View the current channel 0 send which one line	R

4.5.2.22 VIC_VC_CONTROL_FIFO_USE Register (VIC_VC_FIFO_USE,0x0B0)

View the current number of valid data in the buff

	VIC_VC_FIFO_USE																VIC_BA+0x0B0)														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																vs_syfifo_valid	Reserved			vc_syfifo_use										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect, read as zero.	R
15	vc_syfifo_valid	Send data number valid	R
14:12	Reserved	Writing has no effect, read as zero.	R
11:0	vc_syfifo_use	Valid data number (unit double pixel)	R

4.5.2.23 VIC_CB_1ST Register (VIC_CB_1ST,0x0C0)

The VIC_CB_1ST register is used to configure the first color bar's YUV

	VIC_CB_1ST																VIC_BA+0x0C0													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								y_ value								cb_ value								cr_value							
RST	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect. Read as zero.	R
23:16	y_value	Y component value	RW
15:8	cb_value	Cb component value	RW
7:0	cr_ value	Cr component value	RW

4.5.2.24 VIC_CB_2ND Register (VIC_CB_2ND,0x0C4)

The VIC_CB_2ND register is used to configure the second color bar's YUV.

	VIC_CB_2ND																VIC_BA+0x0C4													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								y_ value								cb_ value								cr_ value							
RST	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect. Read as zero.	R
23:16	y_value	y component value	RW
15:8	cb_value	cb component value	RW
7:0	cr_value	cr component value	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4.5.2.25 VIC_CB_3RD Register (VIC_CB_3RD,0x0C8)

The VIC_CB_3RD register is used to configure the third color bar's YUV .

	VIC_CB_3RD																VIC_BA+0x0C8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								y_value								cb_ value								cr_ value							
RST	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	0	0	0	0	0	1	1	0	1	1	1	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect. Read as zero.	R
23:16	y_value	y component value	RW
15:8	cb_value	cb component value	RW
7:0	cr_value	cr component value	RW

4.5.2.26 VIC_CB_4TH Register (VIC_CB_4TH,0x0CC)

The VIC_CB_4TH register is used to configure the fourth color bar's YUV

	VIC_CB_4TH																VIC_BA+0x0CC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								y_value								cb_ value								cr_ value							
RST	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	1	0	0	0	0	1	1	0	1	0	1	1	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	y_value	y component value	RW
15:8	cb_value	cb component value	RW
7:0	cr_value	cr component value	RW

4.5.2.27 VIC_CB_5TH Register (VIC_CB_5TH,0x0D0)

The VIC_CB_5TH register is used to configure the fifth color bar's YUV

	VIC_CB_5TH																VIC_BA+0x0D0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								y_ value								cb_ value								cr_ value							

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	1	1	1	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	y_value	y component value	RW
15:8	cb_value	cb component value	RW
7:0	cr_value	cr component value	RW

4.5.2.28 VIC_CB_6TH Register (VIC_CB_6TH,0x0D4)

The VIC_CB_6TH register is used to configure the sixth color bar's YUV

	VIC_CB_6TH																VIC_BA+0x0D4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								y__value								cb_value								cr_value							
RST	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	y_value	Y component value	RW
15:8	cb_value	Cb component value	RW
7:0	cr_value	Cr component value	RW

4.5.2.29 VIC_CB_7TH Register (VIC_CB_7TH,0x0D8)

The VIC_CB_7TH register is used to configure the seventh color bar's YUV.

	VIC_SEVENTH_CB																VIC_BA+0x0D8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								y_value								cb_value								cr_value							
RST	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	1	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	y_value	y component value	RW
15:8	cb_value	cb component value	RW
7:0	cr_value	cr component value	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4.5.2.30 VIC_CB_8TH Register (VIC_CB_8TH,0x0DC)

The VIC_CB_8TH register is used to configure the eighth color bar's YUV.

	VIC_CB_8TH																VIC_BA+0x0DC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								y_value								cb_value								cr_value							
RST	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1	1	0	0	1	0	1	0	1	1	0	1	1	1	1	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	y_value	y component value	RW
15:8	cb_value	cb component value	RW
7:0	cr_value	cr component value	RW

4.5.2.31 VIC_CB2_1ST Register (VIC_CB2_1ST,0x0E0)

The VIC_CB2_1ST register is used to configure the first color bar's RAW line2

	VIC_CB2_1ST																VIC_BA+0x0E0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								raw21_value												raw22_value											
RST	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:12	raw21_value	line2 first raw value	RW
11:0	raw22_value	line2 second raw value	RW

4.5.2.32 VIC_CB2_2ND Register (VIC_CB2_2ND,0x0E4)

The VIC_CB2_2ND register is used to configure the second color bar's RAW line2

	VIC_CB2_2ND																VIC_BA+0x0E4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved								raw21_value												raw22_value											
RST	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:12	raw21_value	line2 first raw value	RW
11:0	raw22_value	line2 second raw value	RW

4.5.2.33 VIC_CB2_3RD Register (VIC_CB2_3RD,0x0E8)

The VIC_CB2_3RD register is used to configure the third color bar's RAW.

	VIC_CB2_3RD																VIC_BA+0x0E8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved								raw21_value								raw22_value															
RST	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	0	0	0	0	0	1	1	0	1	1	1	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:12	raw21_value	line2 first raw value	RW
11:0	raw22_value	line2 second raw value	RW

4.5.2.34 VIC_CB2_4TH Register (VIC_CB2_4TH,0x0EC)

The VIC_CB2_4TH register is used to configure the fourth color bar's YUV

	VIC_CB2																VIC_BA+0x0EC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								raw21_value								raw22_value															
RST	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	1	0	0	0	0	1	1	0	1	0	1	1	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:12	raw21_value	line2 first raw value	RW
11:0	raw22_value	line2 second raw value	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4.5.2.35 VIC_CB2_5TH Register (VIC_CB2_5TH,0x0F0)

The VIC_CB2_5TH register is used to configure the fifth color bar's RAW.

	VIC_CB2_5TH																VIC_BA+0x0F0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								raw21_value								raw22_value															
RST	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	1	1	1	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:12	raw21_value	line2 first raw value	RW
11:0	raw22_value	line2 second raw value	RW

4.5.2.36 VIC_CB2_6TH Register (VIC_CB2_6TH,0x0F4)

The VIC_CB2_6TH register is used to configure the sixth color bar's YUV

	VIC_CB2_6TH																VIC_BA+0x0F4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								raw21_value								raw22_value															
RST	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:12	raw21_value	line2 first raw value	RW
11:0	raw22_value	line2 second raw value	RW

4.5.2.37 VIC_CB2_7TH Register (VIC_CB2_7TH,0x0F8)

The VIC_CB2_7TH register is used to configure the seventh color bar's RAW.

	VIC_CB2_7TH																VIC_BA+0x0F8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved	raw21_value	raw22_value
RST	0 0 0 0 0 0 0 0	1 1 0 1 0 0 1 0 0 0 0 1	0 0 0 0 1 0 0 1 0 0 1 0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero.	R
23:12	raw21_value	line2 first raw value	RW
11:0	raw22_value	line2 second raw value	RW

4.5.2.38 VIC_CB2_8TH Register (VIC_CB2_8TH,0x0FC)

The VIC_CB2_8TH register is used to configure the eighth color bar's RAW.

	VIC_CB2_8TH																VIC_BA+0x0FC												
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								raw21_value								raw22_value														
RST	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1	1	0	0	1	0	1	0	1	1	0	1	1	1	1	0

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect. Read as zero.	R
23:12	raw21_value	line2 first raw value	RW
11:0	raw22_value	line2 second raw value	RW

4.5.2.39 MIPI_ALL_WIDTH_4BYTE (MIPI_ALL_WIDTH_4BYTE,0x100)

	MIPI_ALL_WIDTH_4BYTE																VIC_BA+0x100															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																image_all_width_4byte															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Read as zero.	
15:0	image_all_width_4byte	mipi control output line , need have 4byte number.	RW

If one line have 640 valid pixel, line before have invalid pixel 8, line after have invalid pixel 10.
image format is raw10.

(640 + 8 + 10)* 10 / 32 = 205.625, the reg value is 206

image format is raw8

(640 + 8 + 10)* 8 / 32 = 164.5, the reg value is 165

image format is raw12

(640 + 8 + 10)* 12 / 32 = 246.75, the reg value is 247

4.5.2.40 MIPI_VCROP_DEL01 (MIPI_VCROP_DEL01,0x104)

	MIPI_VCROP_DEL01																VIC_BA+0x104															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																vcrop_del0																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect. Read as zero.	R
15:0	vcrop_del0	Line crop, channel 1 effective before the number of rows should be removed.	RW

4.5.2.41 MIPI_SENSOR_CONTROL (MIPI_SENSOR_CONTROL,0x10C)

	MIPI_SENSOR_CONTROL																VIC_BA+0x10C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							mipi_vcomp_en	mipi_hcomp_en	line_sync_mode	work_start_flag	Reserved	data_type_en	data_type_value									del_start	Reserved										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:25	Reserved	Writing has no effect. Read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

24	mipi_vcomp_en	Frame completion can make Only hcomp open to open , and can only open in the defualt mode. If the lack of a few lines of a frame, will be completion.s	RW
23	mipi_hcomp_en	MIPI Interception and completion function can mark. Open automatically after the completion of the number of lines, remove most of the line.	RW
22	line_sync_mode	Sync mode 0: long packet sync mode (In general, choose the pattern) 1: sort packet sync mode	RW
21:20	work_start_flag	Base channel fix 0	RW
18	data_type_en	mipi data type filter en (recommended to open) 0: filtering 1: No filtering	RW
17:12	data_type_value	mipi data type filter 0x1E: YUV422 8bit 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 **Note:** The above types for reference, specific should see the sensor spec	RW
11:8	del_start	Each channel after the start of the number of rows (0-15) **Note:** Under normal circumstances if sony sensor the value is 1, other the value is 0	RW
7:0	Reserved	Writing has no effect. Read as zero.	R

4.5.2.42 MIPI_HCROP_CH0(MIPI_HCROP_CH0,0x110)

	MIPI_HCROP_CH0																VIC_BA+0x110															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	all_image_width																hcrop_del_start_pixel															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	all_image_width	In line have valid and invalid pixel sum	RW
15:0	hcrop_del_start_pixel	Channel 0, one line have before invalid pixel number.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4.5.2.43 MIPI_VCROP_SHADOW_CFG(MIPI_VCROP_SHADOW_CFG,0x120)

	MIPI_VCROP_SHADOW_CFG																VIC_BA+0x120															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											vcrop_del_cfg_e		vcrop_shadow_num		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:5	Reserved	Writing has no effect. Read as zero.	R
4	vcrop_del_cfg_en	Vcrop configuration information valid [4]: channel 0 new configuration valid	R
3:0	vcrop_shadow_num	Vcrop configuration informatino to take effect after a few frames (0-15) 0: next frame valid 1: double next frame valid	RW

4.5.2.44 VC_CONTROL_LIMIT (VC_CONTROL_LIMIT,0x1A0)

The reg to control vic output time.

	VC_CONTROL_LIMIT																VIC_BA+0x1A0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	vc_control_limit_en	vc_control_max_limit															vc_control_vdeleyn															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	vc_control_limit_en	limit function enable bit	RW
30:16	vc_control_max_limit	limit value to output fifo start depth	RW
15:0	vc_control_vdeleyn	output time vsync low min time	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4.5.2.45 VC_CONTROL_DELEY (VC_CONTROL_DELEY,0x1A4)

Control vic output timing interval..

	VC_CONTROL_DELEY																VIC_BA+0x1A4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	vc_hdeley																vc_vdeley															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	vc_hdeley	Output row to delay 1.The line and the time delay between cycles 2.The last line and vsync down time.	RW
15:0	vc_vdeley	In the first line of hsync vsync effective and valid clock cycles	RW

4.5.2.46 VC_CONTROL_TIZIANO_ROUTE(VC_CONTROL_TIZIANO_ROUTE,0x1A8)

With tiziano channel exchange and discarded.

	VC_CONTROL_TIZANO_ROUTE																VIC_BA+0x1A8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															tiziano_route_vc0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect. Read as zero.	R
0	tiziano_route_vc0	Output to tiziano channel 0	RW

4.5.2.47 VC_CONTROL_DMA_ROUTE(VC_CONTROL_DMA_ROUTE,0x1B0)

With dma channel exchange and discarded.

	VC_CONTROL_DMA_ROUTE																VIC_BA+0x1B0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															dma_out
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect. Read as zero.	R
0	dma_out	Current data which is output to the dma channel, each bit said output can make the corresponding channel output.	RW

4.5.2.48 VIC_INT_STATU Register(VIC_INT_STA,0x1E0)

The VIC_INT_STA register is used to indicate the vic's source.

	VIC_INT_STA																VIC_BA+0x1E0														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved														if_scaler_ch2_done	if_scaler_ch1_done	if_scaler_ch0_done	if_vic_done	dvp_hcomp_err	mipi_vcomp_err_ch0	mipi_hcomp_err_ch0	image_syfifo_ovf	vc_output_limit_err	dma_syfifo_ovf	dma_frame_done	hvf_err	ver_err_ch0	hor_err_ch0	asfifo_data_ovf	frame_rst	frame_start_ch0	frame_done_ch0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:18	Reserved	Writing has no effect. Read as zero.	R
17	if_scaler_ch2_done	tiziano ch2 out frame info done	R
16	if_scaler_ch1_done	tiziano ch1 out frame info done	R
15	if_scaler_ch0_done	tiziano(isp) ch0 out frame info done	R
14	if_vic_done	vic done out frame info done	R
13	dvp_hcomp_err	Dvp hcomp err	R
12	mipi_vcomp_err_ch0	Mipi channel 0 vcomp err	R
11	mipi_hcomp_err_ch0	Mipi channel 0 hcomp err	R
10	image_syfifo_ovf	Image line buff ovf	R
9	vc_output_limit_err	Image output limit too small	R
8	dma_syfifo_ovf	image dma out ovf	R
7	dma_frame_done	vic image dma done	R
6	hvf_err	DVP/BT SAV or EAV err	R
5	ver_err_ch0	Channel 0 height error	R
4	hor_err_ch0	Channel 0 width error	R
3	asfifo_data_ovf	Image asynchronous data fifo ovf	R
2	frame_rst	Frame reset	R
1	frame_start_ch0	Channel 0 frame start	R
0	frame_done_ch0	Channel 0 frame done	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4.5.2.49 VIC_INT_MASK Register(VIC_INT_MASK,0x1E8)

The VIC_INT_MSK register is used to indicate the vic's source.

	VIC_INT_MSK																VIC_BA+0x1E8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved														if_scaler_ch2_done_mask	if_scaler_ch1_done_mask	if_scaler_ch0_done_mask	if_vic_done_mask	dvp_hcomp_err_mask	mipi_vcomp_err_ch0_mask	mipi_hcomp_err_ch0_mask	image_syfifo_ovf_mask	vc_output_limit_err_mask	dma_syfifo_ovf_mask	dma_frame_done_mask	hvf_err_mask	ver_err_ch0_mask	hor_err_ch0_mask	asfifo_data_ovf_mask	frame_rst_mask	frame_start_ch0_mask	frame_done_ch0_mask
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:18	Reserved	Writing has no effect. Read as zero.	RW
17	if_scaler_ch2_done_mask	tiziano ch2 out frame info done mask	RW
16	if_scaler_ch1_done_mask	tiziano ch1 out frame info done mask	RW
15	if_scaler_ch0_done_mask	tiziano(isp) ch0 out frame info done mask	RW
14	if_vic_done_mask	vic done out frame info done mask	RW
13	dvp_hcomp_err_mask	Dvp hcomp err mask	RW
12	mipi_vcomp_err_ch0_mask	Mipi channel 0 vcomp err mask	RW
11	mipi_hcomp_err_ch0_mask	Mipi channel 0 hcomp err mask	RW
10	image_syfifo_ovf_mask	Image line buff ovf mask	RW
9	vc_output_limit_err_mask	Image output limit too small mask	RW
8	dma_syfifo_ovf_mask	image dma out ovf mask	RW
7	dma_frame_done_mask	vic image dma done mask	RW
6	hvf_err_mask	DVP/BT SAV or EAV err mask	RW
5	ver_err_ch0_mask	Channel 0 height error mask	RW
4	hor_err_ch0_mask	Channel 0 width error mask	RW
3	asfifo_data_ovf_mask	Image asynchronous data fifo ovf mask	RW
2	frame_rst_mask	Frame reset mask	RW
1	frame_start_ch0_mask	Channel 0 frame start mask	RW
0	frame_done_ch0_mask	Channel 0 frame done mask	RW

4.5.2.50 VIC_INT_CLEAR Register(VIC_INT_CLEAR,0x1F0)

The VIC_INT_CLR register is used to indicate the vic's source.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	VIC_INT_CLR																VIC_BA+0x1F0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	Reserved														if_scaler_ch2_done_clr	if_scaler_ch1_done_clr	if_scaler_ch0_done_clr	if_vic_done_clr	dvp_hcomp_err_clr	mipi_vcomp_err_ch0_clr	mipi_hcomp_err_ch0_clr	image_syfifo_ovf_clr	vc_output_limit_err_clr	dma_syfifo_ovf_clr	dma_frame_done_clr	hvf_err_clr	ver_err_ch0_clr	hor_err_ch0_clr	asfifo_data_ovf_clr	frame_rst_clr	frame_start_ch0_clr	frame_done_ch0_clr
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:18	Reserved	Writing has no effect. Read as zero.	W
17	if_scaler_ch2_done_clr	tiziano ch2 out frame info done clear	W
16	if_scaler_ch1_done_clr	tiziano ch1 out frame info done clear	W
15	if_scaler_ch0_done_clr	tiziano(isp) ch0 out frame info done clear	W
14	if_vic_done_clr	vic done out frame info done clear	W
13	dvp_hcomp_err_clr	Dvp hcomp err clear	W
12	mipi_vcomp_err_ch0_clr	Mipi channel 0 vcomp err clear	W
11	mipi_hcomp_err_ch0_clr	Mipi channel 0 hcomp err clear	W
10	image_syfifo_ovf_clr	Image line buff ovf clear	W
9	vc_output_limit_err_clr	Image output limit too small clear	W
8	dma_syfifo_ovf_clr	image dma out ovf clear	W
7	dma_frame_done_clr	vic image dma done clear	W
6	hvf_err_clr	DVP/BT SAV or EAV err clear	W
5	ver_err_ch0_clr	Channel 0 height error clear	W
4	hor_err_ch0_clr	Channel 0 width error clear	W
3	asfifo_data_ovf_clr	Image asynchronous data fifo ovf clear	W
2	frame_rst_clr	Frame reset clear	W
1	frame_start_ch0_clr	Channel 0 frame start clear	W
0	frame_done_ch0_clr	Channel 0 frame done clear	W

4.5.3 DMA registers

Table 4-1 DMA Registers Map

Name	RW	Reset Value	Address Offset	Access Size
DMA_CONFIGURE	RW	0x0000_0000	0x300	32
DMA_RESOLUTION	RW	0x0000_0000	0x304	32
DMA_RESET	RW	0x0000_0000	0x308	32
DMA_Y_CH_LINE_STRIDE	RW	0x0000_0000	0x314	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

DMA_Y_CH_BUF0_ADDR	RW	0x0000_0000	0x318	32
DMA_Y_CH_BUF1_ADDR	RW	0x0000_0000	0x31C	32
DMA_Y_CH_BUF2_ADDR	RW	0x0000_0000	0x320	32
DMA_Y_CH_BUF3_ADDR	RW	0x0000_0000	0x324	32
DMA_Y_CH_BUF4_ADDR	RW	0x0000_0000	0x328	32
DMA_UV_CH_STRIDE	RW	0x0000_0000	0x334	32
DMA_UV_CH_BUF0_ADDR	RW	0x0000_0000	0x338	32
DMA_UV_CH_BUF1_ADDR	RW	0x0000_0000	0x33C	32
DMA_UV_CH_BUF2_ADDR	RW	0x0000_0000	0x340	32
DMA_UV_CH_BUF3_ADDR	RW	0x0000_0000	0x344	32
DMA_UV_CH_BUF4_ADDR	RW	0x0000_0000	0x348	32

4.5.3.1 DMA Configure Register(DMA_CONFIGURE,0x300)

The DMA_CONFIGURE register is used to control the DMA.

	DMA_CONFIGURE																														
																	DMA_BA+0x300														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	dma en	Reserved																					yuv422_order		Reserved	buffer_number				base_mode		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	dma en	enable DMA	RW
30:8	Reserved	Writing has no effect, read as zero.	R
9:8	yuv422_order	The order in ddr ram for YUV422 packet(base_mode=3) 0: Y2V1Y1U1 1: Y1U1Y2V1 2: V1Y2U1Y1 3: U1Y1V1Y2	RW
7	Reserved	Writing has no effect, read as zero.	R
6:3	Buffer_number	Output buffer number. Value(0~4) is actual buffer number(1~5) minus 1.	RW
2:0	base_mode	DMA output data format. 0: RAW8/10/12(16bits in DDR) 6: NV12 7: NV21	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4.5.3.2 DMA Resolution Register (DMA_RESOLUTION,0x304)

The DMA_RES register is used to configure the resolution of image.

	DMA_RESOLUTION																DMA_BA+0x304															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HORIZONTAL_RESOLUTION																VERTICAL_RESOLUTION															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	HORIZONTAL_ RESOLUTION	The Horizontal Size of resolution, maximum horizontal size of a frame is 2048 because of the maximum horizontal of TIZIANO is 2048.	RW
15:0	VERTICAL_ RESOLUTION	The Vertical Size of resolution, the maximum vertical size of a frame is 2048.	RW

4.5.3.3 DMA RESET Register (DMA_RESET,0x308)

The DMA_RESET register is used to enable and disable DMA.

	DMA_RESET																DMA_BA+0x308															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															DMA_RESET
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero. As default,please setting these bits 0.	R
0	DMA _RESET	When this bit is set to 1，the DMA will be reset immediately.	RW

4.5.3.4 DMA Y Channel Line Stride Register (DMA_Y_CH_STRIDE,0x314)

The DMA_Y_CH_STRIDE register is used to gate the line stride for y channel buffer.

	DMA_Y_CH_STRIDE																DMA_BA+0x314															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_Y_CH_STRIDE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:0	DMA_Y_CH_STRIDE	the line stride for y channel buffer.unit is byte.	RW

4.5.3.5 DMA Y Channel Buffer0 Address Register (DMA_Y_CH_BUF0_ADDR,0x318)

The DMA_Y_CH_BUF0 register is used to configure the Y channel buffer0 address.

	DMA_Y_CH_BUF0_ADDR																DMA_BA+0x318															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_Y_CH_BUF0_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_Y_CH_BUF0_ADDR	the Y channel buffer0 address.unit is byte.	RW

4.5.3.6 DMA Y Channel Buffer1 Address Register (DMA_Y_CH_BUF1_ADDR,0x31C)

The DMA_Y_CH_BUF1 register is used to configure the Y channel buffer1 address.

	DMA_Y_CH_BUF1_ADDR																DMA_BA+0x31C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_Y_CH_BUF1_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_Y_CH_BUF1_ADDR	the Y channel buffer1 address.unit is byte.	RW

4.5.3.7 DMA Y Channel Buffer2 Address Register (DMA_Y_CH_BUF2_ADDR,0x320)

The DMA_Y_CH_BUF2 register is used to configure the Y channel buffer2 address.

	DMA_Y_CH_BUF2_ADDR																DMA_BA+0x320															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_Y_CH_BUF2_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:0	DMA_Y_CH_BUF2_ADDR	the Y channel buffer2 address.unit is byte.	RW

4.5.3.8 DMA Y Channel Buffer3 Address Register (DMA_Y_CH_BUF3_ADDR,0x324)

The DMA_Y_CH_BUF3 register is used to configure the Y channel buffer3 address.

	DMA_Y_CH_BUF3_ADDR																DMA_BA+0x324															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_Y_CH_BUF3_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_Y_CH_BUF3_ADDR	the Y channel buffer3 address.unit is byte.	RW

4.5.3.9 DMA Y Channel Buffer4 Address Register (DMA_Y_CH_BUF4_ADDR,0x328)

The DMA_Y_CH_BUF4 register is used to configure the Y channel buffer4 address.

	DMA_Y_CH_BUF4_ADDR																DMA_BA+0x328															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_Y_CH_BUF4_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_Y_CH_BUF4_ADDR	the Y channel buffer4 address.unit is byte.	RW

4.5.3.10 DMA UV Channel Line Stride Register (DMA_UV_CH_STRIDE,0x334)

The DMA_UV_CH_STRIDE register is used to gate the line stride for y channel buffer.

	DMA_UV_CH_STRIDE																DMA_BA+0x334															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_UV_CH_STRIDE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:0	DMA_UV_CH_STRIDE	the line stride for y channel buffer.unit is byte.	RW

4.5.3.11 DMA UV Channel Buffer0 Address Register (DMA_UV_CH_BUF0_ADDR,0x338)

The DMA_UV_CH_BUF0 register is used to configure the UV channel buffer0 address.

	DMA_UV_CH_BUF0_ADDR																DMA_BA+0x338															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_UV_CH_BUF0_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_UV_CH_BUF0_ADDR	the UV channel buffer0 address.unit is byte.	RW

4.5.3.12 DMA UV Channel Buffer1 Address Register (DMA_UV_CH_BUF1_ADDR,0x33C)

The DMA_UV_CH_BUF1 register is used to configure the UV channel buffer1 address.

	DMA_UV_CH_BUF1_ADDR																DMA_BA+0x33C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_UV_CH_BUF1_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_UV_CH_BUF1_ADDR	the UV channel buffer1 address.unit is byte.	RW

4.5.3.13 DMA UV Channel Buffer2 Address Register (DMA_UV_CH_BUF2_ADDR,0x340)

The DMA_UV_CH_BUF2 register is used to configure the UV channel buffer2 address.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	DMA_UV_CH_BUF2_ADDR																DMA_BA+0x340															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_UV_CH_BUF2_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_UV_CH_BUF2_ADDR	the UV channel buffer2 address.unit is byte.	RW

4.5.3.14 DMA UV Channel Buffer3 Address Register (DMA_UV_CH_BUF3_ADDR,0x344)

The DMA_UV_CH_BUF3 register is used to configure the UV channel buffer3 address.

	DMA_UV_CH_BUF3_ADDR																DMA_BA+0x344															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_UV_CH_BUF3_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DMA_UV_CH_BUF3_ ADDR	the UV channel buffer3 address.unit is byte.	RW

4.5.3.15 DMA UV Channel Buffer4 Address Register (DMA_UV_CH_BUF4_ADDR,0x348)

The DMA_UV_CH_BUF4 register is used to configure the UV channel buffer4 address.

	DMA_UV_CH_BUF4_ADDR																DMA_BA+0x348															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_UV_CH_BUF4_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:0	DMA_UV_CH_BUF4_ADDR	the UV channel buffer4 address.unit is byte.	RW

4.6 Operation Flow

4.6.1 Overview

The image system start up operation flow is described in Figure 4-6

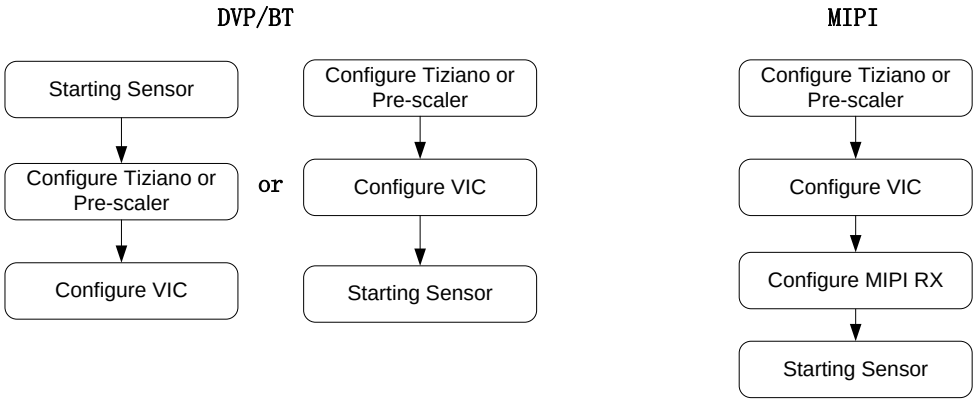


Figure 4-6 Image system start up Operation Flow

The start up steps are as follows:

In DVP or BT input interface, vic can the sensor start after the start.

1.Configure TIZIANO(ISP in figure above) Pipeline to star the working state.

2.Configure VIC.

3.Starting Sensor.

or

1.Starting Sensor.

2.Configure TIZIANO(ISP in figure above) Pipeline to star the working state.

3.Configure VIC.

In MIPI input interface.

1.Configure TIZIANO(ISP in figure above) Pipeline to star the working state.

2.Configure VIC.

3.Configure MIPI TX.

4.Starting Sensor.

The system shut down operation flow is described in Figure 4-7

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

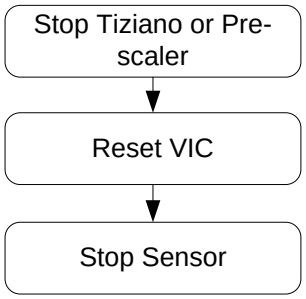


Figure 4-7 System Shut Down Operation Flow

4.6.2 Configure VIC

4.6.2.1 Image mode

a) VIC_INPUT_INTF:
   1) Select the input interface(0x00C)
   2) if interface is dvp/bt, VIC_INPUT_DVP should be configure(0x010)
   3) if interface is MIPI, VIC_IN_CSI_FMT should be configure(0x014)

b) Interface configure

   VIC_INPUT_DVP: the following bit field should be configured
   1) vsyn_polar
   2) hsyn_polar
   3) dvp_timing_mode
   4) dvp_data_type
   5) dvp_raw_alignment (this bit need only configure when input data is raw8/10/12)
   6) yuv_data_order (this bit need only configure when input data is yuv422)

   BT656:

   the following bit field should be configured of VIC_INPUT_DVP
   1) bt_sav_eav
   2) yuv422_order
   3) start_field
   4) interlace_en

   BT1120:

   the following bit field should be configured of VIC_INPUT_DVP
   1) bt_intf_wide
   2) bt_sav_eav
   3) yuv422_order
   4) start_field
   5) interlace_en

   BT601(CEA-801):

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

1) bt601_ mode
2) bt_intf_wide
3) yuv422_order
4) start_field
5) interlace_en
6) vsyn_polar
7) hsyn_polar

MIPI:

1) MIPI_ALL_WIDTH_4BYTE(0x100)
2) MIPI_VCROP_DEL(0x104,0x108)
3) MIPI_SENSOR_CONTROL(0x10C)
4) MIPI_HCROP_CH(0x110,0x114,0x118,0x11C)

b) VIC_INPUT_HPARA0 (this reg need configure when dvp is hsync or sony mode)
c) VIC_INPUT_VPARA3 (this reg need configure when dvp is hsync or sony mode)
1.when dvp hsync mode, configure VIC_INPUT_VPARA3[31:0], unit is pixel clock
2.when dvp sony mode, configure VIC_INPUT_VPARA3[15:0], unit is line.
d) VIC_RESOLUTION (0x04)
e) VIC_OUTPUT.
1) VC_CONTROL_CONTROL(0x1A0)
2) VC_CONTROL_DELEY(0x1A4)
3) VC_CONTROL_TIZIANO_ROUTE(0x1A8)
4) VC_CONTROL_DMA_ROUTE(0x1B0)
f) Write VIC_CONTROL 0x02, then read it until be 0.
g) Write 0x01 to control register to start VIC.

4.6.2.2 Back Color Bar Mode

Back Color bar is after VIC's asynchronous fifo，and support 8 color bars in one frame，each frame color can be configure。

a) configure bar's color value ,please refer tables as below.
b) configure back color bar blanking reg(0x2C);
c) configure back color bar control reg(0x28);
d) configure control register to start VIC.

RAW(RGGB)	black	white	red	green	blue	yellow	purple	cyan
0xC0~0xDC	0x000000	0xFFFFFF	0x000FFF	0xFFF000	0x000000	0xFFFFFF	0x0007FF	0xFFF000
0xE0~0xFC	0x000000	0xFFFFFF	0x000000	0x000FFF	0xFFF000	0x000FFF	0x7FF000	0xFFFFFF

RGB888	black	white	red	green	blue	yellow	purple	cyan
0xC0~0xDC	0x000000	0xFFFFFF	0xFF0000	0x00FF00	0x0000FF	0xFFFF00	0x800080	0x00FFFF
0xE0~0xFC	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4.7 Index

Table 4-2 Description of Proprietary Vocabulary

Name	Description
3A	Auto focus, Auto exposure, Auto white balance
AXI	Advanced Extensible Interface
TIZIANO	Image Signal Processor
LUT	Look Up Table
MSB	Most Significant Bit
VIC	Video Input Controller
WDR/HDR	Wide/High Dynamic Range

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Section 3

IMAGE CORE

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

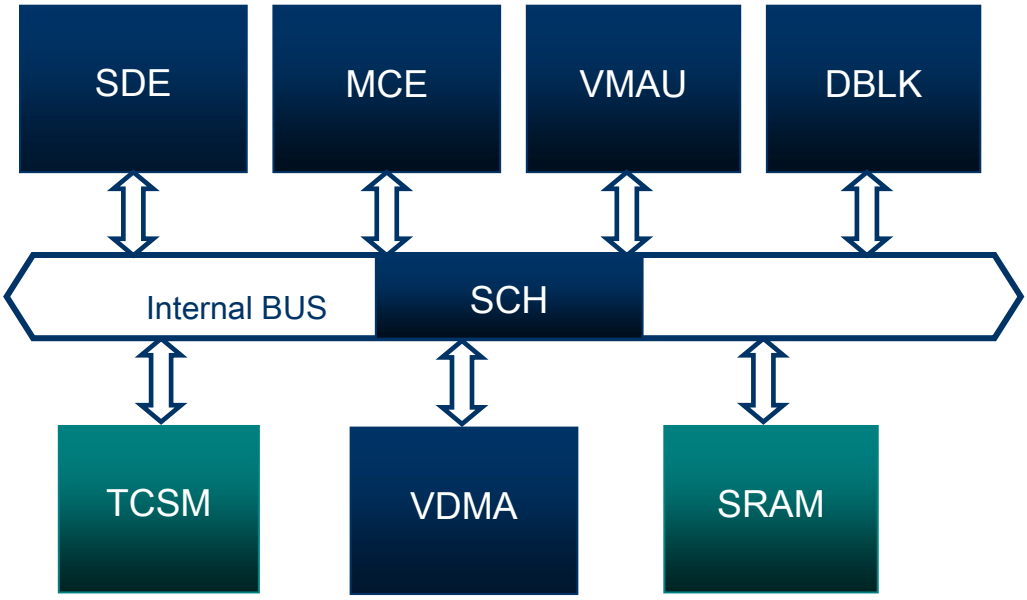
5 Felix

5.1 Overview

FELIX is the name of H264 decoder in this chip. FELIX embeds application specified hardware accelerators for common video decompress algorithms, which includes Stream Parser, Motion Compensation, Inverse Quant, Inverse DCT and De-block engines. Also a scheduler named SCH is embedded to manage the whole control and data flow.

Performance of FELIX in the chip:
H.264 decoding up to 1080P 30fps

5.1.1 Block Diagram



5.1.2 Features of FELIX

Table 5-1 FELIX Features

Item	Features
General Purpose DMA(VDMA)	Descriptor based DMA self automatic configure supported
Parser (SDE)	Parser is a bit-stream engine (named as SDE) in FELIX H.264 Context adaptive binary arithmetic (CABAC) decoding support, PCM not supported H.264 Context adaptive variable length (CAVLC) decoding support,

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	PCM not supported
Motion (MC)	Motion compensation **Reference data cache embed** **Descriptor based task fetching** Programmable processing size from 2x2 to 16x16 (in estimation the size is from 4x4 to 16x16) Programmable interplation filter from 2-tap to 8-tap Programmable sub-pixel accuracy from 1/2-pixel to 1/8-pixel Interlaced mode support Intensity compensation support Weighted prediction support **A**utomatic rotation support for rotated referenced pictures Automatic expanding support for outside frame's refe**rence**
Recover (VMAU)	Recover is a Matrix Arithmetic Unit(named as VMAU), it serves for pixel's recovery and reconstruction during video decoding. Descriptor based task fetching Configurable format intra prediction support Configurable format Inverse quant support Configurable format IDCT support Residual add for pixel's recovery
Deblock (DBLK)	Descriptor based task fetching H.264 in loop filter support, FMO/MBAFF not supported tile-based write buffer for DMA out
Scheduler (SCH)	Scheduler is a special unit which is used to manage internel functional engines' handshake. 4 programable channels 2 programable groups
Interrupt control center (INTC)	Task end interrupt (frame/slice end) Bitstream error interrupt VDMA ACFG error interrupt

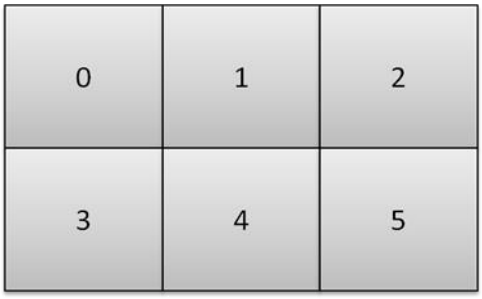
5.1.3 Data Format

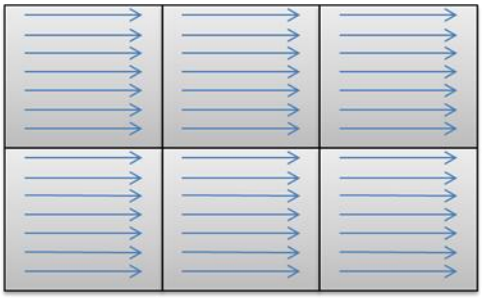
Input data is Bit-Stream to be decoded.

Output data is reconstructed YUV frame. Felix outputs Two separated YUV frame, one for next frame reference, called Tile; one for display, called NV12

Tile format: frame is grouped by 16x16 pixel block, blocks are raster-scan. Pixels inside blocks are raster-scan.

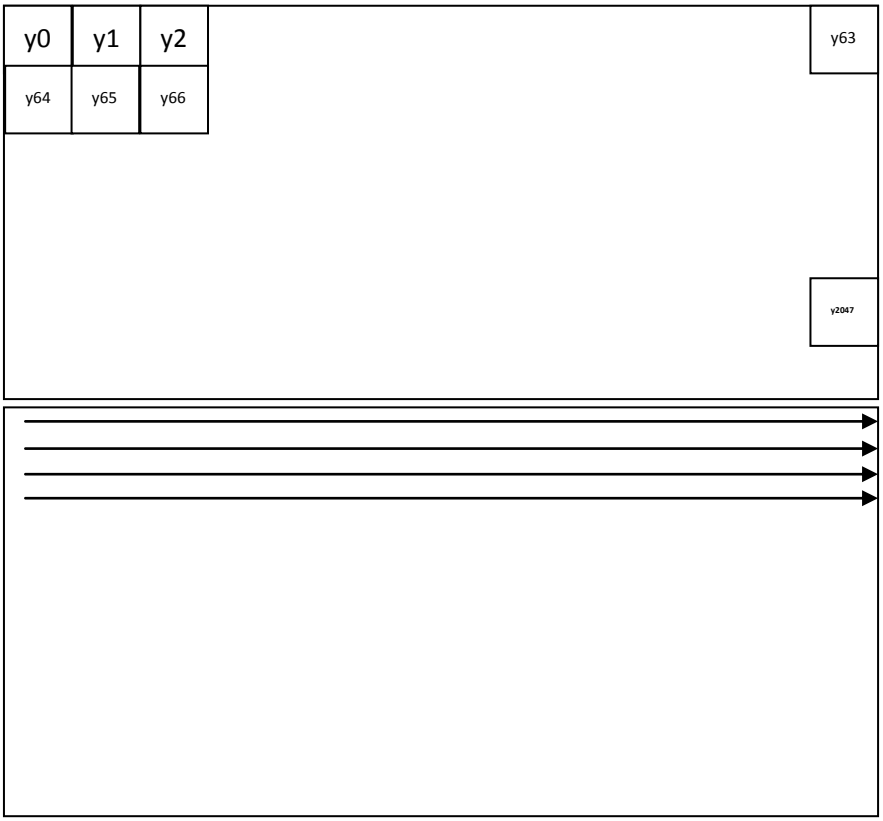
Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.





NV12 format: Pixels are raster-scan inside frame.

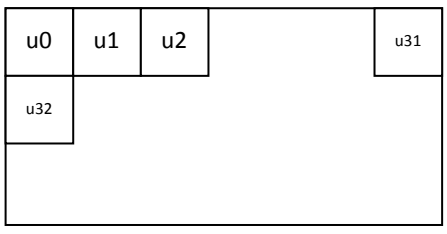
For example, picture size is 64x32,y0,y1,y2...y2047 are pixels name

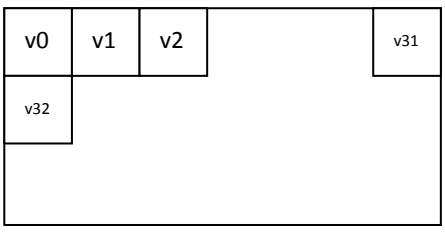


Y pixel order:

y0 -- y1 -- y2 --- ..... ---- y63 --- y64 --- y65 --- y66 ---- ....---- y2047

UV pixel name: u0,u1,u2...v0,v1,v2





Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

UV pixel order:
u0 -- v0 -- u1 --- v1 ---- u2 --- v2 --- ... --- u31 --- v31--- u32 --- v32 --- ...

5.1.4 Internal physical address base definition

Table 5-2 FELIX Internal physical address base definition

Module	Physical address base
SCH	0x1320_0000
VDMA	0x1321_0000
MC	0x1325_0000
DBLK	0x1327_0000
VMAU	0x1328_0000
SDE	0x1329_0000

5.2 VDMA

5.2.1 Overview

VDMA is a general purpose DMA embedded in FELIX. It supports normal data transferring (we named as TRAN mode) between external memory and internal on-chip-memories (TCSM/SRAM) by the operation defined by a descriptor table, furthermore a special mode named as ACFG is used for FELIX self slaver registers or on-chip-memories' automatic configuration according to a descriptor table which defined in the external memory.

TRAN mode descriptor node is composed by 4 words, from the LSB to the MSB is named as TSI, TDI, DMY and TCI. Their details are defined as:

Bits	Name	Description
TSI: Transfer source information		
31:2	TSA	Transfer source address. In EXT source it should be 32 words aligned. In INN source it can be single word aligned.
1	N/C	Note cared
0	TSL	Transfer source location. 0: INN, indicates the transfer source data located in the internal on-chip-memory (TCSM/SRAM). 1: EXT, indicates the transfer source data located in the external memory.
TDI: Transfer destination information		
31:2	TDA	Transfer destination address.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		In EXT destination it should be 32 words aligned. In INN destination it can be single word aligned.
1	N/C	Not cared
0	TDL	Transfer destination location. 0: INN, indicates the transfer destination located in the internal on-chip-memory (TCSM/SRAM). 1: EXT, indicates the transfer destination located in the external memory.
DMY: dummy		
31:0	DMY	Not cared
TCI: Transfer control information		
31	LK	Node link Set as 1 to indicate the followed node needs to be fetched and executed. Set as 0 to indicated current node is the final task and after current task's transferring VDMA would stop.
30: 10	NC	Not cared
9:0	TSZ	Transfer data size minus 1 (unit: word). From INN to INN, any number between 0 ~ 1023 is legal. From INN to EXT or from EXT to INN, transfer data size should be multiplied by 2. From EXT to EXT, the transfer is illegal.

ACFG mode descriptor node is composed by 2 words, from the LSB to the MSB is named as CVAL and CCTL. Their details are defined as:

Bits	Name	Description
CVAL: Configure value		
31:0	CVAL	The value to be configured into the FELIX registers indicated by CCTL.
CCTL: configure control		
31	CVLD	Only 1 indicates current node is valid, otherwise the VDMA would stop working and ACFG error interrupt would be sent if the relative interrupt enabled in SCH.CFGC.
30	CTMF	Configure terminate flag 0 indicates more node need to be read. 1 indicates current node is final one and VDMA would stop after current configuration's execution.
29:20	NC	Not cared
19:0	CIDX	Configure index Indicates which register should be configured. It should be word aligned.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

5.2.2 Task trigger (TRIG)

	TRIG																												0x8	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DHA																												Reserved		MD	RUN
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0

Bits	Name	Description	RW
31:4	DHA	Descriptor Head Address. For ACFG mode, the descriptor chain must be located in the external memory and should be 32 word aligned. For TRAN mode, the descriptor chain must be located in the on-chip-memory (TCSM/SRAM) and should be 4 word aligned.	RW
3:2	Reserved	Writing has no effect, read as zero.	R
1	MD	VDMA work mode 0: ACFG mode 1: TRAN mode	RW
0	RUN	VDMA trigger bit, set 1 to startup VDMA.	W

5.2.3 VDMA status (STAT)

	STAT																												0xC	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												ACFG_ERR	ACFG_END	DESC_END	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect, read as zero.	R
3	ACFG_ERR	ACFG error	RW
2	ACFG_END	ACFG end	RW
1	DESC_END	Indicates the ending of final transfer task in TRAN mode	RW
0	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

5.3 Global

5.3.1 Global control

	GLBC																OFST															0x00000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											ACFGERR_INTE	Reserved			ENDF_INTE	Reserved						EPRI			Reserved							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:21	Reserved	Writing has no effect, read as zero.	R
20	ACFGERR_INTE	Vdma error interrupt enable	R/W
19:17	Reserved	Writing has no effect, read as zero.	R
16	ENDF_INTE	Helix end flag interrupt enable	R/W
15:10	Reserved	Writing has no effect, read as zero.	R
9:7	EPRI	AXI bus priority	R/W
6:0	Reserved	Writing has no effect, read as zero.	R
Bits to be config: [20]:0x1, [16]:0x1 [9:7]:0x4, others bits config 0.			

5.3.2 Interrupt state

	INTST																OFST															0x00034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								BS_ERR	Reserved				ACFG_ERR	Reserved	END_FLG
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7	BS_ERR	Bitstream error when decoding	R
6:3	Reserved	Writing has no effect, read as zero.	R
2	ACFG_ERR	Vdma error	R
1	Reserved	Writing has no effect, read as zero.	R
0	END_FLG	Helix end flag	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

5.4 FELIX RESET

```
#define   CPM_FELIX_SWRST     cpm_addr + C4;
#define   CPM_FELIX0_SR       (0X1<<31)
#define   CPM_FELIX0_STP      (0X1<<30)
#define   CPM_FELIX0_ACK      (0X1<<29)
#define   CPM_FELIX1_SR       (0X1<<28)
#define   CPM_FELIX1_STP      (0X1<<27)
#define   CPM_FELIX1_ACK      (0X1<<26)
#define   SET_CPM_FELIX_CTRL(a)       cpu_write(CPM_FELIX_SWRST, a)
#define   GET_CPM_FELIX_CTRL()        cpu_read(CPM_FELIX_SWRST)
```

5.4.1 reset process

1. CPU read CPM_FELIX_SWRST register, and set bit30 to 1 for request for Helix to stop bus transfer.

   e.g. SET_CPM_FELIX_CTRL(GET_CPM_FELIX_CTRL() | CPM_FELIX0_STP);

2.CPU read CPM_FELIX_SWRST register, and wait bit29 to 1 for Helix bus stop ack.

   e.g. while(! (GET_CPM_FELIX_CTRL() & CPM_FELIX0_ACK))

3. CPU read CPM_FELIX_SWRST register, and config bit31 to 1 for request Helix enters soft reset mode,.and config bit30 to 0 for request Helix clear stop bus transfer command.

   e.g. SET_CPM_FELIX_CTRL((GET_CPM_FELIX_CTRL() | CPM_FELIX0_SR) & ~CPM_FELIX0_STP);

4. CPU read CPM_FELIX_SWRST register, and config bit31 to 0 for request Helix jump out of soft reset mode,.and config bit30 to 0 for request Helix clear stop bus transfer command.

   e.g. SET_CPM_FELIX_CTRL(GET_CPM_FELIX_CTRL() & ~CPM_FELIX0_SR & ~CPM_FELIX0_STP);

5.5 Interrupt

5.5.1 Interrupt state

Refer to Interrupt state register definition

5.5.2 Interrupt processing

FELIX decode normal termination: END_FLG effect

FELIX decode abnormal termination: BS_ERR effect, or ACFG_ERR effect

If FELIX decode abnormal termination, we suggest :

1.ACFG_ERR: re-decode.

2.BS_ERR: drop frame.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

5.5.3 Interrupt clear

Physical address base	Operation
FELIX_BASE + 0x0_0000	write 0

5.6 Operational process

FELIX use API data-structure and function to configure internal registers. Software programmer should fill the data-structure with valid values, then follow steps below:
Configure global control register.
Configure Task trigger register to start FELIX, FELIX send interrupt signal to cpu when finish encode.
CPU enter the interrupt handler function, when it receive FELIX's interrupt signal.
CPU read FELIX state register, and clear FELIX's interrupt register.
According the FELIX's different state, CPU make the different response.

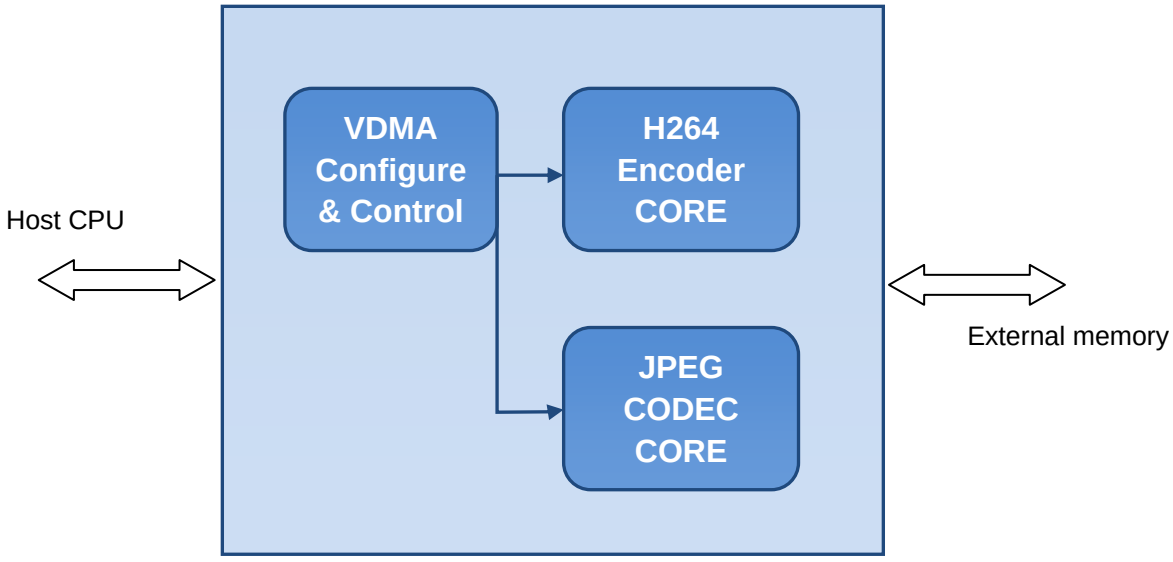
Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

6 Helix

6.1 Overview

Helix is the name of Video Processing Unit core in this chip, capable of H264 video encoding and JEPG compression and decompression. Helix embeds a JPEG CODEC core and a H264 encoder CORE, and control & configure modules.

6.1.1 Block Diagram



as illustrated above, there are 2 interfaces in HELIX

-- HELIX can be configured by Host CPU though AHB bus

-- HELIX can access External memory through a AXI bus

6.1.2 Features

H264 encoder features

- H.264 encoding up to 1080P 30fps
- Support hardware rbsp bytes recognize and eliminate
- Support auto-read of slice header
- Support reference frame lossless compression

JPEG Codec feature

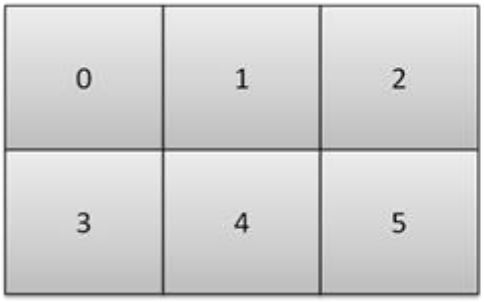
- JPEG compressing/decompressing up to 70Mega-pixels per second
- Baseline ISO/IEC 10918-1 JPEG compliant
- 8-bit pixel depth support
- Support for YUY2 color
- Up to four programmable Quantization tables
- Fully programmable Huffman tables

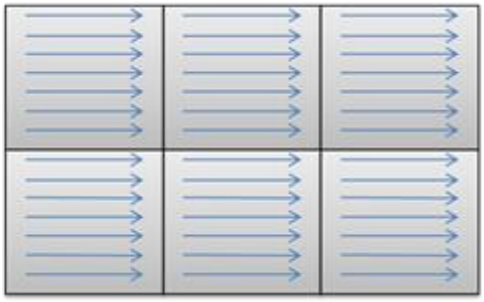
Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

6.1.3 Data Format

H264 encoder

- Input data format
  - YUV420P
  - NV12
  - NV21
- Output Bitstream
  - H264 raw bitstream
- Reference Frame
  - Tile format: frame is grouped by 16x16 pixel block, blocks are raster-scan. Pixels inside blocks are raster-scan.





JPEG Encoder

- Input data format
  - NV12
  - NV21
- Output data format
  - JPEG raw bitstream

JPEG Decoder

- Input data format
  - JPEG raw bitstream
- Output data format
  - NV12
  - Tile

6.2 VDMA

VDMA is used to auto-configure HELIX internal registers.

ACFG mode descriptor node is composed by 2 words, from the LSB to the MSB is named as CVAL and CCTL. Their details are defined as:

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description
CVAL: Configure value		
31:0	CVAL	The value to be configured into the HELIX registers indicated by CCTL.
CCTL: configure control		
31	CVLD	Only 1 indicates current node is valid, otherwise the VDMA would stop working and ACFG error interrupt would be sent if the relative interrupt enabled in SCH.CFGC.
30	CTMF	Configure terminate flag 0 indicates more node need to be read. 1 indicates current node is final one and VDMA would stop after current configuration's execution.
29:20	NC	Not cared
19:0	CIDX	Configure index Indicates which register should be configured. It should be word aligned.

6.3 Register Definition

6.3.1 VDMA status (STAT)

	STAT																												0x1000C	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												ACFG_ERR	ACFG_END	DESC_END	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect, read as zero.	R
3	ACFG_ERR	ACFG error	RW
2	ACFG_END	ACFG end	RW
1	DESC_END	Indicates the ending of final transfer task in TRAN mode	RW
0	Reserved	Writing has no effect, read as zero.	R

6.3.2 LIX Task trigger

	TRIG																OFST														0x10008	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DHA																												Reserved			RUN
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:4	DHA	Descriptor Head Address. For ACFG mode, the descriptor chain must be located in the external memory and should be 32 word aligned.	RW
3:1	Reserved	Writing has no effect, read as zero.	R
0	RUN	VDMA trigger bit, set 1 to startup VDMA.	W

6.3.3 HELIX Global control

	GLBC																OFST														0x00000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											ACFGERR_INTE	Reserved			ENDF_INTE	Reserved						EPRI			Reserved						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:21	Reserved	Writing has no effect, read as zero.	R
20	ACFGERR_INTE	Vdma error interrupt enable	R/W
19:17	Reserved	Writing has no effect, read as zero.	R
16	ENDF_INTE	Helix end flag interrupt enable	R/W
15:10	Reserved	Writing has no effect, read as zero.	R
9:7	EPRI	AXI bus priority	R/W
6:0	Reserved	Writing has no effect, read as zero.	R
Bits to be config: [20]:0x1, [16]:0x1 [9:7]:0x4, others bits config 0.			

6.3.4 HELIX Interrupt state

	INTST																OFST														0x00034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													ACFG_ERR	Reserved	END_FLG
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
2	ACFG_ERR	Vdma error	R
1	Reserved	Writing has no effect, read as zero.	R
0	END_FLG	Helix end flag	R

6.3.5 H264 Encode Slice bs len

	SLBL																OFST															0x90038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								SLICE_BS_LEN																								
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:24	Reserved	Writing has no effect, read as zero	R
23:0	SLICE_BS_LEN	Encoded bitstream size for current slice in Bytes.	R

6.3.6 H264 Encode Y SAD

	YSAD																OFST															0x80080
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Y SAD																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	Y_SAD	Luma sad.	R

6.3.7 H264 Encode C SAD

	CSAD																OFST															0x80084
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C SAD																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:0	C_SAD	Chroma sad.	R

6.3.8 JPGC trigger

	TRIG																0xE0000														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved																												TERM	PPT	BST	COPEN
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0

Bits	Name	Description	R/W
31:4	reserved	Writing has no effect, read as zero.	R
3	TERM	Indicates current trigger is the one of the last MCU. Its only need be set in UNIV encoding mode.	RW
2	PPT	Pixel Plane Trigger. In SPEC mode, it should be only set once as the startup of pixel plane working of the whole decoding/encoding process. In UNIV mode, it should be set each MCU as the startup of current MCU's start working.	W
1	BST	Bit-Stream Trigger. For both SPEC and UNIV mode, it should only be set once as the startup of bitstream fetching/storing of the whole decoding/encoding process.	W
0	COPEN	JPGC core open, it should be set at each trigging.	RW

6.3.9 JPGC Status

	STAT																0x E0008														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ENDF	reserved							BSLEN																							
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31	ENDF	Task done ending flag. For SPEC mode, it indicates whole frame's ending. For UNIV mode, it indicates current MCU's ending.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

30:24	reserved	Writing has no effect, read as zero.	R
23:0	BSLEN	Bitstream length (unit: byte) Its only used in encoding process.	RW

6.3.10 JPEG Bitstream buffer address

	BSA																													0x E000C							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSA																									Reserved						
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:7	BSA	Bitstream buffer address. Note: its always be aligned as 32 words it would be updated during the process of decoding/encoding	RW
6:0	reserved	Writing has no effect, read as zero.	R

6.3.11 JPEG Component 0 plane buffer address

	P0A																													0x E0010							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	P0A																													reserved		
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0

Bits	Name	Description	R/W
31:3	P0A	Component 0 plane buffer address. Note: 1. In UNIV mode, component plane buffer should be located in the TCSM/SRAM, so the MSB 12bit would not be cared. And also in this mode P0A should be 8-byte aligned. 2. In SPEC mode, component plane buffer should be located in the external memory and should be 256-byte aligned, that is to say the LSB 8bit would not be cared. Furthermore, P0A would be updated during the decoding/encoding process in this mode.	RW
2:0	reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

6.3.12 JPEG Component 1 plane buffer address

	P1A																												0x E0014		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	P1A																													reserved		
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0

Bits	Name	Description	R/W
31:3	P1A	Component 1 plane buffer address. Note: 1. it is similar with P0A.	RW
2:0	reserved	Writing has no effect, read as zero.	R

6.3.13 JPEG Component 2 plane buffer address

	P2A																												0x E0018		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HELIX_BASE												P2A																	reserved		
RST	0	0	0	1	0	0	1	1	0	0	1	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0

Bits	Name	Description	R/W
31:20	HELIX_BASE	Fixed as 0x132	R
19:3	P2A	Component 2 plane buffer address. Note: 1. its only used in UNIV mode	RW
2:0	reserved	Writing has no effect, read as zero.	R

6.3.14 JPEG Component 3 plane buffer address

	P2A																												0x E001C		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HELIX_BASE												P3A																	reserved		
RST	0	0	0	1	0	0	1	1	0	0	1	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:20	HELIX_BASE	Fixed as 0x132	R
19:3	P3A	Component 3 plane buffer address. Note: 1. its only used in UNIV mode	RW
2:0	reserved	Writing has no effect, read as zero.	R

6.3.15 JPEG MCU number

	NMCU																0x E0028														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved						NMCU																									
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:26	reserved	Writing has no effect, read as zero.	R
25:0	NMCU	Number of MCU minus 1 to be processing of current picture	RW

6.3.16 JPEG Re-Sync-Marker gap number

	NRSM																0x E002C														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved																													NRSM		
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:3	reserved	Writing has no effect, read as zero.	R
2:0	NRSM	Number of MCU minus 1 between 2 Re-Sync-Marker.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

6.3.17 JPEG Component configure information

	C0CI C1CI C2CI C3CI																0x E0030 0x E0034 0x E0038 0x E003C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved																								NBLK				QT		HA	HD
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:8	reserved	Writing has no effect, read as zero.	R
7:4	NBLK	Number of block minus 1 in a MCU	RW
3:2	QT	Quant table select of current component	RW
1	HA	Huffman AC table select of current component	RW
0	HD	Huffman DC table select of current component	RW

6.3.18 JPEG EFE control

	CTRL																													0x40000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved		YUY2	reserved													CFMT		reserved												EN	RUN
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	?	?	?	?	?	?	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:30	reserved	Writing has no effect, read as zero.	R
29	YUY2	When yuv format is YUY2, set it to be 1	RW
28:16	reserved	Writing has no effect, read as zero.	R
15:14	CFMT	Codec format 00: X264; 01: JPEG; 10: VP8E; others: reserved	RW
13:2	reserved	Writing has no effect, read as zero.	R
1	EN	EFE module enable. Its also be used as the module clock gating for power consumption consideration.	RW
0	RUN	EFE startup trigger	W
Note: multi-slice encoding is not supported by EFE, so AUX is needed to do the work (descriptor chain generation and encoder flow management) if multi-slice is used in encoding.			

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

6.3.19 JPEG Encode slice geometry information

	GEOM																													0x40004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FSTY								FSTX								LSTY								LSTX							
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:24	FSTY	First MB position of Y direction of current slice	RW
23:16	FSTX	First MB position of X direction of current slice Note: Since only rectangle slice partition of a frame is supported, so FSTX should always be set as 0.	RW
15:8	LSTY	Last MB position of Y direction of current slice	RW
7:0	LSTX	Last MB position of X direction of current slice	RW
Note: in JPEG codec mode, bit27:16 stands for LSTY and bit11:0 stands for LSTX and FSTY/FSTX is always 0			

6.3.20 JPEG RAW plane source buffer address

	RAW_SA																													0x40010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RAW_SA																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	RAW_SA	RAW plane source buffer address Note: the RAW buffer basement address should be 8-byte aligned	RW

6.3.21 JPEG RAW destination buffer basement address

	RAW_DBA																													0x40030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HELIX_BASE												RAW_DBA											reserved								
RST	0	0	0	1	0	0	1	1	0	0	1	0	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:20	HELIX_BASE	Fixed as 0x132	R
19:9	RAW_DBA	RAW destination buffer basement address. EFE fetching RAW data from buffer indicated by RAWY_SA and RAWC_SA then binding and delivering to the buffer indicated by RAW_DBA. It should be 512 byte aligned	RW
8:0	Reserved	Writing has no effect, read as zero.	R

6.3.22 JPEG RAW plane stride

	RAW_STR																													0x40038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RAW_STR																reserved															
RST	0	0	0	1	0	0	1	1	0	0	1	0	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	RAW_STR	Raw plane stride	RW
15:0	Reserved	Writing has no effect, read as zero.	R

6.4 JPEG Table definition

6.4.1 Huffman Base Table

The Huffman Base Table is used in decoding mode, the space offset of this table is from 0x1200 ~ 0x12FC. More detailed information is defined as the following illustration.

Mapping offset	Description
0x1200 ~ 0x123C	BASE AC 0 value
0x1240 ~ 0x127C	BASE DC 0 value
0x1280 ~ 0x12BC	BASE AC 1 value
0x12C0 ~ 0x12FC	BASE DC 1 value

6.4.2 Huffman MIN Table

The Huffman MIN Table is used in decoding mode, the space offset of this table is from 0x1300 ~ 0x133C. More detailed information is defined as the following illustration.

Mapping offset	Description
0x1300 ~ 0x130C	MIN AC 0 value
0x1310 ~ 0x131C	MIN DC 0 value

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

0x1320 ~ 0x132C	MIN AC 1 value
0x1330 ~ 0x133C	MIN DC 1 value

6.4.3 Quantization Table

The Quantization Table is used in both decoding and encoding mode, the space offset of this table is from 0x1400 ~ 0x17FC. More detailed information is defined as the following illustration.

Mapping offset	Description
0x1400 ~ 0x14FC	Quantization table 0
0x1500 ~ 0x15FC	Quantization table 1
0x1600 ~ 0x16FC	Quantization table 2
0x1700 ~ 0x17FC	Quantization table 3

6.4.4 Huffman Symbol Table

The Huffman Symbol Table is used in decoding mode, the space offset of this table is from 0x1800 ~ 0x1D3C. More detailed information is defined as the following illustration.

Mapping offset	Description
0x1800 ~ 0x1A84	SYMB AC 0 value
0x1A88 ~ 0x1AB4	SYMB DC 0 and DC 1 value
0x1AB8 ~ 0x1D3C	SYMB AC 1 value

Huffman ENC Table

The Huffman ENC Table is used in encoding mode, the space offset of this table is share with Huffman Symbol Table and it is from 0x1800 ~ 0x1DFC. More detailed information is defined as the following illustration.

Mapping offset	Description
0x1800 ~ 0x1ABC	AC Huffman Table 0
0x1AC0 ~ 0x1D7C	AC Huffman Table 1
0x1D80 ~ 0x1DBC	DC Huffman Table 0
0x1DC0 ~ 0x1DFC	DC Huffman Table 1

6.5 HELIX RESET

```
#define   CPM_HELIX_SWRST     cpm_addr + C4;
#define   CPM_HELIX_SR        (0X1<<31)
#define   CPM_HELIX_STP       (0X1<<30)
#define   CPM_HELIX_ACK       (0X1<<29)
#define   SET_CPM_HELIX_CTRL(a)       cpu_write(CPM_HELIX_SWRST, a)
#define   GET_CPM_HELIX_CTRL()        cpu_read(CPM_HELIX_SWRST)
```


Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

6.5.1 Helix reset process

1. CPU read CPM_HELIX_SWRST register, and set bit30 to 1 for request for Helix to stop bus transfer.
   e.g. SET_CPM_HELIX_CTRL(GET_CPM_HELIX_CTRL() | CPM_HELIX0_STP);
2.CPU read CPM_HELIX_SWRST register, and wait bit29 to 1 for Helix bus stop ack.
   e.g. while(! (GET_CPM_HELIX_CTRL() & CPM_HELIX0_ACK))
3. CPU read CPM_HELIX_SWRST register, and config bit31 to 1 for request Helix enters soft reset mode,.and config bit30 to 0 for request Helix clear stop bus transfer command.
   e.g. SET_CPM_HELIX_CTRL((GET_CPM_HELIX_CTRL() | CPM_HELIX0_SR) & ~CPM_HELIX0_STP);
4. CPU read CPM_HELIX_SWRST register, and config bit31 to 0 for request Helix jump out of soft reset mode,.and config bit30 to 0 for request Helix clear stop bus transfer command.
   e.g. SET_CPM_HELIX_CTRL(GET_CPM_HELIX_CTRL() & ~CPM_HELIX0_SR & ~CPM_HELIX0_STP);

6.6 H264 encoder Interrupt

6.6.1 Interrupt state

Refer to HELIX Interrupt state register definition

6.6.2 Interrupt processing

HELIX encode normal termination: END_FLG effect
HELIX encode abnormal termination: ACFG_ERR effect
If HELIX encode abnormal termination, you can chose re-encode or drop frame.

6.6.3 Interrupt clear

HELIX

Physical address base	Operation
HELIX_BASE + 0x0_0000	write 0

6.7 H264 encoder Operational process

HELIX use API data-structure and function to configure internal registers. Date-structure are defined in《HELIX parameter definition》. Software programmer should fill the data-structure with valid values, then follow steps below:
Configure global control register.
Configure Task trigger register to start HELIX, HELIX send interrupt signal to cpu when finish encode.
CPU enter the interrupt handler function, when it receive HELIX's interrupt signal.
CPU read HELIX state register, and clear HELIX's interrupt register.
According the HELIX's different state, CPU make the different response.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Section 4

DISPLAY/CAMERA/AUDIO

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7 Display Controller specification

7.1 Features

7.1.1 Layer feature

- Support 4 layer DMA channel
- Support input format: RGB888, ARGB8888, RGB565, RGB555, ARGB1555, NV12/NV21
- Support 2 level TLB
- Support frame size up to 720p
- Support Image Crop

7.1.2 Composition feature

- Support 4 layer Alpha Blending
- Support 2 layer scale（bi-cube, output image size 4x4~full screen）
- Support write back DMA
- Support frame size up to 720p

7.1.3 Display feature

- Support TFT(MIPI-DPI),SLCD(MIPI-DBI type A, B and C), MIPI-DSI
- Support 720P@60hz

7.2 Architecture map

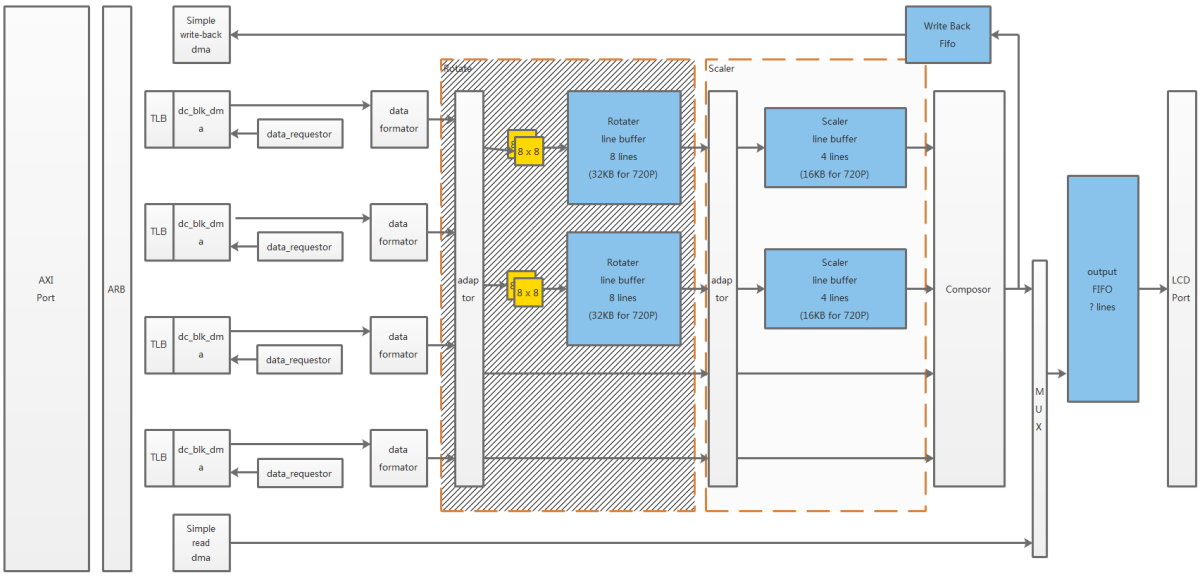


Figure 7-1 Top architecture

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.3 Data Format Description

7.3.1 Source data define (the format of source data in DDR memory)

RGB888

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

ARGB8888

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

RGB565

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

RGB555

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

ARGB1555

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

YUV422package

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
V								Y_1								U								Y_0							

Note: These are examples, the color order can be changed.

7.3.2 SLCD output pin define

8bpp (565)：

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																R7	R6	R5	R4	R3	G7	G6	G5
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																G4	G3	G2	B7	B6	B5	B4	B3

8bpp (888):

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																R7	R6	R5	R4	R3	R2	R1	R0
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																G7	G6	G5	G4	G3	G2	G1	G0
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																B7	B6	B5	B4	B3	B2	B1	B0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9bpp(666):

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															R7	R6	R5	R4	R3	R2	G7	G6	G5
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															G4	G3	G2	B7	B6	B5	B4	B3	B2

16bpp(565):

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								R7	R6	R5	R4	R3	G7	G6	G5	G4	G3	G2	B7	B6	B5	B4	B3

18bpp(666):

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						R7	R6	R5	R4	R3	R2	G7	G6	G5	G4	G3	G2	B7	B6	B5	B4	B3	B2

24bpp(888):

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

1bpp(SPI mode)

The data will be transferred by D0 pin.

7.3.3 GPIO Pads relation

For rgb888 display on LCD: R,G,B align from high to low bits in 24 GPIO Pads,

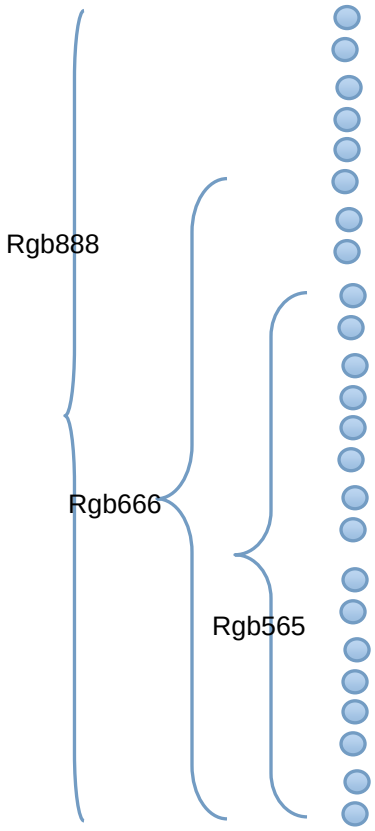
For rgb666: R,G,B align from high to low in Lower 18 GPIO Pads

For rgb565: R,G,B align from high to low in Lower 16 GPIO Pads

For rgb565 on SLCD: R,G,B align from high to low in Lower 16 GPIO Pads

For rgb565 on SLCD but 8bit data width: B,G,R go through Lower 8 GPIO Pads to SLCD

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.



7.4 Descriptor definition

7.4.1.1 Frame Configure descriptor definition

Num	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	FrameNextCfgAddr																															
1					Height																Width											
2							WB_dither_DW							WB_Format													WB_DitherAuto	WB_DitherEn	Change2SRD	DirectEn	WriteBack	Stop
3	WritebackBufferAddr																															
4																				WritebackStride											
5	**Layer0CfgAddr**																															
6	**Layer1CfgAddr**																															
7	**Layer2CfgAddr**																															
8	**Layer3CfgAddr**																															

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9																	Lay3Zorder		Lay2Zorder		Lay1Zorder		Lay0Zorder		Layer3En	Layer2En	Layer1En	Layer0En	Lay3ScaleEn	Lay2ScaleEn	Lay1ScaleEn	Lay0ScaleEn
10														EOD_MSK		EOW_MSK	SOC_MSK					EOC_MSK									

Num	Bits	Name	Description
0	31:0	FrameNextCfg Addr	Frame 's next descriptor address
1	27:16	Height	Frame's height
	11:0	Width	Frame's width
2	25:20	WB_Dither_DW	Dither drop bit. 0: drop low 0 bit(default) 1: drop low 2 bit 2: drop low 3 bit 3: drop low 4 bit [21:20]: configure blue color [23:22]: configure green color [25:24]: configure red color When source pixel is RGB888, and output at RGB666/565, the value should be 010101/100110.
	18:16	WB_Format	WriteBack format. 000：ARGB8888(default) 001：RGB565 010：RGB555 110：RGB888 Others: reserved
	5	WB_DitherAuto	Dither parameter auto select. **NOTE：** The dither function is jointly determined by WB_DitherEn and WB_DitherAuto.
	4	WB_DitherEn	Dither enable. See the instruction of WB_DitherAuto.

DitherAuto	DitherEn	result
1	1	dither enable.Dither drop bit is controlled by the WB_Dither_DW
1	0	dither enable.Dither drop bit is controlled by the WB_Format
0	1	dither enable.Dither drop bit is controlled by the WB_Dither_DW
0	0	dither disable

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

			NOTE: This bit is used only when WriteBack enable. If Wr_Format is not 888, dither need be disabled.
	3	Change2RDMA	Indicate whither need to change to RDMA channel after the current frame end. 0: no change 1: change enable
	2	DirectEn	Indicate the current frame need to be output directly. 0: Direct output disable; 1: Direct output enable.
	1	WriteBack	Indicate the current frame need to be wrote back to memory. 0: WriteBack disable; 1: WriteBack enable. When DirectEn is 1, this field must be 0.
	0	Stop	1: This is the last frame; 0: Keep refreshing.
3	31:0	WritebackBufferAddr	Frame WriteBack Buffer address.
4	31:0	WritebackStride	Frame Writeback Stride. Support 4k(4096)(Unit: pixel)
5	31:0	Layer0CfgAddr	Layer0 Cfg Descriptor address
6	31:0	Layer1CfgAddr	Layer1 Cfg Descriptor address
7	31:0	Layer2CfgAddr	Layer2 Cfg Descriptor address
8	31:0	Layer3CfgAddr	Layer3 Cfg Descriptor address
9	15:14	Lay3ZOrder	Z order of layer.0 is the bottom layer; 3 is the top layer. Note：Lay3-0 order should be exclusive，0 1 2 3 is ok，0 1 1 3 is not allowed
	13:12	Lay2ZOrder	Z order of layer.0 is the bottom layer; 3 is the top layer.
	11:10	Lay1ZOrder	Z order of layer.0 is the bottom layer; 3 is the top layer.
	9:8	Lay0ZOrder	Z order of layer.0 is the bottom layer; 3 is the top layer.
	7	Layer3En	1: enable; 0: disable.
	6	Layer2En	1: enable; 0: disable.
	5	Layer1En	1: enable; 0: disable.
	4	Layer0En	1: enable; 0: disable.
	3	Lay3ScaleEn	1: enable; 0: disable.
	2	Lay2ScaleEn	1: enable; 0: disable.
	1	Lay1ScaleEn	1: enable; 0: disable.
	0	Lay0ScaleEn	1: enable; 0: disable.
10	17	EOD_MSK	mask of DISP_END 1: generate interrupt 0: interrupt is masked
	15	EOW_MSK	mask of WDMA_END 1: generate interrupt 0: interrupt is masked

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	14	SOC_MSK	Mask of CMP_START 1: generate interrupt 0: interrupt is masked
	9	EOC_MSK	mask of CMP_END 1: generate interrupt 0: interrupt is masked

7.4.1.2 Layer Configure descriptor definition

Num	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					Layer_Height																Layer_Width											
1											SHARPL		Format						GAlpha_en		Color				GAlpha							
2	LayerBufferAddr																															
3					TargetHeight																TargetWidth											
4																														Rotation		
5																																
6					YPos																XPos											
7													Layer_Resize_Coef_X																			
8													Layer_Resize_Coef_Y																			
9																					LayerStride											
10	UVBufferAddr																															
11																					UVStride											

Num	Bits	Name	Description
0	27:16	Height	Layer's height
	11:0	Width	Layer's width
1	21:20	SHARPL	resize sharp level selector: 0: lowest sharp level 3: highest sharp level
	19:16	Format	Format of layer. 0000：RGB555 0001：ARGB1555/0555("1" is alpha_en for each individual pixel) 0010：RGB565 0100：RGB888 0101：ARGB8888 0110：MONO(8) 0111：MONO(16) 1000：NV12 1001：NV21 1010：YUV422(vy_1uy_0 in 32bits, v is at [31:24],y_0 is at [7:0])

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td></td><td></td><td></td><td>（Note：only layer0/1 support yuv2rgb change）
others：reserved</td></tr>
<tr><td></td><td>14</td><td>PREMULT</td><td>Premultiplied alpha:
1:enable;0:disable</td></tr>
<tr><td></td><td>13</td><td>GAlpha_en</td><td>1: enable; 0: disable</td></tr>
<tr><td></td><td>12:10</td><td>Color</td><td>Color of source data in memory
000：RGB
001：RBG
010：GRB
011：GBR
100：BRG
101：BGR
The module will transform these colors to RGB, which will be used for composing or output to display module directly. These bits are useless when Format is not RGB kind.</td></tr>
<tr><td></td><td>7:0</td><td>GAlpha</td><td>Global Alpha for layer. This field takes effect in case Format is RGB888, RGB565, RGB555, YUV-tile</td></tr>
<tr><td>2</td><td>31:0</td><td>LayerBufferAddr</td><td>The address of the layer buffer(aligned by 1B),
or address of Y buffer of NV12/NV21(aligned by 8B).</td></tr>
<tr><td rowspan="2">3</td><td>27:16</td><td>TargetHeight</td><td>Layer's target height. If this field is 0, vertical scaling is ignored.
When LayerScaleEn(in Frame configure descriptor definition) is 0, this field must be 0.</td></tr>
<tr><td>11:0</td><td>TargetWidth</td><td>Layer's target width. If this field is 0, horizontal scaling is ignored.
When LayerScaleEn(in Frame configure descriptor definition) is 0, this field must be 0.</td></tr>
<tr><td>4</td><td>2:0</td><td>Rotation</td><td>Rotation for layer. 尚未支持<table><tr><td>Value</td><td>Rotation</td></tr><tr><td>0x0</td><td>0°</td></tr><tr><td>0x1</td><td>90°</td></tr><tr><td>0x2</td><td>180°</td></tr><tr><td>0x3</td><td>270°</td></tr><tr><td>0x4</td><td>Horizontal mirror</td></tr><tr><td>0x5</td><td>Vertical mirror</td></tr><tr><td>0x6</td><td>Reserved</td></tr><tr><td>0x7</td><td>Reserved</td></tr></table></td></tr>
<tr><td>5</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td rowspan="2">6</td><td>27:16</td><td>YPos</td><td>Y position of Left-Top point of layer in frame.</td></tr>
<tr><td>11:0</td><td>XPos</td><td>X position of Left-Top point of layer in frame.</td></tr>
<tr><td>7</td><td>31:0</td><td>Layer_Resize_Coef_X</td><td>Resize Coefficients(h-resize-coefficient)
Val=src_w*512/tar_w</td></tr>
<tr><td>8</td><td>31:0</td><td>Layer_Resize_Coef_Y</td><td>Resize Coefficients(v-resize coefficient)
Val=src_h*512/tar_h</td></tr>
</table>

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9	11:0	LayerStride	Layer Stride(Unit: pixel) Hardware will calculate the next line's head address it self)
10	31:0	UVBufferAddr	the address of the UV buffer in DDR memory(for NV12/NV21)
11	11:0	UVStride	UV Stride(Unit: pixel) (for NV12/NV21) Hardware will calculate the next line's head address it self)

7.4.1.3 Simple read Configure descriptor definition

Num	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RdmaNextCfgAddr																															
1	FrameBufferAddr																															
2																				Stride												
3										Forma				Color																		CHAIN_END
4															EOD_MSK															SOSR_MSK	EOSR_MSK	

Num	Bits	Name	Description
0	31:0	RdmaNextCfg Addr	simple read DMA 's next descriptor address
1	31:0	FrameBufferA ddr	the head address of the frame buffer in DDR memory.
2	12:0	stride	stride. Support 4k(4096)(Unit: pixel)
3	22:19	Format	Format of layer. 0000：RGB555 0001：ARGB1555/0555("1" is alpha_en for each individual pixel) 0010：RGB565 0100：RGB888 others：reserved
	18:16	Color	Color of source data in memory 000：RGB→RGB 001：RBG→RGB 010：GRB→RGB 011：GBR→RGB 100：BRG→RGB 101：BGR→RGB The module will transform these colors to RGB, which will be used for composing or output to display module directly.
	0	CHAIN_END	1: this descriptor is the last one of the chain;

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

			0: not the last one
4	17	EOD_MSK	mask of DISP_END 1: generate interrupt 0: interrupt is masked
	2	SOS_MSK	mask of SRD_START 1: generate interrupt 0: interrupt is masked
	1	EOS_MSK	mask of SRD_END 1: generate interrupt 0: interrupt is masked

7.5 Registers Description

7.5.1 Instructions

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. The registers can be read and written by AHB2 bus
3. Register read/write attribute
   - ✧ R - Read only
   - ✧ W - Write only
   - ✧ RW - read and write
   - ✧ RCW - read and write, but clear to 0 by read
   - ✧ RSW - read and write, but set to 1 by read
   - ✧ RWC - read and write, clear to 0 by write 1, write 0 has no effect
   - ✧ RWS - read and write, set to 1 by write 1, write 0 has no effect
   - ✧ RC - read only, and clear to 0 by read
   - ✧ RS - read only, and set to 1 by read
   - ✧ SPEC - special access method, relate to its description
4. Reset Value
   - – 1 - reset to 1
   - – 0 - reset to 0
   - – ? - value unknown after reset

7.5.2 Map

The DC's registers map base address is 0x13050000

The DC is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Table 7-1 DC Registers Map

Name	Reset Value	Address Offset	Description	RW	Mask
FRM_CFG_ADDR	0x0000_0000	0x0000	frame descriptor's address	RW	0xFFFF_FFFF
FRM_CFG_CTRL	0x0000_0000	0x0004	frame descriptor's control	W	0x0000_0003
SRD_CHAIN_ADDR	0x0000_0000	0x1000	RDMA descriptor's address	RW	0xFFFF_FFFF
SRD_CHAIN_CTRL	0x0000_0000	0x1004	RDMA descriptor's control	W	0x0000_0003
CTRL	0x0000_0000	0x2000	DC control	W	0x0000_001F
ST	0x0000_0000	0x2004	DC status	R	0x8083_FFFF
CLR_ST	0x0000_0000	0x2008	DC clear status	W	0x8081_FFC6
INTC	0x0000_0000	0x200C	DC interrupt mask	RW	0x8083_FFC6
INT_FLAG	0x0000_0000	0x2010	DC interrupt flag	R	0x8083_FFC6
COM_CFG	0x0000_0000	0x2014	DC common config	RW	0x003F_00FE
PCFG_RD_CTRL	0x0000_0006	0x2018	Back door for read channel's QoS	RW	0x0000_0007
PCFG_WB_CTRL	0x0000_0006	0x201C	Back door for write back channel's QoS	RW	0x0000_0007
PCFG_OFIFO	0x0319_0842	0x2020	Priority level threshold config when comp direct or rdma	RW	0x07FF_FFFF
PCFG_WDMA	0x00C0_4010	0x2024	Priority level threshold config for when write back	RW	0x07FF_FFFF
PCFG_CMPW	0x0000_000b	0x2028	config conditons for priority when comp write back with direct output disable	RW	0x0000_07FF
PCFG0_CMPW	0x0060_0400	0x202C	Priority level threshold0 config when comp write back with direct output disable	RW	0x01FF_FFFF
PCFG1_CMPW	0x0100_0400	0x2030	Priority level threshold1 config when comp write back with direct output disable	RW	0x01FF_FFFF
PCFG2_CMPW	0x01E0_0400	0x2034	Priority level threshold2 config when comp write back with direct output disable	RW	0x01FF_FFFF
frame_DES_READ	0x0000_0000	0x2100	for debug	R	0xFFFF_FFFF
LAY0_DES_READ	0x0000_0000	0x2104	for debug	R	0xFFFF_FFFF
LAY1_DES_READ	0x0000_0000	0x2108	for debug	R	0xFFFF_FFFF
LAY2_DES_READ	0x0000_0000	0x210c	for debug	R	0xFFFF_FFFF
LAY3_DES_READ	0x0000_0000	0x2110	for debug	R	0xFFFF_FFFF
RDMA_DES_READ	0x0000_0000	0x2104	for debug	R	0xFFFF_FFFF
FRM_CHAIN_SITE	0x0000_0000	0x2200	frame descriptor's current site	R	0xFFFF_FFFF
RDMA_CHAIN_SITE	0x0000_0000	0x2204	rdma descriptor's current site	R	0xFFFF_FFFF
LAY0_SITE	0x0000_0000	0x3100	layer0's current site	R	0xFFFF_FFFF

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

LAY1_SITE	0x0000_0000	0x3104	layer1's current site	R	0xFFFF_FFFF
LAY2_SITE	0x0000_0000	0x3108	layer2's current site	R	0xFFFF_FFFF
LAY3_SITE	0x0000_0000	0x310c	layer3's current site	R	0xFFFF_FFFF
RDMA_SITE	0x0000_0000	0x3110	rdma's current site	R	0xFFFF_FFFF
WDMA_SITE	0x0000_0000	0x221c	wdma's current site	R	0xFFFF_FFFF
TLB_GLBC	0x0000_0000	0x3000	TLB Global Control	RW	0x0000_0F0F
TLB_TLBA	0x0000_0000	0x3010	TLB table entry address	RW	0xFFFF_F000
TLB_TLBC	0x0000_0000	0x3020	TLB trigger control	W	0x0000_00FF
TLB0_VPN	0x0000_0000	0x3030	VPN probe 0	R	0xFFFF_F000
TLB1_VPN	0x0000_0000	0x3034	VPN probe 1	R	0xFFFF_F000
TLB2_VPN	0x0000_0000	0x3038	VPN probe 2	R	0xFFFF_F000
TLB3_VPN	0x0000_0000	0x303C	VPN probe 3	R	0xFFFF_F000
TLB_TLBV	0x0000_0000	0x3040	TLB table entry verification	RW	0x8FFF_0FFF
TLB_STAT	0x0000_0000	0x3050	TLB status	R	0x0000_000F
CSC_MULT_YRV	0x0662_04a8	0x3200	CSC mult-coef for Y and RV	RW	0x07FF_07FF
CSC_MULT_GUGV	0x0341_0190	0x3204	CSC mult-coef for GU and GV	RW	0x03FF_01FF
CSC_MULT_BU	0x0000_0812	0x3208	CSC mult-coef for BU	RW	0x0000_0FFF
CSC_SUB_YUV	0x0080_0000	0x320C	CSC sub-coef for YUV	RW	0x00FF_001F
DISP_COM	0x0000_0000	0x8000	display common configure	RW	0x003F_00E0
TFT_HSYNC	0x0000_0000	0x9000	TFT HSYNC	RW	0xFFF_FFF
TFT_VSYNC	0x0000_0000	0x9004	TFT VSYNC	RW	0xFFF_FFF
TFT_HDE	0x0000_0000	0x9008	TFT HDE	RW	0xFFF_FFF
TFT_VDE	0x0000_0000	0x900C	TFT VDE	RW	0xFFF_FFF
TFT_CFG	0x0000_0000	0x9010	TFT configure	RW	0x003F_0707
TFT_ST	0x0000_0000	0x9014	TFT status	R	0x0000_0003
SLCD_CFG	0x0154_0D20	0xA000	SLCD configure	RW	0x0FFF_0F7F
SLCD_WR_DUTY	0x0000_0000	0xA004	SLCD WR's duty	RW	0xFFFF_FFFF
SLCD_TIMING	0x0000_0000	0xA008	SLCD timing	RW	0xFFFF_FFFF
SLCD_FRM_SIZE	0x0000_0000	0xA00C	frame size	RW	0xFFFF_FFFF
SLCD_SLOW_TIME	0x0000_0000	0xA010	slow time	RW	0x0000_FFFF
SLCD_REG_IF	0x8000_0000	0xA014	SLCD reg-op interface	RW	0xE0FF_FFFF
SLCD_ST	0x0000_0000	0xA018	SLCD status	R	0x0000_0001
SLCD_REG_CTRL	0x0000_0000	0xA01C	SLCD reg-op interface control	W	0x0000_0001

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.5.3 Composer configure

7.5.3.1 Frame configure

7.5.3.1.1 Frame descriptor address

	DC_FRM_CFG_ADDR																															BASE+0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRM_CHAIN_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FRM_CHAIN_ADDR	This is the address of the 1st descriptor before working; After start working, it is the address of the next descriptor. It can be changed by software for descriptor inserting operation. Note: the address must aligned to 64bits	RW

7.5.3.1.2 Frame descriptor control

	DC_FRM_CFG_CTRL																														BASE+0x0004	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														CHANGE_2_SRD	FRM_CFG_START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	CHANGE_2_SRD	Write 1 to change to simple read channel after the current frame. Write 0 has no effect. This bit will be cleared after changing end.	RW
0	FRM_CFG_START	Frame descriptor DMA start	W

7.5.3.2 Simple read DMA descriptor configure

7.5.3.2.1 RDMA descriptor address

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	DC_SRD_CHAIN_ADDR																BASE+0x1000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRD_CHAIN_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	SRD_CHAIN_ADDR	This is the address of the 1st descriptor before working; After start working, it is the address of the next descriptor. It can be changed by software for descriptor inserting operation. Note: the address must aligned to 64bits	RW

7.5.3.2.2 RDMA descriptor control

	DC_SRD_CHAIN_CTRL																BASE+0x1004															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															SRD_CHAIN_START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
0	SRD_CHAIN_START	RDMA descriptor DMA start	W

7.5.3.3 Control configure

	DC_CTRL																BASE+0x2000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											GEN_STP_SRD	GEN_STP_CMP	DES_CNT_RST	QCK_STP_SRD	QCK_STP_CMP
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect, read as zero.	R
4	GEN_STP_SRD	Generic stop the simple read channel. Assure integrity of the current frame	W
3	GEN_STP_CMP	Generic stop the display channel. Assure integrity of the current frame	W
2	DES_CNT_RST	Reset the counter of FRM_DES, LAYx_DES and RDMA_DES	W
1	QCK_STP_SRD	Quick stop the simple read channel. Stop as quickly as possible, the integrity of the current frame not be guaranteed.	R
0	QCK_STP_CMP	Quick stop the display channel. Stop as quickly as possible, the integrity of the current frame not be guaranteed.	W

7.5.3.4 Status Register

	DC_ST																BASE+0x2004													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMP_W_SLOW	Reserved													DISP_END	WDMA_OVER	WDMA_END	CMP_START	LAY3_END	LAY2_END	LAY1_END	LAY0_END	CMP_END	TFT_UNDR	STOP_SRD_ACK	STOP_CMP_ACK	WRBK_WORKING	DIRECT_WORKING	SRD_WORKING	SRD_START	SRD_END	WORKING
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	CMP_W_SLOW	Write back frame rate is slower than reference frame rate.	R
30:18	Reserved	Writing has no effect, read as zero.	R
17	DISP_END	One frame display end	R
16	WDMA_OVER	write back DMA is over-run	R
15	WDMA_END	write back DMA end	R
14	CMP_START	Composer start reading one frame	R
13	LAY3_END	layer3 is read end	R
12	LAY2_END	layer2 is read end	R
11	LAY1_END	layer1 is read end	R
10	LAY0_END	layer0 is read end	R
9	CMP_END	composer end of each frame	R
8	TFT_UNDR	TFT jump into under-run mode	R
7	STOP_SRD_ACK	Simple read channel is generic stopped	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

6	STOP_CMP_ACK	Composer channel is generic stopped	R
5	WRBK_WORKING	Write back channel is working	R
4	DIRECT_WORKING	Composer direct output channel is working	R
3	SRD_WORKING	Simple read channel is working	R
2	SRD_START	Start reading one frame by SRD channel	R
1	SRD_END	One frame read end by SRD channel	R
0	WORKING	display controller is working	R

7.5.3.5 Clear status Register

	DC_CSR																BASE+0x2008													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLR_CMP_W_SLOW	Reserved													CLR_DISP_END	CLR_WDMA_OVER	CLR_WDMA_END	CLR_CMP_START	CLR_LAY3_END	CLR_LAY2_END	CLR_LAY1_END	CLR_LAY0_END	CLR_CMP_END	CLR_TFT_UNDR	CLR_STP_SRD_ACK	CLR_STP_CMP_ACK	Reserved			CLR_SRD_START	CLR_SRD_END	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	CLR_CMP_W_SLOW	Clear CMP_W_SLOW	W
30:18	Reserved	Writing has no effect, read as zero.	R
17	CLR_DISP_END	clear DISP_END	W
16	CLR_WDMA_OVER	clear WDMA_OVER	W
15	CLR_WDMA_END	clear WDMA_END	W
14	CLR_CMP_START	clear CMP_START	W
13	CLR_LAY3_END	clear LAY3_END	W
12	CLR_LAY2_END	clear LAY2_END	W
11	CLR_LAY1_END	clear LAY1_END	W
10	CLR_LAY0_END	clear LAY0_END	W
9	CLR_CMP_END	clear CMP_END	W
8	CLR_TFT_UNDR	clear TFT_UNDR	W
7	CLR_STP_SRD_ACK	clear STOP_SRD_ACK	W
6	CLR_STP_CMP_ACK	clear STOP_CMP_ACK	W
5:3	Reserved	Writing has no effect, read as zero.	R
2	CLR_SRD_START	clear SRD_RD_START	W
1	CLR_SRD_END	clear SRD_RD_END	W
0	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.5.3.6 DPU INTC register

	DC_DPU_INTC																BASE+0x200c													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CWS_MSK	Reserved													EOD_MSK	OOW_MSK	EOW_MSK	SOC_MSK	EOB3_MSK	EOB2_MSK	EOB1_MSK	EOB0_MSK	EOC_MSK	UOT_MSK	SSA_MSK	SCA_MSK	Reserved		SOS_MSK	EOS_MSK	Reserved	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	CWS_MSK	mask of CMP_W_SLOW 1: generate interrupt 0: interrupt is masked	RW
30:18	Reserved	Writing has no effect, read as zero.	R
17	EOD_MSK	mask of DISP_END 1: generate interrupt 0: interrupt is masked	RW
16	OOW_MSK	mask of WDMA_OVER 1: generate interrupt 0: interrupt is masked	RW
15	EOW_MSK	mask of WDMA_END 1: generate interrupt 0: interrupt is masked	RW
14	SOC_MSK	mask of SRD_START 1: generate interrupt 0: interrupt is masked	RW
13	EOL3_MSK	mask of LAY3_END 1: generate interrupt 0: interrupt is masked	RW
12	EOL2_MSK	mask of LAY2_END 1: generate interrupt 0: interrupt is masked	RW
11	EOL1_MSK	mask of LAY1_END 1: generate interrupt 0: interrupt is masked	RW
10	EOL0_MSK	mask of LAY0_END 1: generate interrupt 0: interrupt is masked	RW
9	EOC_MSK	mask of CMP_END 1: generate interrupt	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: interrupt is masked	
8	UOT_MSK	mask of TFT_UNDR 1: generate interrupt 0: interrupt is masked	RW
7	SSA_MSK	mask of STOP_SRD_ACK 1: generate interrupt 0: interrupt is masked	RW
6	SCA_MSK	mask of STOP_CMP_ACK 1: generate interrupt 0: interrupt is masked	RW
5:3	Reserved	Writing has no effect, read as zero.	R
2	SOS_MSK	mask of SRD_START 1: generate interrupt 0: interrupt is masked	RW
1	EOS_MSK	mask of SRD_END 1: generate interrupt 0: interrupt is masked	RW
0	Reserved	Writing has no effect, read as zero.	R

7.5.3.7 INT flag register

	DC_INTC																BASE+0x2010													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INT_CWS	Reserved													INT_EOD	INT_OOW	INT_EOW	INT_SOC	INT_EOL3	INT_EOL2	INT_EOL1	INT_EOL0	INT_EOC	INT_UOT	INT_SSA	INT_SCA	Reserved			INT_SOS	INT_EOS	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	INT_CWS	interrupt of CMP_W_SLOW	R
30:18	Reserved	Writing has no effect, read as zero.	R
17	INT_EOD	interrupt of DISP_END	R
16	INT_OOW	interrupt of WDMA_OVER	R
15	INT_EOW	interrupt of WDMA_END	R
14	INT_SOC	interrupt of CMP_START	R
13	INT_EOL3	interrupt of LAY3_END	R
12	INT_EOL2	interrupt of LAY2_END	R
11	INT_EOL1	interrupt of LAY1_END	R
10	INT_EOL0	interrupt of LAY0_END	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9	INT_EOC	interrupt of CMP_END	R
8	INT_UOT	interrupt of TFT_UNDR	R
7	INT_SSA	interrupt of STOP_SRD_ACK	R
6	INT_SCA	interrupt of STOP_CMP_ACK	R
5:3	Reserved	Writing has no effect, read as zero.	R
2	INT_SOS	interrupt of SRD_START	R
1	INT_EOS	interrupt of SRD_END	R
0	Reserved	Writing has no effect, read as zero.	R

7.5.3.8 Common configure register

	DC_COM_CONFIG																BASE+0x2014													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										SCALE1_CLKGATE_EN	SCALE0_CLKGATE_EN	LAYER3_CLKGATE_EN	LAYER2_CLKGATE_EN	LAYER1_CLKGATE_EN	LAYER0_CLKGATE_EN	Reserved								BURST_LEN_WDMA		BURST_LEN_RDMA		BURST_LEN_BDMA		CH_SEL	Reserved
RST	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
21	SCALE1_CLK GATE_EN	Clk gate enable, 1:indicate open clk gate. 0:indicate disable clk gate,scale1's DMA always has clock.	
20	SCALE0_CLK GATE_EN	Clk gate enable, 1:indicate open clk gate. 0:indicate disable clk gate, scale0's DMA always has clock.	
19	LAYER3_CLK GATE_EN	Clk gate enable, 1:indicate open clk gate. 0:indicate disable clk gate, Layer3's DMA always has clock.	
18	LAYER2_CLK GATE_EN	Clk gate enable, 1:indicate open clk gate. 0:indicate disable clk gate, Layer2's DMA always has clock.	
17	LAYER1_CLK GATE_EN	Clk gate enable, 1:indicate open clk gate. 0:indicate disable clk gate, Layer1's DMA always has clock.	
16	LAYER0_CLK GATE_EN	Clk gate enable, 1:indicate open clk gate. 0:indicate disable clk gate, Layer0's DMA always has clock.	

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

15:8	Reserved	Writing has no effect, read as zero.	R
7:6	BURST_LEN_WDMA	The max length of the write back DMA's burst. 00: 4(default) 01: 8 10: 16 11: 32	RW
5:4	BURST_LEN_RDMA	The max length of the simple read DMA's burst. 00: 4(default) 01: 8 10: 16 11: 32	RW
3:2	BURST_LEN_BDMA	The max length of the block DMA's burst. 00: 4(default) 01: 8 10: 16 11: 32	RW
1	CH_SEL	select data channel 1: simple read channel 0: composer direct output channel(default)	RW
0	Reserved	Writing has no effect, read as zero.	R

7.5.3.9 Priority configure register

7.5.3.9.1 PCFG_RD_CTRL register

	DC_PCFG_RD_CTRL																BASE+0x2018														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													arqos_val		arqos_ctrl
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
2:1	Arqos_val	QoS value. 00~11, and reset value is 11.	RW
0	Arqos_ctrl	Whether use the value set by software. 0: the value is generated by the hardware; 1: the value is specified by software.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.5.3.9.2 PCFG_WB_CTRL register

	DC_PCFG_WB_CTRL																BASE+0x201c																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													awqos_val		awqos_ctrl
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
2:1	Awqos_val	QoS value. 00~11, and reset value is 11.	RW
0	Awqos_ctrl	Whether use the value set by software. 0: the value is generated by the hardware; 1: the value is specified by software.	RW

7.5.3.9.3 OFIFO's PCFG register

	DC_OFIFO_PCFG																BASE+0x2020															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					Pcfg2									Pcfg1									Pcfg0								
RST	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0

OFIFO_PCFG is used when composer output direct or simple read dma

The 3 thresholds cut the output FIFO into 4 space. When the entries remained triggers one of them, the priority level will be altered by hardware. And the 3 thresholds must follow the order: pcfg2 ≥ pcfg1 ≥ pcfg0.

Priority level（arqos）

Priority_lv	Space
11	Empty ~ threshold0
10	Threshold0 ~ threshold1
01	Threshold1 ~ threshold2
00	Threshold2 ~ full

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26:18	Pcfg2	Threshold2:0~263	RW
17:9	Pcfg1	Threshold1:0~263	RW
8:0	Pcfg0	Threshold0:0~263	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.5.3.9.4 WDMA's PCFG register

	DC_WDMA_PCFG																BASE+0x2024															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					Pcfg2									Pcfg1									Pcfg0								
RST	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0

WDMA_PCFG is used when write back dma

The 3 thresholds cut the wdma buffer into 4 space. When the entries remained triggers one of them, the priority level will be altered by hardware. And the 3 thresholds must follow the order: pcfg2 ≥ pcfg1 ≥ pcfg0.

Priority level（awqos）

Priority_lv	Space
00	Empty ~ threshold0
01	Threshold0 ~ threshold1
10	Threshold1 ~ threshold2
11	Threshold2 ~ full

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26:18	Pcfg2	Threshold2:0~63	RW
17:9	Pcfg1	Threshold1:0~63	RW
8:0	Pcfg0	Threshold0:0~63	RW

7.5.3.9.5 CMP_W's PCFG register

7.5.3.9.5.1 CMPW_PCFG register

	DC_COMP_W_CFG																BASE+0x2028															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					Wrbk_frm_rate_ctrl	num_mclk									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

NOTE : only used when writeback without direct display.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect, read as zero.	R
10	wrbk_frm_rate_ctrl	If write back frame rate is faster than reference frame rate, the next frame would not start immediately. 1: enable 0: disable	RW
9:0	num_mclk	based on the reference frame rate, how many clk cycle is needed for sending one pixel.	RW

For example, if mclk is 250MHz，standard output frequency is 60Hz, then

*num_mclk=250M/(60*frame_size).*

num_mclk=10.85 (frame_size =800x480).

num_mclk=40.69 (frame_size =320x320).

num_mclk=72.33 (frame_size =240x240).

num_mclk=4.52 (frame_size =1280x720).

num_mclk=1.69 (frame_size =1920x1080).

7.5.3.9.5.2 CMPW_PCFG0 register

	DC_CMPW_PCFG0																BASE+0x202c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							Pcfg_cycle0				Pcfg_count0																					
RST	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

NOTE : only used when writeback without direct display.

7.5.3.9.5.3 CMPW_PCFG1 register

	DC_CMPW_PCFG1																BASE+0x2030															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							Pcfg_cycle1				Pcfg_count1																					
RST	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

NOTE : only used when writeback without direct display.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.5.3.9.5.4 CMPW_PCFG2 register

	DC_CMPW_PCFG2																BASE+0x2034															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							Pcfg_cycle2				Pcfg_count2																					
RST	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

NOTE : only used when writeback without direct display.

7.5.3.10 Descriptor read registers

7.5.3.10.1 Frame configure descriptor register

	DC_FRM_DES																BASE+0x2100															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRM_DES																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FRM_DES	Read the frame configure descriptor in order, one at a time. The counter will reset when writing DES_CNT_RST	R

7.5.3.10.2 Layer0 configure descriptor register

	DC_LAY0_DES																BASE+0x2104															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LAY0_DES																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LAY0_DES	Read the layer0 configure descriptor in order, one at a time. The counter will reset when writing DES_CNT_RST	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.5.3.10.3 Layer1 configure descriptor register

	DC_LAY1_DES																BASE+0x2108															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LAY01_DES																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LAY1_DES	Read the layer1 configure descriptor in order, one at a time. The counter will reset when writing DES_CNT_RST	R

7.5.3.10.4 Layer2 configure descriptor register

	DC_LAY2_DES																BASE+0x210c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LAY2_DES																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LAY2_DES	Read the layer2 configure descriptor in order, one at a time. The counter will reset when writing DES_CNT_RST	R

7.5.3.10.5 Layer3 configure descriptor register

	DC_LAY3_DES																BASE+0x2110															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LAY3_DES																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LAY3_DES	Read the layer3 configure descriptor in order, one at a time. The counter will reset when writing DES_CNT_RST	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.5.3.10.6 Simple read configure descriptor register

	DC_FRM_DES																															BASE+0x2114
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDMA_DES																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	RDMA_DES	Read the simple read DMA configure descriptor in order, one at a time. The counter will reset when writing DES_CNT_RST	R

7.5.3.11 Software locate register

7.5.3.11.1 Frame descriptor's current site register

	DC_FRM_CHAIN_SITE																															BASE+0x2200
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRM_CHAIN_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FRM_CHAIN_SITE	Read the address to locate current descriptor's site in the chain.	R

7.5.3.11.2 RDMA descriptor's current site register

	DC_RDMA_CHAIN_SITE																															BASE+0x2204
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDMA_CHAIN_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	RDMA_CHAIN_SITE	Read the current descriptor site in DDR memory of simple reading.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.5.3.11.3 Layer0's current pixel site register

	DC_LAY0_SITE																BASE+0x3100															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LAY0_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LAY0_SITE	Read the current pixel site in DDR memory of layer0.	R

7.5.3.11.4 Layer1's current pixel site register

	DC_LAY1_SITE																BASE+0x3104															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LAY1_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LAY1_SITE	Read the current pixel site in DDR memory of layer1.	R

7.5.3.11.5 Layer2's current pixel site register

	DC_LAY2_SITE																BASE+0x3108															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LAY2_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LAY2_SITE	Read the current pixel site in DDR memory of layer2.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.5.3.11.6 Layer3's current pixel site register

	DC_LAY3_SITE																BASE+0x310c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LAY3_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	LAY3_SITE	Read the current pixel site in DDR memory of layer3.	R

7.5.3.11.7 Simple read DMA's current pixel site register

	DC_RDMA_SITE																BASE+0x3110															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDMA_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	RDMA_SITE	Read the current pixel site in DDR memory of simple reading.	R

7.5.3.11.8 Write back DMA's current pixel site register

	DC_WDMA_SITE																BASE+0x221c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WDMA_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	WDMA_SITE	Read the current pixel site in DDR memory of writing back.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.5.3.12 TLB configure

7.5.3.12.1 Global control

	GLBC																BASE+0x3000													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				FMODE				Reserved				TLBE			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:12	Reserved	Writing has no effect, read as zero.	R
11:8	FMODE	TLB fetch mode, for STB miss 0 - fetch 1 entry for each miss; 1 - fetch 8 entry for each miss Bit 11: Display Controller Channel 3 TLB pre-fetch mode Bit 10: Display Controller Channel 2 TLB pre-fetch mode Bit 9 : Display Controller Channel 1 TLB pre-fetch mode Bit 8 : Display Controller Channel 0 TLB pre-fetch mode	RW
3:0	TLBE	TLB enable Bit 3: Display Controller Channel 3 TLB enable Bit 2: Display Controller Channel 2 TLB enable Bit 1: Display Controller Channel 1 TLB enable Bit 0: Display Controller Channel 0 TLB enable	RW

7.5.3.12.2 TLB table address

	GLBA																BASE+0x3010													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TLBA																				Reserved											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:12	TLBA	TLB table address Its only used and must be initialized when GLBC.TLBEn was set.	RW
11:0	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.5.3.12.3 TLB control Trigger

	TLBC																BASE+0x3020															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								RETRY				INVLD			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:8	Reserved	Writing has no effect, read as zero.	R
7:4	RETRY	When TLB table entry un-usable case occurs, SW set this bit to inform to retry reading the TLB table entry again.	W
3:0	INVLD	Write 1 to invalidate all TLB caches.	W

7.5.3.12.4 TLB VPN Status

	VPN0,1,2,3																BASE+0x3030,0x3034,0x3038,0x303C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VPNX																				Reserved											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:12	VPNX	When working in TLB enable case, if the relative TLB table entry in the external DDR is un-useable, VPU will record its virtual address bit31:12 into VPN. SW can read-out VPN for TLB table entry's rebuilding.	RW
11:0	Reserved	Writing has no effect, read as zero.	R

7.5.3.12.5 TLB table entry verification

	TLBV																BASE+0x3040															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCI	reserved			CNM												reserved				GCN											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31	RCI	Check bit ignored(ignore the vld bit for PEntry, SEntry in memory)	RW
30:28	Reserved	Writing has no effect, read as zero.	R
27:16	CNM	Check number mask	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	GCN	Golden Check number VPU will check its secondary table entry to judge whether it is valid. If (GCN & CNM) == (TLB entry data readed by TLB [11:0] & CNM) indicates current entry is valid, otherwise it is unusable.	RW

7.5.3.12.6 SCH status

	STAT																BASE+0x3050													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												CH3_TLB_ERR	CH2_TLB_ERR	CH1_TLB_ERR	CH0_TLB_ERR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:4	Reserved	Writing has no effect, read as zero.	R
3	CH3_TLB_ERR	CH3 TLB error occurs. Write 0 to cleared.	RW
2	CH2_TLB_ERR	CH2 TLB error occurs. Write 0 to cleared.	RW
1	CH1_TLB_ERR	CH1 TLB error occurs. Write 0 to cleared.	RW
0	CH0_TLB_ERR	CH0 TLB error occurs. Write 0 to cleared.	RW

7.5.3.13 CSC configure registers

BASE+0x320X is for layer0, and BASE+0x321X is for layer1.

Calculation flow

---

sub_y_w= p_csc_yuv_data[23:16]-p_csc_sub_y_coef;
sub_u_w= p_csc_yuv_data[15:8]-p_csc_sub_uv_coef；
sub_v_w= p_csc_yuv_data[7:0]- p_csc_sub_uv_coef；

---

mul_y_w = coef_y*sub_y_w;
mul_rv_w = coef_rv*sub_v_w;
mul_gu_w = coef_gu*sub_u_w;

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

```
mul_gv_w = coef_gv*sub_v_w;
mul_bu_w = coef_bu*sub_u_w;
-------------------------------------------
rgb_r_w     = mul_y_w + mul_rv_w;
rgb_g_w     = mul_y_w - mul_gu_w - mul_gv_w;
rgb_b_w     = mul_y_w + mul_bu_w;
```

7.5.3.13.1 CscMultYRv

	LCDC_TINY_CSC_MULT_YRV																BASE+0x3200/3210													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					CSC_MULT_RV											Reserved					CSC_MULT_Y									
RST	0	0	0	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0	1	0	1	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
26:16	CSC_MULT_RV	CSC multiplication coefficient for RV **NOTE**: reference value mode 0: CSC_MULT_RV = 0x48f mode 1: CSC_MULT_RV = 0x662 (default) mode 2: CSC_MULT_RV = 0x59c mode 3: CSC_MULT_RV = 0x57c	RW
15:11	Reserved	Writing has no effect, read as zero.	R
10:0	CSC_MULT_Y	CSC multiplication coefficient for Y **NOTE**: reference value mode 0: CSC_MULT_Y = 0x400 mode 1: CSC_MULT_Y = 0x4a8 (default) mode 2: CSC_MULT_Y = 0x400 mode 3: CSC_MULT_Y = 0x47c	RW

7.5.3.13.2 CscMultGuGv

	LCDC_TINY_CSC_MULT_GUGV																BASE+0x3204/3214													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						CSC_MULT_GV										Reserved							CSC_MULT_GU							
RST	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	CSC_MULT_GV	CSC multiplication coefficient for GV **NOTE**: reference value mode 0: CSC_MULT_Y = 0x253 mode 1: CSC_MULT_Y = 0x341 (default) mode 2: CSC_MULT_Y = 0x2db mode 3: CSC_MULT_Y = 0x2cb	RW
15:9	Reserved	Writing has no effect, read as zero.	R
8:0	CSC_MULT_GU	CSC multiplication coefficient for GU **NOTE**: reference value mode 0: CSC_MULT_Y = 0x193 mode 1: CSC_MULT_Y = 0x190 (default) mode 2: CSC_MULT_Y = 0x160 mode 3: CSC_MULT_Y = 0x15a	RW

7.5.3.13.3 CscMultBu

	LCDC_TINY_CSC_MULT_BU																BASE+0x3208/3218													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CSC_MULT_BU															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
11:0	CSC_MULT_BU	CSC multiplication coefficient for BU **NOTE**: reference value mode 0: CSC_MULT_Y = 0x820 mode 1: CSC_MULT_Y = 0x812(default) mode 2: CSC_MULT_Y = 0x717 mode 3: CSC_MULT_Y = 0x6ee	RW

7.5.3.13.4 CscSubYUV

	LCDC_TINY_CSC_SUB_YUV																BASE+0x320C/321C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								CSC_SUB_UV								Reserved											CSC_SUB_Y				
RST	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	CSC_SUB_UV	CSC subtraction coefficient for UV **NOTE**: reference value mode 0: CSC_MULT_Y = 0x0 mode 1: CSC_MULT_Y = 0x80 (default) mode 2: CSC_MULT_Y = 0x80 mode 3: CSC_MULT_Y = 0x80	RW
15:5	Reserved	Writing has no effect, read as zero.	R
4:0	CSC_SUB_Y	CSC subtraction coefficient for Y **NOTE**: reference value mode 0: CSC_MULT_Y = 0x0 mode 1: CSC_MULT_Y = 0x0(default) mode 2: CSC_MULT_Y = 0x0 mode 3: CSC_MULT_Y = 0x0	RW

7.5.4 Display interfaces configure

7.5.4.1 Common

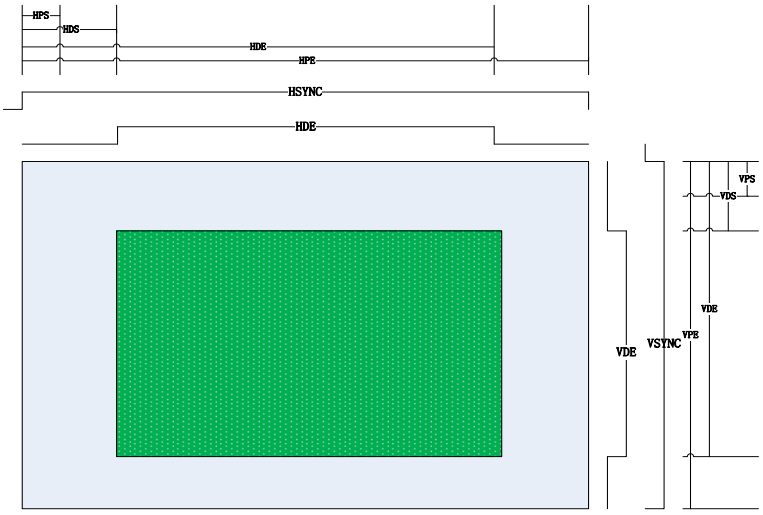
	DISP_COM																BASE+0x8000													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										DP_DITHER_DW						Reserved								DITHER_CLKGATE_EN	LCD_CLKGATE_EN	TFT_CLKGATE_EN	DP_DITHER_EN	Reserved		DP_IF_SEL	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writing has no effect, read as zero.	R
21:16	DP_DITHER_DW	Dither drop bit. 0: drop low 0 bit(default) 1: drop low 2 bit 2: drop low 3 bit 3: drop low 4 bit [17:16]: configure blue color [19:18]: configure green color [21:20]: configure red color When source pixel is RGB888, and output at RGB666/565, the value should be 010101/100110.	RW

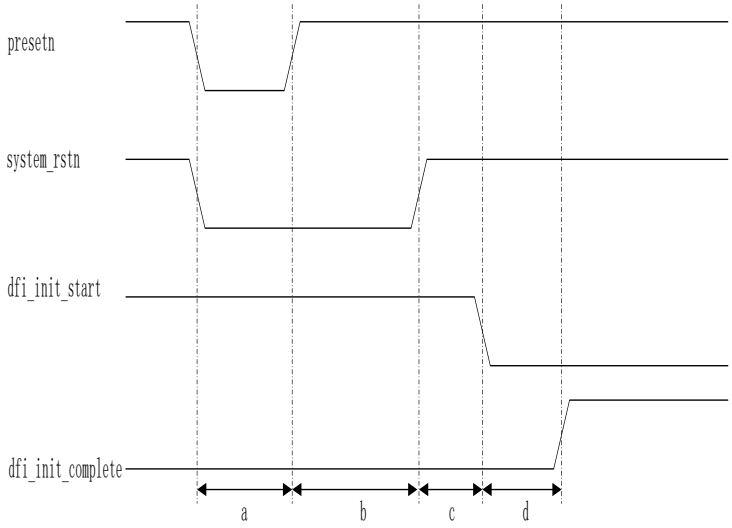
Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

15:8	Reserved	Writing has no effect, read as zero.	R
7	DITHER_CLKGATE_EN	Clk gate enable, 1:indicate open clk gate. 0:indicate disable clk gate, Dither always has clock.	RW
6	SLCD_CLKGATE_EN	Clk gate enable, 1:indicate open clk gate. 0:indicate disable clk gate, SLCD always has clock.	RW
5	TFT_CLKGATE_EN	Clk gate enable, 1:indicate open clk gate. 0:indicate disable clk gate, TFT always has clock.	RW
4	DP_DITHER_EN	Dither enable. 0: dither disable(default) 1: dither enable **NOTE**: If source data is not 888 format, dither need be disabled.	RW
3:2	Reserved	Writing has no effect, read as zero.	R
1:0	DP_IF_SEL	Display interfaces select. 0: no display(default) 1: TFT 2: SLCD 3: SLCD_MIPI	RW

7.5.4.2 TFT



Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.



7.5.4.2.1 TIMING_HSYNC

	TFT_TIMING_HSYNC																BASE+0x9000													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				HPS												Reserved				HPE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	HPS	HSYNC pulse start point(base on dot clock cycle) This bit must not be 0.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	HPE	HSYNC pulse end point(base on dot clock cycle) This bit must not be 0.	RW

7.5.4.2.2 TIMING_VSYNC

	TFT_TIMING_VSYNC																BASE+0x9004													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				VPS												Reserved				VPE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	VPS	VSYNC pulse start point(base on dot clock cycle) This bit must not be 0.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	VPE	VSYNC pulse end point(base on dot clock cycle) This bit must not be 0.	RW

7.5.4.2.3 TIMING_HDE

	TFT_TIMING_HDE																BASE+0x9008															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			HDS													Reserved			HDE												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	HDS	Horizontal display area start point (base on dot clock cycle). And it is also the DE pulse start point in horizontal. It indicate the end point of horizontal back porch.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	HDE	Horizontal display area end point (base on dot clock cycle). And it is also the DE pulse end point in horizontal. It indicate the end point of horizontal front porch.	RW

7.5.4.2.4 TIMING_VDE

	TFT_TIMING_VDE																BASE+0x900C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			VDS													Reserved			VDE												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:16	VDS	Vertical display area start point(base on dot clock cycle). And it is also the DE pulse start point in vertical.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		It indicate the end point of vertical back porch.	
15:12	Reserved	Writing has no effect, read as zero.	R
11:0	VDE	Vertical display area end point(base on dot clock cycle). And it is also the DE pulse end point in vertical. It indicate the start point of vertical front porch.	RW

7.5.4.2.5 TRANS_CONFIG

	TFT_TRAN_CFG																BASE+0x9010													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										COLOR_EVEN			COLOR_ODD			Reserved					PIXCLK_INV	DE_DL	SYNC_DL	Reserved					MODE		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
21:19	COLOR_EVEN	Output color mode of even lines(2, 4, 6...) 000: RGB→RGB 001: RGB→RBG 010: RGB→BGR 011: RGB→BRG 100: RGB→GBR 101: RGB→GRB	RW
18:16	COLOR_ODD	Output color mode of odd lines(1, 3, 5...) 000: RGB→RGB 001: RGB→RBG 010: RGB→BGR 011: RGB→BRG 100: RGB→GBR 101: RGB→GRB	RW
15:11	Reserved	Writing has no effect, read as zero.	R
10	PIX_CLK_INV	Inverse the polarity of the DOT_CLK	RW
9	DE_DL	Default level of DE(invalid level)	RW
8	SYNC_DL	Default level of HSYNC and VSYNC(invalid level)	RW
7:3	Reserved	Writing has no effect, read as zero.	R
2:0	MODE	000: 888 parallel mode 001: 666 parallel mode 010: 565 parallel mode 100: 8bits serial mode without dummy(RGB)	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		101: 8bits serial mode with dummy(RGBD)	

7.5.4.2.6 STATUS

	TFT_ST																													BASE+0x9014	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														WORKING	UNDER
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	WORKING	0: TFT is not working 1: TFT is working	R
0	UNDER	Indicate the controller jump into recovery state, and starting trans one frame 0 to panel. 0: TFT is working order 1: TFT is in UNDER mode.	R

7.5.4.3 SLCD (Smart LCD)

7.5.4.3.1 SLCD_CONFIG

	SLCD_PANEL_CFG																													BASE+0xA000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				RDY_JIT	FMT_EN	DBI_TYPE			PIX_FMT		TE_JIT	TE_MD	TE_SWITCH	RDY_SWITCH	CS_EN	Reserved				CS_DP	RDY_DP	DC_MD	WR_MD	Reserved	TE_DP	DWIDTH			CWIDTH			
RST	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27	RDY_ANTI_JIT	Anti-jitter for RDY. 0: sample RDY with 1 pixclk cycle(default) 1: sample RDY with 3 pixclk cycles for anti-jitter.	RW
26	FMT_EN	Whether the pixels by REG_IF need conversion 0: no use conversion;(default) 1: need conversion.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

25:23	DBI_TYPE	001: typeA(6800) 010: typeB(8080)(default) 100: typeC(SPI-3line) 101: typeC(SPI-4line) other: reserved	RW
22:21	PIX_FMT	Color format. 00: 565 (typeA/B、typeC) 01: 666 (typeA/B) 01: 444 (typeC) 10: 888 (typeA/B、typeC)(default) NOTE: typeA/B For 565, the DWIDTH can be 8bits and 16bits; For DWIDTH = 9bits, there is only 666 format; For DWIDTH = 16bits, there is only 565 format; For DWIDTH = 18bits, there is only 666 format; For 888, the DWIDTH can be 8bits and 24bits; Note: The pairing of DWIDTH and DATA_FMT is only these 5 modes, other configure is error. typeC: There are 444、565、888（for 888,high six bits are valid each byte for lcd screen, so format is 666 for lcd screen）	
20	TE_ANTI_JIT	Anti-jitter for TE. 0: sample TE with 1 pixclk cycle; 1: sample TE with 3 pixclk cycles for anti-jitter(default).	RW
19	TE_MD	The active edge of TE. 0: the front edge(default) 1: the back edge	RW
18	TE_SWITCH	0: do not wait TE, send pix_data after SLCD_START; 1: wait TE, and then send pix_data.(default)	RW
17	RDY_SWITCH	0: do not wait RDY, send command or data immediately;(default) 1: wait RDY, and then send command or data.	RW
16	CS_EN	CS control enable. 0: The CS pin is controlled by GPIO.(default) 1: The CS pin is controlled by SLCD.	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11	CS_DP	The CS's default polarity 0: the default(invalid) level is low; 1: the default(invalid) level is high;(default)	RW
10	RDY_DP	The RDY's default polarity 0: the default(invalid) level is low; 1: the default(invalid) level is high;(default)	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9	DC_MD	DC's definition. 0: Command DC = low, Data DC = high(default) 1: Command DC = high, Data DC = low	RW
8	WR_MD	WR's definition. 0: drive at posedge(drive level is high) sample at negedge(sample level is low); 1: drive at negedge(drive level is low) sample at posedge(sample level is high).(default) Note: When typeC, the WR pin is SPI_CLK.	RW
7	TE_SWITCH_MIPI	0: do not wait TE, send pix_data after SLCD_START; 1: wait TE, and then send pix_data.	RW
6	TE_DP	The TE' default polarity 0: the default(invalid) level is low;(default) 1: the default(invalid) level is high;	RW
5:3	DWIDTH	Panel's data bus width at typeA/B. 000: 8bits(typeA/B) 001: 9bits(typeA/B) 010: 16bits(typeA/B) 011: 18bits(typeA/B) 100: 24bits(typeA/B) (default) Note: When typeC, DWIDTH is no use.	RW
2:0	CWIDTH	The width of panel's command and it's parameters. 000: 8bits(typeA/B) (default) 001: 9bits(typeA/B) 010: 16bits(typeA/B) 011: 18bits(typeA/B) 100: 24bits(typeA/B) Note: When typeC, CWIDTH is no use. But only 8bits command can be supported.	RW

NOTE1: When configure stage, keep CS inactive.

NOTE2:

When DMA mode, pixels will be formatted, not controlled by FMT_EN;

When register mode, command and parameters will not be formatted, not controlled by FMT_EN;

When register mode, pixels will be controlled by FMT_EN (0: SLCD will directly output the low 8/16/18 bits of content of REG_IF directly; 1: SLCD will convert the content of REG_IF.

Note4:

When send command by REG_IF, the output command is only decided by CWIDTH. If CWIDTH is 8bits, only the low 8 bits of content of REG_IF are useful, other bits will be lost; if CWIDTH is 9bits, only the low 9bit of content of REG_IF are useful, other bits will be lost; and so on.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.5.4.3.2 SLCD_WR_DUTY

	SLCD_WR_DUTY																BASE+0xA004													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSTIME								DDTIME								CSTIME								CDTIME							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	DSTIME	WR's sample level period when transmitting pixels or parameters.	RW
23:16	DDTIME	WR's drive level period when transmitting pixels or parameters.	RW
15:8	CSTIME	WR's sample level period when transmitting command	RW
7:0	CDTIME	WR's drive level period when transmitting command	RW

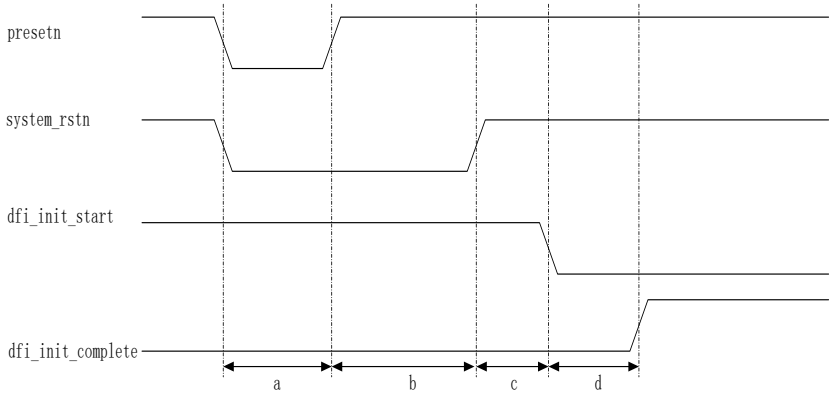
NOTE: The description is based on 8080(MIPI DBI TypeB) and SPI(MIPI DBI TypeC)mode, it's opposite when 6800(MIPI DBI TypeA) mode. The actual cycle is n+1.

7.5.4.3.3 SLCD_TIMING

	SLCD_TIMING																BASE+0xA008													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCH								TCS								TAH								TAS							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	TCH	Chip select hold time.	RW
23:16	TCS	Chip select setup time.	RW
15:8	TAH	Address hold time.	RW
7:0	TAS	Address setup time.	RW

Note：TAS, TCS, TCH are used in both parallel and serial mode, while TAH is only used in serial mode. The actual cycle is n+1.



Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.5.4.3.4 SLCD_FRM_SIZE

	SLCD_FRM_SIZE																BASE+0xA00C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	V_SIZE																H_SIZE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	V_SIZE	Line number of each frame.	RW
15:0	H_SIZE	Pixel number of each line.	RW

7.5.4.3.5 SLCD_SLOW_TIME

	SLCD_SLOW_TIME																BASE+0xA010															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SLOW_TIME															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	SLOW_TIME	SLCD will delay some period of pixclk before transmitting data, after TE's relative edge. Note: SLOW_TIME must be 0 when DP_IF_SEL==SLCD_MIPI.	WR

7.5.4.3.6 SLCD_REG_IF

	SLCD_REG_IF																BASE+0xA014															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FLAG		CMD_END	Reserved					content																							
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	FLAG	It is used to decide the meanings of the DATA/CMD/PARAMETER. 00: pix_data;	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		01: parameter; 1x: command(default).	
29	CMD_END	Indicate this is the last content, the hardware will disable the CS	RW
28:24	Reserved	Writing has no effect, read as zero.	R
23:0	content	content	RW

NOTE: The next command(include its parameters) or pix_data must wait BUSY is 0 when using the reg_if for transferring.

There would no frm_end when sending pixels by SLCD_REG_IF.

7.5.4.3.7 SLCD_STATUS

	SLCD_ST																BASE+0xA018															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															BUSY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	BUSY	Indicate whether the SLCD DBI interface controller is working or not. 0: idle 1: busy	R

7.5.4.3.8 SLCD_REG_CTRL

	SLCD_REG_CTRL																BASE+0xA01C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															RESET_3LINE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	RESET_3LINE	Write 1 to reset an inner counter when sending frame by SLCD_REG_IF, write one before each frame(only used at typeC 3line 444 mode	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.6 Operation guide

7.6.1 Composer operation

(1) Prepare four layer and frame descriptor chain. In first, you should create four layer's descriptor, because frame descriptor has four layer descriptor's address.
(2) Set frame descriptor's address by DC_FRM_CFG_ADDR register.
(3) Set DIS_IF_SEL register for TFT or SLCD.
(4) Set DC_FRM_CFG_CTRL register to start composer.
(5) Wait until FRM_CFG_END interrupt, indicate frame's descriptor has been read, then software should update frame descriptor chain.

7.6.2 TFT operation

(1) Set TFT_TIMING_HSYNC, TFT_TIMING_VSYNC, TFT_TIMING_HDE, TFT_TIMING_VDE;

for example, see picture of 7.5.4.2: HS, invalid time of HSYNC, need 5 cycles at least, HBP need 10 cycles, HFP need 10 cycles, and there are 800 pixels per line. So HPS need set 5, HPE need set 825; HDS need set 15, HDE need set 815; configure VSYNC and VDE use same method.

(2) Set TFT_TRAN_CFG

PIX_CLK_INV, DE_DL and SYNC_DL respectively used to adjust the phase of DOT_CLK, DE, HSYNC and VSYNC; COLOR_EVEN and COLOR_ODD used to change the output mode of pixel color mode; MODE used to configure the transfer mode.

(3) Start to configure composer as steps 7.6.1

7.6.3 SLCD operation

(1) Configure each bit of SLCD_PANEL_CFG according to the relevant instructions;
(2) Set SLCD_WR_DUTY, SLCD_TIMING and SLCD_SLOW_TIME to meet panel requirements;
(3) Set SLCD_FRM_SIZE to the actual size;
(4) Start to configure composer as steps 7.6.1
(5) Set FMT_EN of SLCD_PANEL_CFG to 0(if no command, skip this step);
(6) Write a command and its flag to SLCD_CMD(if no command, skip this step);
(7) Wait BUSY of SLCD_ST is 0(if no command, skip this step);
(8) Repeat step(5) and (6) until all command send out(if no command, skip this step);
(9) Set FMT_EN to 1;
(10) Write SLCD_START;
(11) Wait FRM_END of DC_ST, and clear it;
(12) Repeat step(5) to (11) for next frame transfer.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7.6.4 Data channel switch

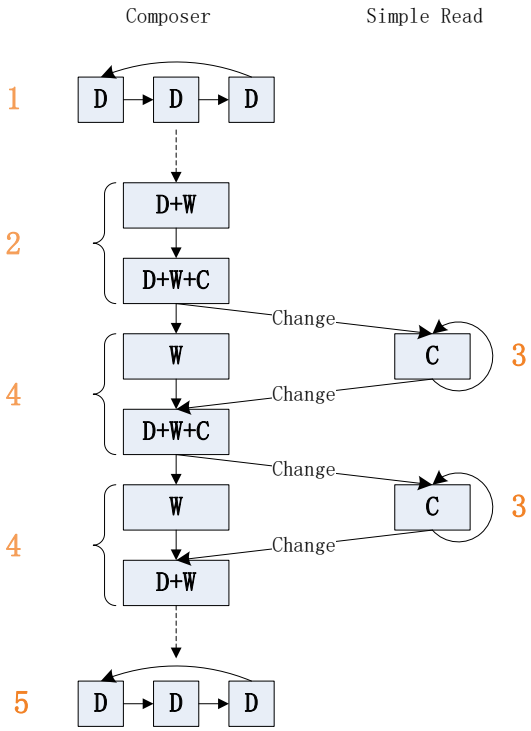


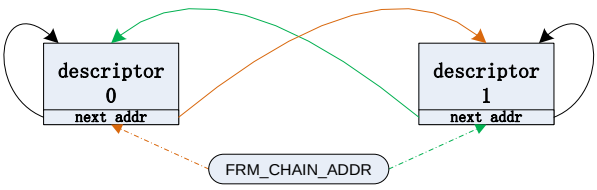
Figure 7-2 7 layers OSD

- ✧ Direct display(D)
- ✧ Direct display(D) and write back(W), with change flag(C)(there's two way for setting C flag: set DC_FRM_CFG_CTRL or set the frame descriptor), hardware will change to simple read channel(SRD) after composing end
- ✧ When there is a new D frame, hardware will change to composer channel(CMP) when the current SRD frame end, or else, hardware will refresh SRD image continuously to keep the frame rate.

Note：

- For composer(CMP) channel, if current frame has C flag, display channel will change to simple read; composer channel will stop if there's stop flag(S), otherwise, CMP channel will execute the next frame, and the next frame must be W frame.
- The priority of general stop op. is higher than C flag. For example, the current frame has C flag, hardware will change to SRD channel when composing end, but if software set general stop, hardware will stop after current frame end, and changing will not happen.

7.6.5 Insert new descriptor into current chain



Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Write the new descriptor's address in FRM_CHAIN_ADDR/SRD_CHAIN_ADDR, hardware will change to the new chain at appropriate time.

7.6.6 Simple Rdma/Composer switch

Simple read dma display picture by simple read data from ddr , while compose-dma can directly display picture after compose 4layer.

From compose-dma to rdma, for example, before start compose-descriptor-dma, set compose-descriptor-6th node change2rdma bit, config rdma address register，start compose-dma; At 6th frame, DPU read compose-descriptor and find out switch to rdma request， after this frame finished， it will switch to rdma。

From rdma to compose-dma, for example, while rdma running, config compose-dma addres and frame dma register change2comp bit, after this frame finished， it will switch to compose-dma

7.6.7 interrupt control

The mask of interrupt in descriptor must cooperate with the same mask in INTC reg, interrupt can be generate only if both mask is 1; other interrupt are controlled only by INTC reg.

7.7 Software Notes

when frame is less than 500 pixels, descriptor chain cannot be continuous, only one descriptor can be executed.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

8 Rotator

8.1 Features

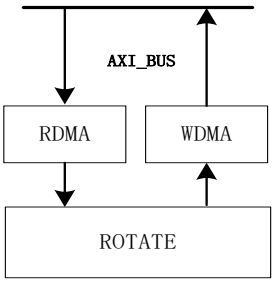
8.1.1 Frame feature

- Support input format：RGB888，ARGB8888，RGB565，RGB555， ARGB1555，YUV422
- Support frame size 4x4~2047x2047
- Support ImageCut
- Support write back format: ARGB8888，RGB565，RGB555，YUV422

8.1.2 Rotate feature

- Support Rotate Angle: 0°, 90°, 180°, 270°, Horizontal mirror，Vertical mirror

8.2 Architecture map



8.3 Descriptor definition

8.3.1.1 Frame Configure descriptor definition

	NextDesAddr																0x0														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NextDesAddr																															

Bits	Name	Description
31:0	NextCfgAddr	Next descriptor address

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	SrcBufferAddr	0x4
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	WritebackBufferAddr	

Bits	Name	Description
31:0	SrcBufferAddr	Frame's buffer address. Note：RGB ： pixel alignment YUV ： 2 pixel alignment

	SrcStride	0x8
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	Reserved	WritebackStride

Bits	Name	Description
31:11	Reserved	Writing has no effect, read as zero.
10:0	SrcStride	Src Stride. Support 4k(2047) Note：RGB ： pixel alignment YUV ： 2 pixel alignment

	FrameStop	0xc
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	Reserved	Frame_stop

Bits	Name	Description
31:1	Reserved	Writing has no effect, read as zero.
0	FrameStop	1: This is the last frame; 0: Keep refreshing.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	TargetBufferAddr																0x10													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WritebackBufferAddr																															

Bits	Name	Description
31:0	TargetBufferAddr	Frame WriteBack Buffer address. Note：RGB ： pixel alignment YUV ： 2 pixel alignment

	TargetStride																					0x14									
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					TargetStride									

Bits	Name	Description
31:11	Reserved	Writing has no effect, read as zero.
10:0	TargetStride	Target Stride. Support 4k(2047) Note：RGB ： pixel alignment YUV ： 2 pixel alignment

	Interrupt Control																												0x18		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												SOF_MASK	EOF_MASK	Reserved	

Bits	Name	Description
31:4	Reserved	Writing has no effect, read as zero.
3	SOF_MASK	mask of frame start 1: generate interrupt 0: interrupt is masked
2	EOF_MASK	mask of FRM_END

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: generate interrupt 0: interrupt is masked
1:0		

8.4 Registers Description

8.4.1 Instructions

Following chapter will descript the functions of all software accessible registers.

Conventions:

5. Register Address = Base + Address offset
6. The registers can be read and written by AHB2 bus
7. Register read/write attribute
   - ✧ R - Read only
   - ✧ W - Write only
   - ✧ RW - read and write
   - ✧ RCW - read and write, but clear to 0 by read
   - ✧ RSW - read and write, but set to 1 by read
   - ✧ RWC - read and write, clear to 0 by write 1, write 0 has no effect
   - ✧ RWS - read and write, set to 1 by write 1, write 0 has no effect
   - ✧ RC - read only, and clear to 0 by read
   - ✧ RS - read only, and set to 1 by read
   - ✧ SPEC - special access method, relate to its description
8. Reset Value
   - – 1 - reset to 1
   - – 0 - reset to 0
   - – ? - value unknown after reset

8.4.2 Map

The DC's registers map base address is 0x13070000

The DC is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 8-1 DC Registers Map

Name	Reset Value	Address Offset	Description	RW	Mask
FRM_CFG_ADDR	0x0000_0000	0x0000	frame descriptor's address	RW	0xFFFF_FFFF
FRM_SIZE	0x03FF_03FF	0x0004	frame's size	RW	0x03FF_03FF
GLB_CFG	0x0014_0000	0x0008	global config	RW	0x03C1_C63F
CTRL	0x0000_0000	0x000C	Rotator control	W	0x0000_0007
STATUS	0x0000_0000	0x0010	Rotator status	R	0x0000_000F

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

CLR_STATUS	0x0000_0000	0x0014	Rotator clear status	W	0x0000_0007
INT_MASK	0x0000_0000	0x0018	Rotator interrupt mask	RW	0x0000_0007
RDMA_SITE	0x0000_0000	0x0020	RDMA's current site	RW	0xFFFF_FFFF
WDMA_SITE	0x0000_0000	0x0024	WDMA's current site	RW	0xFFFF_FFFF
DS_FRM_DES	0x0000_0000	0x0028	descriptor register	R	0xFFFF_FFFF
ROT_QOS	0x0804_0207	0x0030	Rotator qos config	RW	0xFFFF_FFFF

8.4.3 Common config registers

8.4.3.1 Frame config addr register

	FRM_CFG_ADDR																BASE+0x0000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRM_CHAIN_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FRM_CHAIN_ADDR	This is the address of the 1st descriptor when rotator is not working; When rotator is working, it can not be set and changed ,it is the address of the next descriptor.	RW

8.4.3.2 Frame size register

	FRAM_SIZE																BASE+0x0004															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					FRAM_HEIGHT											Reserved					FRAM_WIDTH										
RST	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	RW
26:16	FRAM_HEIGHT	Frame's height	RW
15:11	Reserved	Writing has no effect, read as zero.	RW
10:0	FRAM_WIDTH	Frame's width	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

8.4.3.3 Global config register

DC_GLB_CFG																															
																	BASE+0x0008														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	DS_ROT_EN	DS_BDMA_EN	DS_WDMA_EN	RDMA_FMT				Reserved					RDMA_ORDER			Reserved	WDMA_FMT			Reserved				ROT_ANGLE				BURST_LEN_WDMA		BURST_LEN_BDMA	
RST	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Reserved	Writing has no effect, read as zero.	RW
30	DS_ROT_EN	rotator clkgate. 0: rotator enable(default) 1: rotator disable	RW
29	DS_BDMA_EN	bdma clkgate. 0: bdma enable(default) 1: bdma disable	RW
28	DS_WDMA_EN	wdma clkgate. 0: wdma enable(default) 1: wdma disable	RW
27:24	RDMA_FMT	Format of source data 0000：RGB555 0001：ARGB1555 0010：RGB565 0100：RGB888 0110：MONO(Y8) 0101：ARGB8888(default) 1010：YUV422	RW
23:19	Reserved	Writing has no effect, read as zero.	RW
18:16	RDMA_ORDER	Color of source data 000：RGB→RGB(default) 001：RBG→RGB 010：GRB→RGB 011：GBR→RGB 100：BRG→RGB 101：BGR→RGB The module will transform these colors to RGB, which will be used for composing or output to display module directly.	RW
15	Reserved	Writing has no effect, read as zero.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

14:12	WDMA_FMT	Target format 000：ARGB8888(default) 001：RGB565 010：RGB555 011：YUV422 100：MONO(Y8)	RW
11:8	Reserved	Writing has no effect, read as zero.	RW
7	Horizontal mirror	Image will be fipped horizontally if set to 1	RW
6	Vertical mirror	Image will be fipped vertically if set to 1	RW
5:4	ROT_ANGLE	00: 0°(default) 01: 90° 10: 180° 11: 270°	RW
3:2	WDMA_BURST_LEN	The max length of the write back DMA's burst. 00: 4(default) 01: 8 10:16 11:32	RW
1:0	RDMA_BURST_LEN	The max length of the block DMA's burst. 00: 4(default) 01: 8 10:16 11:32	RW

8.4.3.4 Control register

	CTRL																BASE+0x000C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												DES_CNT_RST	GEN_STOP	START	START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect, read as zero.	R
3	DES_CNT_RST	Reset the counter of FRM_DES	W
2	GEN_STOP	General stop rotator. Assure integrity of the current frame	W
1	QUICK_STOP	Quick stop rotator. Stop as quickly as possible, the integrity of the current frame not be guaranteed.	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	START	Write 1 to start rotator.	W

8.4.3.5 Status Register

DC_ST																	BASE+0x0010														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												SOF_MASK_ST	EOF_MASK_ST	GSA_MASK_ST	Reserved													SOF	EOF	GEN_STOP_ACK	WORKING
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as zero.	R
19	SOF_MASK_ST	mask of FRM_START 1: generate interrupt 0: interrupt is masked	R
18	EOF_MASK_ST	mask of FRM_END 1: generate interrupt 0: interrupt is masked	R
17	GSA_MASK_ST	mask of GEN_STOP_ACK 1: generate interrupt 0: interrupt is masked	R
16:4	Reserved	Writing has no effect, read as zero.	R
3	SOF	One frame start reading	R
2	EOF	One frame read end	R
1	GEN_STOP_ACK	Rotator is general stop	R
0	WORKING	Rotator is working	R

8.4.3.6 Clear status Register

DC_CSR																	BASE+0x0014														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												CLR_SOF	CLR_EOF	CLR_GEN_STOP_ACK	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
3	CLR_SOF	clear FRM_START.	W
2	CLR_EOF	clear FRM_END.	W
1	CLR_GEN_STP_ACK	Clear general stop acknowledge.	W
0	Reseved		R

8.4.3.7 INT_MASK register

	INT_MASK																BASE+0x0018															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												SOF_MASK	EOF_MASK	GSA_MASK	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect, read as zero.	R
3	SOF_MASK	mask of FRM_START 1: generate interrupt 0: interrupt is masked	RW
2	EOF_MASK	mask of FRM_END 1: generate interrupt 0: interrupt is masked	RW
1	GSA_MASK	mask of GEN_STOP_ACK 1: generate interrupt 0: interrupt is masked	RW
0	Reserved	Writing has no effect, read as zero.	R

8.4.3.8 Software locate register

8.4.3.8.1 READ DMA's current pixel site register

	RDMA_SITE																BASE+0x0020															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BDMA_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	RDMA_SITE	Read the current pixel site in DDR memory of block dma reading.	R

8.4.3.8.2 Write back DMA's current pixel site register

	WDMA_SITE																BASE+0x0024															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WDMA_SITE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	WDMA_SITE	Read the current pixel site in DDR memory of writing back.	R

8.4.3.9 Descriptor definition

8.4.3.9.1 frame configure descrigure definition

	DS_FRM_DES																BASE+0x28															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DS_FRM_DES																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DS_FRM_DES	Read the frame configure descriptor in order,one at a time. The counter will reset when writing DES_CNT_RST	R

8.4.3.10 Rotator QOS config

	ROT_QOS																BASE+0x30															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	STD_THR2								STD_THR1								STD_THR0								STD_CLK							
RST	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:24	STD_THR2	rotator qos threshold 2	RW
23:16	STD_THR1	rotator qos threshold 1	RW
15:8	STD_THR0	rotator qos threshold 0	RW
7:0	STD_CLK	the number of clocks between two pixel。 computing method: STD_CLK = frequency * 1 / (framerate * resolution)。	RW

8.5 Operation guide

8.5.1 Composer operation

(1) Prepare frame descriptor chain.

(2) Set frame descriptor's address by FRM_CFG_ADDR register.

(3) Set DC_CTRL register for start rotator.

(4) If need to update descriptor chain when rotator is working , wait until INT_SOF interrupt, indicate frame's descriptor has been read, then software can update frame descriptor chain(when continuous frame mode), clear DC_ST register.

Wait until INT_EOF interrupt, indicate frame's has been rotate and writeback, clear DC_ST register , if this is the last frame, then repeat(1)~(4), else repeat(4).

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9 MIPI DSI Controller

9.1 Overview

The Display Serial Interface (DSI) is part of a group of communication protocols defined by the MIPI Alliance. The MIPI DSI Controller is a host digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI DSI controller provides an interface between the system and the MIPI D-PHY, allowing the communication with a DSI-compliant display.

Features:

- Compliant with MIPI Alliance standards
- Supports all commands defined in the MIPI Alliance specification for Display Command Set (DCS)
- Supports up to two D-PHY data lanes
- Bidirectional communication and escape mode support through data lane 0
- Supports non-continuous clock in D-PHY clock lane for additional power saving
- Supports Ultra Low-Power mode with PLL disabled
- ECC and Checksum capabilities
- Support for End of Transmission Packet (EoTp)
- Fault recovery schemes
- 3D transmission support
- Enhanced DPI (eDPI) interface features
- Support for all DPI features (Standard Video Mode)
- Additional support for sending large amounts of data through the memory_write_start (WMS) and memory_write_continue (WMC) DCS command
- Vertical and horizontal color bar generation without DPI stimuli
- BER pattern without DPI stimuli

9.2 Registers

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute

   R - Read only

   W - Write only

   RW - read and write

   RCW - read and write, but clear to 0 by read

   RSW - read and write, but set to 1 by read

   RWC - read and write, clear to 0 by write 1, write 0 has no effect

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

RWS - read and write, set to 1 by write 1, write 0 has no effect
RC - read only, and clear to 0 by read
RS - read only, and set to 1 by read
SPEC - special access method, relate to its description

3. Reset Value
1 - reset to 1
0 - reset to 0
? - value unknown after reset

9.2.1 Registers Memory Map

Table 9-1 Registers Memory Map-Address Base

Name	Base	Description
MIPI_DSI	0x103014000	Address base of MIPI DSI controller

Table 9-2 MIPI DSI Register Description

Name	Description	Reset Value	Address Offset	Access Size
VERSION	Version of the DSI host controller	0x3133302A	0x000	32
PWR_UP	Core power-up	0x00000000	0x004	32
CLKMGR_CFG	Configuration of the internal clock dividers	0x00000000	0x008	32
DPI_VCID	DPI virtual channel id	0x00000000	0x00C	32
DPI_COLOR_CODING	DPI color coding	0x00000000	0x010	32
DPI_CFG_POL	DPI polarity configuration	0x00000000	0x014	32
DPI_LP_CMD_TIM	Low-power command timing configuration	0x00000000	0x018	32
PCKHDL_CFG	Packet handler configuration	0x00000000	0x02C	32
GEN_VCID	Generic interface virtual channel id	0x00000000	0x030	32
MODE_CFG	Video or Command mode selection	0x00000001	0x034	32
VID_MODE_CFG	Video mode configuration	0x00000000	0x038	32
VID_PKT_SIZE	Video packet size	0x00000000	0x03C	32
VID_NUM_CHUNKS	Number of chunks	0x00000000	0x040	32
VID_NULL_SIZE	Null packet size	0x00000000	0x044	32
VID_HSA_TIME	Horizontal Sync Active time	0x00000000	0x048	32
VID_HBP_TIME	Horizontal Back Porch time	0x00000000	0x04C	32
VID_HLINE_TIME	Line time	0x00000000	0x050	32
VID_VSA_LINES	Vertical Sync Active period	0x00000000	0x054	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

VID_VBP_LINES	Vertical Back Porch period	0x00000000	0x058	32
VID_VFP_LINES	Vertical Front Porch period	0x00000000	0x05C	32
VID_VACTIVE_LINES	Vertical resolution	0x00000000	0x060	32
EDPI_CMD_SIZE	Size for eDPI packets	0x00000000	0x064	32
CMD_MODE_CFG	Command mode configuration	0x00000000	0x068	32
GEN_HDR	Generic packet header configuration	0x00000000	0x06C	32
GEN_PLD_DATA	Generic payload data in and out	0x00000000	0x070	32
CMD_PKT_STATUS	Command packet status	0x00001515	0x074	32
TO_CNT_CFG	Timeout timers configuration	0x00000000	0x078	32
HS_RD_TO_CNT	Peripheral response timeout definition after high-speed read operations	0x00000000	0x07C	32
LP_RD_TO_CNT	Peripheral response timeout definition after low-power read operations	0x00000000	0x080	32
HS_WR_TO_CNT	Peripheral response timeout definition after high-speed write operations	0x00000000	0x084	32
LP_WR_TO_CNT	Peripheral response timeout definition after low-power write operations	0x00000000	0x088	32
BTA_TO_CNT	Peripheral response timeout definition after bus turnaround	0x00000000	0x08C	32
SDF_3D	3D control configuration	0x00000000	0x090	32
LPCLK_CTRL	Low-power in clock lane	0x00000000	0x094	32
PHY_TMR_LPCLK_CFG	D-PHY timing configuration for the clock lane	0x00000000	0x098	32
PHY_TMR_CFG	D-PHY timing configuration for data lanes	0x00000000	0x09C	32
PHY_RSTZ	D-PHY reset control	0x00000000	0x0A0	32
PHY_IF_CFG	D-PHY interface configuration	0x00000000	0x0A4	32
PHY_ULPS_CTRL	D-PHY Ultra Low-Power control	0x00000000	0x0A8	32
PHY_TX_TRIGGERS	D-PHY transmit triggers	0x00000000	0x0AC	32
PHY_STATUS	D-PHY PPI status interface	0x00001528	0x0B0	32
PHY_TST_CTRL0	D-PHY test interface control 0	0x00000001	0x0B4	32
PHY_TST_CTRL1	D-PHY test interface control 1	0x00000000	0x0B8	32
INT_ST0	Interrupt status register 0	0x00000000	0x0BC	32
INT_ST0	Interrupt status register 1	0x00000000	0x0C0	32
INT_MSK0	Masks the interrupt generation triggered by the INT_ST0 register	0x00000000	0x0C4	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

INT_MSK1	Masks the interrupt generation triggered by the INT_ST1 register	0x00000000	0x0C8	32
INT_FORCE0	Force interrupts that affect the INT_ST0 register	0x00000000	0x0D8	32
INT_FORCE1	Force interrupts that affect the INT_ST1 register	0x00000000	0x0DC	32
VID_SHADOW_CTRL	Controls DPI shadow register mechanism feature	0x00000000	0x100	32
DPI_VCID_ACT	Configures the virtual channel id for the DPI traffic	0x00000000	0x10C	32

9.2.2 Registers and Fields Description

9.2.3 VERSION

This register contains the version of the MIPI DSI Host Controller

																		BASE + 0x000													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VERSION																															
RST	0	0	0	1	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	0	1	0	1	0

Bits	Name	Description	RW
31:0	VERSION	This field indicates the version of the MIPI DSI Host Controller	R

9.2.4 PWR_UP

This register controls the power-up of the MIPI DSI Controller.

																		BASE + 0x004													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															shutdownz
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Reserved	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	shutdownz	This bit configures the core either to power up or to reset. shutdownz is the soft reset register. Its default value is 0. After the core configuration, to enable the MIPI DSI Controller, set this register to 1. 0: Reset 1: Power-up	RW

9.2.5 CLKMGR_CFG

This register configures the factor for the internal dividers to divide lanebyteclk for timeout purpose.

BASE + 0x008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																to_clk_division								tx_esc_clk_division							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Reserved	R
15:8	to_clk_division	This field indicates the division factor for the Time Out clock used as the timing unit in the configuration of HS to LP and LP to HS transition error.	RW
7:0	tx_esc_clk_division	This field indicates the division factor for the TX Escape clock source (lanebyteclk). The values 0 and 1 stop the TX_ESC clock generation.	RW

9.2.6 DPI_VCID

This register configures the virtual channel id for DPI traffic.

BASE + 0x00C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														dpi_vcid	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Reserved	R
1:0	dpi_vcid	This field configures the DPI virtual channel id that is indexed to the Video mode packets.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.2.7 DPI_COLOR_CODING

This register configures the DPI color coding.

																															BASE + 0x010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																							lose18_en	Reserved				dpi_color_coding			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:9	Reserved	Reserved	R
8	loosely18_en	When set to 1, this bit activates loosely packed variant to 18-bit configurations.	RW
7:4	Reserved	Reserved	R
3:0	dpi_color_coding	This field configures the DPI color coding as follows: 0000: 16-bit configuration 1 0001: 16-bit configuration 2 0010: 16-bit configuration 3 0011: 18-bit configuration 1 0100: 18-bit configuration 2 0101: 24-bit 0110-1111: Reserved	RW

9.2.8 DPI_CFG_POL

This register configures the polarity of the DPI signals.

																															BASE + 0x014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											colorm_act	shutd_act	hsync_act	vsync_act	dataen_act
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Reserved	R
4	colorm_active_low	When set to 1, this bit configures the color mode pin as active low.	RW
3	shutd_active_low	When set to 1, this bit configures the shutdown pin as active low.	RW
2	hsync_active_low	When set to 1, this bit configures the horizontal synchronism pin as active low.	RW
1	vsync_active_low	When set to 1, this bit configures the vertical synchronism pin as	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		active low.	
0	dataen_active_low	When set to 1, this bit configures the data enable pin as active low.	RW

9.2.9 DPI_LP_CMD_TIM

This register configures the timing for the low-power commands sent while in video mode.

																														BASE + 0x018	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								outvact_lpcmd_line								Reserved								invact_lpcmd_time							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Reserved	R
23:16	outvact_lpcmd_time	This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VSA, VBP, and VFP regions.	RW
15:8	Reserved	Reserved	R
7:0	invact_lpcmd_time	This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VACT region.	RW

9.2.10 PCKHDL_CFG

This register configures how EoTp, BTA, CRC, and ECC are to be used, to meet the peripheral's characteristics.

																												BASE + 0x02C			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											crc_rx_en	ecc_rx_en	bta_en	eotp_rx_en	eotp_tx_en
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Reserved	R
4	crc_rx_en	When set to 1, this bit enables the CRC reception and error reporting.	RW
3	ecc_rx_en	When set to 1, this bit enables the ECC reception, error correction, and reporting.	RW
2	bat_en	When set to 1, this bit enables the Bus Turn-Around (BTA) request.	RW
1	etop_rx_en	When set to 1, this bit enables the EoTp reception.	RW
0	etop_tx_en	When set to 1, this bit enables the EoTp transmission.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.2.11 GEN_VCID

This register configures the virtual channel id of the read responses to store and return to the Generic interface.

																	BASE + 0x030														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														gen_vcid	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Reserved	R
1:0	gen_vcid_rx	This field indicates the Generic interface read-back virtual channel identification.	RW

9.2.12 MODE_CFG

This register configures the mode of operation - Video mode or Command mode (Commands can be sent even in video mode too).

																	BASE + 0x034														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															cmd_video
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:1	Reserved	Reserved	R
0	cmd_video_mode	This bit configures the operation mode: 0: Video mode 1: Command mode	RW

9.2.13 VID_MODE_CFG

This register configures several aspects of the Video mode operation such as the transmission mode, switching to low-power in the middle of a frame, enabling acknowledge, and whether to send the commands in low-power.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

																	BASE + 0x038													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							vpg_orient	Reserved			vpg_mode	Reserved			vpg_en	lp_cmd_en	frame_bta	lp_hfp_en	lp_hpb_en	lp_vact_en	lp_vfp_en	lp_vbp_en	lp_vsa_en	Reserved						vid_mode	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:25	Reserved	Reserved	R
24	vpg_orientation	This field indicates the color bar orientation as follows: 0: Vertical mode 1: Horizontal mode	RW
23:21	Reserved	Reserved	R
20	vpg_mode	This field is to select the pattern: 0: Color bar (horizontal or vertical) 1: BER pattern (vertical only)	RW
19:17	Reserved	Reserved	R
16	vpg_en	When set to 1, this bit enables the video mode pattern generator.	RW
15	lp_cmd_en	When set to 1, this bit enables the command transmission only in low-power mode.	RW
14	frame_bta_ack_en	When set to 1, this bit enables the request for an acknowledge response at the end of a frame.	RW
13	lp_hfp_en	When set to 1, this bit enables the return to low-power inside the Horizontal Front Porch (HFP) period when timing allows.	RW
12	lp_hbp_en	When set to 1, this bit enables the return to low-power inside the Horizontal Back Porch (HBP) period when timing allows.	RW
11	lp_vact_en	When set to 1, this bit enables the return to low-power inside the Vertical Active (VACT) period when timing allows.	RW
10	lp_vfp_en	When set to 1, this bit enables the return to low-power inside the Vertical Front Porch (VFP) period when timing allows.	RW
9	lp_vbp_en	When set to 1, this bit enables the return to low-power inside the Vertical Back Porch (VBP) period when timing allows.	RW
8	lp_vsa_en	When set to 1, this bit enables the return to low-power inside the Vertical Sync Time (VSA) period when timing allows.	RW
7:2	Reserved	Reserved	R
1:0	vid_mode_type	This field indicates the video mode transmission type as follows: 00: Non-burst with sync pulses 01: Non-burst with sync events 10 and 11: Burst mode	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.2.14 VID_PKT_SIZE

This register configures the video packet size.

																													BASE + 0x03C	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		vid_pkt_size													
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:14	Reserved	Reserved	R
13:0	vid_pkt_size	This field configures the number of pixels in a single video packet. For 18-bit not loosely packed data types, this number must be a multiple of 4.	RW

9.2.15 VID_NUM_CHUNKS

This register configures the number of chunks to use. The data in each chunk has the size provided by VID_PKT_SIZE.

																													BASE + 0x040	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																			vid_num_chunks												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:13	Reserved	Reserved	R
12:0	vid_num_chunks	This register configures the number of chunks to be transmitted during a Line period (a chunk consists of a video packet and a null packet). If set to 0 or 1, the video line is transmitted in a single packet. If set to 1, the packet is part of a chunk, so a null packet follows it if vid_null_size > 0. Otherwise, multiple chunks are used to transmit each video line.	RW

9.2.16 VID_NULL_SIZE

This register configures the size of null packets.

																													BASE + 0x044	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																			vid_null_size												
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:13	Reserved	Reserved	R
12:0	vid_null_size	This register configures the number of bytes inside a null packet. Setting it to 0 disables the null packets.	RW

9.2.17 VID_HSA_TIME

This register configures the video Horizontal Synchronism Active (HSA) time.

																														BASE + 0x048	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																vid_hsa_time															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Reserved	R
11:0	vid_hsa_time	This field configures the Horizontal Synchronism Active period in lane byte clock cycles.	RW

9.2.18 VID_HBP_TIME

This register configures the video Horizontal Back Porch (HBP) time.

																														BASE + 0x04C	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																vid_hbp_time															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Reserved	R
11:0	vid_hbp_time	This field configures the Horizontal Back Porch period in lane byte clock cycles.	RW

9.2.19 VID_HLINE_TIME

This register configures the overall time for each video line

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

																														BASE + 0x050	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																vid_hline_time															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:15	Reserved	Reserved	R
14:0	vid_hline_time	This field configures the size of the total line time (HSA+HBP+HACT+HFP) counted in lane byte clock cycles.	RW

9.2.20 VID_HSA_LINES

This register configures the Vertical Synchronism Active (VSA) period.

																													BASE + 0x054	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																						vsa_lines									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:10	Reserved	Reserved	R
9:0	vsa_lines	This field configures the Vertical Synchronism Active period measured in number of horizontal lines.	RW

9.2.21 VID_VBP_HLINES

This register configures the Vertical Back Porch (VBP) period.

																													BASE + 0x058	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																						vbp_lines									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:10	Reserved	Reserved	R
9:0	vbp_lines	This field configures the Vertical Back Porch period measured in number of horizontal lines.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.2.22 VID_VFP_LINES

This register configures the Vertical Front Porch (VFP) period.

																														BASE + 0x05C	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																						vfp_lines									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:10	Reserved	Reserved	R
9:0	vfp_lines	This field configures the Vertical Front Porch period measured in number of horizontal lines.	RW

9.2.23 VID_VACTIVE_LINES

This register configures the vertical resolution of the video.

																													BASE + 0x060	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		v_active_lines													
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:14	Reserved	Reserved	R
13:0	v_active_lines	This field configures the Vertical Active period measured in number of horizontal lines.	RW

9.2.24 EDPI_CMD_SIZE

This register configures the size of the eDPI packets.

																													BASE + 0x064	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																edpi_allowed_cmd_size															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Reserved	R
15:0	edpi_allowed_cmd_size	This field configures the maximum allowed size for an eDPI	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		write memory command, measured in pixels. Automatic partitioning of data obtained from eDPI is permanently enabled.	

9.2.25 CMD_MODE_CFG

This register configures several aspects of the command mode operation, tearing effect, acknowledge for each packet, and the speed mode to transmit each data type related to commands.

BASE + 0x068

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							max_rd_pk	Reserved				dcs_lw_tx	dcs_sr_0p	dcs_sr_1p	dcs_sw_0p	Reserved	gen_lw_tx	gen_sr_2p	gen_sr_1p	gen_sr_0p	gen_sw_2	gen_sw_1	gen_sw_0	Reserved						ack_rqst	tear_fx_en
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:25	Reserved	Reserved	R
24	max_rd_pkt_size	This bit configures the maximum read packet size command transmission type: 0: High-speed 1: Low-power	RW
23:20	Reserved	Reserved	R
19	dcs_lw_tx	This bit configures the DCS long write packet command transmission type: 0: High-speed 1: Low-power	RW
18	dcs_sr_0p_tx	This bit configures the DCS short read packet with zero parameter command transmission type: 0: High-speed 1: Low-power	RW
17	dcs_sw_1p_tx	This bit configures the DCS short write packet with one parameter command transmission type: 0: High-speed 1: Low-power	RW
16	dcs_sw_0p_tx	This bit configures the DCS short write packet with zero parameter command transmission type: 0: High-speed 1: Low-power	RW
15	Reserved	Reserved	R
14	gen_lw_tx	This bit configures the Generic long write packet command transmission type:	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: High-speed 1: Low-power	
13	gen_sr_2p_tx	This bit configures the Generic short read packet with two parameters command transmission type: 0: High-speed 1: Low-power	RW
12	gen_sr_lp_tx	This bit configures the Generic short read packet with one parameter command transmission type: 0: High-speed 1: Low-power	RW
11	gen_sr_0p_tx	This bit configures the Generic short read packet with zero parameter command transmission type: 0: High-speed 1: Low-power	RW
10	gen_sw_2p_tx	This bit configures the Generic short write packet with two parameters command transmission type: 0: High-speed 1: Low-power	RW
9	gen_sw_1p_tx	This bit configures the Generic short write packet with one parameter command transmission type: 0: High-speed 1: Low-power	RW
8	gen_sw_0p_tx	This bit configures the Generic short write packet with zero parameter command transmission type: 0: High-speed 1: Low-power	RW
7:2	Reserved	Reserved	R
1	ack_rqst_en	When set to 1, this bit enables the acknowledge request after each packet transmission.	RW
0	tear_fx_en	When set to 1, this bit enables the tearing effect acknowledge request.	RW

9.2.26 GEN_HDR

This register sets the header for new packets sent using the Generic interface.

																														BASE + 0x06C	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								gen_wc_msbyte								gen_wc_lsbyte								gen_vc		gen_dt					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:24	Reserved	Reserved	R
23:16	gen_wc_msbyte	This field configures the most significant byte of the header packet's word count for long packets or data 1 for short packets.	RW
15:8	gen_wc_lsbyte	This field configures the least significant byte of the header packet's Word count for long packets or data 0 for short packets.	RW
7:6	gen_vc	This field configures the virtual channel id of the header packet.	RW
5:0	gen_dt	This field configures the packet data type of the header packet.	RW

9.2.27 GEN_PLD_DATA

This register sets the payload for the packets sent using the Generic interface and, when read, returns the contents of the read responses from the peripheral.

BASE + 0x070

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	gen_pld_b4								gen_pld_b3								gen_pld_b2								gen_pld_b1							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	gen_pld_b4	This field indicates byte 4 of the packet payload.	RW
23:16	gen_pld_b3	This field indicates byte 3 of the packet payload.	RW
15:8	gen_pld_b2	This field indicates byte 2 of the packet payload.	RW
7:0	gen_pld_b1	This field indicates byte 1 of the packet payload.	RW

9.2.28 CMD_PKT_STATUS

This register contains information about the status of the FIFOs related to the DBI and the Generic interfaces.

BASE + 0x074

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									gen_rd_cm	gen_pld_r	gen_pld_r	gen_pld_f	gen_pld_e	gen_cmd_f	gen_cd_e
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1	0	1	0	1

Bits	Name	Description	RW
31:7	Reserved	Reserved	R
6	gen_rd_cmd_busy	This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO.	
5	gen_pld_r_full	This bit indicates the full status of the generic read payload	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		FIFO.	
4	gen_pld_r_empty	This bit indicates the empty status of the generic read payload FIFO.	R
3	gen_pld_w_ful	This bit indicates the full status of the generic write payload FIFO.	R
2	gen_pld_w_empty	This bit indicates the empty status of the generic write payload FIFO.	R
1	gen_cmd_full	This bit indicates the full status of the generic command FIFO.	R
0	gen_cmd_empty	This bit indicates the empty status of the generic command FIFO.	R

9.2.29 TO_CNT_CFG

This register configures the counters that trigger the timeout errors. These are used to warn the system about a failure, through an interrupt, and restart the core in case of unexpected situations that cause deadlock conditions.

																	BASE + 0x078														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	hstx_to_cnt																lprx_to_cnt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	hstx_to_cnt	This field configures the timeout counter that triggers a high-speed transmission timeout contention detection (measured in TO_CLK_DIVISION cycles). If using the non-burst mode and there is no sufficient time to switch from HS to LP and back in the period which is from one line data finishing to the next line sync start, the DSI link returns the LP state once per frame, then you should configure the TO_CLK_DIVISION and hstx_to_cnt to be in accordance with: hstx_to_cnt * lanebyteclkperiod * TO_CLK_DIVISION >= the time of one FRAME data transmission * (1 + 10%) In burst mode, RGB pixel packets are time-compressed, leaving more time during a scan line. Therefore, if in burst mode and there is sufficient time to switch from HS to LP and back in the period of time from one line data finishing to the next line sync start, the DSI link can return LP mode and back in this time interval to save power. For this, configure the TO_CLK_DIVISION and hstx_to_cnt to be in accordance with: hstx_to_cnt * lanebyteclkperiod * TO_CLK_DIVISION >= the time of one LINE data transmission * (1 + 10%)	
15:0	lprx_to_cnt	This field configures the timeout counter that triggers a low-power	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		reception timeout contention detection (measured in TO_CLK_DIVISION cycles).	

9.2.30 HS_RD_TO_CNT

This register configures the Peripheral Response timeout after high-speed read operations.

																	BASE + 0x07C														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																hs_rd_to_cnt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Reserved	R
15:0	hs_rd_to_cnt	This field sets a period for which the MIPI DSI Controller keeps the link still, after sending a high-speed read operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.	RW

9.2.31 LP_RD_TO_CNT

This register configures the Peripheral Response timeout after the low-power read operations..

																	BASE + 0x080														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																lp_rd_to_cnt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Reserved	R
0	lp_rd_to_cnt	This field sets a period for which the MIPI DSI Controller keeps the link still, after sending a low-power read operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.	RW

9.2.32 HS_WR_TO_CNT

This register configures the Peripheral Response timeout after the high-speed write operations.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

																	BASE + 0x084													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							presp_to_	Reserved								hs_wr_to_cnt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:25	Reserved	Reserved	R
24	presp_to_mode	When set to 1, this bit ensures that the peripheral response timeout caused by hs_wr_to_cnt is used only once per eDPI frame, when both the following conditions are met: dpivsync_edpiwms has risen and fallen. Packets originated from eDPI have been transmitted and its FIFO is empty again. In this scenario no non-eDPI requests are sent to the D-PHY, even if there is traffic from generic or DBI ready to be sent, making it return to stop state. When it does so, PRESP_TO counter is activated and only when it finishes does the controller send any other traffic that is ready.	RW
23:16	Reserved	Reserved	R
15:0	hs_wr_to_cnt	This field sets a period for which the MIPI DSI Controller keeps the link inactive after sending a high-speed write operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.	RW

9.2.33 LP_WR_TO_CNT

This register configures the Peripheral Response timeout after the low-power write operations.

																	BASE + 0x088													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																lp_wr_to_cnt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Reserved	R
15:0	lp_wr_to_cnt	This field sets a period for which the MIPI DSI Controller keeps the link still, after sending a low-power write operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.2.34 BTA_TO_CNT

This register configures the Peripheral Response timeout after the Bus Turnaround completion.

																	BASE + 0x08C														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																bta_to_cnt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Reserved	R
15:0	bta_to_cnt	This field sets a period for which the MIPI DSI Controller keeps the link still, after completing a Bus Turn-Around. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.	RW

9.2.35 SOF_3D

This register stores the 3D control information for the VSS packets in video mode.

																	BASE + 0x004														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															send_3d	Reserved										right_fist	second_vs	format_3d		mode_3d	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:17	Reserved	Reserved	R
16	send_3d_cfg	When set, causes the next VSS packet to include 3D control payload in every VSS packet.	RW
15:6	Reserved	Reserved	R
5	right_first	This bit defines the left or right order: 0: Left eye data is sent first, and then the right eye data is sent. 1: Right eye data is sent first, and then the left eye data is sent.	RW
4	second_vsync	This field defines whether there is a second VSYNC pulse between Left and Right Images, when 3D Image Format is Frame-based: 0: No sync pulses between left and right data 1: Sync pulse (HSYNC, VSYNC, blanking) between left and right data	RW
3:2	format_3d	This field defines the 3D image format:	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		00: Line (alternating lines of left and right data) 01: Frame (alternating frames of left and right data) 10: Pixel (alternating pixels of left and right data) 11: Reserved	
1:0	mode_3d	This field defines the 3D mode on/off and display orientation: 00: 3D mode off (2D mode on) 01: 3D mode on, portrait orientation 10: 3D mode on, landscape orientation 11: Reserved	RW

9.2.36 LPCLK_CTRL

This register configures using the non-continuous clock in the clock lane.

																														BASE + 0x004	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														auto_clkla	phy_txreq
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Reserved	R
1	auto_clklane_ctrl	This bit enables the automatic mechanism to stop providing clock in the clock lane when time allows.	RW
0	phy_txrequestclkhs	This bit controls the D-PHY PPI txrequestclkhs signal.	RW

9.2.37 PHY_TMR_LPCLK_CFG

This register sets the time that the MIPI DSI Controller assumes in calculations for the clock lane to switch between high-speed and low-power.

																														BASE + 0x098	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						phy_clkhs2lp_time										Reserved						phy_clklp2hs_time									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Reserved	R
25:16	phy_clkhs2lp_time	This field configures the maximum time that the D-PHY clock lane takes to go from high-speed to low-power transmission measured in lane byte clock cycles.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

15:10	Reserved	Reserved	R
9:0	phy_clklp2hs_time	This field configures the maximum time that the D-PHY clock lane takes to go from low-power to high-speed transmission measured in lane byte clock cycles.	RW

9.2.38 PHY_TMR_CFG

This register sets the time that the MIPI DSI Controller assumes in calculations for the data lanes to switch between high-speed and low-power.

BASE + 0x09C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	phy_hs2lp_time								phy_lp2hs_time								Reserved	max_rd_time														
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	phy_hs2lp_time	This field configures the maximum time that the D-PHY data lanes take to go from high-speed to low-power transmission measured in lane byte clock cycles.	R
23:16	phy_lp2hs_time	This field configures the maximum time that the D-PHY data lanes take to go from low-power to high-speed transmission measured in lane byte clock cycles.	RW
15	Reserved	Reserved	R
14:0	max_rd_time	This field configures the maximum time required to perform a read command in lane byte clock cycles. This register can only be modified when no read command is in progress.	RW

9.2.39 PHY_RSTZ

This register controls the resets and the PLL of the D-PHY.

BASE + 0x0A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												phy_forcep	phy_enab	phy_rstz	phy_shutd
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Reserved	R
3	phy_forcepll	When the D-PHY is in ULPS, this bit enables the D-PHY PLL..	RW
2	phy_enableclk	When set to1, this bit enables the D-PHY Clock Lane module.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	phy_rstz	When set to 0, this bit places the digital section of the D-PHY in the reset state.	RW
0	phy_shutdownz	When set to 0, this bit places the D-PHY macro in power-down state.	RW

9.2.40 PHY_IF_CFG

This register configures the number of active lanes and the minimum time to remain in the Stop state.

BASE + 0x0A4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																phy_stop_wait_time								Reserved						n_lanes	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Reserved	R
15:8	phy_stop_wait_time	This field configures the minimum wait period to request a high-speed transmission after the Stop state.	RW
7:2	Reserved	Reserved	R
1:0	n_lanes	This field configures the number of active data lanes: 00: One data lane (lane 0) 01: Two data lanes (lanes 0 and 1) 10-11: Reserved	RW

9.2.41 PHY_ULPS_CTRL

This register configures entering and leaving the ULPS in the D-PHY.

BASE + 0x0A8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												phy_txexit	phy_txreq	phy_txexit	phy_txreq
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Reserved	R
3	phy_txexitulpslan	ULPS mode Exit on all active data lanes.	RW
2	phy_txrequlpslan	ULPS mode Request on all active data lanes.	RW
1	phy_txexitulpsclk	ULPS mode Exit on clock lane.	RW
0	phy_txrequlpsclk	ULPS mode Request on clock lane.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.2.42 PHY_TX_TRIGGERS

This register configures the signals that activate the triggers in the D-PHY.

																	BASE + 0x0AC														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												phy_tx_tri			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Reserved	R
3:0	phy_tx_triggers	This field controls the trigger transmissions.	RW

9.2.43 PHY_STATUS

This register contains information about the status of the D-PHY.

																													BASE + 0x0B0		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																							phy_ulpsa	phy_stop	phy_rxulps	phy_ulpsa	phy_stop	phy_ulpsa	phy_stopst	phy_direct	phy_lock
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	0	1	0	0	0

Bits	Name	Description	RW
31:9	Reserved	Reserved	R
8	phy_ulpsactivenot1lane	This bit indicates the status of ulpsactivenot1lane D-PHY signal.	RW
7	phy_stopstate1lane	This bit indicates the status of phystopstate1lane D-PHY signal.	RW
6	phy_rxulpsesc0lane	This bit indicates the status of rxulpsesc0lane D-PHY signal.	RW
5	phy_ulpsactivenot0lane	This bit indicates the status of ulpsactivenot0lane D-PHY signal.	RW
4	phy_stopstate0lane	This bit indicates the status of phystopstate0lane D-PHY signal.	RW
3	phy_ulpsactivenotclk	This bit indicates the status of phyulpsactivenotclk D-PHY signal.	RW
2	phy_stopstateclklane	This bit indicates the status of phystopstateclklane D-PHY signal.	RW
1	phy_direction	This bit indicates the status of phydirection D-PHY signal.	RW
0	phy_lock	This bit indicates the status of phylock D-PHY signal.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.2.44 PHY_TST_CTRL0

This register controls the clock and the clear signals of the D-PHY vendor specific interface.

																	BASE + 0x0B4														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														phy_testclk	phy_testclr
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:2	Reserved	Reserved	R
1	phy_testclk	This bit is used to clock the TESTDIN bus into the D-P	
0	phy_testclr	PHY test interface clear (active high	RW

9.2.45 PHY_TST_CTRL1

This register controls the data and the enable pins of the D-PHY vendor specific interface.

																	BASE + 0x0B8														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															phy_testen	phy_testdout								phy_testdin							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:17	Reserved	Reserved	R
16	phy_testen	PHY test interface operation selector: 1: The address write operation is set on the falling edge of the testclk signal. 0: The data write operation is set on the rising edge of the testclk signal.	RW
15:8	pht_testdout	PHY output 8-bit data bus for read-back and internal probing functionalities.	R
7:0	phy_testdin	PHY test interface input 8-bit data bus for internal register programming and test functionalities access	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9.2.46 INT_ST0

This register contains the status of the interrupt sources from the acknowledge reports and the D-PHY.

																	BASE + 0x0BC													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											errors_4	errors_3	errors_2	errors_1	errors_0	ack_err_15	ack_err_14	ack_err_13	ack_err_12	ack_err_11	ack_err_10	ack_err_9	ack_err_8	ack_err_7	ack_err_6	ack_err_5	ack_err_4	ack_err_3	ack_err_2	ack_err_1	ack_err_0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:21	Reserved	Reserved	R
20	dphy_errors_4	This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0.	R
19	dphy_errors_3	This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0.	R
18	dphy_errors_2	This bit indicates the ErrControl error from Lane 0.	R
17	dphy_errors_1	This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0.	R
16	dphy_errors_0	This bit indicates ErrEsc escape entry error from Lane 0.	R
15	ack_with_err_15	This bit retrieves the DSI protocol violation from the Acknowledge error report.	R
14	ack_with_err_14	This bit retrieves the reserved (specific to device) from the Acknowledge error report.	R
13	ack_with_err_13	This bit retrieves the invalid transmission length from the Acknowledge error report.	R
12	ack_with_err_12	This bit retrieves the DSI VC ID Invalid from the Acknowledge error report.	R
11	ack_with_err_11	This bit retrieves the not recognized DSI data type from the Acknowledge error report.	R
10	ack_with_err_10	This bit retrieves the checksum error (long packet only) from the Acknowledge error report.	R
9	ack_with_err_9	This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error report.	R
8	ack_with_err_8	This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error report.	R
7	ack_with_err_7	This bit retrieves the reserved (specific to device) from the Acknowledge error report.	R
6	ack_with_err_6	This bit retrieves the False Control error from the Acknowledge error report.	R
5	ack_with_err_5	This bit retrieves the Peripheral Timeout error from the Acknowledge	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Error report.	
4	ack_with_err_4	This bit retrieves the LP Transmit Sync error from the Acknowledge error report.	R
3	ack_with_err_3	This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report.	R
2	ack_with_err_2	This bit retrieves the EoT Sync error from the Acknowledge error report.	R
1	ack_with_err_1	This bit retrieves the SoT Sync error from the Acknowledge error report.	R
0	ack_with_err_0	This bit retrieves the SoT error from the Acknowledge error report	R

9.2.47 INT_ST1

This register contains the status of the interrupt sources related to timeouts, ECC, CRC, packet size, EoTp, Generic, and DBI interfaces.

																													BASE + 0x0C0	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																			gen_pld_re	gen_pld_r	gen_pld_s	gen_pld_w	gen_cmd_	dpi_pld_w	eopt_err	pkt_size_e	crc_err	ecc_multi	ecc_si_e	to_lp_rx	to_hs_tx
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:13	Reserved	Reserved	R
12	gen_pld_recev_err	This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted.	R
11	gen_pld_rd_err	This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted.	R
10	gen_pld_send_err	This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent.	R
9	gen_pld_wr_err	This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written.	R
8	gen_cmd_wr_err	This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written.	R
7	dpi_pld_wr_err	This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted.	R
6	eopt_err	This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

5	pkt_size_err	This bit indicates that the packet size error is detected during the packet reception.	R
4	crc_err	This bit indicates that the CRC error is detected in the received packet payload.	R
3	ecc_multi_err	This bit indicates that the ECC multiple error is detected in a received packet.	R
2	ecc_single_err	This bit indicates that the ECC single error is detected and corrected in a received packet.	R
1	to_lp_rx	This bit indicates that the low-power reception timeout counter reached the end and contention is detected.	R
0	to_hs_tx	This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected.	R

9.2.48 INT_MSK0

This register configures the masks for the sources of interrupts that affect the INT_ST0 register.

																	BASE + 0x0C4														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											errors_4	errors_3	errors_2	errors_1	errors_0	ack_err_15	ack_err_14	ack_err_13	ack_err_12	ack_err_11	ack_err_10	ack_err_9	ack_err_8	ack_err_7	ack_err_6	ack_err_5	ack_err_4	ack_err_3	ack_err_2	ack_err_1	ack_err_0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:21	Reserved	Reserved	R
20	dphy_errors_4	This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0.	R
19	dphy_errors_3	This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0.	R
18	dphy_errors_2	This bit indicates the ErrControl error from Lane 0.	R
17	dphy_errors_1	This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0.	R
16	dphy_errors_0	This bit indicates ErrEsc escape entry error from Lane 0.	R
15	ack_with_err_15	This bit retrieves the DSI protocol violation from the Acknowledge error report.	R
14	ack_with_err_14	This bit retrieves the reserved (specific to device) from the Acknowledge error report.	R
13	ack_with_err_13	This bit retrieves the invalid transmission length from the Acknowledge error report.	R
12	ack_with_err_12	This bit retrieves the DSI VC ID Invalid from the Acknowledge error	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		report.	
11	ack_with_err_11	This bit retrieves the not recognized DSI data type from the Acknowledge error report.	R
10	ack_with_err_10	This bit retrieves the checksum error (long packet only) from the Acknowledge error report.	R
9	ack_with_err_9	This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error report.	R
8	ack_with_err_8	This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error report.	R
7	ack_with_err_7	This bit retrieves the reserved (specific to device) from the Acknowledge error report.	R
6	ack_with_err_6	This bit retrieves the False Control error from the Acknowledge error report.	R
5	ack_with_err_5	This bit retrieves the Peripheral Timeout error from the Acknowledge Error report.	R
4	ack_with_err_4	This bit retrieves the LP Transmit Sync error from the Acknowledge error report.	R
3	ack_with_err_3	This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report.	R
2	ack_with_err_2	This bit retrieves the EoT Sync error from the Acknowledge error report.	R
1	ack_with_err_1	This bit retrieves the SoT Sync error from the Acknowledge error report.	R
0	ack_with_err_0	This bit retrieves the SoT error from the Acknowledge error report	R

9.2.49 INT_MSK1

This register configures the masks for the sources of the interrupts that affect the INT_ST1 register.

																					BASE + 0x0C8										
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																			gen_pld_re	gen_pld_r	gen_pld_s	gen_pld_w	gen_cmd_	dpi_pld_w	eopt_err	pkt_size_e	crc_err	ecc_multi	ecc_si_e	to_lp_rx	to_hs_tx
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:13	Reserved	Reserved	R
12	gen_pld_recev_err	This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

11	gen_pld_rd_err	This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted.	R
10	gen_pld_send_err	This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent.	R
9	gen_pld_wr_err	This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written.	R
8	gen_cmd_wr_err	This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written.	R
7	dpi_pld_wr_err	This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted.	R
6	eopt_err	This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission.	R
5	pkt_size_err	This bit indicates that the packet size error is detected during the packet reception.	R
4	crc_err	This bit indicates that the CRC error is detected in the received packet payload.	R
3	ecc_multi_err	This bit indicates that the ECC multiple error is detected in a received packet.	R
2	ecc_single_err	This bit indicates that the ECC single error is detected and corrected in a received packet.	R
1	to_lp_rx	This bit indicates that the low-power reception timeout counter reached the end and contention is detected.	R
0	to_hs_tx	This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected.	R

9.2.50 INT_FORCE0

This register configures the masks for the sources of interrupts that affect the INT_ST0 register.

																	BASE + 0x0D8														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											errors_4	errors_3	errors_2	errors_1	errors_0	ack_err_15	ack_err_14	ack_err_13	ack_err_12	ack_err_11	ack_err_10	ack_err_9	ack_err_8	ack_err_7	ack_err_6	ack_err_5	ack_err_4	ack_err_3	ack_err_2	ack_err_1	ack_err_0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:21	Reserved	Reserved	R
20	dphy_errors_4	This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

19	dphy_errors_3	This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0.	R
18	dphy_errors_2	This bit indicates the ErrControl error from Lane 0.	RW
17	dphy_errors_1	This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0.	R
16	dphy_errors_0	This bit indicates ErrEsc escape entry error from Lane 0.	R
15	ack_with_err_15	This bit retrieves the DSI protocol violation from the Acknowledge error report.	R
14	ack_with_err_14	This bit retrieves the reserved (specific to device) from the Acknowledge error report.	R
13	ack_with_err_13	This bit retrieves the invalid transmission length from the Acknowledge error report.	R
12	ack_with_err_12	This bit retrieves the DSI VC ID Invalid from the Acknowledge error report.	R
11	ack_with_err_11	This bit retrieves the not recognized DSI data type from the Acknowledge error report.	R
10	ack_with_err_10	This bit retrieves the checksum error (long packet only) from the Acknowledge error report.	R
9	ack_with_err_9	This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error report.	R
8	ack_with_err_8	This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error report.	R
7	ack_with_err_7	This bit retrieves the reserved (specific to device) from the Acknowledge error report.	R
6	ack_with_err_6	This bit retrieves the False Control error from the Acknowledge error report.	R
5	ack_with_err_5	This bit retrieves the Peripheral Timeout error from the Acknowledge Error report.	R
4	ack_with_err_4	This bit retrieves the LP Transmit Sync error from the Acknowledge error report.	R
3	ack_with_err_3	This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report.	R
2	ack_with_err_2	This bit retrieves the EoT Sync error from the Acknowledge error report.	R
1	ack_with_err_1	This bit retrieves the SoT Sync error from the Acknowledge error report.	R
0	ack_with_err_0	This bit retrieves the SoT error from the Acknowledge error report	R

9.2.51 INT_FORCE1

This register configures the masks for the sources of the interrupts that affect the INT_ST1 register.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

																														BASE + 0x0DC	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																			gen_pld_re	gen_pld_r	gen_pld_s	gen_pld_w	gen_cmd_	dpi_pld_w	eopt_err	pkt_size_e	crc_err	ecc_multi	ecc_si_e	to_lp_rx	to_hs_tx
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:13	Reserved	Reserved	R
12	gen_pld_recev_err	This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted.	R
11	gen_pld_rd_err	This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted.	R
10	gen_pld_send_err	This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent.	R
9	gen_pld_wr_err	This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written.	R
8	gen_cmd_wr_err	This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written.	R
7	dpi_pld_wr_err	This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted.	R
6	eopt_err	This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission.	R
5	pkt_size_err	This bit indicates that the packet size error is detected during the packet reception.	R
4	crc_err	This bit indicates that the CRC error is detected in the received packet payload.	R
3	ecc_multi_err	This bit indicates that the ECC multiple error is detected in a received packet.	R
2	ecc_single_err	This bit indicates that the ECC single error is detected and corrected in a received packet.	R
1	to_lp_rx	This bit indicates that the low-power reception timeout counter reached the end and contention is detected.	R
0	to_hs_tx	This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected.	R

9.2.52 VID_SHADOW_CTRL

This register controls the DPI shadow register mechanism feature.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

																	BASE + 0x100													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															vid_sh_pin	Reserved							vid_sh_req	Reserved							vid_sh_en
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:17	Reserved	Reserved	R
16	vid_shadow_pin_req	When set to 1, the video request is done by external pin. In this mode, vid_shadow_req is ignored.	RW
15:9	Reserved	Reserved	R
8	vid_shadow_req	When set to 1, the DPI registers are copied to the auxiliary registers. After copying, this bit is auto cleared.	RW
7:1	Reserved	Reserved	R
0	vid_shadow_en	When set to 1, DPI receives the active configuration from the auxiliary registers. When this bit is set along with the vid_shadow_req bit, the auxiliary registers are automatically updated.	RW

9.2.53 DPI_VCID_ACT

This register configures the virtual channel id for the DPI traffic.

																	BASE + 0x10C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														dpi_vcid	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Reserved	R
1:0	dpi_vcid	This field configures the DPI virtual channel id that is indexed to the Video mode packets.	RW

9.2.54 Static and Dynamic Registers

Some of the registers of the MIPI DSI Controller are static and can be configured only when the MIPI DSI Controller is idle and not transmitting. The dynamic registers can be configured when needed and do not require the MIPI DSI Controller to be in reset or idle.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Below table lists the static and dynamic registers.

Static Read/Write Registers	Dynamic Read/Write Registers	Static Read-Only Registers	Dynamic Read-Only/ Write-Only Registers
PWR_UP CLKMGR_CFG DPI_VCID PCKHDL_CFG VID_PKT_SIZE VID_HBP_TIME VID_VFP_LINES HS_RD_TO_CNT BTA_TO_CNT PHY_TMR_CFG DPI_COLOR_CODING DPI_CFG_POL DPI_LP_CMD_TIM GEN_VCID VID_MODE_CFG VID_NUM_CHUNKS VID_NULL_SIZE VID_HSA_TIME VID_HLINE_TIME VID_VSA_LINES VID_VBP_LINES VID_VACTIVE_LINES EDPI_CMD_SIZE CMD_MODE_CFG TO_CNT_CFG LP_RD_TO_CNT HS_WR_TO_CNT LP_WR_TO_CNT LPCLK_CTRL	MODE_CFG GEN_HDR GEN_PLD_DATA SDF_3D PHY_RSTZ PHY_ULPS_CTRL PHY_TX_TRIGGERS PHY_TST_CTRL0 PHY_TST_CTRL1 INT_MSK0 INT_MSK1 VID_SHADOW_CTRL	Read-Only: VERSION	Read-Only: CMD_PKT_STATUS PHY_STATUS INT_ST0 INT_ST1 DPI_VCID_ACT Write-Only: INT_FORCE0 INT_FORCE1

9.3 MIPI DSI Host Controller Guide

To operate MIPI DSI Controller, you must be familiar with the MIPI DSI specification.

9.3.1 Initializing MIPI DSI Host Controller and D-PHY

9.3.2 Configuring the DPI Resolution for Transmission

1. Global configuration: Configure n_lanes (PHY_IF_CFG) to define the number of lanes with which the controller can perform high-speed transmissions.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

2. Configure the DPI interface to define how the DPI interface interacts with the controller.
   1) Configure dpi_vcid (DPI_VCID): This field configures the virtual channel that the packets generated by the DPI interface is indexed to.
   2) Configure dpi_color_coding (DPI_COLOR_CODING): This field configures the bits per pixel that the interface transmits and also the variant configuration of each bpp. If you select 18 bpp, and multiple of four.
   3) Configure dataen_active_low (DPI_CFG_POL): This bit configures the polarity of the dpidataen signal and sets it to be active low.
   4) Configure vsync_active_low (DPI_CFG_POL): This bit configures the polarity of the dpivsync signal and sets it to be active low.
   5) Configure hsync_active_low (DPI_CFG_POL): This bit configures the polarity of the dpihsync signal and sets it to be active low.
   6) Configure shutd_active_low (DPI_CFG_POL): This bit configures the polarity of the dpishutdn signal and sets it to be active low.
   7) Configure colorm_active_low (DPI_CFG_POL): This bit configures the polarity of the dpicolorm signal and sets it to be active low.
   8) Configure loosely18_en (DPI_COLOR_CODING): This bit configures if the pixel packing is done loosely or packed when dpi_color_coding is 18 bpp. This bit enables loosely packing.
3. Select the Video transmission mode to define how the processor requires the video line to be transported through the DSI link.
   1) Configure the low-power transitions (VID_MODE_CFG): This defines the video periods which are permitted to go to low-power if there is time available to do so.
   2) Configure frame_bta_ack_en (VID_MODE_CFG): This specifies if the controller should request the peripheral acknowledge message at the end of frames. Configure lp_cmd_en (VID_MODE_CFG): This specifies that commands are to be transmitted in low-power.
   3) Burst mode:
      a) Configure the register field vid_mode_type (VID_MODE_CFG) with value 2'b1x. Configure vid_pkt_size (VID_PKT_SIZE) with the size of the active line period, measured in pixels.
      b) The fields vid_num_chunks and vid_null_size are ignored by the MIPI DSI Controller.
   4) Non-Burst mode:
      a) Configure the vid_mode_type field (VID_MODE_CFG) with 2'b0x.
      b) Configure the vid_mode_type field (VID_MODE_CFG) with 2'b00 to enable the transmission of sync pulses.
      c) Configure the vid_mode_type field (VID_MODE_CFG) with 2'b01 to enable the transmission of sync events.
      d) Configure the vid_pkt_size field (VID_MODE_CFG) with the number of pixels to be transmitted in a single packet. Selecting this value depends on

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

the available memory of the attached peripheral, if the data is first stored, or on the memory you want to select for the FIFOs in MIPI DSI Controller.

e) Configure the vid_num_chunks field (VID_NUM_CHUNKS) with the number of packets to be transmitted per video line. The value of vid_pkt_size * vid_num_chunks is the number of pixels per line of video, except if vid_num_chunks is 0, which disables the multi-packets. If you set it to 1, there is still only one packet per line, but it can be part of a chunk, followed by a null packet.

f) Configure the vid_null_size field (VID_NULL_SIZE) with the size of null packets to be inserted as part of the chunks. Setting it to 0 disables null packets.

4. Define the DPI Horizontal timing configuration as follows:
   1) Configure the vid_hline_time field (VID_HLINE_TIME) with the time taken by a DPI video line measured in cycles of lane byte clock (for a clock lane at 500 MHz the lane byte clock period is 8 ns). When the periods of DPI clock and lane byte clock are not multiples, the value to program the vid_hline_time needs to be rounded. A timing mismatch is introduced between the lines due to the rounding of configuration values. If the MIPI DSI Controller is configured not to go to low-power, this timing divergence accumulates on every line, introducing a significant amount of mismatch towards the end of the frame. The reason for this is that the MIPI DSI Controller cannot re-synchronize on every new line because it transmits the blanking packets when the Horizontal Sync event occurs on the DPI interface. However, the accumulated mismatch should become extinct on the last line of a frame, where, according to the DSI specification, the link should always return to low-power regaining synchronization, when a new frame starts on a vertical sync event. If the accumulated timing mismatch is greater than the time in low-power on the last line, a malfunction occurs. This phenomenon can be avoided by configuring the MIPI DSI Controller to go to low-power once per line.
   2) Configure the vid_hsa_time field (VID_HSA_TIME) with the time taken by a DPI Horizontal Sync Active period measured in cycles of lane byte clock (normally a period of 8 ns).
   3) Configure the vid_hbp_time field (VID_HBP_TIME) with the time taken by the DPI Horizontal Back Porch period measured in cycles of lane byte clock (normally a period of 8 ns). Special attention should be given to the calculation of this parameter.
5. Define the Vertical line configuration:
   1) Configure the vsa_lines field (VID_VSA_LINES) with the number of lines existing in the DPI Vertical Sync Active period.
   2) Configure the vbp_lines field (VID_VBP_LINES]) with the number of lines existing in the DPI Vertical Back Porch period.
   3) Configure the vfp_lines field (VID_VFP_LINES) with the number of lines existing in the DPI Vertical Front Porch period.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4) Configure the v_active_lines field (VID_VACTIVE_LINES) with the number of lines existing in the DPI Vertical Active Period.

6. Illustrates the steps for configuring the DPI packet transmission.

9.3.3 Initializing D-PHY

1. By default, the PHY_RSTZ register activates the D-PHY reset signals physhutdownz and phyrstz, and disables the enableclk signal. The PHY_TST_CTRL0 register, by default, asserts the testclr signal. All the D-PHY reset pins are activated by default.
2. Configure the PHY_IF_CFG register with the number of lanes to be used by the MIPI DSI Controller.
3. Configure the TX_ESC clock frequency to a frequency lower than 20 MHz, the maximum allowed frequency for the D-PHY escape mode. This is done by writing into tx_esc_clk_division field of the CLKMGR_CFG register. The tx_esc_clk_division field divides the byte clock, and generates a TX_ESC clock for the D-PHY.
4. Configure the D-PHY PLL clock frequency through the Test interface.
5. Configure bit 0 of the register LPCLK_CTRL to generate high-speed clock TXREQUESTHSCLK.
6. Only after the PLL is locked and clock lane is in the Stop state, D-PHY drives the correct LP sequence to configure the receiver end for HS.
7. The D-PHY starts transmitting HS clock on the clock lane.

9.3.4 Video Mode Pattern Generator

1. Configure the MODE_CFG register to enable Video mode. Configure the Video mode type using VID_MODE_CFG[1:0] configuration pins.
2. Configure the DPI_COLOR_CODING register.
3. Configure the frame using registers.
4. Configure the pattern generation mode (VID_MODE_CFG [20]) and pattern orientation (VID_MODE_CFG[24]) and enable it (VID_MODE_CFG[16]).

9.3.5 ULPM Flow

9.3.6 Process Flow to Enter the ULPM

1. Verify the initial status of the MIPI DSI Controller:
   1) PHY_RSTZ[3:0] = 4'hF
   2) PHY_ULPS_CTRL[3:0] = 4'h0
   3) PHY_TX_TRIGGERS[3:0] = 4'h0
   4) Verify that all active lanes are in Stop state and the D-PHY PLL is locked:
      a) One-lane configuration:
         PHY_STATUS[6:4] = 3'h3
         PHY_STATUS[1:0] = 2'h1
      b) Two -lanes configuration:
         PHY_STATUS[8:4] = 5'h1B
         PHY_STATUS[1:0] = 2'h1

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

2. Set PHY_ULPS_CTRL [3:0] = 4'hA to enter ULPM in the data and the clock lanes.
3. Wait until the D-PHY active lanes enter into ULPM:
   1) One-lane configuration: PHY_STATUS[6:0] = 7'h001
   2) Two-lanes configuration: PHY_STATUS[8:0] = 9'h001

   The MIPI DSI Controller is now in ULPM. To turn off the D-PHY PLL, perform the next two steps.
4. Turn off the D-PHY PLL by setting PHY_RSTZ[3] = 1'b0
5. Wait until the D-PHY PLL is unlocked: PHY_STATUS [0] = 1'b0

9.3.7 Process Flow to Exit the ULPM

1. Verify that all active lanes are in ULPM:
   1) One-lane configuration: PHY_STATUS[6:1] = 6'h00
   2) Two-lanes configuration: PHY_STATUS[8:1] = 8'h00
2. If the D-PHY PLL is already locked (PHY_STATUS [0] = 1'b1), go to step 5, else continue.
3. Turn on the D-PHY PLL by setting PHY_RSTZ [3] = 1'b1.
4. Wait until D-PHY PLL locked ： PHY_STATUS[0] = 1'b1
5. Without deasserting the ULPM request bits, assert the Exit ULPM bits by setting PHY_ULPS_CTRL[3:0] = 4'hF.
6. Wait until all active lanes exit ULPM:
   1) One-lane configuration:
      PHY_STATUS [5] = 1'b1
      PHY_STATUS [3] = 1'b1
   2) Two-lanes configuration:
      PHY_STATUS [8] = 1'b1
      PHY_STATUS [5] = 1'b1
      PHY_STATUS [3] = 1'b1
7. Wait for 1 ms.
8. Deassert the ULPM requests and the ULPM exit bits by setting PHY_ULPS_CTRL [3:0] = 4'h0.
9. The MIPI DSI Controller is now in Stop state and the D-PHY PLL is locked:
   1) One-lane configuration:
      PHY_STATUS [6:4] = 3'h3
      PHY_STATUS [1:0] = 2'h1
   2) Two-lanes configuration:
      PHY_STATUS [8:4] = 5'h1B
      PHY_STATUS [1:0] = 2'h1

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

10 MIPI_CSI Interface

10.1 Overview

The CSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 Specification, providing an interface between the System and the MIPI D-PHY, allowing the communication with a MIPI CSI-2 compliant Camera Sensor.

10.1.1 Features

- Support i2c interface to configure.
- Support up to 2 D-PHY Rx Data Lanes.
- Compliant with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2).
- Dynamically configurable multi-lane merging.
- Long and Short packet decoding.
- Timing accurate signaling of Frame and Line synchronization packets.
- 32-bit Image Data.
- Support all primary and secondary data formats:
  - RGB, YUV and RAW color space definitions
  - From 24-bit down to 6-bit per pixel
  - Generic or user-defined byte-based data types.
- Error detection and correction.

10.2 Register Descriptions

10.2.1 Register Mapping

Following chapter will descript the functions of all software accessible registers.
Conventions:
1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RW - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

The base address of MIPI_CSI is 0x13013000.

Table 10-1 MIPI_CSI Registers Description

Name	Description	RW	Reset Value	Offset Address	Width
VERSION	Version of the CSI-2 host controller	R	CSI_VERSION_ID	0x000	32
N_LANES	Number of active data lanes	R/W	CSI_N_LANES	0x004	2
PHY_SHUTDOWNZ	PHY shutdown control	R/W	0	0x008	1
DPHY_RSTZ	DPHY reset control	R/W	0	0x00c	1
CSI2_RESETN	CSI-2 controller reset	R/W	0	0x010	1
PHY_STATE	General settings for all blocks	R	0	0x014	12
DATA_IDS_1	List of Data Ids for which IDI reports line boundary matching errors (CSI2_HOST_N_DATA_IDS > 0)	R/W	0	0x018	32
DATA_IDS_2	List of Data Ids for which IDI reports line boundary matching errors (CSI2_HOST_N_DATA_IDS > 1)	R/W	0	0x01c	32
ERR1	Error state register 1	R	0	0x020	29
ERR2	Error state register 2	R	0	0x024	24
MASK1	Masks for errors 1	R/W	0	0x028	29
MASK2	Masks for errors 2	R/W	0	0x02c	24
PHY_TST_CRTL0	D-PHY Test interface control 0	R/W	0	0x030	2
PHY_TST_CRTL1	D-PHY Test interface control 1	R/W	0	0x034	17

10.2.2 VERSION

- Name: Controller Version Identification
- Address Offset:0x000
- Size:32 bits
- Value after Reset: CSI_VERSION_ID
- Access: Read

	VERSION																BASE+0x000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VERSION																															
RST																																

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:0	VERSION	Version of the CSI-2 Host Controller	R

10.2.3 N_LANES

- Address Offset:0x004
- Size:2 bits
- Value after Reset:CSI_N_LANES
- Access:Read/Write

	N_LANES																												BASE+0x004	
Bit																													1	0
																													N_LANES	
RST																														

Bits	Name	Description	R/W
1:0	N_LANES	Number of Active Data Lanes. • 00: 1 Data Lane (Lane 0) • 01: 2 Data Lanes (Lane 0, and 1) • 10: 3 Data Lanes (Lane 0,1 and 2) • 11: 4 Data Lanes (All) Can only be updated when the PHY lane is in stopstate	R/W

10.2.4 PHY_SHUTDOWNZ

- Name: Phy shutdown control
- Address Offset:0x008
- Size:1 bit
- Value after Reset:0
- Access: Read/Write

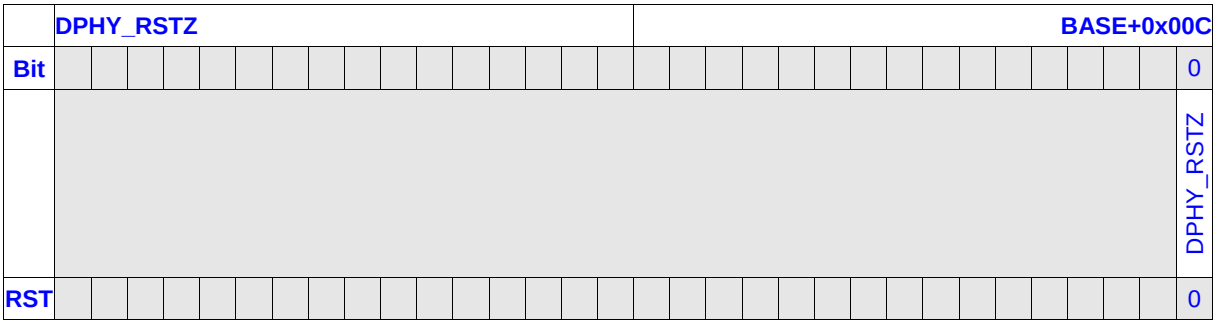
	PHY_SHUTDOWNZ																												BASE+0x008	
Bit																														0
																														PHY_SHUTDOWNZ
RST																														0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
0	PHY_SHUTDOWNZ	Shutdown input. This line is used to place the complete macro in power down. All analog blocks are in power down mode and digital logic is cleared. Active Low.	R/W

10.2.5 DPHY_RSTZ

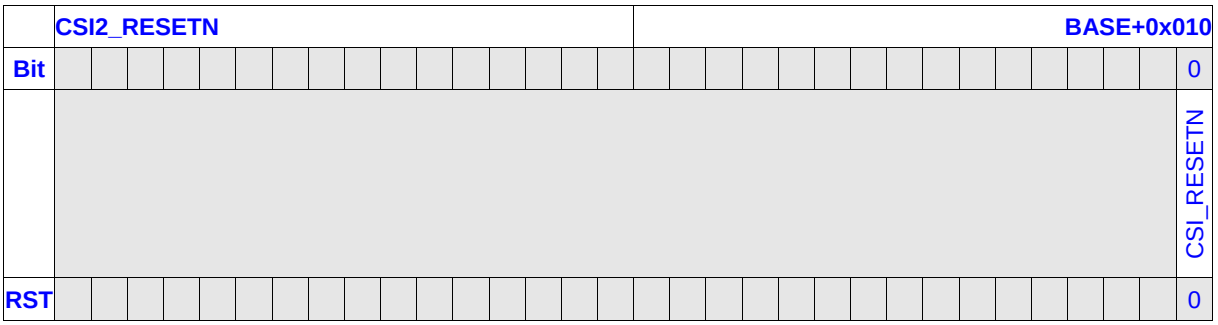
- Name: Phy reset control
- Address Offset:0x00C
- Size:1 bit
- Value after Reset:0
- Access: Read/Write



Bits	Name	Description	R/W
0	DPHY_RSTZ	DPHY reset output. Active Low.	R/W

10.2.6 CSI2_RESETN

- Name:CSI-2 controller reset
- Address Offset:0x010
- Size:1 bit
- Value after Reset:0
- Access: Read/Write



Bits	Name	Description	R/W
0	CSI_RESETN	CSI-2 controller reset output. Active Low.	R/W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

10.2.7 PHY_STATE

- Name: General settings for all blocks
- Address Offset:0x014
- Size:12 bits
- Value after Reset:0
- Access: Read (with the exception of bit 11 which is Read/Write)

	PHY_STATE																			BASE+0x014											
Bit																				11	10	9	8	7	6	5	4	3	2	1	0
																				bypass_2ecc_tst	phy_stopstateclk	phy_rxclkactivehs	phy_rxclkactiivehs	phy_stopstatedata_3	phy_stopstatedata_2	phy_stopstatedata_1	phy_stopstatedata_0	phy_rxulpsesc_3	phy_rxulpsesc_2	phy_rxulpsesc_1	phy_rxulpsesc_0
RST																				0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
0	phy_rxulpsesc_0	Lane module 0 has entered the Ultra Low Power mode	R
1	phy_rxulpsesc_1	Lane module 1 has entered the Ultra Low Power mode	R
2	phy_rxulpsesc_2	Lane module 2 has entered the Ultra Low Power mode	R
3	phy_rxulpsesc_3	Lane module 3 has entered the Ultra Low Power mode	R
4	phy_stopstatedata_0	Data Lane 0 in Stop state	R
5	phy_stopstatedata_1	Data Lane 1 in Stop state	R
6	phy_stopstatedata_2	Data Lane 2 in Stop state	R
7	phy_stopstatedata_3	Data Lane 3 in Stop state	R
8	phy_rxclkactivehs	Indicates that the clock lane is actively receiving a DDR clock	R
9	phy_rxulpsclknot	Active Low. This signal indicates that the Clock Lane module has entered the Ultra Low Power state	R
10	phy_stopstateclk	Clock Lane in Stop state	R
11	bypass_2ecc_tst	Payload Bypass test mode for double ECC errors	R/W

10.2.8 DATA_IDS_1

- Address Offset:0x018
- Size:32 bits
- Value after Reset:0
- Access: Read/Write

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	DATA_IDS_1																BASE+0x018													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	di3_vc		di3_dt						di2_vc		di2_dt						di1_vc		di1_dt						di0_vc		di0_dt					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
5:0	di0_dt	Data ID 0 Data Type	R/W
7:6	di0_vc	Data ID 0 Virtual channel	R/W
13:8	di1_dt	Data ID 1 Data Type	R/W
15:14	di1_vc	Data ID 1 Virtual channel	R/W
21:16	di2_dt	Data ID 2 Data Type	R/W
23:22	di2_vc	Data ID 2 Virtual channel	R/W
29:24	di3_dt	Data ID 3 Data Type	R/W
31:30	di3_vc	Data ID 3 Virtual channel	R/W

10.2.9 DATA_IDS_2

- Address Offset:0x01C
- Size:32 bits
- Value after Reset:0
- Access: Read/Write

	DATA_IDS_2																BASE+0x01C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	di7_vc		di7_dt						di6_vc		di6_dt						di5_vc		di5_dt						di4_vc		di4_dt					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
5:0	di4_dt	Data ID 4 Data Type	R/W
7:6	di4_vc	Data ID 4 Virtual channel	R/W
13:8	di5_dt	Data ID 5 Data Type	R/W
15:14	di5_vc	Data ID 5 Virtual channel	R/W
21:16	di6_dt	Data ID 6 Data Type	R/W
23:22	di6_vc	Data ID 6 Virtual channel	R/W
29:24	di7_dt	Data ID 7 Data Type	R/W
31:30	di7_vc	Data ID 7 Virtual channel	R/W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

10.2.10 ERR1

- Name: Error state register 1
- Address Offset:0x020
- Size:29 bits
- Value after Reset:0
- Access: Read

ERR1																														BASE+0x020
Bit				28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				err_ecc_double	vc3_err_crc	vc2_err_crc	vc1_err_crc	vc0_err_crc	err_l_seq_di3	err_l_seq_di2	err_l_seq_di1	err_l_seq_di0	err_l_bndry_match_di3	err_l_bndry_match_di2	err_l_bndry_match_di1	err_l_bndry_match_di0	err_frame_data_vc3	err_frame_data_vc2	err_frame_data_vc1	err_frame_data_vc0	err_f_seq_vc3	err_f_seq_vc2	err_f_seq_vc1	err_f_seq_vc0	err_f_bndry_match_vc3	err_f_bndry_match_vc2	err_f_bndry_match_vc1	err_f_bndry_match_vc0	phy_errsotsynchs_3	phy_errsotsynchs_2	phy_errsotsynchs_1	phy_errsotsynchs_0
RST				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
0	phy_errsotsynchs_0	Start of Transmission Error on data lane 0 (no synchronization achieved)	R
1	phy_errsotsynchs_1	Start of Transmission Error on data lane 1 (no synchronization achieved)	R
2	phy_errsotsynchs_2	Start of Transmission Error on data lane 2 (no synchronization achieved)	R
3	phy_errsotsynchs_3	Start of Transmission Error on data lane 3 (no synchronization achieved)	R
4	err_f_bndry_match_vc0	Error matching Frame Start with Frame End for Virtual Channel 0	R
5	err_f_bndry_match_vc1	Error matching Frame Start with Frame End for Virtual Channel 1	R
6	err_f_bndry_match_vc2	Error matching Frame Start with Frame End for Virtual Channel 2	R
7	err_f_bndry_match_vc3	Error matching Frame Start with Frame End for Virtual Channel 3	R
8	err_f_seq_vc0	Incorrect Frame Sequence detected in Virtual Channel 0	R
9	err_f_seq_vc1	Incorrect Frame Sequence detected in Virtual Channel 1	R
10	err_f_seq_vc2	Incorrect Frame Sequence detected in Virtual Channel 2	R
11	err_f_seq_vc3	Incorrect Frame Sequence detected in Virtual Channel 3	R
12	err_frame_data_vc0	Last received frame, in Virtual Channel 0, had at least one CRC error	R
13	err_frame_data_vc1	Last received frame, in Virtual Channel 1, had at least one CRC error	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

14	err_frame_data_vc2	Last received frame, in Virtual Channel 2, had at least one CRC error	R
15	err_frame_data_vc3	Last received frame, in Virtual Channel 3, had at least one CRC error	R
16	err_l_bndry_match_di0	Error matching Line Start with Line End for vc0 and dt	R
17	err_l_bndry_match_di1	Error matching Line Start with Line End for vc1 and dt	R
18	err_l_bndry_match_di2	Error matching Line Start with Line End for vc2 and dt	R
19	err_l_bndry_match_di3	Error matching Line Start with Line End for vc3 and dt	R
20	err_l_seq_di0	Error in the sequence of lines for vc0 and dt0	R
21	err_l_seq_di1	Error in the sequence of lines for vc0 and dt1	R
22	err_l_seq_di2	Error in the sequence of lines for vc0 and dt2	R
23	err_l_seq_di3	Error in the sequence of lines for vc0 and dt3	R
24	vc0_err_crc	Checksum Error detected on Virtual Channel 0	R
25	vc1_err_crc	Checksum Error detected on Virtual Channel 1	R
26	vc2_err_crc	Checksum Error detected on Virtual Channel 2	R
27	vc3_err_crc	Checksum Error detected on Virtual Channel 3	R
28	err_ecc_double	Header ECC contains 2 errors. Unrecoverable	R

10.2.11 ERR2

- Name: Error state register 2
- Address Offset:0x024
- Size:24 bits
- Value after Reset:0
- Access: Read

	ERR2																											BASE+0x024
Bit									23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									err_l_seq_di7	err_l_seq_di6	err_l_seq_di5	err_l_seq_di4	err_l_bndry_match_di7	err_l_bndry_match_di6	err_l_bndry_match_di5	err_l_bndry_mastch_di4	err_id_vc3	err_id_vc2	err_id_vc1	err_id_vc0	Vc3_err_ecc_corrected	Vc2_err_ecc_corrected	Vc1_err_ecc_corrected	vc0_err_ecc_corrected	phy_errsoths_3	phy_errsoths_2	phy_errsoths_1	phy_errsoths_0	phy_ erresc 3	phy_ erresc _2	phy_ erresc _1	phy_erresc_0
RST									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
0	phy_erresc_0	Escape Entry Error (ULPM) on data lane 0	R
1	phy_ erresc _1	Escape Entry Error (ULPM) on data lane 1	R
2	phy_ erresc _2	Escape Entry Error (ULPM) on data lane 2	R
3	phy_ erresc _3	Escape Entry Error (ULPM) on data lane 3	R
4	phy_errsoths_0	Start of Transmission Error on data lane 0(synchronization can still be achieved)	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

5	phy_errsoths_1	Start of Transmission Error on data lane 1(synchronization can still be achieved)	R
6	phy_errsoths_2	Start of Transmission Error on data lane 2(synchronization can still be achieved)	R
7	phy_errsoths_3	Start of Transmission Error on data lane 3(synchronization can still be achieved)	R
8	vc0_err_ecc_corrected	Header error detected and corrected on Virtual Channel 0	R
9	vc1_err_ecc_corrected	Header error detected and corrected on Virtual Channel 1	R
10	vc2_err_ecc_corrected	Header error detected and corrected on Virtual Channel 2	R
11	vc3_err_ecc_corrected	Header error detected and corrected on Virtual Channel 3	R
12	err_id_vc0	Unrecognized or unimplemented data type detected in Virtual Channel 0	R
13	err_id_vc1	Unrecognized or unimplemented data type detected in Virtual Channel 1	R
14	err_id_vc2	Unrecognized or unimplemented data type detected in Virtual Channel 2	R
15	err_id_vc3	Unrecognized or unimplemented data type detected in Virtual Channel 3	R
16	err_l_bndry_match_di4	Error matching Line Start with Line End for vc4 and dt4	R
17	err_l_bndry_match_di5	Error matching Line Start with Line End for vc5 and dt5	R
18	err_l_bndry_match_di6	Error matching Line Start with Line End for vc6 and dt6	R
19	err_l_bndry_match_di7	Error matching Line Start with Line End for vc7 and dt7	R
20	err_l_seq_di4	Error in the sequence of lines for vc0 and dt4	R
21	err_l_seq_di5	Error in the sequence of lines for vc0 and dt5	R
22	err_l_seq_di6	Error in the sequence of lines for vc0 and dt6	R
23	err_l_seq_di7	Error in the sequence of lines for vc0 and dt7	R

10.2.12 MASK1

- Name: Masks for errors 1
- Address Offset:0x028
- Size:29 bits
- Value after Reset:0
- Access: Read/Write

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	MASK1																BASE+0x028													
Bit				28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				mask_err_ecc_double	mask_vc3_err_crc	mask_vc2_err_crc	mask_vc1_err_crc	mask_vc0_err_crc	mask_err_l_seq_di3	mask_err_l_seq_di2	mask_err_l_seq_di1	mask_err_l_seq_di0	mask_err_l_bndry_match_di3	mask_err_l_bndry_match_di2	mask_err_l_bndry_match_di1	mask_err_l_bndry_match_di0	mask_err_frame_data_vc3	mask_err_frame_data_vc2	mask_err_frame_data_vc1	mask_err_frame_data_vc0	mask_err_f_seq_vc3	mask_err_f_seq_vc2	mask_err_f_seq_vc1	mask_err_f_seq_vc0	mask_err_f_bndry_match_vc3	mask_err_f_bndry_match_vc2	mask_err_f_bndry_match_vc1	mask_err_f_bndry_match_vc0	mask_phy_errsotsynchs_3	mask_phy_errsotsynchs_2	mask_phy_errsotsynchs_1	mask_phy_errsotsynchs_0
RST				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
0	mask_phy_errsotsynchs_0	Mask for phy_errsotsynchs_0	R/W
1	mask_phy_errsotsynchs_1	Mask for phy_errsotsynchs_1	R/W
2	mask_phy_errsotsynchs_2	Mask for phy_errsotsynchs_2	R/W
3	mask_phy_errsotsynchs_3	Mask for phy_errsotsynchs_3	R/W
4	mask_err_f_bndry_match_vc0	Mask for err_f_bndry_match_vc0	R/W
5	mask_err_f_bndry_match_vc1	Mask for err_f_bndry_match_vc1	R/W
6	mask_err_f_bndry_match_vc2	Mask for err_f_bndry_match_vc2	R/W
7	mask_err_f_bndry_match_vc3	Mask for err_f_bndry_match_vc3	R/W
8	mask_err_f_seq_vc0	Mask for err_f_seq_vc0	R/W
9	mask_err_f_seq_vc1	Mask for err_f_seq_vc1	R/W
10	mask_err_f_seq_vc2	Mask for err_f_seq_vc2	R/W
11	mask_err_f_seq_vc3	Mask for err_f_seq_vc3	R/W
12	mask_err_frame_data_vc0	Mask for err_frame_data_vc0	R/W
13	mask_err_frame_data_vc1	Mask for err_frame_data_vc1	R/W
14	mask_err_frame_data_vc2	Mask for err_frame_data_vc2	R/W
15	mask_err_frame_data_vc3	Mask for err_frame_data_vc3	R/W
16	mask_err_l_bndry_match_di0	Mask for err_l_bndry_match_di0	R/W
17	mask_err_l_bndry_match_di1	Mask for err_l_bndry_match_di1	R/W
18	mask_err_l_bndry_match_di2	Mask for err_l_bndry_match_di2	R/W
19	mask_err_l_bndry_match_di3	Mask for err_l_bndry_match_di3	R/W
20	mask_err_l_seq_di0	Mask for err_l_seq_di0	R/W
21	mask_err_l_seq_di1	Mask for err_l_seq_di1	R/W
22	mask_err_l_seq_di2	Mask for err_l_seq_di2	R/W
23	mask_err_l_seq_di3	Mask for err_l_seq_di3	R/W
24	mask_vc0_err_crc	Mask for vc0_err_crc	R/W
25	mask_vc1_err_crc	Mask for vc1_err_crc	R/W
26	mask_vc2_err_crc	Mask for vc2_err_crc	R/W
27	mask_vc3_err_crc	Mask for vc3_err_crc	R/W
28	mask_err_ecc_double	Mask for err_ecc_double	R/W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

10.2.13 MASK2

- Name: Masks for errors 2
- Address Offset:0x02C
- Size:24 bits
- Value after Reset:0
- Access: Read/Write

	MASK2																BASE+0x02C														
Bit									23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									mask_err_l_seq_di7	mask_err_l_seq_di6	mask_err_l_seq_di5	mask_err_l_seq_di4	mask_err_l_bndry_match_di7	mask_err_l_bndry_match_di6	mask_err_l_bndry_match_di5	mask_err_l_bndry_mastch_di4	mask_err_id_vc3	mask_err_id_vc2	mask_err_id_vc1	mask_err_id_vc0	mask_vc3_err_ecc_corrected	mask_vc2_err_ecc_corrected	mask_vc1_err_ecc_corrected	mask_vc0_err_ecc_corrected	mask_phy_errsoths_3	mask_phy_errsoths_2	mask_phy_errsoths_1	mask_phy_errsoths_0	mask_phy_ erresc 3	mask_phy_ erresc _2	mask_phy_ erresc _1	mask_phy_erresc_0
RST									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
0	mask_phy_erresc_0	Mask for phy_erresc_0	R/W
1	mask_phy_ erresc _1	Mask for phy_erresc_1	R/W
2	mask_phy_ erresc _2	Mask for phy_erresc_2	R/W
3	mask_phy_ erresc _3	Mask for phy_erresc_3	R/W
4	mask_phy_errsoths_0	Mask for phy_errsoths_0	R/W
5	mask_phy_errsoths_1	Mask for phy_errsoths_1	R/W
6	mask_phy_errsoths_2	Mask for phy_errsoths_2	R/W
7	mask_phy_errsoths_3	Mask for phy_errsoths_3	R/W
8	mask_vc0_err_ecc_corrected	Mask for vc0_err_ecc_corrected	R/W
9	mask_vc1_err_ecc_corrected	Mask for vc1_err_ecc_corrected	R/W
10	mask_vc2_err_ecc_corrected	Mask for vc2_err_ecc_corrected	R/W
11	mask_vc3_err_ecc_corrected	Mask for vc3_err_ecc_corrected	R/W
12	mask_err_id_vc0	Mask for err_id_vc0	R/W
13	mask_err_id_vc1	Mask for err_id_vc1	R/W
14	mask_err_id_vc2	Mask for err_id_vc2	R/W
15	mask_err_id_vc3	Mask for err_id_vc3	R/W
16	mask_err_l_bndry_match_di4	Mask for err_l_bndry_match_di4	R/W
17	mask_err_l_bndry_match_di5	Mask for err_l_bndry_match_di5	R/W
18	mask_err_l_bndry_match_di6	Mask for err_l_bndry_match_di6	R/W
19	mask_err_l_bndry_match_di7	Mask for err_l_bndry_match_di7	R/W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

20	mask_err_l_seq_di4	Mask for err_l_seq_di4	R/W
21	mask_err_l_seq_di5	Mask for err_l_seq_di5	R/W
22	mask_err_l_seq_di6	Mask for err_l_seq_di6	R/W
23	mask_err_l_seq_di7	Mask for err_l_seq_di7	R/W

10.2.14 PHY_TST_CRTL0

- Name: D-PHY Test interface control 0
- Address Offset:0x030
- Size:2 bits
- Value after Reset:0
- Access: Read/Write

	PHY_TST_CRTL0																														BASE+0x030	
Bit																															1	0
																															phy_testclk	phy_testclr
RST																															0	0

Bits	Name	Description	R/W
0	phy_testclr	PHY test interface clear. Used when active performs vendor specific interface initialization (Active High).	R/W
1	phy_testclk	PHY test interface strobe signal. Used to clock TESTDIN bus into the DPHY. In conjunction with TESTEN signal controls the operation selection.	R/W

10.2.15 PHY_TST_CRTL1

- Name: D-PHY Test interface control 1
- Address Offset:0x034
- Size:17 bits
- Value after Reset:0
- Access: Read/Write

	PHY_TST_CRTL1																															BASE+0x034	
Bit																	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	phy_testen	phy_testdout								phy_testdin							
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
0:7	phy_testdin	PHY test interface input 8-bit data bus for internal register programming and test functionalities access	R/W
8:15	phy_testdout	PHY output 8-bit data bus for read-back and internal probing functionalities.	R
16	phy_testen	PHY test interface operation selector: • 1: Configures address write operation on the falling edge of TESTCLK • 0: Configures a data write operation on the rising edge of TESTCLK	R/W

10.3 Operation

The following sections describe the MIPI_CSI operations of configuration.

The Initialization steps are as follows:

1. De-assert CSI-2 presetn signal (global reset).
2. Set number of Lanes(register N_LANES).
3. De-assert PHY shutdown (register PHY_SHUTDOWNZ)
4. De-assert PHY reset (register PHY_RSTZ)
5. De-assert CSI reset (register CSI2-RESETN)
6. Wait for 200us, read the PHY status register (PHY_STATE) to confirm that all data and clock lanes of the D-PHY are in Stop State.
7. Configure the camera sensor to start transmitting a clock on the D-PHY clock lane.
8. Read the PHY status register(PHY_STATE) to confirm that the D-PHY is receiving a clock on the D-PHY clock lane.
9. Meting the steps above, configure the camera sensor to start transmitting packages.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

11 Camera Interface Module(CIM)

11.1 Overview

The camera interface module (CIM) supports commonly available CMOS/CCD type image sensors. The CIM sources the digital image stream through 8bit DVP or MIPI interface. The CIM can directly connect to external CMOS/CCD image sensors and ITU656 standard video decoders. It is a member of Display System.

11.2 Features

- ✓ Support ITU656, YCbCr 4:2:2, RGB888, RGB565, MONO(8) input
- ✓ Support YUV422, RGB888, RGB565, MONO output
- ✓ Support DVP interface and CSI(max 2 lane)
- ✓ Support max to 2047x2047 input and output
- ✓ Crop
- ✓ Support exposure control
- ✓ auto recovery
- ✓ Support histogram (applies to YUV & MONO formats)

11.3 Function Description

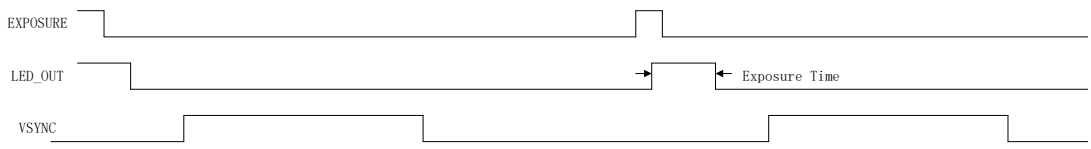
11.3.1 Mode

11.3.1.1 Normal

Camera continuous send frames, the CIM receive selective.

11.3.1.2 Snapshot

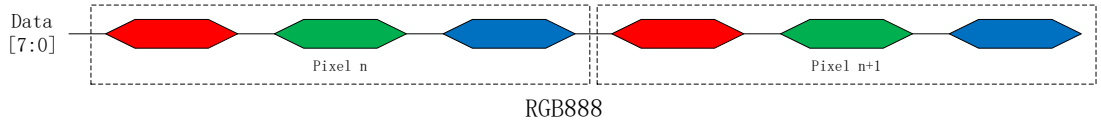
The CIM send an exposure pulse to camera, then receive one frame from camera.



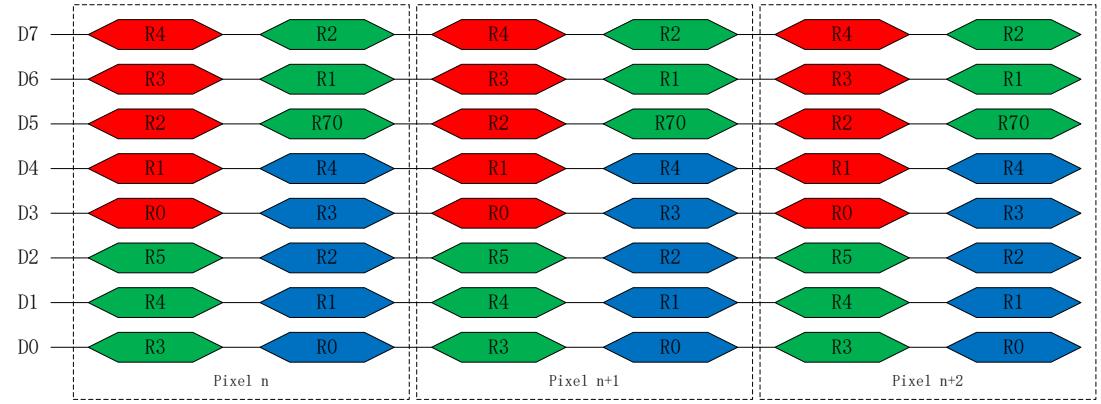
Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.4 Data Format Description

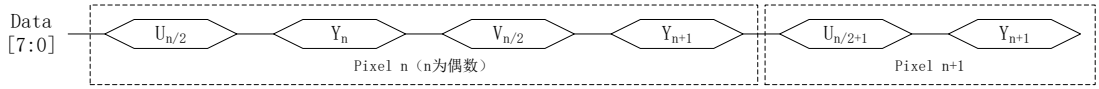
11.4.1 Input Data(DVP Interface)



RGB888



RGB565



UYVY

11.4.2 Output Data(memory)

RGB888

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								R	R	R	R	R	R	R	R	G	G	G	G	G	G	G	G	B	B	B	B	B	B	B	B

RGB565

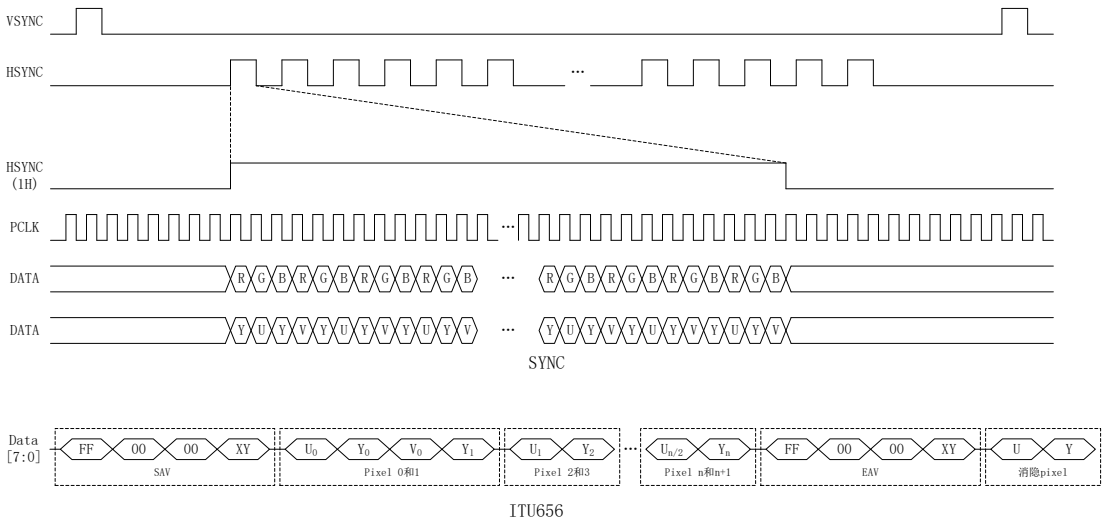
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	G	G	G	G	G	G	G	G	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B

YUV422package

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
V								Y_1								U								Y_0							

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.4.3 Timing



ITU656

11.4.4 Others

Start-stop code of ITU656 is composed of FF+00+00+XY. Constitute of XY is as below:

[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	F	V	H	Reserved	Reserved	Reserved	Reserved

F field flag（0：top field，1：bottom field）

V vertical sync（0：active，1：invalid）

H horizontal sync（0：SAV-start of active video，1：EAV-end of active video）

P3-P0 check flag，algorithm is as below

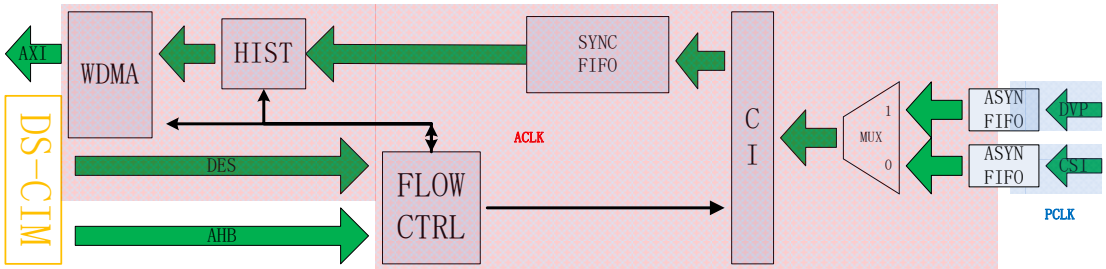
F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.5 Pins Description

Name	Width	I/O	Description
Data	[7:0]	I	DVP interface
hsync	[0:0]	I	
vsync	[0:0]	I	
pixclk	[0:0]	I	pixel clock
exposure	[0:0]	O	Control when to expose

11.6 Architecture map



11.7 Descriptors define

DES_NEXT_ADDR 1st

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NEXT_ DES_ADDR																															

Bits	Name	Description	RW
31:0	NEXT_ DES_ADDR	The next descriptor's address. **NOTE:** Write **DS_CIM_DES_ADDR** will cover the value.	RW

FRM_WRBK_ADDR 2nd

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRM_WRBK_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	FRM_WRBK_ADDR	Frame WriteBack Buffer head address(aligned to pixel size) When scan mode is 'interlace', these bits are first field buffer's address.	RW

WRBK_STRD 3rd

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					FRM_WRBK_STRD										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
30:11	Reserved	Writing has no effect, read as zero.	R
10:0	FRM_WRBK_STRD	Frame WriteBack stride.(max 2047)(Unit: pixel) Note: For YUV422 format, please set an even.	RW

DES_INTC 4th

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													SOF_MSK	EOF_MSK	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
2	SOF_MSK	Mask of SOF. 0: interrupt is masked 1: generate interrupt Work together with DS_CIM_INTC, only when both are 1 will generate interrupt.	RW
1	EOF_MSK	Mask of EOF 0: interrupt is masked 1: generate interrupt Work together with DS_CIM_INTC, only when both are 1 will generate interrupt.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

DES_CFG 5th

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRM_ID						Reserved							FRM_WRBK_FMT			Reserved															DES_END
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	FRM_ID	Frame ID	RW
18:16	FRM_WRBK_FMT	Frame WriteBack format. 000：reserved(default) 001：RGB565 010：Reserved 011：YUV422(vy_1uy_0 occupy 32bits, v is at [31:24],y_0 is at [7:0]) 100：MONO(8) 101：reserved 110：RGB888	RW
0	DES_END	1: this descriptor is the last one of the chain; 0: not the last one	RW

HIST_CFG 6th

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HIST_EN	Reserved															GAIN_ADD								GAIN_MUL							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	HIST_EN	1: enable 0: disable Note: Histogram size is fixed 256 words. applies to yuv & MONO formats.	RW
30:16	Reserved	Writing has no effect, read as zero.	R
15:8	GAIN_ADD	Gain addition coeficient	RW
7:0	GAIN_MUL	Gain multiplication coeficient **Note**: GAIN_MUL=real_mul << 5 ,for float-point	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		DATAOUT = real_mul * DATAIN + GAIN_ADD GAIN woks only when HIST is valid.	

HIST_WRBK_ADDR 7th

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HIST_WRBK_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	HIST_WRBK_ADDR	Hist WriteBack Buffer address(aligned to word)	RW

SF_WRBK_ADDR 8th

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SF_WRBK_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	SF_WRBK_ADDR	Second field Write Back Buffer head address. When scan mode is 'progressive', these bits can be any value.	RW

11.8 Registers Description

11.8.1 Instructions

Following chapter will descript the functions of all software accessible registers.

Conventions:

9. Register Address = Base + Address offset
10. The registers can be read and written by AHB bus
11. Register read/write attribute
    - ✧ R - Read only
    - ✧ W - Write only
    - ✧ RW - read and write
    - ✧ RCW - read and write, but clear to 0 by read
    - ✧ RSW - read and write, but set to 1 by read
    - ✧ RWC - read and write, clear to 0 by write 1, write 0 has no effect

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

- ✧ RWS - read and write, set to 1 by write 1, write 0 has no effect
- ✧ RC - read only, and clear to 0 by read
- ✧ RS - read only, and set to 1 by read
- ✧ SPEC - special access method, relate to its description

12. Reset Value
    - 1 - reset to 1
    - 0 - reset to 0
    - ? - value unknown after reset

11.8.2 Map

The DC's registers map base address is 0x13060000

The DC is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 11-1 DC Registers Map

Name	Reset Value	Address Offset	Description	RW	Mask
GLB_CFG	0x0000_0001	0x0000	Global configure	RW	0x00F7_E73F
CROP_SIZE	0x0000_0000	0x0004	Org frame size	RW	0x07FF_07FF
CROP_SITE	0x0000_0000	0x0008	Crop start site	RW	0x07FF_07FF
SCAN_CFG	0x0000_0000	0x0018	Second field configure	RW	0xC000_07FF
DLY_CFG	0x0000_0000	0x001C	Delay configure	RW	0xC0FF_FFFF
QOS_CTRL	0x0000_0000	0x0020	QoS control	RW	0x0000_0007
QOS_CFG	0x0319_0842	0x0024	Priority level configure	RW	0x07FF_FFFF
DES_ADDR	0x0000_0000	0x1000	Descriptor's head address	RW	0xFFFF_FFFF
CTRL	0x0000_0000	0x2000	control	W	0x0000_001F
ST	0x0000_0000	0x2004	status	R	0x0000_007F
CLR_ST	0x0000_0000	0x2008	clear status and interrupt flag	W	0x0000_007E
CIM_INTC	0x0000_0000	0x200C	interrupt mask	RW	0x0000_007E
INT_FLAG	0x0000_0000	0x2010	interrupt flag	R	0x0000_007E
FRM_ID	0x0000_0000	0x2014	Frame ID	R	0x0000_003F
ACT_SIZE	0x0000_0000	0x2018	Actual size of image	R	0x07FF_07FF
DBG_DES	0x0000_0000	0x3000	descriptor's debug reading	R	0xFFFF_FFFF
DBG_DMA	0x0000_0000	0x3004	WDMA's debug reading	R	0xFFFF_FFFF
DBG_CGC	0x0000_003F	0x3008	Clock gating control	RW	0x0000_003F

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.8.3 Registers

11.8.3.1 GLOBAL register

	GLB_CFG																BASE+0x0000													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								C_ORDER				Reserved	ORG_FMT			DE_PCLK	DL_VSYNC	DL_HSYNC	Reserved		EXPO_WIDTH			Reserved		SIZE_CHK	IF_SEL	MODE	BURST_LEN		[illegible]
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:20	C_ORDER	Source data's color order 0000：RGB(default) 0001：RBG 0010：GRB 0011：GBR 0100：BRG 0101：BGR 1000：Y_0UY_1V 1001：Y_0VY_1U 1010：UY_0VY_1 1011：VY_0UY_1 Note: when DVP interface, indicate the send order; when IDI interface, indicate the position in the 32bits width bus. For example, when DVP, Y_0UY_1V means the Y_0 send first; when IDI, Y_0UY_1V means the Y_0 at high bits.	RW
19	Reserved	Writing has no effect, read as zero.	R
18:16	ORG_FMT	The source frame's format. 000：RGB565(default) 001：RGB888 010：YUV422 011：ITU656 100：MONO(Y8)	RW
15	DE_PCLK	default edge of PCLK 0: sample at pos-edge(default) 1: sample at neg-edge	RW
14	DL_VSYNC	default level of VSYNC 0: default level is low, active level is high(default)	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: default level is high, active level is low	
13	DL_HSYNC	default level of HSYNC 0: default level is low, active level is high(default) 1: default level is high, active level is low	RW
12:11	Reserved	Writing has no effect, read as zero.	R
10:8	EXPO_WIDTH	Pulse width.(Num+1 pclk cycles)	RW
7: 6	Reserved	Writing has no effect, read as zero.	R
5	SIZE_CHK	Whether the actual size of image is less than the expect size. 0: disable(default) 1: enable	RW
4	DAT_IF_SEL	Data Interface select. 0: DVP(default) 1: IDI for CSI	RW
3	MODE	Camera operation mode. 0: normal(default) 1: snapshot	RW
2:1	BURST_LEN	The max length of the write back DMA's burst. 00: 4(default) 01: 8 10: 16 11: 32	RW
0	AUTO_RECOVERY	0: stop immediately; 1: If over-run, or size check error when function enabled, the CIM will drop the current image, then receive the next image to fill the current buffer.(default)	RW

11.8.3.2 Crop size register

	DS_CIM_CROP_SIZE																BASE+0x0004													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					crop_Height											Reserved					crop_Width										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
30:27	Reserved	Writing has no effect, read as zero.	R
26:16	crop_Height	frame height after cropping **NOTE:** Configured as the full image's height when no need	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		crop; When interlace mode, it is the first field's height.	
15:11	Reserved	Writing has no effect, read as zero.	R
10:0	crop_Width	frame width after cropping **NOTE:** Configured as the full image's width when no need crop;	RW

11.8.3.3 Crop site register

	DS_CIM_CROP_SITE																BASE+0x0008															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					crop_y											Reserved					crop_x											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
30:27	Reserved	Writing has no effect, read as zero.	R
26:16	crop_y	The start site of the cropped image(start from 0)	RW
15:11	Reserved	Writing has no effect, read as zero.	R
10:0	crop_x	The start site of the cropped image(start from 0)	RW

11.8.3.4 Scan configure register

	DS_CIM_SCAN_CFG																BASE+0x0018															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCAN_MD	F_ORDER	Reserved																			SF_Height										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	SCAN_MD	0：progressive(default) 1：interlace **NOTE:** It is used only when ITU656, in other mode, this bit is use-less; when interlace mode, resize and crop function are not supported.	R
30	F_ORDER	Field order. 0: top field first, then bottom field(default)	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: bottom field first, then top field	
30:12	Reserved	Writing has no effect, read as zero.	R
11:0	SF_Height	Second field height, used when interlace scan mode.	RW

11.8.3.5 Delay counter register

	DS_CIM_DLY_CFG																															
	BASE+0x001C																															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DLY_EN	DLY_MD	Reserved						DLY_NUM																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	DLY_EN	0: When continuous descriptor chain, start the next frame operation immediately after the current frame operation done; 1: When continuous descriptor chain, delay DLY_NUM after the current frame operation done, then start the next frame operation.	RW
30	DLY_MD	0: only ensure that delay conditions are met within one consecutive frame burst; 1: not only guarantee the delay condition in the frame burst, but also ensure the delay condition between two burst.	RW
29:24	Reserved	Writing has no effect, read as zero.	R
23:0	DLY_NUM	Interval between two frame operating. When normal mode, unit is one frame time; When snapshot mode, unit is 256 PCLK cycles.	RW

11.8.3.6 QOS CTRL register

	DS_CIM_QOS_CTRL																															
	BASE+0x0020																															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													QOS_VAL	QOS_CTRL	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

2:1	QOS_VAL	QoS value set by software.	RW
0	QOS_CTRL	0: The QoS value is controlled by PCFG register; 1: The QoS value is set by QOS_VAL bits	RW

11.8.3.7 QOS configure register

	DS_CIM_QOS_CFG																BASE+0x0024															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					TH2									TH1									TH0								
RST	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26:18	TH2	Threshold2: (TH1+1)~263	RW
17:9	TH1	Threshold1: (TH0+1)~262	RW
8:0	TH0	Threshold0: 0~261	RW

PCFG is used to control the write back rate.

The 3 thresholds cut the output FIFO into 4 spaces. When the entries remained triggering one of them, the priority level will be altered by hardware:

QoS	Space
00	Empty ~ TH0
01	TH0 ~ TH1
10	TH1 ~ TH2
11	TH2 ~ Full

11.8.3.8 Descriptor address register

	DS_CIM_DES_ADDR																BASE+0x1000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DES_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	DES_ADDR	This is the address of the 1st descriptor before working; After start working, it is the address of the next descriptor. It can be changed by software for descriptor inserting operation. Note: the address must aligned to 64bits	RW

11.8.3.9 Control register

	DS_CIM_CTRL																BASE+0x2000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DBG_DES_RST	SOFT_RST	GEN_STOP	QCK_STOP	START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect, read as zero.	R
4	DBG_DES_RST	reset the reading point of DEBUG_DES register.	W
3	SOFT_RST	Soft reset	W
2	GEN_STOP	General stop. Assure integrity of the current frame	W
1	QCK_STOP	Quick stop. Stop as quickly as possible, the integrity of the current frame not be guaranteed.	W
0	START	module start	W

11.8.3.10 Status register

	DS_CIM_ST																BASE+0x2004															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								SRA	SZ_ERR	EOW	OVER	GSA	SOF	EOF	WORKING
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
30:8	Reserved	Writing has no effect, read as zero.	R
7	SRA	Soft reset acknowledge	R
6	SZ_ERR	Size check error	R
5	EOW	End of normal work	R
4	OVER	over-run	R
3	GSA	General stop acknowledge	R
2	SOF	Start of frame	R
1	EOF	End of frame	R
0	WORKING	Module is working	R

11.8.3.11 Clear status register

	DC_CLR_ST																BASE+0x2008													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								CLR_SRA	CLR_SZ_ERR	CLR_EOW	CLR_OVER	CLR_GSA	CLR_SOF	CLR_EOF	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
30:8	Reserved	Writing has no effect, read as zero.	R
7	CLR_SRA	clear SRA	W
6	CLR_SZ_ERR	clear SZ_ERR	W
5	CLR_EOW	clear EOW	W
4	CLR_OVER	clear OVER	W
3	CLR_GSA	clear GSA	W
2	CLR_FRM_START	clear SOF	W
1	CLR_FRM_END	clear EOF	W
0	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.8.3.12 CIM INTC register

	DS_CIM_INTC																BASE+0x200c													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									MSK_SZ_ERR	MSK_EOW	MSK_OVER	MSK_GSA	MSK_SOF	MSK_EOF	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
30:7	Reserved	Writing has no effect, read as zero.	R
6	MSK _SZ_ERR	Mask of SZ_ERR 0: interrupt is masked 1: generate interrupt	RW
5	MSK _EOW	Mask of EOW 0: interrupt is masked 1: generate interrupt	RW
4	MSK _OVER	Mask of OVER 0: interrupt is masked 1: generate interrupt	RW
3	MSK _GSA	Mask of GSA 0: interrupt is masked 1: generate interrupt	RW
2	MSK _SOF	Mask of SOF 0: interrupt is masked 1: generate interrupt Work together with DES_INTC, only when both are 1 will generate interrupt.	RW
1	MSK _EOF	Mask of EOF 0: interrupt is masked 1: generate interrupt Work together with DES_INTC, only when both are 1 will generate interrupt.	RW
0	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.8.3.13 INT flag register

	DS_CIM_INT_FLAG																BASE+0x2010														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									INT_SZ_ERR	INT_EOW	INT_OVER	INT_GSA	INT_SOF	INT_EOF	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
30:7	Reserved	Writing has no effect, read as zero.	R
6	INT_SZ_ERR	interrupt of SZ_ERR	R
5	INT_EOW	interrupt of EOW	R
4	INT_OVER	interrupt of OVER	R
3	INT_GSA	interrupt of GSA	R
2	INT_SOF	interrupt of SOF	R
1	INT_EOF	interrupt of EOF	R
0	Reserved	Writing has no effect, read as zero.	R

11.8.3.14 Frame ID register

	DS_CIM_FRM_ID																BASE+0x2014														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										FRM_ID					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
30:6	Reserved	Writing has no effect, read as zero.	R
5:0	FRM_ID	Indicate which frame the EOF belongs to.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

11.8.3.15 Actual image size register

	DS_CIM_ACT_SIZE																BASE+0x2018															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					Act_height											Reserved					Act_width											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
30:27	Reserved	Writing has no effect, read as zero.	R
26:16	Act_height	The actual height of the image	R
15:11	Reserved	Writing has no effect, read as zero.	R
10:0	Act_width	The actual width of the image	R

11.8.3.16 Descriptor content register(for debug)

	DS_CIM_DBG_DES																BASE+0x3000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBG_DES																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DBG_DES	the content of descriptors	R

11.8.3.17 DMA current address register(for debug)

	DS_CIM_DBG_DMA																BASE+0x3004															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBG_DMA_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	DBG_DMA_ADDR	WDMA's current operating address	R

11.8.3.18 Clock gating control register(for debug)

	DS_CIM_DBG_CGC																BASE+0x3008													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										CGC_REG	CGC_WRBK	CGC_DES	CGC_SCALE	CGC_DVP	CGC_FLOW
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
5	CGC_REG	0: disable clock gating for com_reg module; 1: enable clock gating for com_reg module.	RW
4	CGC_WRBK	0: disable clock gating for wrbk module; 1: enable clock gating for wrbk module.	RW
3	CGC_DES	0: disable clock gating for des module; 1: enable clock gating for des module.	RW
2	CGC_SCALE	0: disable clock gating for scale module; 1: enable clock gating for scale module.	RW
1	CGC_DVP	0: disable clock gating for dvp module; 1: enable clock gating for dvp module.	RW
0	CGC_FLOW	0: disable clock gating for flow_ctrl module; 1: enable clock gating for flow_ctrl module.	RW

11.9 Operation guide

11.9.1 Configure flow

11.9.1.1 Common flow

configure **DS_CIM_GLB_CFG**, **DS_CIM_FRM_SIZE**, **DS_CIM_CROP_SITE**.
configure **DS_CIM_SF_CFG** when ITU656 mode(this register could not be configured at other mode)
configure **DS_CIM_DLY_CFG**(when DLY_EN is 0, DLY_NUM could not be configured)
configure **DS_CIM_INTC**

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

configure **DS_CIM_DES_ADDR**
write START at **DS_CIM_CTRL**
wait **EOF**

11.9.1.2 Single frame flow

If the DES_END is 1, the hardware will stop working after Common flow, and then if write START directly, the hardware will use the NEXT_DES_ADDR, read by last descriptor, as the **DS_CIM_DES_ADDR** to execute the next frame flow(read the descriptor and receive one frame, similarly hereinafter); or can the software configure a new **DS_CIM_DES_ADDR**.

11.9.1.3 Continuous frame flow

If the DES_END is 0, the hardware will start counting the DLY_NUM(if DLY_EN is 1) after Common flow, and then execute the next frame flow.

11.9.2 Interlace scan mode

Only used when ITU656 protocol.
Two descriptor are needed, corresponding top and bottom field respectively. They have different WRBK_ADDR and appropriate WRBK_STRD, but the DES_INTC and WRBK_FMT must be the same.
DES_END at the first descriptor must be 0.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12 Audio Interface Controller

12.1 Overview

12.1.1 Features

- DMA Features
  - AHB master
  - Support up to 10 independent DMA channels
  - Support Descriptor or No-Descriptor Transfer mode
  - Transfer data units: 1-word, 2- word, 4- word, 8- word, 16- word, 32- word
  - Transfer number of data unit: 1 ~ 2^{24} - 1
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Support Address Increment

- Format Converter Features
  - Support up to 10 independent DMA channels
  - Data right justified
  - Support audio sample data size: 8/12/13/16/18/20/24/32 bit
  - 18/20/24 bit audio sample data size Support compression and no- compression mode

- Internal Control Bus Feature
  - AHB slave
  - Support CPU read/write mode

- Internal Data Bus Feature
  - 32 timeslot
  - 15 receive FIFO and 12 transmit FIFO
  - Support one by one and one by multiple mode

- BAIC Feature
  - Serial audio data MSB transfer at the rising of frame synchronization SYNC or the next BCLK edge after
  - Support eleven audio data formats

  PCM Formats：

  — PCM mode A

  — PCM mode B

  — DSP mode A

  — DSP mode B

  I2S Formats：

  — I2S mode

  — I2S LEFT Justified

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

— I2S RIGHT Justified
— TDM1 mode
— TDM1 LEFT Justified mode
— TDM2 mode
— TDM2 LEFT Justified mode

- BASIC interface transfer audio data always MSB first
- Support master or slave mode
- Support sample valid data bit width：

— I2S formats support 8/12/13/16/18/20/24/32 bit sample width
— PCM format support 8/16/32 bit sample width

- Support different sample rate：

—I2S format support 8kHz，11.025kHz，16kHz，22.05kHz，32kHz，44.1kHz，48kHz，88.2kHz，96kHz，176.4kHz，192kHz，352.8kHz and 384kHz sample rate
—PCM format support 8kHz, 16kHz 和 32kHz sample rate

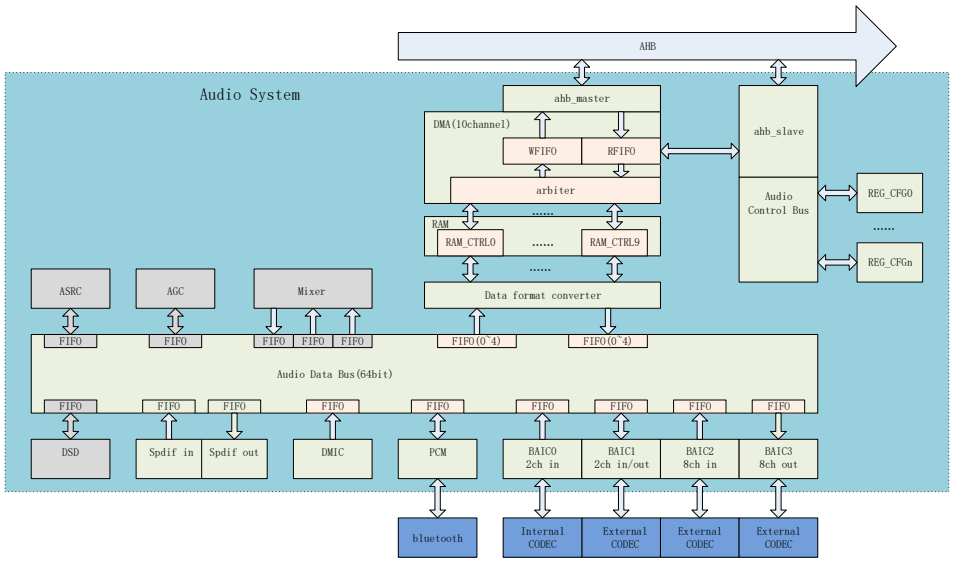
- One sample have 32/64/128/256/512 BCLK period and can configure
- I2S format valid clock edge：Data is sampled on the rising edge of the BCLK and data is send out on the falling edge of the BCLK
- PCM format valid clock edge: mode 1，Data is sampled on the rising edge of the BCLK and data is send out on the falling edge of the BCLK； mode 2, Data is sampled on the falling edge of the BCLK and data is send out on the rising edge of the BCLK
- PCM format frame synchronization SYNC signal high level continued time can configure but it should less than N BCLK period(one sample period contain N BCLK periods)
- PCM formats support mono, stereo and multi channel mode, I2S format support stereo mode
- I2S formats stereo mode support LR or RL transmission mode
- BAIC interface support between signed ←→unsigned data transfer format

➢ DMIC Feature

- Low power DMIC Controller
- 16 bits data interface and 20bit precision internal controller
- SNR: 90dB, THD: -90dB @ FS -20dB
- Linear high pass filter include. Attenuation: -2.9dB@100Hz, -22dB@27Hz. -36dB@10Hz
- Low power voice trigger when waiting to start talking
- 1/2/3/4 channel digital MIC support
- Support voice data pre-fetch when trigger enable and the data interface disable, but do not increase the power dissipation
- Sample frequency supported: 8k, 16k
- Support low power mode, user for decrease DMIC sensor and DMIC Controller power dissipation

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.1.2 Architecture Map



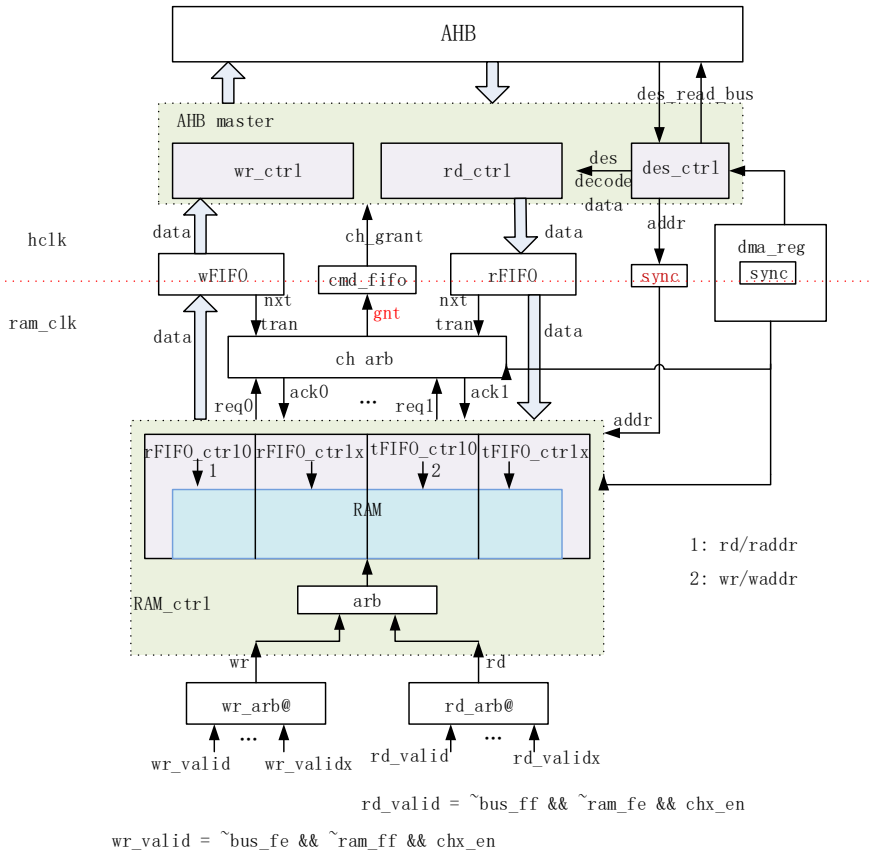
NOTE: current version is not include ASRC/AGC/DSD

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2 SubModule

12.2.1 DMA

12.2.1.1 Block Diagram



12.2.1.2 Descriptor Structure:

Word	Bit	Name	Function
1st (DES0)	31-11	Reserved	--
	10-9	Reserved	--
	8	BAI	Target Address Increment
	7	Reserved	
	6-4	TSZ	Transfer Data Size
	3	LTE	Last Descriptor Transfer end Status
	2	LINK	Descriptor Link Enable
	1-0	Reserved	
2nd (DES1)	31-0	DBA	Bus Address
3rd (DES2)	31-0	DOA	Descriptor Next Offset address
4th (DES3)	31-24	Reserved	
	23-0	DTC	Transfer Counter

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.1.3 DMA Register Descriptions

Name	Base	Description
A_DMA	134d0000	Base address of Audio DMA.

12.2.1.3.1 DMA Bus Address (DBAn, n = 0 ~ 9)

	DBAn																BASE + 0x0 + (n*0x18)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BA																															
RST	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	BA	Bus physical address.	RW

12.2.1.3.2 DMA Transfer Count (DTCn, n = 0 ~ 9)

	DTCn																BASE + 0x4 + (n*0x18)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								TC																							
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:24	Reserved	Write has no effect, read as zero.	R
23:0	TC	TC records the number of data unit to be transferred. TC automatically counts down to 0 at the end.	RW

12.2.1.3.3 DMA Channel Control Register (DCRn, n = 0 ~ 9)

	DCRn																BASE + 0x8 + (n*0x18)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														DFS	CTE
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:2	Reserved	Write has no effect, read as zero.	R
1	DFS	DMA Force Stop. Writing 0 to this bit has no effect and this bit is always reading 0.	W
0	CTE	Channel transfer enable: 0: disable; 1: enable.	RW

12.2.1.3.4 DMA Channel Status Register (DSRn, n = 0 ~ 9)

	DSRn																BASE + 0x0C + (n*0x18)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CDOA								Reserved		TT_INT	LTT_INT	TT	LTT	Reserved	LINK
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Write has no effect, read as zero.	R
15:8	CDOA	Copy of offset address of last completed descriptor from that in DMA command register. (The field is Ignored in No-Descriptor Transfer)	R
7:6	Reserved	Write has no effect, read as zero.	R
5	TT_INT	Transfer Terminate Interrupt. Set 1 clear the Interrupt, Set 0 has no effect.	RWC
4	LTT_INT	Last Transfer Terminate Interrupt. Set 1 clear the Interrupt, Set 0 has no effect.	RWC
3	TT	Transfer Terminate. 0: Descriptor or No-Descriptor DMA transfer does not end 1: No-Link Descriptor or No-Descriptor DMA transfer end Set 1 clear the status, Set 0 has no effect.	RWC
2	LTT	Last Transfer Terminate. 0: Last Descriptor DMA transfer does not end 1: Last Descriptor DMA transfer end (The field is Ignored in No-Descriptor Transfer) Set 1 clear the status, Set 0 has no effect.	RWC
1	Reserved	Write has no effect, read as zero.	R
0	LINK	Descriptor Link Enable. 0: disable; 1: enable. (the field is ignored in No-Descriptor Transfer mode, for debug)	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.1.3.5 DMA Channel Command (DCMn, n = 0 ~ 9)

	DCMn																BASE + 0x10 + (n*0x18)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NDES	Reserved																						BAI	Reserved	TSZ			Reserved		TIE	LTIE
RST	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	NDES	Descriptor or No-Descriptor Transfer Select. 0: Descriptor Transfer; 1: No-descriptor Transfer.	RW
30:9	Reserved	Write has no effect, read as zero	R
8	BAI	Bus Address Increment. 0: no increment; 1: increment.	RW
7	Reserved	Write has no effect, read as zero	R
6:4	TSZ	Burst Length Selection, Transfer Data Size of a data unit.	RW
3:2	Reserved	Write has no effect, read as zero	R
1	TIE	Transfer Interrupt Enable (TIE). 0: disable interrupt; 1: enable interrupt when TT is set to 1.	RW
0	LTIE	Last Transfer Interrupt Enable 0: disable interrupt; 1: enable interrupt when TT is set to 1.	RW

	Burst Length
000	1 word
001	4 word
010	8 word
011	16 word
100	32 word

12.2.1.3.6 DMA Descriptor Address (DDAn, n = 0 ~ 9)

This register is ignored in No-Descriptor Transfer mode.

	DDAn																BASE + 0x14 + (n*0x18)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DBA	Descriptor Base Address.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.1.3.7 DMA Global Reset Register (DGRR)

	DGRR																BASE + 0x100															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															RESET
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0

Bits	Name	Description	RW
31:1	Reserved	Write has no effect, read as zero.	R
0	RESET	DMA Global Reset.	W

12.2.1.3.8 DMA Global Enable Register (DGER)

	DGER																BASE + 0x104															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															DMA_EN
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0

Bits	Name	Description	RW
31:1	Reserved	Write has no effect, read as zero.	R
0	DMA_EN	DMA Global Enable.	WR

12.2.1.3.9 AUDIO Exception Interrupt Enable Register (AEER)

	AEER																BASE + 0x108															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															EXP_EN
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0

Bits	Name	Description	RW
31:1	Reserved	Write has no effect, read as zero.	R
0	EXP_EN	Exception Interrupt Enable.	WR

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.1.3.10 AUDIO Exception Interrupt Status Register (AESR)

	AESR																BASE + 0x10c													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															EXP
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0

Bits	Name	Description	RW
31:1	Reserved	Write has no effect, read as zero.	R
0	EXP	Exception Interrupt status. 0: AHB slave data transfer is normal. 1: AHB slave data transfer is exception. Set 1 clear the status, Set 0 has no effect.	R

12.2.1.3.11 AUDIO Interrupt Pending Register (AIPR)

	AIPR																				BASE + 0x110										
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				EXP_INT	DMIC_INT	DMA_INT9	DMA_INT8	DMA_INT7	DMA_INT6	DMA_INT5	DMA_INT4	DMA_INT3	DMA_INT2	DMA_INT1	DMA_INT0
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Write has no effect, read as zero.	R
11	EXP_INT	Exception Interrupt	R
10	DMIC_INT	DMIC Interrupt	R
9	DMA_INT9	DMA9 Interrupt	R
8	DMA_INT8	DMA8 Interrupt	R
7	DMA_INT7	DMA7 Interrupt	R
6	DMA_INT6	DMA6 Interrupt	R
5	DMA_INT5	DMA5 Interrupt	R
4	DMA_INT4	DMA4 Interrupt	R
3	DMA_INT3	DMA3 Interrupt	R
2	DMA_INT2	DMA2 Interrupt	R
1	DMA_INT1	DMA1 Interrupt	R
0	DMA_INT0	DMA0 Interrupt	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.1.4 FIFO Control Register Descriptions

Name	Base	Description
A_DMA	134d1000	Base address of Audio DMA.

12.2.1.4.1 FIFO Address Space (FASn, n = 0 ~ 9)

	FASn																BASE + 0x00 + (n*0x10)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																FAD															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:13	Reserved	Write has no effect, read as zero.	RW
12:0	FAD	FIFO Address Depth.	RW

NOTE: FAD0 + …… FADn <= Total Space

12.2.1.4.2 FIFO Control Register(FCR, n = 0 ~ 9)

	FCRn																BASE + 0x04 + (n*0x10)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													FLUSH	FULL_EN	FIFO_EN
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Write has no effect, read as zero.	RW
2	FLUSH	FIFO Flush. Write 1 to this bit flush FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
1	FULL_EN	Writing 1 to this bit, data is block in receive FIFO.	RW
0	FIFO_EN	Enable FIFO Function. This bit is used to disable or enable the FIFO . 0: FIFO Function Disable 1: FIFO Function Enable	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.1.4.3 FIFO Configuration Register(FFR, n = 0 ~ 9)

	FFRn																BASE + 0x08 + (n*0x10)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			FTH													Reserved						TUR/RORE	FSE	FIFO_TD	Reserved						
RST	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	0	0	0	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:29	Reserved	Write has no effect, read as zero.	R
28:16	FTH	FIFO threshold for interrupt or DMA request. The FTH valid value is 0 ~ 31. Note: IN dma mode, FTH should be equal to dma burstlen	RW
15:10	Reserved	Write has no effect, read as zero.	R
9	TUR/RORE	Enable TUR/ROR Interrupt. This bit is used to control the TUR/ROR interrupt enable or disable. 0: Disable 1: Enable	RW
8	FSE	Enable TFS/RFS Interrupt. This bit is used to control the TFS/RFS interrupt enable or disable. 0: Disable 1: Enable	RW
7	FIFO_TD	FIFO Transfer Direction. 0: Data Transfer from DDR to Audio System FIFO(read) 1: Data Transfer from Audio System FIFO to DDR (write)	RW
6:0	Reserved	Write has no effect, read as zero.	R

12.2.1.4.4 FIFO Status Register(FSR, n = 0 ~ 9)

	FSRn																BASE + 0x0C + (n*0x10)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			FLEVEL													Reserved										TUR/TOR_INPRO	TFS/RFS_INPRO	Reserved	TUR/ROR	Reserved	TFS/RFS
RST	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	0	0	?	0	?	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>RW</th></tr>
<tr><td>31:29</td><td>Reserved</td><td>Write has no effect, read as zero.</td><td>R</td></tr>
<tr><td>28:16</td><td>FLEVEL</td><td>FIFO Level. The bits indicate the amount of valid PCM data in FIFO.</td><td>R</td></tr>
<tr><td>15:6</td><td>Reserved</td><td>Write has no effect, read as zero.</td><td>RW</td></tr>
<tr><td>5</td><td>TUR/ROR_INPO</td><td>When 1’b1: Clear of TUR/ROT is in progress</td><td>R</td></tr>
<tr><td>4</td><td>TFS/RFS_INPRO</td><td>When 1’b1: Clear of TFS/RFS is in progress</td><td>R</td></tr>
<tr><td>3</td><td>Reserved</td><td>Write has no effect, read as zero.</td><td>RW</td></tr>
<tr><td>2</td><td>TUR/ROR</td><td>Transmit FIFO Under Run/Receive FIFO Over Run. This bit indicates that transmit FIFO has or has not experienced an under-run.
Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun.
Set 1 clear the status, Set 0 has no effect.</td><td>RWC</td></tr>
<tr><td>1</td><td>Reserved</td><td>Write has no effect, read as zero.</td><td>R</td></tr>
<tr><td>0</td><td>TFS/RFS</td><td>Transmit FIFO Service Request. This bit indicates that transmit FIFO level is below Transmit FIFO threshold, which is controlled by FCR.FTH. When TFS is 1, it may trigger interrupt or DMA request depends on the interrupt enable and DMA setting.
Set 1 clear the status, Set 0 has no effect.
<table>
<tr><th>TFS</th><th>Description</th></tr>
<tr><td>0</td><td>Transmit FIFO level exceeds TFL threshold.</td></tr>
<tr><td>1</td><td>Transmit FIFO level at or below TFL threshold.</td></tr>
</table>
Receive FIFO Service Request. This bit indicates that receive FIFO level is or not below receive FIFO threshold, which is controlled by FCR.FTH. When RFS is 1, it may trigger interrupt or DMA request depends on the interrupt enable and DMA setting.
Set 1 clear the status, Set 0 has no effect.
<table>
<tr><th>RFS</th><th>Description</th></tr>
<tr><td>0</td><td>Receive FIFO level below RFL threshold.</td></tr>
<tr><td>1</td><td>Receive FIFO level at or above RFL threshold.</td></tr>
</table></td><td>RWC</td></tr>
</table>

12.2.1.5 DMA operation

12.2.1.5.1 DMA initialize in descriptor mode

1. Select DMAn(n=0~9) and reset it, set DCRn.RESET=1
2. Set DCMn.NDES=0
3. Set first descriptor’s address in DDAn. Fill in descriptor refer to Descriptor Structure
4. Configure DCMn.TIE, DCMn.LTIE to choose whether to use interrupt
5. Set DCRn.CTE = 1 to enable and activate DMAn

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.1.5.2 DMA initialize in no descriptor mode

1. Select DMAn(n=0~9) and reset it, set DCRn.RESET=1
2. Set DCMn.NDES=1
3. Configure DBA, DTC, DCM.BAI, DCM.TSZ
4. Configure DCMn.TIE, DCMn.LTIE to choose whether to use interrupt
5. Set DCRn.CTE = 1 to enable and activate DMAn

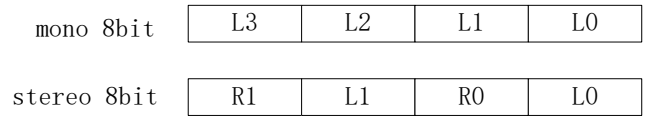
12.2.1.5.3 FIFO initialize

1. Select FIFOn(n=0~9), please accommodate FIFOn to DMAn
2. Configure FASn.FAD
3. Configure FFRn.FTH, when using dma mode, please accommodate FFRn.FTH to DMAn transfer data size
4. Configure FFRn.FIFO_TD
5. Set FFRn.FIFO_EN to enable and activate FIFOn

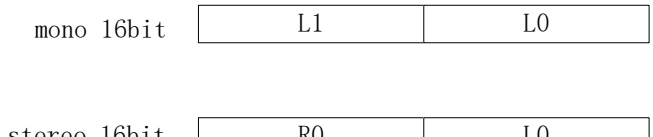
12.2.2 Format Converter

12.2.2.1 DATA FORMAT Diagram

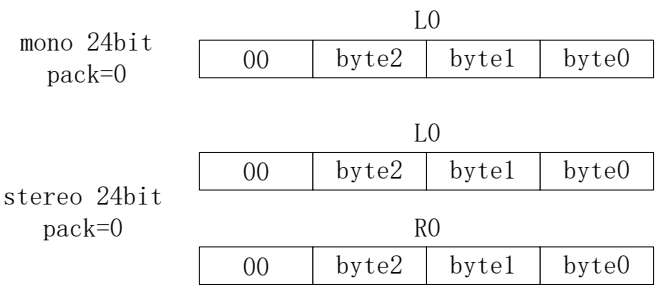
Data format in register(32bit):



8bit Data Format

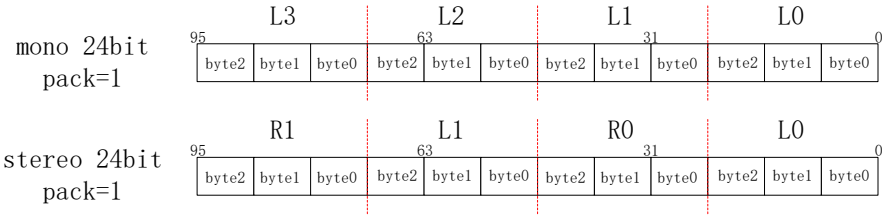


16bit Data Format



24bit Data Format of no-compression

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.



24bit Data Format of compression

12.2.2.2 Register Descriptions

Name	Base	Description
A_DFMT	134d2000	Base address of Audio Data Format.

12.2.2.2.1 Data Format Control Register(DFCRn, n=0~9)

DFCRn																	BASE + 0x00 + (n*0x04)												
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CHNUM				Reserved	SS			Reserved					PACK_EN	RESET	ENABLE
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	?	0	0	0	?	?	?	?	?	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Write has no effect, read as zero.	R
15:12	CHNUM	data interface channel number. 0: Mono 1: Stereo 3: 4 channel 5: 6 channel 7: 8 channel 9: 10 channel 11:12 channel Other: Reserved	RW
11	Reserved	Write has no effect, read as zero.	R
10:8	SS	Sample Size. These bits reflect output/input sample data size from/to memory or register. The data sizes supported are: 8/12/13/16/18/20/24/32 bits. The sample data is LSB-justified in memory/register.	

OSS	Sample Size
0x0	8 bit.
0x1	12 bit.
0x2	13 bit.
0x3	16 bit.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

			0x4	18 bit.		
			0x5	20 bit.		
			0x6	24 bit.		
			0x7	32 bit.		
7:3	Reserved	Write has no effect, read as zero.				R
2	PACK_EN	Pack the 18/20/24-bit data to FIFO aim to economize the FIFO. Only used for replay. Set this bit to '1' will enable the function.(8/12/13/16/32 only pack mode)				RW
1	RESET	software-reset.				RW
0	ENABLE	Enable Recording Function. This bit is used to disable or enable the channel used for data receiving.				RW

NOTE: T_EN and R_EN only one enable

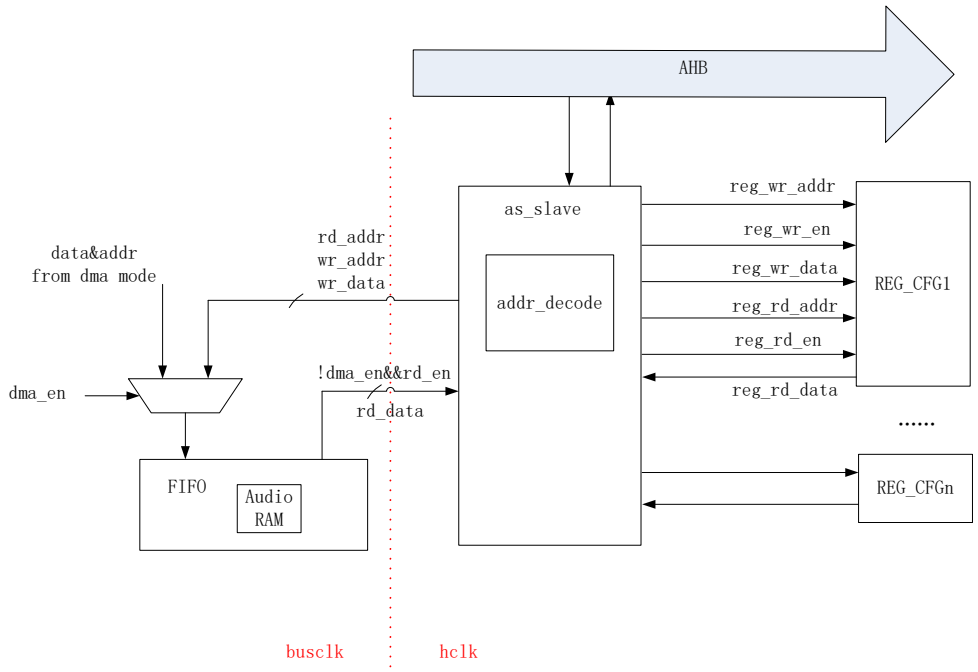
12.2.2.3 FMT OPERATION

1. Select DFMTn(n=0~9), please accommodate DFMTn to DMAn
2. Configure DFCRn.CHUNUM, if DFMTn is used for SPDIF IN, keep DFCRn.CHNUM=0x0
3. Configure DFCRn.SS, if DFMTn is used for SPDIF IN, keep DFCRn.SS=0x7
4. Configure DFCRn.PACK_EN, if DFMTn is used for recording, keep DFCRn.PACK_EN=0x0
5. Set DFCRn.ENABLE to enable and activate FMTn

12.2.3 Internal CBUS

12.2.3.1 Block Diagram

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.



12.2.3.2 Register Descriptions

Name	Base	Description
A_DFMT	134d3000	Base address of Audio Data Format.

12.2.3.2.1 FIFO Data Register (FDR)

	FDRn																BASE + 0x00															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FDATA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FDATA	FIFO data register. This register is connect to the FIFO. Only used for CPU mode	RW

12.2.3.3 CPU mode operation

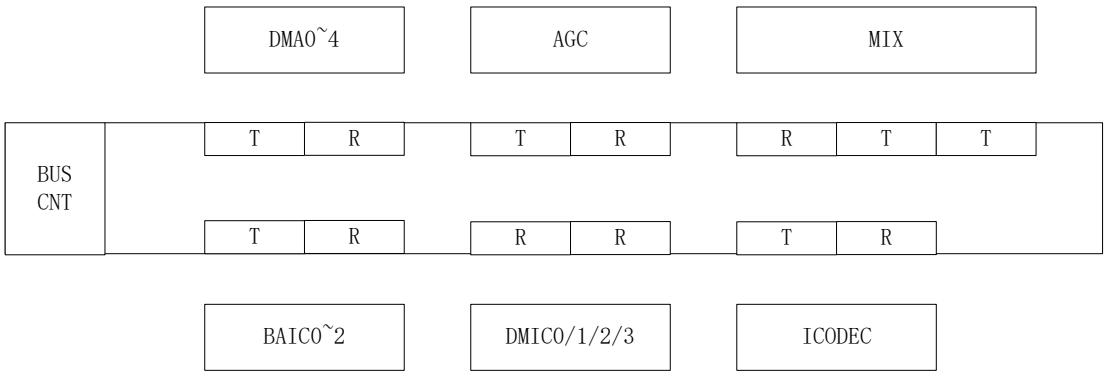
1. Set DCRn.CTE = 0
2. FIFOn initialization
3. FMTn initialization

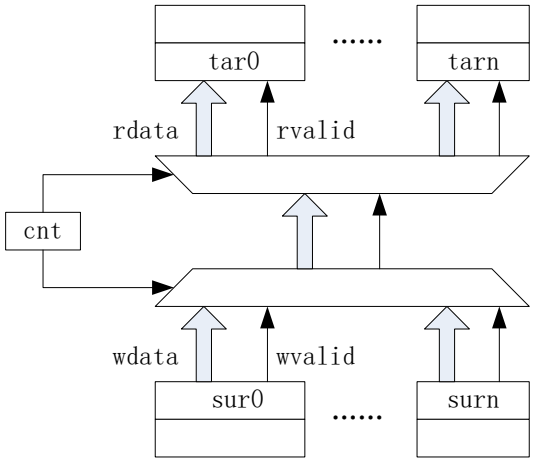
Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4. Wait FSRn.TRS/RFS=1, than read FDR address

12.2.4 nternal DBUS

12.2.4.1 Block Diagram





12.2.4.2 Register Descriptions

Name	Base	Description
Audio_IBUS	134d4000	Base address of Audio Internal Bus.

12.2.4.2.1 BUS TimeSlot Set Register (BTSET)

	BTSET																BASE + 0x0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSLOT_SET																															Reserved

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?

Bits	Name	Description	RW
31:1	TSLOT_SET	Timeslot Set Enable. Set 1 enable the timeslot, Set 0 has no effect.	W
0	Reserved	Write has no effect, read as zero.	R

12.2.4.2.2 BUS TimeSlot Clear Register (BTCLR)

	BTCLK																BASE + 0x4														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSLOT_CLR																															Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?

Bits	Name	Description	RW
31:1	TSLOT_CLR	Timeslot Clear Enable. Set 1 clear the timeslot, Set 0 has no effect.	W
0	Reserved	Write has no effect, read as zero.	RW

12.2.4.2.3 BUS TimeSlot Status Register (BTSR)

	BTSR																BASE + 0x8														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSLOT_EN																															Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?

Bits	Name	Description	RW
31:1	TSLOT_EN	Timeslot Clear Enable. Set 1 clear the timeslot, Set 0 has no effect.	R
0	Reserved	Write has no effect, read as zero.	RW

12.2.4.2.4 BUS FIFO Status Register (BFSR)

	BFSR																BASE + 0xC														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved				DEV11_TUR	DEV10_TUR	DEV9_TUR	DEV8_TUR	DEV7_TUR	DEV6_TUR	DEV5_TUR	DEV4_TUR	DEV3_TUR	DEV2_TUR	DEV1_TUR	DEV0_TUR	Reserved	DEV14_ROR	DEV13_ROR	DEV12_ROR	DEV11_ROR	DEV10_ROR	DEV9_ROR	DEV8_ROR	DEV7_ROR	DEV6_ROR	DEV5_ROR	DEV4_ROR	DEV3_ROR	DEV2_ROR	DEV1_ROR	DEV0_ROR
RST	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Write has no effect, read as zero.	RW
27	DEV11_TUR	DEV Port Transmit FIFO Under Run. This bit indicates that transmit FIFO has or has not experienced an under-run. 0: When read, indicates under-run has not been found. 1: When read, indicates data has even been read from empty transmit FIFO.	R
26	DEV10_TUR	DEV Port Transmit FIFO Under Run. This bit indicates that transmit FIFO has or has not experienced an under-run. 0: When read, indicates under-run has not been found. 1: When read, indicates data has even been read from empty transmit FIFO.	R
25	DEV9_TUR	DEV Port Transmit FIFO Under Run. This bit indicates that transmit FIFO has or has not experienced an under-run. 0: When read, indicates under-run has not been found. 1: When read, indicates data has even been read from empty transmit FIFO.	R
24	DEV8_TUR	DEV Port Transmit FIFO Under Run. This bit indicates that transmit FIFO has or has not experienced an under-run. 0: When read, indicates under-run has not been found. 1: When read, indicates data has even been read from empty transmit FIFO.	R
23	DEV7_TUR	DEV Port Transmit FIFO Under Run. This bit indicates that transmit FIFO has or has not experienced an under-run. 0: When read, indicates under-run has not been found. 1: When read, indicates data has even been read from empty transmit FIFO.	R
22	DEV6_TUR	DEV Port Transmit FIFO Under Run. This bit indicates that transmit FIFO has or has not experienced an under-run. 0: When read, indicates under-run has not been found. 1: When read, indicates data has even been read from empty transmit FIFO.	R
21	DEV5_TUR	DEV Port Transmit FIFO Under Run. This bit indicates that transmit FIFO has or has not experienced an under-run. 0: When read, indicates under-run has not been found. 1: When read, indicates data has even been read from empty transmit	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		FIFO.	
20	DEV4_TUR	DEV Port Transmit FIFO Under Run. This bit indicates that transmit FIFO has or has not experienced an under-run. 0: When read, indicates under-run has not been found. 1: When read, indicates data has even been read from empty transmit FIFO.	R
19	DEV3_TUR	DEV Port Transmit FIFO Under Run. This bit indicates that transmit FIFO has or has not experienced an under-run. 0: When read, indicates under-run has not been found. 1: When read, indicates data has even been read from empty transmit FIFO.	R
18	DEV2_TUR	DEV Port Transmit FIFO Under Run. This bit indicates that transmit FIFO has or has not experienced an under-run. 0: When read, indicates under-run has not been found. 1: When read, indicates data has even been read from empty transmit FIFO.	R
17	DEV1_TUR	DEV Port Transmit FIFO Under Run. This bit indicates that transmit FIFO has or has not experienced an under-run. 0: When read, indicates under-run has not been found. 1: When read, indicates data has even been read from empty transmit FIFO.	R
16	DEV0_TUR	DEV Port Transmit FIFO Under Run. This bit indicates that transmit FIFO has or has not experienced an under-run. 0: When read, indicates under-run has not been found. 1: When read, indicates data has even been read from empty transmit FIFO.	R
15	Reserved	Write has no effect, read as zero.	
14	DEV14_ROR	DEV Port Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun. 0: When read, indicates over-run has not been found. 1: When read, indicates data has even been written to full receive FIFO.	R
13	DEV13_ROR	DEV Port Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun. 0: When read, indicates over-run has not been found. 1: When read, indicates data has even been written to full receive FIFO.	R
12	DEV12_ROR	DEV Port Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun. 0: When read, indicates over-run has not been found. 1: When read, indicates data has even been written to full receive FIFO.	R
11	DEV11_ROR	DEV Port Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun. 0: When read, indicates over-run has not been found. 1: When read, indicates data has even been written to full receive FIFO.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

10	DEV10_ROR	DEV Port Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun. 0: When read, indicates over-run has not been found. 1: When read, indicates data has even been written to full receive FIFO.	R
9	DEV9_ROR	DEV Port Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun. 0: When read, indicates over-run has not been found. 1: When read, indicates data has even been written to full receive FIFO.	R
8	DEV8_ROR	DEV Port Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun. 0: When read, indicates over-run has not been found. 1: When read, indicates data has even been written to full receive FIFO.	R
7	DEV7_ROR	DEV Port Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun. 0: When read, indicates over-run has not been found. 1: When read, indicates data has even been written to full receive FIFO.	R
6	DEV6_ROR	DEV Port Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun. 0: When read, indicates over-run has not been found. 1: When read, indicates data has even been written to full receive FIFO.	R
5	DEV5_ROR	DEV Port Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun. 0: When read, indicates over-run has not been found. 1: When read, indicates data has even been written to full receive FIFO.	R
4	DEV4_ROR	DEV Port Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun. 0: When read, indicates over-run has not been found. 1: When read, indicates data has even been written to full receive FIFO.	R
3	DEV3_ROR	DEV Port Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun. 0: When read, indicates over-run has not been found. 1: When read, indicates data has even been written to full receive FIFO.	R
2	DEV2_ROR	DEV Port Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun. 0: When read, indicates over-run has not been found. 1: When read, indicates data has even been written to full receive FIFO.	R
1	DEV1_ROR	DEV Port Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun. 0: When read, indicates over-run has not been found. 1: When read, indicates data has even been written to full receive FIFO.	R
0	DEV0_ROR	DEV Port Receive FIFO Over Run. This bit indicates that receive FIFO has or has not experienced an overrun. 0: When read, indicates over-run has not been found.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: When read, indicates data has even been written to full receive FIFO.	

12.2.4.2.5 BUS FIFO Control Register0 (BFCR0)

	BFCR0																BASE + 0x10													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				DEV11_RFIFO	DEV10_RFIFO	DEV9_RFIFO	DEV8_RFIFO	DEV7_RFIFO	DEV6_RFIFO	DEV5_RFIFO	DEV4_RFIFO	DEV3_RFIFO	DEV2_RFIFO	DEV1_RFIFO	DEV0_RFIFO	Reserved	DEV14_RFIFO	DEV13_RFIFO	DEV12_RFIFO	DEV11_RFIFO	DEV10_RFIFO	DEV9_RFIFO	DEV8_RFIFO	DEV7_RFIFO	DEV6_RFIFO	DEV5_RFIFO	DEV4_RFIFO	DEV3_RFIFO	DEV2_RFIFO	DEV1_RFIFO	DEV0_RFIFO
RST	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Write has no effect, read as zero.	RW
27	DEV11_TFIFO	DEV11 Port Transmit FIFO Flush. Write 1 to this bit flush transmit FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
26	DEV10_TFIFO	DEV10 Port Transmit FIFO Flush. Write 1 to this bit flush transmit FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
25	DEV9_TFIFO	DEV9 Port Transmit FIFO Flush. Write 1 to this bit flush transmit FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
24	DEV8_TFIFO	DEV8 Port Transmit FIFO Flush. Write 1 to this bit flush transmit FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
23	DEV7_TFIFO	DEV7 Port Transmit FIFO Flush. Write 1 to this bit flush transmit FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
22	DEV6_TFIFO	DEV6 Port Transmit FIFO Flush. Write 1 to this bit flush transmit FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
21	DEV5_TFIFO	DEV5 Port Transmit FIFO Flush. Write 1 to this bit flush transmit FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
20	DEV4_TFIFO	DEV4 Port Transmit FIFO Flush. Write 1 to this bit flush transmit FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
19	DEV3_TFIFO	DEV3 Port Transmit FIFO Flush. Write 1 to this bit flush transmit FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
18	DEV2_TFIFO	DEV2 Port Transmit FIFO Flush. Write 1 to this bit flush transmit FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
17	DEV1_TFIFO	DEV1 Port Transmit FIFO Flush. Write 1 to this bit flush transmit FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
16	DEV0_TFIFO	DEV0 Port Transmit FIFO Flush. Write 1 to this bit flush transmit FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
15	Reserved	Write has no effect, read as zero.	
14	DEV14_R	DEV14 Port Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	FIFO	empty. Writing 0 to this bit has no effect and this bit is always reading 0.	
13	DEV13_RFIFO	DEV13 Port Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
12	DEV12_RFIFO	DEV12 Port Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
11	DEV11_RFIFO	DEV11 Port Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
10	DEV10_RFIFO	DEV10 Port Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
9	DEV9_RFIFO	DEV9 Port Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
8	DEV8_RFIFO	DEV8 Port Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
7	DEV7_RFIFO	DEV7 Port Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
6	DEV6_RFIFO	DEV6 Port Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
5	DEV5_RFIFO	DEV5 Port Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
4	DEV4_RFIFO	DEV4 Port Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
3	DEV3_RFIFO	DEV3 Port Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
2	DEV2_RFIFO	DEV2 Port Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
1	DEV1_RFIFO	DEV1 Port Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W
0	DEV0_RFIFO	DEV0 Port Receive FIFO Flush. Write 1 to this bit flush receive FIFOs to empty. Writing 0 to this bit has no effect and this bit is always reading 0.	W

12.2.4.2.6 BUS FIFO Control Register1 (BFCR1)

	BFCR1																BASE + 0x14													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				DEV11_LSMP	DEV10_LSMP	DEV9_LSMP	DEV8_LSMP	DEV7_LSMP	DEV6_LSMP	DEV5_LSMP	DEV4_LSMP	DEV3_LSMP	DEV2_LSMP	DEV1_LSMP	DEV0_LSMP
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Write has no effect, read as zero.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

11	DEV11_LSMP	Select between play last sample or play ZERO sample in TX FIFO underflow. ZERO sample means sample value is zero. This bit is better be changed while audio replay is stopped. 1: Play ZERO sample when TX FIFO underflow. 0: Play last sample when TX FIFO underflow.	RW
10	DEV10_LSMP	Select between play last sample or play ZERO sample in TX FIFO underflow. ZERO sample means sample value is zero. This bit is better be changed while audio replay is stopped. 1: Play ZERO sample when TX FIFO underflow. 0: Play last sample when TX FIFO underflow.	RW
9	DEV9_LSMP	Select between play last sample or play ZERO sample in TX FIFO underflow. ZERO sample means sample value is zero. This bit is better be changed while audio replay is stopped. 1: Play ZERO sample when TX FIFO underflow. 0: Play last sample when TX FIFO underflow.	RW
8	DEV8_LSMP	Select between play last sample or play ZERO sample in TX FIFO underflow. ZERO sample means sample value is zero. This bit is better be changed while audio replay is stopped. 1: Play ZERO sample when TX FIFO underflow. 0: Play last sample when TX FIFO underflow.	RW
7	DEV7_LSMP	Select between play last sample or play ZERO sample in TX FIFO underflow. ZERO sample means sample value is zero. This bit is better be changed while audio replay is stopped. 1: Play ZERO sample when TX FIFO underflow. 0: Play last sample when TX FIFO underflow.	RW
6	DEV6_LSMP	Select between play last sample or play ZERO sample in TX FIFO underflow. ZERO sample means sample value is zero. This bit is better be changed while audio replay is stopped. 1: Play ZERO sample when TX FIFO underflow. 0: Play last sample when TX FIFO underflow.	RW
5	DEV5_LSMP	Select between play last sample or play ZERO sample in TX FIFO underflow. ZERO sample means sample value is zero. This bit is better be changed while audio replay is stopped. 1: Play ZERO sample when TX FIFO underflow. 0: Play last sample when TX FIFO underflow.	RW
4	DEV4_LSMP	Select between play last sample or play ZERO sample in TX FIFO underflow. ZERO sample means sample value is zero. This bit is better be changed while audio replay is stopped. 1: Play ZERO sample when TX FIFO underflow. 0: Play last sample when TX FIFO underflow.	RW
3	DEV3_LSMP	Select between play last sample or play ZERO sample in TX FIFO underflow. ZERO sample means sample value is zero. This bit is better be changed while audio replay is stopped.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: Play ZERO sample when TX FIFO underflow. 0: Play last sample when TX FIFO underflow.	
2	DEV2_LSMP	Select between play last sample or play ZERO sample in TX FIFO underflow. ZERO sample means sample value is zero. This bit is better be changed while audio replay is stopped. 1: Play ZERO sample when TX FIFO underflow. 0: Play last sample when TX FIFO underflow.	RW
1	DEV1_LSMP	Select between play last sample or play ZERO sample in TX FIFO underflow. ZERO sample means sample value is zero. This bit is better be changed while audio replay is stopped. 1: Play ZERO sample when TX FIFO underflow. 0: Play last sample when TX FIFO underflow.	RW
0	DEV0_LSMP	Select between play last sample or play ZERO sample in TX FIFO underflow. ZERO sample means sample value is zero. This bit is better be changed while audio replay is stopped. 1: Play ZERO sample when TX FIFO underflow. 0: Play last sample when TX FIFO underflow.	RW

12.2.4.2.7 BUS FIFO Control Register2 (BFCR2)

	BFCR2																BASE + 0x18													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	DEV14_DBE	DEV13_DBE	DEV12_DBE	DEV11_DBE	DEV10_DBE	DEV9_DBE	DEV8_DBE	DEV7_DBE	DEV6_DBE	DEV5_DBE	DEV4_DBE	DEV3_DBE	DEV2_DBE	DEV1_DBE	DEV0_DBE
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:15	Reserved	Write has no effect, read as zero.	R
14	DEV14_DBE	Data trans block enable in RX FIFO overflow. 1: Data is blocking(not discard) when RX FIFO overflow. 0: Data is discard when RX FIFO overflow.	RW
13	DEV13_DBE	Data trans block enable in RX FIFO overflow. 1: Data is blocking(not discard) when RX FIFO overflow. 0: Data is discard when RX FIFO overflow.	RW
12	DEV12_DBE	Data trans block enable in RX FIFO overflow. 1: Data is blocking(not discard) when RX FIFO overflow. 0: Data is discard when RX FIFO overflow.	RW
11	DEV11_DBE	Data trans block enable in RX FIFO overflow. 1: Data is blocking(not discard) when RX FIFO overflow. 0: Data is discard when RX FIFO overflow.	RW
10	DEV10_D	Data trans block enable in RX FIFO overflow.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	BE	1: Data is blocking(not discard) when RX FIFO overflow. 0: Data is discard when RX FIFO overflow.	
9	DEV9_DBE	Data trans block enable in RX FIFO overflow. 1: Data is blocking(not discard) when RX FIFO overflow. 0: Data is discard when RX FIFO overflow.	RW
8	DEV8_DBE	Data trans block enable in RX FIFO overflow. 1: Data is blocking(not discard) when RX FIFO overflow. 0: Data is discard when RX FIFO overflow.	RW
7	DEV7_DBE	Data trans block enable in RX FIFO overflow. 1: Data is blocking(not discard) when RX FIFO overflow. 0: Data is discard when RX FIFO overflow.	RW
6	DEV6_DBE	Data trans block enable in RX FIFO overflow. 1: Data is blocking(not discard) when RX FIFO overflow. 0: Data is discard when RX FIFO overflow.	RW
5	DEV5_DBE	Data trans block enable in RX FIFO overflow. 1: Data is blocking(not discard) when RX FIFO overflow. 0: Data is discard when RX FIFO overflow.	RW
4	DEV4_DBE	Data trans block enable in RX FIFO overflow. 1: Data is blocking(not discard) when RX FIFO overflow. 0: Data is discard when RX FIFO overflow.	RW
3	DEV3_DBE	Data trans block enable in RX FIFO overflow. 1: Data is blocking(not discard) when RX FIFO overflow. 0: Data is discard when RX FIFO overflow.	RW
2	DEV2_DBE	Data trans block enable in RX FIFO overflow. 1: Data is blocking(not discard) when RX FIFO overflow. 0: Data is discard when RX FIFO overflow.	RW
1	DEV1_DBE	Data trans block enable in RX FIFO overflow. 1: Data is blocking(not discard) when RX FIFO overflow. 0: Data is discard when RX FIFO overflow.	RW
0	DEV0_DBE	Data trans block enable in RX FIFO overflow. 1: Data is blocking(not discard) when RX FIFO overflow. 0: Data is discard when RX FIFO overflow.	RW

12.2.4.2.8 BUS Source Timeslot0 (BST0)

	BST0																**BASE + 0x1C**														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	DEV5_SUR					DEV4_SUR					DEV3_SUR					Reserved	DEV2_SUR					DEV1_SUR					DEV0_SUR				
RST	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31	Reserved	Write has no effect, read as zero.	RW
30:26	DEV5_SUR	DEV5 Source Timeslot ID	
25:21	DEV4_SUR	DEV4 Source Timeslot ID	
20:16	DEV3_SUR	DEV3 Source Timeslot ID	
15	Reserved	Write has no effect, read as zero.	
14:10	DEV2_SUR	DEV 2 Source Timeslot ID	
9:5	DEV1_SUR	DEV 1 Source Timeslot ID	
4:0	DEV0_SUR	DEV0 Source Timeslot ID	

12.2.4.2.9 BUS Source Timeslot1 (BST1)

	BST1																BASE + 0x20															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						DEV10_SUR					DEV9_SUR					Reserved	DEV8_SUR					DEV7_SUR					DEV6_SUR				
RST	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Write has no effect, read as zero.	R
25:21	DEV10_SUR	DEV10 Channel4 Source Timeslot ID	RW
20:16	DEV9_SUR	DEV9 Channel3 Source Timeslot ID	RW
15	Reserved	Write has no effect, read as zero.	R
14:10	DEV 8_SUR	DEV8 Channel2 Source Timeslot ID	RW
9:5	DEV7_SUR	DEV7 Channel1 Source Timeslot ID	RW
4:0	DEV6_SUR	DEV6 Channel0 Source Timeslot ID	RW

12.2.4.2.10 BUS Source Timeslot2 (BST2)

	BST2																BASE + 0x24															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											DEV14_SUR					Reserved	DEV13_SUR					DEV12_SUR					DEV11_SUR				
RST	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:21	Reserved	Write has no effect, read as zero.	R
20:16	DEV14_SUR	DEV14 Source Timeslot ID	RW
15	Reserved	Write has no effect, read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

14:10	DEV13_SUR	DEV13 Source Timeslot ID	RW
9:5	DEV12_SUR	DEV12 BF Source Timeslot ID	RW
4:0	DEV11_SUR	DEV11 LR Source Timeslot ID	RW

12.2.4.2.11 BUS Target Timeslot0 (BTT0)

	BTT0																BASE + 0x28														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	DEV5_SUR					DEV4_SUR					DEV3_SUR					Reserved	DEV2_SUR					DEV1_SUR					DEV0_SUR				
RST	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Reserved	Write has no effect, read as zero.	R
30:26	DEV5_TAR	DEV5 Target Timeslot ID	RW
25:21	DEV4_ TAR	DEV4 Target Timeslot ID	RW
20:16	DEV3_ TAR	DEV3 Target Timeslot ID	RW
15	Reserved	Write has no effect, read as zero.	R
14:10	DEV2_ TAR	DEV2 Target Timeslot ID	RW
9:5	DEV1_ TAR	DEV1 Target Timeslot ID	RW
4:0	DEV 0_ TAR	DEV0 Target Timeslot ID	RW

12.2.4.2.12 BUS Target Timeslot1 (BTT1)

	BTT1																BASE + 0x2C														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						SUR4					SUR3					Reserved	SUR2					SUR1					SUR0				
RST	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Reserved	Write has no effect, read as zero.	RW
30:26	DEV11_TAR	DEV11 Target Timeslot ID	RW
25:21	DEV10_TAR	DEV10 Target Timeslot ID	RW
20:16	DEV9_TAR	DEV9 Target Timeslot ID	RW
15	Reserved	Write has no effect, read as zero.	R
14:10	DEV8_TAR	DEV8 Target Timeslot ID	RW
9:5	DEV7_TAR	DEV7 Target Timeslot ID	RW
4:0	DEV6_TAR	DEV6 Target Timeslot ID	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.4.3 device map

		Receive ID		
bus_receive0	DMIC	1	bus_transmit0	Reserved
bus_receive1	SPDIF_IN	2	bus_transmit1	BAIC1
bus_receive2	BAIC0	3	bus_transmit2	SPDIF_OUT
bus_receive3	BAIC1	4	bus_transmit3	BAIC3
bus_receive4	BAIC2	5	bus_transmit4	BAIC4
bus_receive5	Reserved	6	bus_transmit5	DMA5
bus_receive6	BAIC4	7	bus_transmit6	DMA6
bus_receive7	MIXER_out	8	bus_transmit7	DMA7
bus_receive8	DMA0	9	bus_transmit8	DMA8
bus_receive9	DMA1	10	bus_transmit9	DMA9
bus_receive10	DMA2	11	bus_transmit10	MIXER_in0
bus_receive11	DMA3	12	bus_transmit11	MIXER_in1
bus_receive12	DMA4	13		
bus_receive13	Reserved			
bus_receive14	Reserved			

12.2.4.4 Internal DBUS operation

i.e: playback path from DMA0 to BAIC3

1. According to device map, find out using bus receive8, bus transmit3, slot9
2. Configure source timeslot, set DEV8_SUR=0x9
3. Configure target timeslot, set DEV3_TAR=0x9
4. Set slot enable, set BTSET.TSOT_SET[9]=1

12.2.5 BAIC

12.2.5.1 Block Diagram

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

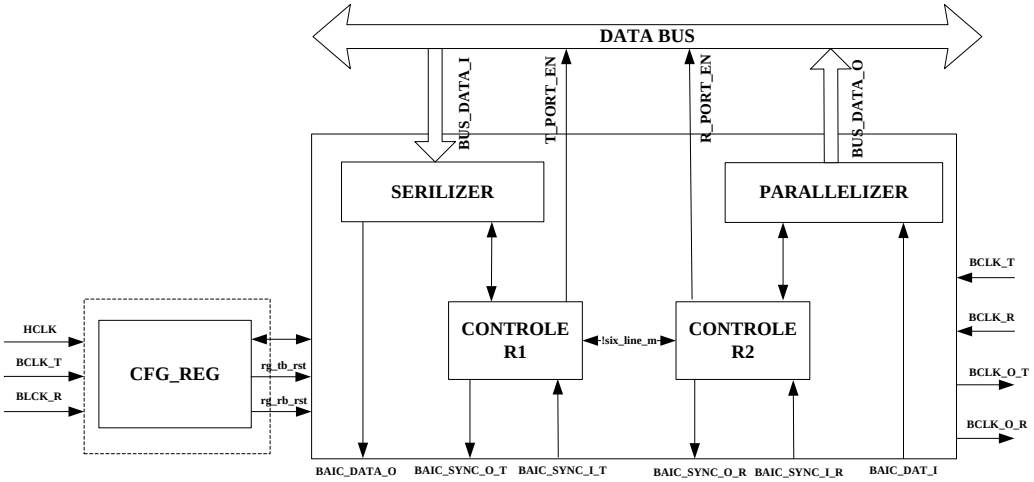


Figure 12-1 BAIC system structure

12.2.5.2 Register Descriptions

For all the users, should know here named the five BAIC(Basic Audio Interface Controller) in our Audio System as BAIC0, BAIC1,BAIC2,BAIC3 and BAIC4.

Registers Memory Map

Name	Base	Description
A_BAIC0	134d5000	Base address of BAIC0.
A_BAIC1	134d6000	Base address of BAIC1.
A_BAIC2	134d7000	Base address of BAIC2.
A_BAIC3	134d8000	Base address of BAIC3.
A_BAIC4	134d9000	Base address of BAIC4.

Name	Description	Reset Value	Address offset	Access Size
BAICRCTL	BAIC Receiver Control Register	0x00000000	0x000	32
BAICRCFG	BAIC Receiver Configure Register	0x00000001	0x004	32
BAICRDIV	BAIC Receiver CLK divide register	0x00000000	0x008	32
BAICRCGR	BAIC Receiver CLK gate Register	0x00000000	0x00c	32
BAICTCTL	BAIC Transmitter Control Register	0x00000000	0x010	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

BAICTCFG	BAIC Transmitter Configure Register	0x00000001	0x014	32
BAICTDIV	BAIC Transmitter CLK divide register	0x00000000	0x018	32
BAICTCGR	BAIC Transmitter CLK gate Register	0x00000000	0x01c	32
BAICTLCR	BAIC Top level Configure Register	0x00000000	0x020	32
BAICCCR	BAIC Common Control Register	0x00000000	0x024	32
BAICISR	BAIC Interrupt Status Register	0x00000000	0x028	32
BAICIMR	BAIC Interrupt Mask Register	0x00000000	0x02c	32

BAIC Receiver Register description

Note：Pay attention specially. When write CLK_SPLIT_EN to '1'b0', Receiver willing sharing Transmitter's registers (0x010 ~ 0x01c). Receiver's registers (0x000~0x00c) are reserved.

12.2.5.2.1 BAIC Receiver Control Register (BAICRCTL) description

	BAICRCTL																**BASE + 0x000**															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															R_RST
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	R_RST	Write 1 to this bit reset BAIC shift registers and controller. Writing 0 to this bit has no effect and this bit is always reading 0.	W

12.2.5.2.2 BAIC Receiver Configuration Register (BAICRCFG) description

	BAICRCFG																**BASE + 0x004**															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				R_SLOT				Reserved			R_SWLR	R_CHANNEL				Reserved	R_SLS		R_ISYNC	R_ASVTSU		ISS			Reserved		R_MODE				R_NEG	R_MASTER
RST	?	?	?	?	0	0	0	0	?	?	?	0	0	0	0	?	?	0	0	0	0	0	0	0	?	?	0	0	0	0	0	1

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th></th></tr>
<tr><td>31:28</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>27:24</td><td>R_SLOT</td><td>Controls the amount of valid PCM timeslot in one BAICSYN frame. Only for TDM mode.
<table>
<tr><th>R_SLOT</th><th>Number of slot in one frame</th></tr>
<tr><td>0000</td><td>1 slots</td></tr>
<tr><td>0001</td><td>2 slots</td></tr>
<tr><td>0010</td><td>Reserved</td></tr>
<tr><td>0011</td><td>4 slots</td></tr>
<tr><td>0100</td><td>Reserved</td></tr>
<tr><td>0101</td><td>6 slots</td></tr>
<tr><td>0110</td><td>Reserved</td></tr>
<tr><td>0111</td><td>8 slots</td></tr>
</table>
BAIC0, BAIC1 and BAIC4 support 1, 2 slot only. BAIC2 and BAIC3 support all the slots as the list.</td><td>RW</td></tr>
<tr><td>23:21</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>20</td><td>R_SWLR</td><td>Receiver Switch LR channels audio data. This bit control whether the low address data is L or R. It takes effective immediately when the bit is changed. Change this before record started.
<table>
<tr><th>R_SWLR</th><th>Description</th></tr>
<tr><td>0</td><td>Have no effect</td></tr>
<tr><td>1</td><td>Switch LR</td></tr>
</table></td><td>RW</td></tr>
<tr><td>19:17</td><td>R_CHANNEL</td><td>Only use for Receiver, when it work in I2S/LEFT/RIGHT Multichannel (7.1 channel) mode. These registers decide the channel number of receiver can send serial data into DATA BUS during one frame synchronization. You can configure these bits as list.
<table>
<tr><th>R_CHANNEL</th><th>Description</th></tr>
<tr><td>000</td><td>Reserved</td></tr>
<tr><td>001</td><td>2channels (1 pin)</td></tr>
<tr><td>010</td><td>4 channels (2 pins)</td></tr>
<tr><td>011</td><td>6 channels (3 pins)</td></tr>
<tr><td>100</td><td>8 channels (4 pins)</td></tr>
<tr><td>101~111</td><td>Reserved</td></tr>
</table>
BAIC0,BAIC1 and BAIC4 support stereo only. BAIC2 and BAIC3 can support 2,4,6 and 8 channel.</td><td>RW</td></tr>
<tr><td>16:15</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td></td></tr>
<tr><td>14:13</td><td>R_SLS</td><td>Receiver Slot Size can configure as list. Only for TDM mode.
<table>
<tr><th>R_SLS</th><th>Description</th></tr>
<tr><td>00</td><td>equal to data size(default)</td></tr>
</table></td><td>RW</td></tr>
</table>

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td></td><td></td><td>
<table>
<tr><td>01</td><td>16 BCLK cycles</td></tr>
<tr><td>10</td><td>32 BCLK cycles</td></tr>
<tr><td>11</td><td>64 BCLK cycles</td></tr>
</table>
Note: R_SLS is "00" slot size reference ISS.
</td><td></td></tr>
<tr><td>12</td><td>R_ISYNC</td><td>This bit use to invert SYNC. Configure this bit '1',BAIC will use invert SYNC for logic, if this bit write '0', have no effect to this block.
<table>
<tr><td>R_ISYNC</td><td>Description</td></tr>
<tr><td>0</td><td>no change (default)</td></tr>
<tr><td>1</td><td>Invert SYNC</td></tr>
</table>
</td><td>RW</td></tr>
<tr><td>11</td><td>R_ASVTSU</td><td>Audio Sample Value Transfer between Signed and Unsigned data format. This bit is used to control the signed ←→unsigned data transfer. If it is 1, the incoming or outgoing audio sample data will be transferred by toggle its most significant bit.
<table>
<tr><td>ASVTSU_R</td><td>Description</td></tr>
<tr><td>0</td><td>No audio sample value signed ←→unsigned transfer.</td></tr>
<tr><td>1</td><td>Do audio sample value signed ←→unsigned transfer.</td></tr>
</table>
</td><td>RW</td></tr>
<tr><td>10:8</td><td>ISS</td><td>BAIC input sample size. These bits reflect input data size to memory or register. The data sizes supported: 8/12/13/14/16/18/20/24/32bits. The sample data is MSB-justified in memory/register.
<table>
<tr><td>ISS</td><td>data Size</td></tr>
<tr><td>000</td><td>8 bit</td></tr>
<tr><td>001</td><td>12 bit</td></tr>
<tr><td>010</td><td>13 bit</td></tr>
<tr><td>011</td><td>16 bit</td></tr>
<tr><td>100</td><td>18bit</td></tr>
<tr><td>101</td><td>20 bit</td></tr>
<tr><td>110</td><td>24 bit</td></tr>
<tr><td>111</td><td>32 bit</td></tr>
</table>
</td><td>RW</td></tr>
<tr><td>7:6</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>5:2</td><td>R_MODE</td><td>BAIC data mode select
0000 = PCM Format mode A
0001 = PCM Format mode B
0010 = DSP Format mode A
0011 = DSP Format mode B
0100 = I2S justified mode
0101 = LEFT justified mode
0110 = RIGHT justified mode
0111：Reserved</td><td>RW</td></tr>
</table>

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1000 = TDM 1 A 1001 = TDM 1 B 1010 = TDM 2 A 1011 = TDM 2 B 1100~1111：Reserved Note: Only I2S , LEFT and RIGHT can configure to 7+1 mode. TDM 1 A and TMD 1 B have one data pin. TDM2 A and TDM2 B have two data pins.	
1	R_NEG	0：Receiver use BCLK rising edge receive serial data and sync (only in master mode) out BAIC 1：Receiver use BCLK falling edge receive serial data and sync (only in master mode) out BAIC	RW
0	R_MASTER	Mode select. 0: slave mode; 1: Master mode.	RW

Note：

1. BAIC0/ BAIC1

PCM A /PCM B

R_SLOT: Reserved;

R_SWLR: Reserved;

R_CHANNEL: Reserved;

R_SLS: Reserved;

R_ISYNC: Reserved;

R_ASVTSU: Used;

ISS: Support 8, 16 and 32bits;

R_NEG: Used;

R_MASTER: Used.

DSP A/DSP B:

R_SLOT: Support 1 and 2 slots ;

R_SWLR: Used;

R_CHANNEL: Reserved;

R_SLS: Reserved;

R_ISYNC: Reserved;

R_ASVTSU: Used;

ISS: Support 8, 16 and 32bits;

R_NEG: Used;

R_MASTER: Used.

I2S/LEFT/RIGHT:

R_SLOT: Reserved;

R_SWLR: Used;

R_CHANNEL: Stereo;

R_SLS: Reserved;

R_ISYNC: Used;

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

R_ASVTSU: Used;

ISS: Support all bits width;

R_NEG: Used;

R_MASTER: Used.

2. BAIC2

TDM 1 A /TDM 1 B:

R_SLOT: Support all configure;

R_SWLR: Reserved ;

R_CHANNEL: Reserved;

R_SLS: Support all configure ;

R_ISYNC: Used;

R_ASVTSU: Used;

ISS: Support 8, 16, 24 and 32 bits;

R_NEG: Used;

R_MASTER: Used.

TDM 2 A /TDM 2 B:

R_SLOT: Support 8 slots only;

R_SWLR: Used;

R_CHANNEL: Must write "010";

R_SLS: Support all configure ;

R_ISYNC: Reserved;

R_ASVTSU: Used;

ISS: Support 8, 16, 24 and 32 bits;

R_NEG: Used;

R_MASTER: Used.

I2S 7+1/LEFHT Justified 7+1/RIGHT Justified 7+1:

R_SLOT: Reserved ;

R_SWLR: Used;

R_CHANNEL: Support all configure, but 1 channel;

R_SLS: Reserved ;

R_ISYNC: Used;

R_ASVTSU: Used;

ISS: Support all configure;

R_NEG: Used;

R_MASTER: Used.

3. BAIC4

PCM A /PCM B

R_SLOT: Reserved;

R_SWLR: Reserved;

R_CHANNEL: Reserved;

R_SLS: Reserved;

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

R_ISYNC: Reserved;

R_ASVTSU: Used;

ISS: Support 8, 16 and 32bits;

R_NEG: Used;

R_MASTER: Used.

12.2.5.2.3 BAIC Receiver CLK divide register (BAICRDIV) description

	BAICRDIV																**BASE + 0x008**													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								R_BCLKDIV								R_SYNL								R_SYNC_DIV							
RST	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	R_BCLKDIV	Audio BIT_CLK clock divider value . BAICDIV.BCLKDV is used to control the generating of BIT_CLK from dividing SYS_CLK. The dividing value only can be even . BAICDIV.BCLKDV depends on SYS_CLK frequency FS_{SYS_CLK}, which is selected according to external CODEC's requirement and internal PLL frequency.	R
15:8	R_SYNL	For receiver, controls the time of the BAICSYN keep to "1". The length of BAICSYN = (R_SYNL + 1) * BAICCLK cycle length. NOTE: Only PCM mode this bit is available, in I2S mode have no use.	RW
7:0	R_SYNC_DIV	For receiver, controls the sample rate of the SYNC_I/SYNC_O signal based upon the BAICCLK. PCM mode: SYNC_I or SYNC_O = BCLK/(8*(R_SYNC_DIV+1)) Note: sample rate is 8kHz,16kHz or 32kHz. I2S mode: BCLK= 2*(SYNC_I or SYNC_O)*8* (R_SYNC_DIV + 1)	RW

BAICRDIV Notes:

R_SYNL: Use for PCM, DSP and TDM mode.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.5.2.4 BAIC Receiver CLK Gate Register (BAICRCGR) description

	BAICDIV																BASE + 0x00C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											R_GFCLK	R_GTCLK	R_GSCLK	R_GHCLK	R_GCLK
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect, read as zero.	R
4	R_GFCLK	0: Have no effect to transmitter I2S 7+1 Fourth stereo CLK。 1: Keep transmitter's I2S 7+1 Fourth stereo CLK work regular	RW
3	R_GTCLK	0: Have no effect to transmitter I2S 7+1 Third stereo CLK。 1: Keep transmitter's I2S 7+1 Third channel CLK work regular	RW
2	R_GSCLK	0: Have no effect to transmitter I2S 7+1 Second stereo CLK。 1: Keep transmitter's I2S 7+1 Second stereo CLK work regular	RW
1	R_GHCLK	0: Have no effect to receiver's HCLK 1: Keep receiver's HCLK work regular	RW
0	R_GCLK	0: Have no effect to receiver's CLK 1: Keep receiver's CLK work regular	RW

Note: Use as the back door of CLK gate, only use to debug.

12.2.5.2.5 BAIC Transmitter Control Register (BAICTCTL) description

	BAICTCTL																BASE + 0x010													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															T_RST
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
4	CODE_RST	Write 1 to create reset pluse for codec Write 0 have no efferct	
3:0	Reserved	Writing has no effect, read as zero.	
0	T_RST	Write 1 to this bit reset BAIC transmitter controller2. Writing 0 to this	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		bit has no effect and this bit is always reading 0.	

12.2.5.2.6 BAIC Transmitter Configuration Register (BAICTCFG) description

	BAICTCFG																BASE + 0x014													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				T_SLOT				Reserved			T_SWLR	T_CHANNEL			Reserved	T_SLS			T_ISYNC	T_ASVTSU	OSS			Reserved		T_MODE				T_NEG	T_MASTER
RST	?	?	?	?	0	0	0	0	?	?	?	0	0	0	0	?	?	0	0	0	0	0	0	0	?	?	0	0	0	0	0	1

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:24	T_SLOT	Controls the amount of valid PCM timeslot in one BAICSYN frame. Only For TDM mode. T_SLOT: Number of slot in one frame 0000: 1 slots 0001: 2 slots 0010: Reserved 0011: 4 slots 0100: Reserved 0101: 6 slots 0110: Reserved 0111: 8 slots BAIC0, BAIC1 and BAIC4 support 1 and 2 slots. BAIC2 and BAIC3 support all the configure as list.	RW
23:21	Reserved	Writing has no effect, read as zero.	
20	T_SWLR	Transmitter Switch LR channels audio data. This bit control whether the low address data is L or R. It takes effective immediately when the bit is changed. Change this before replay started. T_SWLR: Description 0: Have no effect 1: Switch LR	RW
19:17	T_CHANNEL	Only use for Transmitter, when it work in I2S/LEFT/RIGHT Multichannel (7.1 channel) mode. These registers decide the channel number of transmitter can send serial data out to external devices during one frame synchronization. You can configure these bits as list.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td></td><td></td><td>
<table>
<tr><th>T_CHANNEL</th><th>Description</th></tr>
<tr><td>000</td><td>1 channel (1pin)</td></tr>
<tr><td>001</td><td>2 channels (1 pin)</td></tr>
<tr><td>010</td><td>4 channels (2 pins)</td></tr>
<tr><td>011</td><td>6 channels (3 pins)</td></tr>
<tr><td>100</td><td>8 channels (4 pins)</td></tr>
<tr><td>101~111</td><td>Reserved</td></tr>
</table>
In TDM2 mode, 'T_CHANNEL' must keep '010'.
</td><td></td></tr>
<tr><td>16:15</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td></td></tr>
<tr><td>14:13</td><td>T_SLS</td><td>Transmitter Slot Size can configure as list. only for TDM mode
<table>
<tr><th>T_SLS</th><th>Description</th></tr>
<tr><td>00</td><td>equal to data size(default)</td></tr>
<tr><td>01</td><td>16 BCLK cycles</td></tr>
<tr><td>10</td><td>32 BCLK cycles</td></tr>
<tr><td>11</td><td>64 BCLK cycles</td></tr>
</table>
Note: T_SLS is "00" slot size reference OSS.</td><td>RW</td></tr>
<tr><td>12</td><td>T_ISYNC</td><td>This bit use to invert SYNC. Configure this bit '1',BAIC will use invert SYNC for logic, if this bit write '0', have no effect to this block.
<table>
<tr><th>T_ISYNC</th><th>Description</th></tr>
<tr><td>0</td><td>no change (default)</td></tr>
<tr><td>1</td><td>Invert SYNC</td></tr>
</table></td><td>RW</td></tr>
<tr><td>11</td><td>T_ASVTSU</td><td>Audio Sample Value Transfer between Signed and Unsigned data format. This bit is used to control the signed ←→unsigned data transfer. If it is 1, the incoming or outgoing audio sample data will be transferred by toggle its most significant bit.
<table>
<tr><th>ASVTSU_R</th><th>Description</th></tr>
<tr><td>0</td><td>No audio sample value signed ←→unsigned transfer.</td></tr>
<tr><td>1</td><td>Do audio sample value signed ←→unsigned transfer.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>10:8</td><td>OSS</td><td>BAIC transmitter output sample size. These bits reflect output data size to memory or register. The data sizes supported: 8/12/13/14/16/18/20/24/32bits. The sample data is MSB-justified in memory/register.
<table>
<tr><th>OSS</th><th>data Size</th></tr>
<tr><td>000</td><td>8 bit</td></tr>
<tr><td>001</td><td>12 bit</td></tr>
<tr><td>010</td><td>13 bit</td></tr>
<tr><td>011</td><td>16 bit</td></tr>
</table></td><td>RW</td></tr>
</table>

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

			100	18bit		
			101	20 bit		
			110	24 bit		
			111	32 bit		
7:6	Reserved	Writing has no effect, read as zero.				R
5:2	T_MODE	BAIC data mode select 0000 = PCM Format mode A 0001 = PCM Format mode B 0010 = DSP Format mode A 0011 = DSP Format mode B 0100 = I2S justified mode 0101 = LEFT justified mode 0110 = RIGHT justified mode 0111：Reserved 1000 = TDM 1 A 1001 = TDM 1 B 1010 = TDM 2 A 1011 = TDM 2 B 1100~1111：Reserved Note: Only I2S , LEFT and RIGHT have 7+1 mode. TDM 1 A and TMD 1 B have one data pin. TDM2 A and TDM2 B have two data pins.				RW
1	T_NEG	0：Transmitter use BCLK falling edge send serial data and sync (only in master mode) out BAIC 1：Transmitter use BCLK rising edge send serial data and sync (only in master mode) out BAIC				RW
0	T_MASTER	Mode select. 0: slave mode; 1: Master mode.				RW

Note:BAIC0/BAIC1

PCM A /PCM B

T_SLOT: Reserved;

T_SWLR: Reserved;

T_CHANNEL: Reserved;

T_SLS: Reserved;

T_ISYNC: Reserved;

T_ASVTSU: Used;

OSS: Support 8, 16 and 32bits;

T_NEG: Used;

T_MASTER: Used.

DSP A/DSP B:

T_SLOT: Support 1 and 2 slots ;

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

T_SWLR: Used;

T_CHANNEL: Reserved;

T_SLS: Reserved;

T_ISYNC: Reserved;

T_ASVTSU: Used;

OSS: Support 8, 16 and 32bits;

T_NEG: Used;

T_MASTER: Used.

I2S/LEFT/RIGHT:

T_SLOT: Reserved;

T_SWLR: Used;

T_CHANNEL: Mono or Stereo(1 or 2);

T_SLS: Reserved;

T_ISYNC: Used;

T_ASVTSU: Used;

OSS: Support all bits width;

T_NEG: Used;

T_MASTER: Used.

1. BAIC3

TDM 1 A /TDM 1 B:

T_SLOT: Support all configure;

T_SWLR: Used;

T_CHANNEL: Reserved;

T_SLS: Support all configure ;

T_ISYNC: Reserved;

T_ASVTSU: Used;

OSS: Support 8, 16, 24 and 32 bits;

T_NEG: Used;

T_MASTER: Used.

TDM 2 A /TDM 2 B:

T_SLOT: Support 8 slots only;

T_SWLR: Used;

T_CHANNEL: Must write "010";

T_SLS: Support all configure ;

T_ISYNC: Reserved;

T_ASVTSU: Used;

OSS: Support 8, 16, 24 and 32 bits;

T_NEG: Used;

T_MASTER: Used.

I2S 7+1/LEFHT Justified 7+1/RIGHT Justified 7+1:

T_SLOT: Reserved ;

T_SWLR: Used;

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

T_CHANNEL: Support all configure;

T_SLS: Reserved ;

T_ISYNC: Used;

T_ASVTSU: Used;

OSS: Support all configure;

T_NEG: Used;

T_MASTER: Used.

2. BAIC4

PCM A /PCM B

T_SLOT: Reserved;

T_SWLR: Reserved;

T_CHANNEL: Reserved;

T_SLS: Reserved;

T_ISYNC: Reserved;

T_ASVTSU: Used;

OSS: Support 8, 16 and 32bits;

T_NEG: Used;

T_MASTER: Used.

12.2.5.2.7 BAIC Transmitter CLK divide register (BAICTDIV）description

	BAICTDIV																**BASE + 0x018**															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								T_BCLKDIV								T_SYNL								T_SYNC_DIV							
RST	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	T_BCLKDIV	Audio BIT_CLK clock divider value . BAICDIV.BCLKDV is used to control the generating of BIT_CLK from dividing SYS_CLK. The dividing value only can be even. BAICDIV.BCLKDV depends on SYS_CLK frequency FS_{SYS_CLK}, which is selected according to external CODEC's requirement and internal PLL frequency.	R
15:8	T_SYNL	For transmitter, controls the time of the BAICSYN keep to "1". The length of BAICSYN = (T_SYNL + 1) * BAICCLK cycle. NOTE: PCM, DSP and TDM is available , for I2S, LEFT and RIGHT justified mode have no use.	RW
7:0	T_SYNC_DI	For transmitter, controls the sample rate of the	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	V	SYNC_I/SYNC_O signal based upon the BAICCLK. PCM mode: SYNC_I or SYNC_O = BCLK/(8*(T_SYNC_DIV+1)) Note: sample rate is 8kHz,16kHz or 32kHz. I2S mode: BCLK= 2*(SYNC_I or SYNC_O)*8* (T_SYNC_DIV + 1)	

BAICTDIV Notes:

T_SYNL: Use for PCM, DSP and TDM mode.

12.2.5.2.8 BAIC Transmitter CLK Gate Register (BAICTCGR) description

	BAICTCGR																**BASE + 0x01C**															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											T_GFCLK	T_GTCLK	T_GSCLK	T_GHCLK	T_GCLK
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect, read as zero.	R
4	T_GFCLK	0: Have no effect to transmitter I2S 7+1 Fourth stereo CLK。 1: Keep transmitter's I2S 7+1 Fourth stereo CLK work regular	RW
3	T_GTCLK	0: Have no effect to transmitter I2S 7+1 Third stereo CLK。 1: Keep transmitter's I2S 7+1 Third channel CLK work regular	RW
2	T_GSCLK	0: Have no effect to transmitter I2S 7+1 Second stereo CLK。 1: Keep transmitter's I2S 7+1 Second stereo CLK work regular	RW
1	T_GHCLK	0: Have no effect to transmitter HCLK 1: Keep transmitter HCLK work regular	RW
0	T_GCLK	0: Have no effect to transmitter 's CLK 1: Keep transmitter's CLK work regular	RW

Note: Use as the back door of CLK gate, only use to debug.

12.2.5.2.9 BAIC Top Level Configure Register (BAICTLCR) description

	BAICTCGR																**BASE + 0x020**															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved																												ICDC	CLK_SPLIT_EN
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	CLK_SPLIT_EN	0: Transmitter and Receiver clock separate disable 1: Transmitter and Receiver clock separate enable	RW

Note: BAIC0,BAIC2 and BAIC3, register BAICTLCR is reserved.

12.2.5.2.10 BAIC Common Control Register (BAICCCR) description

	BAICTCGR																**BASE + 0x024**													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												TEN	REN	Reserved	
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	?	?

Bits	Name	Description	RW
31:4	Reserved	Writing has no effect, read as zero.	R
3	TEN	Control transmitter access TEN: Description 0: BAIC transmitter is Disabled. 1: BAIC transmitter is Enabled.	RW
2	REN	Control receiver access REN: Description 0: BAIC receiver is Disabled. 1: BAIC receiver is Enabled.	RW
1:0	Reserved	Writing has no effect, read as zero.	R

12.2.5.3 BAIC Operation

12.2.5.3.1 Audio Replay

Outgoing audio sample data (from BAIC to CODEC or other devices) is put data to BAIC transmit data bus FIFO from memory via DMA. Then BAIC takes the data from FIFO, serializes it, and sends it over the serial wire BAIC_DATA_O to an external CODEC or over an internal wire to an internal

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

CODEC.

Here is the audio replay flow

1. Configure the CODEC as needed
2. Configure master or slaver by BAICTCFG.T_MASTER
3. Configure BAICTDIV generate BCLK and BAIC_SYNC
   (1) Write BAICTDIV.T_BCLKDIV to generate BCLK from MCLK
   (2) Write BAICTDIV.T_SYNC_DIV to generate BAIC_SYNC from BCLK
4. Configure sample size by BAICTCFG.OSS
5. Configure sample channels
   (1) BAICTCFG.T_CHANNEL configure pins number
   (2) BAICTCFG.T_SLOT decide time slot
6. Configure protocol mode by BAICTCFG.T_MODE
7. Configure other features: BAICTCFG.T_SWLR, BAICTCFG.ISYNC, BAICTCFG.T_ASVTSU and so on.
8. Write 1 to BAICCCR.TEN, enable BAIC

12.2.5.3.2 Audio Record

Incoming audio sample data (from CODEC to BAIC) is received from BAIC_DATA_IN (for an external CODEC) serially and converted to parallel word and send to data DMA's FIFO. Then the data can be taken from the FIFO to processor via load instruction or to memory via DMA.

Here is the audio record flow

1. Configure the CODEC as needed
2. Configure whether to use clock separate by BAICTLCR.CLK_SPLIT_EN.

if BAICTLCR.CLK_SPLIT_EN be writed 1

3. Configure master or slaver by BAICRCFG.T_MASTER
4. Configure BAICRDIV generate BCLK and BAIC_SYNC
   (3) Write BAICRDIV.T_BCLKDIV to generate BCLK from MCLK
   (4) Write BAICRDIV.T_SYNC_DIV to generate BAIC_SYNC from BCLK
5. Configure sample size by BAICRCFG.OSS
6. Configure sample channels
   (3) BAICRCFG.T_CHANNEL configure pins number
   (4) BAICRCFG.T_SLOT decide time slot
7. Configure protocol mode by BAICRCFG.T_MODE
8. Configure other features: BAICRCFG.T_SWLR, BAICRCFG.ISYNC, BAICRCFG.T_ASVTSU and so on.

if BAICTLCR.CLK_SPLIT_EN be writed 0, Step 3 to 8 configure BAICTCFG, BAICTDIV

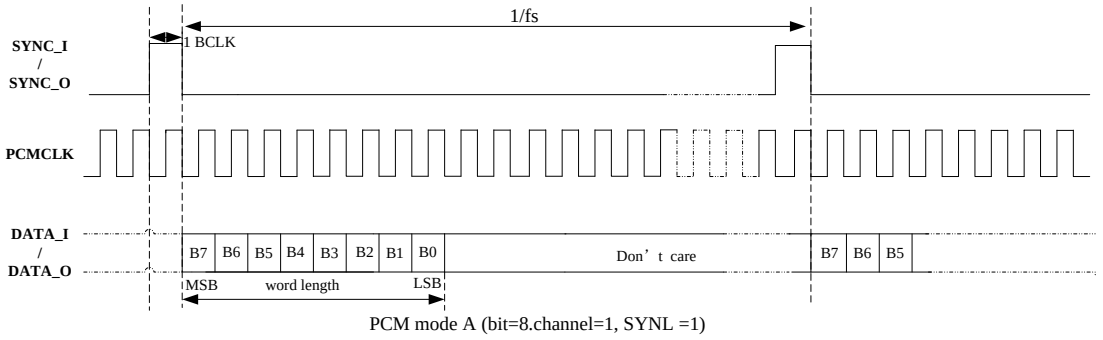
9. Write 1 to BAICCCR.REN, enable BAIC

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.5.4 BAIC Protocol

PCM data format have four port signals: clock PCMCLK, serial data BAIC_DATA_O, serial data BAIC_DATA_I and frame synchronization BAIC_SYNC. PCM format include PCM mode A, PCM mode B, DSP mode A，and DSP mode-B

12.2.5.4.1 PCM and DSP protocol



PCM mode A (bit=8.channel=1, SYNL =1)

Figure 12-2 PCM mode A format（8bit，falling edge，sync length one cycle）

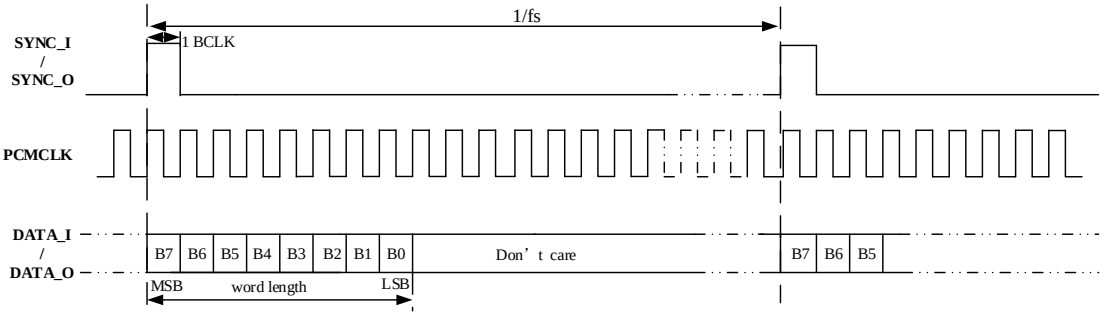


Figure 12-3 PCM mode B format（8bit，falling edge，sync length one cycle）

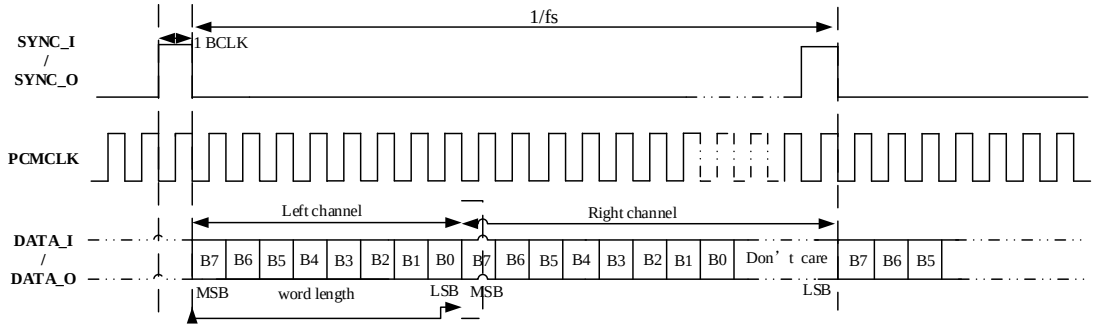


Figure 12-4 DSP mode A format（8bit，falling edge，sync length one cycle）

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

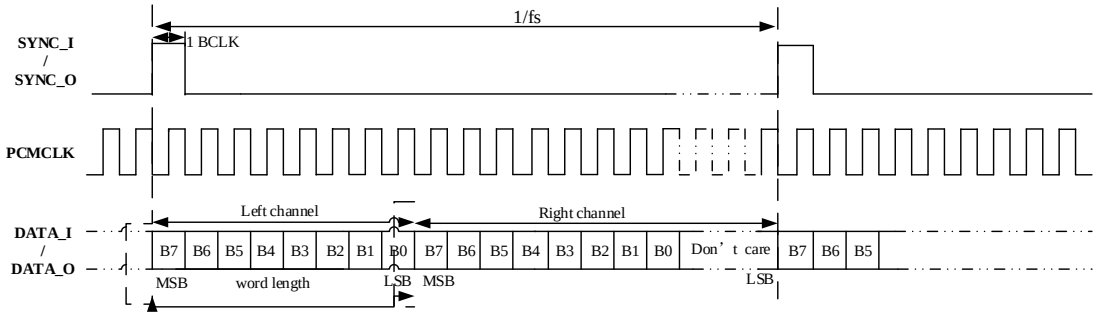


Figure 12-5 DSP mode B format（8bit，falling edge，sync length one cycle）

12.2.5.4.2 I2S and Justified protocol

I2S and Justified formal inclue I2S normal mode, I2S Left justified mode and I2S right justified mode Normal I2S and Justified formal have stable two data signal: serial data BAIC_DATA_O, serial data BAIC_DATA_I

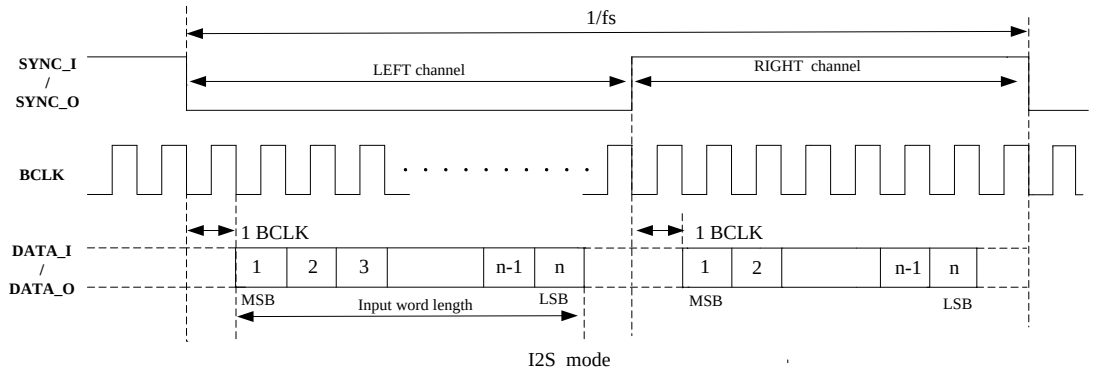


Figure 12-6 I2S normal format（falling edge）

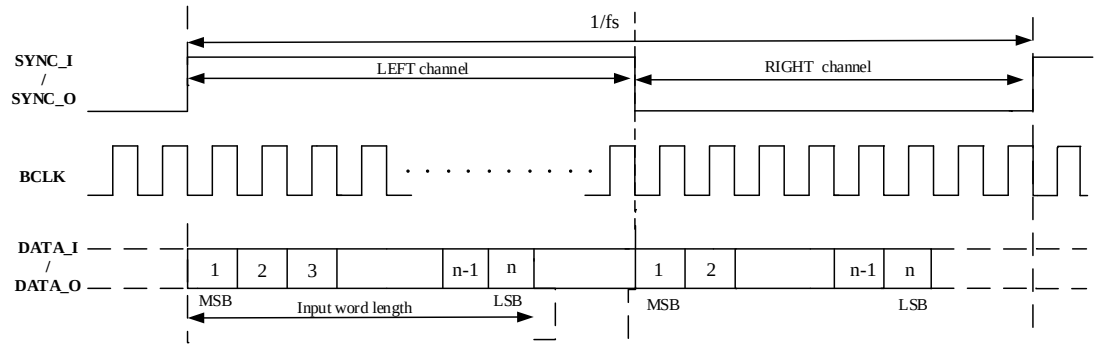


Figure 12-7 I2S LEFT-Justied format（falling edge）

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

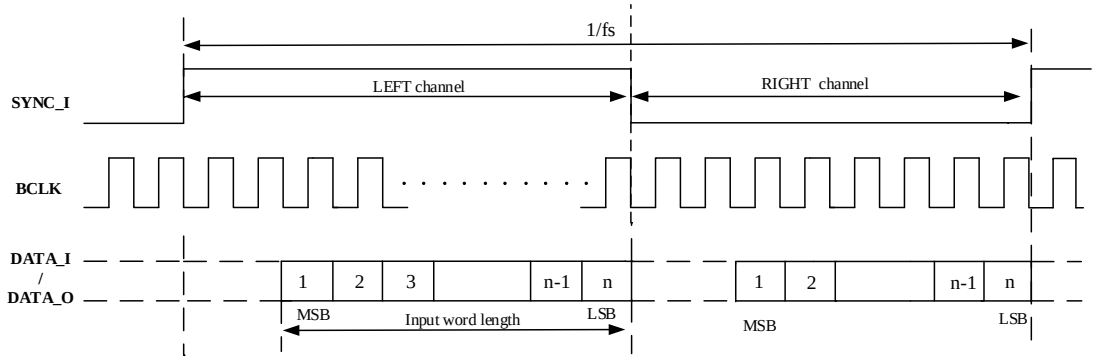
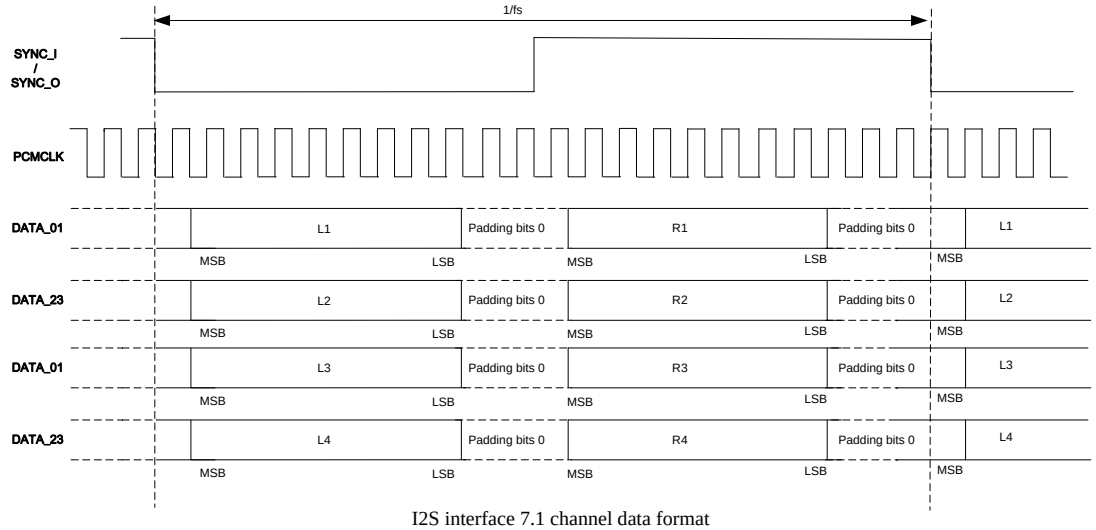


Figure 12-8 I2S RIGHT-Justied format（falling edge）

Multi-channel I2S and Justified formal have configurable data signal:



I2S interface 7.1 channel data format

Figure 12-9 I2S Mulit-channel-normal- format（8channel,falling edge）

12.2.5.4.3 TDM and Justified protocol

TDM format include TDM1_A model, TDM1_B model, TDM2_A model and TDM2_B model TDM1_A model and TDM1_B model have stable two data signal: BAIC_DATA_O, BAIC_DATA_I. TDM2_A model and TDM2_B model have stable four data signal:BAIC_DATA_O1, BAIC_DATA_O2,BAIC_DATA_I1, BAIC_DATA_i2. TDM1_A model and TDM2_A model use normal data alignment. TDM1_B model and TDM2_B model use left Justified data alignment

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

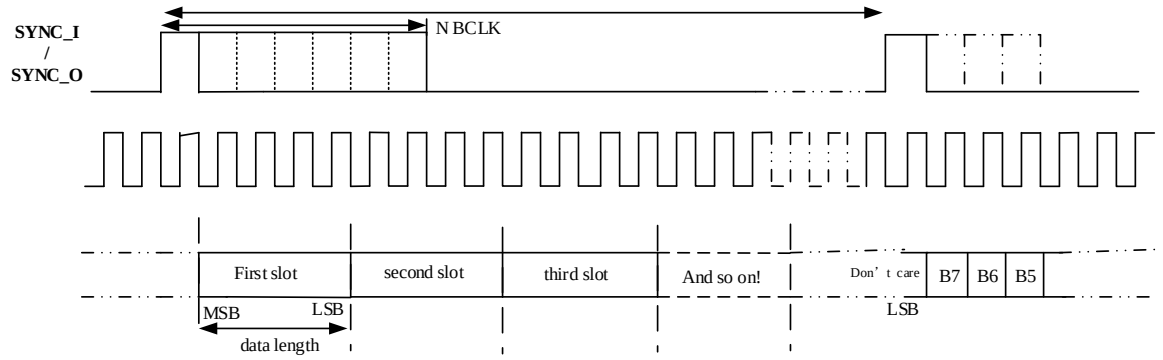


Figure 12-10 TDM1- format（8channel,falling edge）

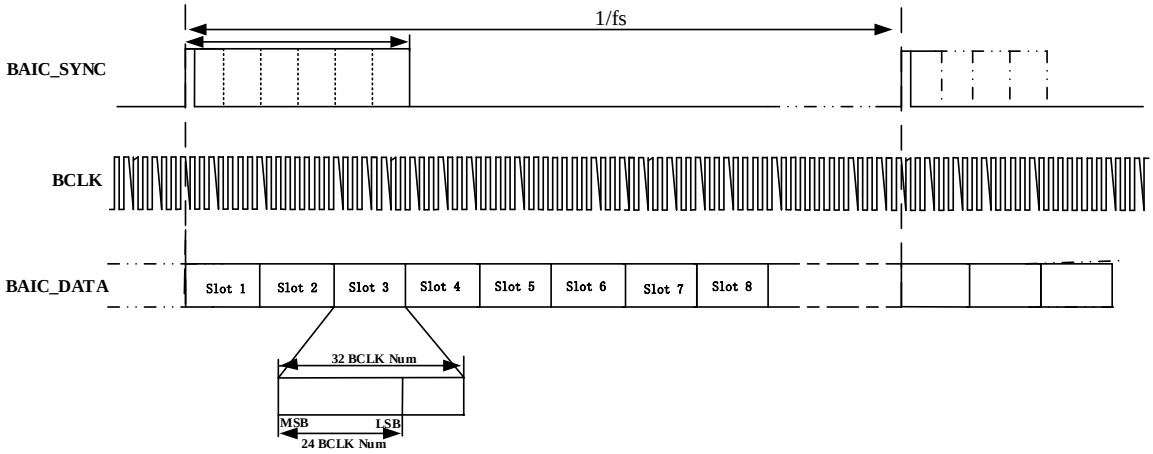
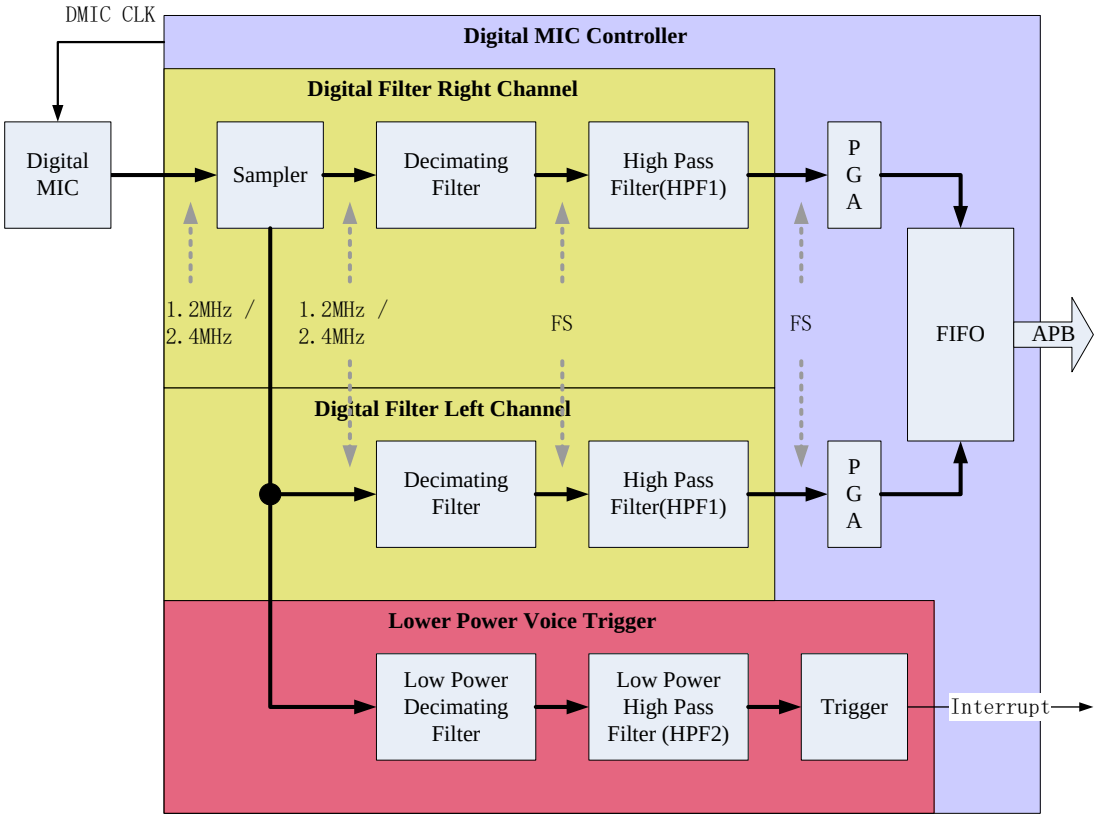


Figure 12-11 TDM2- format（8channel,falling edge）

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.6 DMIC

12.2.6.1 Block Diagram



12.2.6.2 Register Descriptions

Name	Base	Description
A_DMIC	134da000	Base address of DMIC.

Table 12-1 DMIC Controller Registers Description

Name	Description	Address offset	Access Size
DMIC_CR0	DMIC Control register 0	0x000	32
DMIC_GCR	DMIC Gain Control Register	0x004	32
DMIC_IER	DMIC Interrupt Mask Register	0x008	32
DMIC_ICR	DMIC Interrupt Control Register	0x00C	32
TRI_TCR	DMIC Trigger Control Register	0x010	32
THR_L1	DMIC Trigger 1 Low Threshold	0x014	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

THR_H2	DMIC Trigger 2 High Threshold	**0x018**	32
THR_L2	DMIC Trigger 2 Low Threshold	**0x01c**	32
TRI_M_MAX	DMIC Trigger number M Max value	**0x020**	32
TRI_N_MAX	DMIC Trigger number N Max value	**0x024**	32
THR_L3	DMIC Trigger 3 Low Threshold	**0x028**	32
THR_TM	DMIC voice trigger timer	**0x02c**	32
FFGDIS	DMIC clock disable Control register	**0x030**	32
SFGDIS	DMIC clock disable Control register	**0x034**	32
TFGDIS	DMIC clock disable Control register	**0x038**	32
CGDIS	DMIC clock disable Control Register	**0x03c**	32
VTSR	DMIC Voice Trigger status	**0x040**	32

12.2.6.3 Register Description

12.2.6.3.1 DMIC Control register 0 (DMIC_CR0)

	DMIC_CR0																BASE + 0x000													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RESET	RESET_TRI	Reserved							HPF2_EN	LPF_EN	HPF1_EN	CHNUM				Reserved		OSS		SW_LR	Reserved		SR			Reserved					DMIC_EN
RST	0	0	?	?	?	?	?	?	?	0	0	0	0	0	0	0	?	?	0	0	0	?	?	0	0	0	?	?	?	?	?	0

Bits	Name	Description	RW
31	RESET	If set this bit to '1' will reset all DMIC (data interface \ trigger block but without software configuration registers).	RWS
30:23	Reserved	Writes to these bits have no effect and always read as 0.	R
22	HPF2_EN	HPF2(High pass filter) enable. Set this bit to '1' will enable the function.	RW
21	LPF_EN	LPF(Low pass filter) enable. Set this bit to '1' will enable the function.	RW
20	HPF1_EN	HPF1(High pass filter) enable. Set this bit to '1' will enable the function.	RW
19:16	CHNUM	DMIC data interface channel number. 0000: Mono 0001: Stereo 0011: 4 Channels 0101: 6 Channels 0111: 8 Channels	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1001: 10 Channels 1011: 12 Channels Others: Reserved	
15:14	Reserved	Writes to these bits have no effect and always read as 0.	R
13:12	OSS	DMIC controller Output Sample Size 00:16 bits 01:24 bits others: Reserved	RW
11	SW_LR	Switch left and right channel when data input. Set this bit to '1' will enable the function.	RW
10:9	Reserved	Writes to these bits have no effect and always read as 0.	R
8:6	SR	DMIC interface output sample rate: 000: 8k 001: 16k 010: 48k 011: 96k others: Reserved	RW
5:1	Reserved	Writes to these bits have no effect and always read as 0.	R
0	DMIC_EN	DMIC enable. Set this bit to '1' will enable the function.	RW

12.2.6.3.2 DMIC Gain Control Register (DMIC_GCR)

	DMIC_GCR																BASE + 0x004													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DGAIN				
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writes to these bits have no effect and always read as 0.	R
4:0	DGAIN	Digital gain register. The gain of PGA equal to DGAIN * 3 dB.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.6.3.3 DMIC Interrupt Enable Register (DMIC_IER)

	DMIC_IMR																BASE + 0x008																	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											TRI_FAIL_INT_EN	Reserved			WAKEUP_INT_EN
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	?	?	?	0

Bits	Name	Description	RW
31:5	Reserved	Writes to these bits have no effect and always read as 0.	R
4	TRI_FAIL_INT_EN	Enable Trigger fail Interrupt. 0: Disable; 1:Enable	RW
3:1	Reserved	Writes to these bits have no effect and always read as 0.	R
0	WAKEUP_INT_EN	Enable Wake up Interrupt. 0: Disable; 1:Enable	RW

12.2.6.3.4 DMIC Interrupt Control Register (DMIC_ICR)

	DMIC_ICR																BASE + 0x00c																	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											TRI_FAIL_FLAG	Reserved			WAKEUP_FLAG
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	?	?	?	0

Bits	Name	Description	RW
31:5	Reserved	Writes to these bits have no effect and always read as 0.	R
4	TRI_FAIL_FLAG	When this bit is '1' indicate that trigger fail status was generate. Write this bit '1' will clear it.	RWC
3:1	Reserved	Writes to these bits have no effect and always read as 0.	R
0	WAKEUP_FLAG	When this bit is '1' indicate that voice trigger was triggered. Write this bit '1' will clear it.	RWC

12.2.6.3.5 DMIC Trigger Control register (DMIC_TCR)

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	DMIC_TCR																													BASE + 0x010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												TRI2_MODE				Reserved				TRI1_CLR	TRI2_CLR	TRI3_CLR	Reserved		TRI3_EN	TRI2_EN	TRI1_EN	Reserved			TRI_RESET
RST	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	?	?	?	?	0	0	0	?	?	0	0	0	?	?	?	0

Bits	Name	Description	RW
31:20	Reserved	Writes to these bits have no effect and always read as 0.	R
19:16	TRI2_MODE	Trigger 2 mode: 0. If the signal great than the THR_L level, trigger generate. 1. If the signal peak is great than THR_L and less than THR_H, trigger generate. 2. If the signal great than the THR_L level and continue num N times, trigger generate. 3. If the signal peak is great than THR_L and less than THR_H and continue num N times, trigger generate. 4. Same as mode 2, but use THR_L and THR_H to Schmitt mode. 5~15. Reserved. Note: Trigger 2 work mode can configure by these bits。Trigger 1 and Trigger 3 always work in mode 0.	RW
15:12	Reserved	Writes to these bits have no effect and always read as 0.	
11	TRI1_CLR	If write this bit '1' will clear trigger.	RWC
10	TRI2_CLR	If write this bit '1' will clear trigger.	RWC
9	TRI3_CLR	If write this bit '1' will clear trigger.	RWC
8:7	Reserved	Writes to these bits have no effect and always read as 0.	R
6	TRI3_EN	Trigger 3 enable. Set this bit to '1' will enable the function. Note: This bit only use in the condition "DMIC_EN=1".	RW
5	TRI2_EN	Trigger 2 enable. Set this bit to '1' will enable the function. Note: This bit only use in the condition "DMIC_EN=1".	RW
4	TRI1_EN	Trigger 1 enable. Set this bit to '1' will enable the function. Note: This bit only use in the condition "DMIC_EN=1".	RW
3:1	Reserved	Writes to these bits have no effect and always read as 0.	R
0	TRI_RESET	If set this bit to '1' will reset DMIC TRI block. (Without software configuration registers).	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.6.3.6 DMIC Trigger 1 Low Threshold (DMIC_THR_L1)

	DMIC_THR_L1																BASE + 0x014															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								THR_L1																							
RST	?	?	?	?	?	?	?	?	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writes to these bits have no effect and always read as 0.	R
23:0	THR_L1	DMIC Trigger 1 Low Threshold.	RW

Note: THR_L1 use as signed.

12.2.6.3.7 DMIC Trigger 2 High Threshold (DMIC_THR_H2)

	DMIC_THR_H2																BASE + 0x018															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								THR_H2																							
RST	?	?	?	?	?	?	?	?	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writes to these bits have no effect and always read as 0.	R
23:0	THR_H2	DMIC Trigger 2 High Threshold.	RW

Note: THR_H2 use as signed.

12.2.6.3.8 DMIC Trigger 2 Low Threshold (DMIC_THR_L2)

	DMIC_THR_L2																BASE + 0x01c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								THR_L2																							
RST	?	?	?	?	?	?	?	?	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:24	Reserved	Writes to these bits have no effect and always read as 0.	R
23:0	THR_L2	DMIC Trigger 2 Low Threshold.	RW

Note: THR_L2 use as signed.

12.2.6.3.9 DMIC Trigger 2 number M Max value (TRI_M_MAX)

	TRI_M_MAX																													BASE + 0x020	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								M_MAX																							
RST	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writes to these bits have no effect and always read as 0.	R
23:0	M_MAX	The num m max value used for the **time out.** After M cycle, if the trigger have not generate and the generate times of trigger less than N_MAX, the counter of N will be clear. The time of M one cycle is 1 / 12MHz.	RW

12.2.6.3.10 DMIC Trigger 2 number N Max value (TRI_N_MAX)

	TRI_N_MAX																													BASE + 0x024	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																N2_MAX															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writes to these bits have no effect and always read as 0.	R
15:0	N_MAX	The number n max value used for the time. If trigger generated N times, Interrupt will be generate.	RW

12.2.6.3.11 DMIC Trigger 3 Low Threshold (DMIC_THR_L3)

	DMIC_THR_L3																													BASE + 0x028	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								THR_L3																							
RST	?	?	?	?	?	?	?	?	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:24	Reserved	Writes to these bits have no effect and always read as 0.	R
23:0	THR_L3	DMIC Trigger Low Threshold.	RW

Note: THR_L3 use as signed.

12.2.6.3.12 DMIC Trigger 3 Timer Register(DMIC_TRI_TM)

	DMIC_TRI_TM1																BASE + 0x02c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								TM_LEN																							
RST	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Name	Description	RW
31:22	Reserved	Writes to these bits have no effect and always read as 0.	R
21:0	TM_LEN	DMIC Trigger 3 timer length. Cycle length of the counter is sample time.	RW

12.2.6.3.13 DMIC First Filter clock Gate Disable Register (DMIC_FFGDIS) **(Internal use !)**

	DMIC_FFGDIS																BASE + 0x030															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH3_LPF_GDIS	CH3_HPF2_GDIS	CH3_HPF1_GDIS	CH3_SRC3_GDIS	CH3_SRC2_GDIS	CH3_SRC1_GDIS	CH3_FIR2_GDIS	CH3_FIR3_GDIS	CH2_LPF_GDIS	CH2_HPF2_GDIS	CH2_HPF1_GDIS	CH2_SRC3_GDIS	CH2_SRC2_GDIS	CH2_SRC1_GDIS	CH2_FIR2_GDIS	CH2_FIR3_GDIS	CH1_LPF_GDIS	CH1_HPF2_GDIS	CH1_HPF1_GDIS	CH1_SRC3_GDIS	CH1_SRC2_GDIS	CH1_SRC1_GDIS	CH1_FIR2_GDIS	CH1_FIR3_GDIS	CH0_LPF_GDIS	CH0_HPF2_GDIS	CH0_HPF1_GDIS	CH0_SRC3_GDIS	CH0_SRC2_GDIS	CH0_SRC1_GDIS	CH0_FIR2_GDIS	CH0_FIR3_GDIS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	CH3_LPF_GDIS	LPF of fourth channel clock gate disable.	RW
30	CH3_HPF2_GDIS	HPF2 of fourth channel clock gate disable.	RW
29	CH3_HPF1_GDIS	HPF1 of fourth channel clock gate disable.	RW
28	CH3_SRC3_GDIS	SRC3 of fourth channel clock gate disable.	RW
27	CH3_SRC2_GDIS	SRC2 of fourth channel clock gate disable.	RW
26	CH3_SRC1_GDIS	SRC1 of fourth channel clock gate disable.	RW
25	CH3_FIR2_GDIS	FIR2 of fourth channel clock gate disable.	RW
24	CH3_FIR3_GDIS	FIR3 of fourth channel clock gate disable.	RW
23	CH2_LPF_GDIS	LPF of third channel clock gate disable.	RW
22	CH2_HPF2_GDI	HPF2 of third channel clock gate disable.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	S		
21	CH2_HPF1_GDIS	HPF1 of third channel clock gate disable.	RW
20	CH2_SRC3_GDIS	SRC3 of third channel clock gate disable.	RW
19	CH2_SRC2_GDIS	SRC2 of third channel clock gate disable.	RW
18	CH2_SRC1_GDIS	SRC1 of third channel clock gate disable.	RW
17	CH2_FIR2_GDIS	FIR2 of third channel clock gate disable.	RW
16	CH2_FIR3_GDIS	FIR3 of third channel clock gate disable.	RW
15	CH1_LPF_CGDIS	LPF of second channel clock gate disable.	RW
14	CH1_HPF2_GDIS	HPF2 of second channel clock gate disable.	RW
13	CH1_HPF1_GDIS	HPF1 of second channel clock gate disable.	RW
12	CH1_SRC3_GDIS	SRC3 of second channel clock gate disable.	RW
11	CH1_SRC2_GDIS	SRC2 of second channel clock gate disable.	RW
10	CH1_SRC1_GDIS	SRC1 of second channel clock gate disable.	RW
9	CH1_FIR2_GDIS	FIR2 of second channel clock gate disable.	RW
8	CH1_FIR3_GDIS	FIR3 of second channel clock gate disable.	RW
7	CH0_LPF_GDIS	LPF of first channel clock gate disable.	RW
6	CH0_HPF2_GDIS	HPF2 of first channel clock gate disable.	RW
5	CH0_HPF1_GDIS	HPF1 of first channel clock gate disable.	RW
4	CH0_SRC3_GDIS	SRC3 of first channel clock gate disable.	RW
3	CH0_SRC2_GDIS	SRC2 of first channel clock gate disable.	RW
2	CH0_SRC1_GDIS	SRC1 of first channel clock gate disable.	RW
1	CH0_FIR2_GDIS	FIR2 of first channel clock gate disable.	RW
0	CH0_FIR3_GDIS	FIR3 of first channel clock gate disable.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.6.3.14 DMIC Second Filter clock Gate Disable Register (DMIC_SFGDIS) (Internal use !)

	DMIC_SFGDIS																BASE + 0x034													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH7_LPF_GDIS	CH7_HPF2_GDIS	CH7_HPF1_GDIS	CH7_SRC3_GDIS	CH7_SRC2_GDIS	CH7_SRC1_GDIS	CH7_FIR2_GDIS	CH7_FIR3_GDIS	CH6_LPF_GDIS	CH6_HPF2_GDIS	CH6_HPF1_GDIS	CH6_SRC3_GDIS	CH6_SRC2_GDIS	CH6_SRC1_GDIS	CH6_FIR2_GDIS	CH6_FIR3_GDIS	CH5_LPF_GDIS	CH5_HPF2_GDIS	CH5_HPF1_GDIS	CH5_SRC3_GDIS	CH5_SRC2_GDIS	CH5_SRC1_GDIS	CH5_FIR2_GDIS	CH5_FIR3_GDIS	CH4_LPF_GDIS	CH4_HPF2_GDIS	CH4_HPF1_GDIS	CH4_SRC3_GDIS	CH4_SRC2_GDIS	CH4_SRC1_GDIS	CH4_FIR2_GDIS	CH4_FIR3_GDIS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	CH7_LPF_GDIS	LPF of fourth channel clock gate disable.	RW
30	CH7_HPF2_GDIS	HPF2 of fourth channel clock gate disable.	RW
29	CH7_HPF1_GDIS	HPF1 of fourth channel clock gate disable.	RW
28	CH7_SRC3_GDIS	SRC3 of fourth channel clock gate disable.	RW
27	CH7_SRC2_GDIS	SRC2 of fourth channel clock gate disable.	RW
26	CH7_SRC1_GDIS	SRC1 of fourth channel clock gate disable.	RW
25	CH7_FIR2_GDIS	FIR2 of fourth channel clock gate disable.	RW
24	CH7_FIR3_GDIS	FIR3 of fourth channel clock gate disable.	RW
23	CH6_LPF_GDIS	LPF of third channel clock gate disable.	RW
22	CH6_HPF2_GDIS	HPF2 of third channel clock gate disable.	RW
21	CH6_HPF1_GDIS	HPF1 of third channel clock gate disable.	RW
20	CH6_SRC3_GDIS	SRC3 of third channel clock gate disable.	RW
19	CH6_SRC2_GDIS	SRC2 of third channel clock gate disable.	RW
18	CH6_SRC1_GDIS	SRC1 of third channel clock gate disable.	RW
17	CH6_FIR2_GDIS	FIR2 of third channel clock gate disable.	RW
16	CH6_FIR3_GDIS	FIR3 of third channel clock gate disable.	RW
15	CH5_LPF_CGDIS	LPF of second channel clock gate disable.	RW
14	CH5_HPF2_GDIS	HPF2 of second channel clock gate disable.	RW
13	CH5_HPF1_GDIS	HPF1 of second channel clock gate disable.	RW
12	CH5_SRC3_GDIS	SRC3 of second channel clock gate disable.	RW
11	CH5_SRC2_GDIS	SRC2 of second channel clock gate disable.	RW
10	CH5_SRC1_GDIS	SRC1 of second channel clock gate disable.	RW
9	CH5_FIR2_GDIS	FIR2 of second channel clock gate disable.	RW
8	CH5_FIR3_GDIS	FIR3 of second channel clock gate disable.	RW
7	CH4_LPF_GDIS	LPF of first channel clock gate disable.	RW
6	CH4_HPF2_GDIS	HPF2 of first channel clock gate disable.	RW
5	CH4_HPF1_GDIS	HPF1 of first channel clock gate disable.	RW
4	CH4_SRC3_GDIS	SRC3 of first channel clock gate disable.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3	CH4_SRC2_GDIS	SRC2 of first channel clock gate disable.	RW
2	CH4_SRC1_GDIS	SRC1 of first channel clock gate disable.	RW
1	CH4_FIR2_GDIS	FIR2 of first channel clock gate disable.	RW
0	CH4_FIR3_GDIS	FIR3 of first channel clock gate disable.	RW

12.2.6.3.15 DMIC Third Filter clock Gate Disable Register (DMIC_TFGDIS) (Internal use !)

	DMIC_SFGDIS																BASE + 0x038													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH11_LPF_GDIS	CH11_HPF2_GDIS	CH11_HPF1_GDIS	CH11_SRC3_GDIS	CH11_SRC2_GDIS	CH11_SRC1_GDIS	CH11_FIR2_GDIS	CH11_FIR3_GDIS	CH10_LPF_GDIS	CH10_HPF2_GDIS	CH10_HPF1_GDIS	CH10_SRC3_GDIS	CH10_SRC2_GDIS	CH10_SRC1_GDIS	CH10_FIR2_GDIS	CH10_FIR3_GDIS	CH9_LPF_GDIS	CH9_HPF2_GDIS	CH9_HPF1_GDIS	CH9_SRC3_GDIS	CH9_SRC2_GDIS	CH9_SRC1_GDIS	CH9_FIR2_GDIS	CH9_FIR3_GDIS	CH8_LPF_GDIS	CH8_HPF2_GDIS	CH8_HPF1_GDIS	CH8_SRC3_GDIS	CH8_SRC2_GDIS	CH8_SRC1_GDIS	CH8_FIR2_GDIS	CH8_FIR3_GDIS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	CH11_LPF_GDIS	LPF of fourth channel clock gate disable.	RW
30	CH11_HPF2_GDIS	HPF2 of fourth channel clock gate disable.	RW
29	CH11_HPF1_GDIS	HPF1 of fourth channel clock gate disable.	RW
28	CH11_SRC3_GDIS	SRC3 of fourth channel clock gate disable.	RW
27	CH11_SRC2_GDIS	SRC2 of fourth channel clock gate disable.	RW
26	CH11_SRC1_GDIS	SRC1 of fourth channel clock gate disable.	RW
25	CH11_FIR2_GDIS	FIR2 of fourth channel clock gate disable.	RW
24	CH11_FIR3_GDIS	FIR3 of fourth channel clock gate disable.	RW
23	CH10_LPF_GDIS	LPF of third channel clock gate disable.	RW
22	CH10_HPF2_GDIS	HPF2 of third channel clock gate disable.	RW
21	CH10_HPF1_GDIS	HPF1 of third channel clock gate disable.	RW
20	CH10_SRC3_GDIS	SRC3 of third channel clock gate disable.	RW
19	CH10_SRC2_GDIS	SRC2 of third channel clock gate disable.	RW
18	CH10_SRC1_GDIS	SRC1 of third channel clock gate disable.	RW
17	CH10_FIR2_GDIS	FIR2 of third channel clock gate disable.	RW
16	CH10_FIR3_GDIS	FIR3 of third channel clock gate disable.	RW
15	CH9_LPF_CGDIS	LPF of second channel clock gate disable.	RW
14	CH9_HPF2_GDIS	HPF2 of second channel clock gate disable.	RW
13	CH9_HPF1_GDIS	HPF1 of second channel clock gate disable.	RW
12	CH9_SRC3_GDIS	SRC3 of second channel clock gate disable.	RW
11	CH9_SRC2_GDIS	SRC2 of second channel clock gate disable.	RW
10	CH9_SRC1_GDIS	SRC1 of second channel clock gate disable.	RW
9	CH9_FIR2_GDIS	FIR2 of second channel clock gate disable.	RW
8	CH9_FIR3_GDIS	FIR3 of second channel clock gate disable.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

7	CH8_LPF_GDIS	LPF of first channel clock gate disable.	RW
6	CH8_HPF2_GDIS	HPF2 of first channel clock gate disable.	RW
5	CH8_HPF1_GDIS	HPF1 of first channel clock gate disable.	RW
4	CH8_SRC3_GDIS	SRC3 of first channel clock gate disable.	RW
3	CH8_SRC2_GDIS	SRC2 of first channel clock gate disable.	RW
2	CH8_SRC1_GDIS	SRC1 of first channel clock gate disable.	RW
1	CH8_FIR2_GDIS	FIR2 of first channel clock gate disable.	RW
0	CH8_FIR3_GDIS	FIR3 of first channel clock gate disable.	RW

12.2.6.3.16 DMIC Trigger Clock Gate Disable Register (DMIC_CGDIS) (Internal use !)

	DMIC_CGDIS																BASE + 0x03c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DAT_MASK_DIS	Reserved			TRI_GDIS
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	?	?	?	0

Bits	Name	Description	RW
31:5	Reserved	Writes to these bits have no effect and always read as 0.	R
4	DAT_MASK_DIS	Mask data when DMIC controller interface begin enable, write "1" all data will write to FIFO. BACK door	RW
3:1	Reserved	Writes to these bits have no effect and always read as 0.	R
0	TRI_GDIS	Voice Trigger clock gate disable.	RW

12.2.6.3.17 DMIC Voice Trigger Status Register (DMIC_VTSR)

	DMIC_VTSR																BASE + 0x040															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													VT2_TRI_ST	VT2_TRI_ST	VT1_TRI_ST
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Writes to these bits have no effect and always read as 0.	R
2	VT3_TRI_ST	When this bit is '1' indicate that voice trigger 3 was triggered. Write this bit '1' will clear it.	RWC

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	VT2_TRI_ST	When this bit is '1' indicate that voice trigger 2 was triggered. Write this bit '1' will clear it.	RWC
0	VT1_TRI_ST	When this bit is '1' indicate that voice trigger 1 was triggered. Write this bit '1' will clear it.	RWC

12.2.6.4 DMIC Control Operation

12.2.6.4.1 DMIC record application flow

1. Configure filter and gain
2. Set DMIC_CR0.RESET = ‘1’ and then wait for this bit read ‘0’
3. Set DMIC_EN = ‘1’, DMIC Controller will transfer the data to FIFO

12.2.6.4.2 Trigger application flow

1. Configure as DMIC record application flow
2. Configure trigger threshold and trigger mode
3. Set DMIC_CR0.RESET = ‘1’ and DMIC_CR0.RESET_TRI = ‘1’, and then wait for these bit read ‘0’.
4. Set DMIC_EN = '1', and set TRI_EN = '1'.
5. Wait trigger interrupt.
6. When the interrupt is generated , then DMIC Controller will transfer the data to FIFO.

12.2.6.4.3 Wakeup by DMIC Trigger flow

1. Configure as DMIC record application flow
2. Configure trigger threshold and trigger mode
3. Set DMIC_CR0.RESET = ‘1’ and DMIC_CR0.RESET_TRI = ‘1’, and then wait for these bit read ‘0’.
4. Set DMIC_EN = '1', and set TRI_EN = '1'.
5. Configure CPM to mask INTC’s interrupt
6. Disable CPU’s IE
7. Configure CPM to make system turn into sleep
8. When the voice meet the trigger requirement, DMIC will generate a interrupt to INTC and then wakeup CPU.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.7 SPDIF OUT

12.2.7.1 Spdif protocol format

12.2.7.1.1 SPDIF protocol frame format

0-31	32-63	64-95	……	1520-1551	1552-1583
Subframe0	Subframe1	Subframe1		Subframe190	Subframe191

Note: One bit status format be included in one subframe

Note: subformat.P is One bit in status format

12.2.7.1.2 SPDIF protocol status format

0byte	0	1	2	3	4	5	6	7
	a	b	c	d			mode	
1byte	8	9	10	11	12	13	14	15
	Category code							
2byte	16	17	18	19	20	21	22	23
	Source number				Channel number			
3byte	24	25	26	27	28	29	30	31
	sampling frequency				CLOCK ACCRACY			
4byte	32	33	34	35	36	37	38	39
	Word length				Original sampling frequency			
5byte	40	41	42					
	CGMS-A							
….								
23byte	184	185	186	187	188	189	190	191

Note: ingenic spdif out status format

If(SPFCFG2[0] = 1'b0 && SPFCFG2[1] = 1'b1)

a = 1'b0

b = 1'b1

c = SPFCFG2[2]

d = 3'b000

mode = 2'b00

category code = SPFCFG2[15:8]

source number = 4'b0000

channel number = 4'b0000

sampling frequency = SPFCFG2[29:26]

clock accuracy = SPFCFG2[17:16]

word length =4'b0000

original sampling frequency = 4'b0000

CGMS-A = 3'b000

else

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

a = SPFCFG2[0]
b = SPFCFG2[1]
c = SPFCFG2[2]
d = {2'b00,SPFCFG2[3]}
mode = SPFCFG2[7:6]
category code = SPFCFG2[15:8]
source number = SPFCFG1[11:8]
channel number = SPFCFG1[7:4] / SPFCFG1[3:0]
sampling frequency = SPFCFG2[29:26]
clock accuracy = SPFCFG2[17:16]
word length = {SPFCFG2[18]: SPFCFG2[21:19]}
original sampling frequency = SPFCFG2[25:22]
CGMS-A = 3'b000

12.2.7.1.3 SPDIF protocol subframe format

0-3	4-7	8-27	28	29	30	31
Sync peamble	Auxiliary	Audio sample data	V	U	C	P

Note: ingenic spdif out subframe format:
Sync preamble [3:0] = 4'b0000
Auxiliary [3:0] = 4'b0000
Audio sample data[23:0] = { 4'b0000,sample_data}

12.2.7.2 Register Descriptions

Name	Base	Description
SPDIF_OUT	134db000	Base address of SPDIF OUT.

12.2.7.2.1 SPDIF Enable Register (SPENA)

The register SPENA is used to trigger SPDIF transmitter to work.

	SPENA																BASE + 0x00													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															SPEN
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	SPEN	Enable / disable the SPDIF transmitter. 0: SPDIF transmitter is disabled 1: SPDIF transmitter is enabled	RW

12.2.7.2.2 SPDIF Control Register (SPCTRL)

The register SPCTRL is used to control SPDIF to work.

	SPCTRL																BASE + 0x04											
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	D_TYPE	SIGN_N	INVALID	SFT_RST	Reserved										
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:15	Reserved	Writing has no effect, read as zero.	R
14	D_TYPE	If the bit number of data is less than16, the data in memory is as follows: 0: XXXXXXXXXXXXXXXX | Data 0 XXXXXXXXXXXXXXXX | Data 1 1: Data 1 | Data 0 Data 3 | Data 2	RW
13	SIGN_N	Signed to unsigned or not. If it is 1, the incoming and outgoing audio sample data will be transferred by toggle its most significant bit. 0: Not transfer 1: Do transfer	RW
12	INVALID	Data invalid bit. The data transmitted on SPDIF is valid or not. 0: Valid 1: Invalid	RW
11	SFT_RST	SPDIF FIFO software-reset. Set it to 1 and later it will be cleared by hardware auto. When SFT_RST returns back to 0, the FIFO finish reset. 0: Stop reset 1: Start reset	RW
10:0	Reserved	Writing has no effect, read as zero.	R

12.2.7.2.3 SPDIF Configure 1 Register (SPCFG1)

The register SPCFG1 is used to configure SPDIF.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	SPCFG1																BASE + 0x08															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														INIT_LVL	ZRO_VLD	Reserved				SRC_NUM				CH1_NUM				CH2_NUMl			
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:18	Reserved	Writing has no effect, read as zero.	R
17	INIT_LVL	Initial level set bit. 0: SPDIF initial level is low 1: SPDIF initial level is high	RW
16	ZRO_VLD	The valid bit of channel state is 0 or 1 when play ZERO sample under FIFO underflow. 0: Valid 1: Invalid	RW
15:12	Reserved	Writing has no effect, read as zero.	R
11:8	SRC_NUM	Source number.	RW
7:4	CH1_NUM	Channel 1 number. 0000:Unspecified	RW
3:0	CH2_NUM	Channel 2 number. 0000:Unspecified 0001~1111:A~O	RW

Note: SPCFG1[SRC_NUM], SPCFG1[CH1_NUM], SPCFG1[CH2_NUM] only use in spdif protocol status format

12.2.7.2.4 SPDIF Configure 2 Register (SPCFG2)

The register SPCFG2 is used to configure SPDIF.

	SPCFG2																BASE + 0x0c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		FS				ORG_FRQ				SAMPL_WL			MAX_WL	CLK_ACU		CAT_CODE								CH_MD		Reserved		PRE	COPY_N	AUDIO_N	CON_PRO	
RST	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	0	0	0	0

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, read as zero.	R
29:26	FS	Sampling frequency.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0000:44.1kHz 0010:48kHz 0011:32kHz 1010:96kHz 1110:192kHz Others: Reference IEC60958-3	
25:22	ORG_FRQ	Original sampling frequency. 1111:44.1kHz 1101:48kHz 1100:32kHz 0101:96kHz 0001:192kHz Others: Reference IEC60958-3	RW
21:19	SAMPL_WL	Sample word length. When MAX_WL=1: 001:20 bit 110:21 bit 010:22 bit 100:23 bit 101:24 bit Others: reserved When MAX_WL=0: 001:16 bit 110:17 bit 010:18 bit 100:19 bit 101:20 bit Others: reserved	RW
18	MAX_WL	Maximum audio sample word length. 0:20 bit; 1:24 bit.	RW
17:16	CLK_ACU	Clock Accuracy of transmitted clock. 00: Level II 01: Level I 10: Level III 11: Interface frame rate not matched to sampling frequency	RW
15:8	CAT_CODE	Category code. Reference IEC60958-3 for full details. 00 indicates “general” mode.	RW
7:6	CH_MD	Channel mode choose bit. 00: Mode 0 01~11: Reserved	RW
5:4	Reserved	Writing has no effect, read as zero.	R
3	PRE	Pre-emphasis set bit.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: None 1: 15us/15us	
2	COPY_N	Copyright set bit. 0: Copyright is asserted 1: Copyright is not asserted	RW
1	AUDIO_N	Linear PCM identification bit. 0: Audio sample word represents linear PCM samples 1: Audio sample word used for other purpose	RW
0	CON_PRO	Consumer mode and professional mode choose bit. 0: Consumer mode 1: Professional mode Professional is not supported in the chip.	RW

Note: SPCFG2 only use in spdif protocol status format

12.2.7.2.5 SPDIF Clock Divider Register (SPDIV)

SPDIV is used to set clock divider to generated spdif clk.

	I2SDIV																BASE + 0x10													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								DV							
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	DV	SPDIF clock divider value . SPDIV.DV is used to control the generating of SPDIF_CLK from dividing SYS_CLK. The dividing value only can be even .	RW

12.2.8 SPDIF IN

12.2.8.1 Register Descriptions

Name	Base	Description
SPDIF_IN	**134db100**	**Base address of SPDIF IN.**

12.2.8.1.1 SPDIF IN Enable Register (SPIENA)

The register SPIENA is used to trigger SPDIF receiver to work.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	SPIENA																BASE + 0x00													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															SPIEN
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	SPIEN	Enable / disable the SPDIF transmitter. 0: SPDIF receiver is disabled 1: SPDIF receiver is enabled	RW

12.2.8.1.2 SPDIF IN Configure 1 Register (SPICFG1)

The register SPICFG1 is used to configure SPDIF IN.

	SPICFG1																BASE + 0x04													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SRC1_NUM				SRC2_NUM				CH1_NUM				CH2_NUMl			
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:12	SRC1_NUM	Source number.(Channel A) 0000:Unspecified 0000~1111:1~15	R
11:8	SRC2_NUM	Source number.(Channel B) 0000:Unspecified 0001~1111:1~15	R
7:4	CH1_NUM	Channel 1 number.(Channel A) 0000:Unspecified 0001~1111:A~O	R
3:0	CH2_NUM	Channel 2 number.(Channel B) 0000:Unspecified 0001~1111:A~O	R

12.2.8.1.3 SPDIF IN Configure 2 Register (SPICFG2)

The register SPICFG2 is used to configure SPDIF IN.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	SPICFG2																BASE + 0x08													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CAT2_CODE								CAT1_CODE								CH2_MD		CH1_MD		PRE2			PRE1			COPY2_N	COPY1_N	AUDIO2_N	AUDIO1_N	CON2_PRO	CON1_PRO
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	CAT2_CODE	Category code.(Channel B) Reference IEC60958-3 for full details. 00 indicates “general” mode.	R
23:16	CAT1_CODE	Category code.(Channel A) Reference IEC60958-3 for full details. 00 indicates “general” mode.	R
15:14	CH2_MD	Channel mode choose bit.(Channel B) 00: Mode 0 01~11: Reserved	R
13:12	CH1_MD	Channel mode choose bit.(Channel A) 00: Mode 0 01~11: Reserved	R
11:9	PRE2	Pre-emphasis (Channel B) 000: 2 audio channels without pre-emphasis 001: 2 audio channels with 15us/15us pre-emphasis 010~011:Reserved (2 audio channels with pre-emphasis) Other states not defined	R
8:6	PRE1	Pre-emphasis (Channel A) 000: 2 audio channels without pre-emphasis 001: 2 audio channels with 15us/15us pre-emphasis 010~011:Reserved (2 audio channels with pre-emphasis) Other states not defined	R
5	COPY2_N	Copyright set bit.(Channel B) 0: Copyright is asserted 1: Copyright is not asserted	R
4	COPY1_N	Copyright set bit.(Channel A) 0: Copyright is asserted 1: Copyright is not asserted	R
3	AUDIO2_N	Linear PCM identification bit.(Channel B) 0: Audio sample word represents linear PCM samples 1: Audio sample word used for other purpose	R
2	AUDIO1_N	Linear PCM identification bit.(Channel A) 0: Audio sample word represents linear PCM samples 1: Audio sample word used for other purpose	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	CON2_PRO	Consumer mode and professional mode choose bit.(Channel B) 0: Consumer mode 1: Professional mode Professional is not supported in the chip.	R
0	CON1_PRO	Consumer mode and professional mode choose bit.(Channel A) 0: Consumer mode 1: Professional mode Professional is not supported in the chip.	R

12.2.8.1.4 SPDIF IN Configure 3 Register (SPICFG3)

The register SPCFG3 is used to configure SPDIF IN.

	SPCFG2																BASE + 0x0c													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				FS2				FS1				ORG2_FRQ				ORG1_FRQ				SAMPL2_WL			SAMPL1_WL			MAX2_WL	MAX1_WL	CLK2_ACU		CLK1_ACU	
RST	?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Writing has no effect, read as zero.	R
27:24	FS2	Sampling frequency.(Channel B) 0000:44.1kHz 0001:Sampling frequency not indicated 0010:48kHz 0011:32kHz 0100:22.05kHz 0110:24kHz 1000:88.2kHz 1001:768kHz 1010:96kHz 1100:176.4kHz 1110:192kHz Reference IEC60958-3	R
23:20	FS1	Sampling frequency.(Channel A) 0000:44.1kHz 0001:Sampling frequency not indicated 0010:48kHz 0011:32kHz 0100:22.05kHz 0110:24kHz	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1000:88.2kHz 1001:768kHz 1010:96kHz 1100:176.4kHz 1110:192kHz Reference IEC60958-3	
19:16	ORG2_FRQ	Original sampling frequency.(Channel B) 1111:44.1kHz 1110:Reserved 1101:48kHz 1100:32kHz 1011:22.05kHz 1010:11.025kHz 1001:24kHz 1000:16kHz 0111:88.2kHz 0110:8kHz 0101:96kHz 0100:Reserved 0011:176.4kHz 0010:12kHz 0001:192kHz 0000:not indicated(default) Reference IEC60958-3	R
15:12	ORG1_FRQ	Original sampling frequency. (Channel A) 1111:44.1kHz 1110:Reserved 1101:48kHz 1100:32kHz 1011:22.05kHz 1010:11.025kHz 1001:24kHz 1000:16kHz 0111:88.2kHz 0110:8kHz 0101:96kHz 0100:Reserved 0011:176.4kHz 0010:12kHz 0001:192kHz 0000:not indicated(default) Reference IEC60958-3	R
11:9	SAMPL2_WL	Sample word length.(Channel B)	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		When MAX_WL=1: 001:20 bit 110:21 bit 010:22 bit 100:23 bit 101:24 bit Others: reserved When MAX_WL=0: 001:16 bit 110:17 bit 010:18 bit 100:19 bit 101:20 bit Others: reserved	
8:6	SAMPL1_WL	Sample word length.(Channel A) When MAX_WL=1: 001:20 bit 110:21 bit 010:22 bit 100:23 bit 101:24 bit Others: reserved When MAX_WL=0: 001:16 bit 110:17 bit 010:18 bit 100:19 bit 101:20 bit Others: reserved	R
5	MAX2_WL	Maximum audio sample word length.(Channel B) 0:20 bit; 1:24 bit.	R
4	MAX1_WL	Maximum audio sample ssword length.(Channel A) 0:20 bit; 1:24 bit.	R
3:2	CLK2_ACU	Clock Accuracy of transmitted clock.(Channel B) 00: Level II 01: Level I 10: Level III 11: Interface frame rate not matched to sampling frequency	R
1:0	CLK1_ACU	Clock Accuracy of transmitted clock.(Channel A) 00: Level II 01: Level I 10: Level III 11: Interface frame rate not matched to sampling frequency	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.8.1.5 SPDIF IN Clock Divider Register (SPIDIV)

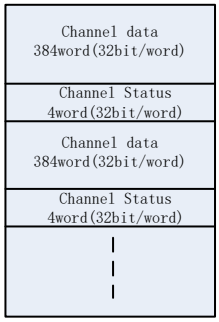
SPIDIV is used to set clock divider to generated spdif in clk.

	I2SDIV																BASE + 0x10													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								DV							
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	DV	SPDIF clock divider value . SPDIV.DV is used to control the generating of SPDIF_CLK from dividing SYS_CLK. The dividing value only can be even .	RW

Note: You can't configure the value of DV at will. You must make sure that the working clock is 640 times bigger than sample clock after frequency division. The accurate value of the working clock need not care. Just guarantee working clock 640times bigger than sample clock.

12.2.8.2 Spdif in guide



Channel status is consist of 4 word. Channel Status is used for storage 40bit of spdif protocol status , structure of Channel status is:

Spdif protocol status	Frame1status: 0-31	Frame1status: 32-39	Frame2status: 0-31	Frame2status: 32-39
Channel status	Word0[0:31]	Word1[24:31]	Word2[0:31]	Word3[24:31]

Channel Data is consist of 384 word. Channel Data is used for storage spdif protocol subframe, The storage of structure is

One word in channel data	0:27	28	29:31
	subframe[0:27]	Parity	3'b000

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

12.2.9 MIXER

12.2.9.1 Block Diagram

12.2.9.2 Register Descriptions

Name	Base	Description
MIXER	134dc000	Base address of MIXER.

12.2.9.2.1 Mixer Control Register (MIX_CTL)

	MIX_CTL																												BASE + 0x000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													MIX_RESET	MIX_EN	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writes to these bits have no effect and always read as 0.	R
1	MIX_RESET	If set this bit to '1' will reset all MIXER registers.	RWS
0	MIX_EN	Mixer enable. Set this bit to '1' will enable the function.	RW

12.2.9.2.2 Mixer Configure Register (MIX_CFR)

	MIX_CFR																												BASE + 0x004	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									MIX_CH		MIX_MODE			Lr_mix	Last_smp
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:7	Reserved	Writes to these bits have no effect and always read as 0.	R
6:5	MIX_CH	Mixed channel number 00: Mono 01: Stereo 10~11: Reserved	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4:3	MIX_MODE	Mixed mode choice: 00: Linear weighted plus 01: Average 10: Clamping 11: Nonlinear Distort	RW
2	Reserved	Writes to these bits have no effect and always read as 0.	R
1	LR_MIX	Lr mix When set 1'b0, normal When set 1'b1, MixerL input0 = Mix_in1[63:32]， MixerL input0 = Mix_in0[31:0] MixerH do not use Mix_out[63:0] = [MixerL_output, MixerL_output]	RW
0	LAST_SMP	LAST_SMP When set 1'b0, nomal When set 1'b1 When FIFOIN0 is emply， but FIFOIN1 is not emply MixerL, MixerH, do not stop MixerL input0 = FIFOIN0 last samp[31:0] MixerH input0 = FIFOIN0 last samp[63:32] Vice verse	RW

12.2.9.2.3 Mixer GATE CLOCK Register (MIX_GCLKR)

	MIX_GCLKR																														BASE + 0x008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															GCLK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
0	GCLK	When mix_en = 1'b1, the bit is not effect When mix_en = 1'b0, and the bit is 1'b1, mix clock is not gated	W WR

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

13 Internal CODEC

13.1 DESCRIPTOR

Ingenic Codec is a low power, high resolution, mono CODEC solution which employs Sigma-Delta noise-shaping technique. The ADC，DAC and power amplifier are integrated to provide total solutions. With 24 bits resolution for DAC and 24 bits resolution for ADC. Ingenic Codec is suitable for applications in high end consumer digital, automobile audio, multimedia and digital system.

13.2 BLOCK DIAGRAM

Ingenic Codec contains 1 DAC channel for playback through double end headphone and 1 ADC channel for recording from double end microphone.

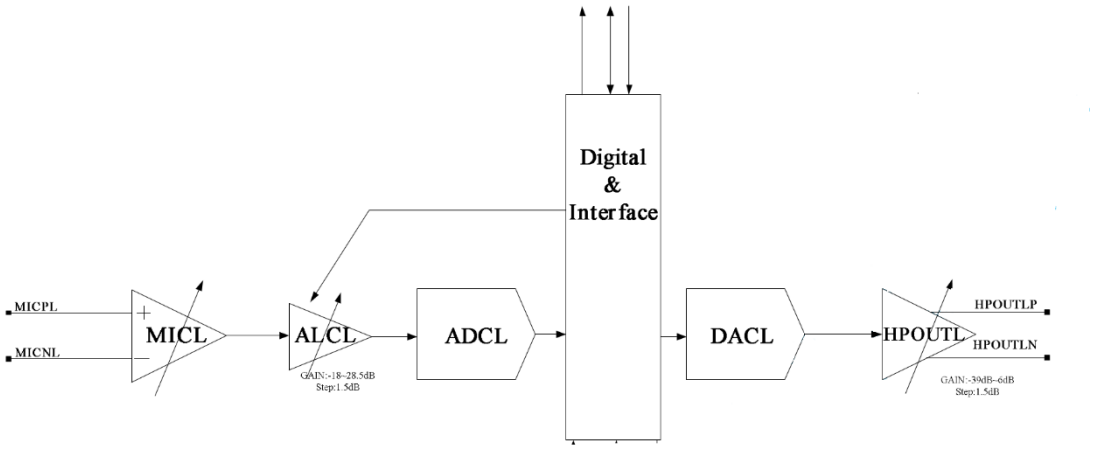


Figure 13-1 Codec Overview

13.3 Electrical Characteristics

Measurement conditions: T = 25°C, AVDD = 1.8 V, DVDD = 0.9V, 1KHz Sine Input, FS = 48KHZ					
Parameter	Test conditions	Min.	Type	Max.	Unit
Analog Supply		1.62	1.8	1.98	V
Digital Supply		0.81	0.9	0.99	V
Temperature		-40		125	℃
ADC					
SNR	A-weighted		92		
THD			-81		
Bias Voltage		0.5*A		0.85*AV	V

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		VDD		DD	
Bias Current				3	mA
Mic Gain		0		20	dB
ALC Gain		-18		28.5	dB
Gain Step Size			1.5		dB
input Resistance		8		88	KΩ
input Capacitance			10		pF
DAC					
SNR	A-weighted		93		dB
THD	60mWΩ		-70		dB
	30mWΩ		-75		dB
	600Ω		-80		dB
Programmable Gain		-39		6	dB
Gain Step Size			1.5		
Output Resistance				1	Ω
Output Capacitance			20		pF
Power Supply Rejection	1KHZ		55		dB
Power Consumption					
Standby			0.1		mA
Recording			2.5		mA
Playback			2.5		mA

13.4 I2S MASTER AND SLAVER OPERATION

Ingenic Codec provides the I2S interface of audio data stream which gets into DAC and out from ADC, both of which can be configured in master or slave mode. Different audio data formats are available for different operating modes. This is demonstrated in following table.

Table 13-1 Supported Data Formats in Different Modes

Data Format	ADC		DAC	
	Master	Slave	Master	slave
Left Justified	OK	NO	OK	OK
NORMAL	OK	OK	OK	OK

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

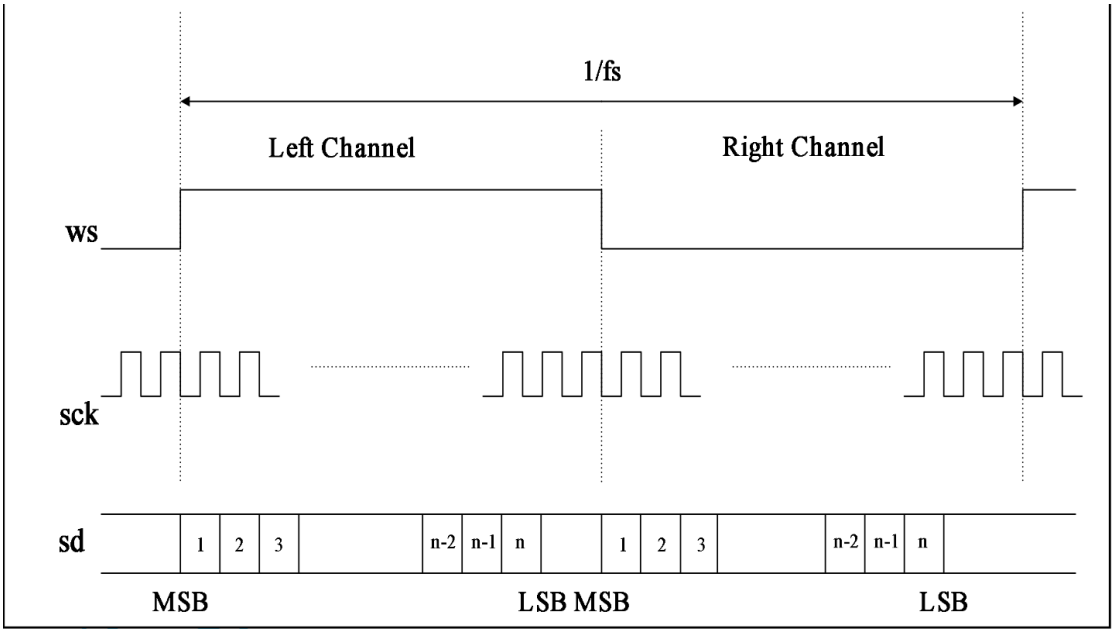


Figure 13-2 Left Justified Mode

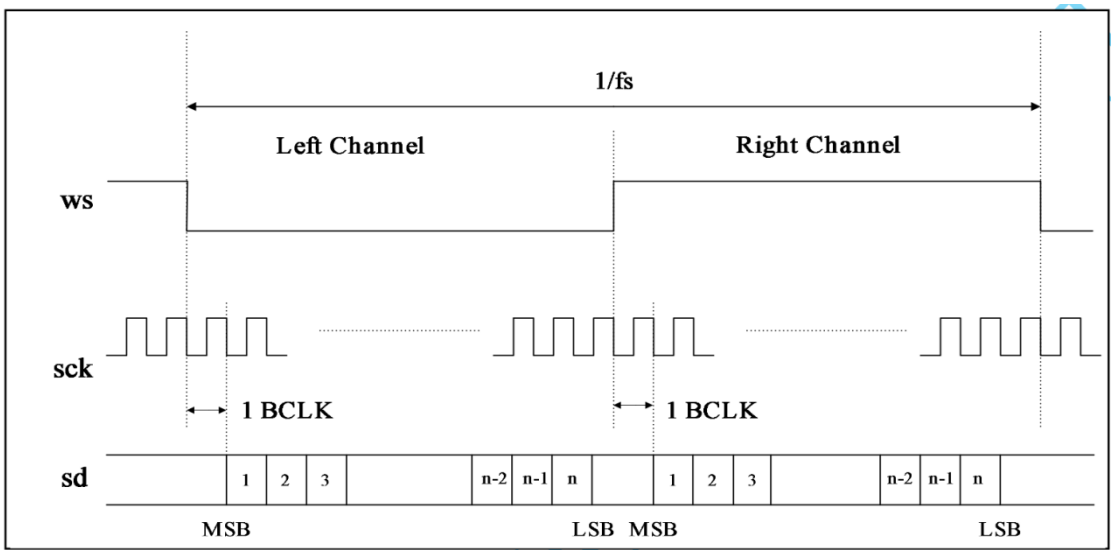


Figure 13-3 I2S Mode

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

13.5 Register descriptor

13.5.1 Reset register(0x00)

																														BASE+0x00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								BIST RST	Reserved					DIGITAL RST	SYSTEM RST
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	RW
7	BIST RST	Bist module reset 0: Reset 1: work	R
6:2		Reserved	RW
1	DIGITAL RST	Codec digital core reset, The reset only reset codec data path 0: Reset 1: work	R
0	SYS RST	Codec system reset, The signal will reset the register which control all the digital and analog part 0: Reset 1: work	RW

13.5.2 ADC-DAC Configure1 Register(0x02)

																														BASE+0x08
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								ADC LP	ADC VL		ADC MODE			ADC SWAP	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0

Bits	Name	Description
7	ADC LRC POL	ADC LRC Polarity 0: Normal 1: Reversal
6:5	ADC VALID LEN	ADC Valid Word Length in one 1/2 Frame 11:32bits 10:24bits 01:20bits 00:16bits
4:3	ADC MODE	ADC Mode 10:I2S Mode 01:Left Justified Mode

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		00,11 Reserved Node
2		Reserved
1	ADC SWAP	ADC Left-Right SWAP 0: Normal 1: Swap
0		Reserved

13.5.3 ADC-DAC Configure2 Register(0x03)

BASE+0x0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								DAC IO M	DAC IN M	ADC IO M	ADC IN M	ADC LEN		ADC RST	ADC BIT P
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bits	Name	Description
7	DAC IO Master	DAC Mode Select for IO pin 0：Slaver mode 1：Master mode
6	DAC inner Master	DAC Mode Select for inner module 0：Slaver mode 1：Master mode
5	ADC IO Master	ADC Mode Select for IO pin 0：Slaver mode 1：Master mode
4	ADC inner Master	ADC Mode Select for inner module 0：Slaver mode 1：Master mode
3:2	ADC LENGTH	ADC 1/2 Frame Word Length 11:32bits 10:24bits 01:20bits 00:16bits
1	ADC RESET	ADC reset 0: Reset 1: work
0	ADC BIT POLARITY	ADC Bit Clock Polarity 0: Normal 1: Reversal

13.5.4 ADC-DAC Configure3 Register(0x04)

BASE+0x10

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								DAC ENC P	DAC VL		DAC MODE	DAC SWAP			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description
7	DAC LRC POLARITY	DAC LRC Polarity 0: Normal 1: Reversal
6:5	DAC VALID LENGTH	DAC Valid Word Length in one 1/2 Frame 11:32bits 10:24bits 01:20bits 00:16bits
4:3	DAC MODE	DAC mode 10:I2S Mode 01:Left Justified Mode 00,11 Reserved Node
2	DAC SWAP	DAC Left-Right SWAP 0: Normal 1: Swap
1:0		Reserved

13.5.5 ADC-DAC Configure4 Register(0x05)

BASE+0x14

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												DAC LEN		DAC RST	DAC BIT P
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	11	0

Bits	Name	Description
7:4		Reserved
3:2	DAC LENGTH	DAC 1/2 Frame Word Length 11:32bits 10:24bits 01:20bits 00:16bits
1	DAC RESET	DAC reset 0: Reset 1: work
0	DAC BIT POLARITY	DAC Bit Clock Polarity 0: Normal 1: Reversal

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

13.5.6 Choose ALC Gain register(0x0a)

BASE+0x28

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																										PGA_GAIN_SEL	Reserved				
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
7		Reserved
5	PGA_GAIN_SEL	1: choose the register 0x94[4:0] to control the gain of the PGA 0: choose the register ALCL to control the gain of the PGA
4:0		Reserved

13.5.7 Select Pre-charge / Dis-charge Register(0x21)

BASE+0x84

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																									CHOOSE2	CHOOSE4	CHOOSE8	CHOOSE16	CHOOSE32	CHOOSE64	CHOOSE128
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
7		Reserved
6	CHOOSE2	1: Choose the current 2*I
5	CHOOSE4	1: Choose the current 4*I
4	CHOOSE8	1: Choose the current 8*I
3	CHOOSE16	1: Choose the current 16*I
2	CHOOSE32	1: Choose the current 32*I
1	CHOOSE64	1: Choose the current 64*I
0	CHOOSE128	1: Choose the current 128*I

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

13.5.8 Control1 Register(0x22)

BASE+0x88

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																										REF VOL EN	ADCCUR E	BAIS VOL E	BIAS VOL		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6		Reserved
5	REF VOL EN	The enable signal of reference voltage module 0: Disable 1: Enable I
4	ADC CUR EN	The enable signal of current source for ADC 0: Disable 1: Enable
3	BIAS VOL EN	The enable signal of MIC bias voltage buffer 0: Stop Working 1: Working
2:0	BIAS VOL	The level range control signal of MIC bias voltage 000: 1.0*VREF 111: 1.7*VREF, Step: 0.1*VREF

13.5.9 Control2 Register(0x23)

BASE+0x8C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								ADCL MUTE	ADCL INIT	ADCL VOL E	ADCL ZERO				
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
7	ADCL MUTE	The mute signal of MIC module in the ADCL 0: mute 1: work
6	ADCL INITIAL	The initial signal of MIC module in the ADCL 0: initialization 1: work
5	ADCL VOL EN	The enable signal of reference voltage buffer of ADCL 0: Disable 1: enable
4	ADCL ZERO	The enable signal of the ADCL input zero-crossing

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: Stop Working 1: Working
3:0		Reserved

13.5.10 Control3 Register(0x24)

BASE+0x90

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								ADCL MIC G		ALCL EN	ADCL MIC E				
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	ADCL MIC GAIN	The gain signal of MIC module in the ADCL 00: 0db 01: 6db 10: 20db 11: 30db
5	ALCL EN	The enable signal of ALCL module 0: Stop Working 1: Work
4	ADCL MIC EN	The enable signal of MIC module in the ADCL 0: Disable 1: Enable
3:0		Reserved

13.5.11 Control4 Register(0x25)

BASE+0x94

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											ALCL GAIN			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Name	Description
7:5		Reserved

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

4:0	ALCL GAIN	The gain control of ALCL module 0000: -16.5db 1111: 6db Step: 1.5db

13.5.12 Control5 Register(0x26)

BASE+0x98

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								ADCL_ALC I	ADCL CLK E	ADCLADC E		DAC CUR E	DAC REF E	POP CTL	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description
7	ADCL_ALC INIT	The initial signal of ALC module in the ADCL 0: Initialization 1: Work
6	ADCL CLK EN	The enable signal of Clock for ADCL signal 0: Set to logic “1” 1: Work
5	ADCL_ADC EN	The enable signal of ADC module in the ADCL 0: Disable 1: Enable
4	ADCL_ADC INIT	The initial signal of ADC module in the ADCL 0: Initialization 1: Work
3	DAC CUR EN	The enable signal of current source for DAC channel 0: Disable 1: Enable
2	DAC REF EN	The enable signal of reference voltage buffer in the left DAC channel 0: Disable 1:Enable
1:0	POP CTL	The Control Signal of POP sound in the left DAC channel 01: Initialization 10: Work

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

13.5.13 Control6 Register(0x27)

BASE+0x9C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								DACL_ERFE	DACL CLK E	DACL EN	DACL INIT				
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
7	DACL_REF_EN	The enable signal of reference voltage of DACL module 0: Disable 1:Enable
6	DACL CLK EN	The enable signal of CLOCK module for DACL 0: Set CLOCK to logic “1” 1: Work
5	DACL EN	The enable signal of DACL module 0: Disable 1:Enable
4	DACL INIT	The initial signal of DACL module 0: initialization 1: work
3:0		Reserved

13.5.14 Control7 Register(0x28)

BASE+0xA0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								HPOUTL M	HPOUTL E	HPOUTL I	HPOUTL G				
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
7	HPOUTL MUTE	The mute signal of HPOUTL module 0: Mute 1: Work
6	HPOUTL EN	The enable signal of HPOUTL module 0: Disable 1:Enable
5	HPOUTL INIT	The initial signal of HPOUTL module 0: initialization 1:work
4:0	HPOUTL GAIN	The gain control of HPOUTL module

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0000: -39db 11111: 6db Step: 1.5db

13.5.15 ALG CONFIG1(0x44)

																														BASE+0x110	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												SLOW CLKE	SAMPLE RATE		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7:4		reserved bit
3	SLOW CLK EN	Slow clock enabled, used for the zero cross timeout
2:0	SAMPLE RATE	Approximate sample rate 000: 96KHZ 001: 48KHZ 010: 44.1KHZ 011: 32KHZ 100: 24KHZ 101: 16KHZ 110: 12KHZ 111: 8KHZ

13.5.16 ALG MAXL(0x45)

																														BASE+0x114	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								ALG_MAXL							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0

Bits	Name	Description
7:0	ALG MAXL	The low 8 bit of the ALGC maximum level

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

13.5.17 ALGMAXH(0x46)

BASE+0x118

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								ALG_MAXH							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Name	Description
7:0	ALGMAXH	The high 8 bit of the ALGC maximum level

13.5.18 ALG MINL(0x47)

BASE+0x11C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								ALG_MINL							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0

Bits	Name	Description
7:0	ALG_MIN	The low 8 bit of the ALGC minimum level

13.5.19 ALG MINH(0x48)

BASE+0x120

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								ALG_MINH							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Name	Description
7:0		The high 8 bit of the AGC minimum level

13.5.20 ALG CONFIG2(0x49)

BASE+0x124

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

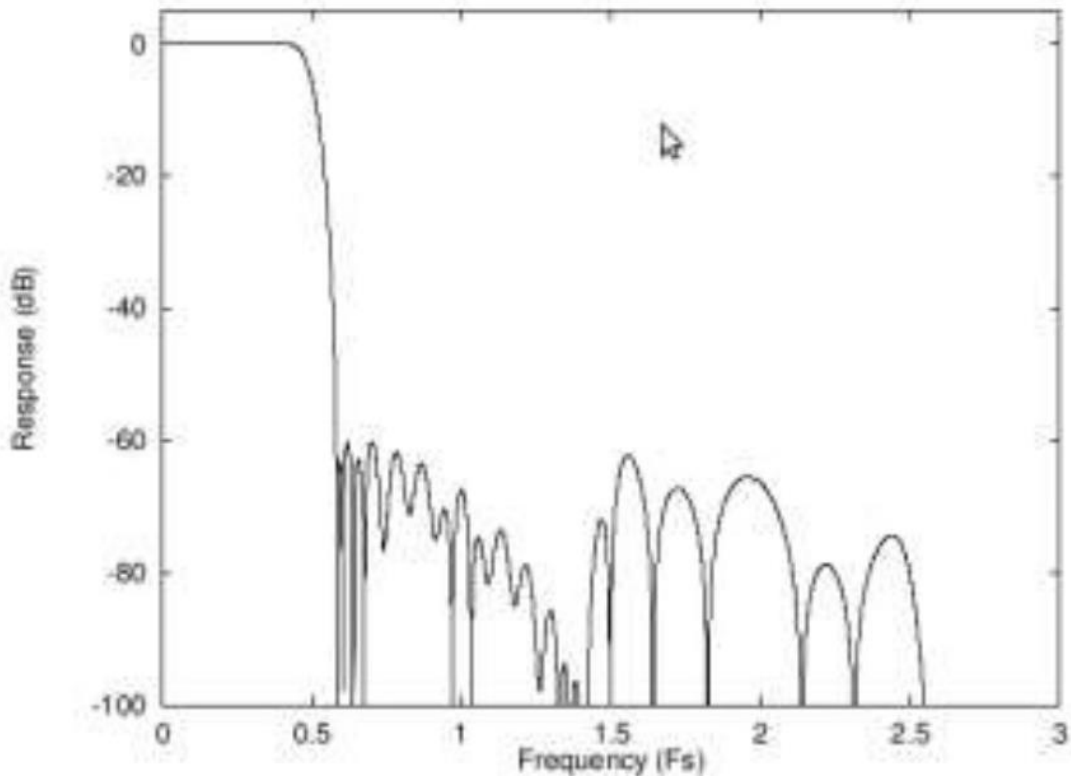
Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Reserved																							ENABLE	MAXGAIN			MINGAIN		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

Bits	Name	Description
7		reserved bit
6	ALG ENABLE	ALGC function select 0: ALGC function off 1: ALGC function enable
5:3	ALG MAXGAIN	Set maximum gain of PGA 000: -13.5db 111: 28.5db step is 6db
2:0	ALG MINGAIN	Set minimum gain of PGA 000: -18db 111: 24db step is 6db

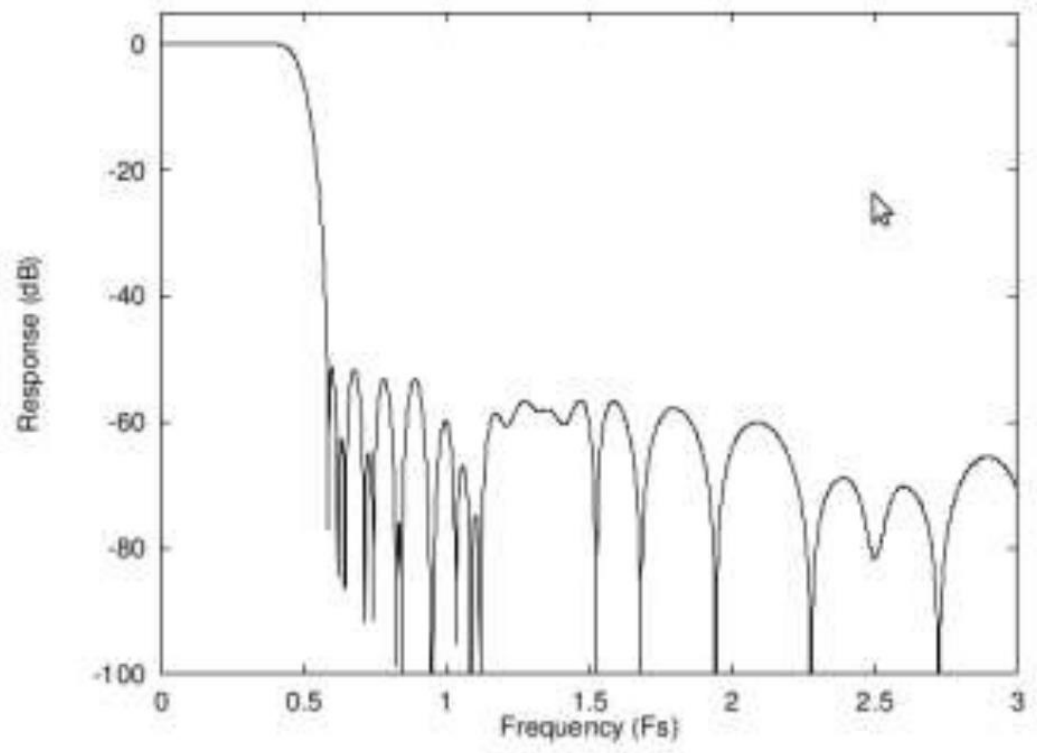
13.6 FREQUENCY AMPLITUDE RESPONSE

The in-band ripple is within 0.1db and output of band rejection is over 93db.



ADC frequence responese

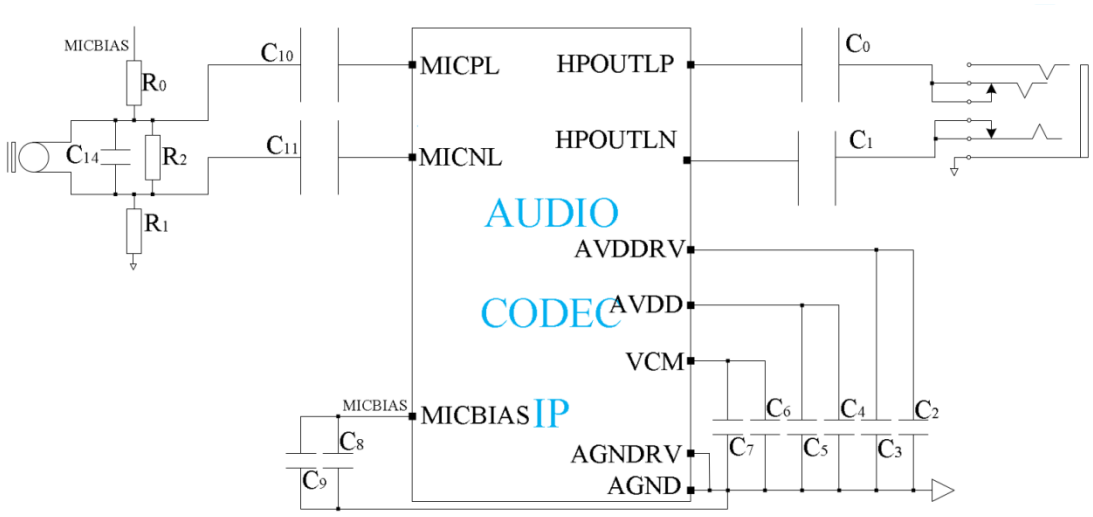
Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.



DAC frequence responese

13.7 PCB LAYOUT GUIDE

The typical connection of Ingenic Codec is shown in the following figure. Customer can modify the connection according to the practical application.



Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

13.8 APPLICATION REFERENCE

13.8.1 POWER UP

STEP	DESCRIPTION
0	Supply the power of the digital part and the analog part
1	Configure the register 0x98 [1:0] to 2'b01, to setup dc voltage of the DAC channel output
2	Configure the register 0x84[7:0] to 8'b0000 0001,
3	Configure the register 0x88[5] to 1, to setup reference voltage
4	Configure the register 0x84[7:0] to 8'b1111 1111, the suggestion slot time of the step is 20ms
5	Wait until the voltage of VCM keep stable at the AVDD/2,
6	Configure the register 0x84[7:0] to the appropriate value,

13.8.2 POWER OFF

STEP	DESCRIPTION
0	Keep the power on and disable the DAC and ADC
1	Configure the register 0x84[7:0] to 8'b0000 0001
2	Configure the register 0x88[5] to 1'b1,
3	Configure the register 0x84[7:0] to 8'b1111 1111, the suggestion slot time of the step is 20ms
4	Wait until the voltage of VCM keep stable at AGND
5	Power off the analog power supply and digital power supply

13.8.3 ENABLE ADC

STEP	DESCRIPTION
0	Power up the CODEC
1	Configure the register 0x8C[7] to 1, to end the mute station of the ADC left channel
2	Configure the register 0x88[4] to 1, to enable the current source of audio
3	Configure the register 0x8C[5] to 1, to enable the reference voltage buffer in ADC left channel
4	Configure the register 0x90[5] to 1, to enable the ALC module in ADC left channel
5	Configure the register 0x98[6] to 1, to enable the clock module in ADC left channel
6	Configure the register 0x98[5] to 1, to enable the ADC module in ADC left channel
7	Configure the register 0x98[4] to 1, to end the initialization of the ADCL module
8	Configure the register 0x98[7] to 1, to end the initialization of the ALC left module
9	Configure the register 0x8C[6] to 1, to end the initialization of the MIC left module
10	Configure the register 0x90[7:6] , to select the gain of the MIC left module
11	Configure the register 0x94[4:0] , to select the gain of the ALC left module
12	Configure the register 0x90[3] , to enable the zero-crossing detection function in ADC left channel

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

13.8.4 DISABLE ADC

STEP	DESCRIPTION
0	Keep ADC channel work and stop recording
1	Configure the register 0x8C[4] to 0, to disable the zero-crossing detection function in ADC left channel
2	Configure the register 0x98[5] to 0, to disable the ADC module in ADC left channel
3	Configure the register 0x98[6] to 0, to disable the clock module in ADC left channel
4	Configure the register 0x90[5] to 0, to disable the ALC module in ADC left channel
5	Configure the register 0x90[4] to 0, to disable the MIC module in ADC left channel
6	Configure the register 0x8C[5] to 0, to disable the reference voltage buffer in ADC left channel
7	Configure the register 0x88[4] to 0, to disable the microphone bias voltage buffer
8	Configure the register 0x98[4] to 0, to begin the initialization of the ADC left module
9	Configure the register 0x98[7] to 0, to begin the initialization of the ADC left module
10	Configure the register 0x8C[6] to 0, to begin the initialization of the MIC left module

13.8.5 ENABLE DAC

STEP	DESCRIPTION
0	Power up the CODEC
1	Configure the register 0x98[3] to 1, to enable the current source of DAC
2	Configure the register 0x98[2] to 1, to enable the reference voltage buffer of the DACL channel
3	Configure the register 0x98[1:0] to 2’b10, to enable POP sound in the DAC left channel
4	Configure the register 0xA0[4] to 1, to enable the HPDRV module in the DAC left channel
5	Configure the register 0xA0[5] to 1, to end the initialization of the HPDRV module in the left DAC channel
6	Configure the register 0x9C[7] to 1, to enable the reference voltage of DACL module
7	Configure the register 0x9C[6] to 1, to enable the clock module of DACL module
8	Configure the register 0x9C[5] to 1, to enable the DACL module
9	Configure the register 0x9C[4] to 1, to end the initialization of the DAC module in the DAC left channel
10	Configure the register 0xA0[6] to 1, to end the mute station of the DAC module in the DAC left channel
11	Configure the register 0xA0[4:0] to 1, to select the gain of HPDRV module in the DAC left channel

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

13.8.6 DISABLE DAC

STEP	DESCRIPTION
0	Keep DAC channel work and input the mute signal
1	Configure the register 0xA0[4:0], to 4'b0000, to select the gain of HPDRV in the DAC left channel
2	Configure the register 0xA0[6] to 0, to mute the HPDRV module in the DAC left channel
3	Configure the register 0xA0[5] to 0, to initialize the DAC module in the DAC left channel
4	Configure the register 0xA0[4] to 0, to disable the HPDRV module in the DAC left channel
5	Configure the register 0x9C[5] to 0, to disable the DACL module
6	Configure the register 0x9C[6] to 0, to disable the clock module of DACL module
7	Configure the register 0x9C[7] to 0, to disable the reference voltage of DACL module
8	Configure the register 0x98[1:0] to 2'b01, to initialize of POP sound in the DAC left channel
9	Configure the register 0x98[2] to 0, to disable the reference voltage buffer of the DAC left channel
10	Configure the register 0x98[3] to 0, to disable the current source of DAC
11	Configure the register 0x9C[4] to 0, to begin the initialization of the HPDRV module in the DAC left channel

13.8.7 ENABLE ALC

The Ingenic CODEC has the ALC function which can adjust the amplitude of the input analog signal automatically. You can use the register to enable or disable this function. We will give you some application reference about how to use this function.

STEP	DESCRIPTION
0	set the Max level and Min level of the ALC need to control
1	Configure the register 0x44[2:0] according to the sample rate,
2	Configure the register 0x49[6] to 1, to enable the ALC module
3	Configure the register 0xa[5] to 1, to choose the ALC module to control the gain of the PGA

Note:
The register 0x45 and 0x46 control the max level of the ALC
Max_level = {reg0x46, reg0x45}
The relationship between the max_level and signal amplitude(db) is equal to :
Amplitude(dB) = 20log(max_level/16h'7FFF)
16'7FFF means the full scale amplitude

The register 0x47 and 0x48 control the min level of the ALC
Min_level = {reg0x48, reg0x47}
The relationship between the min_level and signal amplitude(db) is equal to :
Amplitude(dB) = 20log(min_level/16h'7FFF)
16'7FFF means the full scale amplitude

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

13.8.8 DISABLE ALC

STEP	DESCRIPTION
0	Configure the register 0x49[6] to 0, to disable the ALC module, then the ALC output gain will keep to the last value
1	Configure the register 0xa[5] to 0, to choose to use the register to control the gain of the PGA

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Section 5

MEMORY INTERFACE

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

14 DDR Controller

14.1 Overview

DDRC (DDR Controller) is a general IP which provides an interface to LPDDR2 and LPDDR3 memories. The DDRC IP is designed for SOC usage and is configurable, scalable to meet the requirement of various SOCs.

Features:

- Highly configurable Quality of Service system
- Support clock-stop mode
- Support auto-refresh and self-refresh
- Support power-down mode and deep-power-down mode
- Programmable DDR timing parameters
- Programmable DDR row and column address width
- Programmable remapping from Logic address to Physical address

Supported DDR SDRAM Types

- LPDDR2
- LPDDR3

14.1.1 Block Diagram

Following figure shows the functional block diagram of DDR system.

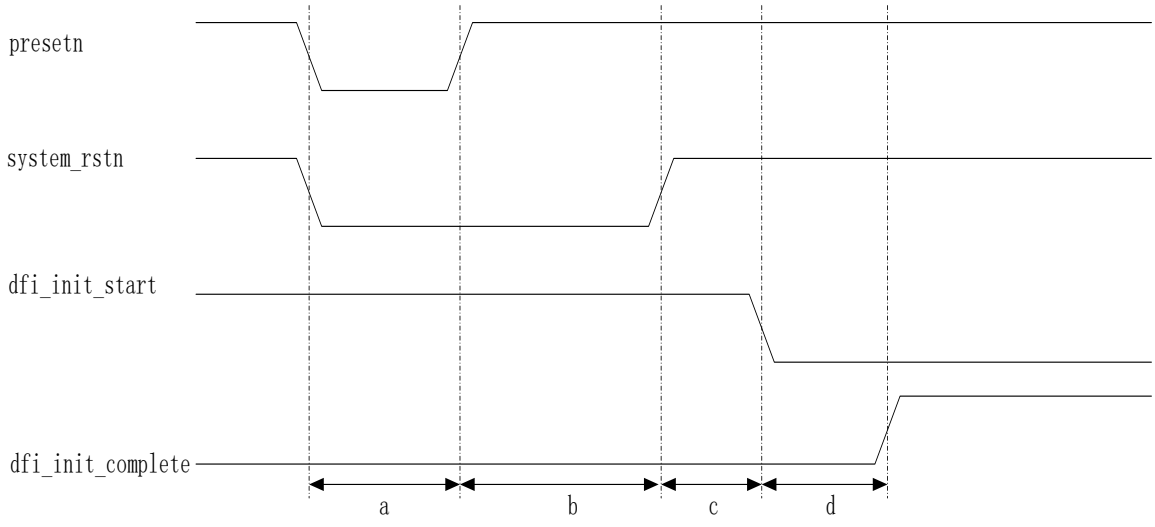


Figure 14-1 DDR system block diagram

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.2 DDR Controller Register Description

Following table lists the registers of DDR Controller. Registers are divided into two groups: AHB2 group and APB0 group, both of which are 32bit.

DDRC_AHB:

Registers access by AHB2

Base Address: *0x134F0000 ~ 0x134F0FFF*

DDRC_APB:

Registers access by APB0

Base Address: *0x13012000 ~ 0x13012FFF*

Table 14-1 DDRC Register

Name	Group	Address offset	Width	Access	Description
DSTS	DDRC_AHB	0x00	32	RW	DDR status register
DCFG	DDRC_AHB	0x08	32	RW	DDR configure register
DCTRL	DDRC_AHB	0x10	32	RW	DDR control register
DLMR	DDRC_AHB	0x18	32	RW	DDR load-mode register
DDLP	DDRC_AHB	0x20	32	RW	DFI low power handshake register
DASR_EN	DDRC_AHB	0x28	32	RW	Auto self-refresh enable register
DASR_CNT	DDRC_AHB	0x30	32	RW	Auto self-refresh counter configuration register
DREFCNT	DDRC_AHB	0x38	32	RW	Auto-refresh counter register
DTIMING1	DDRC_AHB	0x40	32	RW	DDR timing configure register 1
DTIMING2	DDRC_AHB	0x48	32	RW	DDR timing configure register 2
DTIMING3	DDRC_AHB	0x50	32	RW	DDR timing configure register 3
DTIMING4	DDRC_AHB	0x58	32	RW	DDR timing configure register 4
DTIMING5	DDRC_AHB	0x60	32	RW	DDR timing configure register 5
DMMAP0	DDRC_AHB	0x78	32	RW	DDR memory CS0 map configure register
DMMAP1	DDRC_AHB	0x80	32	RW	DDR memory CS1 map configure register
DBWMCFG	DDRC_AHB	0x88	32	RW	DDR bandwidth monitor configure

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

					register
DBWMSTP	DDRC_AHB	0x90	32	RW	DDR bandwidth monitor sample time period register
DBWP0W	DDRC_AHB	0x98	32	R	DDR bandwidth monitor port 0 write sample register
DBWP0R	DDRC_AHB	0xA0	32	R	DDR bandwidth monitor port 0 read sample register
DBWP1W	DDRC_AHB	0xA8	32	R	DDR bandwidth monitor port 1 write sample register
DBWP1R	DDRC_AHB	0xB0	32	R	DDR bandwidth monitor port 1 read sample register
DBWP2W	DDRC_AHB	0xB8	32	R	DDR bandwidth monitor port 2 write sample register
DBWP2R	DDRC_AHB	0xC0	32	R	DDR bandwidth monitor port 2 read sample register
DBWP3W	DDRC_AHB	0xC8	32	R	DDR bandwidth monitor port 3 write sample register
DBWP3R	DDRC_AHB	0xD0	32	R	DDR bandwidth monitor port 3 read sample register
HREGPRO	DDRC_AHB	0xD8	32	RW	AHB register-field protection register
DWCFG	DDRC_APB	0x00	32	RW	DDR device configure register
DREMAP1	DDRC_APB	0x08	32	RW	DDR address remapping register 1
DREMAP2	DDRC_APB	0x0C	32	RW	DDR address remapping register 2
DREMAP3	DDRC_APB	0x10	32	RW	DDR address remapping register 3
DREMAP4	DDRC_APB	0x14	32	RW	DDR address remapping register 4
DREMAP5	DDRC_APB	0x18	32	RW	DDR address remapping register 5
CPAC	DDRC_APB	0x1C	32	RW	Controller port arbiter configure register
CCHC0	DDRC_APB	0x20	32	RW	Controller port configure channel 0 register
CCHC1	DDRC_APB	0x24	32	RW	Controller port configure channel 1 register
CCHC2	DDRC_APB	0x28	32	RW	Controller port configure channel 2 register

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

CCHC3	DDRC_APB	0x2C	32	RW	Controller port configure channel 3 register
CCHC4	DDRC_APB	0x30	32	RW	Controller port configure channel 4 register
CCHC5	DDRC_APB	0x34	32	RW	Controller port configure channel 5 register
CCHC6	DDRC_APB	0x38	32	RW	Controller port configure channel 6 register
CCHC7	DDRC_APB	0x3C	32	RW	Controller port configure channel 7 register
CSCHC0	DDRC_APB	0x40	32	RW	Controller scheduler configure register 0
CSCHC1	DDRC_APB	0x44	32	RW	Controller scheduler configure register 1
CSCHC2	DDRC_APB	0x48	32	RW	Controller scheduler configure register 2
CSCHC3	DDRC_APB	0x4C	32	RW	Controller scheduler configure register 3
CMONC0	DDRC_APB	0x50	32	RW	Controller monitor configure register 0
CMONC1	DDRC_APB	0x54	32	RW	Controller monitor configure register 1
CMONC2	DDRC_APB	0x58	32	RW	Controller monitor configure register 2
CMONC3	DDRC_APB	0x5C	32	RW	Controller monitor configure register 3
CMONC4	DDRC_APB	0x60	32	RW	Controller monitor configure register 4
CCGUC0	DDRC_APB	0x64	32	RW	Controller clock gate configure register 0
CCGUC1	DDRC_APB	0x68	32	RW	Controller clock gate configure register 1
PREGPRO	DDRC_APB	0x6C	32	RW	APB register-field protection register
BUFCFG	DDRC_APB	0x70	32	RW	Controller buffer configure register

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.2.1 DSTS

DDR status register

	DSTS																DDR_AHB_BASE+0x00													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								AHB_COH_WR								Reserved									MISS	DPD	PD	AREF	SREF	CKE1	CKE0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Access
23:16	**AHB_COH_WR**: AHB coherence occurred with an AHB write followed by an AXI read. Self cleaning by reading.	R
6	**MISS**: If DCFG. MISPE is set, any dummy access, namely, access not either mapping to CS0 nor CS1, will set this bit HIGH. Self cleaning by reading.	R
5	**DPD**: If set, DDR memory is in deep power down status.	R
4	**PD**: If set, DDR memory is in power down status.	R
3	**AREF**: If set, DDR memory is in refresh status.	R
2	**SREF:** If set, DDR memory is in self refresh status.	R
1	**CKE1:** Chip select 1 enable.	R
0	**CKE0:** Chip select 0 enable.	R

14.2.2 DCFG

DDR configure register. Don't change the value on-the-fly.

	DCFG																DDR_AHB_BASE+0x08													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ROW1			COL1			BA1	Reserved								IMBA	ROW0			COL0			BA0	Reserved			TYPE			ODTEN	CS1EN	CS0EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><th>Bit</th><th>Description</th><th>Access</th></tr>
<tr><td>31:29</td><td>ROW1:
Row address configure for chip select 1.</td><td>RW</td></tr>
<tr><td>28:26</td><td>COL1:
Column address configure for chip select 1.</td><td>RW</td></tr>
<tr><td>25</td><td>BA1:
Bank address configure for chip select 1.
1: 8 bank device
0: 4 bank device</td><td>RW</td></tr>
<tr><td>16</td><td>IMBA:
0: CS0, CS1 are connected to 2 memory chips which have same ROW, COL, BA configuration. In this mode, both chips are configured by ROW0,COL0, BA0. Also ROW1,COL1 and BA1 does not affect the system configuration.
1: CS0, CS1 are connected to 2 memory chips which have different ROW, COL, BA configuration. Chip0 is configured by ROW0, COL0, BA0; Chip1 is configured by ROW1, COL1, BA1;</td><td>RW</td></tr>
<tr><td>15:13</td><td>ROW0:
Row address configure for chip select 0.</td><td>RW</td></tr>
<tr><td>12:10</td><td>COL0:
Column address configure for chip select 0.</td><td>RW</td></tr>
<tr><td>9</td><td>BA0:
Bank address configure for chip select 0.
1: 8 bank device
0: 4 bank device</td><td>RW</td></tr>
<tr><td>5:3</td><td>TYPE:
DDR memory type.
<table>
<tr><td>000</td><td>Normal SDR SDRAM (Not support).</td></tr>
<tr><td>001</td><td>Mobile SDR (Not support).</td></tr>
<tr><td>010</td><td>Normal DDR1 (Not support)</td></tr>
<tr><td>011</td><td>Mobile DDR (Not support).</td></tr>
<tr><td>100</td><td>Normal DDR2 (Not support).</td></tr>
<tr><td>101</td><td>LPDDR2/LPDDR3.</td></tr>
<tr><td>110</td><td>DDR3.</td></tr>
<tr><td>111</td><td>(Not support).</td></tr>
</table></td><td>RW</td></tr>
<tr><td>2</td><td>ODTEN:
On-die-terminate enable. Only support for</td><td>RW</td></tr>
</table>

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	DDR2, DDR3 and LPDDR3	
1	**CS1EN**: 1: Chip select 1 is in use 0: Chip select 1 is not in use	RW
0	**CS0EN**: 1: Chip select 0 is in use 0: Chip select 0 is not in use	RW

Note:

1. ROW0/1: Row address configure table.

Bit	Description	Remark
000	12-bit row address	
001	13-bit row address	
010	14-bit row address	
011	15-bit row address	
100	16-bit row address	
Others	Reserved	

2. COL0/1: Column address configure table.

Bit	Description	Remark
000	8-bit Column address.	
001	9-bit Column address	
010	10-bit Column address	
011	11-bit Column address	
100	12-bit Column address	
Others	Reserved	

14.2.3 DCTRL

DDR control register.

	DCTRL																DDR_AHB_BASE+0x10													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								DFI_RST	Reserved		PHY_RST	Reserved				ACTPD	PDTIMER			Reserved				PD_CCE	DPD	SR	SR_CCE	Reserved		CKE_HIGH	RESET
RST	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Access
23	**DFI_RST**: DFI reset.	RW
20	**PHY_RST**:	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	DDR PHY reset	
15	**ACTPD**: If set LOW, SDRAM devices will pre-charge all active banks before entering Power-Down If set HIGT, SDRAM devices will go into Power-Down mode without pre-charge all bank. active banks, some banks are still active in Power-Down mode, so called Active-Power-Down.	RW
14:12	**PDTIMER**: Power down timer. When there's no access to DDR memory for a period of time, hardware drives DDR into power-down mode to reduce power consumption. Hardware can exit Power-Down mode automatically when new access arrives. If set 0, power-down function is disabled. If set larger than 0 power-down function is enable. It is recommended to set after DDR initialization.	RW
7	**PD_CCE**: Power down clock frequency change enable.	RW
6	**DPD**: Deep power down enable. If set HIGH, hardware drives DRAM device entering Deep-Power-Down mode instead of Power-Down mode, when there's no access to DDR memory for a period of time. So you must firstly enable Power-Down mode (refer to PDT). Software needs to reset DDR controller and re-do a complete initial process to exit Deep-Power-Down mode. When DRAM device goes into Deep-Power-Down mode, it lose all data store in memory and registers.	RW
5	**SR**: Self refresh enable. If set HIGH, hardware drives DRAM device entering self-refresh mode; If set LOW, hardware drives DRAM device exiting self-refresh mode;	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	During self refresh, the clock to external DDR device would be stopped; But the clock supplied to DDR controller logic would not stop. Software can read & write DDR controller registers in this mode. Software can NOT read or write memory data in this mode. **NOTE:** Software must guarantee that there's no memory access during self-refresh mode. Otherwise, software can NOT exit this mode, **system would be hang-up!!**	
4	**SR_CCE：** Self refresh clock stop request enable. If set, DDRC request clock stop to CPM when DDR is in auto self refresh state.	RW
1	**CKE_HIGH**: Set CKE pin HIGH for one clock cycle pulse.	RW
0	**RESET**: Software reset DDR controller. Self cleaning.	RW

NOTE. 1. PDT configure table

Bit [14:13]	Description	Remark
000	power-down disabled, hardware never drive SDRAM into power-down mode.	(reset value)
001	Enter power-down after 8 tCK idle.	
010	Enter power-down after 16 tCK idle.	
011	Enter power-down after 32 tCK idle.	
100	Enter power-down after 64 tCK idle.	
101	Enter power-down after 128 tCK idle.	
110 - 111	Reserved.	

14.2.4 DLMR

DLMR register is used for initializing the DDR SDRAM memory device.

On the positive edge of START, the command selected by CMD field will be performed.

	DLMR																DDR_AHB_BASE+0x18													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDR_ADDR																				BA			CMD			tMRD					START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit 7~6, 2~1: Reserved. Writing has no effect, read as zero.
DDR_ADDR: When performing a DDR command, DDR_ADDR[13:0] corresponding to
external DDR address Pin A[13:0]; DDR_ADDR[15:14] are reserved.

Bit [31:12]	Description	Remark
0_0000	{OP[9:0]，MA[9:0] } for LPDDR2 For other DDR the low bit 14 bit corresponding to external DDR address Pin A[13:0].	(reset value)

BA: Bank Address.
When performing a DDR command, BA[2:0] corresponding to external DDR address Pin BA[2:0].

Bit [10:8]	Description	Remark
000	corresponding to external DDR address Pin BA[2:0].	(reset value)

CMD: Select command to process when setting START from low to high.
On the positive edge of START, one of the following commands will be performed.

Bit [5:3]	Description	Remark
000	Precharge one bank / All banks. (dependent field : BA, DDR_ADDR)	(reset value)
001	Auto-Refresh.	
010	Load Mode Register. (dependent field : BA, DDR_ADDR)	
011	ZQCL for DDR3 on CS0	
100	ZQCL for DDR3 on CS1	
101	ZQCS for DDR3 on CS0	
110	ZQCS for DDR3 on CS1	
101~111	Reserved.	

tMRD: Load-Mode-Register to next valid command period, cooperating with register DLMR.
tMRD defines the Load-Mode-Register to next valid command period. Delay time is tMRD*4tCK

START: Start to perform a command to external DDR memory.
The command is performed on the positive edge of START; Hardware will

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

clear START bit to zero when command issued out to external DDR memory.
Write 0 to START will be ignored and take no effect;
START=1 means hardware is busy executing current command and can NOT accept new command;
Software must check START=0 before writing 1 to START.

Bit [0]	Description	Remark
0	No command is performed.	(reset value)
1	On the positive edge of START, perform a command defined by CMD field.	

14.2.5 DDLP

DDR DFI low power handshake control register

	DDLP																DDR_AHB_BASE+0x20													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	tCTLUPD								Reserved					ONLY	UAR	UZQ	SLP				FLP				Reserved					FSR	FPD	LPEN
RST	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1

LPEN: DFI low power interface handshake enable

FPD: 1: Use fast low power handshake process during power down.
0: Use slow lp handshake process during power down.

FSR: 1: Use fast low power handshake process during self-refresh.
0: Use slow low power handshake process during self-refresh.

SLP, FLP: Slow LP handshake and fast LP handshake timing register, keep them as reset values.

ONLY, UAR, UZQ: Keep them as reset values.

tCTLUPD: Controller update delay time. Delay time is tCTLUPD x4.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.2.6 DASR_EN

Auto self refresh enable.

	DASR_EN																DDR_AHB_BASE+0x28													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															DASR_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	Access
0	**DASR_EN**: DDR auto self-refresh enable. 0: disenable auto self-refresh 1: enable auto self-refresh	RW

14.2.7 DASR_CNT

DASR: auto self-refresh. When the DDRC bus interface is idle for some time, the DDRC can issue a command to put the DRAM into self-refresh mode. This will save much power in off-chip DRAM.

	DASR_CNT																DDR_AHB_BASE+0x30													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	tRFC								Reserved				DASR_CNT																			
RST	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Description	ACCESS
31:24	**tRFC**: Refresh to Next vaild command counter. Indicate how many tRFC*2 cycles after a Refresh command can next valid command issued	RW
19:0	**DASR_CNT**: DDR auto self-refresh counter. When the bus interface is idle(all transfer are finished), the internal timer is going to run, after the counter value is meet, DDR start self-refresh	RW

tRFC: AUTO-REFRESH command period.
tRFC defines the minimum delay after an AUTO-REFRESH command.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

During tRFC period, no command can be issued to DDR memory.
Delay Time = (**2 * tRFC)tCK**

14.2.8 DREFCNT

DDR Auto-Refresh Counter.

	DREFCNT																DDR_AHB_BASE+0x38													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PBREF_EN	PREREF_EN	Reserved						CON								CNT								PREREF_CNT				CLK_DIV			REF_EN
RST	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

CON: A constant value used to compare with the CNT value.
After reset, CON=0xFF and CNT=0x00;
It is not recommended to set CON=0x00.

CNT: 8-bit counter; When the value of CNT match the value of CON, an auto-refresh command will be issued to DRAMs. READ only.

PREREF_CNT: 4-bit counter; If PREREF_EN is set, PREREF_CNT indicates the pre-refresh command number can be issued for PULLING-IN refresh condition, which may increase DRAM useful bandwidth. More information please refer to JEDEC specifications.

CLK_DIV : Clock Divider.
Divide the dclk to generate a lower frequency of clock to drive the auto-refresh counter. This helps to save power consumption.
Set CLK_DIV=0 can disable the clock to auto-refresh counter.
dclk is CKO clock, When ddr work in 500Mbps, dclk is 250Mhz.

Bit [3:1]	Description	Remark
000	dclk / 16.	(reset value)
001	dclk / 32.	
010	dclk / 64.	
011	dclk / 128.	
100	dclk / 256.	
101	dclk / 512.	
110	dclk / 1024.	
111	Reserved	

REF_EN: Enable Refresh Counter.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Software set REF_EN=1 right after initialize ddr memory.

Bit [0]	Description	Remark
0	Enable auto-refresh counter.	(reset value)
1	Disable auto-refresh counter.	

PREREF_EN: PULLING-IN refresh enable; If set, extra refresh command will be issued when DDR controller in is idle state, and when not idle, refresh commands can be hided to increase DRAM useful bandwidth. More information please refer to JEDEC specifications. This function is only designed for DDR3, LPDDR2 and LPDDR3.

PBREF_EN: Enable per-bank refresh, only support LPDDR2/3.

.

Bit [24]	Description	Remark
0	Disenable per-bank refresh.	(reset value)
1	Enable per-bank refresh counter.	

14.2.9 DTIMING1

DDR timing configure register.

	DTIMMING1																DDR_AHB_BASE+0x40													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		tWRLAT						Reserved		tWTR						Reserved		tWR						Reserved		tWL					
RST	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1

tWRLAT: DFI interface write command to write enable latency, defined as tphy_wrlat in DFI specification. Recommended setting is tWL-1(when use LPDDR2/3, set tWDLAT=tWL).

tWTR: Write command to read command delay.

SDRAM type	Definition in JEDEC spec.
DDR3	tWTR = tWL + tCCD + tWTRinternal
LPDDR2/3	tWTR = tWL + tCCD + tWTRinternal + 1

Note. "RU" means round up. tWTRinternal is defined by JEDEC specification.

tWR: WRITE recovery delay.

tWL: Write latency, write command to write data delay.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.2.10 DTIMING2

DDR timing configure register.

	DTIMMING2																DDR_AHB_BASE+0x48													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		tRDLAT						Reserved		tRTW						Reserved		tRTP						Reserved		tRL					
RST	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1

tRDLAT: DFI interface read command to read enable latency, defined as trdata_en in DFI specification. Recommended setting is tRL-2. (when use LPDDR2, set tRDLAT=tRL-2).

tRTW: Read command to write command latency.
Value is defined below:

SDRAM type	Definition in JEDEC spec.
DDR3	tRTW = tRL + tCCD + 2 - tWL
LPDDR2/3	tRTW = tRL + tCCD + RU(tDQSCK/tCK) + 1 - tWL

Note. "RU" means round up.

tRTP: READ to PRECHARGE command delay.

tRL: Read latency, read command to read data delay.

14.2.11 DTIMING3

DDR timing configure register.

	DTIMMING3																DDR_AHB_BASE+0x50													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					tEXTRW			Reserved		tRCD						Reserved		tCCD						Reserved		tRP					
RST	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1

tEXTRW: External clock add for read to read, or write to write from one chip select the other.

tRCD: ACTIVE to READ or WRITE command period.
tRCD defines the ACTIVE to READ/WRITE command period to the same bank.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

tCCD: CAS to CAS command delay.

tRP: PRECHARGE command period

tRP defines the PRECHARGE to next command period to the same bank.

14.2.12 DTIMING4

DDR timing configure register.

DTIMING4																															DDR_AHB_BASE+0x58
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	tFAW								Reserved	tRC							Reserved	tRAS								Reserved	tRRD						
RST	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0

tFAW: Four-active command window.

tRC: ACTIVE to ACTIVE command delay to the same bank.

tRAS: ACTIVE to PRECHARGE command delay to the same bank.

tRRD: ACTIVE bank A to ACTIVE bank B command delay.

14.2.13 DTIMING5

DDR timing configure register.

DTIMMING5																															DDR_AHB_BASE+0x60
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	tXS								tCKESR								tCKSRE				Reserved				tXP				tCKE			
RST	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	1	0	0	1	0

tXS: Exit self-refresh to READ command delay. Definition is shown in the chart below:

SDRAM type	Definition in JEDEC spec.
DDR3	tXSDLL
LPDDR2/3	tXSR

Delay time is **tXS*4 (tCK)**

Note: You can set this registers as tXS(or tXSNR), but must make sure the system do not read DDR before tXS in wakeup.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

tCKESR: Minimum Self-Refresh time.

After DDR memory turns into Self-Refresh mode, it will NOT exit until tCKESR delay meets.

SDRAM type	Definition in JEDEC spec.
DDR3	tCKESR
LPDDR2/3	tCKESR

tCKSRE: Valid clock after enter self-refresh(tCKSRX = tCKSRE in this version).

For LPDDR2, 4 tCK is recommended.

For DDR3, please refer to JEDEC spec.

tXP: EXIT-POWER-DOWN to next valid command delay.

Value is defined below:

SDRAM type	Definition in JEDEC spec.
DDR3	tXP (active power down mode, or precharged power down mode with power down DLL-on) tXPDLL (precharged power down mode with power down DLL-off)
LPDDR2/3	tXP

Note: Power down DLL on/off is set by MR0 register A12 bit. More detail refer to JEDEC specification.

tCKE: minimum CKE pulse width when CKE goes HIGH for EXIT-POWER-DOWN.

tCKE define the minimum CKE pulse width, include high level and low level.

14.2.14 DMMAP0/1

DDR Memory Map Configure Register

The physical base address and size of external DDR Memory can be configured by DMMAP register.

The size of external DDR Memory must be: **2^(24+n), n=0, 1, 2, 3, ….**

When the following equation is met:

(BUS_ADDRESS[31:24] & MASK[7:0]) == BASE

The DDR Memory is selected.

	DMMAP0/1																DDR_AHB_BASE+0x78/80															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																BASE								MASK							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits 31~16: Reserved. Writing has no effect, read as zero.
BASE: base address.
MASK: address mask.
Examples:

Memory capacity : 0x0000_0000 ~ 0x3FFF_FFFF (512MB x 2)
Chip select : 2

BASE	MASK	Chip select 0 memory space	Chip select 1 memory space
CS0: 0x00	CS0: 0x20	0x0000_0000 ~ 0x1FFF_FFFF	0x2000_0000 ~ 0x3FFF_FFFF
CS1: 0x20	CS1: 0x20		

14.2.15 DBWCFG

DDR bandwidth monitor configure register.

	DBWCFG																DDR_AHB_BASE+0x88															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												BW_DONE	BW_INT_EN	BW_CLR	BW_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	ACCESS
3	**BW_DONE**: DDR bandwidth sample done.	R
2	**BW_INT_EN**: DDR bandwidth sample done interrupt enable. If set, an interrupt would raise after DDR bandwidth sample done.	RW
1	**BW_CLR**: DDR bandwidth sample data clear. If set, all the sample data would be cleared. This bit is self-clear.	RW
0	**BW_EN**: DDR bandwidth sample enable. If set, bandwidth sample will start, and if clear, bandwidth sample will stop.	RW

14.2.16 DBWSTP

DDR bandwidth monitor configure register.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	DBWCFG																DDR_AHB_BASE+0x90															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBWSTP																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	ACCESS
31:0	**DBWSTP**: DDR bandwidth sample time period. If set, bandwidth sample will stop after this counter counts to zero.	RW

14.2.17 DBWP0W/R

DDR bandwidth monitor port 0 write sample register.

	DBWP0W																DDR_AHB_BASE+0x98															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBWP0W																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	ACCESS
31:0	**DBWP0W**: Write package number for port 0.	R

DDR bandwidth monitor port 0 write sample register.

	DBWP0R																DDR_AHB_BASE+0xA0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBWP0R																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	ACCESS
31:0	**DBWP0R**: Read package number for port 0.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.2.18 DBWP1W/R

DDR bandwidth monitor port 1 write sample register.

	DBWP1W																DDR_AHB_BASE+0xA8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBWP1W																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	ACCESS
31:0	**DBWP1W**: Write package number for port 1.	R

DDR bandwidth monitor port 1 write sample register.

	DBWP1R																DDR_AHB_BASE+0xB0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBWP1R																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	ACCESS
31:0	**DBWP1R**: Read package number for port 1.	R

14.2.19 DBWP2W/R

DDR bandwidth monitor port 2 write sample register.

	DBWP2W																DDR_AHB_BASE+0xB8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBWP2W																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	ACCESS
31:0	**DBWP2W**: Write package number for port 2.	R

DDR bandwidth monitor port 2 write sample register.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	DBWP2R																DDR_AHB_BASE+0xC0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBWP2R																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	ACCESS
31:0	**DBWP2R**: Read package number for port 2.	R

14.2.20 DBWP3W/R

DDR bandwidth monitor port 3 write sample register.

	DBWP3W																DDR_AHB_BASE+0xC8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBWP3W																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	ACCESS
31:0	**DBWP3W**: Write package number for port 3.	R

DDR bandwidth monitor port 3 write sample register.

	DBWP3R																DDR_AHB_BASE+0xD0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBWP3R																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	ACCESS
31:0	**DBWP3R**: Read package number for port 3.	R

14.2.21 HREGPRO

AHB bus register protection.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	HREGPRO																DDR_AHB_BASE+0xD8													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RESERVED																														HUNPRO_WR	HPRO_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Access
1	**HUNPRO_WR**: AHB bus register un-protected write flag. 1: un-protected register write occurred; 0: un-protected register write not occurred; Note: this bit will clear when writing.	R
0	**HPRO_EN**: AHB bus register protection enable. 1: un-protected register write occurred; 0: un-protected register write not occurred; Note: it is recommended to set this bit after DDR controller configuration.	RW

14.2.22 DBGEN

AHB bus debug enable.

	DBGEN																DDR_AHB_BASE+0xE0													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RESERVED																															DBGEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Description	Access
1	**DBGEN**: AHB bus debug enable: 1: Enable debug logic works; 0: Disenable debug logic; Note: for power consuming consideration, it is recommended to disenable this bit before normal work.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.2.23 DBGINFO

AHB bus debug information.

	DBGINFO																DDR_AHB_BASE+0xE8													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBGINFO																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Access
31:0	**DBGINFO**: AHB bus debug information.	R

14.2.24 DWCFG

DDR device data width configure register

	DWCFG																DDR_APB_BASE+0x00															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											PHY_PD	DFI_INIT_START	FREQ_EXIT	SUBREMAP	DW
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Access
4	**PHY_PD:** DDR PHY power down. 1: the PHY is in power down status 0: the PHY is in power on status	RW
3	**DFI_INIT_START:** Control bit of dfi_init_start. 1: set dfi_init_start HIGH 0: set dfi_init_start LOW	RW
2	**FREQ_EXIT:** Control bit to exit device out of frequency change flow. 1: set controller out of frequency change flow 0: clear this bit	RW
1	**SUBREMAP:** Sub-remap logic enable.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	1: enable the sub-remap logic 0: disenable the sub-remap logic **Note: don't change the value of this register after initialization.**	
0	**DW**: DDR device data width configure 1: 32 bit data width DRAM (default) 0: 16 bit data width DRAM **Note: don't change the value of this register after initialization.**	RW

14.2.25 DWSTATUS

DDR device status register

	DWSTATUS																DDR_APB_BASE+0x04																
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											DRAM_SR	FREQ_PHY_DONE	FREQ_DDR_DONE	PHY_PLLLOCK	DFI_INIT_COMPLETE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Access
4	**DRAM_SR:** Flag bit when DRAM is in self-refresh status. 1: DRAM is in self-refresh status 0: DRAM is not in self-refresh status	R
3	**FREQ_PHY_DONE:** Flag bit when PHY finished frequency change. 1: PHY finished frequency change 0: PHY still in frequency change	R
2	**FREQ_DDR_DONE:** Flag bit when controller finished frequency change. 1: controller finished frequency change 0: controller still in frequency change	R
1	**PHY_PLL_LOCK:** DDR PHY PLL lock flag.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	1: the PLL is lock 0: the PLL isn't lock	
0	**DFI_INIT_COMPLETE:** Flag of dfi_init_complete.	R

14.2.26 DREMAP1/2/3/4/5

DDR Address Remapping Register 1/2/3/4/5

	DREMAP1																**DDR_APB_BASE+0x08**													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			BIT3MP					Reserved			BIT2MP					Reserved			BIT1MP					Reserved			BIT0MP			
RST	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	DREMAP2																**DDR_APB_BASE+0x0C**													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			BIT7MP					Reserved			BIT6MP					Reserved			BIT5MP					Reserved			BIT4MP			
RST	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0

	DREMAP3																**DDR_APB_BASE+0x10**													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			BIT11MP					Reserved			BIT10MP					Reserved			BIT9MP					Reserved			BIT8MP			
RST	0	0	0	0	1	0	1	1	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0

	DREMAP4																**DDR_APB_BASE+0x14**													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			BIT15MP					Reserved			BIT14MP					Reserved			BIT13MP					Reserved			BIT12MP			
RST	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	0	0	0	0	0	1	1	0	1	0	0	0	0	1	1	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	DREMAP5																DDR_APB_BASE+0x18															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			BIT19MP					Reserved			BIT18MP					Reserved			BIT17MP					Reserved			BIT16MP				
RST	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0

DREMAP1~5 are used to define address mapping in DDRC. The “BITnMP” represents address[31:20]. The low 4KB(bit [11:0]) address are reserved without any change. The high 20 bits are configurable. For example, If you want to remap address between address[27:25] and address[14:12], you can set BIT12MP as 0, BIT13MP as 1, BIT14MP as 2, BIT0MP as 12, BIT1MP as 13 and BIT2MP as 14.

Original address:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11~0
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Reserved

Remapped address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11~0
19	18	17	16	2	1	0	12	11	10	9	8	7	6	5	4	3	15	14	13	Reserved

14.2.27 CPAC

Controller port arbiter configure register.

	CPAC																DDR_APB_BASE+0x1C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																			DYN_WR_CFG								FIX_WR_CNT				FIX_WR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	0	0	0

Bit	Description	Access
12:5	**DYN_WR_CFG**: Dynamic write/read arbitration configure. Keep it 0xAA as the default value.	RW
4:1	**FIX_WR_CNT**: Fix write/read arbitration counter.	RW
0	**FIX_WR**: Port arbiter deal with write/read request in a fixed mode. If set HIGH, write/read request arbitration is done by a fixed number set in CPAC.FIX_WR_CNT.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.2.28 CCHC0/1/2/3/4/5/6/7

Controller channel configure 0.

	CCHC0/1/2/3/4/5/6/7																DDR_APB_BASE+0x20~ 0x3C											
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WTR_TIMEOUT				RTR_TIMEOUT				BW_LIMIT_WCNT								BW_LIMIT_RCNT								BW_LIMIT_WEN	BW_LIMIT_REN	TR_QOS_COMP		TR_FIX_PRI		TR_FIX_PRI_EN	PORT_PRI
RST	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Access
31:28	**WTR_TIMEOUT**: Write transaction pending timeout value. If the transaction is valid but not granted by the arbiter, the timeout counter starts to counter down. As soon as the counter counts to 0, its priority raise. The smaller this value is, the sooner the transaction get higher priority. Note: the actual timeout value is (WTR_TIMEOUT)*4.	RW
27:24	**RTR_TIMEOUT**: Read transaction pending timeout value. If the transaction is valid but not granted by the arbiter, the timeout counter starts to counter down. As soon as the counter counts to 0, its priority raise. The smaller this value is, the sooner the transaction get higher priority. Note: the actual timeout value is (RTR_TIMEOUT)*4.	RW
23:16	**BW_LIMIT_WCNT**: Port bandwidth limit counter for write channel.	RW
15:8	**BW_LIMIT_RCNT**: Port bandwidth limit counter for read channel.	RW
7	**BW_LIMIT_WEN**: Port bandwidth limit enable for write channel.	RW
6	**BW_LIMIT_REN**: Port bandwidth limit enable for read channel.	RW
5:4	**TR_QOS_COMP:** Transaction qolity of service compress value.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	00: the lowest quality of service priority. 01: the lower quality of service priority. 10: normal quality of service priority. 11: the higher quality of service priority.	
3:2	**TR_FIX_PRI**: Transaction fixed priority value.	RW
1	**TR_FIX_PRI_EN**: Transaction fixed priority mode enable. By default, transaction priority depends on the AR/WQOS signal, which is controlled by hardware. If set, this priority will be replaced by the value of CCHCx.TR_FIX_PRI.	RW
0	**PORT_PRI**: Port priority. 1. This port is in high priority. All the access from this port share this priority. 0. This port is in low priority.	RW

14.2.29 CSCHC0

Controller scheduler configure register 0.

	CSCHC0																DDR_APB_BASE+0x40													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								BYPASS1_EN	BYPASS_PORT1			BYPASS_ID1				BYPASS0_EN	BYPASS_PORT0			BYPASS_ID0											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Access
31:24	**ENTRY_TIMEOUT_CNT**: The timeout counter for each entry.	RW
23	**BYPASS1_EN**: 1. The specific transaction using BYPASS_ID1 as ID in port BYPASS_PORT1, will automatically get bypass permission. 0. This bypass permission is closed.	RW
22:20	**BYPASS_PORT1**: If the enable control is set HIGH, these bits correspond to the port number.	RW
19:12	**BYPASS_ID1**:	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	If the enable control is set HIGH, these bits correspond to the ID within transactions.	
11	**BYPASS0_EN**: 1. The specific transaction using BYPASS_ID0 as ID in port BYPASS_PORT0, will automatically get bypass permission. 0. This bypass permission is closed.	RW
10:8	**BYPASS_PORT0**: If the enable control is set HIGH, these bits correspond to the port number.	RW
7:0	**BYPASS_ID0**: If the enable control is set HIGH, these bits correspond to the ID within transactions.	RW

14.2.30 CSCHC1

Controller scheduler configure register 1.

	CSCHC1																DDR_APB_BASE+0x44													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCH_ENTRY_QOS_CFG																															
RST	1	1	1	1	1	1	1	0	1	1	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1	0	0	1	0	0

Bit	Description	Access
31:0	**SCH_ENTRY_QOS_CFG**: Scheduler entry QoS configuration. Keep it 0xFEF9F9E4 as default value.	RW

14.2.31 CSCHC2

Controller scheduler configure register 2.

	CSCHC2																DDR_APB_BASE+0x48													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCH_ENTRY_TIMEOUT						SCH_WR_CNT						SCH_WR_ARB_CFG																			
RST	1	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	1	1	1	0	1	0	0	0	1	1	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	Description	Access
31:26	**SCH_ENTRY_TIMEOUT**: Scheduler entry pending timeout value. Keep it 0x21 as default value.	RW
25:22	**SCH_WR_CNT**: Scheduler write/read arbiter Schmitt trigger counter. Keep it 0x4as default value. **Note:** the real counter value is 4x times larger.	RW
21:0	**SCH_WR_ARB_CFG**: Scheduler write/read arbiter Schmitt trigger counter. Keep it 0x107460 as default value.	RW

14.2.32 CSCHC3

Controller scheduler configure register 3.

	CSCHC3																DDR_APB_BASE+0x4C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										WRMIN						Reserved										WRMAX					
RST	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit	Description	Access
21:16	**WRMIN**: The min write transactions pending in scheduler. Keep it 0x10 as default value.	RW
5:0	**WRMAX**: The max write transactions pending in scheduler. Keep it 0x20 as default value.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.2.33 CMONC0

Controller monitor configure register 0.

	CMONC0																DDR_APB_BASE+0x50													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RESERVED																CMON-ID														CMON_END_POLL	CMON_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0

Bit	Description	Access
15:4	**CMON_ID** Every 3bit indicate a channel number to monitor Default value：channel 6（cpu）， 3（dpu），1（isp）， 0（msc）	R
1	**CMON_END_POLL**: Controller internal bandwidth monitor end polling flag.	R
0	**CMON_EN**: Controller internal bandwidth monitor enable.	RW

Note:

The steps for using controller internal bandwidth monitor is:

1. Get a sequential memory space to store the monitor data.
2. Set CMONC1.CMON_START_ADDR as the beginning of the memory space.
3. Set CMONC2.CMON_END_ADDR as the ending of the memory space.
4. Set CMONC3 to configure the bandwidth that want to sample.
5. Set CMONC4.CMON_SAMPLE_PERIOD as the sample period.
6. Set CMONC0.CMON_EN to trigger the monitor.
7. Poll CMONC0.CMON_END_POLL to know whether the sample come to end.

14.2.34 CMONC1

Controller monitor configure register 1.

	CMONC1																DDR_APB_BASE+0x54													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMON_START_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	Description	Access
31:0	**CMON_START_ADDR**: Controller internal bandwidth monitor start address.	RW

14.2.35 CMONC2

Controller monitor configure register 2.

	CMONC2																DDR_APB_BASE+0x58															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMON_END_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Access
31:0	**CMON_END_ADDR**: Controller internal bandwidth monitor end address.	RW

14.2.36 CMONC3

Controller monitor configure register 3.

	CMONC3																DDR_APB_BASE+0x5C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RESERVED																												CMON_PB_EN	CMON_EB_EN	CMON_IB_EN	CMON_RB_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Access
3	**CMON_PB_EN**: Controller internal bandwidth monitor sample per-bank bandwidth enable.	RW
2	**CMON_EB_EN**: Controller internal bandwidth monitor sample efficient bandwidth enable.	RW
1	**CMON_IB_EN**: Controller internal bandwidth monitor sample	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	idle bandwidth enable.	
0	**CMON_RB_EN**: Controller internal bandwidth monitor sample real bandwidth enable.	RW

14.2.37 CMONC4

Controller monitor configure register 4.

	CMONC4																DDR_APB_BASE+0x60															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MON_PERIOD																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Access
31:0	**MON_PERIOD**: Controller monitor sample period, counted in cycle.	RW

14.2.38 CCGUC0

Controller clock gate unit configure 0.

	CCGUC0																DDR_APB_BASE+0x64															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CGU_PORT7				CGU_PORT6				CGU_PORT5				CGU_PORT4				CGU_PORT3				CGU_PORT2				CGU_PORT1				CGU_PORT0			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Access
31:28	**CGU_PORT7**: Clock gate unit for port 7. 0xF: Clock gate enable; 0x0: Clock gate disenable; Note: do not change this on-the-fly.	RW
27:24	**CGU_PORT6**: Clock gate unit for port 6. 0xF: Clock gate enable; 0x0: Clock gate disenable; Note: do not change this on-the-fly.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

23:20	**CGU_PORT5**: Clock gate unit for port 5. 0xF: Clock gate enable; 0x0: Clock gate disenable; Note: do not change this on-the-fly.	RW
19:16	**CGU_PORT4**: Clock gate unit for port 4. 0xF: Clock gate enable; 0x0: Clock gate disenable; Note: do not change this on-the-fly.	RW
15:12	**CGU_PORT3**: Clock gate unit for port 3. 0xF: Clock gate enable; 0x0: Clock gate disenable; Note: do not change this on-the-fly.	RW
11:8	**CGU_PORT2**: Clock gate unit for port 2. 0xF: Clock gate enable; 0x0: Clock gate disenable; Note: do not change this on-the-fly.	RW
7:4	**CGU_PORT1**: Clock gate unit for port 1. 0xF: Clock gate enable; 0x0: Clock gate disenable; Note: do not change this on-the-fly.	RW
3:0	**CGU_PORT0**: Clock gate unit for port 0. 0xF: Clock gate enable; 0x0: Clock gate disenable; Note: do not change this on-the-fly.	RW

14.2.39 CCGUC1

Controller clock gate unit configure1.

	CCGUC1																DDR_APB_BASE+0x68													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ASYN_SEL								AHB_COH_PROT	RESERVED														CGU_BWM	CGU_PCTRL				CGU_SCH			CGU_PA
RST	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	Description	Access
31:24	**ASYN_SEL**: Asynchronous selection for each port. 1: 3-registers asynchronous; 0: 2-registers asynchronous; Note: do not change this on-the-fly.	RW
23	**AHB_COH_PROT**: AHB port write-read coherence protection enable. If set, any coherence situation between an AHB write followed by an AXI read will be protected. Also, this will be recorded to **DSTS.**	RW
8	**CGU_BWM**: Clock gate unit for bandwidth monitor. 1: Clock gate enable; 0: Clock gate disenable; Note: do not change this on-the-fly.	RW
7:4	**CGU_PCTRL**: Clock gate unit for p-controller. 0xF: Clock gate enable; 0x0: Clock gate disenable; Note: do not change this on-the-fly.	RW
3:1	**CGU_SCH**: Clock gate unit for scheduler. 0x7: Clock gate enable; 0x0: Clock gate disenable; Note: do not change this on-the-fly.	RW
0	**CGU_PA**: Clock gate unit for port arbiter. 1: Clock gate enable; 0: Clock gate disenable; Note: do not change this on-the-fly.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.2.40 PREGPRO

APB bus register protection.

PREGPRO																DDR_APB_BASE+0x6C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RESERVED																														PUNPRO_WR	PPRO_EN
RST	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Access
1	**PUNPRO_WR**: APB bus register un-protected write flag. 1: un-protected register write occurred; 0: un-protected register write not occurred; Note: this bit will clear when writing.	R
0	**PPRO_EN**: APB bus register protection enable. 1: un-protected register write occurred; 0: un-protected register write not occurred; Note: it is recommended to set this bit after DDR controller configuration.	RW

14.2.41 BUFCFG

DRAM controller internal buffer configure register.

BUFCFG																DDR_APB_BASE+0x70													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BUF_ADDR																											RESERVED				BUF_EN
RST	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Access
31:5	**BUF_ADDR**: DRAM controller internal buffer address configure.	RW
0	**BUF_EN**: DRAM controller internal buffer. 1: buffer is enable; 0:buffer is disenable;	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.3 DDR PHY Register Description

Note： PHY registers aligned in byte

Following table lists the registers of DDR PHY..

PHY_APB:

Registers access by APB0

Base Address: *0x13011000 ~ 0x13011FFF*

Table 14-2 PHY Registers Address Mapping

Name	Group	Address offset	Width	Access	Description
PHY_RST	DDRP_APB	0x000	8	RW	RHY reset register
MEM_CFG	DDRP_APB	0x004	8	RW	Memory configure register
TRAIN_CTRL	DDRP_APB	0x008	8	RW	Training control register
WL_MODE1	DDRP_APB	0x00c	8	RW	Write leveling load mode1 register
WL_MODE2	DDRP_APB	0x010	8	RW	Write leveling load mode2 register
CL	DDRP_APB	0x014	8	RW	CL register
AL	DDRP_APB	0x018	8	RW	AL register
CWL	DDRP_APB	0x01c	8	RW	CWL register
CMD_NRCOMP	DDRP_APB	0x040	8	RW	CMD NRCOMP register
CMD_PRCOMP	DDRP_APB	0x044	8	RW	CMD PRCOMP register
CK/CKB_NRCOMP	DDRP_APB	0x048	8	RW	CK/CKB NRCOMP register
CK/CKB_NRCOMP	DDRP_APB	0x04c	8	RW	CK/CKB PRCOMP register
PU/PD	DDRP_APB	0x050	8	RW	CMD weak pull up/down register
CMD_DLL	DDRP_APB	0x054	8	RW	CMD DLL register
CK_DLL	DDRP_APB	0x058	8	RW	CMD CK DLL register

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

DFILP_RESP	DDRP_APB	0x060	8	RW	Response timing register
DQ_WIDTH	DDRP_APB	0x07c	8	RW	DQ Width register
PLL_FBDIV	DDRP_APB	0x080	8	RW	PLL feed back divider register
PLL_CTRL	DDRP_APB	0x84	8	RW	PLL control register
PLL_PDIV	DDRP_APB	0x088	8	RW	PLL divider register
WL_DONE	DDRP_APB	0x0c0	8	R	PHY write-leveling done register
PLL_LOCK	DDRP_APB	0x0c8	8	R	PLL lock register
CALIB_DONE	DDRP_APB	0x0cc	8	R	Calibration done register
INIT_COMP	DDRP_APB	Oxd0	8	R	PHY initialize complete
PHY_BIST	DDRP_APB	Oxd8	8	R	The bist complete flag and the bist result

14.3.1 DDR PHY RST

																										PHY_APB_BASE+0x000						
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												SRST1	SRST0	Reserved	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bits	Name	Description	RW
[3]	SRST1	soft reset digital core, active low	RW
[2]	SRST0	soft reset analog core, active low	RW

14.3.2 DDR PHY MEM_CFG

																								MEM_CFG				PHY_APB_BASE+0x004			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											BSTSEL	Reserved		MEMSEL	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
[4]	BSTSEL	Burst select calibration 0: Reserved 1: burst8	RW
[1:0]	MEMSEL	memory select 3: LPDDR2 2: LPDDR3	RW

14.3.3 DDR PHY TRAINING_CTRL

	TRAINING_CTRL																PHY_APB_BASE+0x008															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												WLBYPASS	WLCTRL	DSCSE	DSACE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Name	Description	RW
[3]	WLBYPASS	Write leveling calibration bypass mode, active high	RW
[2]	WLCTRL	Write leveling calibration control, active high	RW
[1]	DSCSE	DQS gating calibration bypass mode, active high 1:register bypass mode 0:no bypass mode	RW
[0]	DSACE	DQS gating calibration control, active high	RW

14.3.4 DDR PHY WL_MODE1

	WL_MODE1																PHY_APB_BASE+0x00c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								WLMDL							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[7:0]	WLMDL	write leveling load mode [7:0]. Related to the register TRAIN_CTRL[2].	WR

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.3.5 DDR PHY WL_MODE2

	WL_MODE2																PHY_APB_BASE+0x010													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								WLMDS		WLMDH					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[7:6]	WLMDS	write leveling load mode select[1:0]. Related to the register TRAIN_CTRL[2].	WR
[5:0]	WLMDH	write leveling load mode [13:8]. Related to the register TRAIN_CTRL[2].	WR

14.3.6 DDR PHY CL

	CL																PHY_APB_BASE+0x014													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												CL			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Name	Description	RW
[3:0]	CL	LPDDR3/2 CAS Read Latency Note: When the phy choose the LPDDR3/2 mode, this value should keep the same value to the value of the SDRAM RL.	RW

14.3.7 DDR PHY AL

	AL																PHY_APB_BASE+0x018													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												AL			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[3:0]	AL	LPDDR3/2 Additional Latency Note: Please keep zero when the phy choose the LPDDR3/2.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.3.8 DDR PHY CWL

	CWL																PHY_APB_BASE+0x01c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												CWL			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[3:0]	CWL	LPDDR3/2 CAS Write Latency Note: When the phy choose the LPDDR3/2 mode, this value should keep the same with WL.	RW

14.3.9 DDR CMD NRCOMP

																	PHY_APB_BASE+0x040															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												CMD_NRCOMP			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	RW
[3:0]	CMD_NRCOMP	CMD NRCOMP, except for CK/CKB. The larger the value, the stronger the drive strength	RW

14.3.10 DDR CMD PRCOMP

																	PHY_APB_BASE+0x044															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												CMD_PRCOMP			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	RW
[3:0]	CMD_PRCOMP	CMD PRCOMP, except for CK/CKB. The larger the value, the stronger the drive strength	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.3.11 DDR CK/CKB NRCOMP

PHY_APB_BASE+0x048

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												CK_NRCOMP			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	RW
[3:0]	CK_NRCOMP	CK/CKB NRCOMP. The larger the value, the stronger the drive strength	RW

14.3.12 DDR CK/CKB PRCOMP

PHY_APB_BASE+0x04c

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												CK_PRCOMP			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	RW
[3:0]	CK_PRCOMP	CK/CKB PRCOMP. The larger the value, the stronger the drive strength	RW

14.3.13 DDR Weak Pull Up/Down

PHY_APB_BASE+0x050

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														CMDWPU	CMDWPD
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
[1]	CMDWPU	CMD weak pull up enable, active high	RW
[0]	CMDWPD	CMD weak pull down enable, active high	RW

14.3.14 DDR CMD DLL

PHY_APB_BASE+0x054

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												CMDDLL_en	CMDDLL_delay		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Name	Description	RW
[3]	CMDDLL_en	CMD DLL Enable	RW
[2:0]	CMDDLL_delay	CMD DLL delay 0: no delay 1: 22.5° delay 2: 45° delay 3: 67.5° delay 4: 90° delay 5: 112.5° delay 6: 135° delay 7: 157.5° delay	RW

14.3.15 DDR CK DLL

PHY_APB_BASE+0x058

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												CKDLL_Phase	CKDLL_Delay		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[3]	CKDLL_Phase	CK DLL clock phase select in bypass mode 0: no delay 1: 90 degree	RW
[2:0]	CKDLL_Delay	CK DLL delay 0: no delay 1: 22.5° delay 2: 45° delay 3: 67.5° delay 4: 90° delay 5: 112.5° delay 6: 135° delay 7: 157.5° delay	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.3.16 DDR DFI LP Response Timing

PHY_APB_BASE+0x060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								Resptm_ack				Resptm_req			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Name	Description	RW
[7:4]	Resptm_ack	The response timing when high the dfi_lp_ack. Unit: dfi_clk1x.	RW
[3:0]	Resptm_req	The response timing when detect the dfi_lp_req is high. Unit: dfi_clk1x.	RW

14.3.17 DDR DQ Width

PHY_APB_BASE+0x07c

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														DQWidth	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	RW
[1:0]	DQWidth	The DQ width select signal. 2'h3: 16bit 2'h1: 8bit	RW

14.3.18 DDR PLL Feedbackdive

PHY_APB_BASE+0x080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								PLL_FbdivL							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
[7:0]	PLL_FbdivL	PLL Feedbackdivide [7:0] (fbdiv[7:0]). It combines with register 0x024[1] to generate the fbdiv[8:0]. Note: fbdiv >=8.	RW

14.3.19 DDR PLL PowerDown Enable

PHY_APB_BASE+0x084

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														PLL_PowDown	PLL_FbdivH
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

Bits	Name	Description	RW
[31:2]	Reserved		
[1]	PLL_PowDown	PLL power down enable 1: power down 0: power up.	RW
[0]	PLL_FbdivH	PLL Feedbackdivide [8].	RW

14.3.20 DDR PLL Post Divide

PHY_APB_BASE+0x088

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								PLL_postdiv			PLL_prediv				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Name	Description	RW
[31:8]	Reserved		
[7:5]	Pll_postdiv	PLL Post-divide(postdiv[2:0])	RW
[4:0]	Pll_prediv	PLL Pre-divide(prediv[4:0])	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.3.21 DDR Write Leveling Complete

PHY_APB_BASE+0x0c0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														WL_done	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[1:0]	WL_done	The Write leveling complete signal. [0]: The complete flag of left channel A. High valid. [1]: The complete flag of right channel A. High valid	R

14.3.22 DDR PHY PLL_LOCK

PLL_LOCK PHY_APB_BASE+0x0c8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												PLL_LOCK	Reserved		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[3]	PLL_LOCK	PLL lock signal. High is valid.	R

14.3.23 DDR PHY CALIB_DONE

CALIB_DONE PHY_APB_BASE+0x0cc

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														HDQCFA	LDQCFA
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[1]	HDQCFA	The complete flag of the calibration of the channel A high 8bits DQ. High is valid.	R
[0]	LDQCFA	The complete flag of the calibration of the channel A low 8bits DQ. High is valid.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Note :

1.Channel A low 8bit signals: A_DQS0, A_DQSB0, A_DQ7~A_DQ0, A_DM0

Channel A high 8bit signals: A_DQS1, A_DQSB1, A_DQ15~A_DQ8, A_DM1

2.Dllsel: one step is 1/8 dfi_clk2x time

Ophsel: one step is 1 dfi_clk2x time

Cyclese: one step is 1 dfi_clk1x time

14.3.24 DDR PHY INIT_COMP

	INIT_COMP																PHY_APB_BASE+0x0d0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															INIT_COMP
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[0]	INIT_COMP	PHY initialize complete flag: 0: Not complete 1: Complete	R

14.3.25 DDR PHY Bist

																	PHY_APB_BASE+0x0d8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											Bist_Reg	Bist_CMD	Bist_DM	Bist_DQ	Bist_Comp
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
[4]	Bist_Reg	The bist result of the bist_reg mode. High means error	R
[3]	Bist_CMD	The bist result of the command. High means error.	R
[2]	Bist_DM	The bist result of the dm. High means error.	R
[1]	Bist_DQ	The bist result of the dq channel. High means error	R
[0]	Bist_Comp	The bist complete flag. High valid	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.4 Power-up and Initialize Sequence

14.4.1 Main initialize flow

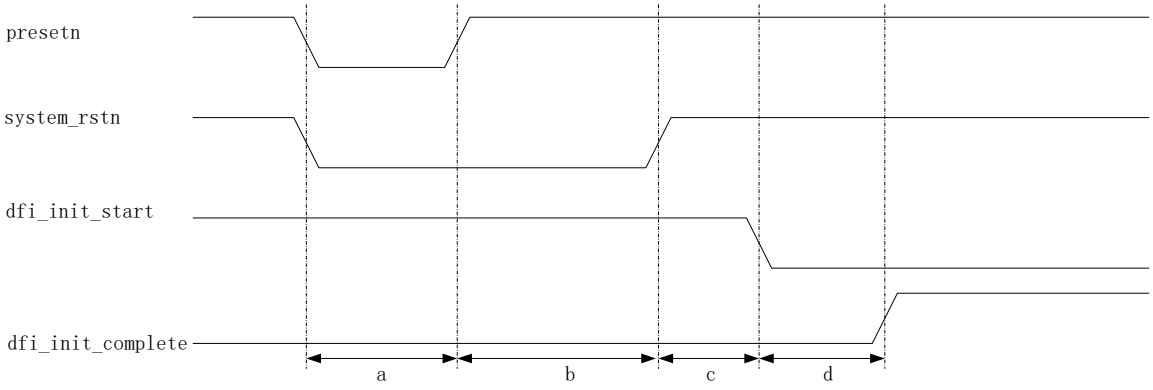
1. RESET flow
2. PHY PLL initialization.
3. PHY register configuration
4. DFI initialization
5. PHY Write-leveling training.(Only for DDR3)
6. PHY read calibration.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

14.4.2 RESET flow

1	Provide stable ***pclk*and *dfi_clk1x*** to the DDR PHY.
2	Low the ***presetn*** and ***system_rstn*** to reset the register module and digital core.
3	High the ***presetn*** signal to release the register module.
4	Configure the related register. Such as choose the memory type, CL, AL, PLL and DQ width.
5	High the system_rstn to release the digital core.
6	Enable the pll and wait for the PLL lock. **NOTE:** When we enable the PLL, the reference clock dfi_clk1x need to keep stable.
7	Low ***dfi_init_start*** to begin the initialization of the DDR PHY and wait ***dfi_init_comlete*** change from low to high.
8	Begin the initialization of the SDRAM and wait for the complte.
9	Begin the RX Calibration and Write-Leveling.
10	Begin to do the normal write or read operation.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.



Note:
a. At least 2 pclk cycles
b. Wait dfi_clk1x stable, at least 2 dfi_clk1x cycles.
c. At least 2 dfi_clk1x cycles.
d. Not more than 1024 dfi_clk1x cycles.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

15 External Memory Controller

15.1 Overview

The External Memory Controller (EMC) divides the off-chip memory space and outputs control signals complying with specifications of various types of static memory and bus interfaces. It enables the connection of static memory such as NOR flash memory, etc. to this processor.

- Static memory interface
  - Support 2 external chip selection CS2~1#. Each bank can be configured separately
  - The size and base address of static memory banks are programmable
  - Direct interface to 8-bit or 16-bit (no byte control) bus width external memory interface devices or external static memory to each bank. Read/Write strobe setup time and hold time periods can be programmed and inserted in an access cycle to enable connection to low-speed memory
  - Wait insertion by WAIT pin
  - Automatic wait cycle insertion to prevent data bus collisions in case of consecutive memory accesses to different banks, or a read access followed by a write access to the same bank

15.2 Pin Description

Following table list the EMC pins.

Table 15-1 EMC Pin Description

Pin Name	I/O	Signal	Description
Data Bus	I/O	SD15–SD0	Data I/O.
Address bus	O	SA12–SA0	Address output.
Static chip select 2 ~ 1	O	CS2~1#	Chip select signal that indicates the static bank being accessed.
Read enable	O	RD# /	For Static memory read enable signal.
Write enable	O	WE# /	Static memory write enable signal.
Wait	I	Wait# /	External wait state request signal for memory-like devices.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

15.3 Physical Address Space Map

Both virtual spaces and physical spaces are 32-bit wide in this architecture. Virtual addresses are translated by MMU into physical address which is further divided into several partitions for static memory, SDRAM, and internal I/O.

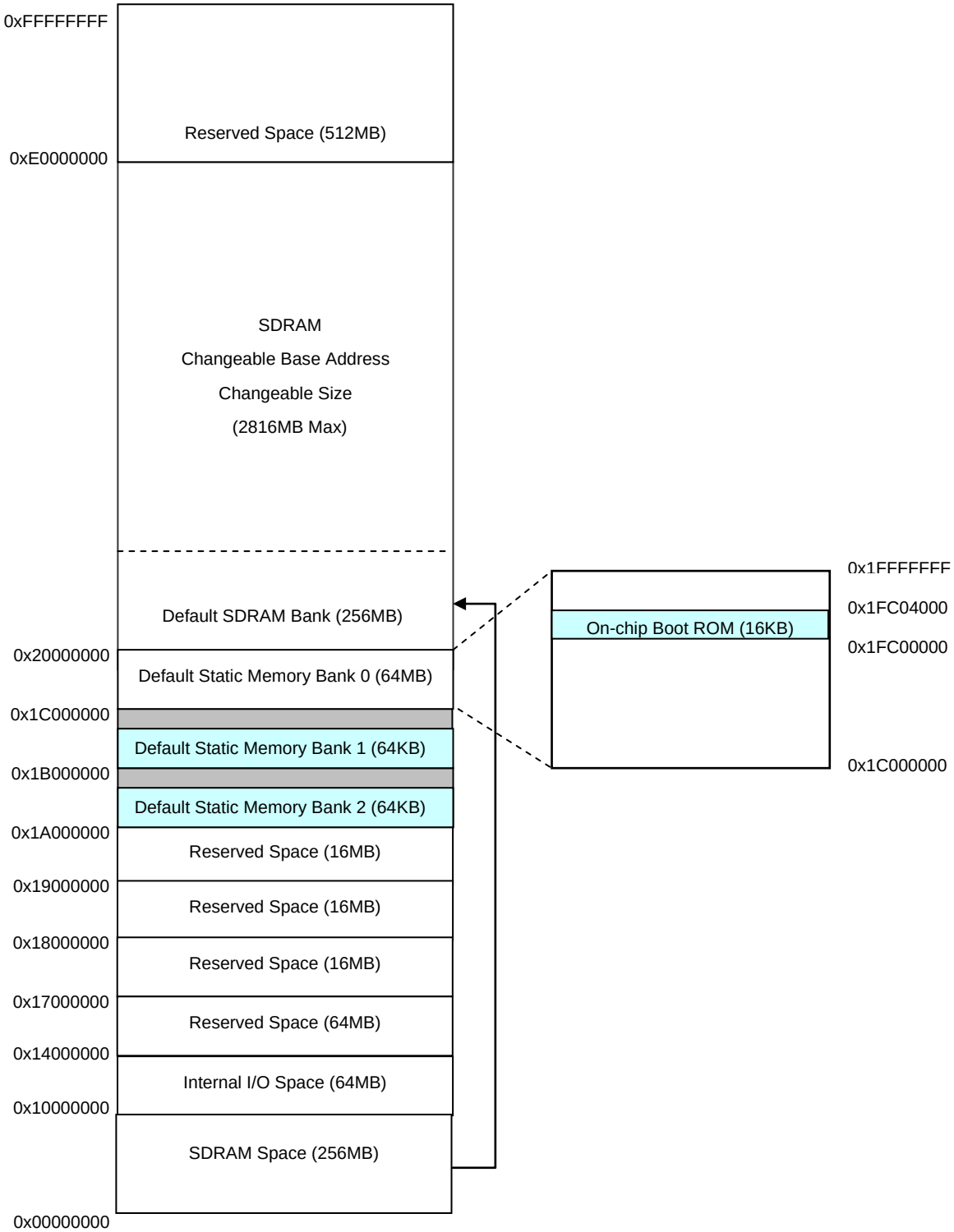


Figure 15-1 Physical Address Space Map

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Table 15-2 Physical Address Space Map

Start Address	End Address	Connectable Memory	Capacity
0x00000000	0x0FFFFFFF	SDRAM Memory	256MB
0x10000000	0x13FFFFFF	Internal I/O Devices	64MB
0x14000000	0x14FFFFFF	Reserved	16MB
0x15000000	0x15FFFFFF	Reserved	16MB
0x16000000	0x1600003F	Reserved	64B
0x16000040	0x16FFFFFF	Reserved	
0x17000000	0x1700003F	Reserved	64B
0x17000040	0x17FFFFFF	Reserved	
0x18000000	0x1800003F	Reserved	64B
0x18000040	0x18FFFFFF	Reserved	
0x19000000	0x1900003F	Reserved	64B
0x19000040	0x19FFFFFF	Reserved	
0x1A000000	0x1A00FFFF	Static Memory, CS2#	64KB
0x1A000040	0x1AFFFFFF	Reserved	
0x1B000000	0x1B00FFFF	Static Memory, CS1#	64KB
0x1B000040	0x1BFFFFFF	Reserved	
0x1C000000	0x1FBFFFFF	Reserved	
0x1FC00000	0x1FC02FFF	On-chip Boot ROM (16kB)	16KB
0x1FC04000	0x1FFFFFFF	Reserved	
0x20000000	0xDFFFFFFF	SDRAM Memory	3072MB
0xE0000000	0xFFFFFFFF	Reserved	512MB

The base address and size of each memory banks are configurable. Software can re-configure these memory banks according to the actual connected memories. Following table lists the default configuration after reset.

Table 15-3 Default Configuration of EMC Chip Select Signals

Chip-Select Signal	Connected Memory	Capacity	Memory Width *1	Start Address	End Address
CS1#	Static memory bank 1	64 KB	8, 16	0x1B000000	0x1B00FFFF
CS2#	Static memory bank 2	64 KB	8, 16	0x1A000000	0x1A00FFFF

NOTES:

1 Data width of static memory banks can be configured to 8, 16 bits by software.

2 The 16KB address space from H'1FC00000 to H'1FC03FFF in bank 0 is mapped to on-chip boot ROM. The other memory spaces in bank 0 are not used.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

15.4 Static Memory Interface

EMC provides a glueless interface to normal static memory which don't need byte control like SRAM, memory interface IO devices, etc.. It can directly control up to 2 devices using two chip select lines. Additional devices may be supported through external decoding of the address bus.

Each chip select can directly access memory or IO devices that are 8-bits or 16-bits wide. Each device connected to a chip select line has 2 associated registers that control its operation and the access timing to the external device. The Static Memory Control Register SMCRn specifies various configurations for the device. The Static Memory Address Configuration Register SACRn specifies the base address and size for each device, enabling any device to be located anywhere in the physical address range.

The static memory interface includes the following signals:

- Six chip selects, CS2~1#
- Thirteen address signals, SA12-SA0
- One read enable, RD#
- One write enable, WE#
- One wait pin, WAIT#

The SMT field in SMCRn registers specifies the type of memory and BW field specifies the bus width. BOOT_SEL[1:0] pin defines system boot from Nor.

15.4.1 Register Description

Table 15-4 Static Memory Interface Registers

Name	Description	RW	Reset Value	Address	Access Width
SMCR1	Static memory control register 1	RW	0x0FFF7700	0x13410014	32
SMCR2	Static memory control register 2	RW	0x0FFF7700	0x13410018	32
SACR1	Static memory bank 1 address configuration register	RW	0x00001AFE	0x13410034	32
SACR2	Static memory bank 2 address configuration register	RW	0x000018FE	0x13410038	32

15.4.1.1 Static Memory Control Register (SMCR1~2)

SMCR1~2 are 32-bit read/write registers that contain control bits for static memory. On reset, SMCR1~2 are initialized to 0x0FFF7700.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	SMCR1																													0x13410014
	SMCR2																													0x13410018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		STRV						TAW				TBP				TAH				TAS				BW		Reserved			BL		SMT
RST	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	Reserved	Writing has no effect, read as zero.	R
29:24	STRV	**Static Memory Recovery Time.** Its value is the number of idle cycles (0~63 cycles) inserted between bus cycles when switching from one bank to another bank or between a read access to a write access in the same bank. Its initial value is 0xF (15 cycles).	RW
23:20	TAW	**Access Wait Time.** For normal memory, these bits specify the number of wait cycles to be inserted in read strobe time. For burst ROM, these bits specify the number of wait cycles to be inserted in first data read strobe time. **TAW3~0 Wait cycle Wait# Pin** 0000 0 cycle Ignored 0001 1 cycle Enabled 0010 2 cycles Enabled 0011 3 cycles Enabled 0100 4 cycles Enabled 0101 5 cycles Enabled 0110 6 cycles Enabled 0111 7 cycles Enabled 1000 8 cycles Enabled 1001 9 cycles Enabled 1010 10 cycles Enabled 1011 12 cycles Enabled 1100 15 cycles Enabled 1101 20 cycles Enabled 1110 25 cycles Enabled 1111 31 cycles Enabled (Initial Value)	RW
19:16	TBP	**Burst Pitch Time.** For burst ROM, these bits specify the number of wait cycles to be inserted in subsequent access. For normal memory, these bits specify the number of wait cycles to be inserted in write strobe time. **TBP3~0 Wait cycle Wait# Pin** 0000 0 cycle Ignored	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0001 1 cycle Enabled 0010 2 cycles Enabled 0011 3 cycles Enabled 0100 4 cycles Enabled 0101 5 cycles Enabled 0110 6 cycles Enabled 0111 7 cycles Enabled 1000 8 cycles Enabled 1001 9 cycles Enabled 1010 10 cycles Enabled 1011 12 cycles Enabled 1100 15 cycles Enabled 1101 20 cycles Enabled 1110 25 cycles Enabled 1111 31 cycles Enabled (Initial Value)	
15	Reserved	Writing has no effect, read as zero.	R
15:12	TAH	**Address Hold Time.** These bits specify the number of wait cycles to be inserted from negation of read/write strobe to address. **TAH2~0 Wait cycle** 0000 0 cycle 0001 1 cycle 0010 2 cycles 0011 3 cycles 0100 4 cycles 0101 5 cycles 0110 6 cycles 0111 7 cycles (Initial Value) 1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 11 cycles 1100 12 cycles 1101 13 cycles 1110 14 cycles 1111 15 cycles	RW
11	Reserved	Writing has no effect, read as zero.	R
11:8	TAS	**Address Setup Time.** These bits specify the number of wait cycles (0~15 cycles) to be inserted from address to assertion of read/write strobe. **TAS2~0 Wait cycle** 000 0 cycle 001 1 cycle	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		010 2 cycles 011 3 cycles 100 4 cycles 101 5 cycles 110 6 cycles 111 7 cycles (Initial Value) 1000 8 cycles 1001 9 cycles 1010 10 cycles 1011 11 cycles 1100 12 cycles 1101 13 cycles 1110 14 cycles 1111 15 cycles	
7:6	BW	**Bus Width.** These bits specify the bus width. this filed is writeable and are initialized to 0 by a reset. **BW1~0 Bus Width** 00 8 bits (Initial Value) 01 16 bits 10 Reserved 11 Reserved	RW
5:3	Reserved	Writing has no effect, read as zero. **NOTE:** Don't write Bit3 to 1.	R
2:1	BL	**Burst Length (BL1, BL0).** When Burst ROM is connected; these bits specify the number of burst in an access. These bits are only valid when SMT is set to 1. **BL1~0 Burst Length** 00 4 consecutive accesses. Can be used with 8- or 16-bit bus width (Initial Value) 01 8 consecutive accesses. Can be used with 8- or 16-bit bus width 10 16 consecutive accesses. Can only be used with 8- or 16-bit bus width 11 32 consecutive accesses. Can only be used with 8-bit bus width	
0	SMT	**Static Memory Type (SMT).** This bit specifies the type of static memory. **SMT Description** 0 Normal Memory (Initial Value) 1 Burst ROM	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

15.4.1.2 Static Bank Address Configuration Register (SACR1~2)

SACR1~2 defines the physical address for static memory bank 1 to 2, respectively. Each register contains a base address and a mask. When the following equation is met:

(*physical_address* [31:24] & **MASK$_n$**) == **BASE$_n$**

The bank n is active. The *physical_address* is address output on internal system bus. Static bank regions must be programmed so that each bank occupies a unique area of the physical address space. Programming overlapping bank regions will result in unpredictable error. These registers are initialized by a reset.

	SACR1 SACR2																0x13410034 0x13410038													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																BASE								MASK							
RST1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	0
RST2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1	1	1	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:8	BASE	**Address Base:** Defines the base address of Static Bank n (n = 1 to 2). The initial values are: SACR1.BASE 0x1B SACR2.BASE 0x1A	RW
23:20	MASK	**Address Mask**: Defines the mask of Static Bank n (n = 1 to 2). The initial values are: SACR1.MASK 0xFE SACR2.MASK 0xFE	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

15.4.2 Example of Connection

Following figures shows examples of connection to 16- and 8-bit data width normal memory.

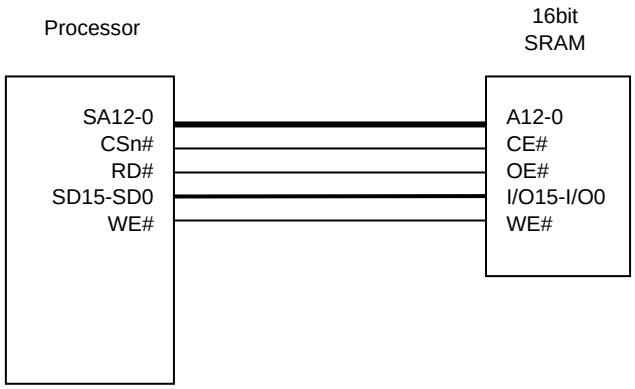


Figure 15-2 Example of 16-Bit Data Width SRAM Connection

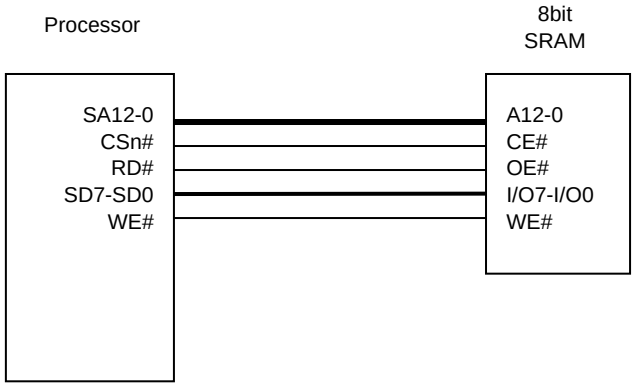


Figure 15-3 Example of 8-Bit Data Width SRAM Connection

15.4.3 Basic Interface

When SMT field in SMCRn (n = 1 to 2) is 0, normal memory (non-burst ROM, Flash, normal SRAM or memory-like device) is connected to bank n. When bank n (n = 1 to 2) is accessed, CSn# is asserted as soon as address is output. In addition, the RD# signal, which can be used as OE#, and write control signals WE# is asserted.

The TAS field in SMCRn is the latency from CSn# to read/write strobe. The TAW3 field is the delay time of RD# in read access. TBP3~0 field is the delay time of WE# and WEn# in write access. In addition, any number of waits can be inserted by means of the external pin (WAIT#). The TAH field is the latency from RD# and WEn# negation to CSn# negation, also the hold time to address and write data.

All kinds of normal memories (non-burst ROM, normal SRAM and Flash) have the same read and

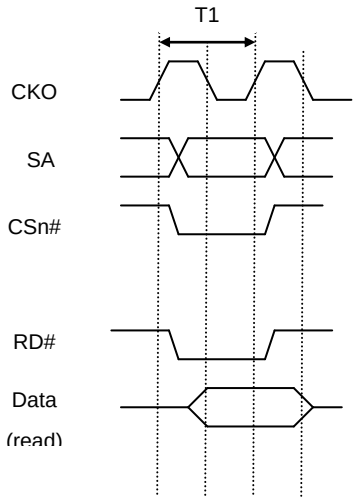
Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

write timing. There are some requirements for writes to flash memory. Flash memory space must be un-cacheable and un-buffered. Writes must be exactly the width of the populated Flash devices on the data bus (no byte writes or word writes to a 16-bit bus, and so on). Software is responsible for partitioning commands and data, and writing them out to Flash in the appropriate sequence.

Glossary

Th – hold cycle
Tw – wait cycle
Ts – setup cycle
T1 – read inherent cycle or first write inherent cycle
T2 – last write inherent cycle
Tb – burst read inherent cycle

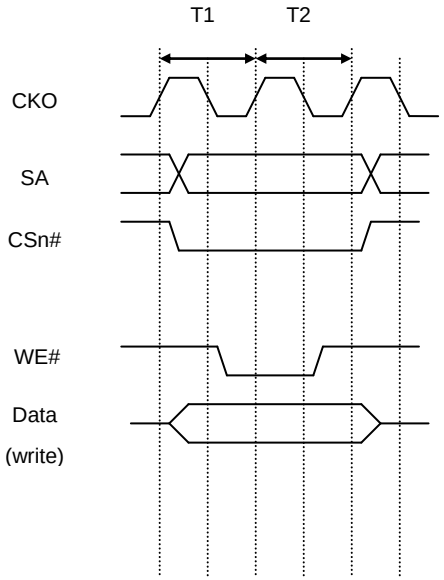
Following figures show the timing of normal memory. A no-wait read access is completed in one cycle and a no-wait write access is completed in two cycles. Therefore, there is no negation period in case of access at minimum pitch.



*In this example, SMCRn:MT = 0, TAS = 0, TAW = 0, TAH = 0

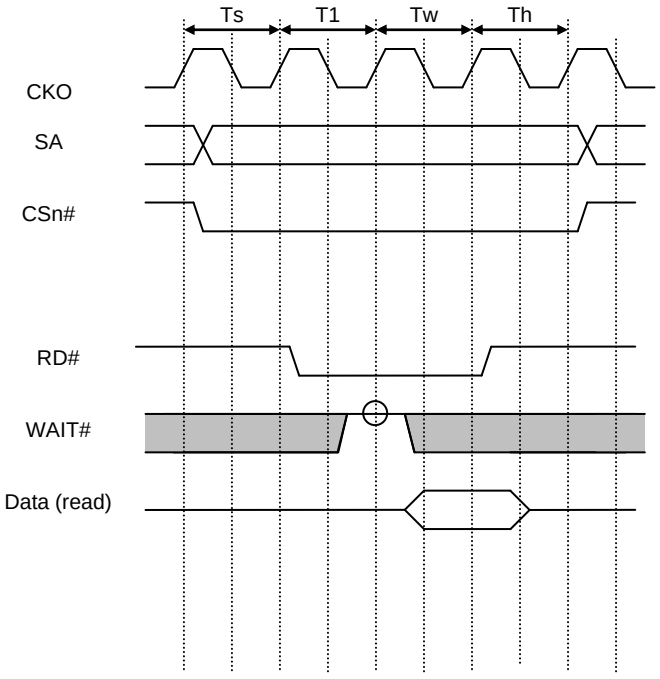
Figure 15-4 Basic Timing of Normal Memory Read

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.



*In this example, SMCRn: SMT = 0, TAS = 0,
TBP = 0, TAH = 0

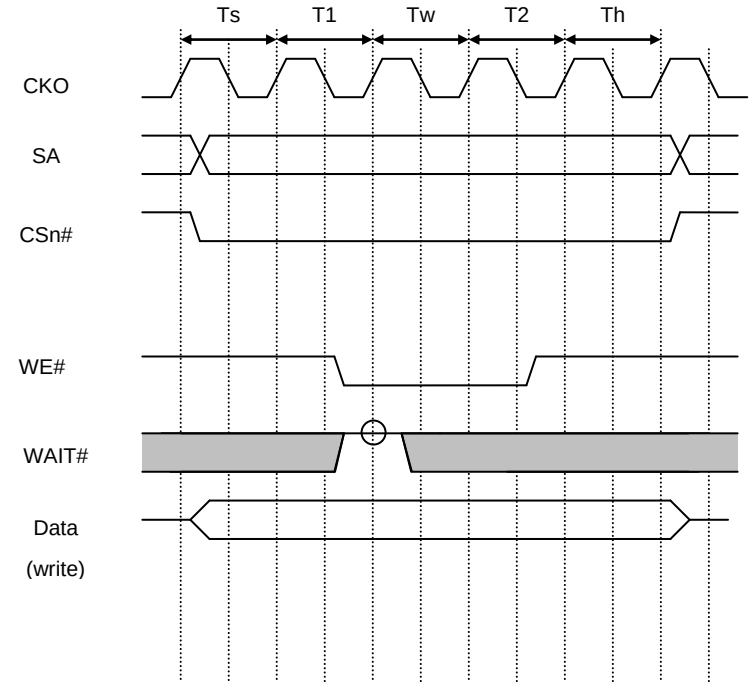
Figure 15-5 Basic Timing of Normal Memory Write



*In this example, SMCRn: SMT = 0, TAS = 1, TAW = 1, TAH = 1

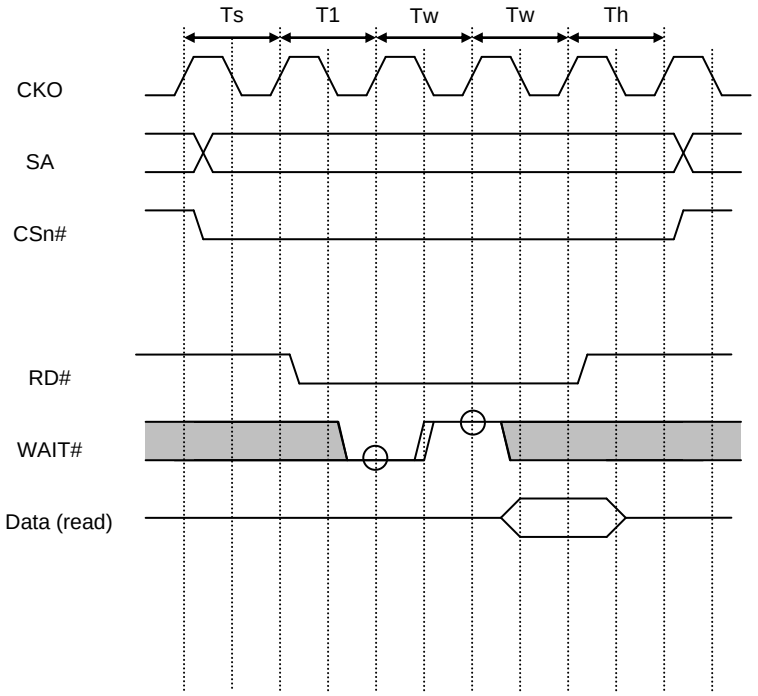
Figure 15-6 Normal Memory Read Timing With Wait (Software Wait Only)

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.



*In this example, SMCRn: SMT = 0, TAS = 1, TBP = 1, TAH = 1

Figure 15-7 Normal Memory Write Timing With Wait (Software Wait Only)



*In this example, SMCRn: SMT = 0, TAS = 1, TAW = 1, TAH=1

Figure 15-8 Normal Memory Read Timing With Wait (Wait Cycle Insertion by WAIT# pin)

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

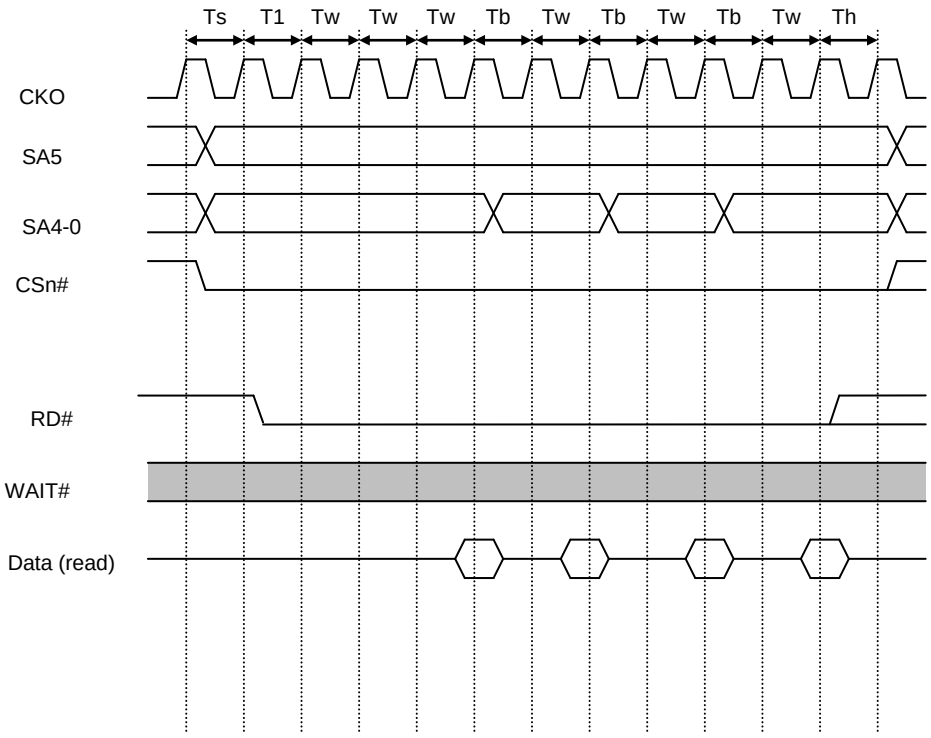
15.4.4 Burst ROM Interface

Setting SMT to 1 in SMCRn allows burst ROM to be connected to bank n (n = 1 to 2). The burst ROM interface provides high-speed access to ROM that has a nibble access function. Basically, access is performed in the same way as for normal memory, but when the first cycle ends, only the address is changed before the next access is executed. When 8-bit burst ROM is connected, the number of consecutive accesses can be set as 4, 8, 16, or 32 with bits BL1~0. When 16-bit ROM is connected, 4, 8, or 16 can be set in the same way.

For burst ROM read, TAW sets the delay time from read strobe to the first data, TBP sets the delay time from consecutive address to data. Burst ROM writes have the same timing as normal memory except TAW instead of TBP is used to set the delay time of write strobe.

WAIT# pin sampling is always performed when one or more wait states are set.

Following figures show the timing of burst ROM.



*In this example, SMT = 1, BL = 0, TAS = 1, TAW = 3,TBP = 1,TAH = 1

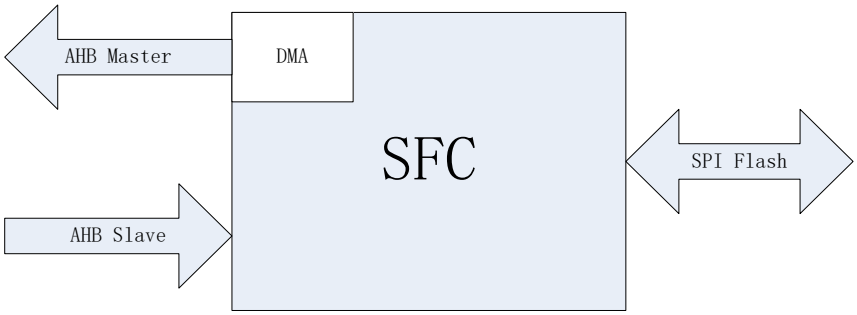
Figure 15-9 Burst ROM Read Timing (Software Wait Only)

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

16 SPI Flash Controller(SFC)

16.1 Overview

This module is an SPI master to control the SPI flash device. Data can be transferred in CPU controlling mode or DMA mode.



16.2 Features

- SPI protocol support: Standard, Dual, Quad, Octal SPI
- transmit-only or receive-only operation
- MSB always be first in intra transfer of one byte. Least Significant Byte first for inter transfer of data bytes, and Most Significant Byte first for inter transfer of command or address bytes.
- 64 entries x 32 bits wide data FIFO
- one device select
- Configurable sampling point for reception
- Configurable timing parameters: tSLCH, tCHSH and tSHSL
- Configurable flash address wide are supported
- 10 transfer formats: Standard SPI, Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI, Octal-Output/Octal-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Octal-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI, Full Octal-I/O SPI,
- two data transfer mode: slave mode and DMA mode
- Configurable 6 phases for software flow
- CDT(command descriptor table)
- DMA descriptor chain for data transfer
- 2 pieces splicing for Octal transmission
- SDR trans mode.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

16.3 Block Diagram

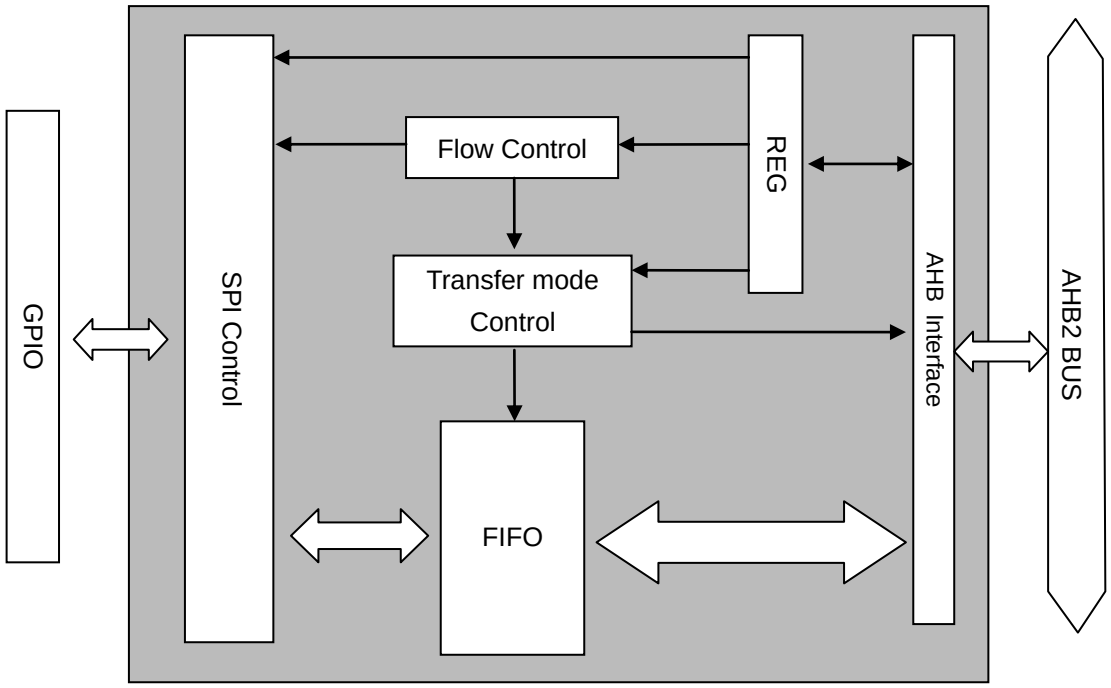


Figure 16-1 SFC Block Diagram

The AHB Interface include one slave interface and one master interface. The slave interface is used for register configuration and slave transfer mode, and the master interface is designed for DMA operation.
The FIFO block is bidirectional, used as data buffer for transmission(from AHB to device) and reception(from device to AHB).
The Flow Control module controls the operation of the 6 phases
The Transfer mode Control act as the handler of slave mode and DMA mode.

16.4 Functional Description

16.4.1 Bus function

16.4.1.1 AHB Slave Interface

- parameter configuration
- transfer data in slave mode.
- data and address must align with 4 bytes.
- only SINGLE transfer is supported.

16.4.1.2 AHB Master Interface

- transfer data in DMA mode
- SINGLE, INCR, INCR4, INCR8, INCR16, INCR32 are supported.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

16.4.2 Configurable Timing parameter

16.4.2.1 Propagation delay

The propagation delay do not effect the data transmission, and it would not effect the data reception when the serial clock has a low frequency, as shown in the Figure 16-2

But when the serial clock run at a fast frequency, the propagation delay will cause the incoming data could not arrival at the right clock edge, then the sampling point should be adjustable as shown in the Figure 16-3

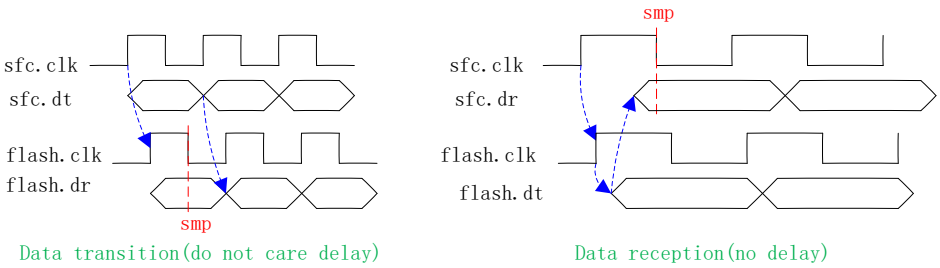


Figure 16-2 Sample point(no delay)

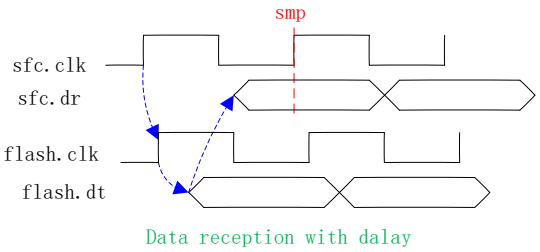


Figure 16-3 Sample point(delay)

16.4.2.2 AC timing

tSETUP(tSLCH), tHOLD(tCHSH), tSH(tSHSL) are configurable.

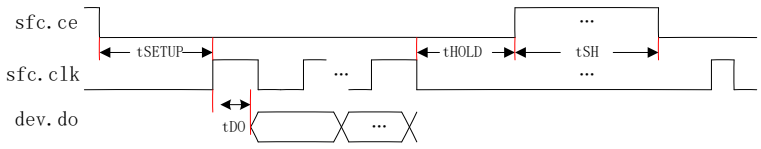


Figure 16-4 AC timing

16.5 Pin Description

Table 16-1 I/O Pin Description

Name	I/O	Description
io_if0.clk	Output	Serial clock
io_if0.ce	Output	Device select

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

io_if0.dt_io0	InOut	Serial data IO0
io_if0.dr_io1	InOut	Serial data IO1
io_if0.wp_io2	InOut	Serial data IO2(WP#)
io_If0.hd_io3	InOut	Serial data IO3(HOLD#)
io_if1.dt_io0	InOut	Serial data IO4
io_if1.dr_io1	InOut	Serial data IO5
io_if1.wp_io2	InOut	Serial data IO6(WP#)
io_If1.hd_io3	InOut	Serial data IO7(HOLD#)

16.6 Data Format Description

16.6.1 1Transfer format

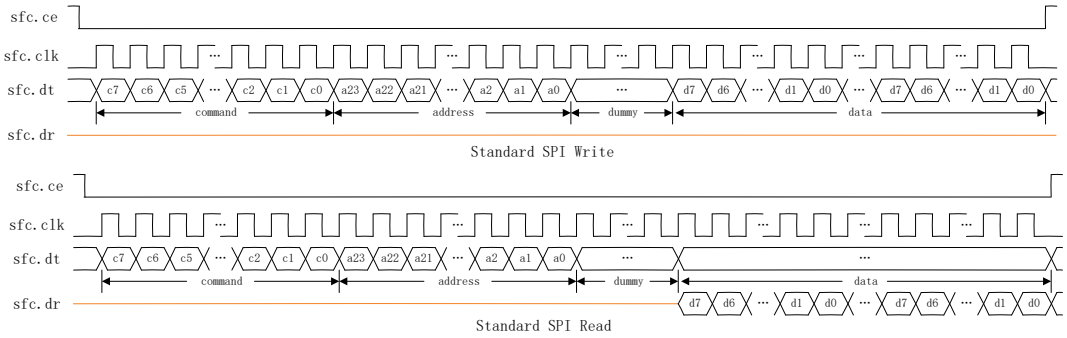


Figure 16-5 Data Format(Standard SPI)

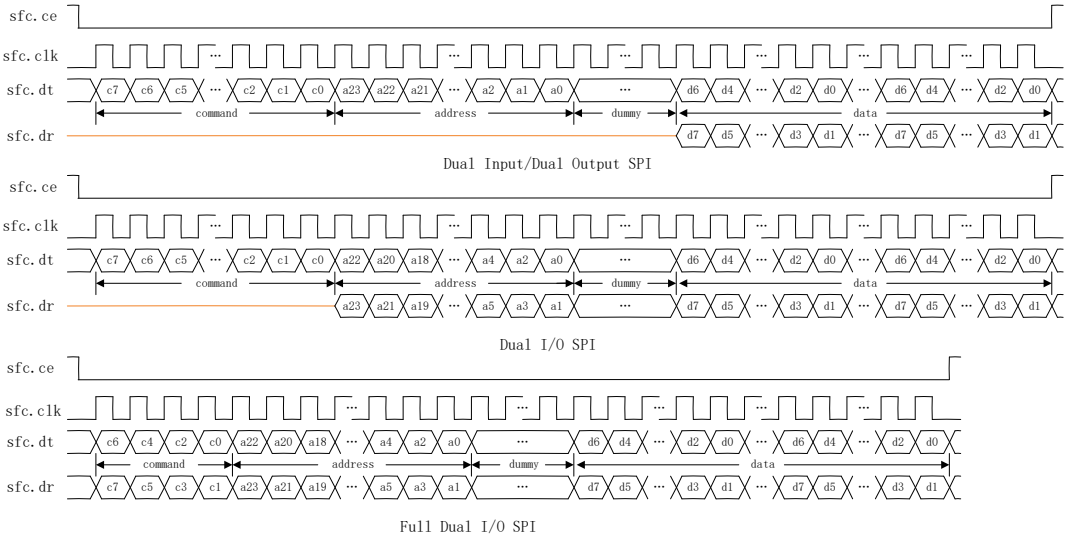


Figure 16-6 Data Format(Dual SPI)

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

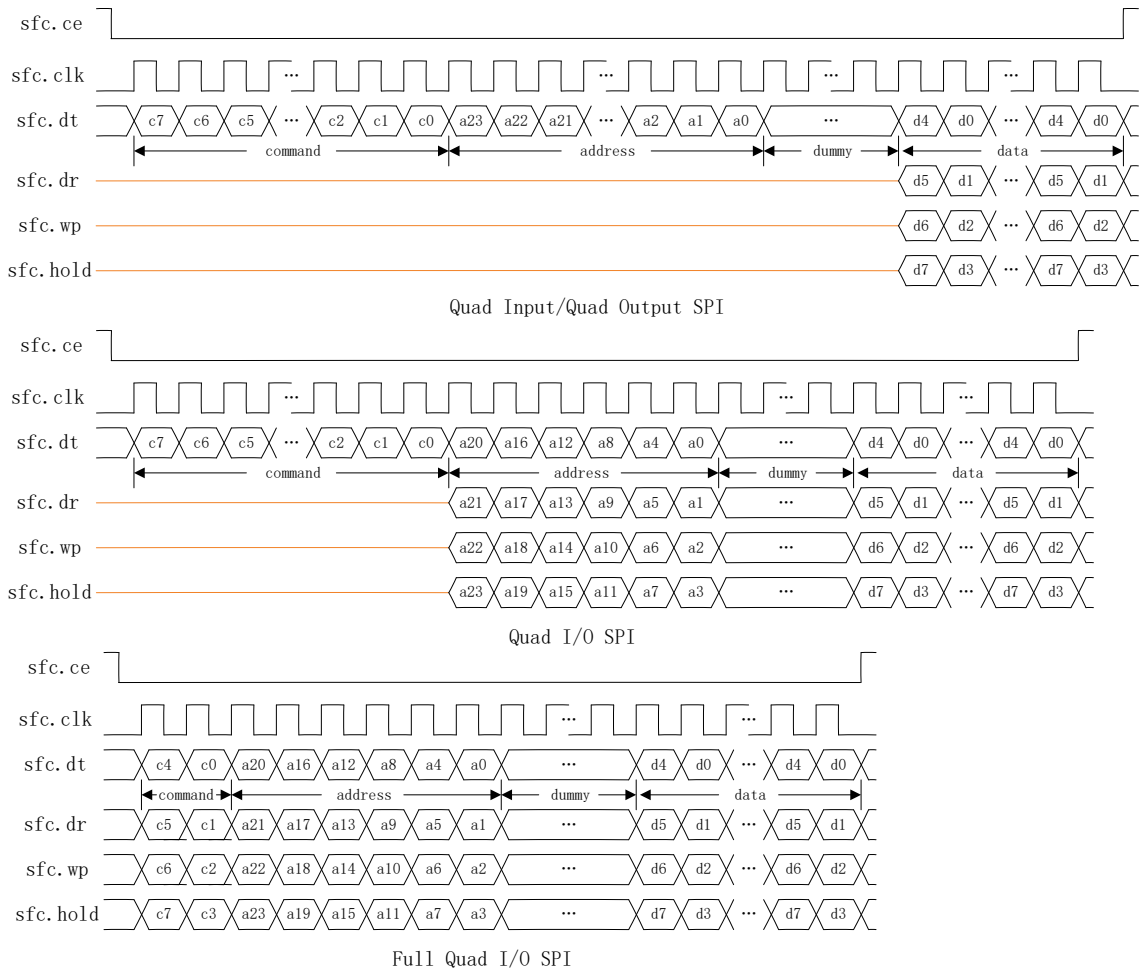


Figure 16-7 Data Format(Quad SPI)

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

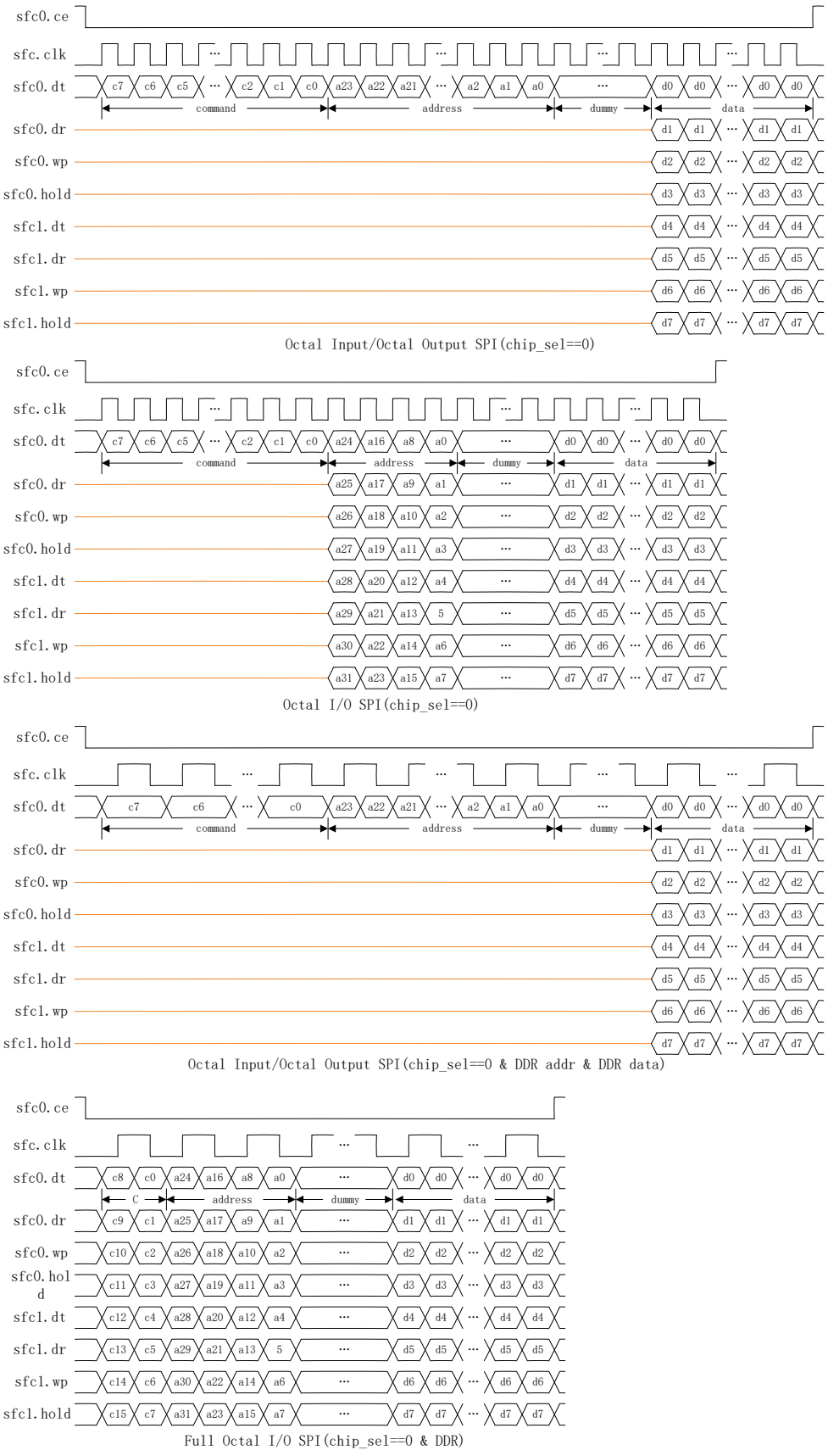


Figure 16-8 Data Format(Octal@CHIP_SEL=0)

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

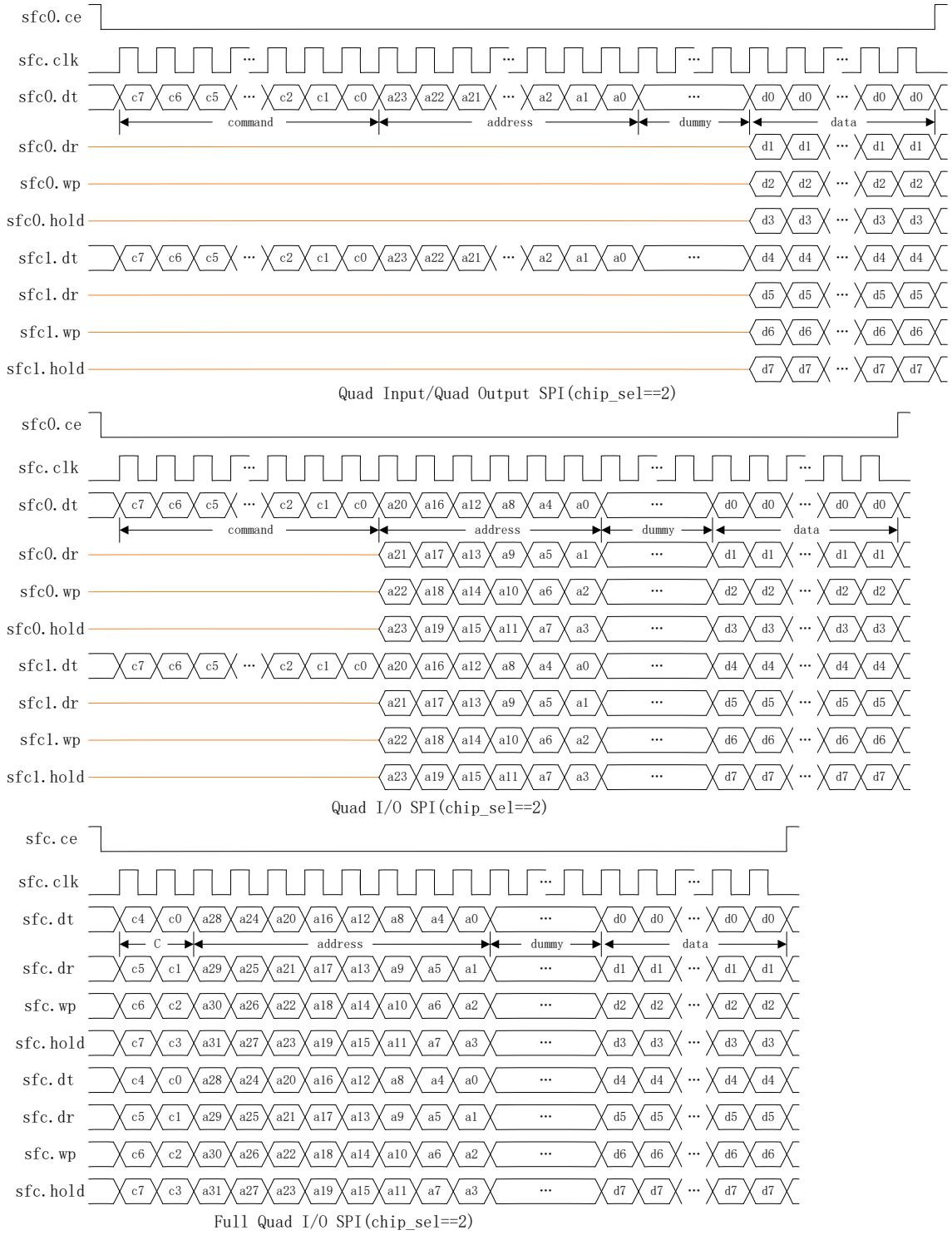


Figure 16-9 Data Format(Quad@CHIP_SEL=2)

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

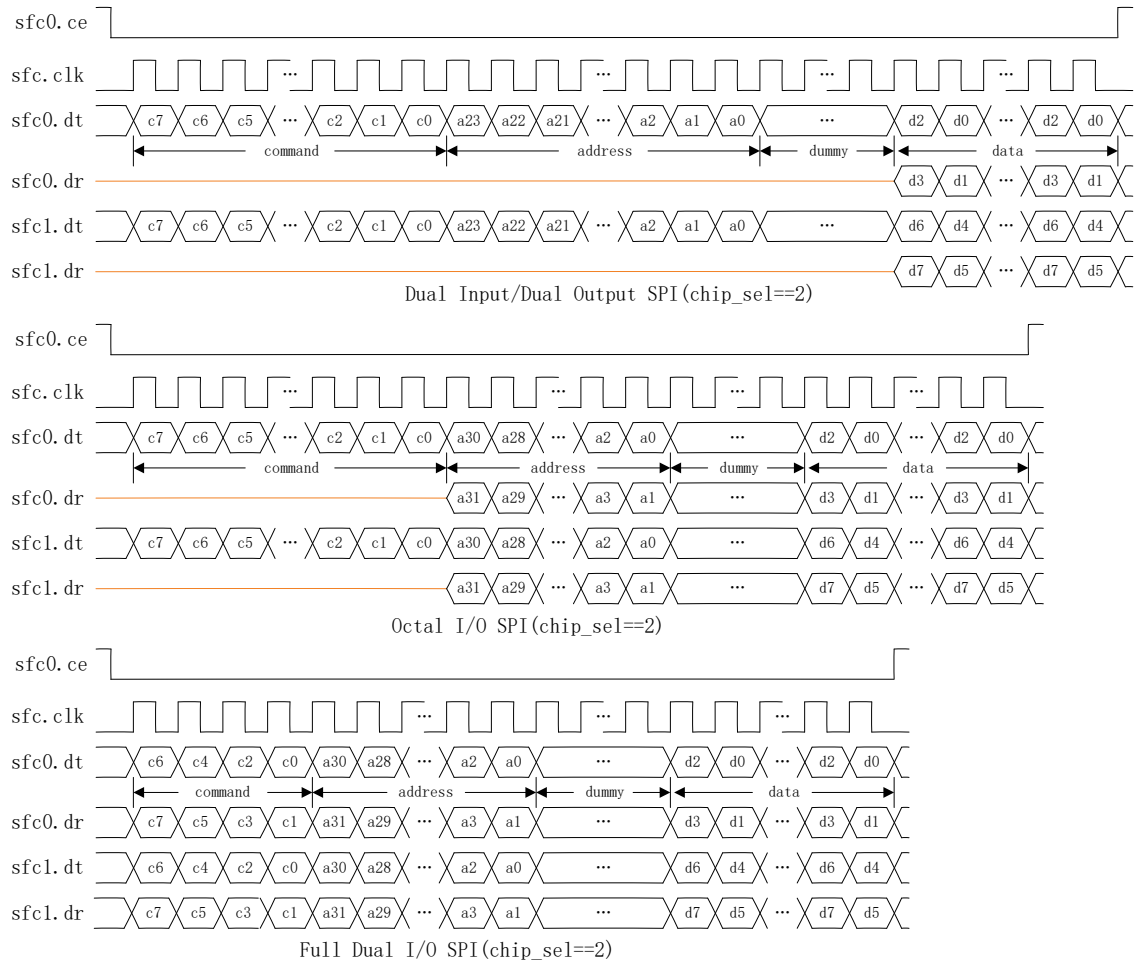


Figure 16-10 Data Format(Dual@CHIP_SEL=2)

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

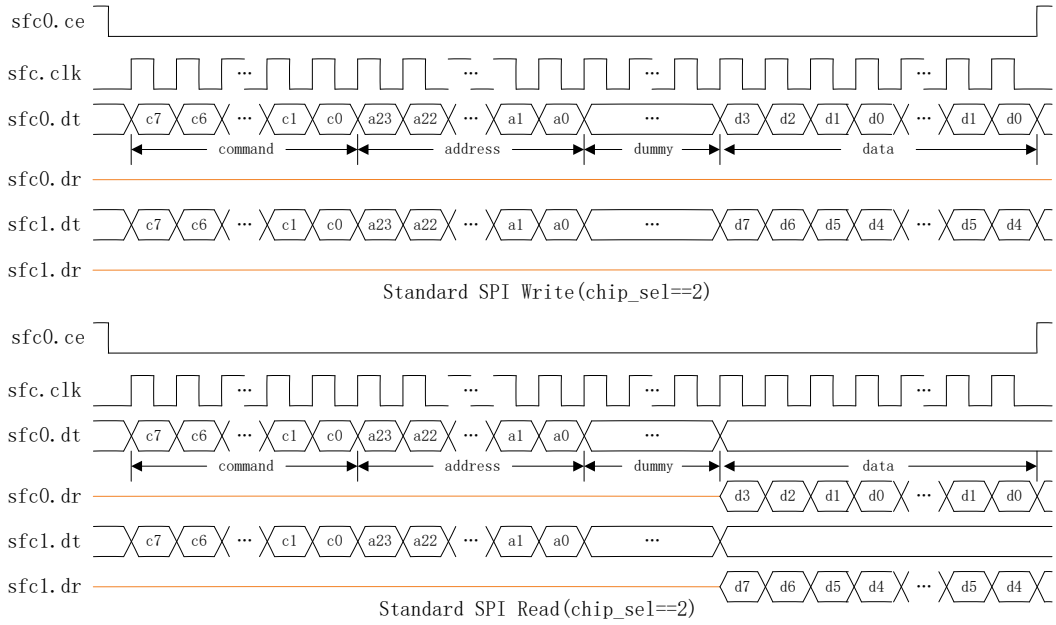


Figure 16-11 Data Format(Standard SPI@CHIP_SEL=2)

16.6.2 Endian Description

Command is MSB first, as shown in the Figure 16-8

Address is MSB first, as shown in the Figure 16-5~ Figure 16-11;

Flash's status can be configured as LSB or MSB by using SFC_DEV_CFG.STA_ENDIAN

Data's endian and unit can be configured by TRAN_CFG1.DATA_ENDIAN and TRAN_CFG1.WORD_UNIT

16.7 Registers Description

16.7.1 Instructions

Following chapter will descript the functions of all software accessible registers.

Conventions:

13. Register Address = Base + Address offset
14. The registers can be read and written by AHB2 bus
15. Register read/write attribute
    - ✧ R - Read only
    - ✧ W - Write only
    - ✧ RW - read and write
    - ✧ RCW - read and write, but clear to 0 by read
    - ✧ RSW - read and write, but set to 1 by read
    - ✧ RWC - read and write, clear to 0 by write 1, write 0 has no effect
    - ✧ RWS - read and write, set to 1 by write 1, write 0 has no effect

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

- ✧ RC - read only, and clear to 0 by read
- ✧ RS - read only, and set to 1 by read
- ✧ SPEC - special access method, relate to its description

16. Reset Value
    - 1 - reset to 1
    - 0 - reset to 0
    - ? - value unknown after reset

16.7.2 Map

The SFC's registers map base address is 0x13440000

The SFC is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 16-2 SFC Registers Map

Name	Reset Value	Address Offset	Description	RW	Mask
GLB0	0x0000_008F	Base+0x0000	Global configure register0	RW	0xFFFF_FFFF
DEV_CONF	0x0000_0027	Base+0x0004	Device parameter	RW	0x0007_FFFF
DEV_STA_EXP	0x0000_0000	Base+0x0008	Expected status of device	RW	0xFFFF_FFFF
DEV0_STA_RT	0x0000_0000	Base+0x000c	Real-time status of device	R	0xFFFF_FFFF
DEV_STA_MSK	0x0000_0000	Base+0x0010	Mask flag of device's status	RW	0xFFFF_FFFF
TRAN_CFG0_0	0x0000_0000	Base+0x0014	Transfer parameter0 of phase0	RW	0xFFFF_FFFF
TRAN_CFG0_1	0x0000_0000	Base+0x0018	Transfer parameter0 of phase1	RW	0xFFFF_FFFF
TRAN_CFG0_2	0x0000_0000	Base+0x001c	Transfer parameter0 of phase2	RW	0xFFFF_FFFF
TRAN_CFG0_3	0x0000_0000	Base+0x0020	Transfer parameter0 of phase3	RW	0xFFFF_FFFF
TRAN_CFG0_4	0x0000_0000	Base+0x0024	Transfer parameter0 of phase4	RW	0xFFFF_FFFF
TRAN_CFG0_5	0x0000_0000	Base+0x0028	Transfer parameter0 of phase5	RW	0xFFFF_FFFF
TRAN_LEN	0x0000_0000	Base+0x002c	Transfer length	RW	0xFFFF_FFFF
DEV_ADR0	0x0000_0000	Base+0x0030	Device address of phase0	RW	0xFFFF_FFFF
DEV_ADR1	0x0000_0000	Base+0x0034	Device address of phase1	RW	0xFFFF_FFFF
DEV_ADR2	0x0000_0000	Base+0x0038	Device address of phase2	RW	0xFFFF_FFFF
DEV_ADR3	0x0000_0000	Base+0x003c	Device address of phase3	RW	0xFFFF_FFFF
DEV_ADR4	0x0000_0000	Base+0x0040	Device address of phase4	RW	0xFFFF_FFFF
DEV_ADR5	0x0000_0000	Base+0x0044	Device address of phase5	RW	0xFFFF_FFFF
DEV_PLUS0	0x0000_0000	Base+0x0048	Plus address of phase0	RW	0xFFFF_FFFF
DEV_PLUS1	0x0000_0000	Base+0x004c	Plus address of phase1	RW	0xFFFF_FFFF

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

DEV_PLUS2	0x0000_0000	Base+0x0050	Plus address of phase2	RW	0xFFFF_FFFF
DEV_PLUS3	0x0000_0000	Base+0x0054	Plus address of phase3	RW	0xFFFF_FFFF
DEV_PLUS4	0x0000_0000	Base+0x0058	Plus address of phase4	RW	0xFFFF_FFFF
DEV_PLUS5	0x0000_0000	Base+0x005c	Plus address of phase5	RW	0xFFFF_FFFF
MEM_ADDR	0x0000_0000	Base+0x0060	DDR address	RW	0xFFFF_FFFF
TRIG	0x0000_0000	Base+0x0064	SFC trigger	RW	0x0000_0007
SR	0x0000_0000	Base+0x0068	Status register	R	0x007F_007F
SCR	0x0000_0000	Base+0x006c	Status clear register	RW	0x0000_003F
INTC	0x0000_001F	Base+0x0070	Interrupt control	RW	0x0000_001F
FSM	0x0001_0111	Base+0x0074	Sub-modules' FSM state	R	0x000F_FF77
CGE	0x0000_003F	Base+0x0078	CLK gate function	RW	0x0000_003F
CMD_IDX	0x0000_0000	Base+0x007c	Cmd index in CDT	RW	0xC000_003F
COL_ADDR	0x0000_0000	Base+0x0080	Column addr	RW	0xFFFF_FFFF
ROW_ADDR	0x0000_0000	Base+0x0084	Row addr	RW	0xFFFF_FFFF
STA_ADDR0	0x0000_0000	Base+0x0088	Status addr0	RW	0xFFFF_FFFF
STA_ADDR1	0x0000_0000	Base+0x008c	Status addr1	RW	0xFFFF_FFFF
DES_ADDR	0x0000_0000	Base+0x0090	DMA descriptor address	RW	0xFFFF_FFFF
GLB1	0x0000_008F	Base+0x0094	Global configure register1	RW	0x0000_0003
DEV1_STA_RT	0x0000_0000	Base+0x0098	Real-time status of device	R	0xFFFF_FFFF
TRAN_CFG1_0	0x0000_0000	Base+0x009c	Transfer parameter1 of phase0	RW	0xFFFF_FFFF
TRAN_CFG1_1	0x0000_0000	Base+0x00a0	Transfer parameter1 of phase1	RW	0xFFFF_FFFF
TRAN_CFG1_2	0x0000_0000	Base+0x00a4	Transfer parameter1 of phase2	RW	0xFFFF_FFFF
TRAN_CFG1_3	0x0000_0000	Base+0x00a8	Transfer parameter1 of phase3	RW	0xFFFF_FFFF
TRAN_CFG1_4	0x0000_0000	Base+0x00ac	Transfer parameter1 of phase4	RW	0xFFFF_FFFF
TRAN_CFG1_5	0x0000_0000	Base+0x00b0	Transfer parameter1 of phase5	RW	0xFFFF_FFFF
CDT	0x0000_0000	Base+0x0800 ~ Base+0x0c00	CDT's register interface	RW	0xFFFF_FFFF
DR	0x0000_0000	Base+0x1000	Data register (slave mode)	RW	0xFFFF_FFFF

16.7.3 Registers

16.7.3.1 SFC Global Configure Register0

	SFC_GLB0																Base + 0x0000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	POLL_TIME																DES_EN	CDT_EN	TRAN_DIR	THRESHOLD						OP_MODE	PHASE_NUM			WP_EN	BURST_LEN		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:16	POLL_TIME	Interval time counter between twice polling op..	RW
15	DES_EN	Descriptor of DMA enable. 1: DMA will use the memory in descriptor, no longer use the SFC_MEM_ADDR 0: disable.	RW
14	CDT_EN	Use CDT. 0: disable(default) 1: enable	RW
13	TRAN_DIR	The direction of transfer. 0: read data from SPI flash (default) 1: write data to SPI flash	RW
12:7	THRESHOLD	FIFO threshold. (unit: word) Natural number, 1-63(default is 1). Note: cannot be 0	RW
6	OP_MODE	0: slave mode (default) 1: DMA mode	RW
5:3	PHASE_NUM	The number of phase in one flow. 001: 1 phase (default) 010: 2 phases 011: 3 phases 100: 4 phases 101: 5 phases 110: 6 phases Note: cannot be 0	RW
2	WP_EN	Enable the hardware write protection 0: disable WP 1: Enable WP (default)	RW
1:0	BURST_MD	The max beats of burst. 00: reserved 01: INCR8 10: INCR16 11: INCR32 (default)	RW

16.7.3.2 SFC Global Configure Register1

	SFC_GLB1																Base + 0x0094															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														CHIP_SEL	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:3	Reserved	Write has no effect. Read as indeterminate value.	R
2	Reserved	Keep default	RW
1:0	CHIP_SEL	Chip select 00: chip 0(default) 01: keep default 10: chip 0 + 1 11: reserved	RW

16.7.3.3 SFC Device Configure Register

	SFC_DEV_CONF																Base + 0x0004															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	STA_ENDIAN	Reserved										SMP_DELAY					CMD_TYPE	STA_TYPE		THOLD		TSETUP		TSH				CPHA	CPOL	CE_DL	HOLD_DL	WP_DL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1

Bits	Name	Description	RW
31	STA_ENDIAN	0: LSB (default) 1: MSB	RW
30:21	Reserved	Write has no effect. Read as zero.	R
20:16	SMP_DELAY	Sample delay, it's depends on the device output delay, PCB delay and the IO ports delay, etc. 00000: no delay (default) 00001: 45 00010: 90 00011: 135 00100: 180 00101: 225 00110: 270 00111: 315 01000: one SFC_CLK cycle 01001: one SFC_CLK cycle + 45 01010: one SFC_CLK cycle + 90 ..... 01111: one SFC_CLK cycle + 315 10000: two SFC_CLK cycle ..... 11111: three SFC_CLK cycle + 315	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

15	CMD_TYPE	0: 1 byte (default) 1: 2 bytes	RW
14:13	STA_TYPE	used for polling 00: 1 byte status (default) 01: 2 bytes status 10: 3 bytes status 11: 4 bytes status	RW
12:11	THOLD	Hold time of SFC_CE, the time between the last edge of SFC_CLK and SFC_CE de-assertion. 00: half SFC_CLK cycle (default) 01: one SFC_CLK cycle 10: one and a half SFC_CLK cycle 11: two SFC_CLK cycle	RW
10:9	TSETUP	Setup time of SFC_CE, the time between SFC_CE assertion and the first edge of SFC_CLK. 00: half SFC_CLK cycle (default) 01: one SFC_CLK cycle 10: one and a half SFC_CLK cycle 11: two SFC_CLK cycle	RW
8:5	TSH	The min interval time between twice assertion of SFC_CE. 0000: one SFC_CLK cycle 0001: one SFC_CLK cycle(default) 0010: one and a half SFC_CLK cycle 0011: two SFC_CLK cycle 0100: two and a half SFC_CLK cycle 0101: three SFC_CLK cycle 0110: three and a half SFC_CLK cycle 0111: four SFC_CLK cycle 1000: four and a half SFC_CLK cycle 1001: five SFC_CLK cycle 1010: five and a half SFC_CLK cycle 1011: six SFC_CLK cycle 1100: six and a half SFC_CLK cycle 1101: seven SFC_CLK cycle 1110: seven and a half SFC_CLK cycle 1111: eight SFC_CLK cycle	RW
4	CPHA	This bit is used to select the SPI clock format. 0 = Sampling of data occurs at odd edges (1,3,5,...) of the SFC_CLK clock (default) 1 = Sampling of data occurs at even edges (2,4,6,...) of the SFC_CLK clock	RW
3	CPOL	This bit selects the active level of SFC_CLK. 0 = Active-high clocks selected. In idle state SFC_CLK is low. (default)	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1 = Active-low clocks selected. In idle state SFC_CLK is high.	
2	CE_DL	The default invalid level of SFC_CE pin 0: low 1: high (default)	RW
1	HOLD_DL	The default invalid level of SFC_HOLD pin 0: low 1: high (default)	RW
0	WP_DL	The default invalid level of SFC_WP pin 0: low 1: high (default)	RW

16.7.3.4 SFC Device Status Expected Register

	SFC_DEV_STA_EXP																															
																	Base + 0x0008															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_STA_EXP																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_STA_EXP	The expected value of flash status for comparing.	RW

16.7.3.5 SFC Device0 Status Real-time Register

	SFC_DEV0_STA_RT																															
																	Base + 0x000c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV0_STA_RT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV0_STA_RT	The real-time status of SPI Flash0	R

16.7.3.6 SFC Device1 Status Real-time Register

	SFC_DEV1_STA_RT																															
																	Base + 0x0098															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV1_STA_RT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	DEV1_STA_RT	The real-time status of SPI Flash1	R

16.7.3.7 SFC Device Status Mask Register

	SFC_DEV_STA_MSK																Base + 0x0010															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_STA_MSK																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_STA_MSK	Flash status mask for comparing. 1: this bit will be checked. 0: this bit will not be checked.	RW

16.7.3.8 SFC Transfer Configure Register0 (phase0-phase5)

	SFC_TRAN_CCFG0(0-5)																Base + 0x0014 - Base + 0x0028															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLK_MODE			ADDR_WIDTH			POLL_EN	CMD_EN	PHASE_FORMAT	DMY_BITS						DATA_EN	TRAN_CMD																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	CLK_MODE	SDR. 000: SDR (default) Note: Keep default	RW
28:26	ADDR_WIDTH	The width of address used in the phase. 000: no address transfer (default) 001: 1 bytes 010: 2 bytes 011: 3 bytes 100: 4 bytes 101: 5 bytes >=110: 6 bytes	RW
25	POLL_EN	The polling function means that SFC checking the flash device's	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		status. 0: no polling transfer (default) 1: has polling transfer. Note: it's priority is higher than tran_dir and data_en	
24	CMD_EN	0: no command transfer(default) 1: has command transfer	RW
23	PHASE_FORMAT	Phase format, see chapter 16.8.1 0: format0(default) 1: format1	RW
22:17	DMY_BITS	The needed dummy cycle num (unit: SFC_CLK cycle) 000000: no dummy transfer (default) 000001: 1 dummy cycles 000010: 2 dummy cycles 000011: 3 dummy cycles ..... 100000: 32 dummy cycles	RW
16	DATE_EN	0: no data transfer(default) 1: has data transfer	RW
15:0	CMD	The transfer command	RW

16.7.3.9 SFC Transfer Configure Register1 (phase0-phase5)

	SFC_TRAN_CFG1																Base + 0x009c - Base + 0x00b0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													DATA_ENDIAN	WORD_UNIT		Reserved								TRAN_MD				Reserved			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:19	Reserved	Write has no effect. Read as zero.	RW
18	DATA_ ENDIAN	0: LSB first 1: MSB first	RW
17:16	WORD_UNIT	00: 1 Byte 01: 2 Bytes 10: 4 Bytes	RW
15:8	Reserved	Write has no effect. Read as zero.	RW
7:4	TRAN_MD	Transfer mode: 0000：Standard SPI（default） 0001：Dual Input/Dual Output SPI 0010：Dual I/O SPI	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0011：Full Dual I/O SPI 0100：reserved 0101：Quad Input/Quad Output SPI 0110：Quad I/O SPI 0111：Full Quad I/O SPI 1000：reserved 1001：Octal Input/Octal Output SPI 1010：Octal I/O SPI 1011：Full Octal I/O SPI Others: reserved	
3:0	Reserved	Write has no effect. Read as zero.	RW

16.7.3.10 SFC Transfer Length Register

	SFC_TRAN_LEN																Base + 0x002c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRAN_LEN																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	TRAN_LEN	Number of bytes to be transferred. 32'h0: no data transfer Note: 1. This register should be 0 when there isn't data phase in the flow, else the DMA or RMC will start when not use DMA descriptor. 2. When CHIP_SEL==2, TRAN_LEN must be even.	RW

16.7.3.11 SFC Device Address Register (phase0 - phase5)

	SFC_DEV_ADDR0-5																Base + 0x0030 - Base + 0x0044															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_ADDR	The low bytes of flash address for transfer when do not use CDT.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

16.7.3.12 SFC Device Address Plus Register (phase0 - phase5)

	SFC_DEV_ADDR_PLUS0-5																Base + 0x0048 - Base + 0x005c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEV_ADDR_PLUS																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DEV_ADDR_PLUS	The high bytes of flash address for transfer when do not use CDT.	RW

16.7.3.13 SFC Memory Address Register

	SFC_MEM_ADDR																Base + 0x0060															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MEM_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	MEM_ADDR	Memory address for DMA when do not use DMA descriptor.	RW

16.7.3.14 SFC Trigger Register

	SFC_TRIG																Base + 0x0064															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													FLUSH	STOP	START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Write has no effect. Read as zero.	R
2	FLUSH	Write 1 to reset the FIFO. Write 0 has no effect.	W
1	STOP	Write 1 to stop all transmission. Write 0 has no effect.	W
0	START	Write 1 to start the transmission Write 0 has no effect.	W

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

16.7.3.15 SFC Status Register

	SFC_SR																													Base + 0x0068
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved									FIFO_NUM							Reserved								WORKING	BUSY		END	TRAN_REQ	RECE_REQ	OVER	UNDER
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:17	Reserved	Write has no effect. Read as zero.	R
22:16	FIFO_NUM	The quantity of data in FIFO (unit: word)	R
15:8	Reserved	Write has no effect. Read as zero.	R
7	WORKING	0: the SFC is IDLE 1: the SFC is working	R
6:5	BUSY	00: the SPI is IDLE 01: the SPI is in transaction 10: the SPI is in reception 11: the SPI is waiting for transfer	R
4	END	Indicate whether the transfer is end 0: the transfer isn't end or SFC is IDLE 1: the transfer is end This bit will generate INT_END signal.	R
3	TRAN_REQ	0: no request 1: vacancy num in FIFO is more than or equal to the threshold. This bit will generate the INT_TREQ interrupt.	R
2	RECE_REQ	0: no request 1: data num in FIFO is more than or equal to the threshold. This bit will generate the INT_RREQ interrupt.	R
1	OVER	0: no over-run 1: FIFO is over-run. This bit will generate the INT_OVER interrupt.	R
0	UNDER	0: no error. 1: FIFO is under-run This bit will generate INT_UNDR signal.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

16.7.3.16 SFC Status Clear Register

	SFC_SCR																												Base + 0x006c				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											CLR_END	CLR_TREQ	CLR_RREQ	CLR_OVER	CLR_RUNDR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Write has no effect. Read as zero.	R
4	CLR_END	0: has no effect. 1: clear the SFC_SR.END flag and the INT_END.	W
3	CLR_TREQ	0: has no effect. 1: clear the SFC_SR.TREQ flag and the INT_TREQ	W
2	CLR_RREQ	0: has no effect. 1: clear the SFC_SR.RREQ flag and the INT_RREQ	W
1	CLR_OVER	0: has no effect. 1: clear the SFC_SR.OVER flag and the INT_OVER	W
0	CLR_UNDR	0: has no effect. 1: clear the SFC_SR.UNDER flag and the INT_UNDR	W

16.7.3.17 SFC Interrupt Controller Register

	SFC_INTC																												Base + 0x0070				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											MASK_END	MASK_TREQ	MASK_RREQ	MASK_OVER	MASK_UNDR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Name	Description	RW
31:5	Reserved	Write has no effect. Read as zero.	R
4	MASK_END	0: the INT_END is not masked, will trigger interrupt signal. 1: the INT_END will be masked (default)	RW
3	MASK_TREQ	0: the INT_TREQ is not masked, will trigger interrupt signal. 1: the INT_TREQ will be masked (default)	RW
2	MASK_RREQ	0: the INT_RREQ is not masked, will trigger interrupt signal. 1: the INT_RREQ will be masked (default)	RW
1	MASK_OVER	0: the INT_OVER is not masked, will trigger interrupt signal. 1: the INT_OVER will be masked (default)	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

0	MASK_UNDR	0: the INT_UNDR is not masked, will trigger interrupt signal. 1: the INT_UNDR will be masked (default)	RW

NOTE: When the interrupt flag is cleared, the next interrupt will be generated immediately, so long as the requirement is contented.

16.7.3.18 SFC FSM Register

SFC_FSM																															Base + 0x0074
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												FSM_AHB				FSM_SPI								Reserved	FSM_DMAC			Reserved	FSM_RMC		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1

Bits	Name	Description	RW
31:20	Reserved	Write has no effect. Read as indeterminate value.	R
19:16	FSM_AHB	The AHB_master module's FSM state	R
15:8	FSM_SPI	The SPI_ctrl module's FSM state	R
7	Reserved	Write has no effect. Read as indeterminate value.	R
6:4	FSM_DMAC	The DMAC module's FSM state	R
3	Reserved	Write has no effect. Read as indeterminate value.	R
2:0	FSM_RMC	The RCM module's FSM state	R

16.7.3.19 SFC Clk_gate Enable register

SFC_CGE																															Base + 0x0078
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										CGE_FLOW_EN		CGE_DMA_EN	CGE_RMC_EN	CGE_SPI_EN	CGE_REG_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bits	Name	Description	RW
31:6	Reserved	Write has no effect. Read as indeterminate value.	R
5	CGE_FLOW_EN	0: disable the flow_ctrl modle's clk_gate function 1: enable the flow_ctrl module's clk_gate function (default)	RW
4			RW
3	CGE_DMA_EN	0: disable the dmac and ahb_mst module's clk_gate function 1: enable the dmac and ahb_mst module's clk_gate function	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		(default)	
2	CGE_RMC_EN	0: disable the rmc module's clk_gate function 1: enable the rmc module's clk_gate function (default)	RW
1	CGE_SPI_EN	0: disable the spi and clk_gen module's clk_gate function 1: enable the spi and clk_gen module's clk_gate function (default)	RW
0	CGE_REG_EN	0: disable the reg module's clk_gate function 1: enable the reg module's clk_gate function (default)	RW

Note：please disable all the clock gate function（clear all bits of SFC_CGE）

16.7.3.20 SFC CMD Index register

	SFC_CMD_IDX																Base + 0x007c													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CDT_DATA_EN	CDT_DIR	Reserved														CMD_IDX															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	CDT_DATA_EN	This command chain need data transmission.	RW
30	CDT_DIR	Direction of the data transmission. 0: read data from SPI flash 1: write data to SPI flash	RW
29:6	Reserved	Write has no effect. Read as indeterminate value.	R
5:0	CMD_IDX	The cmd index of CDT	RW

16.7.3.21 SFC Column Address Register

	SFC_COL_ADDR																Base + 0x0080													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	COL_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	COL_ADDR	Column address, cache address. just for CDT mode.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

16.7.3.22 SFC Row Address Register

	SFC_ROW_ADDR																Base + 0x0084															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ROW_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	ROW_ADDR	Row address, page address. just for CDT mode.	RW

16.7.3.23 SFC Status Address0 Register

	SFC_STA_ADDR0																Base + 0x0088															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	STA_ADDR0																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	STA_ADDR0	Status address0. just for CDT mode.	RW

16.7.3.24 SFC Status Address1 Register

	SFC_STA_ADDR1																Base + 0x008c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	STA_ADDR1																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	STA_ADDR1	Status address1. just for CDT mode.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

16.7.3.25 SFC DMA Descriptor Address Register

	SFC_DES_ADDR																Base + 0x0090															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DES_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DES_ADDR	Descriptor address for DMA.	RW

16.7.3.26 SFC CDT register

	SFC_CDT																Base + 0x0800 ~ Base + 0x0c00															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CDT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	CDT	CDT's register interface	RW

16.7.3.27 SFC Date Register

	SFC_DR																Base + 0x1000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DR	Data register interface for data buffer.	RW

16.8 Software Guideline

16.8.1 CDT Description

Each command consists of 4 words, and each one can link the next one or not.

Hardware execute one command chain each time. At most only once data transmission in one command chain.

The structure of each command as follows:

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Num	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LINK													ENDIAN	WORD_UNIT										TRAN_MODE						ADDR_KIND	
1	CLK_MODE			ADDR_WIDTH			POLL_EN	CMD_EN	PHASE_FORMAT	DMY_BITS						DATA_EN	TRAN_CMD																
2	DEV_STA_EXP																															
3	DEV_STA_MSK																															

Name	Description
LINK	1: it is not the last command of the chain. 0: it is the last command of the chain.
ADDR_KIND	0: Column address(SFC_COL_ADDR) 1: Row address(SFC_ROW_ADDR) 2: Status address0(SFC_STA_ADDR0) 3: Status address1(SFC_STA_ADDR1)
others	the definition of the rest signals are consistent with the above register definition.

16.8.2 DMA Descriptor

Each descriptor consists of 4 words. Hardware execute one descriptor chain each time.

The structure of each descriptor as follows:

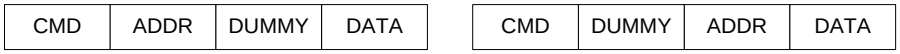
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st	NEXT_DES_ADDR																															
2nd	MEM_ADDR																															
3rd	TRAN_LEN																															
4th																																LINK

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Name	Description
NEXT_DES_ADDR	The next descriptor's phy address.
MEM_ADDR	Current transfer data phy address
TRAN_LEN	Current transfer data length
LINK	1: this is not the last descriptor. 0: this is the last descriptor.
others	the definition of the rest signals are consistent with the above register definition.

16.8.3 Phase Description

- ✧ The phase is consisted of four sections: CMD, ADDR, DUMMY, DATA.
- ✧ Each phase could have one or more sections, four at the most.
- ✧ For one section, one phase could have one at the most.
- ✧ In all phases, only one phase can have DATA section.(we call this phase as data phase, other are command phase)
- ✧ Sections in a phase will be operated by two sequence format:



Format0 Format1

- ✧ For one flow, only one kind of the direction of transmission is supported.

16.8.4 Multi phases flow

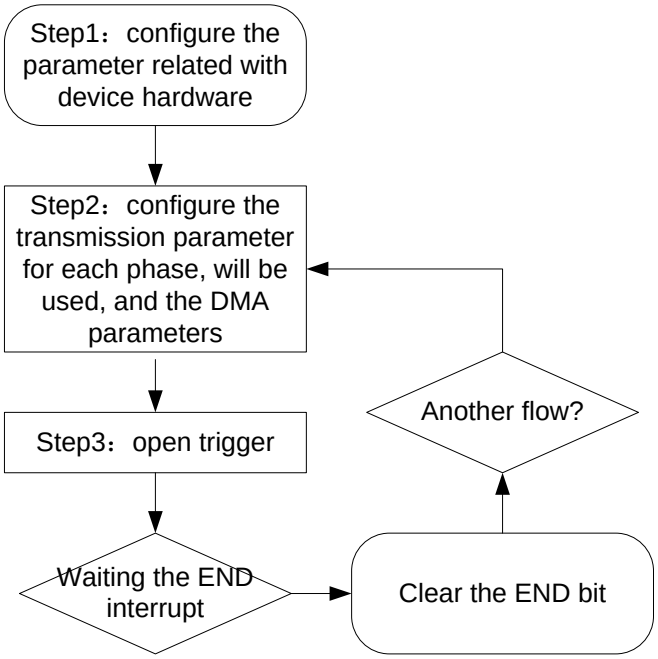


Figure 16-12 Multi phases flow

1 Configure the parameter related to the device hardware.
Such as the default level of IO port, timing parameter, etc.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

related reg：SFC_DEV_CONF

2 Configure the parameter related to this transmission flow.
Such as num of phase, command format, operation mode, source address and target address, transfer direction and length, etc.
related reg：SFC_GLB、SFC_DEV_STA_EXP、SFC_DEV_STA_MSK、SFC_TRAN_CONF0-6、SFC_TRAN_LEN、SFC_DEV_ADDR0-6、SFC_MEM_ADDR

3 Open the trigger
related reg：SFC_TRIG

4 Waiting for end_end

5 Repeat step 2 for other flow

16.8.5 One phase flow

The flow can also be executed by only one phase. The NAND write perspective flow shown in the Figure 16-13 as follow:

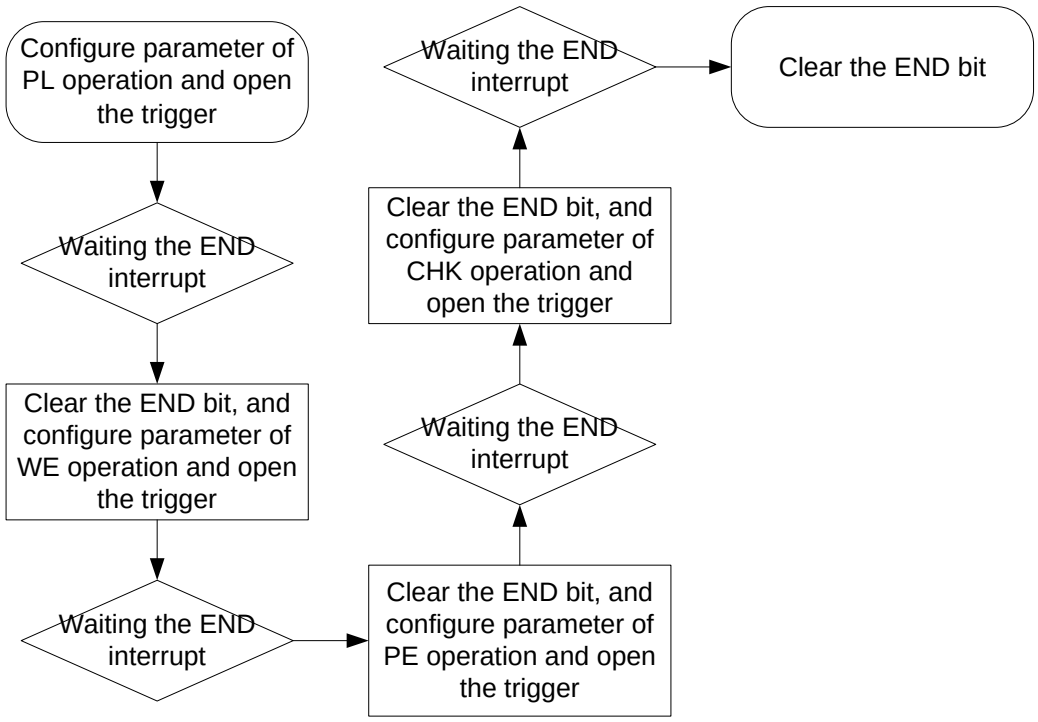


Figure 16-13 One phase flow

16.8.6 Meters of DMA operation need attention

DMA need some other parameter on the basic configuration.

- configure SFC_GLB (BURST_LEN、OP_MODE、BURST_LEN)
- configure SFC_MEM_ADDR (the memory address)

16.8.7 Meters of slave mode operation need attention

- For each data transfer phase, there must a flush operation before phase starting.
- The SFC will generate request according to the THRESHOLD. When CPU polling the SFC_SR

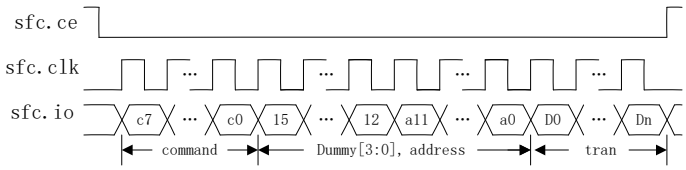
Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

register or waiting an interrupt, the number of data, that transferred by AHB bus each time must match the THRESHOLD.

16.8.8 Example (NAND flash write with multi phases in DMA mode)

a) configure SFC_DEV_CONF and SFC_GLB register

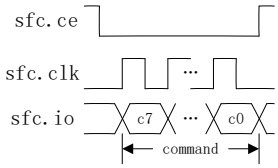
b) program load (PL)



Configure the parameter of PL into phase0 registers:

- configure the SFC_TRAN_CONF0(TRAN_MODE, CMD_EN, ADDR_WIDTH, DMY_NUM, etc)
- configure SFC_DEV_ADDR0
- configure SFC_TRAN_LEN

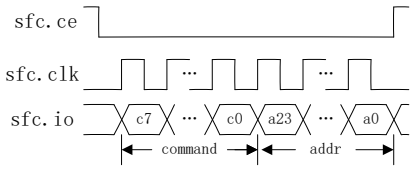
c) write enable (WE)



Configure the parameter of WE into phase1 registers:

- configure SFC_TRAN_CONF1(TRAN_MODE, CMD_EN, CMD, etc)

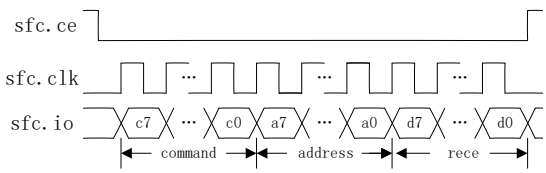
d) program execute



Configure the parameter of PE into phase2 registers:

- configure SFC_TRAN_CONF2(TRAN_MODE, CMD_EN, ADDR_WIDTH, CMD, etc)
- configure SFC_DEV_ADDR2

e) get features command to read the status



Configure the parameter of PE into phase3 registers:

- configure SFC_TRAN_CONF3(TRAN_MODE, CMD_EN, ADDR_WIDTH, CMD, POLL_EN, etc)
- configure SFC_DEV_ADDR3

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

- configure SFC_DEV_STA_EXP
- configure SFC_DEV_STA_MSK

f) Start

g) waiting the END interrupt

h) clear the END bit zone

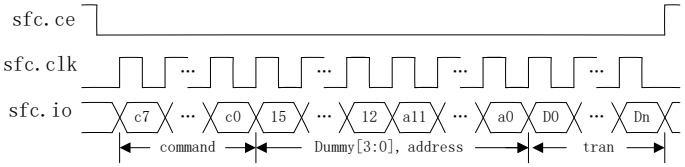
16.8.9 Example (NAND flash write with multi phases in DMA descriptor mode)

a) configure SFC_DEV_CONF and SFC_GLB register

b) configure DMA descriptor

- create dma descriptor in system mem
- configure SFC_DES_ADDR(the first descriptor phy address of the descriptor link)

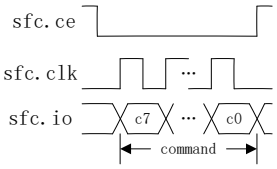
c) program load (PL)



Configure the parameter of PL into phase0 registers:

- configure the SFC_TRAN_CONF0(TRAN_MODE, CMD_EN, ADDR_WIDTH, DMY_NUM, etc)
- configure SFC_DEV_ADDR0

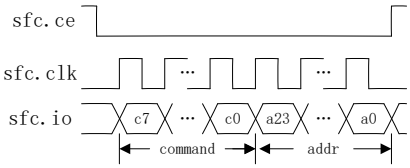
d) write enable (WE)



Configure the parameter of WE into phase1 registers:

- configure SFC_TRAN_CONF1(TRAN_MODE, CMD_EN, CMD, etc)

e) program execute

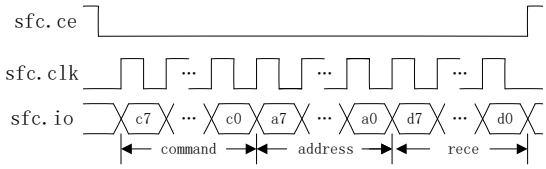


Configure the parameter of PE into phase2 registers:

- configure SFC_TRAN_CONF2(TRAN_MODE, CMD_EN, ADDR_WIDTH, CMD, etc)
- configure SFC_DEV_ADDR2

f) get features command to read the status

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.



Configure the parameter of PE into phase3 registers:

- configure SFC_TRAN_CONF3(TRAN_MODE, CMD_EN, ADDR_WIDTH, CMD, POLL_EN, etc)
- configure SFC_DEV_ADDR3
- configure SFC_DEV_STA_EXP
- configure SFC_DEV_STA_MSK

g) Start

h) waiting the END interrupt

i) clear the END bit zone

16.8.10 Example (NAND flash write with multi phases in CDT mode)

a) configure SFC_DEV_CONF and SFC_GLB register

b) configure CDT registers

c) According CDT ADDR_KIND to config Address regiters(SFC_COL_ADDR, SFC_ROW_ADDR, SFC_STA_ADDR0, SFC_STA_ADDR1)

d) configure CDT index register SFC_CMD_IDX

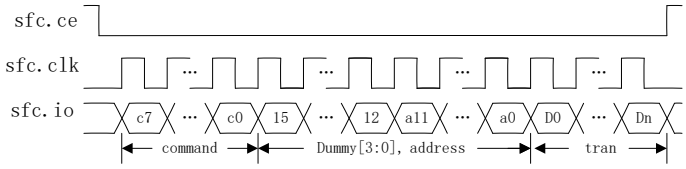
e) Start

f) Waiting END and clear.

16.8.11 Example (NAND flash write with single phase in REG mode)

a) configure SFC_DEV_CONF and SFC_GLB register

b) program load (PL)



i. Set SFC_CTRL.FLUSH

ii. Configure the parameter of PL into phase0 registers:

- configure the SFC_TRAN_CONF0(TRAN_MODE, CMD_EN, ADDR_WIDTH, DMY_NUM, etc)
- configure SFC_DEV_ADDR0
- configure SFC_TRAN_LEN
- configure SFC_GLB.TRANS_DIR

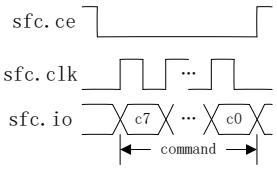
iii. Start

iv. waiting SFC_SR.TREQ and clear, then set data to FIFO according to the THRESHOLD. Looping until all data trans end.

v. Waiting END and clear.

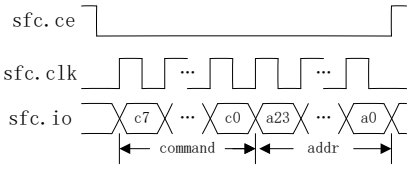
Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

c) write enable (WE)



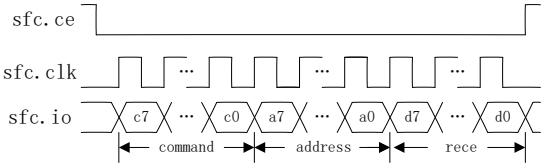
i. Configure the parameter of WE into phase0 registers:
– configure SFC_TRAN_CONF0(TRAN_MODE, CMD_EN, CMD, etc)
ii. Start
iii. Waiting END and clear.

d) program execute



i. Configure the parameter of PE into phase0 registers:
– configure SFC_TRAN_CONF0(TRAN_MODE, CMD_EN, ADDR_WIDTH, CMD, etc)
– configure SFC_DEV_ADDR0
ii. Start
iii. Waiting END and clear.

e) get features command to read the status



i. Configure the parameter of PE into phase0 registers:
– configure SFC_TRAN_CONF0(TRAN_MODE, CMD_EN, ADDR_WIDTH, CMD, etc)
– configure SFC_DEV_ADDR0
– configure SFC_TRANS_LEN
– configure SFC_GLB.TRANS_DIR
ii. Start
iii. waiting SFC_SR.RREQ and clear, then get data from FIFO according to the THRESHOLD. Looping until all data trans end.
iv. Waiting END and clear.

16.9 Index

Table 16-3 Terms and Abbreviations

Name	Description
AHB	Advanced Microcontroller Bus Architecture

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Dual SPI	See SPI
CPU	Central Processing Unit
DMA	Direct Memory Access
LUT	Look up table.
Endian	The convention used to interpret the bytes making up a data word when those bytes are stored in computer memory. See Endianness at Wikipedia
FIFO	First In, First Out, a method for organizing and manipulating a data buffer
LSB	See Endian
MSB	See Endian
Quad SPI	See SPI
SPI	Serial Peripheral Interface
Standard SPI	See SPI
tCHSH	Time from clock pull high to select pull low. See a NOR Flash device spec
tSHSL	Time from select pull high to select pull low. See a NOR Flash device spec
tSLCH	Time from select pull low to clock pull high. See a NOR Flash device spec

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Section 6

SYSTEM FUNCTIONS

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

17 Clock Reset and Power Controller

17.1 Overview

The Clock & Power management block consists of: Clock control, PLL control, and Power control, Reset control.

The Clock control logic can generate the required clock signals including CCLK for CPU/L2CACHE, HHCLK for BIU, H0CLK for the AHB0, H2CLK for the AHB2, PCLK for the APB bus peripherals , DDR_CLK for DDR.

The Chip has three Phase Locked Loops (PLL):

1. APLL mainly is used to CPU and L2CACHE, also may use the AHB0 and AHB2, or other peripherals
2. MPLL mainly is used to DDR, also uses AHB0 and AHB2 APB, or other peripherals
3. EPLL mainly is used to AUDIO and other peripherals.

For the power control logic, there are various power management schemes to keep optimal power consumption for a given task. The power management block can activate four modes: NORMAL mode, IDLE mode, PD_IDLE mode, SLEEP mode.

For reset control logic, the hardware reset and hibernate reset is extended to more 10ms. It controls or distributes all of the system reset signals.

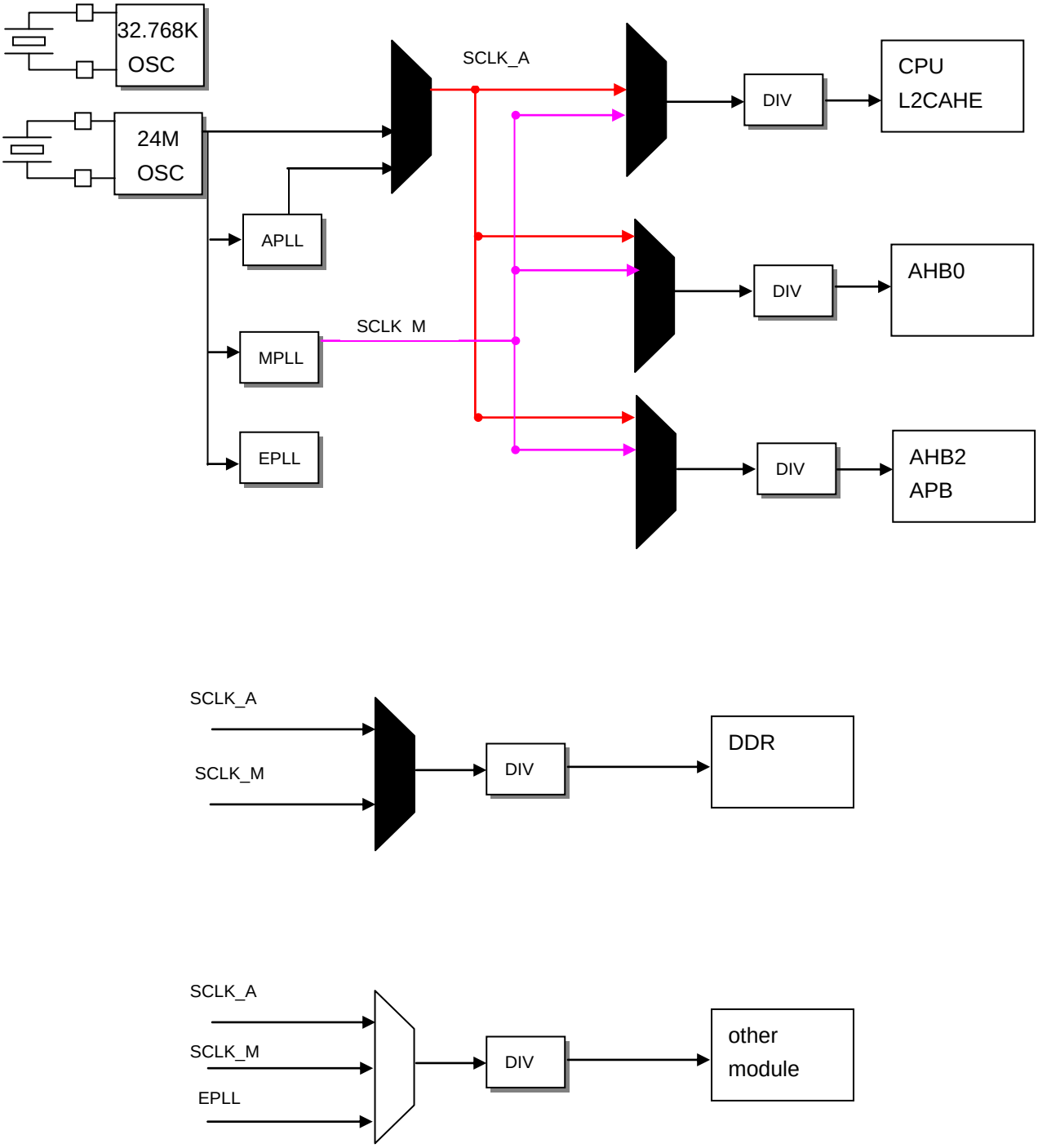
Feature:

- On-chip 2MHz~27MHZ oscillator circuit
- On-chip 32.768KHZ oscillator circuit
- One three-chip phase-locked loops (PLL) with programmable multiplier
- CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK frequency can be changed separately for software by setting registers
- MSC clock supports 100M clock
- Functional-unit clock gating

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

17.1.1 CGU Block Diagram

Following figure illustrates a block diagram of CGU.



Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Note:

Clock mux **in grey color** represents **glitch-free** clock mux, which is free of glitches if clock selection is changed. Clock mux in white color represents non-glitch-free clock mux, which can suffer from glitches when changing clock sources. **Care must be taken in using each of clock muxes**.

17.1.2 CGU Registers

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

Table 17-1 Registers Memory Map-Address Base

Name	Base	Description
CPM	0x10000000	Address base of CPM

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Table 17-2 CGU Registers Configuration

Name	description	RW	Reset Value	Address offset	Access Size
CPCCR	Clock Control Register	RW	0x95000000	0x0000	32
CPCSR	Clock status register	RW	0x00000000	0x00D4	32
DDCDR	DDR clock divider Register	RW	0x40000000	0x002C	32
MACPHYCDR	MACPHY divider Register	RW	0x00000000	0x0054	32
MACTXCDR	MACTX divider Register	RW	0x00000000	0x0058	32
MACTXCDR1	MACTX1 divider Register	RW	0x00000000	0x00DC	32
MACPTPCDC	MACPTP divider Register	RW	0x00000000	0x004C	32
I2S0CDR	I2S device clock divider Register	RW	0x00000000	0x0060	32
I2S0CDR1	I2S device clock divider Register	RW	0x00000000	0x0070	32
I2S1CDR	I2S device clock divider Register	RW	0x00000000	0x007C	32
I2S1CDR1	I2S device clock divider Register	RW	0x00000000	0x0080	32
I2S2CDR	I2S device clock divider Register	RW	0x00000000	0x0084	32
I2S2CDR1	I2S device clock divider Register	RW	0x00000000	0x0088	32
I2S3CDR	I2S device clock divider Register	RW	0x00000000	0x008C	32
I2S3CDR1	I2S device clock divider Register	RW	0x00000000	0x00A0	32
AUDIOCR	Audio clock control Register	RW	0x00000000	0x00AC	32
LPCDR	LCD pix clock divider Register	RW	0x00000000	0x0064	32
MSC0CDR	MSC0 clock divider Register	RW	0x40000000	0x0068	32
MSC1CDR	MSC1 clock divider Register	RW	0x00000000	0x00A4	32
MSC2CDR	MSC2 clock divider Register	RW	0x00000000	0x00A8	32
SFCCDR	SFC clock divider Register	RW	0x00000000	0x0074	32
SSICDR	SSI clock divider Register	RW	0x00000000	0x005C	32
CIMCDR	CIM MCLK clock divider Register	RW	0x00000000	0x0078	32
PWMCDR	PWM clock divider Register	RW	0x00000000	0x006C	32
RSACDR	RSA clock divider Register	RW	0x00000000	0x0050	32
MACPHYC0	GMAC0 PHY Control Register	RW	0x00000000	0x00E4	32
MACPHYC1	GMAC1 PHY Control Register	RW	0x00000000	0x00E8	32
CPM_INTR	CPM interrupt Register	RW	0x00000000	0x00B0	32
CPM_INTRE	CPM interrupt Enable Register	RW	0x00000000	0x00B4	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

CPM_SFTINT	CPM software interrupt	RW	0x00000000	0x00BC	32
DRCG	DDR clk gate register	RW	0x00000001	0x00D0	32
CPSPR	CPM Scratch Pad Register	RW	0x????????	0x0034	32
CPSPPR	CPM Scratch Protected Register	RW	0x0000a5a5	0x0038	32
USBPCR	USB Parameter control register	RW	0x409919b8	0x003C	32
USBRDT	USB Reset Detect Timer Register	RW	0x02000096	0x0040	32
USBVBFIL	USB jitter filter Register	RW	0x00ff0080	0x0044	32
USBPCR1	USB Parameter control register 1	RW	0x00000004	0x0048	32
CPPCR	PLL Control Register	RW	0x00000020	0x000C	32
CPAPCR	APLL Control Register	RW	0x06305060	0x0010	32
CPMPCR	MPLL Control Register	RW	0x06305060	0x0014	32
CPEPCR	EPLL Control Register	RW	0x06305060	0x0018	32

17.1.2.1 Clock Control Register(CPCCR,0x00)

The Clock Control Register (CPCCR) is a 32-bit read/write register, which controls CCLK, H0CLK, H2CLK and PCLK division ratios. It is initialized to 0x95000000 by any reset. Only word access can be used on CPCCR.

	CPCCR																BASE+0x00													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SEL_SRC		SEL_CPLL		SEL_H0PLL		SEL_H2PLL		GATE_SCLKA	CE_CPU	CE_AHB0	CE_AHB2	PDIV				H2DIV				H0DIV				L2CDIV				CDIV			
RST	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	SEL_SRC	00: stop MUX clock output 01: EXCLK 10: APLL The mux clock output is SCLK_A The clock mux is free of glitches if clock selection is changed When switching clock source, it should be ensured that the clock switched from and the clock switched to both are running.	RW
29:28	SEL_CPLL	00: stop MUX clock output 01: SCLK_A 10: MPLL	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td></td><td></td><td>The mux clock output is to CPU and L2CAHE
The clock mux is free of glitches if clock selection is changed
When switching clock source, it should be ensured that the clock switched from and the clock switched to both are running.</td><td></td></tr>
<tr><td>27:26</td><td>SEL_H0PLL</td><td>00: stop MUX clock output
01: SCLK_A
10: MPLL
The mux clock output is to AHB0
The clock mux is free of glitches if clock selection is changed
When switching clock source, it should be ensured that the clock switched from and the clock switched to both are running.</td><td>RW</td></tr>
<tr><td>25:24</td><td>SEL_H2PLL</td><td>00 : stop MUX clock output
01: SCLK_A
10: MPLL
The mux clock output is to AHB2
The clock mux is free of glitches if clock selection is changed
When switching clock source, it should be ensured that the clock switched from and the clock switched to both are running.</td><td>RW</td></tr>
<tr><td>23</td><td>GATE_SCLKA</td><td>0: SCLK_A not gating
1: SCLK_A is gating.
Gating modules: LCD MSC MAC AIC USB SSI PCM CIM etc</td><td>RW</td></tr>
<tr><td>22</td><td>CE_CPU</td><td>Change enable for CPU and L2CAHE. If CE_CPU is 1 , write on CDIV,
L2CDIV will start a frequency changing sequence immediately. If CE_CPU is 0, writes on CDIV and L2CDIV have no affect.</td><td>RW</td></tr>
<tr><td>21</td><td>CE_AHB0</td><td>Change enable for AHB0. If CE_AHB0 is 1 , write on H0DIV will start a frequency changing sequence immediately. If CE_AHB0 is 0, writes on H0DIV have no affect.</td><td>RW</td></tr>
<tr><td>20</td><td>CE_AHB2</td><td>Change enable for AHB2. If CE_AHB2 is 1 , write on H2DIV, PDIV will start a frequency changing sequence immediately. If CE_AHB2 is 0, writes on H2DIV, PDIV have no affect.</td><td>RW</td></tr>
<tr><td>19:16</td><td>PDIV</td><td>Divider for Peripheral Frequency. Specified the PCLK division ratio.
<table>
<tr><th colspan="4">Bit 19~16: PDIV</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>X1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>X1/2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>X1/3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>X1/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>X1/5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>X1/6</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>X1/7</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>X1/8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>X1/9</td></tr>
</table></td><td>RW</td></tr>
</table>

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

			1	0	0	1	X1/10	
			1	0	1	0	X1/11	
			1	0	1	1	X1/12	
			1	1	0	0	X1/13	
			1	1	0	1	X1/14	
			1	1	1	0	X1/X15	
			1	1	1	1	X1/16	
15:12	H2DIV	Divider for AHB2 Frequency. Specified the AHB2 CLK division ratio.						RW
			Bit 15~12: H2DIV				Description	
			0	0	0	0	X1	
			0	0	0	1	X1/2	
			0	0	1	0	X1/3	
			0	0	1	1	X1/4	
			0	1	0	0	X1/5	
			0	1	0	1	X1/6	
			0	1	1	0	X1/7	
			0	1	1	1	X1/8	
			1	0	0	0	X1/9	
			1	0	0	1	X1/10	
			1	0	1	0	X1/11	
			1	0	1	1	X1/12	
			1	1	0	0	X1/13	
			1	1	0	1	X1/14	
			1	1	1	0	X1/15	
			1	1	1	1	X1/16	
11:8	H0DIV	Divider for AHB0 Frequency. Specified the AHB0 CLK division ratio.						RW
			Bit 11~8: H0DIV				Description	
			0	0	0	0	X1	
			0	0	0	1	X1/2	
			0	0	1	0	X1/3	
			0	0	1	1	X1/4	
			0	1	0	0	X1/5	
			0	1	0	1	X1/6	
			0	1	1	0	X1/7	
			0	1	1	1	X1/8	
			1	0	0	0	X1/9	
			1	0	0	1	X1/10	
			1	0	1	0	X1/11	
			1	0	1	1	X1/12	
			1	1	0	0	X1/13	
			1	1	0	1	X1/14	

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

			1	1	1	0	X1/15	
			1	1	1	1	X1/16	
7:4	L2CDIV	Divider for L2CACHE output bus（BIU）Frequency. Specified the L2C CLK division ratio.						RW
			Bit 7~4: L2CDIV				Description	
			0	0	0	0	1	
			0	0	0	1	X1/2	
			0	0	1	0	X1/3	
			0	0	1	1	X1/4	
			0	1	0	0	X1/5	
			0	1	0	1	X1/6	
			0	1	1	0	X1/7	
			0	1	1	1	X1/8	
			1	0	0	0	X1/9	
			1	0	0	1	X1/10	
			1	0	1	0	X1/ 1	
			1	0	1	1	X1/12	
			1	1	0	0	X1/13	
			1	1	0	1	X1/14	
			1	1	1	0	X1/15	
			1	1	1	1	X1/16	
3:0	CDIV	Divider for CPU Frequency. Specified the CPU CLK division ratio.						
			Bit 3~0: CDIV				Description	
			0	0	0	0	X1	
			0	0	0	1	X1/2	
			0	0	1	0	X1/3	
			0	0	1	1	X1/4	
			0	1	0	0	X1/5	
			0	1	0	1	X1/6	
			0	1	1	0	X1/7	
			0	1	1	1	X1/8	
			1	0	0	0	X1/9	
			1	0	0	1	X1/10	
			1	0	1	0	X1/11	
			1	0	1	1	X1/12	
			1	1	0	0	X1/13	
			1	1	0	1	X1/14	
			1	1	1	0	X1/15	
			1	1	1	1	X1/16	

Import Note1 : for PDIV and AHB2DIV, AHB2's clock frequency must be 1 or 2 times of PDIV's clock frequency. For L2CDIV and CDIV, CPU's clock frequency must be 1,2,3, or 4 times of

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

L2CACHE's clock frequency.

Import Note2 : After reset, H0DIV and CE_AHB0 will be zero, and ahb0's clock freq and apb0's clock freq will be 1:1, but if you have ever set CE_AHB0 and change the value of H0DIV, ahb0's clock freq and apb0's clock freq will be 2:1 from then on.

17.1.2.2 Clock Status Register(CPCSR,0xD4)

Clock status register (CPCSR) is a 32-bit read/write register that specifies the status of CPCCR .This register is initialized to 0x00000000 only by any reset. Only word access can be used on CPCSR.

	CPCSR																													BASE+0xD4	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRC_MUX	CPU_MUX	AHB0_MUX	AHB2_MUX	DDR_MUX	Reserved																								H2DIV_BUSY	H0DIV_BUSY	CDIV_BUSY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	SRC_MUX	0: it indicates that mux switch has not stable 1: it indicates that mux switch has stable Software must check the value, then go next	R
30	CPU_MUX	0: it indicates that mux switch has not stable 1: it indicates that mux switch has stable Software must check the value, then go next	R
29	AHB0_MUX	0: it indicates that mux switch has not stable 1: it indicates that mux switch has stable Software must check the value, then go next	R
28	AHB2_MUX	0: it indicates that mux switch has not stable 1: it indicates that mux switch has stable Software must check the value, then go next	R
27	DDR_MUX	0: it indicates that mux switch has not stable 1: it indicates that mux switch has stable Software must check the value, then go next	R
26:3	Reserved	Writing has no effect, read as zero.	R
2	H2DIV_BUSY	The bit is a read-only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until H2DIV_BUSY == 0, then may begin another frequency change.	R
1	H0DIV_BUSY	The bit is a read-only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished.,	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		otherwise it indicates the frequency change is on going Software should be wait until H0DIV_BUSY == 0, then may begin another frequency change.	
0	CDIV_BB BUSY	The bit is a read-only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until CDIV_BUSY == 0, then may begin another frequency change.	R

17.1.2.3 DDR Memory clock divider Register(DDRCDR,0x2C)

DDR memory clock divider Register (DDRCDR) is a 32-bit read/write register that specifies the divider of DDR memory clock . This register is initialized to 0x40000000 only by any reset. Only word access can be used on DDRCDR.

	DDRCDR																BASE+0x002C														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCS		CE_DDR	DDR_BUSY	DDR_STOP	GATE_EN	CHANGE_EN	FLAG	DDR_PHY_GATE	Reserved																			DDRCDR			
RST	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	DCS	DDR Clock Source Selection. Selects the DDR clock source between APLL output and MPLL output. 00: stop MUX clock output 01: DDR clock source is SCLK_A 10: DDR clock source is MPLL The clock mux is free of glitches if clock selection is changed When switching clock source, it should be ensured that the clock switched from and the clock switched to both are running.	RW
29	CE_DDR	Change enable for DDR. If CE_DDR is 1 , write on DDRCDR will start a frequency changing sequence immediately. If CE_DDR is 0, writes on DDRCDR have no affect	RW
28	DDR_BU SY	The bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until DDR_BUSY == 0, then may begin another frequency change.	R
27	DDR_ST OP	When DDR_STOP is 1 and CE_DDR is 1, the DDR clock will stop. When DDR_STOP is 0 and CE_DDR is 1, the DDR clock will continue.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Software should wait until DDR_BUSY == 0, then may begin another frequency change. DDR_STOP is prior to DDRCDR.	
~~26~~	~~GATE_EN~~	~~1'b1: if DDR gives a clock stop request to CPM, and CPM will gate DDR's clock~~.	
~~25~~	~~CHANGE_EN~~	~~When this bit set high, CPM will change DDR's clock when CE_DDR is high and FLAG is low~~	RW
~~24~~	~~FLAG~~	~~1: DDR reject frequency change~~ ~~0: DDR not reject frequency change~~	R
~~23~~	~~DDR_PHY_GATE~~	~~0: not gate DDR PHY clock~~ ~~1: gate DDR PHY clock~~	RW
22:4	Reserved	Writing has no effect, read as zero.	R
3:0	DDRCDR	Divider for DDR Frequency. Specified the DDR memory clock division ratio, which varies from 1 to 16 (division ratio = DDRCDR + 1).	RW

17.1.2.4 MACPHY clock divider Register(MACCDR,0x54)

MAC clock divider Register (MACCDR) is a 32-bit read/write register that specifies the divider of MAC PHY clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on MACCDR.

	MACCDR																															BASE+0x54
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MACPCS		CE_MAC	MAC_BUSY	MAC_STOP	Reserved																			MACCDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	MACPCS	MAC PHY Clock Source Selection. Selects the MAC PHY clock source 00: MAC PHY clock source is SCLK_A 01: MAC PHY clock source is MPLL 10: MAC PHY clock source is EPLL It is no glitch free mux.	RW
29	CE_MAC	Change enable for MAC. If CE_MAC is 1 , write on MACCDR ill start a frequency changing sequence immediately. If CE_MAC is 0, writes on MACCDR have no affect	RW
28	MAC_BUSY	The bit is read only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should wait until MAC_BUSY == 0, may begin another frequency change.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

27	MAC_STOP	When MAC_STOP is 1 and CE_MAC is 1, the MAC clock will stop. When MAC_STOP is 0 and CE_MAC is 1, the MAC clock will continue. Software should wait until MAC_BUSY == 0, may begin another frequency change.	RW
26:8	Reserved	Writing has no effect, read as zero.	R
7:0	MACCDR	Divider for MAC PHY Frequency. Specified the MAC device clock division ratio division ratio = MACCDR + 1	RW

17.1.2.5 MACTXPHY clock divider Register(MACTXCDR,0x58)

MAC TX clock divider Register (MACTXCDR) is a 32-bit read/write register that specifies the divider of MAC TX clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on MACTXCDR.

	MACTXCDR																														
																													BASE+0x58		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MACTCS		CE_MACTX	MTX_BUSY	MTX_STOP	Reserved																			MACTXCDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	MACTCS	MAC TX PHY Clock Source Selection. Selects the MAC TX PHY clock source 00: MAC TX PHY clock source is SCLK_A 01: MAC TX PHY clock source is MPLL 10: MAC TX PHY clock source is EPLL It is no glitch free mux.	RW
29	CE_MACTX	Change enable for MAC TX. If CE_MACTX is 1 , write on MACTXCDR ill start a frequency changing sequence immediately. If CE_MACTX is 0, writes on MACTXCDR have no affect	RW
28	MTX_BUSY	The bit is read only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should wait until MTX_BUSY == 0, may begin another frequency change.	R
27	MTX_STOP	When MTX_STOP is 1 and CE_MTX is 1, the MTX clock will stop. When MTX_STOP is 0 and CE_MTX is 1, the MTX clock will continue. Software should wait until MTX_BUSY == 0, may begin another frequency change.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

26:8	Reserved	Writing has no effect, read as zero.	R
7:0	MACTXCDR	Divider for MACTX PHY Frequency. Specified the MAC device clock division ratio division ratio = MACTXCDR + 1	RW

17.1.2.6 MACTXPHY1 clock divider Register(MACTXCDR1,0xDC)

MAC TX clock divider Register (MACTXCDR1) is a 32-bit read/write register that specifies the divider of MAC TX clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on MACTXCDR1.

	MACTXCDR1																BASE+0xDC													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MACTCS		CE_MACTX	MTX_BUSY	MTX_STOP	Reserved																			MACTXCDR1							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	MACTCS	MAC TX PHY Clock Source Selection. Selects the MAC TX PHY clock source 00: MAC TX PHY clock source is SCLK_A 01: MAC TX PHY clock source is MPLL 10: MAC TX PHY clock source is EPLL It is no glitch free mux.	RW
29	CE_MACTX	Change enable for MAC TX. If CE_MACTX is 1 , write on MACTXCDR ill start a frequency changing sequence immediately. If CE_MACTX is 0, writes on MACTXCDR have no affect	RW
28	MTX_BUSY	The bit is read only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should wait until MTX_BUSY == 0, may begin another frequency change.	R
27	MTX_STOP	When MTX_STOP is 1 and CE_MTX is 1, the MTX clock will stop. When MTX_STOP is 0 and CE_MTX is 1, the MTX clock will continue. Software should wait until MTX_BUSY == 0, may begin another frequency change.	RW
26:8	Reserved	Writing has no effect, read as zero.	R
7:0	MACTXCDR1	Divider for MACTX PHY Frequency. Specified the MAC device clock division ratio division ratio = MACTXCDR1 + 1	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

17.1.2.7 MACPTP clock divider Register(MACPTPCDR,0x4c)

MAC PTP clock divider Register (MACPTPCDR) is a 32-bit read/write register that specifies the divider of MAC PTP clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on MACPTPCDR.

	MACTXCDR																BASE+0x4C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MPTP_CS		CE_MPTP	MPTP_BUSY	MPTP_STOP	Reserved																			MACPTPCDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	MPTP_CS	MAC PTP Clock Source Selection. Selects the MAC PTP clock source 00: MAC PTP clock source is SCLK_A 01: MAC PTP clock source is MPLL 10: MAC PTP clock source is EPLL It is no glitch free mux.	RW
29	CE_MPTP	Change enable for MAC PTP. If CE_MACTX is 0, writes on MACPTPCDR have no affect	RW
28	MPTP_BUSY	The bit is read only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished. otherwise it indicates the frequency change is on going Software should wait until MPTP_BUSY == 0, may begin another frequency change.	R
27	MPTP_STOP	When MPTP_STOP is 1 and CE_MPTP is 1, the MPTP clock will stop. When MPTP_STOP is 0 and CE_MPTP is 1, the MPTP clock will continue. Software should wait until MPTP_BUSY == 0, may begin another frequency change.	RW
26:8	Reserved	Writing has no effect, read as zero.	R
7:0	MACPTPCDR	Divider for MACPTP PHY Frequency. Specified the MAC ptp clock division ratio division ratio = MACTXCDR + 1	RW

17.1.2.8 I2S device clock divider Register(I2SxCDR,0x60/7c/84/8c)

I2S device clock divider Register (I2SxCDR) is a 32-bit read/write register that specifies the divider of I2S device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on I2SxCDR.(adr offset: **I2S0: 0x60, I2S1:0x7c I2S2:0x84 I2S3: 0x8c)**

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Note: I2S0 for i2s0_rclk、i2s1_rclk; I2S1 for i2s0_dev_tclk、i2s1_dev_tclk

	I2SxCDR																BASE+0x60/7c/84/8c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	I2PCS	CE_I2S	I2SDIV_M									I2SDIV_N																			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Reserved	Writing has no effect, read as zero.	R
30	I2PCS	0: SCLK_A output 1: EPLL output	RW
29	CE_I2S	AIC M/N divider(1) enable.	RW
28:20	I2SDIV_M	Number M of AIC M/N divider(1).	RW
19:0	I2SDIV_N	Number N of AIC M/N divider(1).	RW

Note (1): AIC M/N divider is a decimal divider. The output clock frequency of AIC M/N divider is:

Fout = Fin * M / N.

N should not be less than M*2.

AIC M/N divider output clock duty cycle is possible not 50%. But adjusting the M and N value, which makes the duty cycle is close to 50%. Error of duty cycle is:

De_p = (ceill(N / M) - (N / M)) / (N / M). ceil: Round toward positive infinity.

and:

De_n = (floor(N / M) - (N / M)) / (N / M). floor: Round toward negative infinity.

Recommend the De_p is less than 5% and De_n is great than -5%.

17.1.2.9 I2S device clock divider Register1(I2SxCDR1,0x70/80/88/A0)

I2S device clock divider Register 1(I2SxCDR1) is a 32-bit read/write register that specifies the divider of I2S device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on I2SxCDR1. (**address offset: I2S0: 0x70 I2S1: 0x80 I2S2:0x88 I2S3: 0xA0**)

	I2SxCDR1																BASE+0x70/80/88/A0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	I2S_NEN	I2S_DEN	Reserved										I2SDIV_D																			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31	I2S_NEN	0: The number N of AIC M/N divider is automatic calculate. 1: The number N of AIC M/N divider is set by I2SDIV_N. The automatic calculation is: $f_{out} = f_{in} * M/(N-0x1fff+M)$	RW
30	I2S_DEN	0: The number D of AIC M/N divider is automatic calculate. 1: The number D of AIC M/N divider is set by I2SDIV_D.	RW
29:20	Reserved	Writing has no effect, read as zero.	R
19:0	I2SDIV_D	The number D of AIC M/N divider(2).	RW

Note (2): General D = N/2. Normal we can keep I2S_DEN \ I2S_NEN to '0' and don't care 'I2SDIV_D'.

There is a little mistake in this register: the 30 and 31 bit is miss-connected. For example, write 30 bit to "1", but it will be reflected in 31 bit； write 31 bit to "1", but it will be reflected in 30 bit.

17.1.2.10 Audio clock control Register(AUDIOCR,0xAC)

Audio clock control Register is a 32-bit read/write register that specifies the divider of I2S device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on AUDIOCR.

	AUDIOCR																														BASE+0xAC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMIC_EXCLK_EN	AUDIO_RAM_SEL	Reserved																									SPDIF_SEL		PCM_SEL		DMIC_SEL
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	DMIC_EXCLK_EN	0: enable 1: disable	RW
30	AUDIO_RAM_SEL	0: select HCLK 1: EXCLK	RW
29:5	Reserved	Writing has no effect, read as zero.	
4:3	SPDIF_SEL	00: I2S0 01: I2S1 10: I2S2 11: I2S3	RW
2:1	PCM_SEL	00: I2S0 01: I2S1 10: I2S2	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		11: I2S3	
0	DMIC_SEL	0 : EXCLK 1: I2S3	RW

17.1.2.11 LCD pix clock divider Register(LPCDR,0x64)

LCD pix clock divider Register (LPCDR) is a 32-bit read/write register that specifies the divider of LCD pixel clock (LPCLK). This register is initialized to 0x00000000 by any reset. Only word access can be used on LPCDR.

	LPCDR																													BASE+0x64
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LPCS		CE_LCD	LCD_BUSY	LCD_STOP	LCD_IO_INV	Reserved																		LPCDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	LPCS	00: SCLK_A output 01: MPLL output 10: EPLL It is no glitch free mux. Software should be stop PIX clock, when change this bit.	RW
29	CE_LCD	Change enable for LCD. If CE_LCD is 1 , write on LPCDR will start a frequency changing sequence immediately. If CE_LCD is 0, writes on LPCDR have no affect	RW
28	LCD_BUSY	The bit is read only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until LCD_BUSY == 0, may begin another frequency change.	R
27	LCD_STOP	When LCD_STOP is 1 and CE_LCD is 1, the LCD clock will stop. When LCD_STOP is 0 and CE_LCD is 1, the LCD clock will continue. Software should wait until LCD_BUSY == 0, may begin another frequency change. LCD_STOP is prior to LPCDR. If system don't use this module, may set this bit to reduce power .	RW
26	LCD_IO_INV	LCD IO clock invert enable.	RW
25:8	Reserved	Writing has no effect, read as zero.	RW
7:0	LPCDR	Divider for Pixel Frequency. Specified the LCD pixel clock (LPCLK) division ratio, which varies from 1 to 256 (division ratio = LPCDR + 1).	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

17.1.2.12 MSC0 device clock divider Register(MSC0CDR,0x68)

MSC0 device clock divider Register (MSC0CDR) is a 32-bit read/write register that specifies the divider of MSC0 device clock . This register is initialized to 0x40000000 only by any reset. Only word access can be used on MSC0CDR.

	MSC0CDR																													BASE+0x68
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MPCS		CE_MSC0	MSC0_BUSY	MSC0_STOP	Reserved					MSC_EXCK_E	TUNING_DIS	RX_SEL			TX_SEL	Reserved								MSC0CDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	MPCS	00: select SCLK_A clock output 01: select MPLL clock output 10: EXCLK The clock mux is not free of glitches if clock selection is changed The clock mux output is to MSC0, MSC1 . It is source clock of MSC0, MSC1.	RW
29	CE_MSC0	Change enable for MSC0. If CE_MSC0 is 1 , write on MSC0CDR ill start a frequency changing sequence immediately. If CE_MSC0 is 0, writes on MSC0CDR have no affect	RW
28	MSC0_BUSY	The bit is read only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until MSC0_BUSY == 0, may begin another frequency change.	R
27	MSC0_STOP	When MSC0_STOP is 1 and CE_MSC0 is 1, the MSC0 clock will stop. When MSC0_STOP is 0 and CE_MSC0 is 1, the MSC0 clock will continue. Software should wait until MSC0_BUSY == 0, may begin another frequency change.MSC0_STOP is prior to MSC0CDR. If system don't use this module, may set this bit to reduce power .	RW
26:22	Reserved	Writing has no effect, read as zero.	R
21	MSC_EXCK_E	0: disable 1: enable	RW
20	TUNING_DIS	Tuning disable, software adjust rx phase	RW
19:17	RXCLK_SEL	MSC sample clock selection: 000: Sample clock is 0-degree phase shifted by device clock	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		001: Sample clock is 45-degree phase shifted by device clock 010: Sample clock is 90-degree phase shifted by device clock 011: Sample clock is 135-degree phase shifted by device clock 100: Sample clock is 180-degree phase shifted by device clock 101: Sample clock is 225-degree phase shifted by device clock 110: Sample clock is 270-degree phase shifted by device clock 111: Sample clock is 325-degree phase shifted by device clock	
16:15	TX_SEL	MSC transmit clock selection: 00: 90-degree 01: 135-degree 10: 180-degree 11: 270-degree	RW
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	MSC0CDR	Divider for MSC0 Frequency. Specified the MSC0 device clock division ratio division ratio = (MSC0CDR + 1)*4.	RW

17.1.2.13 MSC1 device clock divider Register(MSC1CDR,0xA4)

MSC1 device clock divider Register (MSC1CDR) is a 32-bit read/write register that specifies the divider of MSC1 device clock . This register is initialized to 0x40000000 only by any reset. Only word access can be used on MSC1CDR.

	MSC1CDR																														BASE+0xA4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MPCS		CE_MSC1	MSC1_BUSY	MSC1_STOP	Reserved						TUNING_DIS	RX_SEL			TX_SEL	Reserved								MSC1CDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	MPCS	00: select SCLK_A clock output 01: select MPLL clock output 10: EXCLK The clock mux is not free of glitches if clock selection is changed The clock mux output is to MSC0, MSC1, MSC2 . It is source clock of MSC0, MSC1, MSC2.	RW
29	CE_MSC1	Change enable for MSC1. If CE_MSC1 is 1 , write on MSC1CDR ill start a frequency changing sequence immediately. If CE_MSC1 is 0, writes on MSC1CDR have no affect	RW
28	MSC1_BUSY	The bit is read only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Software should be wait until MSC1_BUSY == 0, may begin another frequency change.	
27	MSC1_STOP	When MSC1_STOP is 1 and CE_MSC1 is 1, the MSC1 clock will stop. When MSC1_STOP is 0 and CE_MSC1 is 1, the MSC1 clock will continue. Software should wait until MSC1_BUSY == 0, may begin another frequency change.MSC1_STOP is prior to MSC1CDR. If system don't use this module, may set this bit to reduce power .	RW
26:21	Reserved	Writing has no effect, read as zero.	R
20	TUNING_DIS	Tuning disable, software adjust rx phase	RW
19:17	RXCLK_SEL	MSC sample clock selection: 000: Sample clock is 0-degree phase shifted by device clock 001: Sample clock is 45-degree phase shifted by device clock 010: Sample clock is 90-degree phase shifted by device clock 011: Sample clock is 135-degree phase shifted by device clock 100: Sample clock is 180-degree phase shifted by device clock 101: Sample clock is 225-degree phase shifted by device clock 110: Sample clock is 270-degree phase shifted by device clock 111: Sample clock is 325-degree phase shifted by device clock	RW
16:15	TX_SEL	MSC transmit clock selection: 00: 90-degree 01: 135-degree 10: 180-degree 11: 270-degree	RW
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	MSC1CDR	Divider for MSC1 Frequency. Specified the MSC1 device clock division ratio division ratio = (MSC1CDR + 1)*4.	RW

17.1.2.14 MSC2 device clock divider Register(MSC2CDR,0xA8)

MSC2 device clock divider Register (MSC2CDR) is a 32-bit read/write register that specifies the divider of MSC2 device clock . This register is initialized to 0x40000000 only by any reset. Only word access can be used on MSC2CDR.

	MSC2CDR																BASE+0xA8													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MPCS		CE_MSC2	MSC2_BUSY	MSC2_STOP	Reserved						TUNING_DIS	RX_SEL			TX_SEL	Reserved								MSC2CDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:30	MPCS	00: select SCLK_A clock output 01: select MPLL clock output 10: EXCLK The clock mux is not free of glitches if clock selection is changed The clock mux output is to MSC0, MSC1 MSC2. It is source clock of MSC0, MSC1, MSC2.	RW
29	CE_MSC2	Change enable for MSC2. If CE_MSC2 is 1 , write on MSC2CDR ill start a frequency changing sequence immediately. If CE_MSC2 is 0, writes on MSC2CDR have no affect	RW
28	MSC2_BUSY	The bit is read only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until MSC2_BUSY == 0, may begin another frequency change.	R
27	MSC2_STOP	When MSC2_STOP is 1 and CE_MSC2 is 1, the MSC2 clock will stop. When MSC2_STOP is 0 and CE_MSC2 is 1, the MSC2 clock will continue. Software should wait until MSC2_BUSY == 0, may begin another frequency change.MSC2_STOP is prior to MSC2CDR. If system don't use this module, may set this bit to reduce power .	RW
26:21	Reserved	Writing has no effect, read as zero.	R
20	TUNING_DIS	Tuning disable, software adjust rx phase	RW
19:17	RXCLK_SEL	MSC sample clock selection: 000: Sample clock is 0-degree phase shifted by device clock 001: Sample clock is 45-degree phase shifted by device clock 010: Sample clock is 90-degree phase shifted by device clock 011: Sample clock is 135-degree phase shifted by device clock 100: Sample clock is 180-degree phase shifted by device clock 101: Sample clock is 225-degree phase shifted by device clock 110: Sample clock is 270-degree phase shifted by device clock 111: Sample clock is 325-degree phase shifted by device clock	RW
16:15	TX_SEL	MSC transmit clock selection: 00: 90-degree 01: 135-degree 10: 180-degree 11: 270-degree	RW
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	MSC2CDR	Divider for MSC2 Frequency. Specified the MSC2 device clock division ratio division ratio = (MSC2CDR + 1)*4.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

17.1.2.15 SFC device clock divider Register(SFCCDR,0x74)

SFC device clock divider Register (SFCCDR) is a 32-bit read/write register that specifies the divider of SFC device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on SFCCDR.the clk relation ship of SFC as follows:

	SFCCDR																BASE+0x74													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SFCS		CE_SFC	SFC_BUSY	SFC_STOP	Reserved																			SFCCDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	SFCS	00: select SCLK_A output 01: select MPLL output 10: EPLL It is direct to SFC module It is no glitch free mux. Software should be stop the module clock, when change this bit	RW
29	CE_SFC	Change enable for SFC. If CE_SFC is 1 , write on SFCCDR will start a frequency changing sequence immediately. If CE_SFC is 0, writes on SFCCDR have no affect	RW
28	SFC_BUSY	this bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until SFC_BUSY == 0, may begin another frequency change.	R
27	SFC_STOP	When SFC_STOP is 1 and CE_SFC is 1, the SFC clock will stop. When SFC_STOP is 0 and CE_SFC is 1, the SFC clock will continue. Software should wait until SFC_BUSY == 0, may begin another frequency change. SFC_STOP is prior to SFCCDR. If system don't use this module, may set this bit to reduce power .	RW
26:8	Reserved	Writing has no effect, read as zero.	R
7:0	SFCCDR	Divider for SFC Frequency. Specified the SFC device clock division ratio, which varies from 1 to 256 (division ratio = SFCCDR + 1).	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

17.1.2.16 SSI device clock divider Register(SSICDR,0x5C)

SSI device clock divider Register (SSICDR) is a 32-bit read/write register that specifies the divider of SSI device clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on SSICDR.the clk relation ship of SSI is as follows:

	SSICDR																BASE+0x5C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SPCS		CE_SSI	SSI_BUSY	SSI_STOP	Reserved																			SSICDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	SPCS	00: select SCLK_A output 01: select MPLL output 10: EPLL It is direct to SSI module It is no glitch free mux. Software should be stop the module clock, when change this bit	RW
29	CE_SSI	Change enable for SSI. If CE_SSI is 1 , write on SSICDR will start a frequency changing sequence immediately. If CE_SSI is 0, writes on SSICDR have no affect	RW
28	SSI_BUSY	this bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until SSI_BUSY == 0, may begin another frequency change.	R
27	SSI_STOP	When SSI_STOP is 1 and CE_SSI is 1, the SSI clock will stop. When SSI_STOP is 0 and CE_SSI is 1, the SSI clock will continue. Software should wait until SSI_BUSY == 0, may begin another frequency change. SSI_STOP is prior to SSICDR. If system don’t use this module, may set this bit to reduce power .	RW
26:8	Reserved	Writing has no effect, read as zero.	R
7:0	SSICDR	Divider for SSI Frequency. Specified the SSI device clock division ratio, which varies from 1 to 256 (division ratio = SSICDR + 1).	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

17.1.2.17 CIM MCLK clock divider Register(CIMCDR,0x78)

CIM mclk clock divider Register (CIMCDR) is a 32-bit read/write register that specifies the divider of CIM mclk clock (CIM_MCLK). This register is initialized to 0x00000000 only by any reset. Only word access can be used on CIMCDR.

	CIMCDR																													BASE+0x78
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CIMPCS		CE_CIM	CIM_BUSY	CIM_STOP	Reserved																			CIMCDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Description	RW
31:30	CIMPCS	00: select SCLK_A clock output 01: select MPLL clock output 10: EPLL It is no glitch free mux. Software should be stop the module clock, when change this bit	RW
29	CE_CIM	Change enable for CIM. If CE_CIM is 1 , write on CIMCDR ill start a frequency changing sequence immediately. If CE_CIM is 0, writes on CIMCDR have no affect	RW
28	CIM_BUSY	The bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until CIM_BUSY == 0, may begin another frequency change.	R
27	CIM_STOP	When CIM_STOP is 1 and CE_CIM is 1, the CIM clock will stop. When CIM_STOP is 0 and CE_CIM is 1, the CIM clock will continue. Software should wait until CIM_BUSY == 0, may begin another frequency change. CIM_STOP is prior to CIMCDR. If system don’t use this module, may set this bit to reduce power.	RW
26:8	Reserved	Writing has no effect, read as zero.	R
7:0	CIMCDR	Divider for CIM MCLK Frequency. Specified the CIM MCLK clock (CIM_MCLK) division ratio, which varies from 1 to 256 (division ratio = CIMCDR + 1). the output clock is "io_setup.cim_mclk_o".	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

17.1.2.18 PWM clock divider Register(PWMCDR,0x6C)

PWM clock divider Register (PWMCDR) is a 32-bit read/write register that specifies the divider of PWM clock. This register is initialized to 0x00000000 only by any reset. Only word access can be used on PWMCDR.

	PWMCDR																BASE+0x6C														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PWMPCS		CE_PWM	PWM_BUSY	PWM_STOP	Reserved																							CIMCDR			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Description	RW
31:30	PWMPCS	00: select SCLK_A clock output 01: select MPLL clock output 10: EPLL It is no glitch free mux. Software should be stop the module clock, when change this bit	RW
29	CE_PWM	Change enable for PWM. If CE_PWM is 1 , write on PWMCDR will start a frequency changing sequence immediately. If CE_PWM is 0, writes on PWMCDR have no affect	RW
28	PWM_BUSY	The bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until PWM_BUSY == 0, may begin another frequency change.	R
27	PWM_STOP	When PWM_STOP is 1 and CE_PWM is 1, the PWM clock will stop. When PWM_STOP is 0 and CE_PWM is 1, the PWM clock will continue. Software should wait until PWM_BUSY == 0, may begin another frequency change. PWM_STOP is prior to PWMCDR. If system don't use this module, may set this bit to reduce power.	RW
26:4	Reserved	Writing has no effect, read as zero.	R
3:0	PWMCDR	Divider for PWM clock Frequency. Specified the clock division ratio, which varies from 1 to 256 (division ratio = PWMCDR + 1).	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

17.1.2.19 ISP clock divider Register(ISPCDR,0x30)

ISP clock divider Register (ISPCDR) is a 32-bit read/write register that specifies the divider of ISP clock . This register is initialized to 0x00000000 only by any reset. Only word access can be used on ISPCDR.

	ISPCDR																															BASE + 0x30
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ISPCS		CE_ISP	ISP_BUSY	ISP_STOP	Reserved																							ISPCDR			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	ISPCS	00: select SCLK_A output 01: select MPLL output 10: select EPLL output It is no glitch free mux. Software should be stop the module clock, when change this bit	RW
29	CE_ISP	Change enable for ISP. If CE_ISP is 1 , write on ISPCDR ill start a frequency changing sequence immediately. If CE_ISP is 0, writes on ISPCDR have no affect	RW
28	ISP_BUSY	The bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until ISP_BUSY == 0, may begin another frequency change.	RW
27	ISP_STOP	When ISP_STOP is 1 and CE_ISP is 1, the ISP clock will stop. When ISP_STOP is 0 and CE_ISP is 1, the ISP clock will continue. Software should wait until ISP_BUSY == 0, may begin another frequency change. ISP_STOP is prior to ISPCDR. If system don't use this module, may set this bit to reduce power .	RW
26:4	Reserved	Writing has no effect, read as zero.	R
3:0	ISPCDR	Divider for ISP Frequency. Specified the ISP clock division ratio, which varies from 1 to 16 (division ratio = ISPCDR + 1).	RW

17.1.2.20 RSA clock divider Register(SRACDR,0x50)

RSA clock divider Register (RSACDR) is a 32-bit read/write register that specifies the divider of SRA clock. This register is initialized to 0x00000000 only by any reset. Only word access can be used on RSACDR.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	RSACDR																														BASE + 0x50
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MACPCS		CE_MAC	MAC_BUSY	MAC_STOP	Reserved																							RSACDR			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	RSACS	RSA Clock Source Selection : 00: RSA clock source is SCLK_A 01: RSA clock source is MPLL 10: RSA clock source is EPLL It is no glitch free mux. Software should be stop RSA clock, when change this bit.	**RW**
29	CE_RSA	Change enable for RSA. If CE_RSA is 1 , write on RSACDR will start a frequency changing sequence immediately. If CE_RSA is 0, writes on RSACDR have no affect	RW
28	RSA_BUSY	The bit is ready only bit. It indicates whether the frequency change has finished. When the bit is 0, it indicates frequency change has finished., otherwise it indicates the frequency change is on going Software should be wait until RSA_BUSY == 0, may begin another frequency change.	RW
27	RSA_STOP	When RSA_STOP is 1 and CE_RSA is 1, the RSA clock will stop. When RSA_STOP is 0 and CE_RSA is 1, the RSA clock will continue. Software should wait until RSA_BUSY == 0, may begin another frequency change. RSA_STOP is prior to RSACDR. If system don't use this module, may set this bit to reduce power.	RW
26:4	Reserved	Writing has no effect, read as zero.	R
3:0	RSACDR	Divider for RSA Frequency. Specified the RSA clock division ratio, which varies from 1 to 16 (division ratio = RSACDR + 1).	RW

17.1.2.21 MAC PHY0 Control Register(MPHY0C,0xE4)

The MAC PHY0 Control Register is a 32-bit read/write register that control GMAC interface.It is initialized to 0x0000000 0by reset.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	MPHY0C																															0xE4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Mode_sel	MAC_SPEED		Reserved									TX_SEL	TX_DELAY							RX_SEL	RX_DELAY							SOFT_RST	PHY_INTF		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Mode_sel	useless now	RW
30:29	MAC_SPEED	It is only read. 0x: 1000M 10: 10M 11: 100M	R
28:20	Reserved		R
19	TX_SEL	0: origin TX_CLK 1: delay TX_CLK	RW
18:12	TX_DELAY	Delay TX_CLK 0: one unit delay … 127: 128 unit delay	RW
11	RX_SEL	0: origin RX_CLK 1: delay RX_CLK	RW
10:4	RX_DELAY	Delay RX_CLK 0: one unit delay … 127: 128 unit delay	RW
3	SOFT_RST	1:reset GMAC0 0:don’t reset GMAC0	RW
2:0	PHY_INTF	000: reserved 001: RGMII 100: RMII	RW

17.1.2.22 MAC PHY1 Control Register(MPHY1C,0xE8)

The MAC PHY1 Control Register is a 32-bit read/write register that control GMAC interface.It is initialized to 0x0000000 0by reset.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	MPHY1C																												0xE8	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Mode_sel	MAC_SPEED		Reserved									TX_SEL	TX_DELAY							RX_SEL	RX_DELAY							SOFT_RST	PHY_INTF		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Mode_sel	useless now	RW
30:29	MAC_SPEED	It is only read. 0x: 1000M 10: 10M 11: 100M	R
28:19	Reserved		R
19	TX_SEL	0: origin TX_CLK 1: delay TX_CLK	RW
18:12	TX_DELAY	Delay TX_CLK 0: one unit delay … 127: 128 unit delay	RW
11	RX_SEL	0: origin RX_CLK 1: delay RX_CLK	RW
10:4	RX_DELAY	Delay RX_CLK 0: one unit delay … 127: 128 unit delay	RW
3	SOFT_RST	1:reset GMAC0 0:don't reset GMAC0	RW
2:0	PHY_INTF	000: reserved 001: RGMII 100: RMII	RW

17.1.2.23 CPM interrupt Register(CPM_INTR,0xB0)

	CPM_INTR																												BASE+0xB0	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														VBUS_INTR	ADEV_INTR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	VBUS_INTR	B device insert interrupt.	R
0	ADEV_INTR	A device insert interrupt.	R

17.1.2.24 CPM interrupt enable Register(CPM_INTRE,0xB4)

	CPM_INTRE																BASE+0xB4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														VBUS_INTRE	ADEV_INTRE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	VBUS_INTRE	B device insert interrupt enable.	RW
0	ADEV_INTRE	A device insert interrupt enable.	RW

17.1.2.25 CPM software interrupt Register(CPM_SFTINT,0xBC)

	CPM_SFTINT																BASE+0xBC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															SOFT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	SOFT	set 1 will send interrupt to each interrupt controller. relate to intc spec.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

~~17.1.2.26 DDR Clk Gate Register(DRCG,0xD0)~~

	DRCG																BASE+0xD0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																							~~DRCG~~								
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: obsolete，keep it just for obsolete code

17.1.2.27 CPM Scratch Pad Protected Register(CPSPPR,0x38)

The Scratch Pad Protected Register is reset to 0x0000a5a5. When CPSPPR value equals to 0x00005a5a, software can write the CPSPR. or else can't.

	CPSPPR																BASE+0x38															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CPSPPR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	CPSPPR	When the value is only = 0x00005a5a, software can write CPSPR.	RW

17.1.2.28 CPM Scratch Pad Register(CPSPR,0x34)

The Scratch Pad Register is a 32-bit read/write register that allows software to preserve some critical data. It is not initialized by power on and WDT reset.

	CPSPR																BASE+0x34															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CPSPR																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

17.1.2.29 USB Parameter Control Register(USBPCR,0x3C)

The USBPCR is a 32-bit read/write register that allows software to control OTG PHY some functions. It is initialized to 0x409919b8.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	USBPCR																														0x3C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	USB_MODE	AVLD_REG	IDPULLUP_MASK		Reserved					POR	Reserved																					
RST	0	1	0	0	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	1	0	1	1	1	0	0	0

Bits	Name	Description	RW
31	USB_MODE	0: work as USB device 1: work as OTG	RW
30	AVLD_REG	This bit is used to set “avalid”(VBUS above A-device session threshold) signal.	RW
29:28	IDPULLUP_MASK	These 2 bits control “idpullup” signal in otg mode. 2’b1x: “idpullup” always active 2’b01: “idpullup” always active when usb suspend 2’b00: use “idpullup” from otg controller	RW
27	INCR_MASK	This bit controls whether the ahb interface enhancement for “incr transfer” takes effect. Set this bit to 0 will active the enhancement.	RW
26:23	Reserved	Writing has no effect, read as zero.	RW
22	POR	This bit controls OTG PHY power on reset. The POR signal must be asserted for a minimum of 10 µs. 1: reset 0: not reset	RW
21:0	Reserved	Writing has no effect, read as zero.	RW

17.1.2.30 USB Reset Detect Timer Register(USBRDT,0x40)

It is initialized to 0x2000096

	USBRDT																														0x40
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Resu_inten	Resu_intclr	Resu_speed		Resume_stat	HB_MASK	VBFIL_LD_EN	IDDIG_EN	IDDIG_REG	USBRDT																						
RST	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0

Bits	Name	Description	RW
31	Resume_inten	Resume interrupt enable from sleep mode	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: enable 0:disable	
30	Resume_intclr	Resume interrupt flag clear 1: clear to 0 0: no effect	RW
29:28	Resume_speed	usb speed before resume 00: high speed 01: full speed 10: low speed	RW
27	Resume_status	Resume status. 1: be Resumed 0: not Resumed	R
26	HB_MASK	Halfword/Byte transfer support mask. 0: enable 1: mask	RW
25	VBFIL_LD_EN	VBUS filter data load enable.	RW
24	IDDIG_EN	This bit indicates using IDDIG_REG to control “iddig” signal.	RW
23	IDDIG_REG	This bit controls “iddig” when IDDIG_REG_EN = 1’b1.	RW
22:0	USBRDT	These bits control USB reset detect time.	RW

17.1.2.31 USB VBUS Jitter Filter Register(USBVBFIL,0x44)

	USBVBFIL																														0x44
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IDDIGFIL																USBVBFIL															
RST	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	IDDIGFIL	These bits controls iddig jitter filter time.	RW
15:0	USBVBFIL	These bits controls VBUS jitter filter time.	RW

17.1.2.32 USB Parameter Control Register1(USBPCR1,0x48)

The USBPCR1 is a 32-bit read/write register that allows software to control OTG and OHCI PHY some functions. It is initialized to 0x8de23360.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	USBPCR1																														0x48
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BVLD_REG	Reserved	dppulldown	dmpulldown	Reserved						PORT0_RST	Reserved																				
RST	1	?	0	0	1	1	0	1	?	?	1	?	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31	BVLD_REG	This bit is used to set "bvalid"(VBUS above B-device session threshold) signal.	R
30	Reserved	Writing has no effect, read as zero.	R
29	Dppulldown	OTG PHY DP pull down 0: OTG PHY DP didn't pull down 1: OTG PHY DP pull down controlled by otg controller	RW
28	Dmpulldown	OTG PHY DM pull down 0: OTG PHY DM didn't pull down 1: OTG PHY DM pull down controlled by otg controller	RW
27:22	Reserved	Writing has no effect, read as zero.	R
21	PORT_RST	OTG PHY Port reset: 1: The transmit and receive finite state machines are reset, and the linestate logic combinatorially reflects the state of the single-ended receivers 0: The transmit and receive finite machines are operational, and the linestate inputs becomes sequential after 11 PHYCLOCK cycles.	RW
20:0	Reserved	Writing has no effect, read as zero.	R

17.1.2.33 PLL Control Register(CPPCR,0x0C)

The PLL Control Register (CPPCR) is a 32-bit read/write register, which controls PLL some controls bits and stabilize time. It is initialized to 0x00000020 only by any reset. Only word access can be used on CPPCR. It is used to control all PLL.

	CPPCR																														BASE+0x0C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	APLL_BP	Reserved	MPLL_BP	Reserved	EPLL_BP	Reserved																		PLLST							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31	**Reserved**		
30	APLL_BP	APLL ByPass Mode: 0 - not bypass 1- bypass mode	RW
29	Reserved		
28	MPLL_BP	MPLL ByPass Mode: 0 - not bypass 1- bypass mode	RW
27	Reserved		
26	EPLL_BP	EPLL ByPass Mode: 0 - not bypass 1- bypass mode	RW
25:8	Reserved		R
7:0	PLLST	PLL Stabilize Time. Specifies the PLL stabilize time by unit of RTCCLK (approximate 32kHz) cycles. It is used when change PLL multiplier or change PLL from off to on. It is initialized to H'20. It is used to control all PLL.	RW

17.1.2.34 APLL Control Register(CPAPCR,0x10)

The APLL Control Register (CPAPCR) is a 32-bit read/write register, which controls PLL multiplier, on/off state and stabilize time. It is initialized to 0x99009020 only by any reset. Only word access can be used on CPAPCR

	CPAPCR																													0x10
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			PLLFD									PLLRD				PLLOD				Reserved				PLLRG			Reserved	PLL_ON	LOCK	Reserved	PLLEN
RST	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0

Bits	Name	Description	RW
28:20	PLLFD	Feedback divider value (binary value + 1.0)	RW
19:14	PLLRD	Th reference divider. value (binary value + 1.0)	RW
13:11	PLLOD	Output divider value 001: 2 100: 16 010: 4 101: 32 011: 8 110: 64	RW
10:8	Reserved		R
7:5	PLLRG	the PLL filter range	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		000: bypass 100: 30-50M 001: 7-11M 101: 50-80M 010: 11-18M 110: 80M-130M 011: 18-30M 111: 130M-200M	
4	Reserved		R
3	PLL_ON	PLL Stabilize Flag. 0: PLL is off or not stable	
2	LOCK	0: the PLL output is not stable 1: the PLL output is stable Software should clear this bit to 0, when this bit equal to 1, it indicates that PLL hadn't stable previously , it is only used to debug.	R
1	Reserved		R
0	PLLEN	PLL Enable. **Note:** to change PLL frequency, set this bit LOW first.	RW

17.1.2.35 MPLL Control Register(CPMPCR,0x14)

The MPLL Control Register (CPMPCR) is a 32-bit read/write register, which controls PLL multiplier, on/off state and stabilize time. It is initialized to 0x99009020 only by any reset. Only word access can be used on CPMPCR.

	CPMPCR																													0x14
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		PLLFD										PLLRD				PLLOD				Reserved				PLLRG			Reserved	PLL_ON	LOCK	Reserved	PLLEN
RST	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0

Bits	Name	Description	RW
28:20	PLLFD	Feedback divider value (binary value + 1.0)	RW
19:14	PLLRD	Th reference divider. value (binary value + 1.0)	RW
13:11	PLLOD	Output divider value 001: 2 100: 16 010: 4 101: 32 011: 8 110: 64	RW
10:8	Reserved		
7:5	PLLRG	the PLL filter range 000: bypass 100: 30-50M 001: 7-11M 101: 50-80M 010: 11-18M 110: 80M-130M	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		011: 18-30M 111: 130M-200M	
4	Reserved		
3	PLL_ON	PLL Stabilize Flag. 0: PLL is off or not stable	
2	LOCK	0: the PLL output is not stable 1: the PLL output is stable Software should clear this bit to 0, when this bit equal to 1, it indicates that PLL hadn't stable previously , it is only used to debug.	R
1	Reserved		R
0	PLLEN	PLL Enable. **Note:** to change PLL frequency, set this bit LOW first.	RW

17.1.2.36 EPLL Control Register(CPEPCR,0x18)

The EPLL Control Register (CPEPCR) is a 32-bit read/write register, which controls PLL multiplier, on/off state and stabilize time. It is initialized to 0x99009020 only by any reset. Only word access can be used on CPEPCR.

	CPEPCR																													0x58
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		PLLFD										PLLRD				PLLOD					Reserved			PLLRG			Reserved	PLL_ON	LOCK	Reserved	PLLEN
RST	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0

Bits	Name	Description	RW
28:20	PLLFD	Feedback divider value (binary value + 1.0)	RW
19:14	PLLRD	Th reference divider. value (binary value + 1.0)	RW
13:11	PLLOD	Output divider value 001: 2 100: 16 010: 4 101: 32 011: 8 110: 64	RW
10:8	Reserved		R
7:5	PLLRG	the PLL filter range 000: bypass 100: 30-50M 001: 7-11M 101: 50-80M 010: 11-18M 110: 80M-130M 011: 18-30M 111: 130M-200M **Note**: the PLL filter is FIN/ (PLLRD+1)	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

4	Reserved		R
3	PLL_ON	PLL Stabilize Flag. 0: PLL is off or not stable	
2	LOCK	0: the PLL output is not stable 1: the PLL output is stable Software should clear this bit to 0, when this bit equal to 1, it indicates that PLL hadn't stable previously , it is only used to debug.	R
1	Reserved		R
0	PLLEN	PLL Enable. **Note:** to change PLL frequency, set this bit LOW first.	RW

17.1.3 PLL Operation

The PLL developed as a macro cell for clock generator. It can generate a stable high-speed clock from a slower clock signal. The output frequency is adjustable from 40Mhz to 2400MHz. The PLL integrates a phase frequency detector (PFD), a low pass filter (LPF), a voltage controlled oscillator (VCO) and other associated support circuitry. All fundamental building blocks as well as fully programmable dividers are integrated on the core. It is useful for clock multiplication of stable crystal oscillator sources and for de-skew clock signals.

The PLL block diagram is shown in following figure:

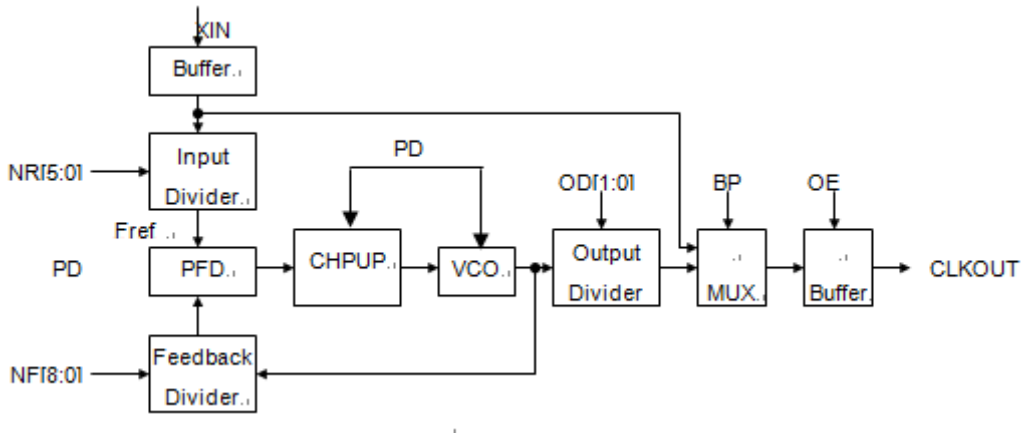


Figure 17-1 Block Diagram of PLL

17.1.3.1 PLL Configuration

PLL Divider Value Setting

There are 3 divider values (N, M and NO) to set the PLL output clock frequency CLKOUT:

1 Input Divider Value N.

N = PLLRD

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

2 Feedback Divider Value M.

M = PLLFD

3 Output Divider Value NO.

Output Divider Setting (OD)	Output Divider Value (NO)
001	2
010	4
011	8
100	16
101	32
110	64

4 The PLL output frequency, FOUT, is determined by the ratio set between the value set in the input divider and the feedback divider. PLL output frequency FOUT is calculated from the following equations:

NF = 1+ M

NR = 1+ N

NO = NO

FREF = FIN / NR

FVCO = FOUT * NO

FOUT = FIN *2* NF / (NR*NO)

For proper operation in normal mode, the following constraints must be satisfied:

5 MHz ≤ FREF ≤ 200 MHz

2400 MHz ≤ FVCO ≤ 4800 MHz

17.1.4 Main Clock Division Change Sequence

Main clock (CCLK, L2CLK, H2CLK, PCLK) frequencies can be changed separately or simultaneously by changing division ratio. Following conditions must be obeyed:

1 the frequency of CCLK must be 1,2,3 or 4 times of the frequency of L2CLK

2 the frequency of H2CLK must be 1 or 2 times of the frequency of PCLK

Don’t violate this limitation, otherwise unpredictable error may occur.

Important Note: When CPU enters sleep mode, the APLLEN must be set to 1.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

17.2 Power Manager

In the Low-Power mode, part or whole processor is halted. This will reduce power consumption. The Power Management Controller contains low-power mode control and reset sequence control.

17.2.1 Low-Power Modes and Function

The processor supports six low-power modes and function:

- NORMAL mode

  In Normal mode, all peripherals and the basic blocks including power management block, the CPU core, the bus controller, the memory controller, the interrupt controller, DMA, and the external master may operate completely. But, the clock to each peripheral, except the basic blocks, can be stopped selectively by software to reduce the power consumption.

- IDLE mode

  In IDLE mode, the clock to the CPU core is stopped except the bus controller, the memory controller, the interrupt controller, and the power management block. To exit the IDLE mode, the any interrupts should be activated.

- SLEEP mode

  In SLEEP mode, all clocks except RTC clock are disabled. PLL is disabled also. SLEEP mode is canceled by reset or interrupt. When SLEEP mode is canceled, PLL is restarted , the PLL needs clock stabilization time (PLL lock time). This PLL stabilization time is automatically inserted by the internal logic with lock time count register. and all clocks start operating after PLL stability time.

- CLOCK GATE function

  CLOCK GATE function is used to gate specified on-chip module when it is not used. Set specified CLKG0~31 bits in CLKGR will enter specified CLK gate function. CLOCK gate function is canceled by reset or clearing specified bits in CLKGR0/1 to 0.

- Power down Mode

  In order to reduce power leakage, software may shut down power supply for no used device. When system enters into SLEEP mode, the software may shut down power for core according to OPCR.PD bit.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

17.2.2 Register Description

All PMC register 32bit access address is physical address.

Table 17-3 Power/Reset Management Controller Registers Configuration

Name	description	RW	Initial Value	Offset Address	Access Size
LCR	Low Power Control Register	RW	0x00000000	0x0004	32
PSWC0ST	Power Switch Chain0 Start Time	RW	0x00000000	0x0090	32
PSWC1ST	Power Switch Chain1 Start Time	RW	0x00000000	0x0094	32
PSWC2ST	Power Switch Chain2 Start Time	RW	0x00000000	0x0098	32
PSWC3ST	Power Switch Chain3 Start Time	RW	0x00000000	0x009c	32
SRBC	Soft Reset and Bus Control Register	RW	0x00000000	0x00C4	32
SLBC	Sleep Boot Control Register	RW	0x00000000	0x00C8	32
SLPC	Sleep PC Register	RW	0x????????	0x00CC	32
CLKGR0	Clock Gate Register0	RW	0x47FFFFE0	0x 0020	32
CLKGR1	Clock Gate Register1	RW	0x37FFFFFF	0x 0028	32
MEMPD0	Sram power down Register0	RW	0x00000000	0x00F8	32
MEMPD1	Sram power down Register1	RW	0x00000000	0x00FC	32
OPCR	Oscillator and Power Control Register	RW	0x10801500	0x 0024	32
MESTSEL	asnyc handshake control register	RW	0x00000000	0x00EC	32

17.2.2.1 Low Power Control Register(LCR,0x04)

The Low Power Control Register (LCR) is a 32-bit read/write register that controls low-power mode status. It is initialized to 0x00000000 by any reset.

	LCR																BASE+0x04													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD_ISP0	PD_ISP1	PD_FELIX	PD_HELIX	PISP0S	PIISP1S	PFELIXS	PHELIXS	Reserved				PST												Reserved			PD_IDLES			LPM	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	PD_ISP0	Power down module isp0 0: not shut down 1: shut down	RW
30	PD_ISP1	Power down module isp1 0: not shut down	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: shut down	
29	PD_FELIX	Power down module FELIX 0: not shut down 1: shut down	RW
28	PD_HELIX	Power down module HELIX 0: not shut down 1: shut down	RW
27	PISP0S	0: isp0 not enter power down mode 1: isp0 enter power down mode	R
26	PISP1S	0: isp1 not enter power down mode 1: isp1 enter power down mode	R
25	PFELIXS	0: FELIX not enter power down mode 1: FELIX enter power down mode	R
24	PHELIXS	0: HELIX not enter power down mode 1: HELIX enter power down mode	R
23:20	Reserved		R
19:8	PST	Power stability Time. Specifies the Power stabilize time by unit of RTCCLK (approximate 32kHz) cycles.	RW
7:5	Reserved		
4	PD_IDLES	0: CPU core not enter power down state 1: CPU core enter power down state	R
3:2	Reserved		
1:0	LPM	Low Power Mode. Specifies which low-power mode will be entered when SLEEP instruction is executed. Bit 1~0: **00**: IDLE mode will be entered when SLEEP instruction is executed **01**: SLEEP mode will be entered when SLEEP instruction is executed **10**: IDEL mode , CPU core will be power gated when SLEEP instruction is executed	RW

17.2.2.2 Power Switch Chain0 Start Time Register(PSWC0ST,0x90)

	PSWC0ST																													0x90
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PSWC0ST															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

17.2.2.3 Power Switch Chain1 Start Time Register(PSWC1ST,0x94)

	PSWC1ST																													0x94
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PSWC1ST															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

17.2.2.4 Power Switch Chain2 Start Time Register(PSWC2ST,0x98)

	PSWC2ST																													0x98
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PSWC2ST															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

17.2.2.5 Power Switch Chain3 Start Time Register(PSWC3ST,0x9C)

	PSWC3ST																													0x1000009C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PSWC3ST															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOTE: The Start Time by the unit of PCLK cycles.

17.2.2.6 Clock Gate Register(CLKGR,0x20)

The Clock Gate Register (CLKGR) is a 32-bit read/write register that controls the CLOCK GATE function of peripherals. It is reset to 0x07FFFF10.

	CLKGR																													BASE+0x20
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLKGR																															
RST	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>RW</th></tr>
<tr><td>31:0</td><td>CLKGR</td><td>Clock gate Bits. Controls the clock supplies to some peripherals. If set, clock supplies to associated devices are stopped, and registers of the device cannot be accessed also.
The reset value of this register reflects the clock gate information of the relative modules.
RST 0: After reset period, the clock is not stopped.
RST 1: After reset period, the clock is stopped.

<table>
<tr><th>Bit</th><th>Module</th><th>Description</th></tr>
<tr><td>31</td><td>DDR</td><td>If set, gate the clock.</td></tr>
<tr><td>29</td><td>AHB0</td><td>If set, gate the clock.</td></tr>
<tr><td>28</td><td>APB0</td><td>If set, gate the clock.</td></tr>
<tr><td>27</td><td>RTC</td><td>If set, gate the clock.</td></tr>
<tr><td>26</td><td>SSI1</td><td>If set, gate the clock.</td></tr>
<tr><td>25</td><td>RSA</td><td>If set, gate the clock.</td></tr>
<tr><td>24</td><td>AES</td><td>If set, gate the clock.</td></tr>
<tr><td>23</td><td>LCD</td><td>If set, gate the clock.</td></tr>
<tr><td>22</td><td>CIM</td><td>If set, gate the clock.</td></tr>
<tr><td>21</td><td>PDMA</td><td>If set, gate the clock.</td></tr>
<tr><td>20</td><td>OST</td><td>If set, gate the clock.</td></tr>
<tr><td>19</td><td>SSI0</td><td>If set, gate the clock.</td></tr>
<tr><td>18</td><td>TCU</td><td>If set, gate the clock.</td></tr>
<tr><td>17</td><td>DTRNG</td><td>If set, gate the clock.</td></tr>
<tr><td>16</td><td>UART2</td><td>If set, gate the clock.</td></tr>
<tr><td>15</td><td>UART1</td><td>If set, gate the clock.</td></tr>
<tr><td>14</td><td>UART0</td><td>If set, gate the clock.</td></tr>
<tr><td>13</td><td>SADC</td><td>If set, gate the clock.</td></tr>
<tr><td>12</td><td>HELIX</td><td>If set, gate the clock.</td></tr>
<tr><td>11</td><td>AUDIO</td><td>If set, gate the clock.</td></tr>
<tr><td>10</td><td>I2C3</td><td>If set, gate the clock.</td></tr>
<tr><td>9</td><td>I2C2</td><td>If set, gate the clock.</td></tr>
<tr><td>8</td><td>I2C1</td><td>If set, gate the clock.</td></tr>
<tr><td>7</td><td>I2C0</td><td>If set, gate the clock.</td></tr>
<tr><td>6</td><td>SCC</td><td>If set, gate the clock.</td></tr>
<tr><td>5</td><td>MSC1</td><td>If set, gate the clock.</td></tr>
<tr><td>4</td><td>MSC0</td><td>If set, gate the clock.</td></tr>
<tr><td>3</td><td>OTG</td><td>If set, gate the clock.</td></tr>
<tr><td>2</td><td>SFC</td><td>If set, gate the clock.</td></tr>
<tr><td>1</td><td>EFUSE</td><td>If set, gate the clock.</td></tr>
<tr><td>0</td><td>NEMC</td><td>If set, gate the clock.</td></tr>
</table>
</td><td>RW</td></tr>
</table>

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Note`: you can use XXCDR.XX_STOP, CLKGR.XX or SRBC.XX_STP to stop XX module's clk, and when CLKGR.XX or SRBC.XX_STP is set high , CPU can turn into sleep mode successfully, but if only set XXCDR.XX_STOP high, CPU may not turn into sleep mode, because XX module can not give out stop_ack when clk is stopped; CPM will not wait for XX module's stop_ack if you stop it's clk by set CLKGR.XX.

Note2: Scc's clk is 1/8 of exclk.

17.2.2.7 Clock Gate Register1(CLKGR1,0x28)

	CLKGR1																BASE+0x28													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CLKGR1															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31	Reserved		R
30	ARB		
29	MIPI_DSI	If set, gate the clock.	RW
28	MIPI_CSI	If set, gate the clock.	RW
27	Reserved		R
26	INTC	If set, gate the clock.	RW
25	MSC2	If set, gate the clock.	RW
24	GMAC1	If set, gate the clock.	RW
23	GMAC0	If set, gate the clock.	RW
22	UART9	If set, gate the clock.	RW
21	UART8	If set, gate the clock.	RW
20	UART7	If set, gate the clock.	RW
19	UART6	If set, gate the clock.	RW
18	UART5	If set, gate the clock.	RW
17	UART4	If set, gate the clock.	RW
16	UART3	If set, gate the clock.	RW
15	Reseved	If set, gate the clock.	RW
14	SPDIF	If set, gate the clock.	RW
13	DMIC	If set, gate the clock.	RW
12	PCM	If set, gate the clock.	RW
11	I2S3	If set, gate the clock.	RW
10	I2S2	If set, gate the clock.	RW
9	I2S1	If set, gate the clock.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

8	I2S0	If set, gate the clock.	RW
7	ROT	If set, gate the clock.	RW
6	HASH	If set, gate the clock.	RW
5	PWM	If set, gate the clock.	RW
4	FELIX	If set, gate the clock.	RW
3	ISP1	If set, gate the clock.	RW
2	ISP0	If set, gate the clock.	RW
1	I2C5	If set, gate the clock.	RW
0	I2C4	If set, gate the clock.	RW

17.2.2.8 Mest Sel Register(MESTSEL,0xEC)

	MESTSEL																BASE+0xEC													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																							TST8	TST7	Reserved		TST4	TST3	Reserved	TST1	TST0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Mux-priority	Dpu-mux-priority isp-mux-priority 31:30 helix 29:28 felix 27:26 tiziano 25:24 tiziano1 23”22 lcd 21:20 cim 19:18 rotate 17:16 null 15:12 null	R
11:9	Reserved	Write has no effect, read as 0	R
8	TST8	AHB0 and APB0	RW
7	TST7	AHB2 and DDR	RW
6:5	Reserved	WR , but useless	RW
4	TST4	AHB0 and DDR	RW
3	TST3	CPU and DDR	RW
2	Reserved	WR , but useless	RW
1	TST1	CPU and AHB0	RW
0	TST0	CPU and AHB2	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

17.2.2.9 Soft Reset and Bus Control Register (SRBC,0xC4)

The Soft Reset and Bus Control Register is a 32-bit read/write register that control some module reset and bus transmission. It is initialized to 0x0000000 0by reset.Remember GMAC's soft reset is in MPHYC.SOFT_RST.

	SRBC																						BASE+0xC4									
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HELIX_SR	HELIX_STP	HELIX_ACK	FELIX_SR	FELIX_STP	FELIX_ACK	ISP0_SR	ISP0_STP	ISP0_ACK	ISP1_SR	ISP1_STP	ISP1_ACK	LCD_SR	CIM_SR	ROT_SR			CPU_ACK	Reserved	OTG_SR	HASH_SR	AES_SR	RSA_SR	Reserved									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	HELIX_SR	0: HELIX does not enter soft reset mode 1: HELIX enters soft reset mode	RW
30	HELIX_STP	Request for HELIX to Stop bus transfer.	RW
29	HELIX_ACK	HELIX Stop Ack.	R
28	FELIX_SR	0: FELIX does not enter soft reset mode 1: FELIX enters soft reset mode	RW
27	FELIX_STP	Request for FELIX to Stop bus transfer.	RW
26	FELIX_ACK	FELIX Stop Ack.	R
25	ISP0_SR	0: ISP0 does not enter soft reset mode 1: ISP0 enters soft reset mode	RW
24	ISP0_STP	Request for ISP0 to Stop bus transfer.	RW
23	ISP0_ACK	ISP0 Stop Ack.	R
22	ISP1_SR	0: ISP1 does not enter soft reset mode 1: ISP1 enters soft reset mode	RW
21	ISP1_STP	Request for ISP1 to Stop bus transfer.	RW
20	ISP1_ACK	ISP1 Stop Ack.	R
19	LCD_SR	LCD soft reset	RW
18	CIM_SR	CIM soft reset	RW
17	ROT_SR	Rot soft reset	
16:15	Reserved	Write has no effect, Read as 0	
14	CPU_ACK	CPU Stop Ack.	R
13	Reserved	Write has no effect, Read as 0	R
12	OTG_SR	OTG soft reset	RW
11	HASH_SR	HASH soft reset	RW
10	AES_SR	AES soft reset	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

9	RSA_SR	RSA soft reset	
8:0	Reserved	Write has no effect, Read as 0	R

17.2.2.10 Exclk Drive Strength Register (EXCLK_DS,0xE0)

The Register is a 32-bit read/write register that control EXCLK drive strength. It is initialized to 0x00000002 by reset.

	EXCLK_DS																												0xE0	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	POC		Reserved						Mac_msc _arbiter																Reserved						DS	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	RW
31:30	POC	0: 3.0v 1: 1.8v 31 bit is mainly controlled SD voltage 30 bit is mainly controlled DVP voltage	RW
23:8	Mac_msc_ arbiter		RW
1:0	DS	Software doesn't change	RW

17.2.2.11 Memory Power Down Control Register0(MEMORY_PD0,0xF8)

The Memory Power Down Control Register 0 is a 32-bit read/write register

	MEMORY_PD0																												BASE + 0xF8	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MPDCR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved		RW
28	NEMC		RW
27	USB		RW
26	SFC		RW
25	PDMA_SE C		RW
24	PDMA		RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

23	MSC2		RW
22	MSC1		RW
21	MSC0		RW
20	GMAC1		RW
19	GMAC0		RW
18	DMIC		RW
17	AUDIO		RW
16	AES		RW
15:13	Reserved		RW
12	DSI		RW
11	SSI1		RW
10	SSI0		RW
9	UART9		RW
8	UART8		RW
7	UART7		RW
6	UART6		RW
5	UART5		RW
4	UART4		RW
3	UART3		RW
2	UART2		RW
1	UART1		RW
0	UART0		RW

Noter: whe shut down these module SRAM, the module clock mustn't be gated.

17.2.2.12 Memory Power Down Control Register1 (MEMORY_PD1,0xFC)

The Memory Power Down Control Register 1 is a 32-bit read/write register

	MEMORY_PD1																BASE + 0xFC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MPDCR1																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:10	Reserved		RW
8	ROT		RW
7	CIM		RW
6	DPU		RW
5	DDR_CH6		RW
4	DDR_CH5		RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

3	DDR_CH3		RW
2	DDR_CH1		RW
1	DDR_CH0		RW
0	DDR_TOP		RW

17.2.2.13 Sleep Boot Control Register (SLBC,0xC8)

The Sleep Boot Control Register is a 32-bit read/write register that control sleep boot mode.It is initialized to 0x0000000 0by reset.

	SLBC																													0xC8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														SLBC	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved		R
0	SLBC	0: Sleep Mode Wake up Boot Process is same with any reset. 1: Sleep Mode Wake up Boot Process is jumped to SLPC, don't care Boot_Sel. The bit is only valid When shut down P0 in Sleep Mode	RW

17.2.2.14 Sleep PC Register (SLPC,0xCC)

The Sleep PC Register is a 32-bit read/write register that control sleep mode jump address.

	SLPC																													0xCC
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SLPC																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	SLPC	When SLBC is 1, sleep boot is jumped to SLPC, not true boot as any reset. The register is only valid When shut down P0 in Sleep Mode and SLBC is set high.	RW

17.2.2.15 Oscillator and Power Control Register (OPCR,0x24)

The Oscillator and Power Control Register is a 32-bit read/write register that specifies some special

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

controls to oscillator and analog block. It is initialized to 0x00801500 by reset.

	OPCR																BASE+0x24													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IDLE_DIS	Mask_int	Reserved	Gate_sclka_bus	Reserved	L2C_PD	Reserved	REQ_MODE	Gate_usbphyclk				O1ST												SPENDN0	Reserved		O1SE	PD	ERCS	BUS_MODE	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	IDLE_DIS	0: when CPU enters idle mode, CPU clock is stopped 1: When CPU enters idle mode, CPU clock is not stopped	RW
30	MASK_INT	0: interrupt not mask 1: interrupt masked When enters sleep/idle mode, cpu should set MASK_INT 1, hardware will clear.	RW
29	Reserved		R
28	GATE_SCLKA_BUS	Gate SCLK_A for AHB0 AHB2 DDR	RW
27	Reserved	Write has no effect, read as 0	RW
26	L2C_PD	L2CC power down select 0: L2C RAM power down mode 1: L2c RAM rentention mode	RW
25	Reserved		
24	REQ_MODE	0: Before go into sleep mode, CPM send stop req signal to relatvie modules in SRBC 1: Before go into sleep mode, CPM doesn't send stop req signal to those modules When DDR enters retention mode, software should be set the bit to 1	RW
23	gate_usbphy_clk	1:gate usb phy clk12m 0:not gate usb phy clk12m	RW
22	Nemc_rom_clr_ds_en	0: after sleep mode return, hardware don't clear rom DS bit 1: after sleep mode return, hardware clear rom DS bit	RW
21	Cpu_sram_ds_en	0: when enters sleep mode, the 32k sram doesn't enter retention mode 1: when enters sleep mode, the 32k sram enters retention mode	RW
20	Ddr_clr_sd_en	0: after sleep mode return, hardware don't clear ddr ram SD bit 1: after sleep mode return, hardware clear DDR ram SD bit	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

19:8	O1ST	EXCLK Oscillator Stabilize Time. This filed specifies the EXCLK oscillator stabilize time by unit of 16 RTCCLK periods (oscillator stable time O1ST × 16 / 32768) cycles. It is initialized to H'15.	RW
7	SPENDN0	force USB PHY to enter suspend mode when OTG is enable. 0: USB PHY has forced to entered SUSPEND mode 1: USB PHY hasn't forced to entered SUSPEND mode	RW
6	Reserved	Write has no effect, Read as 0	R
5	CIM_MCLK_gate	0: don't gate CIM_MCLK_o 1: gate CIM_MCLK_o	RW
4	O1SE	EXCLK Oscillator Sleep Mode Enable. This filed controls the state of the EXCLK oscillator in Sleep mode. 0: EXCLK oscillator is disabled in Sleep mode 1: EXCLK oscillator is enabled in Sleep mode	RW
3	PD	0: no power down cpu_core in sleep mode 1: power down cpu_core in sleep mode	RW
2	ERCS	EXCLK/512 clock and RTCLK clock selection. 0: select EXCLK/512 division ration clock 1: select RTCLK clock the clock only output to CPM INTC SSI TCU etc.	RW
1	BUS_MODE	The default value is 0 When the value is 1, the BUS access is accelerated.	RW
0	reserved	Write has no effect, Read as 0	R

Note: Before you want to power down cpu buy set PD in OPCR, you need to reduce cpu's frequency as the same as L2C's freq; or else unpredictable error will accurs when CPU
is waken up again.

17.2.3 IDLE Mode

In normal mode, when LPM bits in LCR are 0 and SLEEP instruction is executed, the processor enters idle mode. CPU is halted but its register contents are retained All critical application must be finished and peripherals must be configured to generate interrupts when they need CPU attention.

The procedure of entering sleep mode is shown blow:

1 Set LPM bits in LCR to 0.
2 Executes SLEEP instruction.
3 When current operation of CPU core has finished and CPU core is idle, CCLK supply to CPU core is stopped.

IDLE mode is exited by an interrupt (IRQ or on-chip devices) or a reset.

17.2.4 SLEEP Mode

In normal mode, when LPM bits in LCR is 1 and SLEEP instruction is executed, the processor enter

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

SLEEP mode. CPU and on-chip devices are halted, except some wakeup-logic. PLL is shut off. Clock output from CKO pin is also stopped. SDRAM content is preserved by driving into self-refresh state. CPU registers and on-chip devices registers contents are retained.

Before enter SLEEP mode, software should ensure that all peripherals are not running. The procedure of entering SLEEP mode is shown blow:

1 Set LPM bit in LCR to 1.
2 Execute a SLEEP instruction.
3 When current access on system bus complete, the arbiter will not grant any following request. EMC will drive SDRAM from auto-refresh mode to self-refresh mode.
4 When system bus is idle state and SDRAM is self-refresh mode, internal clock supplies are stopped.
5 SLEEP mode can be exited by an interrupt (IRQ or on-chip devices), WDT reset or a poweron reset via the RESETP pin.

17.3 Reset Control Module

17.3.1 Register Description

All RCM register 32bit access address is physical address.

Name	description	RW	Initial Value	Address	Access Size
RSR	Reset Status Register	RW	0x????????	0x0008	32

17.3.1.1 Reset Status Register (RSR)

The Reset Status Register (RSR) is a 32-bit read/write register which records last cause of reset. Each RSR bit is set by a different source of reset. Please refer to Reset Sequence Control for reset sources description.

	RSR																BASE+0x0008															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											FASTBOOT	HR	P0R	WR	PR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect, read as zero.	R
4	FASTBOOT		R
3	HR	Hibernate Reset.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Software can only write 0,Write 1 will be ignored	
2	P0R	P0 power up Reset. It indicates that P0 has been shut down, now it has been power up. When P0 reset is detected, P0R is set and remains set until software clears it or another reset occurs. This bit can only be written with 0. Write with 1 will be ignored. 0: P0 reset has not occurred since the last time the software clears this bit 1: P0 reset has occurred since the last time the software clears this bit	
1	WR	WDT Reset. When a WDT reset is detected, WR is set and remains set until software clears it or another reset occurs. This bit can only be written with 0. Write with 1 will be ignored. 0: WDT reset has not occurred since the last time the software clears this bit 1: WDT reset has occurred since the last time the software clears this bit	RW
0	PR	Power On Reset. When a power-on reset via PRESET pin is detected, PR is set and remains set until software clears it or another reset occurs. This bit can only be written with 0. Write with 1 is ignored. 0: Power on reset has not occurred since the last time the software clears this bit 1: Power on reset has occurred since the last time the software clears this bit	RW

17.3.2 Power On Reset

Power on reset is generated when PRESET pin is driven to low. Internal reset is asserted immediately. All pins return to their reset states. The Power on reset is extended to 40MS.

PRESET pin must be held low until power stabilizes and the EXCLK oscillator stabilize. CPU and peripherals are clocked by EXCLK oscillator output directly. PLL is reset to off state. All internal modules are initialized to their predefined reset states.

17.3.3 WDT Reset

WDT reset is generated when WDT overflow. Internal reset is asserted within two RTCCLK cycles. All pins return to their reset states.

Then WDT reset source is cleared because of internal reset. The internal reset is asserted for about 10 milliseconds. CPU and peripherals are clocked by EXCLK oscillator output directly. PLL is reset to off state.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

18 Timer/Counter Unit

18.1 Overview

The TCU include two Genera Purpose Timer; four Periodical Interrupt Timer; four Quad Timer.

18.2 Features

- TCU1: include 0,1,2,3,4,5,6,7 channel, they can:
  - general mode: counter counts when clock posedge or negedge or double.
  - gate mode: counter counts when gate is 0.
  - quadrature mode: counter counts because of the quadrature input.
  - direction mode: counter add or sub because of input signal.
  - pos mode: counter start counts from 0 because of a posedge or a negedge.
  - capture mode: counter counts a period and output high level time and period time.
  - it can support 1/4/16/64/256/1024 prescale for inner clock.
  - it can support only exclk and input_clk.
  - it can't work on sleep mode.
  - it can't support exclk 1 prescale.
- TCU1 use tcu_int[0]

18.3 Pin Description

Table 18-1 PWM Pins Description

Name	I/O	Description
Gpio_input[15:0]	Input	Use to control counter.

18.4 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute

R - Read only
W - Write only
RW - read and write
RCW - read and write, but clear to 0 by read
RSW - read and write, but set to 1 by read
RWC - read and write, clear to 0 by write 1, write 0 has no effect
RWS - read and write, set to 1 by write 1, write 0 has no effect
RC - read only, and clear to 0 by read

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

RS - read only, and set to 1 by read

SPEC - special access method, relate to its description

3. Reset Value

1 - reset to 1

0 - reset to 0

? - value unknown after reset

18.4.1 Register Memory Map

Table 18-2 Registers Memory Map Base Address

Name	Base	Description
TCU	0x10002000	Address Base of TCU

The Timer/Counter Unit is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 18-3 TCU Registers Map

Name	RW	Reset Value	Address offset	Access Size
TCU_ENABLE_RD	R	0x0000_0000	0x010	16
TCU_ENABLE_SET	W	0x0000_?0??	0x014	16
TCU_ENABLE_CLR	W	0x0000_?0??	0x018	16
TCU_STOP_RD	R	0x0000_0000	0x01C	32
TCU_FLAG_RD	R	0x0000_0000	0x020	32
TCU_FLAG_SET	W	0x00??_?0??	0x024	32
TCU_FLAG_CLR	W	0x00??_?0??	0x028	32
TCU_STOP_SET	W	0x000?_?0??	0x02C	32
TCU_MASK_RD	R	0x01FF_80FF	0x030	32
TCU_MASK_SET	W	0x00??_?0??	0x034	32
TCU_MASK_CLR	W	0x00??_?0??	0x038	32
TCU_STOP_CLR	W	0x000?_?0??	0x03C	32
TCTU_FULL0	RW	0x0000_????	0x040	16
TCU_HALF0	RW	0x0000_????	0x044	16
TCU_COUNT0	RW	0x0000_????	0x048	16
TCU_CONTROL0	RW	0x0000_0000	0x04C	16
TCTU_FULL1	RW	0x0000_????	0x050	16
TCU_HALF1	RW	0x0000_????	0x054	16
TCU_COUNT1	RW	0x0000_????	0x058	16
TCU_CONTROL1	RW	0x0000_0000	0x05C	16
TCTU_FULL2	RW	0x0000_????	0x060	16
TCU_HALF2	RW	0x0000_????	0x064	16
TCU_COUNT2	RW	0x0000_????	0x068	16

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

TCU_CONTROL2	RW	0x0000_0000	0x06C	16
TCTU_FULL3	RW	0x0000_????	0x070	16
TCU_HALF3	RW	0x0000_????	0x074	16
TCU_COUNT3	RW	0x0000_????	0x078	16
TCU_CONTROL3	RW	0x0000_0000	0x07C	16
TCTU_FULL4	RW	0x0000_????	0x080	16
TCU_HALF4	RW	0x0000_????	0x084	16
TCU_COUNT4	RW	0x0000_????	0x088	16
TCU_CONTROL4	RW	0x0000_0000	0x08C	16
TCTU_FULL5	RW	0x0000_????	0x090	16
TCU_HALF5	RW	0x0000_????	0x094	16
TCU_COUNT5	RW	0x0000_????	0x098	16
TCU_CONTROL5	RW	0x0000_0000	0x09C	16
TCTU_FULL6	RW	0x0000_????	0x0A0	16
TCU_HALF6	RW	0x0000_????	0x0A4	16
TCU_COUNT6	RW	0x0000_????	0x0A8	16
TCU_CONTROL6	RW	0x0000_0000	0x0AC	16
TCTU_FULL7	RW	0x0000_????	0x0B0	16
TCU_HALF7	RW	0x0000_????	0x0B4	16
TCU_COUNT7	RW	0x0000_????	0x0B8	16
TCU_CONTROL7	RW	0x0000_0000	0x0BC	16
TCU_CAPTURE0	RW	0x0000_0000	0x0C0	16
TCU_CAPTURE1	RW	0x0000_0000	0x0C4	16
TCU_CAPTURE2	RW	0x0000_0000	0x0C8	16
TCU_CAPTURE 3	RW	0x0000_0000	0x0CC	16
TCU_CAPTURE 4	RW	0x0000_0000	0x0D0	16
TCU_CAPTURE 5	RW	0x0000_0000	0x0D4	16
TCU_CAPTURE 6	RW	0x0000_0000	0x0D8	16
TCU_CAPTURE 7	RW	0x0000_0000	0x0DC	16
TCU_CAP_VALUE0	RW	0x????_????	0x0E0	32
TCU_CAP_VALUE1	RW	0x????_????	0x0E4	32
TCU_CAP_VALUE2	RW	0x????_????	0x0E8	32
TCU_CAP_VALUE3	RW	0x????_????	0x0EC	32
TCU_CAP_VALUE4	RW	0x????_????	0x0F0	32
TCU_CAP_VALUE5	RW	0x????_????	0x0F4	32
TCU_CAP_VALUE6	RW	0x????_????	0x0F8	32
TCU_CAP_VALUE7	RW	0x????_????	0x0FC	32
TCU_FIL_VALUE0	RW	0x0000_0000	0x1A0	32
TCU_FIL_VALUE1	RW	0x0000_0000	0x1A4	32
TCU_FIL_VALUE2	RW	0x0000_0000	0x1A8	32
TCU_FIL_VALUE3	RW	0x0000_0000	0x1AC	32

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

TCU_FIL_VALUE4	RW	0x0000_0000	0x1B0	32
TCU_FIL_VALUE5	RW	0x0000_0000	0x1B4	32
TCU_FIL_VALUE6	RW	0x0000_0000	0x1B8	32
TCU_FIL_VALUE7	RW	0x0000_0000	0x1BC	32

18.4.2 Register and Fields Description

18.4.2.1 Timer Counter Enable Register (TCU_ENABLE_RD,0x010)

The TCER is a 16-bit read-only register. It contains the counter enable control bits for each channel. It is initialized to 0x0000 by any reset. It can only be set by register TCSTR and TCCLR. Since the timer enable control bits are located in the same addresses, two or more timers can be started at the same time.

THIS ENABLE IS ONLY USE IN COUNTER_MODE

	TCU_ENABLE_RD																Base + 0x010													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSTEN	Reserved							TCEN7	TCEN6	TCEN5	TCEN4	TCEN 3	TCEN 2	TCEN 1	TCEN 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	OSTEN	Enable the counter in OST. 0: Stop counting up 1: Begin counting up	R
14:9	Reserved	Writing has no effect, read as zero.	R
7	TCEN 7	Enable the counter in timer 7. 0: Stop counting up 1: Begin counting up	R
6	TCEN 6	Enable the counter in timer 6. 0: Stop counting up 1: Begin counting up	R
5	TCEN 5	Enable the counter in timer 5. 0: Stop counting up 1: Begin counting up	R
4	TCEN 4	Enable the counter in timer 4. 0: Stop counting up 1: Begin counting up	R
3	TCEN 3	Enable the counter in timer 3.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: Stop counting up 1: Begin counting up	
2	TCEN 2	Enable the counter in timer 2. 0: Stop counting up 1: Begin counting up	R
1	TCEN 1	Enable the counter in timer 1. 1: Begin counting up 0: Stop counting up	R
0	TCEN 0	Enable the counter in timer 0. 0: Stop counting up 1: Begin counting up	R

18.4.2.2 Timer Counter Enable Set Register (TCU_ENABLE_SET,0x014)

The TCSTR is a 32-bit write-only register. It contains the counter enable set bits for each channel. Since the timer enable control set bits are located in the same addresses, two or more timers can be started at the same time.

	TCU_ENABLE_SET																Base + 0x014													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSTST	Reserved							TCST 7	TCST 6	TCST 5	TCST 4	TCST 3	TCST 2	TCST 1	TCST 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
15	OSTST	Set OSTEN bit of TER. 0: Ignore 1: Set OSTEN bit to 1	W
14:8	Reserved	Writing has no effect, read as zero.	RW
7	TCST 7	Set TCEN 7 bit of TER. 0: Ignore 1: Set TCEN 7 bit to 1	W
6	TCST 6	Set TCEN 6 bit of TER 0: Ignore. 1: Set TCEN 6 bit to 1	W
5	TCST 5	Set TCEN 5 bit of TER. 0: Ignore 1: Set TCEN 5 bit to 1	W
4	TCST 4	Set TCEN 4 bit of TER. 0: Ignore	W

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: Set TCEN 4 bit to 1	
3	TCST 3	Set TCEN 3 bit of TER. 0: Ignore 1: Set TCEN 3 bit to 1	W
2	TCST 2	Set TCEN 2 bit of TER. 0: Ignore 1: Set TCEN 2 bit to 1	W
1	TCST 1	Set TCEN 1 bit of TER. 0: Ignore 1: Set TCEN 1 bit to 1	W
0	TCST 0	Set TCEN 0 bit of TER. 0: Ignore 1: Set TCEN 0 bit to 1	W

18.4.2.3 Timer Counter Enable Clear Register (TCU_ENABLE_CLR,0x018)

The TCER is a 32-bit write-only register. It contains the counter enable clear bits for each channel. Since the timer enable clear bits are located in the same addresses, two or more timers can be stop at the same time.

	TCU_ENABLE_CLR																Base + 0x018													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																OSTCL	Reserved							TCCL 7	TCCL 6	TCCL 5	TCCL 4	TCCL 3	TCCL 2	TCCL 1	TCCL 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
15	OSTCL	Set OSTEN bit of TER. 0: Ignore 1: Set OSTEN 5 bit to 0	W
14:8	Reserved	Writing has no effect. Read as zero.	RW
7	TCCL 7	Set TCEN 7 bit of TER. 0: Ignore 1: Set TCEN 7 bit to 0	W
6	TCCL 6	Set TCEN 6 bit of TER. 0: Ignore 1: Set TCEN 6 bit to 0	W
5	TCCL 5	Set TCEN 5 bit of TER. 0: Ignore	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: Set TCEN 5 bit to 0	
4	TCCL 4	Set TCEN 4 bit of TER. 0: Ignore 1: Set TCEN 4 bit to 0	W
3	TCCL 3	Set TCEN 3 bit of TER. 0: Ignore 1: Set TCEN 3 bit to 0	W
2	TCCL 2	Set TCEN 2 bit of TER. 0: Ignore 1: Set TCEN 2 bit to 0	W
1	TCCL 1	Set TCEN 1 bit of TER. 0: Ignore 1: Set TCEN 1 bit to 0	W
0	TCCL 0	Set TCEN 0 bit of TER. 0: Ignore 1: Set TCEN 0 bit to 0	W

18.4.2.4 Timer Stop Register (TCU_STOP_RD,0x01C)

The TSR is a 32-bit read-only register. It contains the timer stop control bits for each channel, WDT and OST. It is initialized to 0x00000000 by any reset. It can only be set by register TSSTR and TSCLR. If set, clock supplies to timer n / WDT / OST is stopped, and registers of the timer / WDT / OST cannot be accessed also.

	TCU_STOP_RD																Base + 0x01C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															WDTS	OSTS	Reserved							STOP7	STOP6	STOP5	STOP4	STOP 3	STOP 2	STOP 1	STOP 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:17	Reserved	Writing has no effect, read as zero.	R
16	WDTS	0: The clock supplies to WDT is supplied 1: The clock supplies to WDT is stopped	R
15	OSTS	0: The clock supplies to OST is supplied 1: The clock supplies to OST is stopped	R
14:8	Reserved	Writing has no effect, read as zero.	R
7	STOP 7	0: The clock supplies to timer 7 is supplied 1: The clock supplies to timer 7 is stopped	R
6	STOP 6	0: The clock supplies to timer 6 is supplied	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: The clock supplies to timer 6 is stopped	
5	STOP 5	0: The clock supplies to timer 5 is supplied 1: The clock supplies to timer 5 is stopped	R
4	STOP 4	0: The clock supplies to timer 4 is supplied 1: The clock supplies to timer 4 is stopped	R
3	STOP 3	0: The clock supplies to timer 3 is supplied 1: The clock supplies to timer 3 is stopped	R
2	STOP 2	0: The clock supplies to timer 2 is supplied 1: The clock supplies to timer 2 is stopped	R
1	STOP 1	0: The clock supplies to timer 1 is supplied 1: The clock supplies to timer 1 is stopped	R
0	STOP 0	0: The clock supplies to timer 0 is supplied 1: The clock supplies to timer 0 is stopped	R

18.4.2.5 Timer Flag Register (TCU_FLAG_RD,0x020)

The TFR is a 32-bit read-only register. It contains the comparison match flag bits for all the channels. It can also be set by register TFSTR and TFCLR. It is initialized to 0x00000000 by any reset.

	TCU_FLAG_RD																Base + 0x020													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							HFLAGW	HFLAG 7	HFLAG 6	HFLAG 5	HFLAG 4	HFLAG 3	HFLAG 2	HFLAG 1	HFLAG 0	OSTFLAG	Reserved								FFLAG 7	FFLAG 6	FFLAG 5	FFLAG 4	FFLAG 3	FFLAG 2	FFLAG 1	FFLAG 0
RST	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect, read as zero.	R
24	HFALGW	HALF comparison match flag of WDT. (TCNT = TDHR) 0: Comparison not match 1: Comparison match Note: wdt flag can not set.	R
23:16	HFLAG 7~0	HALF comparison match flag. (TCNT = TDHR) 0: Comparison not match 1: Comparison match	R
15	OSTFLAG	OST comparison match flag. (OSTCNT = OSTDR) 0: Comparison not match 1: Comparison match	R
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FFLAG 7~0	FULL comparison match flag. (TCNT = TDFR) 0: Comparison not match	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: Comparison match	

18.4.2.6 Timer Flag Set Register (TCU_FLAG_SET,0x024)

The TFSTR is a 32-bit write-only register. It contains the comparison match flag set bits for all the channels.

	TCU_FLAG_SET																Base + 0x024													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HFST7	HFST6	HFST5	HFST4	HFST 3	HFST 2	HFST 1	HFST 0	OSTFST	Reserved							FFST7	FFST6	FFST5	FFST4	FFST 3	FFST 2	FFST 1	FFST 0
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	0	0	?	?	0	0	0	0	0	0	0	?	?	?	?	?	0	0	?

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	HFST 7~0	Set HFLAG n bit of THR. 0: Ignore 1: Set HFLAG n bit to 1	W
15	OSTFST	Set OSTFLAG n bit of TFR. 0: Ignore 1: Set OSTFLAG n bit to 1	W
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FFST 7~0	Set FFLAG n bit of TFR. 0: Ignore 1: Set FFLAG n bit to 1	W

18.4.2.7 Timer Flag Clear Register (TCU_FLAG_CLR,0x028)

The TFCLR is a 32-bit write-only register. It contains the comparison match flag clear bits for all the channels.

	TCU_FLAG_CLR																Base + 0x028													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							HFCLW	HFCL7	HFCL6	HFCL5	HFCL4	HFCL 3	HFCL 2	HFCL 1	HFCL 0	OSTFCL	Reserved							FFCL7	FFCL6	FFCL5	FFCL4	FFCL 3	FFCL 2	FFCL 1	FFCL 0
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect, read as zero.	R
24	HFCLW	Clear HFLAG of WDT_THR.	W

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: Ignore 1: Clear FFLAG n bit to 0	
23:16	HFCL 7~0	Clear HFLAG n bit of TFR. 0: Ignore 1: Clear FFLAG n bit to 0	W
15	OSTFCL	Clear OSTFLAG n bit of TFR. 0: Ignore 1: Clear OSTFLAG n bit to 0	W
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FFCL 7~0	Clear FFLAG n bit of TFR. 0: Ignore 1: Clear FFLAG n bit to 0	W

18.4.2.8 Timer Stop Set Register (TCU_STOP_SET,0x02C)

The TSSTR is an 32-bit write-only register. It contains the timer stop set bits for each channel, WDT and OST. Since the timer stop control set bits are located in the same addresses, two or more timers can be started at the same time.

	TCU_STOP_SET																Base + 0x02C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																WDTSS	OSTSS	Reserved						STPS7	STPS6	STPS5	STPS4	STPS 3	STPS 2	STPS 1	STPS 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:17	Reserved	Writing has no effect, read as zero.	R
16	WDTSS	Set WDTS bit of TSR. 0: Ignore 1: Set WDTS bit to 1	W
15	OSTSS	Set OSTS bit of TSR. 0: Ignore 1: Set OSTS bit to 1	W
14:8	Reserved	Writing has no effect, read as zero.	R
7	STPS 7	Set STOP 7 bit of TSR. 0: Ignore 1: Set STOP 7 bit to 1	W
6	STPS 6	Set STOP 6 bit of TSR. 0: Ignore 1: Set STOP 6 bit to 1	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

5	STPS 5	Set STOP 5 bit of SR. 0: Ignore 1: Set STOP 5 bit to 1	W
4	STPS 4	Set STOP 4 bit of TSR. 0: Ignore 1: Set STOP 4 bit to 1	W
3	STPS 3	Set STOP 3 bit of TSR. 0: Ignore 1: Set STOP 3 bit to 1	W
2	STPS 2	Set STOP 2 bit of TSR. 0: Ignore 1: Set STOP 2 bit to 1	W
1	STPS 1	Set STOP 1 bit of SR. 0: Ignore 1: Set STOP 1 bit to 1	W
0	STPS 0	Set STOP 0 bit of TSR. 0: Ignore 1: Set STOP 0 bit to 1	W

18.4.2.9 Timer Mast Register (TCU_MASK_RD,0x30)

The TMR is a 32-bit read-only register. It contains the comparison match flag bits for all the channels. It is initialized to 0x003F003F by any reset. It can only be set by register TMSTR and TMCLR.

	TCU_MASK_RD																													Base + 0x30
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							HMASKW	HMASK7	HMASK6	HMASK5	HMASK4	HMASK 3	HMASK 2	HMASK 1	HMASK 0	OSTMASK	Reserved							FMASK7	FMASK6	FMASK5	FMASK4	FMASK 3	FMASK 2	FMASK 1	FMASK 0	
RST	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect, read as zero.	R
24	HMASKW	HALF mask for WDT. 0: Comparison match interrupt not mask 1: Comparison match interrupt mask	R
23:16	HMASK 7~0	HALF comparison match interrupt mask. 0: Comparison match interrupt not mask 1: Comparison match interrupt mask	R
15	OSTMASK	OST comparison match interrupt mask. 0: Comparison match interrupt not mask	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: Comparison match interrupt mask	
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FMASK 7~0	FULL comparison match interrupt mask. 0: Comparison match interrupt not mask 1: Comparison match interrupt mask	R

18.4.2.10 Timer Mask Set Register (TCU_MASK_SET,0x034)

The TMSTR is a 32-bit write-only register. It contains the comparison match flag set bits for all the channels.

	TCU_MASK_SET																													
																													Base + 0x034	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							HMSTW	HMST7	HMST6	HMST5	HMST4	HMST 3	HMST 2	HMST 1	HMST 0	OSTMST	Reserved							FMST7	FMST6	FMST5	FMST4	FMST 3	FMST 2	FMST 1	FMST 0
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect, read as zero.	R
24	HMSKW	Set HMASK of WDT. 0: Ignore 1: Set HMASKW to 1	W
23:16	HMSK 7~0	Set HMASK n bit of TMR. 0: Ignore 1: Set HMASK n bit to 1	W
15	OSTMSK	Set OSTMASK n bit of TMR. 0: Ignore 1: Set OSTMASK n bit to 1	W
14:8	Reserved	Writing has no effect, read as zero.	R
7:0	FMSK 7~0	Set FMASK n bit of TMR. 0: Ignore 1: Set FMASK n bit to 1	W

18.4.2.11 Timer Mask Clear Register (TCU_MASK_CLR,0x38)

The TMCLR is a 32-bit write-only register. It contains the comparison match flag clear bits for all the channels.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	TCU_MASK_CLR																													Base + 0x38
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							HMCLW	HMCL7	HMCL6	HMCL5	HMCL4	HMCL 3	HMCL 2	HMCL 1	HMCL 0	OSTMCL	Reserved							FMCL7	FMCL6	FMCL5	FMCL4	FMCL 3	FMCL 2	FMCL 1	FMCL 0
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:25	Reserved	Writing has no effect. Read as zero.	R
24	HMCLW	Set HMASK of WDT. 0: Ignore 1: Set HMASKW to 0	W
23:16	HMCL 7~0	Set HMASK n bit of TMR. 0: Ignore 1: Set HMASK n bit to 0	W
15	OSTMCL	Set OSTMASK n bit of TMR. 0: Ignore 1: Set OSTMASK n bit to 0	W
14:8	Reserved	Writing has no effect. Read as zero.	R
7:0	FMCL 7~0	Set FMASK n bit of TMR. 0: Ignore 1: Set FMASK n bit to 0	W

18.4.2.12 Timer Stop Clear Register (TCU_STOP_CLR,0x03C)

The TSCLR is an 32-bit write-only register. It contains the timer stop clear bits for each channel, WDT and OST. Since the timer stop clear bits are located in the same addresses, two or more timers can be stop at the same time.

	TCU_STOP_CLR																													Base + 0x03C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															WDTSC	OSTSC	Reserved							STPC7	STPC6	STPC5	STPC4	STPC 3	STPC 2	STPC 1	STPC 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:17	Reserved	Writing has no effect. Read as zero.	R
16	WDTSC	Clear WDTS bit of TSR. 0: Ignore 1: Clear WDTS bit to 0	W
15	OSTSC	Clear OSTS bit of TSR. 0: Ignore 1: Clear OSTS bit to 0	W
14:8	Reserved	Writing has no effect. Read as zero.	R
7	STPC 7	Clear STOP 7 bit of TSR. 0: Ignore 1: Clear STOP 7 bit to 0	W
6	STPC 6	Clear STOP 6 bit of TSR. 0: Ignore 1: Clear STOP 6 bit to 0	W
5	STPC 5	Clear STOP 5 bit of TSR. 0: Ignore 1: Clear STOP 5 bit to 0	W
4	STPC 4	Clear STOP 4 bit of TSR. 0: Ignore 1: Clear STOP 4 bit to 0	W
3	STPC 3	Clear STOP 3 bit of TSR. 0: Ignore 1: Clear STOP 3 bit to 0	W
2	STPC 2	Clear STOP 2 bit of TSR. 0: Ignore 1: Clear STOP 2 bit to 0	W
1	STPC 1	Clear STOP 1 bit of TSR. 0: Ignore 1: Clear STOP 1 bit to 0	W
0	STPC 0	Clear STOP 0 bit of TSR. 0: Ignore 1: Clear STOP 0 bit to 0	W

18.4.2.13 Timer Data FULL Register0(TCU_FULL0,0x040)

The comparison data FULL registers TDFR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)
the true value is n-1

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	TCU_FULL0																Base + 0x040															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.14 Timer Data HALF Register0 (TCU_HALF0,0x044)

The comparison data HALF registers TDHR0 is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)
the true value is n-1

	TCU_HALF0																Base + 0x044															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.15 Timer Counter0 (TCU_COUNT0,0x048)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR0, it will reset to 0 and continue to count up. **TCU1**: The counter data can be read out at any time. The data can be written at any time. This makes it possible to change the interrupt and/or clock output cycles temporarily.
(Default: indeterminate)

	TCU_COUNT0																Base + 0x048															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.4.2.16 Timer Control Register0 (TCU_CONTROL0,0x04C)

The TCSR0 is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	TCU_CONTROL0																Base + 0x04C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								COUNT_MODE		GPIO1_NEG_EN	GPIO1_POS_EN	GPIO0_NEG_EN	GPIO0_POS_EN	CLK_NEG_EN	CLK_POS_EN	SHUTDOWN	GATE_POLA	DIRECTION_POLA	GATE_SEL		DIRECTION_SEL			GPIO1_EN	GPIO0_EN	PRESCALE			EXT_EN	Reserved	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:22	COUNT_MODE	0：count range 0 <-> full with clear to 0. 1：count range 0 <-> 0xffffffff with clear to 0. 2：count range 0 <-> 0xffffffff with hold on.	RW
21	GPIO1_NEG_EN	Indicate TCU will count when gpio1 input a negedge.	RW
20	GPIO1_POS_EN	Indicate TCU will count when gpio1 input a posedge.	RW
19	GPIO0_NEG_EN	Indicate TCU will count when gpio0 input a negedge.	RW
18	GPIO0_POS_EN	Indicate TCU will count when gpio0 input a posedge.	RW
17	CLK_NEG_EN	Indicate TCU will count when select clock input a negedge.	RW
16	CLK_POS_EN	Indicate TCU will count when select clock input a posedge.	RW
15	SHUTDOWN	When this bit is 1, counter will stop counting after full, the count value is full value.	RW
14	GATE_POLA	0：counter start when control signal is 0. 1：counter start when control signal is 1.	RW
13	DIRECTION_POLA	0：counter sub when control signal is 0. 1：counter sub when control signal is 1.	RW
12:11	GATE_SEl	0：gate signal hold on 0. 1：use clock with gate signal. 2：use gpio0 with gate signal. 3：use gpio1 with gate signal.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td>10:8</td><td>DIRECTION_SEL</td><td>0：direction signal hold on 1.
1：use clock with direction signal.
2：use gpio0 with direction signal.
3：use gpio1 with direction signal.
4: use gpio0 and gpio1 quadrature result with direction signal.</td><td>RW</td></tr>
<tr><td>7</td><td>GPIO1_EN</td><td>Gpio1 function enable.</td><td>RW</td></tr>
<tr><td>6</td><td>GPIO0_EN</td><td>Gpio0 function enable.</td><td>RW</td></tr>
<tr><td>5:3</td><td>PRESCALE</td><td>These bits select the TCNT count clock frequency. Don’t change this field when the channel is running.
<table>
<tr><th>Bit 2</th><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internal clock: CLK/64</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Internal clock: CLK/256</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Internal clock: CLK/1024</td></tr>
<tr><td colspan="3">110~111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>2</td><td>EXT_EN</td><td>Select EXTAL as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
<tr><td>1:0</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
</table>

18.4.2.17 Timer Data FULL Register1 (TCU_FULL1,0x050)

The comparison data FULL registers TDFR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)
the true value is n-1

	TCU_FULL1																Base + 0x050															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.18 Timer Data HALF Register1 (TCU_HALF1,0x054)

The comparison data FULL registers TDFR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)
the true value is n-1

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	TCU_HALF1																Base + 0x054															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.19 Timer Counter1 (TCU_COUNT1,0x058)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR0, it will reset to 0 and continue to count up. **TCU1**: The counter data can be read out at any time. The data can be written at any time. This makes it possible to change the interrupt and/or clock output cycles temporarily. (Default: indeterminate)

	TCU_COUNT1																Base + 0x058															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.20 Timer Control Register1(TCU_CONTROL1,0x05C)

The TCSR1 is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	TCU_CONTROL1																Base + 0x05C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								COUNT_MODE		GPIO1_NEG_EN	GPIO1_POS_EN	GPIO0_NEG_EN	GPIO0_POS_EN	CLK_NEG_EN	CLK_POS_EN	SHUTDOWN	GATE_POLA	DIRECTION_POLA	GATE_SEL		DIRECTION_SEL			GPIO1_EN	GPIO0_EN	PRESCALE			EXT_EN	Reserved		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>RW</th></tr>
<tr><td>31:12</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>23:22</td><td>COUNT_MODE</td><td>0：count range 0 <-> full with clear to 0.
1：count range 0 <-> 0xffffffff with clear to 0.
2：count range 0 <-> 0xffffffff with hold on.</td><td>RW</td></tr>
<tr><td>21</td><td>GPIO1_NEG_EN</td><td>Indicate TCU will count when gpio1 input a negedge.</td><td>RW</td></tr>
<tr><td>20</td><td>GPIO1_POS_EN</td><td>Indicate TCU will count when gpio1 input a posedge.</td><td>RW</td></tr>
<tr><td>19</td><td>GPIO0_NEG_EN</td><td>Indicate TCU will count when gpio0 input a negedge.</td><td>RW</td></tr>
<tr><td>18</td><td>GPIO0_POS_EN</td><td>Indicate TCU will count when gpio0 input a posedge.</td><td>RW</td></tr>
<tr><td>17</td><td>CLK_NEG_EN</td><td>Indicate TCU will count when select clock input a negedge.</td><td>RW</td></tr>
<tr><td>16</td><td>CLK_POS_EN</td><td>Indicate TCU will count when select clock input a posedge.</td><td>RW</td></tr>
<tr><td>15</td><td>SHUTDOWN</td><td>When this bit is 1, counter will stop counting after full, the count value is full value.</td><td>RW</td></tr>
<tr><td>14</td><td>GATE_POLA</td><td>0：counter start when control signal is 0.
1：counter start when control signal is 1.</td><td>RW</td></tr>
<tr><td>13</td><td>DIRECTION_POLA</td><td>0：counter sub when control signal is 0.
1：counter sub when control signal is 1.</td><td>RW</td></tr>
<tr><td>12:11</td><td>GATE_SEl</td><td>0：gate signal hold on 0.
1：use clock with gate signal.
2：use gpio0 with gate signal.
3：use gpio1 with gate signal.</td><td>RW</td></tr>
<tr><td>10:8</td><td>DIRECTION_SEL</td><td>0：direction signal hold on 1.
1：use clock with direction signal.
2：use gpio0 with direction signal.
3：use gpio1 with direction signal.
4: use gpio0 and gpio1 quadrature result with direction signal.</td><td>RW</td></tr>
<tr><td>7</td><td>GPIO1_EN</td><td>Gpio1 function enable.</td><td>RW</td></tr>
<tr><td>6</td><td>GPIO0_EN</td><td>Gpio0 function enable.</td><td>RW</td></tr>
<tr><td>5:3</td><td>PRESCALE</td><td>These bits select the TCNT count clock frequency. Don’t change this field when the channel is running.
<table>
<tr><th>Bit 2</th><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internal clock: CLK/64</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Internal clock: CLK/256</td></tr>
</table></td><td>RW</td></tr>
</table>

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1	0	1	Internal clock: CLK/1024	
		110~111			Reserved	
2	EXT_EN	Select EXTAL as the timer clock input. 0: Disable 1: Enable				RW
1:0	Reserved	Writing has no effect, read as zero.				R

18.4.2.21 Timer Data FULL Register2 (TCU_FULL2,0x060)

The comparison data FULL registers TDFR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)
the true value is n-1

	TCU_FULL2																Base + 0x060															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.22 Timer Data HALF Register2 (TCU_HALF2,0x064)

The comparison data FULL registers TDFR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)
the true value is n-1

	TCU_HALF2																Base + 0x064															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.23 Timer Counter2(TCU_COUNT2,0x068)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR0, it will reset to 0 and continue to count up. **TCU1**: The counter data can be read out at any time. The data can be written at

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

any time. This makes it possible to change the interrupt and/or clock output cycles temporarily. (Default: indeterminate)

	TCU_COUNT2																Base + 0x068															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.24 Timer Control Register2(TCU_CONTROL2,0x06C)

The TCSR1 is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	TCU_CONTROL2																Base + 0x06C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								COUNT_MODE		GPIO1_NEG_EN	GPIO1_POS_EN	GPIO0_NEG_EN	GPIO0_POS_EN	CLK_NEG_EN	CLK_POS_EN	SHUTDOWN	GATE_POLA	DIRECTION_POLA	GATE_SEL		DIRECTION_SEL			GPIO1_EN	GPIO0_EN	PRESCALE			EXT_EN	Reserved		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
23:22	COUNT_MODE	0：count range 0 <-> full with clear to 0. 1：count range 0 <-> 0xffffffff with clear to 0. 2：count range 0 <-> 0xffffffff with hold on.	RW
21	GPIO1_NEG_EN	Indicate TCU will count when gpio1 input a negedge.	RW
20	GPIO1_POS_EN	Indicate TCU will count when gpio1 input a posedge.	RW
19	GPIO0_NEG_EN	Indicate TCU will count when gpio0 input a negedge.	RW
18	GPIO0_POS_EN	Indicate TCU will count when gpio0 input a posedge.	RW
17	CLK_NEG_EN	Indicate TCU will count when select clock input a negedge.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td>16</td><td>CLK_POS_EN</td><td>Indicate TCU will count when select clock input a posedge.</td><td>RW</td></tr>
<tr><td>15</td><td>SHUTDOWN</td><td>When this bit is 1, counter will stop counting after full, the count value is full value.</td><td>RW</td></tr>
<tr><td>14</td><td>GATE_POLA</td><td>0：counter start when control signal is 0.
1：counter start when control signal is 1.</td><td>RW</td></tr>
<tr><td>13</td><td>DIRECTION_POLA</td><td>0：counter sub when control signal is 0.
1：counter sub when control signal is 1.</td><td>RW</td></tr>
<tr><td>12:11</td><td>GATE_SEl</td><td>0：gate signal hold on 0.
1：use clock with gate signal.
2：use gpio0 with gate signal.
3：use gpio1 with gate signal.</td><td>RW</td></tr>
<tr><td>10:8</td><td>DIRECTION_SEL</td><td>0：direction signal hold on 1.
1：use clock with direction signal.
2：use gpio0 with direction signal.
3：use gpio1 with direction signal.
4: use gpio0 and gpio1 quadrature result with direction signal.</td><td>RW</td></tr>
<tr><td>7</td><td>GPIO1_EN</td><td>Gpio1 function enable.</td><td>RW</td></tr>
<tr><td>6</td><td>GPIO0_EN</td><td>Gpio0 function enable.</td><td>RW</td></tr>
<tr><td>5:3</td><td>PRESCALE</td><td>These bits select the TCNT count clock frequency. Don’t change this field when the channel is running.
<table>
<tr><th>Bit 2</th><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internal clock: CLK/64</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Internal clock: CLK/256</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Internal clock: CLK/1024</td></tr>
<tr><td colspan="3">110~111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>2</td><td>EXT_EN</td><td>Select EXTAL as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
<tr><td>1:0</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
</table>

18.4.2.25 Timer Data FULL Register3 (TCU_FULL3,0x070)

The comparison data FULL registers TDFR3 is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)
the true value is n-1

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	TCU_FULL3																Base + 0x070															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.26 Timer Data HALF Register3 (TCU_HALF3,0x074)

The comparison data HALF registers TDHR3 is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)
the true value is n-1

	TCU_HALF3																Base + 0x074															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.27 Timer Counter3 (TCU_COUNT3,0x078)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR3, it will reset to 0 and continue to count up. **TCU1**: The counter data can be read out at any time. The data can be written at any time. This makes it possible to change the interrupt and/or clock output cycles temporarily. (Default: indeterminate)

	TCU_COUNT3																Base + 0x078															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.4.2.28 Timer Control Register3(TCU_CONTROL3,0x07C)

The TCSR3 is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	TCU_CONTROL3																Base + 0x07C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								COUNT_MODE		GPIO1_NEG_EN	GPIO1_POS_EN	GPIO0_NEG_EN	GPIO0_POS_EN	CLK_NEG_EN	CLK_POS_EN	SHUTDOWN	GATE_POLA	DIRECTION_POLA	GATE_SEL		DIRECTION_SEL			GPIO1_EN	GPIO0_EN	PRESCALE			EXT_EN	Reserved	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
23:22	COUNT_MODE	0：count range 0 <-> full with clear to 0. 1：count range 0 <-> 0xffffffff with clear to 0. 2：count range 0 <-> 0xffffffff with hold on.	RW
21	GPIO1_NEG_EN	Indicate TCU will count when gpio1 input a negedge.	RW
20	GPIO1_POS_EN	Indicate TCU will count when gpio1 input a posedge.	RW
19	GPIO0_NEG_EN	Indicate TCU will count when gpio0 input a negedge.	RW
18	GPIO0_POS_EN	Indicate TCU will count when gpio0 input a posedge.	RW
17	CLK_NEG_EN	Indicate TCU will count when select clock input a negedge.	RW
16	CLK_POS_EN	Indicate TCU will count when select clock input a posedge.	RW
15	SHUTDOWN	When this bit is 1, counter will stop counting after full, the count value is full value.	RW
14	GATE_POLA	0：counter start when control signal is 0. 1：counter start when control signal is 1.	RW
13	DIRECTION_POLA	0：counter sub when control signal is 0. 1：counter sub when control signal is 1.	RW
12:11	GATE_SEl	0：gate signal hold on 0. 1：use clock with gate signal. 2：use gpio0 with gate signal. 3：use gpio1 with gate signal.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td>10:8</td><td>DIRECTION_SEL</td><td>0：direction signal hold on 1.
1：use clock with direction signal.
2：use gpio0 with direction signal.
3：use gpio1 with direction signal.
4: use gpio0 and gpio1 quadrature result with direction signal.</td><td>RW</td></tr>
<tr><td>7</td><td>GPIO1_EN</td><td>Gpio1 function enable.</td><td>RW</td></tr>
<tr><td>6</td><td>GPIO0_EN</td><td>Gpio0 function enable.</td><td>RW</td></tr>
<tr><td>5:3</td><td>PRESCALE</td><td>These bits select the TCNT count clock frequency. Don’t change this field when the channel is running.
<table>
<tr><th>Bit 2</th><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internal clock: CLK/64</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Internal clock: CLK/256</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Internal clock: CLK/1024</td></tr>
<tr><td colspan="3">110~111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>2</td><td>EXT_EN</td><td>Select EXTAL as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
<tr><td>1:0</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
</table>

18.4.2.29 Timer Data FULL Register4 (TCU_FULL4,0x080)

The comparison data FULL registers TDFR4 is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)
the true value is n-1

	TCU_FULL4																Base + 0x080															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.30 Timer Data HALF Register4 (TCU_HALF4,0x084)

The comparison data HALF registers TDHR4 is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)
the true value is n-1

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	TCU_HALF4																Base + 0x084															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.31 Timer Counter4 (TCU_COUNT4,0x088)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR4, it will reset to 0 and continue to count up. **TCU1**: The counter data can be read out at any time. The data can be written at any time. This makes it possible to change the interrupt and/or clock output cycles temporarily. (Default: indeterminate)

	TCU_COUNT4																Base + 0x088															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.32 Timer Control Register4(TCU_CONTROL4,0x08C)

The TCSR4 is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	TCU_CONTROL4																Base + 0x08C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								COUNT_MODE	GPIO1_NEG_EN	GPIO1_POS_EN	GPIO0_NEG_EN	GPIO0_POS_EN	CLK_NEG_EN	CLK_POS_EN		SHUTDOWN	GATE_POLA	DIRECTION_POLA	GATE_SEL		DIRECTION_SEL			GPIO1_EN	GPIO0_EN	PRESCALE			EXT_EN	Reserved	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td>23:22</td><td>COUNT_MODE</td><td>0：count range 0 <-> full with clear to 0.
1：count range 0 <-> 0xffffffff with clear to 0.
2：count range 0 <-> 0xffffffff with hold on.</td><td>RW</td></tr>
<tr><td>21</td><td>GPIO1_NEG_EN</td><td>Indicate TCU will count when gpio1 input a negedge.</td><td>RW</td></tr>
<tr><td>20</td><td>GPIO1_POS_EN</td><td>Indicate TCU will count when gpio1 input a posedge.</td><td>RW</td></tr>
<tr><td>19</td><td>GPIO0_NEG_EN</td><td>Indicate TCU will count when gpio0 input a negedge.</td><td>RW</td></tr>
<tr><td>18</td><td>GPIO0_POS_EN</td><td>Indicate TCU will count when gpio0 input a posedge.</td><td>RW</td></tr>
<tr><td>17</td><td>CLK_NEG_EN</td><td>Indicate TCU will count when select clock input a negedge.</td><td>RW</td></tr>
<tr><td>16</td><td>CLK_POS_EN</td><td>Indicate TCU will count when select clock input a posedge.</td><td>RW</td></tr>
<tr><td>15</td><td>SHUTDOWN</td><td>When this bit is 1, counter will stop counting after full, the count value is full value.</td><td>RW</td></tr>
<tr><td>14</td><td>GATE_POLA</td><td>0：counter start when control signal is 0.
1：counter start when control signal is 1.</td><td>RW</td></tr>
<tr><td>13</td><td>DIRECTION_POLA</td><td>0：counter sub when control signal is 0.
1：counter sub when control signal is 1.</td><td>RW</td></tr>
<tr><td>12:11</td><td>GATE_SEl</td><td>0：gate signal hold on 0.
1：use clock with gate signal.
2：use gpio0 with gate signal.
3：use gpio1 with gate signal.</td><td>RW</td></tr>
<tr><td>10:8</td><td>DIRECTION_SEL</td><td>0：direction signal hold on 1.
1：use clock with direction signal.
2：use gpio0 with direction signal.
3：use gpio1 with direction signal.
4: use gpio0 and gpio1 quadrature result with direction signal.</td><td>RW</td></tr>
<tr><td>7</td><td>GPIO1_EN</td><td>Gpio1 function enable.</td><td>RW</td></tr>
<tr><td>6</td><td>GPIO0_EN</td><td>Gpio0 function enable.</td><td>RW</td></tr>
<tr><td>5:3</td><td>PRESCALE</td><td>These bits select the TCNT count clock frequency. Don’t change this field when the channel is running.
<table>
<tr><th>Bit 2</th><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internal clock: CLK/64</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Internal clock: CLK/256</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Internal clock: CLK/1024</td></tr>
<tr><td colspan="3">110~111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
</table>

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

2	EXT_EN	Select EXTAL as the timer clock input. 0: Disable 1: Enable	RW
1:0	Reserved	Writing has no effect, read as zero.	R

18.4.2.33 Timer Data FULL Register5 (TCU_FULL5,0x090)

The comparison data FULL registers TDFR5 is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)
the true value is n-1

	TCU_FULL5																Base + 0x090															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.34 Timer Data HALF Register5 (TCU_HALF5,0x094)

The comparison data HALF registers TDHR5 is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)
the true value is n-1

	TCU_HALF5																Base + 0x094															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.35 Timer Counter5 (TCU_COUNT5,0x098)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR5, it will reset to 0 and continue to count up. **TCU1**: The counter data can be read out at any time. The data can be written at any time. This makes it possible to change the interrupt and/or clock output cycles temporarily. (Default: indeterminate)

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	TCU_COUNT5																Base + 0x098															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.36 Timer Control Register5(TCU_CONTROL5,0x09C)

The TCSR5 is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	TCU_CONTROL5																Base + 0x09C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								COUNT_MODE		GPIO1_NEG_EN	GPIO1_POS_EN	GPIO0_NEG_EN	GPIO0_POS_EN	CLK_NEG_EN	CLK_POS_EN	SHUTDOWN	GATE_POLA	DIRECTION_POLA	GATE_SEL		DIRECTION_SEL			GPIO1_EN	GPIO0_EN	PRESCALE			EXT_EN	Reserved		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
23:22	COUNT_MODE	0：count range 0 <-> full with clear to 0. 1：count range 0 <-> 0xffffffff with clear to 0. 2：count range 0 <-> 0xffffffff with hold on.	RW
21	GPIO1_NEG_EN	Indicate TCU will count when gpio1 input a negedge.	RW
20	GPIO1_POS_EN	Indicate TCU will count when gpio1 input a posedge.	RW
19	GPIO0_NEG_EN	Indicate TCU will count when gpio0 input a negedge.	RW
18	GPIO0_POS_EN	Indicate TCU will count when gpio0 input a posedge.	RW
17	CLK_NEG_EN	Indicate TCU will count when select clock input a negedge.	RW
16	CLK_POS_EN	Indicate TCU will count when select clock input a posedge.	RW
15	SHUTDOWN	When this bit is 1, counter will stop counting after full, the count value is full value.	RW
14	GATE_POLA	0：counter start when control signal is 0.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td></td><td></td><td>1：counter start when control signal is 1.</td><td></td></tr>
<tr><td>13</td><td>DIRECTION_POLA</td><td>0：counter sub when control signal is 0.
1：counter sub when control signal is 1.</td><td>RW</td></tr>
<tr><td>12:11</td><td>GATE_SEl</td><td>0：gate signal hold on 0.
1：use clock with gate signal.
2：use gpio0 with gate signal.
3：use gpio1 with gate signal.</td><td>RW</td></tr>
<tr><td>10:8</td><td>DIRECTION_SEL</td><td>0：direction signal hold on 1.
1：use clock with direction signal.
2：use gpio0 with direction signal.
3：use gpio1 with direction signal.
4: use gpio0 and gpio1 quadrature result with direction signal.</td><td>RW</td></tr>
<tr><td>7</td><td>GPIO1_EN</td><td>Gpio1 function enable.</td><td>RW</td></tr>
<tr><td>6</td><td>GPIO0_EN</td><td>Gpio0 function enable.</td><td>RW</td></tr>
<tr><td>5:3</td><td>PRESCALE</td><td>These bits select the TCNT count clock frequency. Don’t change this field when the channel is running.
<table>
<tr><th>Bit 2</th><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internal clock: CLK/64</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Internal clock: CLK/256</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Internal clock: CLK/1024</td></tr>
<tr><td colspan="3">110~111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>2</td><td>EXT_EN</td><td>Select EXTAL as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
<tr><td>1:0</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
</table>

18.4.2.37 Timer Data FULL Register6 (TCU_FULL6,0x0A0)

The comparison data FULL registers TDFR6 is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)
the true value is n-1

	TCU_FULL6																Base + 0x0A0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.4.2.38 Timer Data HALF Register6 (TCU_HALF6,0x0A4)

The comparison data HALF registers TDHR6 is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)
the true value is n-1

	TCU_HALF6																Base + 0x0A4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.39 Timer Counter6 (TCU_COUNT6,0x0A8)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR6, it will reset to 0 and continue to count up. **TCU1**: The counter data can be read out at any time. The data can be written at any time. This makes it possible to change the interrupt and/or clock output cycles temporarily. (Default: indeterminate)

	TCU_COUNT6																Base + 0x0A8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.40 Timer Control Register6(TCU_CONTROL6,0x0AC)

The TCSR6 is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	TCU_CONTROL6																Base + 0x0AC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								COUNT_MODE		GPIO1_NEG_EN	GPIO1_POS_EN	GPIO0_NEG_EN	GPIO0_POS_EN	CLK_NEG_EN	CLK_POS_EN	SHUTDOWN	GATE_POLA	DIRECTION_POLA	GATE_SEL		DIRECTION_SEL			GPIO1_EN	GPIO0_EN	PRESCALE			EXT_EN	Reserved		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>RW</th></tr>
<tr><td>31:12</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>23:22</td><td>COUNT_MODE</td><td>0：count range 0 <-> full with clear to 0.
1：count range 0 <-> 0xffffffff with clear to 0.
2：count range 0 <-> 0xffffffff with hold on.</td><td>RW</td></tr>
<tr><td>21</td><td>GPIO1_NEG_EN</td><td>Indicate TCU will count when gpio1 input a negedge.</td><td>RW</td></tr>
<tr><td>20</td><td>GPIO1_POS_EN</td><td>Indicate TCU will count when gpio1 input a posedge.</td><td>RW</td></tr>
<tr><td>19</td><td>GPIO0_NEG_EN</td><td>Indicate TCU will count when gpio0 input a negedge.</td><td>RW</td></tr>
<tr><td>18</td><td>GPIO0_POS_EN</td><td>Indicate TCU will count when gpio0 input a posedge.</td><td>RW</td></tr>
<tr><td>17</td><td>CLK_NEG_EN</td><td>Indicate TCU will count when select clock input a negedge.</td><td>RW</td></tr>
<tr><td>16</td><td>CLK_POS_EN</td><td>Indicate TCU will count when select clock input a posedge.</td><td>RW</td></tr>
<tr><td>15</td><td>SHUTDOWN</td><td>When this bit is 1, counter will stop counting after full, the count value is full value.</td><td>RW</td></tr>
<tr><td>14</td><td>GATE_POLA</td><td>0：counter start when control signal is 0.
1：counter start when control signal is 1.</td><td>RW</td></tr>
<tr><td>13</td><td>DIRECTION_POLA</td><td>0：counter sub when control signal is 0.
1：counter sub when control signal is 1.</td><td>RW</td></tr>
<tr><td>12:11</td><td>GATE_SEl</td><td>0：gate signal hold on 0.
1：use clock with gate signal.
2：use gpio0 with gate signal.
3：use gpio1 with gate signal.</td><td>RW</td></tr>
<tr><td>10:8</td><td>DIRECTION_SEL</td><td>0：direction signal hold on 1.
1：use clock with direction signal.
2：use gpio0 with direction signal.
3：use gpio1 with direction signal.
4: use gpio0 and gpio1 quadrature result with direction signal.</td><td>RW</td></tr>
<tr><td>7</td><td>GPIO1_EN</td><td>Gpio1 function enable.</td><td>RW</td></tr>
<tr><td>6</td><td>GPIO0_EN</td><td>Gpio0 function enable.</td><td>RW</td></tr>
<tr><td>5:3</td><td>PRESCALE</td><td>These bits select the TCNT count clock frequency. Don’t change this field when the channel is running.
<table>
<tr><th>Bit 2</th><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internal clock: CLK/64</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Internal clock: CLK/256</td></tr>
</table></td><td>RW</td></tr>
</table>

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1	0	1	Internal clock: CLK/1024		
		110~111			Reserved		
2	EXT_EN	Select EXTAL as the timer clock input. 0: Disable 1: Enable					RW
1:0	Reserved	Writing has no effect, read as zero.					R

18.4.2.41 Timer Data FULL Register7 (TCU_FULL7,0x0B0)

The comparison data FULL registers TDFR7 is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)
the true value is n-1

	TCU_FULL7																Base + 0x0B0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDFR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.42 Timer Data HALF Register7 (TCU_HALF7,0x0B4)

The comparison data HALF registers TDHR7 is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)
the true value is n-1

	TCU_HALF7																Base + 0x0B4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TDHR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.43 Timer Counter7 (TCU_COUNT7,0x0B8)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR7, it will reset to 0 and continue to count up. **TCU1**: The counter data can be read out at any time. The data can be written at any time. This makes it possible to change the interrupt and/or clock output cycles temporarily. (Default: indeterminate)

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	TCU_COUNT7																Base + 0x0B8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

18.4.2.44 Timer Control Register7(TCU_CONTROL7,0x0BC)

The TCSR7 is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	TCU_CONTROL7																Base + 0x0BC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								COUNT_MODE		GPIO1_NEG_EN	GPIO1_POS_EN	GPIO0_NEG_EN	GPIO0_POS_EN	CLK_NEG_EN	CLK_POS_EN	SHUTDOWN	GATE_POLA	DIRECTION_POLA	GATE_SEL		DIRECTION_SEL			GPIO1_EN	GPIO0_EN	PRESCALE			EXT_EN	Reserved		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Writing has no effect, read as zero.	R
23:22	COUNT_MODE	0：count range 0 <-> full with clear to 0. 1：count range 0 <-> 0xffffffff with clear to 0. 2：count range 0 <-> 0xffffffff with hold on.	RW
21	GPIO1_NEG_EN	Indicate TCU will count when gpio1 input a negedge.	RW
20	GPIO1_POS_EN	Indicate TCU will count when gpio1 input a posedge.	RW
19	GPIO0_NEG_EN	Indicate TCU will count when gpio0 input a negedge.	RW
18	GPIO0_POS_EN	Indicate TCU will count when gpio0 input a posedge.	RW
17	CLK_NEG_EN	Indicate TCU will count when select clock input a negedge.	RW
16	CLK_POS_EN	Indicate TCU will count when select clock input a posedge.	RW
15	SHUTDOWN	When this bit is 1, counter will stop counting after full, the count value is full value.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td>14</td><td>GATE_POLA</td><td>0：counter start when control signal is 0.
1：counter start when control signal is 1.</td><td>RW</td></tr>
<tr><td>13</td><td>DIRECTION_ POLA</td><td>0：counter sub when control signal is 0.
1：counter sub when control signal is 1.</td><td>RW</td></tr>
<tr><td>12:11</td><td>GATE_SEl</td><td>0：gate signal hold on 0.
1：use clock with gate signal.
2：use gpio0 with gate signal.
3：use gpio1 with gate signal.</td><td>RW</td></tr>
<tr><td>10:8</td><td>DIRECTION_ SEL</td><td>0：direction signal hold on 1.
1：use clock with direction signal.
2：use gpio0 with direction signal.
3：use gpio1 with direction signal.
4: use gpio0 and gpio1 quadrature result with direction signal.</td><td>RW</td></tr>
<tr><td>7</td><td>GPIO1_EN</td><td>Gpio1 function enable.</td><td>RW</td></tr>
<tr><td>6</td><td>GPIO0_EN</td><td>Gpio0 function enable.</td><td>RW</td></tr>
<tr><td>5:3</td><td>PRESCALE</td><td>These bits select the TCNT count clock frequency. Don’t change this field when the channel is running.
<table>
<tr><th>Bit 2</th><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internal clock: CLK/64</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Internal clock: CLK/256</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Internal clock: CLK/1024</td></tr>
<tr><td colspan="3">110~111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>2</td><td>EXT_EN</td><td>Select EXTAL as the timer clock input.
0: Disable
1: Enable</td><td>RW</td></tr>
<tr><td>1:0</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
</table>

NOTE: The input clock of timer and the PCLK should keep to the rules as follows:

Input clock of timer: IN_CLK	**Clock generated from the frequency divider (PRESCALE): DIV_CLK**
PCK_EN == 0, RTC_EN == 1 and EXT_EN == 0 (IN_CLK = RTCCLK)	$f_{DIV_CLK} < ½ f_{PCLK}$
PCK_EN == 0, RTC_EN == 0 and EXT_EN == 1 (IN_CLK = EXTAL)	$f_{DIV_CLK} < ½ f_{PCLK}$
PCK_EN == 1, RTC_EN == 0 and EXT_EN == 0 (IN_CLK = PCLK)	ANY

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.4.2.45 Capture0(TCU_CAPTURE0,0x0C0)

	TCU_CAPTURE0																Base + 0x0C0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													CAPTURE_SEL			Reserved								CAPTURE_NUM							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18:16	CAPTURE_SEL	0：TCU will capture clock. 1：TCU will capture gpio0. 2：TCU will capture gpio1. * if capture mode is disable then these bits will: 1：counter will clear when gpio0 posedge. 2：counter will clear when gpio1 posedge. 3：counter will clear when gpio0 negedge.	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7:0	CAPTURE_NUM	Capture times, when times is bigger than 0x80, than TCU will always in capture mode.	RW

18.4.2.46 Capture1(TCU_CAPTURE1,0x0C4)

	TCU_CAPTURE1																Base + 0x0C4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													CAPTURE_SEL			Reserved								CAPTURE_NUM							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18:16	CAPTURE_SEL	0：TCU will capture clock. 1：TCU will capture gpio0. 2：TCU will capture gpio1. * if capture mode is disable then these bits will:	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1：counter will clear when gpio0 posedge. 2：counter will clear when gpio1 posedge. 3：counter will clear when gpio0 negedge.	
15:8	Reserved	Writing has no effect, read as zero.	R
7:0	CAPTURE_NUM	Capture times, when times is bigger than 0x80, than TCU will always in capture mode.	RW

18.4.2.47 Capture2(TCU_CAPTURE2,0x0C8)

	TCU_CAPTURE2																Base + 0x0C8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													CAPTURE_SEL			Reserved								CAPTURE_NUM							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18:16	CAPTURE_SEL	0：TCU will capture clock. 1：TCU will capture gpio0. 2：TCU will capture gpio1. * if capture mode is disable then these bits will: 1：counter will clear when gpio0 posedge. 2：counter will clear when gpio1 posedge. 3：counter will clear when gpio0 negedge.	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7:0	CAPTURE_NUM	Capture times, when times is bigger than 0x80, than TCU will always in capture mode.	RW

18.4.2.48 Capture3(TCU_CAPTURE3,0x0CC)

	TCU_CAPTURE3																Base + 0x0CC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													CAPTURE_SEL			Reserved								CAPTURE_NUM							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18:16	CAPTURE_SEL	0：TCU will capture clock. 1：TCU will capture gpio0. 2：TCU will capture gpio1. * if capture mode is disable then these bits will: 1：counter will clear when gpio0 posedge. 2：counter will clear when gpio1 posedge. 3：counter will clear when gpio0 negedge.	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7:0	CAPTURE_NUM	Capture times, when times is bigger than 0x80, than TCU will always in capture mode.	RW

18.4.2.49 Capture4(TCU_CAPTURE4,0x0D0)

TCU_CAPTURE4																Base + 0x0D0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													CAPTURE_SEL			Reserved								CAPTURE_NUM							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18:16	CAPTURE_SEL	0：TCU will capture clock. 1：TCU will capture gpio0. 2：TCU will capture gpio1. * if capture mode is disable then these bits will: 1：counter will clear when gpio0 posedge. 2：counter will clear when gpio1 posedge. 3：counter will clear when gpio0 negedge.	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7:0	CAPTURE_NUM	Capture times, when times is bigger than 0x80, than TCU will always in capture mode.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.4.2.50 Capture5(TCU_CAPTURE5,0x0D4)

	TCU_CAPTURE5																Base + 0x0D4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													CAPTURE_SEL			Reserved								CAPTURE_NUM							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18:16	CAPTURE_SEL	0：TCU will capture clock. 1：TCU will capture gpio0. 2：TCU will capture gpio1. * if capture mode is disable then these bits will: 1：counter will clear when gpio0 posedge. 2：counter will clear when gpio1 posedge. 3：counter will clear when gpio0 negedge.	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7:0	CAPTURE_NUM	Capture times, when times is bigger than 0x80, than TCU will always in capture mode.	RW

18.4.2.51 Capture6(TCU_CAPTURE6,0x0D8)

	TCU_CAPTURE6																Base + 0x0D8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													CAPTURE_SEL			Reserved								CAPTURE_NUM							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18:16	CAPTURE_SEL	0：TCU will capture clock. 1：TCU will capture gpio0. 2：TCU will capture gpio1. * if capture mode is disable then these bits will:	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1：counter will clear when gpio0 posedge. 2：counter will clear when gpio1 posedge. 3：counter will clear when gpio0 negedge.	
15:8	Reserved	Writing has no effect, read as zero.	R
7:0	CAPTURE_NUM	Capture times, when times is bigger than 0x80, than TCU will always in capture mode.	RW

18.4.2.52 Capture7(TCU_CAPTURE7,0x0DC)

	TCU_CAPTURE7																Base + 0x0DC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													CAPTURE_SEL			Reserved								CAPTURE_NUM							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:19	Reserved	Writing has no effect, read as zero.	R
18:16	CAPTURE_SEL	0：TCU will capture clock. 1：TCU will capture gpio0. 2：TCU will capture gpio1. * if capture mode is disable then these bits will: 1：counter will clear when gpio0 posedge. 2：counter will clear when gpio1 posedge. 3：counter will clear when gpio0 negedge.	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7:0	CAPTURE_NUM	Capture times, when times is bigger than 0x80, than TCU will always in capture mode.	RW

18.4.2.53 Capture Value0(TCU_CAP_VALUE0,0x0E0)

	TCU_CAP_VALUE0																Base + 0x0E0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CAPTURE_ALL																CAPTURE_HEIGHT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:16	CAPTURE_ALL	Indicate the whole time of the period.	R
15:0	CAPTURE_HEIGHT	Indicate the time of high level.	R

18.4.2.54 Capture Value1(TCU_CAP_VALUE1,0x0E4)

	TCU_CAP_VALUE1																Base + 0x0E4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CAPTURE_ALL																CAPTURE_HEIGHT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CAPTURE_ALL	Indicate the whole time of the period.	R
15:0	CAPTURE_HEIGHT	Indicate the time of high level.	R

18.4.2.55 Capture Value2(TCU_CAP_VALUE2,0x0E8)

	TCU_CAP_VALUE8																Base + 0x0E8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CAPTURE_ALL																CAPTURE_HEIGHT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CAPTURE_ALL	Indicate the whole time of the period.	R
15:0	CAPTURE_HEIGHT	Indicate the time of high level.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.4.2.56 Capture Value3(TCU_CAP_VALUE3,0x0EC)

	TCU_CAP_VALUE3																Base + 0x0EC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CAPTURE_ALL																CAPTURE_HEIGHT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CAPTURE_ALL	Indicate the whole time of the period.	R
15:0	CAPTURE_HEIGHT	Indicate the time of high level.	R

18.4.2.57 Capture Value4(TCU_CAP_VALUE4,0x0F0)

	TCU_CAP_VALUE4																Base + 0x0F0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CAPTURE_ALL																CAPTURE_HEIGHT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CAPTURE_ALL	Indicate the whole time of the period.	R
15:0	CAPTURE_HEIGHT	Indicate the time of high level.	R

18.4.2.58 Capture Value5(TCU_CAP_VALUE5,0x0F4)

	TCU_CAP_VALUE5																Base + 0x0F4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CAPTURE_ALL																CAPTURE_HEIGHT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:16	CAPTURE_ALL	Indicate the whole time of the period.	R
15:0	CAPTURE_HEIGHT	Indicate the time of high level.	R

18.4.2.59 Capture Value6(TCU_CAP_VALUE6,0x0F8)

	TCAPV6																Base + 0x0F8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CAPTURE_ALL																CAPTURE_HEIGHT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CAPTURE_ALL	Indicate the whole time of the period.	R
15:0	CAPTURE_HEIGHT	Indicate the time of high level.	R

18.4.2.60 Capture Value7(TCU_CAP_VALUE7,0x0FC)

	TCU_CAP_VALUE7																Base + 0x0FC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CAPTURE_ALL																CAPTURE_HEIGHT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CAPTURE_ALL	Indicate the whole time of the period.	R
15:0	CAPTURE_HEIGHT	Indicate the time of high level.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.4.2.61 Filter Value0(TCU_FIL_VALUE0,0x1A0)

	TCU_FIL_VALUE0																Base + 0x1A0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						FIL_B										Reserved						FIL_A									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	FIL_B	Gpio1 filter counter value. Only when gpio1 pos > n*Tpclk, the gpio will be get	RW
15:10	Reserved	Writing has no effect, read as zero.	R
9:0	FIL_A	Gpio0 filter counter value. Only when gpio0 pos > n*Tpclk, the gpio will be get	RW

18.4.2.62 Filter Value1(TCU_FIL_VALUE1,0x1A4)

	TCU_FIL_VALUE1																Base + 0x1A4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						FIL_B										Reserved						FIL_A									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	FIL_B	Gpio1 filter counter value. Only when gpio1 pos > n*Tpclk, the gpio will be get	RW
15:10	Reserved	Writing has no effect, read as zero.	R
9:0	FIL_A	Gpio0 filter counter value. Only when gpio0 pos > n*Tpclk, the gpio will be get	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.4.2.63 Filter Value2(TCU_FIL_VALUE2,0x1A8)

	TCU_FIL_VALUE2																Base + 0x1A8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						FIL_B										Reserved						FIL_A									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	FIL_B	Gpio1 filter counter value. Only when gpio1 pos > n*Tpclk, the gpio will be get	RW
15:10	Reserved	Writing has no effect, read as zero.	R
9:0	FIL_A	Gpio0 filter counter value. Only when gpio0 pos > n*Tpclk, the gpio will be get	RW

18.4.2.64 Filter Value3(TCU_FIL_VALUE3,0x1AC)

	TCU_FIL_VALUE3																Base + 0x1AC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						FIL_B										Reserved						FIL_A									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	FIL_B	Gpio1 filter counter value. Only when gpio1 pos > n*Tpclk, the gpio will be get	RW
15:10	Reserved	Writing has no effect, read as zero.	R
9:0	FIL_A	Gpio0 filter counter value. Only when gpio0 pos > n*Tpclk, the gpio will be get	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.4.2.65 Filter Value4(TCU_FIL_VALUE4,0x1B0)

	TCU_FIL_VALUE4																Base + 0x1B0															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						FIL_B										Reserved						FIL_A									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	FIL_B	Gpio1 filter counter value. Only when gpio1 pos > n*Tpclk, the gpio will be get	RW
15:10	Reserved	Writing has no effect, read as zero.	R
9:0	FIL_A	Gpio0 filter counter value. Only when gpio0 pos > n*Tpclk, the gpio will be get	RW

18.4.2.66 Filter Value5(TCU_FIL_VALUE5,0x1B4)

	TCU_FIL_VALUE5																Base + 0x1B4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						FIL_B										Reserved						FIL_A									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	FIL_B	Gpio1 filter counter value. Only when gpio1 pos > n*Tpclk, the gpio will be get	RW
15:10	Reserved	Writing has no effect, read as zero.	R
9:0	FIL_A	Gpio0 filter counter value. Only when gpio0 pos > n*Tpclk, the gpio will be get	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.4.2.67 Filter Value6(TCU_FIL_VALUE6,0x1B8)

	TCU_FIL_VALUE6																Base + 0x1B8															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						FIL_B										Reserved						FIL_A									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	FIL_B	Gpio1 filter counter value. Only when gpio1 pos > n*Tpclk, the gpio will be get	RW
15:10	Reserved	Writing has no effect, read as zero.	R
9:0	FIL_A	Gpio0 filter counter value. Only when gpio0 pos > n*Tpclk, the gpio will be get	RW

18.4.2.68 Filter Value7(TCU_FIL_VALUE7,0x1BC)

	TCU_FIL_VALUE7																Base + 0x1BC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						FIL_B										Reserved						FIL_A									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	FIL_B	Gpio1 filter counter value. Only when gpio1 pos > n*Tpclk, the gpio will be get	RW
15:10	Reserved	Writing has no effect, read as zero.	R
9:0	FIL_A	Gpio0 filter counter value. Only when gpio0 pos > n*Tpclk, the gpio will be get	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.5 Operation

18.5.1 Operation in TCU1 Mode

18.5.1.1 general mode (example for ch0)

Step1: the value of FULL(use register 0x40) should be bigger than HALF(user register 0x44).

Step2: make sure the interrupt is open.(use register 0x38)

Step3: send a initial value for counter.(use register 0x48).

Step4: if use inner clock, choose the clock choose the prescale, choose CLK_POS/NEG_EN, choose count mode is 0~full.(use register 0x4c)

if use input clock, and if this clock is input by gpio0, choose GPIO0_EN, GPIO0_POS/NEG_EN, choose count mode is 0~full.(use register 0x4c)

Step5: enable TCU counter.(use register 0x14)

Ex:

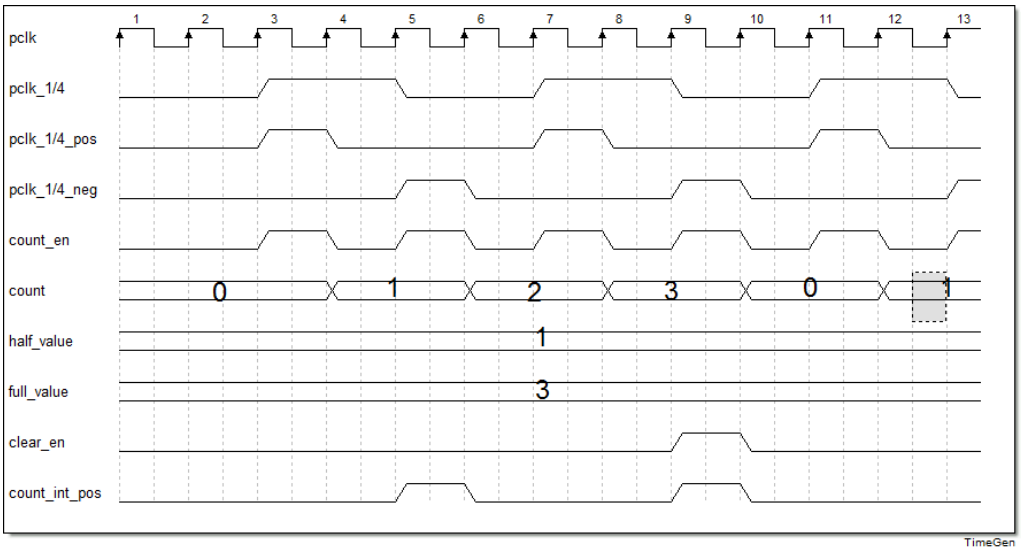
Step1:0x40(full) is 3 and 0x44(half) is 1.

Step2:0x38 bit0 and bit16(mask_clr) is 1

Step3:0x48(cnt_value) write 0

Step4:0x4c bit0 is 1(pclk_en), bit3 is 1(1/4), bit16,17 is 1(use double edge).

Step5:0x14 bit0 is 1(cnt_en).



18.5.1.2 gate mode(example for ch0)

Step1: set value of FULL(0x40) and HALF(0x44).

Step2: make sure the interrupt is open.(use register 0x38)

Step3: send a initial value for counter.(use register 0x48).

Step4: if use inner clock, choose the clock choose the prescale, choose CLK_POS/NEG_EN, choose count mode is 0~full.(use register 0x4c)

if use input clock, and if this clock is input by gpio0, choose GPIO0_EN, GPIO0_POS/NEG_EN, choose count mode is 0~full.(use register 0x4c)

Step5: if use gpio1 to control the gate, choose GPIO1_EN, choose GATE_SEL to 3.(use register

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

0x4c)

Step6: enable TCU counter.(use register 0x14)

Ex:

Step1:0x40(full) is 2 and 0x44(half) don't mind

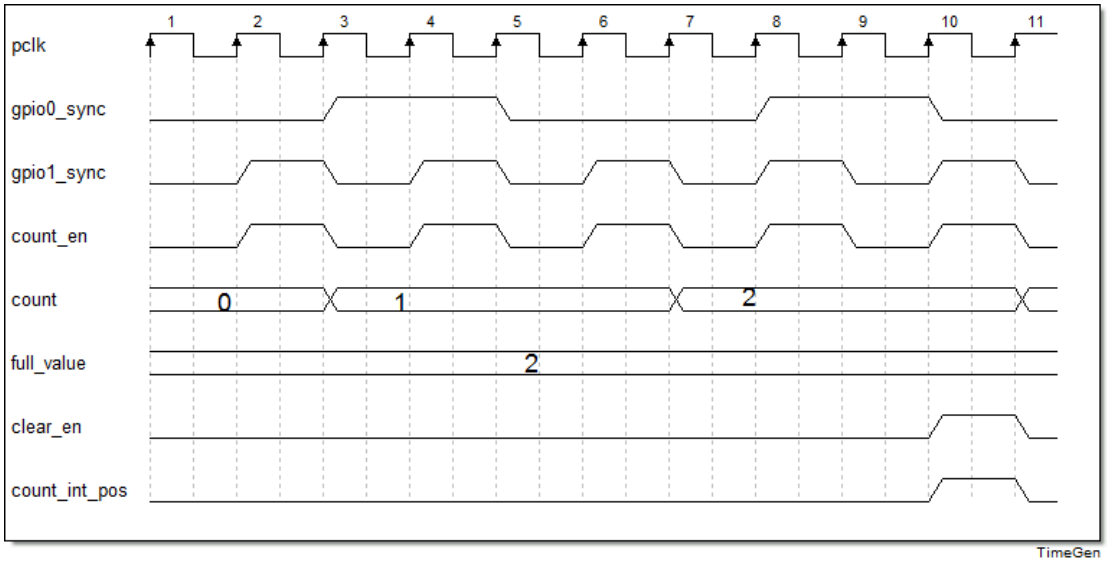
Step2:0x38 bit0(mask_clr) is 1

Step3:0x48(cnt_value) write 0

Step4:0x4c bit6,7(gpio0,1_en) is 1,, bit20(gpio0_pos) is 1.

Step5:0x4c bit[12:11](use gpio0 to be gate) is 2

Step6:0x14 bit0 is 1(cnt_en).



18.5.1.3 direction mode(example for ch0)

Step1: set value of FULL(0x40) and HALF(0x44).

Step2: make sure the interrupt is open.(use register 0x38)

Step3: send a initial value for counter.(use register 0x48).

Step4: if use inner clock, choose the clock choose the prescale, choose CLK_POS/NEG_EN, choose count mode for you want.(use register 0x4c)

if use input clock, and if this clock is input by gpio0, choose GPIO0_EN, GPIO0_POS/NEG_EN, choose count mode for you want.(use register 0x4c)

Step5: if use gpio1 to control the direction, choose GPIO1_EN, choose DIRECTION_SEL to 3.(use register 0x4c)

Step6: enable TCU counter.(use register 0x14)

Ex:

Step1:0x40(full) is 2 and 0x44(half) don't mind

Step2:0x38 bit0(mask_clr) is 1

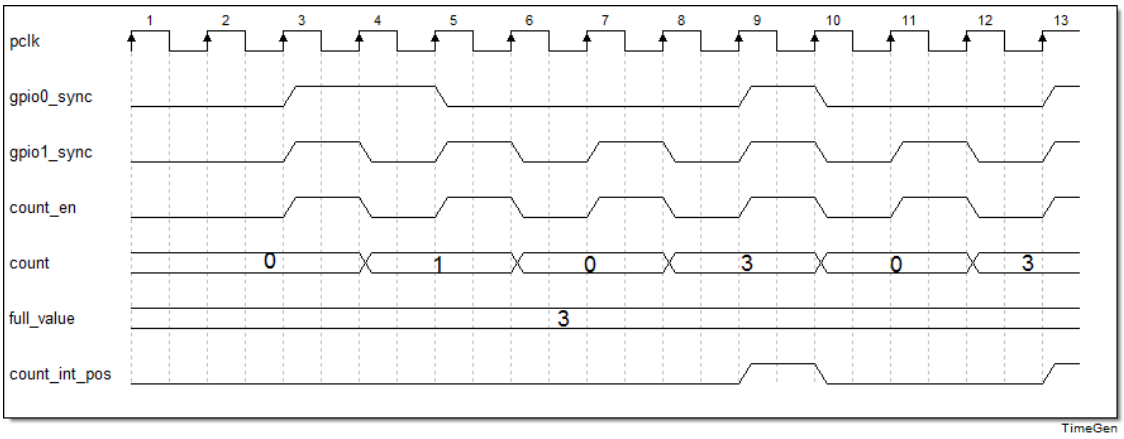
Step3:0x48(cnt_value) write 0

Step4:0x4c bit6,7(gpio0,1_en) is 1,, bit21(gpio0_pos) is 1.

Step5:0x4c bit[10:8](use gpio0 to be direction) is 2

Step6:0x14 bit0 is 1(cnt_en).

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.



18.5.1.4 quadrature mode(example for ch0)

Step1: set value of FULL(0x40) and HALF(0x44).

Step2: make sure the interrupt is open.(use register 0x38)

Step3: send a initial value for counter.(use register 0x48).

Step4: it must use inner clock, choose the clock choose the prescale, choose count mode for you want.(use register 0x4c)

Step5: it must use gpio0 and gpio1 to calculate the quadrature, so choose GPIO0_EN and GPIO1_EN.(use register 0x4c)

Step6: because of use quadrature mode, so if you want to get direction, you should choose DIRECTION_SEL to 4, if not , you will choose 1.(use register 0x4c)

Step7:you can use CLK_POS/NEG_EN or GPIO_POS/NEG_EN to sample the value of quadrature.(use register 0x4c)

Step8: enable TCU counter.(use register 0x14)

Ex:

Step1:0x40(full) is you choose and 0x44(half) is you choose

Step2:0x38 bit0 and bit16(mask_clr) is 1

Step3:0x48(cnt_value) write 0

Step4:0x4c bit6,7(gpio0,1_en) is 1,, bit18,19,20,21(gpio0_pos/neg,gpio1_pos_nge) is 1.

Step5:0x4c bit[10:8](use gpio0 to be direction) is 4

Step6:0x14 bit0 is 1(cnt_en).

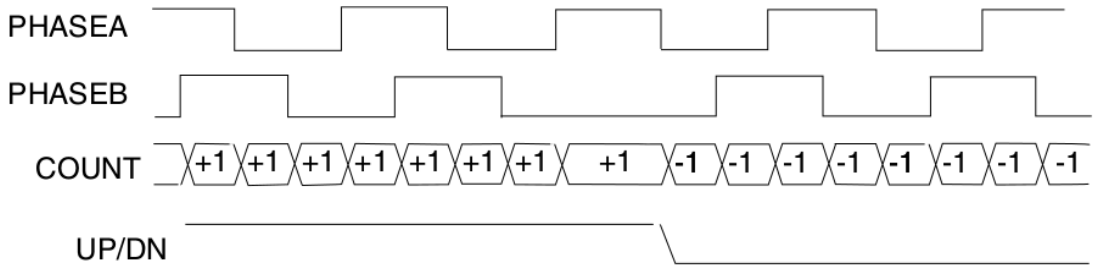


Figure 47-3. Quadrature Incremental Position Encoder

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

18.5.1.5 pos mode(example for ch0)

Step1: set value of FULL(0x40) and HALF(0x44).

Step2: make sure the interrupt is open.(use register 0x38)

Step3: send a initial value for counter.(use register 0x48).

Step4: if use inner clock, choose the clock choose the prescale, choose CLK_POS/NEG_EN, choose count mode is 0~full.(use register 0x4c)

if use input clock, and if this clock is input by gpio0, choose GPIO0_EN, GPIO0_POS/NEG_EN, choose count mode is 0~full.(use register 0x4c)

Step5: if use gpio1 to control the pos, choose GPIO1_EN.(use register 0x4c)

Step6: because of use pos mode, so choose CAPTURE_SEL to 2.(use register 0xc0)

Step7: enable TCU counter.(use register 0x14)

Ex:

Step1:0x40(full) is 3 and 0x44(half) don't mind

Step2:0x38 bit0(mask_clr) is 1

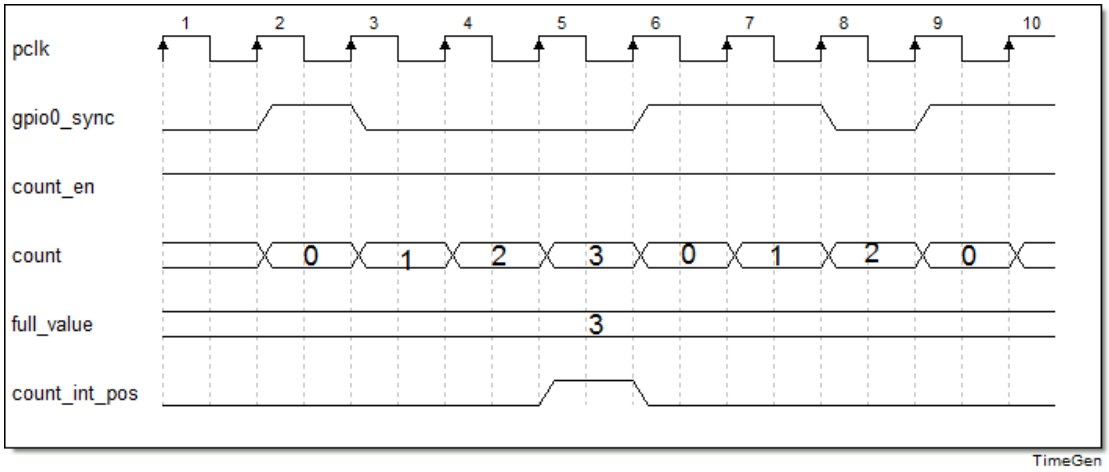
Step3:0x48(cnt_value) write 0

Step4:0x4c bit0(pclk_en) is 1,, bit16(clk_pos) is 1.

Step5:0x4c bit6(gpio0_en) is 1

Step6:0xc0 bit[16:18](gpio0_pos) is 1

Step6:0x14 bit0 is 1(cnt_en).



18.5.1.6 capture mode(example for ch0)

Step1: make sure the interrupt is open.(use register 0x38)

Step2: send a initial value for counter.(use register 0x48).

Step3: if wants to capture gpio1, choose GPIO1_EN.(use register 0x4c)

Step4: if wants to use exclk posedge, choose CLK_POSE_EN.(use register 0x4c)

Step5: because of use capture mode, so choose CAPTURE_SEL to 3.(use register 0xc0)

Step6: send the number you want to capture(if number bigger then 0x80 then the capture will not stop)(use register 0xc0).

Step7: if you want to close the capture mode, advice send capture number for 1.(use register 0xc0)

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

but it can send capture number for 0 also, but if send 0, this time of capture will stop.

Step8:capture mode not need counter enable. It will start counter when captrue number not 0.

18.5.1.7 filter function(example for ch0)

Note: the filter function is default not to open.

the function want to cut the gpio input that we want not.

this function can be open when ever you want.

Step1: Set the value for FIL(0x1a0) for gpio0 and gpio1, 0 means not to open.

Step2: Complete.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

19 Operating System Timer For Time Slice

19.1 Overview

This module has 1 channel: sys_ost32

- sys_ost32: 32-bit timer, used to generate operating system's time slice.
  - Has counter Full-match interrupt.
  - Count by an chip external clock(EXCLK), which can be divided by 1,4,16
  - Read by an asynchronous system clock.

19.2 Convention

Following conventions are convenient for memory mapped registers' description.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 0, write 1 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

19.3 Registers Mapping

Table 19-1 Registers Memory Map-Address Base

Name	Base	Description
CORE_OST$_n$	0x1210_0000+0x100*n	Address base of CORE_OST$_n$ (n=0, 1, 2...)

the maximum n equals the total hart number of an implementation of XBurst2 CPU.

Table 19-2 Registers Configuration

Name	Description	RW	Reset Value	Address offset	Access Size
OSTCCR	OS Timer Clock Control	RW	0x00000000	0x0000	32
OSTER	OS Timer Counter Enable	RW	0x00000000	0x0004	32
OSTCR	OS Timer clear	W	0x00000000	0x0008	32
OSTFR	OS Timer Flag	RWC	0x00000000	0x000C	32
OSTMR	OS Timer Mask	RW	0x00000001	0x0010	32
OSTDFR	OS Timer Data Full	RW	0xFFFFFFFF	0x0014	32
OSTCNT	OS Timer Counter	R	0x00000000	0x0018	32

19.3.1 Register and Fields Description

19.3.1.1 Timer Clock Control Register (OSTCCR,0x00)

	OSTCCR																Base + 0x00															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														PRESCALE	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1:0	PRESCALE	These bits select the OSTCNT count clock frequency. Don't change this field when the channel is running.	RW

Bit1	Bit 0	Description
0	0	Internal clock: CLK/1
0	1	Internal clock: CLK/4
1	0	Internal clock: CLK/16
1	1	Reserved

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

19.3.1.2 Timer Counter Enable Register (OSTER,0x04)

The OSTER is a 32-bit register. It contains the counter enable control bit.

	OSTER																													Base + 0x04
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															OSTEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	OSTEN	Enable the counter 0: disable counting up 1: enable counting up	RW

19.3.1.3 Timer Counter Clear Register (OSTCR,0x08)

The OSTCR is a 32-bit WRITE-ONLY register. It is used to clear the OSTCNT counter to 0.

	OSTCR																													Base + 0x08
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															OSTCLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	OSTCLR	Clear the counter. 0: Invalid 1: Set the OSTCNT counter to 0	W

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

19.3.1.4 Timer Flag Register (OSTFR,0x0C)

The OSTFR is a 32-bit register. It contains the comparison match flag.

.

	OSTFR																Base + 0x0C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															FFLAG
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	FFLAG	Comparison match flag. (OSTCNT == OSTDFR) 0: Comparison not match 1: Comparison match	RW C

19.3.1.5 Timer Mask Register (OSTMR,0x10)

The OSTMR is a 32-bit register. It is used to mask the interrupt caused by OSTCNT== OSTDFR.

	OSTMR																Base + 0x10															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															FMASK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	FMASK	Comparison match interrupt mask. 0: Comparison match interrupt should not be masked 1: Comparison match interrupt should be masked	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

19.3.1.6 Timer Data FULL Register (OSTDFR,0x14)

The comparison data FULL registers OSTDFR is a 32-bit register ,used to contain the maximum counter value to be compared with the content of the counter OSTCNT.

	OSTDFR																Base + 0x14															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSTDFR																															
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

19.3.1.7 Timer Counter (OSTCNT,0x18)

OSTCNT is a 32-bit READ-ONLY register. The up-counter OSTCNT can be reset to 0 by software and counts up using the pre-scale output clock. When OSTCNT reaches the value greater than or equal to OSTDFR, it will reset to 0 and then count-up again. The counter data can be read out at any time. The data can be clear by OSTCR.OSTCLR.

	OSTCNT																Base + 0x18															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSTCNT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

19.4 Operation

19.4.1 Basic Operation

1.Initialization

Writing OSTCCR.PRESCALE to set OSTCNT count clock frequency.

Writing OSTCR.OSTCLR to set the counter number to 0.

2.After initialize the register of timer, start the counter as follows:

Setting the OSTESR.OSTEN to 1 to enable the OSTCNT. Then it will begin to count up.

19.4.2 Stop Operation

Set 0 to the OSTER.OSTEN to disable the OSTCNT.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

19.4.3 Modify The PRE-SCALE

It's not permitted to modify the pre-scale when the counter is running. If you want to do so, you should

1st Setting the OSTER.OSTEN bit to 0 to disable the OSTCNT.

2nd Modify the pre-scale in OSTCCR

3rd Setting the OSTESR.OSTENS bit to 1 to enable the OSTCNT again.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

20 Operating System Timer For Time Elapsed

20.1 overview

This module has 1 channel: sys_ost64

- sys_ost64: 64-bit timer, used to generate operating system's elapsed time
  - Count by an chip external clock(EXCLK), which can be divided by 1,4,16
  - Read by an asynchronous system clock.

20.2 Convention

Following conventions are convenient for memory mapped registers' description.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 0, write 1 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

20.3 Registers Mapping

Table 20-1 Registers Memory Map-Address Base

Name	Base	Description
GLOBAL_OST	0x1200_0000 (valid range is 64KB)	Address base of GLOBAL_OST

Table 20-2 Registers Configuration

Name	Description	RW	Reset Value	Address offset	Access Size
OSTCCR	OS Timer Clock Control	RW	0x00000000	0x0000	32
OSTER	OS Timer Counter Enable	RW	0x00000000	0x0004	32
OSTCR	OS Timer Clear	W	0x00000000	0x0008	32
OSTCNTH	OS Timer Counter High	R	0x00000000	0x000C	32
OSTCNTL	OS Timer Counter Low	R	0x00000000	0x0010	32
OSTCNTB	OS Timer Counter Buffer	R	0x00000000	0x0014	32

20.3.1 Register and Fields Description

20.3.1.1 Timer Clock Control Register (OSTCCR,0x0000)

	OSTCCR																Base + 0x0000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														PRESCALE	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1:0	PRESCALE	These bits select the count clock frequency. Don't change this field when the channel is running.	RW

Bit1	Bit 0	Description
0	0	Internal clock: CLK/1
0	1	Internal clock: CLK/4
1	0	Internal clock: CLK/16
1	1	Reserved

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

20.3.1.2 Timer Counter Enable Register (OSTER,0x0004)

The OSTER is a 32-bit register. It contains the counter enable control bit.

	OSTER																													Base + 0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															OSTEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	OSTEN	Enable the counter 0: disable counting up 1: enable counting up	RW

20.3.1.3 Timer Counter Clear Register (OSTCR,0x0008)

The OSTCR is a 32-bit WRITE-ONLY register. It is used to clear the counter to 0.

	OSTCR																													Base + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															OSTCLR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	OSTCLR	Clear the counter. 0: Invalid 1: Set the counter to 0	W

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

20.3.1.4 Timer Counter (OSTCNTH, OSTCNTL)

The timer has a 64-bit READ-ONLY counter. OSTCNTH is the high 32-bit part and OSTCNTL is the low one. This up-counter can be enabled by software and counts up using the pre-scale output clock. When read OSTCNTL, the OSTCNTH is always stored in OSTCNTB, the software can then read OSTCNTB to get the total 64-bit number.

	OSTCNTH																Base + 0x000C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSTCNTH																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	OSTCNTL																Base + 0x0010															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSTCNTL																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

20.3.1.5 Timer Counter high 32 bits buffer (OSTCNTB,0x0014)

	OSTCNTB																Base + 0x0014															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OSTCNTB																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

20.4 Operation

20.4.1 Basic Operation

1.Initial the configuration.
Writing OSTCCR.PRESCALE to set {OSTCNTH, OSTCNTL} count clock frequency.
Writing OSTCR.OSTCLR to set the counter number to 0.

2.After initialize the register of timer, start the counter as follows:
Setting the OSTESR.OSTEN to 1 to enable the {OSTCNTH, OSTCNTL}. Then it will begin to count up.

20.4.2 Stop Operation

Set the OSTER.OSTEN 0 to disable the {OSTCNTH, OSTCNTL}.

20.4.3 Modify The PRE-SCALE

It's not permitted to modify the pre-scale when the counter is running. If you want to do so, you should

1st Setting the OSTER.OSTEN bit to 0 to disable the {OSTCNTH, OSTCNTL}.
2nd Modify the pre-scale in OSTCCR
3rd Setting the OSTESR.OSTENS bit to 1 to enable the {OSTCNTH, OSTCNTL} again.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

21 Interrupt Controller

21.1 Overview

This chapter describes the interrupt controller included in the XBurst Processor, explains its modes of operation, and defines its registers. The interrupt controller controls the interrupt sources available to the processor and contains the location of the interrupt source to allow software to determine source of all interrupts. It also determines whether an IRQ occurs or not and masks the interrupts.

Features:

- Total 64 interrupt sources
- INTC0, INTC1, INTC2, INTC3 for CPU core
- INTC4 for PDMA
- Each interrupt source can be independently enabled
- Priority mechanism to indicate highest priority interrupt
- INTC 4's Unmasked interrupts can wake up the chip in sleep mode

21.2 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

Table 21-1 Registers Memory Map-Address Base

Name	Base	Description
INTC0	0x12300000	Address base of INTC0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

INTC1	0x12301000	Address base of INTC1
INTC2	0x12302000	Address base of INTC2
INTC3	0x12303000	Address base of INTC3
INTC4	0x10001000	Address base of INTC4

Table 21-2 lists the registers of Interrupt Controller. All of these registers are 32bit, and each bit of the register represents or controls one interrupt source that list in Table 21-2.

Table 21-2 INTC Register

Name	Description	RW	Reset Value	Address offset	Access Size
ICSR0	IRQ Source Register	R	0x00000000	0x00	32
ICMR0	IRQ Mask Register	RW	0xFFFFFFFF	0x04	32
ICMSR0	IRQ Mask Set Register	W	0x????????	0x08	32
ICMCR0	IRQ Mask Clear Register	W	0x????????	0x0C	32
ICPR0	IRQ Pending Register	R	0x00000000	0x10	32
ICSR1	IRQ Source Register	R	0x00000000	0x20	32
ICMR1	IRQ Mask Register	RW	0xFFFFFFFF	0x24	32
ICMSR1	IRQ Mask Set Register	W	0x????????	0x28	32
ICMCR1	IRQ Mask Clear Register	W	0x????????	0x2C	32
ICPR1	IRQ Pending Register	R	0x00000000	0x30	32
DSR0	IRQ Source Register0 for PDMA	R	0x00000000	0x34	32
DMR0	IRQ Mask Register0 for PDMA	RW	0xFFFFFFFF	0x38	32
DPR0	IRQ Pending Register0 for PDMA	R	0x00000000	0x3C	32
DSR1	IRQ Source Register1 for PDMA	R	0x00000000	0x40	32
DMR1	IRQ Mask Register1 for PDMA	RW	0xFFFFFFFF	0x44	32
DPR1	IRQ Pending Register1 for PDMA	R	0x00000000	0x48	32

21.2.1 Interrupt Controller Source Register (ICSR0)

This register contains all the interrupts' status. A "1" indicates that the corresponding interrupt is pending . A "0" indicates that the interrupt is not pending now. The register is read only.

將 R35 電阻 short ,

	ICSR0																0x10001000													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	ROTATE	MIPI_CSI	TCU0	TCU1	TCU2	RSA	AES	HASH	Isp0	Isp1	Vic0	Vic1	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	Mipi_csi1	sadc	Mipi_dsi	SSI0	SSI1	SFC	pwm	PDMAM	PDMAD	PDMA	Reserved	USB-OTG	Audio
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits Of ICSR0	Description
0	The corresponding interrupt source is not pending.
1	The corresponding interrupt source is pending.

21.2.2 Interrupt Controller Source Register (ICSR1)

This register contains all the interrupts' status. A "1" indicates that the corresponding interrupt is pending . A "0" indicates that the interrupt is not pending now. The register is read only.

	ICSR1																														0x10001020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FELIX	HELIX	I2C0	I2C1	I2C2	I2C3	I2C4	I2C5	GMAC	EFUSE	GMAC1	DDR	CPM	HARB0	HARB2	MSC2	UART0	UART1	UART2	UART3	UART4	UART5	UART6	UART7	UART8	UART9	MSC0	MSC1	scc	dtrng	SOFT	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICSR1	Description
0	The corresponding interrupt source is not pending.
1	The corresponding interrupt source is pending.

21.2.3 Interrupt Controller Mask Register (ICMR0)

This register is used to mask the interrupt input sources and defines which active sources are allowed to generate interrupt requests to the processor. Its value can be changed either by writing ICMSR and ICMCR or by writing itself. The masked interrupts are invisible to the processor.

	ICMR0																														0x10001004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	ROTATE	MIPI_CSI	TCU0	TCU1	TCU2	Reserved	AES	HASH	OTG	Reserved	Reserved	Reserved	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	Reserved	Reserved	SSI0	SSI1	SFC	Reserved	PDMAM	PDMAD	PDMA	Reserved	Reserved	Audio
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits Of ICMR0	Description
0	The corresponding interrupt is not masked.
1	The corresponding interrupt is masked.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

21.2.4 Interrupt Controller Mask Register (ICMR1)

This register is used to mask the interrupt input sources and defines which active sources are allowed to generate interrupt requests to the processor. Its value can be changed either by writing ICMSR and ICMCR or by writing itself. The masked interrupts are invisible to the processor.

	ICMR1																														0x10001024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	JPEG	I2C0	I2C1	I2C2	I2C3	I2C4	I2C5	GMAC	EFUSE	Reserved	DDR	CPM	HARB0	HARB2	Reserved	UART0	UART1	UART2	UART3	UART4	UART5	DTRNG	Reserved	Reserved	SCC	MSC0	MSC1	Reserved	Reserved	SOFT	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICMR1	Description
0	The corresponding interrupt is not masked.
1	The corresponding interrupt is masked.

21.2.5 Interrupt Controller Mask Set Register (ICMSR0)

This register is used to set bits in the interrupt mask register. This register is write only.

	ICMSR0																														0x10001008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	ROTATE	MIPI_CSI	TCU0	TCU1	TCU2	Reserved	AES	HASH	OTG	Reserved	Reserved	Reserved	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	Reserved	Reserved	SSI0	SSI1	SFC	Reserved	PDMAM	PDMAD	PDMA	Reserved	Reserved	Audio
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICMSR0	Description
0	Ignore.
1	Will set the corresponding interrupt mask bit.

21.2.6 Interrupt Controller Mask Set Register (ICMSR1)

This register is used to set bits in the interrupt mask register. This register is write only.

	ICMSR1																														0x10001028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	JPEG	I2C0	I2C1	I2C2	I2C3	I2C4	I2C5	GMAC	EFUSE	Reserved	DDR	CPM	HARB0	HARB2	Reserved	UART0	UART1	UART2	UART3	UART4	UART5	DTRNG	Reserved	Reserved	SCC	MSC0	MSC1	Reserved	Reserved	SOFT	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits Of ICMSR1	Description
0	Ignore.
1	Will set the corresponding interrupt mask bit.

21.2.7 Interrupt Controller Mask Clear Register (ICMCR0)

This register is used to clear bits in the interrupt mask register. This register is write only.

	ICMCR0																0x1000100C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	ROTATE	MIPI_CSI	TCU0	TCU1	TCU2	Reserved	AES	HASH	OTG	Reserved	Reserved	Reserved	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	Reserved	Reserved	SSI0	SSI1	SFC	Reserved	PDMAM	PDMAD	PDMA	Reserved	Reserved	Audio
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICMCR0	Description
0	Ignore.
1	Will clear the corresponding interrupt mask bit.

21.2.8 Interrupt Controller Mask Clear Register (ICMCR1)

This register is used to clear bits in the interrupt mask register. This register is write only.

	ICMCR1																0x1000102C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	JPEG	I2C0	I2C1	I2C2	I2C3	I2C4	I2C5	GMAC	EFUSE	Reserved	DDR	CPM	HARB0	HARB2	Reserved	UART0	UART1	UART2	UART3	UART4	UART5	DTRNG	Reserved	Reserved	SCC	MSC0	MSC1	Reserved	Reserved	SOFT	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICMCR1	Description
0	Ignore.
1	Will clear the corresponding interrupt mask bit.

21.2.9 Interrupt Controller Pending Register (ICPR0)

This register contains the status of the interrupt sources after masking. This register is read only.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	ICPR0																0x10001010													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	ROTATE	MIPI_CSI	TCU0	TCU1	TCU2	Reserved	AES	HASH	OTG	Reserved	Reserved	Reserved	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	Reserved	Reserved	SSI0	SSI1	SFC	Reserved	PDMAM	PDMAD	PDMA	Reserved	Reserved	Audio
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICPR0	Description
0	The corresponding interrupt is not active or is masked.
1	The corresponding interrupt is active and is not masked to the processor.

21.2.10 Interrupt Controller Pending Register (ICPR1)

This register contains the status of the interrupt sources after masking. This register is read only.

	ICPR1																0x10001030													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	JPEG	I2C0	I2C1	I2C2	I2C3	I2C4	I2C5	GMAC	EFUSE	Reserved	DDR	CPM	HARB0	HARB2	Reserved	UART0	UART1	UART2	UART3	UART4	UART5	DTRNG	Reserved	Reserved	SCC	MSC0	MSC1	Reserved	Reserved	SOFT	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICPR1	Description
0	The corresponding interrupt is not active or is masked.
1	The corresponding interrupt is active and is not masked to the processor.

21.2.11 Interrupt Source Register0 for PDMA (DSR0)

This register contains status of all interrupts. A “1” indicates the corresponding interrupt is pending. The register is read only.

	DSR0																0x10001034													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	ROTATE	MIPI_CSI	TCU0	TCU1	TCU2	Reserved	AES	HASH	OTG	Reserved	Reserved	Reserved	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	Reserved	Reserved	SSI0	SSI1	SFC	Reserved	PDMAM	PDMAD	PDMA	Reserved	Reserved	Audio
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits Of DSR0	Description
0	The corresponding interrupt source is not pending.
1	The corresponding interrupt source is pending.

21.2.12 Interrupt Mask Register0 for PDMA (DMR0)

This register is used to mask the interrupt input sources and defines which active sources are allowed to generate interrupt requests to the processor. The masked interrupts are invisible to the processor.

	DMR0																0x10001038													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	ROTATE	MIPI_CSI	TCU0	TCU1	TCU2	Reserved	AES	HASH	OTG	Reserved	Reserved	Reserved	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	Reserved	Reserved	SSI0	SSI1	SFC	Reserved	PDMAM	PDMAD	PDMA	Reserved	Reserved	Audio
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of DMR0	Description
0	The corresponding interrupt source is not pending.
1	The corresponding interrupt source is pending.

21.2.13 Interrupt Pending Register0 for PDMA (DPR0)

This register contains the status of the interrupt sources after masking. This register is read only.

	DPR0																0x1000103C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCD	CIM	ROTATE	MIPI_CSI	TCU0	TCU1	TCU2	Reserved	AES	HASH	OTG	Reserved	Reserved	Reserved	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	Reserved	Reserved	SSI0	SSI1	SFC	Reserved	PDMAM	PDMAD	PDMA	Reserved	Reserved	Audio
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of ICPR0	Description
0	The corresponding interrupt is not active or is masked.
1	The corresponding interrupt is active and is not masked to the processor.

21.2.14 Interrupt Source Register1 to PDMA (DSR1)

This register contains status of all interrupts. A “1” indicates the corresponding interrupt is pending.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

The register is read only.

	DSR1																														0x10001040
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	JPEG	I2C0	I2C1	I2C2	I2C3	I2C4	I2C5	GMAC	EFUSE	Reserved	DDR	CPM	HARB0	HARB2	Reserved	UART0	UART1	UART2	UART3	UART4	UART5	DTRNG	Reserved	Reserved	SCC	MSC0	MSC1	Reserved	Reserved	SOFT	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of DSR1	Description
0	The corresponding interrupt source is not pending.
1	The corresponding interrupt source is pending.

21.2.15 Interrupt Mask Register1 for PDMA (DMR1)

This register is used to mask the interrupt input sources and defines which active sources are allowed to generate interrupt requests to the processor. The masked interrupts are invisible to the processor.

	DMR1																														0x10001044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	JPEG	I2C0	I2C1	I2C2	I2C3	I2C4	I2C5	GMAC	EFUSE	Reserved	DDR	CPM	HARB0	HARB2	Reserved	UART0	UART1	UART2	UART3	UART4	UART5	DTRNG	Reserved	Reserved	SCC	MSC0	MSC1	Reserved	Reserved	SOFT	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits Of DMR1	Description
0	The corresponding interrupt is not masked.
1	The corresponding interrupt is masked.

21.2.16 Interrupt Pending Register1 for PDMA (DPR1)

This register contains the status of the interrupt sources after masking. This register is read only.

	DPR1																														0x10001048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	JPEG	I2C0	I2C1	I2C2	I2C3	I2C4	I2C5	GMAC	EFUSE	Reserved	DDR	CPM	HARB0	HARB2	Reserved	UART0	UART1	UART2	UART3	UART4	UART5	DTRNG	Reserved	Reserved	SCC	MSC0	MSC1	Reserved	Reserved	SOFT	RTC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits Of ICPR0	Description
0	The corresponding interrupt is not active or is masked.
1	The corresponding interrupt is active and is not masked to the processor.

21.3 Software Considerations

The interrupt controller is reflecting the status of interrupts sources in the peripheral.

Software should perform the task - determine the interrupt source from in ICPRx. In this chip, pending interrupts have two levels in structure. Interrupting module in the system that contains more than one interrupt sources need software to determine how to service it by reading interrupt status registers within it.

In the interrupt handler, the serviced interrupt source needs to be cleared in the interrupting device. In order to make certain the cleared source request status has been reflected at the corresponding ICPRx bit, software should wait enough time before exiting interrupt state.

The procedure is described following:

1 Interrupt generated.
2 CPU query interrupt sources, saves the current environment and then goes to interrupt common service routine.
3 Get ICPRx.
4 Find the highest priority interrupt and vector it. (The software decides which one has the highest priority)
5 Mask the chosen interrupt by writing the register ICMSRx.
6 Enable the system interrupt to allow the interrupt nesting. (software decided)
7 Execute the interrupt handler and unmask it by writing the register ICMCRx when exit the handler.
8 CPU restores the saved environment and exits the interrupt state.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

22 Watchdog Timer

22.1 Overview

The watchdog timer is used to resume the processor whenever it is disturbed by malfunctions such as noise and system errors. The watchdog timer can generate the reset signal.

22.2 Features

- Generates WDT reset
- A 16-bit Data register and a 16-bit counter
- WDT has a half interrupt.(use flag 24bit, more information please refer to tcu_spec)
- Counter clock uses the input clock selected by software
  - only RTCCLK can be used as the clock for counter
  - The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software

22.3 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

22.3.1 Register Memory Map

Table 22-1 Registers Memory Map Base Address

Name	Base	Description
WDT	0x10002000	Address base of WDT

The WDT is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 22-2 WDT Registers Map

Name	RW	Reset Value	Address offset	Access Size
WDT_FULL	RW	0x0000_0000	0x00	16
WDT_ENABLE	RW	0x0000_0000	0x04	8
WDT_COUNT	R	0x0000_????	0x08	16
WDT_CONTROL	RW	0x0000_0000	0x0C	16

22.3.2 Register and Fields Description

22.3.3 Watchdog Timer Data Register (WDT_FULL,0x00)

The watchdog timer data register TDR is used to store the data to be compared with the content of the watchdog timer up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

	WDT_FULL																Base + 0x00															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	THR																TDR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

22.3.4 Watchdog Enable Register (WDT_ENABLE,0x04)

The TCER is an 8-bit read/write register. It contains the counter enable control bits for watchdog. It is initialized to 0x00 by any reset.

	WDT_ENABLE																Base + 0x04															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															TCEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect, read as zero.	R
0	TCEN	Counter enable control. 0: Timer stop 1: Timer running	RW

22.3.5 Watchdog Timer Counter (WDT_COUNT,0x08)

The watchdog timer counter (TCNT) is a 16-bit read/write counter. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDR, the comparison match signal will be generated and a WDT reset is generated. The data can be read out at any time. (Default: indeterminate)

	WDT_COUNT																Base + 0x08													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

22.3.6 Watchdog Control Register(WDT_CONTROL,0x0C)

The TCSR1 is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

	WDT_CONTROL																Base + 0x0C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					CLRZ	Reserved				PRESCALE			Reserved	RTC_EN	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:11	Reserved	Writing has no effect, read as zero.	R
10	CLRZ	Clear counter to 0. It is only used in TCU2 mode. Writing 1 to this bit will clear the counter to 0. When the counter is finished setting to 0, it will be cleared by hardware. Writing 0 to this bit will be ignored.	RW
9:6	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td>5:3</td><td>PRESCALE</td><td>These bits select the TCNT count clock frequency. Don’t change this field when the channel is running.
<table>
<tr><th>Bit 2</th><th>Bit1</th><th>Bit 0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal clock: CLK/1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal clock: CLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internal clock: CLK/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internal clock: CLK/64</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Internal clock: CLK/256</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Internal clock: CLK/1024</td></tr>
<tr><td colspan="3">110~111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>2</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>1</td><td>RTC_EN</td><td>Select RTCCLK as the timer clock input.
0: Disable 1: Enable</td><td>RW</td></tr>
<tr><td>0</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
</table>

NOTE: The input clock of timer and the PCLK should keep to the rules as follows:

Input clock of timer: IN_CLK	**Clock generated from the frequency divider (PRESCALE): DIV_CLK**
PCK_EN == 0, RTC_EN == 1 and EXT_EN == 0 (IN_CLK = RTCCLK)	$f_{DIV_CLK} < ½ f_{PCLK}$
PCK_EN == 0, RTC_EN == 0 and EXT_EN == 1 (IN_CLK = EXTAL)	$f_{DIV_CLK} < ½ f_{PCLK}$
PCK_EN == 1, RTC_EN == 0 and EXT_EN == 0 (IN_CLK = PCLK)	ANY

22.4 Watchdog Timer Function

Step1:use CLEARZ to clear the counter.(use register 0x0c)

Step2: send a initial value for counter.(use register 0x08)

Step3: it must use inner clock, choose the clock, and choose the prescale.(use register 0x0c)

Step6: enable WDT counter.(use register 0x04)

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

23 PDMA Controller

23.1 Overview

Programmable DMA controller (PDMAC) is dedicated to smartly transfer data between on-chip peripherals (MSC, AIC, UART, etc.), external memories, and memory-mapped external devices.

23.2 Features

- Support up to 32 independent DMA channels
- Descriptor or No-Descriptor Transfer mode compatible with previous JZ SOC
- A simple Xburst-1 CPU supports smart transfer mode controlled by programmable firmware
- Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
- Transfer number of data unit: 1 ~ 2^{24} - 1
- Independent source and destination port width: 8-bit, 16-bit, 32-bit
- Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
- An extra INTC IRQ can be bound to one programmable DMA channel

23.3 Block Diagram

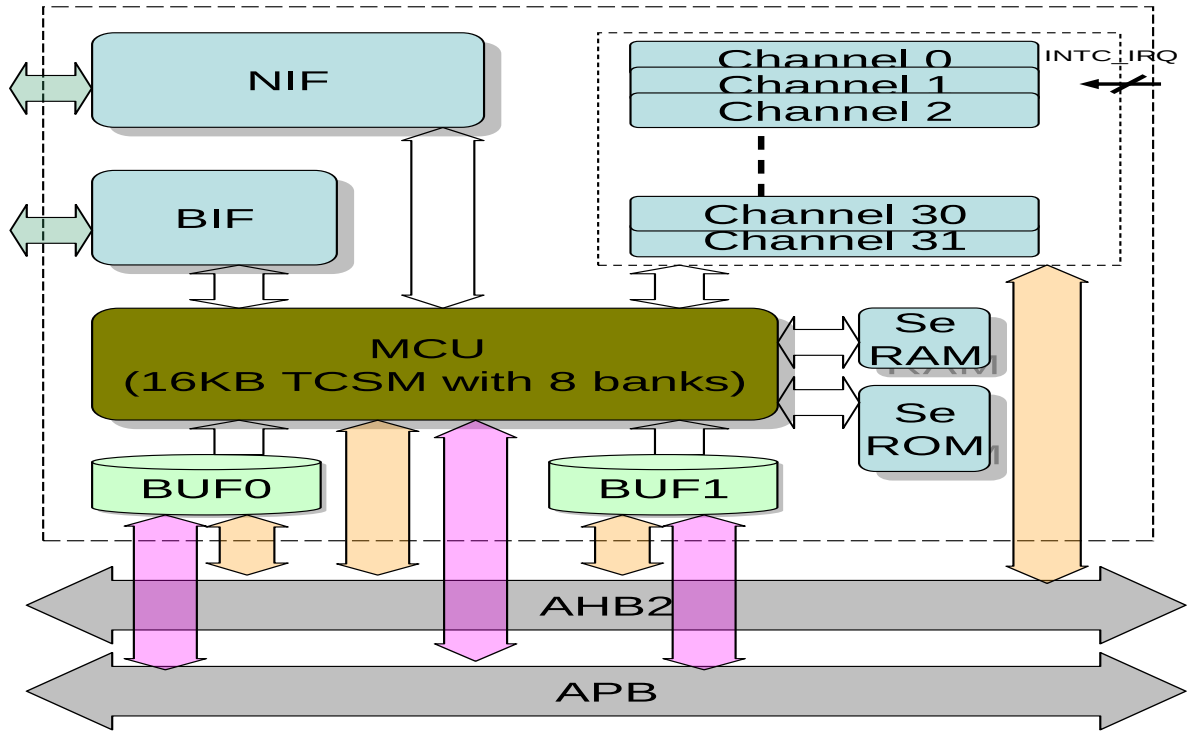


Figure 23-1 Block Diagram of PDMA

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

23.4 Memory Mapped Register Descriptions

23.4.1 DMA Channel Registers

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clears to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - Reset to 1
   0 - reset to 0
   ? - Value unknown after reset

Table 23-1 Registers Memory Map-Address Base

Name	Base	Description
Channel n	0x13420000 + n*0x20	PDMA channel n.

Table 23-2 DMA Channel Registers (n=0~31)

Name	Description	Reset Value	Address offset	Access Size (bit)
DSAn	Channel n Source Address	0x?	0x00 + n*0x20	32
DTAn	Channel n Target Address	0x?	0x04 + n*0x20	32
DTCn	Channel n Transfer Count	0x?	0x08 + n*0x20	32
DRTn	Channel n Request Source	0x?	0x0C + n*0x20	32
DCSn	Channel n Control/Status	0x?	0x10 + n*0x20	32
DCMn	Channel n Command	0x?	0x14 + n*0x20	32
DDAn	Channel n Descriptor Address	0x?	0x18 + n*0x20	32
DSDn	Channel n Stride Difference	0x?	0x1C + n*0x20	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

23.4.2 Global Control Registers

Table 23-3 Registers Memory Map-Address Base

Name	Base	Description
GCR	0x13420000	PDMA global control registers.

Table 23-4 Global Control Registers

Name	Description	Reset Value	Address offset	Access Size (bit)
DMAC	DMA Control	0x0	0x1000	32
DIRQP	DMA Interrupt Pending	0x0	0x1004	32
DDB	DMA Doorbell	0x0	0x1008	32
DDS	DMA Doorbell Set	0x0	0x100C	32
DIP	Descriptor Interrupt Pending	0x0	0x1010	32
DIC	Descriptor Interrupt Clear	0x0	0x1014	32
DMACP	DMA Channel Programmable	0x0	0x101C	32
DSIRQP	Channel soft IRQ to MCU	0x0	0x1020	32
DSIRQM	Channel soft IRQ mask	0xffffffff	0x1024	32
DCIRQP	Channel IRQ to MCU	0x0	0x1028	32
DCIRQM	Channel IRQ to MCU mask	0xffffffff	0x102C	32
DMCS	MCU Control and Status	0xe1	0x1030	32
DMNMB	MCU Normal Mailbox	0x0	0x1034	32
DMSMB	MCU Security Mailbox	0x0	0x1038	32
DMINT	MCU Interrupt	0x3	0x103C	32

NOTES:

Grey ones are obsolete registers defined in previous JZ SOC. They are relative to clock gating and have no real function, and they are not supported any longer.

23.5 DMA Channel Register Definition

23.5.1 DMA Source Address (DSAn, n = 0 ~ 31)

	DSAn																BASE + 0x0 + (n*0x20)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SA																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	SA	Source physical address.	RW

23.5.2 DMA Target Address (DTAn, n = 0 ~ 31)

	DTAn																BASE + 0x4 + (n*0x20)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TA																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	TA	Target physical address.	RW

23.5.3 DMA Transfer Count (DTCn, n = 0 ~ 31)

	DTCn																BASE + 0x8 + (n*0x20)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								TC																							
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:24	Reserved	Write has no effect, read as zero.	R
23:0	TC	TC records the number of data unit to be transferred. Moreover, when Stride transfer mode is enabled, TC composes of two parts: the lower 16 bits is the number of data unit for sub-block transfer, the higher 8 bits is the number of sub-block. TC automatically counts down to 0 at the end.	RW

23.5.4 DMA Request Types (DRTn, n = 0 ~ 31)

	DRTn																BASE + 0xC + (n*0x20)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										RT					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:6	Reserved	Write has no effect, read as zero.	R
5:0	RT	Transfer request type.	RW

Table 23-5 Transfer Request Types

RT5-0	Description
000000 ~ 000111	Reserved.
001000	Auto-request. (external address → external address)
001010	UART5 transmit-fifo-empty transfer request. (external address → UTHR)
001011	UART5 receive-fifo-full transfer request. (URBR → external address)
001100	UART4 transmit-fifo-empty transfer request. (external address → UTHR)
001101	UART4 receive-fifo-full transfer request. (URBR → external address)
001110	UART3 transmit-fifo-empty transfer request. (external address → UTHR)
001111	UART3 receive-fifo-full transfer request. (URBR → external address)
010000	UART2 transmit-fifo-empty transfer request. (external address → UTHR)
010001	UART2 receive-fifo-full transfer request. (URBR → external address)
010010	UART1 transmit-fifo-empty transfer request. (external address → UTHR)
010011	UART1 receive-fifo-full transfer request. (URBR → external address)
010100	UART0 transmit-fifo-empty transfer request. (external address → UTHR)
010101	UART0 receive-fifo-full transfer request. (URBR → external address)
010110	SSI0 transmit-fifo-empty transfer request.
010111	SSI0 receive-fifo-full transfer request.
011000	SSI1 transmit-fifo-empty transfer request.
011001	SSI1 receive-fifo-full transfer request.
100100	I2C0 transmit-fifo-empty transfer request.
100101	I2C0 receive-fifo-full transfer request.
100110	I2C1 transmit-fifo-empty transfer request.
100111	I2C 1 receive-fifo-full transfer request.
101000	I2C 2 transmit-fifo-empty transfer request.
101001	I2C 2 receive-fifo-full transfer request.
101010	I2C 3 transmit-fifo-empty transfer request.
101011	I2C 3 receive-fifo-full transfer request.
101100	I2C 4 transmit-fifo-empty transfer request.
101101	I2C 4 receive-fifo-full transfer request.
101110	I2C 5 transmit-fifo-empty transfer request.
101111	I2C 5 receive-fifo-full transfer request.
110000	UART6 transmit-fifo-empty transfer request. (external address → UTHR)
110001	UART6 receive-fifo-full transfer request. (URBR → external address)

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

110010	UART7 transmit-fifo-empty transfer request. (external address → UTHR)
110011	UART7 receive-fifo-full transfer request. (URBR → external address)
110100	UART8 transmit-fifo-empty transfer request. (external address → UTHR)
110101	UART8 receive-fifo-full transfer request. (URBR → external address)
110110	UART9 transmit-fifo-empty transfer request. (external address → UTHR)
110111	UART9 receive-fifo-full transfer request. (URBR → external address)
111000	SADC receive request
110001 ~ 111111	reserved

NOTES:

1 Only auto request can be concurrently set in all channels with different source and target add1ress.

2 For on-chip device DMA request, the corresponding source or target address that map to on-chip device must be set as fixed.

23.5.5 DMA Channel Control/Status (DCSn, n = 0 ~ 31)

	DCSn																BASE + 0x10 + (n*0x20)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NDES	DES8	TOC														CDOA											AR	TT	HLT	TOE	CTE
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	NDES	Descriptor or No-Descriptor Transfer Select. 0: Descriptor Transfer; 1: No-descriptor Transfer.	RW
30	DES8	Descriptor 8 Word. 0: 4-word descriptor; 1: 8-word descriptor.	RW
29:16	TOC	Time out counter. Available when TOE=1，undefined scratch field	RW
15:8	CDOA	Copy of offset address of last completed descriptor from that in DMA command register. (The field is Ignored in No-Descriptor Transfer)	RW
7:5	Reserved	Write has no effect, read as zero.	R
4	AR	Address Error. Hardware set it to 1 and software clear it to 0. 0: no address error; 1: address error occurred.	RW
3	TT	Transfer Terminate. 0: Descriptor or No-Descriptor DMA transfer does not end 1: No-Link Descriptor or No-Descriptor DMA transfer end	RW
2	HLT	DMA halt. Hardware sets it to 1 when an abnormal case occurs during transfer, then software has to clear it to 0 for re-using the channel later.	RW
1	TOE	Time out enable for transaction of a data unit. 0 – no time out monitor for a data unit's transfer	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1 – after a data unit has already been transferred but not completed yet, TOC field monitors the maximum cycles to be cost, and once exceeding the preset value occurs, a time-out error arises and HLT will be set 1 but TT keeps 0, moreover, if DCMn.TIE=1, a time-out interrupt arises.	
0	CTE	Channel transfer enable: 0: disable; 1: enable.	RW

NOTES:

1. For a working channel, when an address error occurs or an on-going transfer is stopped by software writing 0 to CTE, HLT becomes 1 but TT keeps 0 that denotes an abnormal situation occurs.
2. Software can stop any working channel at any time. However, after setting 0 to CTE, software must read TT, HLT and CTE to ensure the stop behavior has been done for the channel, that is,
   a) TT=0, HALT=0, CTE =1, not halt yet, need polling again
   b) TT=1, HALT=0, CTE=0, the channel just ends its work when software wants to stop it.
   c) TT=0, HALT=1, CTE=0, the channel has been stopped but its transfer not complete yet.

23.5.6 DMA Channel Command (DCMn, n = 0 ~ 31)

	DCMn																BASE + 0x14 + (n*0x20)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				SID		DID		SAI	DAI	Reserved		RDIL				SP		DP		Reserved		TSZ		Reserved					STDE	TIE	LINK
RST	0	0	0	0	0	0	0	0	?	?	0	0	?	?	?	?	?	?	?	?	0	?	?	?	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Reserved	Write has no effect, read as zero	R
27:26	SID	Source identification. Only be used for special channel 0/1. 0: Source is TCSM. 1: Source is BCH (for channel 0) / NEMC (for channel 1) 2: Source is DDR (for channel 1) / Reserved (for channel 0) 3: Reserved. Don't set this bit, keep as 0.	RW
25:24	DID	Destination identification. Only be used for special channel 0/1. 0: Destination is TCSM. 1: Destination is BCH (for channel 0) / NEMC (for channel 1) 2: Destination is DDR (for channel 1) / Reserved (for channel 0) 3: Reserved. Don't set this bit, keep as 0.	RW
23	SAI	Source Address Increment. 0: no increment; 1: increment.	RW
22	DAI	Destination Address Increment. 0: no increment; 1: increment.	RW
19:16	RDIL	Recommended data unit size (unit: byte) for triggering device's DMA request when TSZ is autonomy.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

15:14	SP	Source port width. 00: 32-bit; 01: 8-bit; 10: 16-bit; 11: reserved.	RW
13:12	DP	Destination port width. 00: 32-bit; 01: 8-bit; 10: 16-bit; 11: reserved.	RW
11	Reserved	Write has no effect, read as zero.	R
10:8	TSZ	Transfer Data Size of a data unit. 000: 32-bit; 001: 8-bit; 010: 16-bit; 011: 16-byte; 100: 32-byte; 101: 64-byte; 110: 128-byte; 111: autonomy;	RW
7:3	Reserved	Write has no effect, read as zero.	R
2	STDE	Stride Disable/Enable. 0: address stride disable; 1: address stride enable.	RW
1	TIE	Transfer Interrupt Enable (TIE). 0: disable interrupt; 1: enable interrupt when TT is set to 1.	RW
0	LINK	Descriptor Link Enable. 0: disable; 1: enable. (the field is ignored in No-Descriptor Transfer mode)	RW

NOTES:

SP and DP are only available for device FIFO or NEMC. But when transfer data between device and DDR memory, must set the port width of DDR side as the same as the device side; however, when both source and destination are in DDR memory, both SP and DP must be 32-bit by setting 0.

Table 23-6 Available RDIL

RDIL	Description
0	Reserved
1	Recommended data unit is 1 bytes
2	Recommended data unit is 2 bytes
3	Recommended data unit is 3 bytes
4	Recommended data unit is 4 bytes
5	Recommended data unit is 8 bytes
6	Recommended data unit is 16 bytes
7	Recommended data unit is 32 bytes
8	Recommended data unit is 64 bytes
9	Recommended data unit is 128 bytes
10~15	Reserved

NOTES:

1. if TSZ is autonomy, total bytes to be transferred equal the value of DCTn.TC (so maximum transfer bytes for autonomy are 16MB -1).
2. Programmer must care the detail of the FIFO of the device binding with relative DMA channel to set the correct and best recommended data unit value according to FIFO's data width and depth, refer to following table.

FIFO form	Best recommended RDIL
8x8bits	4 (half of total entries just accommodate 4 bytes)
8x16bits	5 (half of total entries just accommodate 8 bytes)
32x8bits	6 (half of total entries just accommodate 16 bytes)

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

16x16bits	6 (half of total entries just accommodate 16 bytes)
64x8bits	7 (half of total entries just accommodate 32 bytes)
64x32bits	9 (half of total entries just accommodate 128 bytes)
128x16bits	9 (half of total entries just accommodate 128 bytes)
128x32bits	9 (because maximum data unit is 128 bytes)

Moreover, programmer must be carefully obey following rules for correctness and best performance concern of DMA transfer:

1. ***auto-request, both source and destination device are DDR memory***. No alignment constraint for address, however, both source port width and destination port width must be set 32bit, and transferred bytes in a bus transaction denoted by TSZ (when TSZ !=7) must not be less than 4. Setting autonomy (TSZ=7) is the best choice for transfer efficiency[*0]
2. ***auto-request, both source and destination device are NEMC*****,** then
   a) if both source and destination port width are 8bit, no alignment constraint for address, setting autonomy (TSZ=7) is the best choice for transfer efficiency.
   b) If either source port or destination port width is not 8bit, must not set autonomy to TSZ. The relative source or destination address must be 2-byte (port width is 16bit) or 4-byte (port width is 32bit) aligned. Moreover, the byte number denoted by TSZ must not be less than the least common multiple of the byte number denoted by source port width and destination port width. Larger TSZ means better transfer efficiency.
3. ***auto-request, source device is NEMC while destination device is DDR memory*****,** then
   a) if source port width is 8bit. no alignment constraint for address, setting autonomy (TSZ=7) is the best choice for transfer efficiency.
   b) if source port width is 16bit, source address must be 2-byte aligned and TSZ must be the times of 2-byte (so must not set autonomy to TSZ); no alignment constraint for destination address, larger TSZ means better transfer efficiency.
   c) If source port width is 32bit, source address must be 4-byte aligned and TSZ must be the times of 4-byte (so must not set autonomy to TSZ); no alignment constraint for destination address, larger TSZ means better transfer efficiency.
4. ***auto-request, source device is DDR memory while destination device is NEMC***, then
   a) if destination port width is 8bit, no alignment constraint for address, setting autonomy (TSZ=7) is the best choice for transfer efficiency
   b) if destination port width is 16bit, destination address must be 2-byte aligned and TSZ must be the times of 2-byte (so must not set autonomy to TSZ); no alignment constraint for source address, larger TSZ means better transfer efficiency.
   c) If destination port width is 32bit, destination address must be 4-byte aligned and TSZ must be the times of 4-byte (so must not set autonomy to TSZ); no alignment constraint for source address, larger TSZ means better transfer efficiency.
5. ***external device fifo receive request, destination device is DDR memory***, then no alignment constraint for destination address, and
   a) if non-autonomy (TSZ !=7), for transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be times of 2-byte when source port width is 16bit or times of 4-byte when source port width is 32bit.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

b) If autonomy (TSZ=7), for transferred bytes in a bus transaction denoted by RDIL, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be times of 2-byte when source port width is 16bit or times of 4-byte when source port width is 32bit.

6. ***external device fifo receive request, destination device is NEMC***, then
   a) if destination port width is 8bit, no alignment constraint for destination address, and if non-autonomy (TSZ !=7), for transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be times of 2-byte when source port width is 16bit or times of 4-byte when source port width is 32bit. If autonomy (TSZ=7), for transferred bytes in a bus transaction denoted by RDIL, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be times of 2-byte when source port width is 16bit or times of 4-byte when source port width is 32bit.
   b) If destination port width is 16bit, must not set autonomy to TSZ and destination address must be 2-byte aligned. For transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must not be less than the least common multiple of the byte number denoted by source port width and destination port width.
   c) If destination port width is 32bit, must not set autonomy to TSZ and destination address must be 4-byte aligned. For transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must not be less than the least common multiple of the byte number denoted by source port width and destination port width.

7. ***external device fifo transmit request, source device is DDR memory***, then no alignment constraint for source address, and
   a) if destination port width is 8bit, setting autonomy (TSZ=7) is the best choice for transfer efficiency
   b) if destination port width is 16bit, when setting autonomy (TSZ=7), total transferred bytes must be the times of 2-byte, and for transferred bytes in a bus transaction denoted by RDIL, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be the times of 2-byte; when setting non-autonomy (TSZ!=7), for transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be the times of 2-byte.
   c) if destination port width is 32bit, when setting autonomy (TSZ=7), total transferred bytes must be the times of 4-byte, and for transferred bytes in a bus transaction denoted by RDIL, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be the times of 4-byte; when setting non-autonomy (TSZ!=7), for transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request[*1] meanwhile must be the times of 4-byte.

8. ***external device fifo transmit request, source device is NEMC***, then
   a) if source port width is 8bit, no alignment constraint for source address, and if non-autonomy (TSZ !=7), for transferred bytes in a bus transaction denoted by TSZ, it

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

must not exceed the critical value of triggering DMA request*1 meanwhile must be times of 2-byte when destination port width is 16bit or times of 4-byte when destination port width is 32bit.

If autonomy (TSZ=7), for transferred bytes in a bus transaction denoted by RDIL, it must not exceed the critical value of triggering DMA request*1 meanwhile must be times of 2-byte when destination port width is 16bit or times of 4-byte when destination port width is 32bit.

b) If source port width is 16bit, must not set autonomy to TSZ and source address must be 2-byte aligned. For transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request*1 meanwhile must not be less than the least common multiple of the byte number denoted by source port width and destination port width.

c) If source port width is 32bit, must not set autonomy to TSZ and source address must be 4-byte aligned. For transferred bytes in a bus transaction denoted by TSZ, it must not exceed the critical value of triggering DMA request*1 meanwhile must not be less than the least common multiple of the byte number denoted by source port width and destination port width.

NOTES:

*0 - when TSZ is not autonomy, total bytes to be transferred are bytes represented by TSZ * TC, and each bus transaction can only transfer bytes represented by TSZ, so larger data unit is better for transfer efficiency. But since in practical, in most cases, total bytes to be transferred are not the times of the best data unit, or source and/or destination address violates alignment, thus **setting autonomy for TSZ is recommended** when condition is ok.

*1 - Please refer to relative device's spec for detail information of how to set critical trigger value.

23.5.7 DMA Descriptor Address (DDAn, n = 0 ~ 31)

This register is ignored in No-Descriptor Transfer mode.

	DDAn																BASE + 0x18 + (n*0x20)													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBA																				DOA								Reserved			
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0

Bits	Name	Description	RW
31:12	DBA	Descriptor Base Address.	RW
11:4	DOA	Descriptor Offset Address.	RW
3:0	Reserved	Write has no effect, read as zero.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

23.5.8 DMA Stride Difference (DSDn, n = 0 ~ 31)

This register is ignored in No-Descriptor Transfer mode.

When address stride transfer mode is enabled in Descriptor mode, after a sub-block's transfer defined in DTCn completes, the source or target stride difference will be added to perform the new sub-block's start address, and the transfer will keep going until the transfer ends which means TC in DTCn reaches 0.

	DSDn																BASE + 0x1C + (n*0x20)															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSD																SSD															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:16	TSD	Target Stride Difference (next sub-block's start address – current sub-block's end address - 1), value range is -32768 ~ 32767	RW
15:0	SSD	Source Stride Difference (next sub-block's start address – current sub-block's end address - 1), value range is -32768 ~ 32767	RW

23.6 DMA Global Register Definition

23.6.1 DMA Control

	DMAC																BASE+0x1000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FMSC	FSSI	FTSSI	FUART	FAIC	Reserved					INTCC					INTCE	Reserved												HLT	AR	CH01	DMAE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	FMSC	0: 0.5-data/clk for MSC on APB;1: 1-data/clk for MSC on APB.	RW
30	FSSI	0: 0.5-data/clk for SSI on APB;1: 1-data/clk for SSI on APB.	RW
29	FTSSI	0: 0.5-data/clk for TSSI on APB;1: 1-data/clk for TSSI on APB.	RW
28	FUART	0: 0.5-data/clk for UART on APB;1: 1-data/clk for UART on APB.	RW
27	FAIC	0: 0.5-data/clk for AIC on APB;1: 1-data/clk for AIC on APB.	RW
21:17	INTCC	Which channel is bound with INTC_IRQ. Only available when INTCE is enabled	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

16	INTCE	Permit INTC_IRQ to be bound to one of programmable channel. 0, INTC_IRQ is ignored; 1, INTC_IRQ is bound to channel n, n equals to INTCC.	RW
15:4	Reserve	Write has no effect, read as zero.	R
3	HLT	Global halt status, halt occurs in any channel, the bit should be set to 1 by hardware and cleared to 0 by software. 0: no halt occurred 1: halt occurred in one or more channels	RW
2	AR	Global address error status, address error occurs in any channel, the bit should be set to 1 by hardware and cleared to 0 by software. 0: no address error occurred 1: address error occurred	RW
1	CH01	Special channel 0 and channel 1 enable. 1 –enable 0 – disable. Don't set this bit, keep as 0.	RW
0	DMAE	Global DMA enable. 0: disable DMA 1: enable DMA	RW

NOTES:

1. any of FMSC/FSSI/FTSSI/FUART/FAIC has been set，the corresponding DMA transfer on APB for MSC(MSC1, MSC2), SSI(SSI1), UART0~4, AIC will be in fast mode.
2. DMAE is a global switch, so software must be careful to toggle it from 0 to 1 or 1 to 0. It is **UNPREDICTABLE** to set 0 to DMAE abruptly when some channels are still working.
3. For more detail of CH01, refer to later chapter of special channel 0 and channel 1

23.6.2 DMA Interrupt Pending (DIRQP)

	DIRQP																BASE+0x1004													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ31	IRQ30	IRQ29	IRQ28	IRQ27	IRQ26	IRQ25	IRQ24	IRQ23	IRQ22	IRQ21	IRQ20	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	IRQn	IRQn denotes pending IRQ to main CPU for corresponding channel. 0: normal DMA transfer is in-progress or the channel is idle 1: an address error occurs (only available for UARTn) or normal DMA transfer done; moreover, if the relative channel is programmable, MCU can only set 1 to it. Hardware can only set 1 to it and main CPU can only set 0 to it.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

23.6.3 DMA Doorbell (DDB)

	DDB																BASE+0x 1008													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDB31	DDB30	DDB29	DDB28	DDB27	DDB26	DDB25	DDB24	DDB23	DDB22	DDB21	DDB20	DDB19	DDB18	DDB17	DDB16	DDB15	DDB14	DDB13	DDB12	DDB11	DDB10	DDB9	DDB8	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DDBn	DMA Doorbell. Software sets it to 1 and hardware clears it to 0. 0: disable DMA controller to fetch the first descriptor or DMA controller clears it to 0 as soon as it starts to fetch the descriptor 1: Writing 1 to DDS will set the corresponding DDBn bit to 1 and enable DMA controller to fetch the first descriptor For example, write 0x00000001 to DDS, DDB0 bit is set to 1 and enable DMA channel 0 to fetch its first descriptor. Write 0 to DDS, no meaning.	RWS

23.6.4 DMA Doorbell Set (DDS)

	DDS																BASE+0x 100C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DDS31	DDS30	DDS29	DDS28	DDS27	DDS26	DDS25	DDS24	DDS23	DDS22	DDS21	DDS20	DDS19	DDS18	DDS17	DDS16	DDS15	DDS14	DDS13	DDS12	DDS11	DDS10	DDS9	DDS8	DDS7	DDS6	DDS5	DDS4	DDS3	DDS2	DDS1	DDS0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DDSn	DMA Doorbell Set for each channel. Read as zero, and when write: 0: ignore 1: Set the corresponding DDBn bit to 1	W

23.6.5 Descriptor Interrupt Pending (DIP)

	DIP																BASE+0x 1010													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIP31	DIP30	DIP29	DIP28	DIP27	DIP26	DIP25	DIP24	DIP23	DIP22	DIP21	DIP20	DIP19	DIP18	DIP17	DIP16	DIP15	DIP14	DIP13	DIP12	DIP11	DIP10	DIP9	DIP8	DIP7	DIP6	DIP5	DIP4	DIP3	DIP2	DIP1	DIP0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	DIPn	Descriptor interrupt pending. If any of the descriptor, except the last one, set TIE, the corresponding bit of this register shall set after the very descriptor finished. This function provide more flexible method to be aware of the process of the long descriptor links. 0: No descriptor interrupt pending 1: The corresponding bit channel has completed a descriptor with TIE Read only for software..	R

23.6.6 Descriptor Interrupt Clear (DIC)

	DIC																BASE+0x 1014													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIC31	DIC30	DIC29	DIC28	DIC27	DIC26	DIC25	DIC24	DIC23	DIC22	DIC21	DIC20	DIC19	DIC18	DIC17	DIC16	DIC15	DIC14	DIC13	DIC12	DIC11	DIC10	DIC9	DIC8	DIC7	DIC6	DIC5	DIC4	DIC3	DIC2	DIC1	DIC0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DICn	Descriptor interrupt pending clear. 1: ignore 0: Clear the corresponding DIPn bit Only write 1 for software, read has no effect.	W1

23.6.7 DMA Channel Programmable (DMACP)

	DMACP																BASE+0x 101C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCP31	DCP30	DCP29	DCP28	DCP27	DCP26	DCP25	DCP24	DCP23	DCP22	DCP21	DCP20	DCP19	DCP18	DCP17	DCP16	DCP15	DCP14	DCP13	DCP12	DCP11	DCP10	DCP9	DCP8	DCP7	DCP6	DCP5	DCP4	DCP3	DCP2	DCP1	DCP0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DCPn	Channel programmable enable. 0, compatible with previous JZ SOC; 1, firmware controlled channel	RW

23.6.8 DMA Soft IRQ Pending (DSIRQP)

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	DSIRQP																														BASE+0x 1020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SIRQ31	SIRQ30	SIRQ29	SIRQ28	SIRQ27	SIRQ26	SIRQ25	SIRQ24	SIRQ23	SIRQ22	SIRQ21	SIRQ20	SIRQ19	SIRQ18	SIRQ17	SIRQ16	SIRQ15	SIRQ14	SIRQ13	SIRQ12	SIRQ11	SIRQ10	SIRQ9	SIRQ8	SIRQ7	SIRQ6	SIRQ5	SIRQ4	SIRQ3	SIRQ2	SIRQ1	SIRQ0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	SIRQn	Soft IRQ to MCU. Set any bit of this register to 1, if not masked correspond with that in DSIRQM, will issue a software interrupt to MCU. Note that the register is read-only for other masters but is entirely controlled (R/W) by the MCU of PDMA	R

23.6.9 DMA Soft IRQ Mask (DSIRQM)

	DSIRQM																														BASE+0x 1024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SIRQM31	SIRQM30	SIRQM29	SIRQM28	SIRQM27	SIRQM26	SIRQM25	SIRQM24	SIRQM23	SIRQM22	SIRQM21	SIRQM20	SIRQM19	SIRQM18	SIRQM17	SIRQM16	SIRQM15	SIRQM14	SIRQM13	SIRQM12	SIRQM11	SIRQM10	SIRQM9	SIRQM8	SIRQM7	SIRQM6	SIRQM5	SIRQM4	SIRQM3	SIRQM2	SIRQM1	SIRQM0
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:0	SIRQMn	Soft IRQ mask. 0, not mask corresponding DSIRQP soft IRQ; 1, mask corresponding DSIRQP soft IRQ Note that the register is read-only for other masters but is entirely controlled (R/W) by the MCU of PDMA	R

23.6.10 DMA Channel IRQ Pending to MCU (DCIRQP)

	DCIRQP																														BASE+0x 1028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CIRQ31	CIRQ30	CIRQ29	CIRQ28	CIRQ27	CIRQ26	CIRQ25	CIRQ24	CIRQ23	CIRQ22	CIRQ21	CIRQ20	CIRQ19	CIRQ18	CIRQ17	CIRQ16	CIRQ15	CIRQ14	CIRQ13	CIRQ12	CIRQ11	CIRQ10	CIRQ9	CIRQ8	CIRQ7	CIRQ6	CIRQ5	CIRQ4	CIRQ3	CIRQ2	CIRQ1	CIRQ0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	CIRQn	Channel IRQ Pending to MCU. The register is read-only 0, no channel IRQ to MCU; 1, pending channel IRQ to MCU When channel n is not programmable, the CIRQn is ignored by hardware. When channel n is programmable and DCMn.TIE is active 1, DIRQP.IRQn can not be set automatically any more after address error occurs or TT becomes active 1, instead, if DCIRQMn==0, CIRQn may be set 1 immediately to raise an IRQ to MCU. Moreover, when an channel m with above attribute is bound with the INTC_IRQ, if DCIRQMm==0, an active INTC_IRQ request will trigger an active CIRQn immediately	R

23.6.11 DMA Channel IRQ to MCU Mask (DCIRQM)

	DCIRQM																BASE+0x 102C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CIRQM31	CIRQM30	CIRQM29	CIRQM28	CIRQM27	CIRQM26	CIRQM25	CIRQM24	CIRQM23	CIRQM22	CIRQM21	CIRQM20	CIRQM19	CIRQM18	CIRQM17	CIRQM16	CIRQM15	CIRQM14	CIRQM13	CIRQM12	CIRQM11	CIRQM10	CIRQM9	CIRQM8	CIRQM7	CIRQM6	CIRQM5	CIRQM4	CIRQM3	CIRQM2	CIRQM1	CIRQM0
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:0	CIRQMn	Mask of Channel IRQ to MCU. The register is read-only for other master but is entirely controlled (R/W) by the MCU of PDMA 0, not mask corresponding channel's IRQ to MCU; 1, mask corresponding channel's IRQ to MCU When channel n is not programmable, the CIRQMn is ignored by hardware. When channel n is programmable and DCMn.TIE is active 1, CIRQMn can mask corresponding channel's IRQ to MCU.	R

23.6.12 Programmable Channel Bound With INTC_IRQ

In this SOC, all peripheral IRQs originally being issued to main CPU now can be taken over by PDMA through binding special INTC_IRQ to one of programmable channel. Note that INTC_IRQ from INTC may be different to normal IRQ of INTC to main CPU, please refer to the spec of INTC for detail of how to configure INTC_IRQ sources. In practical, maybe it is a better tradeoff to let MCU of PDMA take over trivial transactions of some devices from main CPU.

23.6.13 Special Channel 0 and Channel 1

When a product integrating this SOC need use raw NAND chipset properly through PDMA, the only method is setting special channel 0 and 1, following key bit fields must be preset:

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

1. DMAC.CH01 must be set 1
2. DCM0.TIE and DCM1.TIE must be set 1
3. DCM0.LINK and DCM1.LINK must be set 0
4. DCS0.NDES and DCS1.NDES must be set 1
5. DCM0.STDE and DCM1.STDE must be set 0
6. DCM0.SAI and DCM0.DAI must be set 1
7. DCM1.SAI and DCM1.DAI must be set 1
8. DCM0.SP and DCM0.DP must be set 0
9. DCM1.SP and DCM1.DP must be set 0
10. DCM0.TSZ and DCM1.TSZ must be set 7
11. DMACP.DCP0 and DMACP.DCP1 must be set 1 after relative firmware has been prepared.

23.7 MCU

MCU in PDMA is a mini CPU compatible with XBurst-1 ISA without implementing CACHE, MMU, DEBUG, FPU and MXU. It is very similar as the AUX in VPU but has different memory mapped control and status register.

23.7.1 MCU Control & Status

	DMCS																BASE+0x 1030													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SLEEP	SCMD	Reserved						SC _OFF																BCH			BTB_INV	SC_CALL			SW_RST
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1

Bits	Name	Description	RW
31	SLEEP	Sleep status of MCU. Read only by main CPU.	R
30	SCMD	Security Mode. Read only by main CPU.	R
29:24	reserved	Write has no effect, read as zero.	R
23:8	SC_OFF	Set the offset of the caller's data structure for SC_CALL	RW
7	BCH_DB	Block syndrome of BCH decoding, low level active	R
6	BCH_DF	BCH decoding finished, low level active	R
5	BCH_EF	BCH encoding finished, low level active	R
4	BTB_INV	Writing 1 invalidates BTB in MCU. Writing 0 has no effect, read as zero.	W
3	SC_CALL	Security Call. Writing 1 triggers a security exception which directs MCU to run security code located in the on-chip security ROM., read as zero.	W
2:1	reserved	Write has no effect, read as zero.	R
0	SW_RST	Software reset. 1, MCU keeps at reset state; 0, do not soft-reset MCU any more	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

NOTES:

BCH_DB, BCH_DF and BCH_EF are only available when special channel 0 and channel 1 is used for implementing storage of raw NAND chipsets. Please refer to BCH spec for detail.

23.7.2 MCU Normal MailBox

	DMNMB																BASE+0x 1034															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MB																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	MB	Contents of Normal Mailbox. Writing any value to the register will trigger a normal mailbox IRQ to main CPU when relative MASK field in DMINT is not set	RW

23.7.3 MCU Security MailBox

	DMSMB																BASE+0x 1038															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MB																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	MB	Contents of Security Mailbox. Writing any value to the register will trigger a security mailbox IRQ to main CPU when relative MASK field in DMINT is not set. Note that writing the register is inhibited by HW when DMCS.SCMD == 0	RW

23.7.4 MCU Interrupt

	DMINT																BASE+0x 103C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														S_IP	N_IP	Reserved														S_IMSK	N_IMSK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:18	Reserved	Write has no effect, read as zero.	R
17	S_IP	Security Mailbox IRQ pending. 1-pending IRQ. Hardware only set 1 by writing DMSMB when DMCS.SCMD == 1. Can be clear to 0 in any mode.	RW
16	N_IP	Normal Mailbox IRQ pending. 1-pending IRQ. Hardware only set 1 by writing DMNMB. Can be clear to 0 in any mode.	RW
15:2	Reserved	Write has no effect, read as zero.	R
1	S_IMSK	Security Mailbox IRQ mask. 1-mask; 0-not mask Can only be modified in security mode.	RW
0	N_IMSK	Normal Mailbox IRQ mask. 1-mask; 0-not mask	RW

23.7.5 Multiple Bank Tightly Coupled Sharing Memory

In MCU, there is a Tightly Coupled Sharing Memory (TCSM) with 32KB size and total 8 banks. Multiple- bank TCSM permits several masters accessing different banks in parallel. TCSM works at the same speed as MCU and both instruction fetch and data read/write to TCSM by MCU can be performed in one cycle.

BANK0~BANK1 can be configured with "Deep Sleep" mode, all the data read out are "0" during this mode, When out of "Deep Sleep" mode, the data in ram can recover.. BANK4~BANK7 can also be configured with "Shutdown" mode, but BANK0~BANK3 can not, all the data read out are "0" during this mode. The data is still "0" when out of "Shutdown" mode, which means the data has lost and can not be recovered. Please reference "CPM spec" about how to configure "Deep Sleep" and "Shutdown".

Table 23-7 TCSM space

	VA (only available for MCU)	PA (not remapped)	PA (remapped)
BANK0	F4000000h ~ F4000FFFh	13422000h ~ 13422FFFh	F3422000h ~ F3422FFFh
BANK1	F4001000h ~ F4001FFFh	13423000h ~ 13423FFFh	F3423000h ~ F3423FFFh
BANK2	F4002000h ~ F4002FFFh	13424000h ~ 13424FFFh	F3424000h ~ F3424FFFh
BANK3	F4003000h ~ F4003FFFh	13425000h ~ 13425FFFh	F3425000h ~ F3425FFFh
BANK4	F4004000h ~ F4004FFFh	13426000h ~ 13426FFFh	F3426000h ~ F3426FFFh
BANK5	F4005000h ~ F4005FFFh	13427000h ~ 13427FFFh	F3427000h ~ F3427FFFh
BANK6	F4006000h ~ F4006FFFh	13428000h ~ 13428FFFh	F3428000h ~ F3428FFFh
BANK7	F4007000h ~ F4007FFFh	13429000h ~ 13429FFFh	F3429000h ~ F3429FFFh

23.7.6 CP0 Registers of MCU

Available CP0 registers of MCU are not entirely compatible with MIPS PRA spec, they are listed below.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

CP0 Name (number)	Description	*sIt*
STATUS (12)	Bit 31~27:: reserved, read as zero Bit26: readable; only 1 can bet written into*1 Bit25: readable; only 1 can bet written into*1 Bit24: only being active during running Security Call routine *2 Bit2: ERL, Bit1: EXL, Bit0: IE	*0*
INTCTL (12)	Bit31~3: reserved, read as zero; Bit2: IRQ pending of soft IRQ to MCU; Bit1: IRQ pending of channel IRQ to MCU; Bit0: IRQ pending of INTC_IRQ Note that the register is read-only by MCU	*1*
CAUSE (13)	Bit31:BD， whether the interrupted PC is located in branch delay slot Bit30 ~ 0: reserved, read as zero	*0*
SeCAUSE (13)	Bit31:BD, similar as CAUSE, but being active when an IRQ interrupted a running Security Call routine. Bit30 ~ 0: reserved, read as zero	*1*
EPC (14)	IRQ Exception program counter	*0*
SePC (24)	Security Exception program counter	*0*
ErrorPC (30)	*Reset exception program counter*	*0*

NOTE:
*1 : once value 1 is set, only chip reset signal can clear it to 0.
*2 : STATUS.Bit24 is hard wired outside of PDMA.

23.7.7 Normal Exceptions Accepted by MCU

There are two kinds of normal exceptions that can be accepted by MCU: RESET and IRQ.
Note that RESET exception has the handler entry: 0xF4000000, while IRQ has another one: 0xF4000100.
Once the MCU accepts a normal exception, according to the definition of XBurst-1 Programming Manual, current interrupted PC will be pushed into CP0.EPC or CP0.ErrPC, and further CP0.STATUS.ERL or CP0.SATUS.EXL will be automatically set 1. Firmware can take use of MTC0/MFC0 to access these three CP0 registers: EPC, ErrPC and STATUS. Firmware must use ERET instruction to return to the interrupted locale to resume executing.

23.7.8 How to Boot MCU Up

After power-on reset, MCU keeps at reset state due to DMCS.SW_RST==1. To boot MCU up, first of all, RESET exception handler must be loaded into TCSM at the physical address range beginning from 0x13422000 or 0xF3422000 for remapped case. Programmer can use main CPU or some Non-programmable DMA channel to finish this loading work. Then clear DMCS.SW_RST to 0 by main CPU so that MCU can acknowledge a RESET exception, now MCU begins to run from the PC

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

0xF4000000. Following is a simple example.

1. Prepare a simple RESET exception handler, total 3 instructions:

   1: WAIT //sleep

   B 1b //endless loop

   NOP //delay slot

2. Load the handler into TCSM at the physical address range beginning from 0x13422000 or 0xF3422000 for remapped case.
3. Clear DMCS.SW_RST to 0 by main CPU

Now MCU will execute WAIT instruction and then enter sleep state

23.7.9 Security features

In additional to the above security used registers, several security objects and functions, such as security ROM, RAM and security call, are added to PDMA and its MCU, to compose the JZ4780 security engine. For the details, please reference to security engine section.

23.8 DMA manipulation

23.8.1 Descriptor Transfer Mode

23.8.1.1 Non-Stride (1-Dimensional) Transfer Mode

To do proper Descriptor DMA transfer in a channel, do following steps:

1 Check whether the status of DMA controller is available, that is, for global control (DMAC), ensure that DMAC.AR=0 and DMAC.HLT=0; and then for expected channel n, ensure that DCSn.AR=0, DCSn.HLT=0, DCSn.TT=0, DTCn=0.

2 guarantee DCSn.NDES=0, and select 4 word or 8 word descriptor by DCSn.DES8.

3 Build descriptor in memory. Write the first descriptor's address in DDAn and the address must be 16Bytes aligned for 4word descriptor and 32Bytes aligned for 8word descriptor, otherwise, the hardware behavior later is **UNPREDICTABLE**. The address includes two parts: Base and Offset address. If the descriptor is linked, the 32-bit address of next descriptor is composed of 20-bit Base address in DDAn and 8-bit Offset address in DESn.CDOA. See Table 23-8 Descriptor Structure for the detailed descriptor structure.

4 Don't update DRTn manually by software, instead, hardware will manage the request type of descriptor's transfer automatically.

5 Set 1 to the corresponding bit in DDB to initiate descriptor fetch.

6 Set DMAC.DMAE=1 and expected DCSn.CTE=1 to activate channel n.

7 Hardware will automatically clear the corresponding bit in DDB as soon as it starts to fetch the descriptor.

8 Wait for DMA request from peripherals to start channel n's DMA transfer.

9 After DMA transfers described by the current descriptor complete, if current DCMn.LINK =0, then DCSn.TT will be set to 1 immediately. Further, if DCMn.TIE=1, it will issue an interrupt request. However, if DCMn.LINK=1, next descriptor will be automatically fetched to repeat

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

step 8 and 9 but ignore setting DCSn.TT until a final descriptor with settting of DCMn.LINK=0 has been done.

10 When channel n's transfer ends normally (DCSn.TT=1) or abnormally (DCSn.HLT=1), to correctly reuse the channel later, software must close the channel first by setting 0 to DCSn.CTE, and then safely clear DCSn.TT or DCSn.HLT to 0.

Table 23-8 Descriptor Structure

Word	Bit	Name	Function
1st (DES0)	31	EACKS	External DMA DACKn output polarity select
	30	EACKM	External DMA DACKn output Mode select
	29-28	ERDM	External DMA request detection Mode
	27-24	Reserved	--
	23	SAI	Source Address Increment
	22	DAI	Target Address Increment
	21-20	Reserved	--
	19-16	RDIL	Request Detection Interval Length
	15-14	SP	Source port width
	13-12	DP	Target port width
	11	Reserved	--
	10-8	TSZ	Transfer Data Size
	7-3	Reserved	--
	2	STDE	Stride transfer enable
	1	TIE	Transfer Interrupt Enable
	0	LINK	Descriptor Link Enable
2nd (DES1)	31-0	DSA	Source Address
3rd (DES2)	31-0	DTA	Target Address
4th (DES3)	31-24	DOA	Descriptor Offset address
	23-0	DTC	Transfer Counter
5th (DES4)	31-16	TSD	Target Stride Address
	15-0	SSD	Source Stride Address
6th(DES5)	31-6	Reserved	--
	5-0	DRT	DMA Request Type
7th(DES6)	31-0	Reserved	--
8th(DES7)	31-0	Reserved	--

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

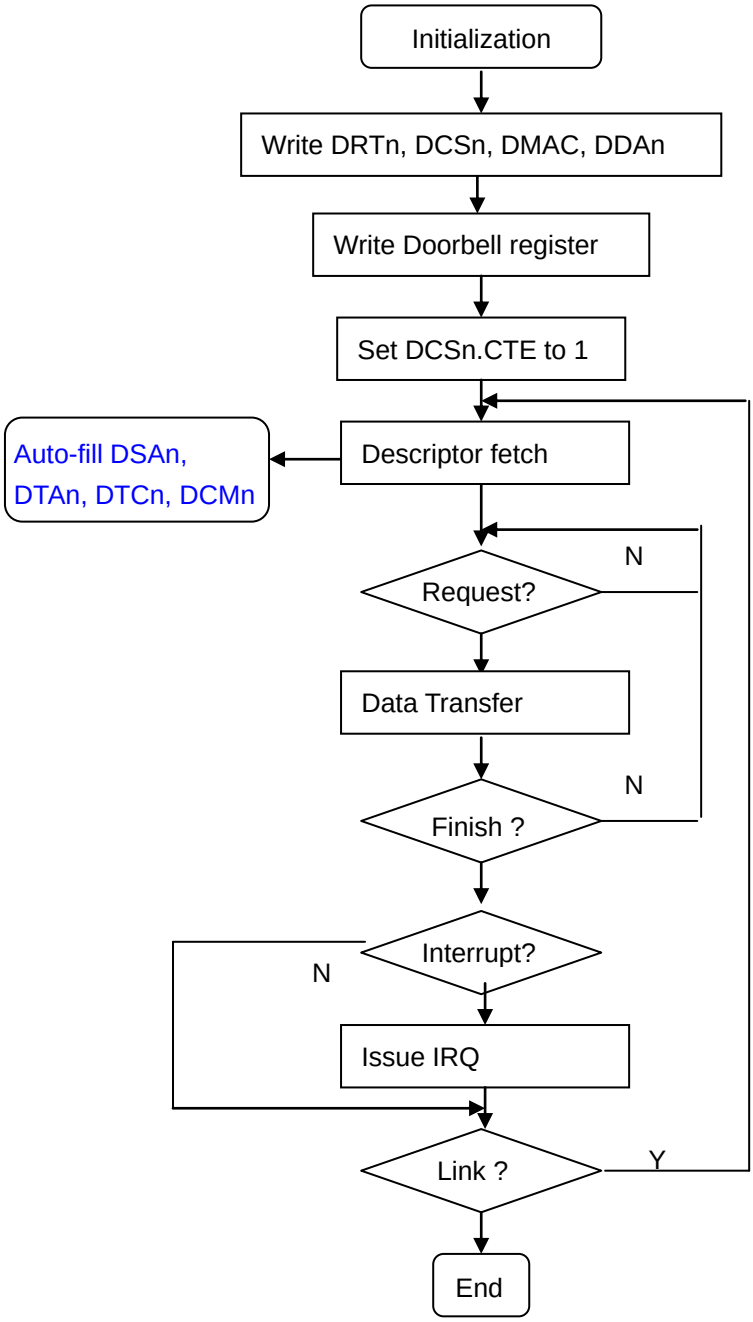


Figure 23-2 Descriptor Transfer Flow

23.8.1.2 Stride (2-dimensional) Transfer Mode

Stride transfer mode means total transfer counts are subdivided into dozens of or even hundreds of sub-blocks with same size, and each adjacent two sub-blocks has fixed nonzero address gap between the tail of preceding one and the head of subsequent one.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

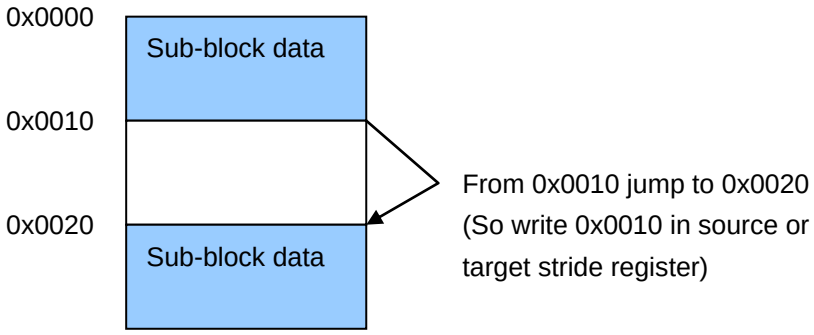


Figure 23-3 Example for Stride Transfer Mode

Manipulation steps of Stride Transfer Mode are similar to Non-stride Transfer Mode. However, each new sub-block's start address (source or destination) is performed by adding the next adjacent byte address of very completed sub-block's end address to corresponding stride difference.

23.8.2 No-Descriptor Transfer Mode

To do proper No-Descriptor DMA transfer, do following steps:

1 Check whether the status of DMA controller is available, that is, for global control (DMAC), ensure that DMAC.AR=0 and DMAC.HLT=0; and then for expected channel n, ensure that DCSn.AR=0, DCSn.HLT=0, DCSn.TT=0, DTCn=0.
2 Forx channel n, initialize DSAn, DTAn, DTCn, DRTn, DCSn, DCMn properly.
3 Set DMAC.DMAE=1 and DCSn.CTE=1 to launch DMA transfer.

For a channel with auto-request (DRTn.RT=0x8), the transfer begins automatically when the DCSn.CTE bit and DMAC.DMAE bit are set to 1. While for a channel with other request types, the transfer does not start until a transfer request is issued and detected.

For any channel n, The DTCn value is decremented by 1 for each successful transaction of a data unit. When the specified number of transfer data unit has been completed (DTCn = 0), the transfer ends normally. Meanwhile if DCMn.TIE=1, corresponding bit of DIRQP will be set to 1 to raise an interrupt request. However, during the transfer, if a DMA address error occurs, the transfer should be suspended, both DCSn.AR and DMAC.AR are set to 1 as well as corresponding bit of DIRQP to raise an interrupt request despite of DCMn.TIE.

Sometimes, for example, an UART parity error occurs for a channel that is transferring data between such UART and another terminal. In the case, both DCSn.HLT and DMAC.HLT are set to 1 and the transfer is suspended. Software should identify halt status by checking such two bits and re-configure DMA to let DMA rerun properly later.

23.8.3 Descriptor Transfer Interrupt/Stop control

DMA descriptor provides a more fast and easy way to transfer data. Usually in a long descriptor

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

linked-line, it's hard to specifically know where the current descriptor point is. Here are the recommended ways to help software to control this.

Register	Part	Name	Function
DCSn	15:8	CDOA	Copy of offset address of last completed descriptor from that in DMA command register.
	0:0	CTE	Channel transfer enable: 0: disable; 1: enable. **Note: If set during a long descriptor linked-line, DMA will finish the current data unit transfer and terminate the whole transfer. If it is not necessary, don't use this method to end the transfer.**
DCMn	1:1	TIE	Transfer Interrupt Enable (TIE). 0: disable interrupt; 1: enable interrupt when TT is set to 1. **Note: If set during a long descriptor linked-line, DMA will raise a interrupt to INTC, if not masked, and this can be acknowledged by visit DSP register. Also if TIE has already been set in the descriptor, DMA will also raise interrupt except that is the last descriptor, and if it happens, DIRQP will raise instead of DIP.**
	0:0	LINK	Descriptor Link Enable. 0: disable; 1: enable. **Note: If set during a long descriptor linked-line, DMA will finish the current descriptor, and then regard it as a no-linked descriptor and stop transfer. However, it has a change that write this bit to 0 is ignored by hardware, so a double write or a read-check is recommended.**
DIP	7:0	DIP	Descriptor interrupt pending. If any of the descriptor, except the last one, set TIE, the corresponding bit of this register shall set after the very descriptor finished. This function provide more flexible method to be aware of the process of the long descriptor links. 0: No descriptor interrupt pending 1: The corresponding bit channel has completed a descriptor with TIE Read only for software. **Note: DIP will raise if the two conditions satisfy, one is this is not the last descriptor, the other is the current TIE in DCMn or TIE in current descriptor is set.**

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

23.9 DMA Requests

DMA transfer requests are normally generated from either the data transfer source or target, but also they can be issued by on-chip peripherals that are neither the source nor the target. There are two DMA transfer request types: auto-request, and on-chip peripheral request. For any channel n, its transfer request type is determined through DRTn.

23.9.1 Auto Request

When there is no explicit transfer request signal available, for example, memory-to-memory transfer or memory to some on-chip peripherals like GPIO, the auto-request mode allows the DMA to automatically generate a transfer request signal internally. Therefore, when DMA initialization done, once the DMAC.DMAE and DCSn.CTE are set to 1, the transfer begins immediately in channel n which DRTn=0x8.

23.9.2 On-Chip Peripheral Request

In the mode, transfer request signals come from on-chip peripherals or even off-chip devices. When a device issues a peripheral request to its corresponding channel n, the transferred byte number for the request is equals to:

1. byte number determined by the bytes denoted by DCMn.TSZ when DCMn.TSZ != 7
2. byte number determined by the bytes denoted by RDIL when DCMn.TSZ == 7

Be careful that the above number must not exceed the device's expected one otherwise FIFO under-run or over-run may occur. However, if the number is too small than the expected one, DMA's bus efficiency will become worse.

23.10 How to Use Programmable DMA Channel

When system needs to setup one programmable channel for later use of smart data transfer, do following steps:

1. Load elaborate firmware to TCSM, should use physical address 0x13422xxx. Common code fragment of IRQ exception handler must be located at physical address range beginning from 0x13422100.
2. Prepare a DMA channel n using expected transfer mode as description in preceding chapters
3. Must set DCMn.TIE=1 and DMACP.DCPn=1
4. Must ensure DCIRQM.CIRQMn==0
5. Launch the channel n as description in preceding chapters

Now the channel n becomes a working programmable channel. It is the responsibility of local channel IRQ's handler to remove corresponding channel IRQ source by setting 0 to DCSn.TT.

Moreover, if programmer wants to let the channel can be triggered by local soft IRQ, DSIRQM.SIRQMn must be set 0, then at expected moment, the MCU sets 1 to DSIRQP.SIRQn to trigger a soft IRQ. It is the responsibility of this soft IRQ's handler to remove the IRQ by setting 0 to DSIRQP.SIRQn.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

24 SAR A/D Controller

24.1 Overview

The A/D is CMOS low-power dissipation 10bit touch screen SAR(successive Approximation Register) analog to digital converter. It operates with 3.3V power supply. It is developed as an embedded high resolution ADC targeting to the 40nm CMOS process and has wide application in portable electronic devices, high-end home entertainment center, communication systems and so on.

The SAR A/D controller is dedicated to control A/D to work at two different modes: normal operation mode and repeat sampling. The sampling data can transfer to memory though CPU.

24.2 Features

- 6 Channels
- Resolution: 10-bit
- Integral nonlinearity: ±1 LSB
- Differential nonlinearity: ±2 LSB
- Resolution/speed: up to 1Msps
- Max Clock Frequency: 24MHZ
- Low power dissipation: 1.5mW(worst)
- Support three auxiliary input (Through pin AUX0 to AUX4)
- Pin Description

24.3 Block Diagram

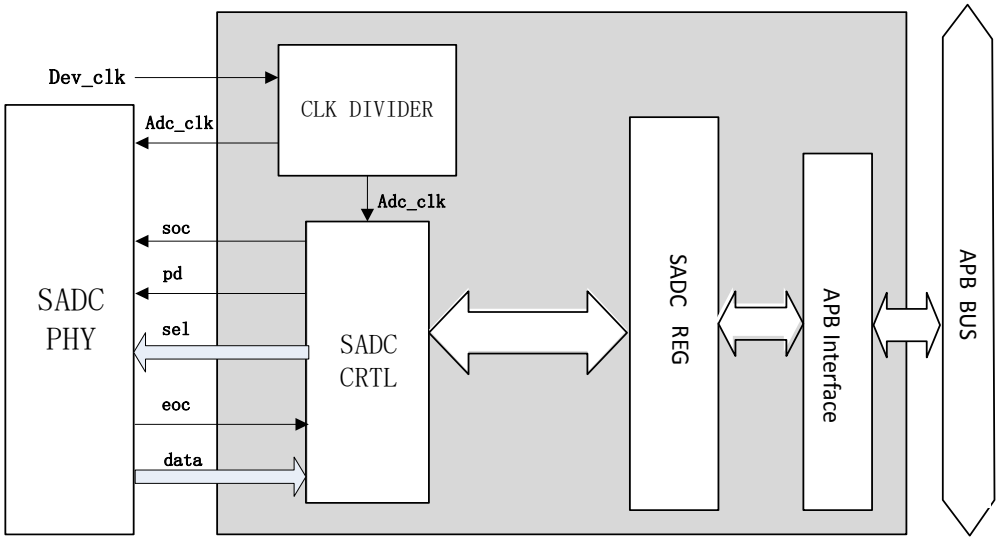


Figure 24-1 Block Diagram of SADC

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

24.4 Pins Description

SADC has 5 analog input pin. They are listed and described in.

Table 24-1 SADC Analog Pin

Name	I/O	Description
AUX0	AI	Auxiliary Input
AUX1	AI	Auxiliary Input
AUX2	AI	Auxiliary Input
AUX3	AI	Auxiliary Input
AUX4	AI	Auxiliary Input
AUX5	AI	Auxiliary Input

24.5 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. The registers can be read and written by APB bus
3. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
4. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

24.5.1 Register Memory Map

Table 24-2 Registers Memory Map Base Address

Name	Base	Description
SADC	0x10070000	Address base of SADC

The SAR A/D Controller is controlled by a set of registers that the application configures before

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

every operation. The following table lists all the registers.

Table 24-3 SADC Registers Map

Name	RW	Reset Value	Address Offset	Access Size
ADENA	RW	0x8000	0x0000	16
ADCFG	RW	0x0000_0001	0x0004	32
ADCTRL	RW	0xFF	0x0008	8
ADSTATE	RW	0x00	0x000C	8
ADATA0	RW	0x0000_0000	0x0010	32
ADATA1	RW	0x0000_0000	0x0014	32
ADATA2	RW	0x0000_0000	0x0018	32
ADCLK	RW	0x0004_1000	0x0020	32
ADSTB	RW	0x0000	0x0024	16
ADRETM	RW	0x0000_0000	0x0028	32

24.5.2 Register and Fields Description

24.5.2.1 ADC Enable Register (ADENA,0x0000)

The register ADENA is used to trigger A/D to work.

	ADENA																BASE + 0x0000													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																POWRR	Pow_opt_	Reserved				REPTEN	Reserved				AUX4EN	AUX3EN	AUX2EN	AUX1EN	AUX0EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15	POWER	SADC Power control bit. 1: SADC power down 0: SADC power on When POWER is set from 1 to 0, you should wait at least 2ms to enable SADC.	RW
14	POW_OPT	Power optimize enable 1: enable 0: disable	RW
13:10	Reserved	Writing has no effect, read as zero.	R
9	REPTEN	Repeat sampling enable	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

8:5	Reserved	Writing has no effect, read as zero.	RW
4	AUX4EN	AUX4 Enable Control.	RW
3	AUX3EN	AUX3 Enable Control.	RW
2	AUX2EN	AUX2 Enable Control.	RW
1	AUX1EN	AUX1 Enable Control.	RW
0	AUX0EN	AUX0 Enable Control.	RW

Note:

When two or more channel enable, the controller will sampling all the enabled channel from low to high.

24.5.2.2 ADC Configure Register (ADCFG,0x0004)

The register ADCFG is used to Sadc's PHY testmode and rst_n to work.

	ADCFG																BASE + 0x0004															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADC_TRIM																Reserved															ADC_RST
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:16	ADC_TRIM	Connection to SAR_ADC's PHY for control SAR_ADC's PHY saradc_ana_reg, only used in adc testmode. please keep the value to 16'h0.	R
15:1	Reserved	Writing has no effect, read as zero.	RW
0	ADC_RST	Connection to ADC's PHY for control SAR_ADC's PHY saradc_rst_n 0: soft reset valid 1: soft reset unvalid	RW

24.5.2.3 ADC Control Register (ADCTRL,0x0008)

The register ADCTRL is used to control A/D to work.

	ADCTRL																BASE + 0x0008															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											ARDYM4	ARDYM3	ARDYM2	ARDYM1	ARDYM0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect. Read as zero.	RW
4	ARDYM4	AUX4 data ready interrupt mask. 0: enabled 1: masked	RW
3	ARDYM3	AUX3 data ready interrupt mask. 0: enabled 1: masked	RW
2	ARDYM2	AUX2 data ready interrupt mask. 0: enabled 1: masked	RW
1	ARDYM1	AUX1 data ready interrupt mask. 0: enabled 1: masked	RW
0	ARDYM0	AUX0 data ready interrupt mask. 0: enabled 1: masked	RW

24.5.2.4 ADC Status Register (ADSTATE,0x000C)

The register ADSTATE is used to keep the status of A/D.

	ADSTATE																BASE + 0x000C														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																											ARDY4	ARDY3	ARDY2	ARDY1	ARDY0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:5	Reserved	Writing has no effect. Read as zero.	R
4	ARDY4	AUX4 data ready interrupt flag. Write 1 to this bit, the bit will clear to 0. 1: active 0: not active	RWC
3	ARDY3	AUX3 data ready interrupt flag. Write 1 to this bit, the bit will clear to 0. 1: active 0: not active	RWC
2	ARDY2	AUX2 data ready interrupt flag. Write 1 to this bit, the bit will clear to 0.	RWC

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: active 0: not active	
1	ARDY1	AUX1 data ready interrupt flag. Write 1 to this bit, the bit will clear to 0. 1: active 0: not active	RWC
0	ARDY0	AUX0 data ready interrupt flag. Write 1 to this bit, the bit will clear to 0. 1: active 0: not active	RWC

24.5.2.5 ADC AUX Data Register (ADATA0,0x0010)

The read-only ADATA0 is a 32-bit register, it keep the sample data.

	ADATA0																BASE + 0x0010													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						ADATA1										Reserved						ADATA0									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect. Read as zero.	R
25:16	ADATAH	Data of AUX1. When write to the register, DATA will be clear to 0.	RW
15:10	Reserved	Writing has no effect. Read as zero.	R
9:0	ADATAL	Data of AUX0. When write to the register, DATA will be clear to 0.	RW

24.5.2.6 ADC AUX Data Register (ADATA1,0x0014)

	ADATA1																BASE + 0x0014													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						ADATA3										Reserved						ADATA2									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Read as zero.	
25:16	ADATAH	Data of AUX3. When write to the register, DATA will be clear to 0.	RW
15:10	Reserved	Writing has no effect. Read as zero.	R
9:0	ADATAL	Data of AUX2. When write to the register, DATA will be clear to 0.	RW

24.5.2.7 ADC AUX Data Register (ADATA2,0x0018)

	ADATA1																BASE + 0x0018															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																						ADATA4									
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:10	Reserved	Writing has no effect. Read as zero.	R
9:0	ADATAL	Data of AUX4. When write to the register, DATA will be clear to 0.	RW

The measured voltage V_{AUX} (V_{AUX1} and V_{AUX2}) is as follows:

$$V_{SAD} = \frac{ADATA}{1024} \bullet VREF_ADC$$

24.5.2.8 ADC Clock Divide Register (ADCLK,0x0020)

The register ADCLK is used to set the A/D's clock dividing number.

	ADCLK																BASE + 0x0020															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLKDIV_MS																CLKDIV_US								CLKDIV							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	CLKDIV_MS	Dividing number to get ms clock from ADC clock.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		ms_clk = us_clk / (CLK_MS +1)	
15:8	CLKDIV_US	Dividing number to get us clock from ADC clock. us_clk = adc_clk / (CLKDIV_US+1) 0 ≤CLKDIV_10 ≤127	RW
7:0	CLKDIV	Dividing number to get ADC clock from device clock. The A/D works at the frequency between 20KHz and 200KHz. If CLKDIV = N, Then the freq of adc_clk = dev_clk / (N+1). 0 ≤ N ≤ 255	RW

24.5.2.9 ADC Stable Register (ADSTB,0x0024)

ADC Stable register is used for delay some ADC clock cycle to wait ADC stable when sampling AUX voltage.

	ADSTB																BASE + 0x0024															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																STABLE															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

24.5.2.10 ADC REPEAT TIME Register (ADRETM,0x0028)

ADC REPEAT TIME register is used to set the sampling VBAT delay time when ADENA.REPEN is set to 1, and the repeat sampling wait time is RETTIME multiply clk_ms.

	ADRETM																BASE + 0x0028															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RETIME																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

24.6 SAR A/D Controller Guide

The following describes steps of using SAR-ADC.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

24.6.1 Power Down Mode

1 When initial value of ADENA POWER is 1, the state of SADC is in power down state.
2 When you want to use SADC, you should first set ADENA.POWERON to 0 to power on SADC. And wait for at least 2ms, then you can enable required AUX.
3 When you want to power down SADC to get lower power, you should disable AUX, and then set ADENA.POWER to 1.

24.6.2 AUX Sample Operation

1 Set ADCLK.CLKDIV, ADCLK.CLKDIV_US and ADCLK.CLKDIV_MS to set A/D clock frequency.
2 Set ADENA.AUXn(0-2) to 1 to enable the channel.
3 When ADSTATE.VRDYn(0-2) = 1, you can read the sample data from corresponding ADVDATn(0-2). And the AUXEN will be set to 0 auto.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

25 Real Time Clock

25.1 Overview

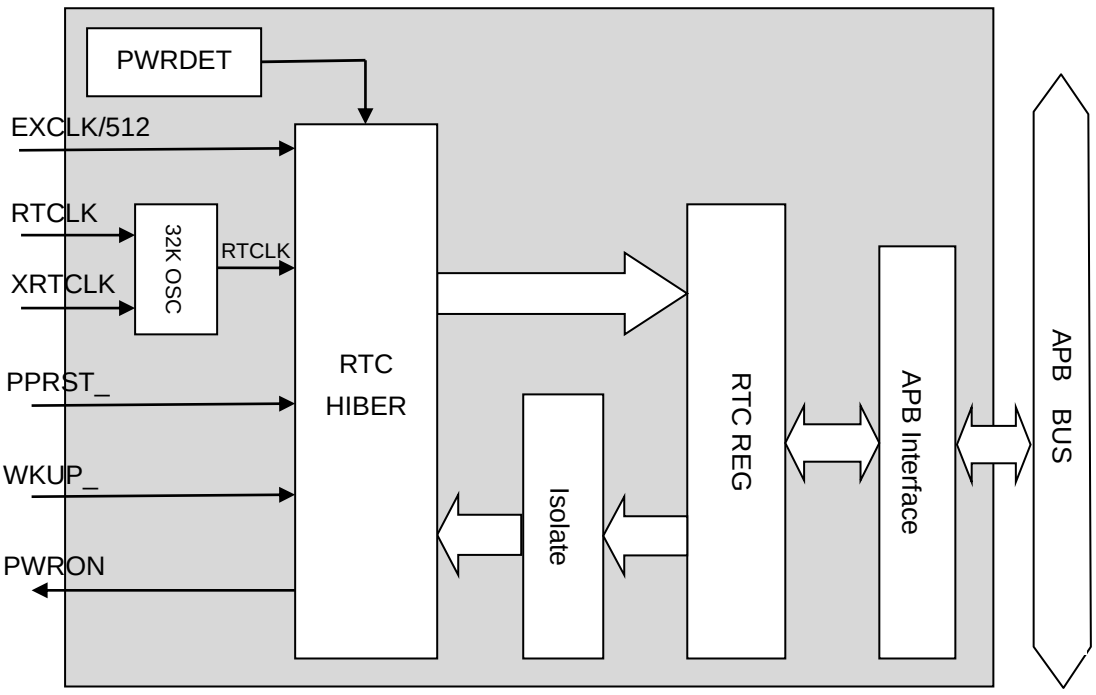
The Real-Time Clock (RTC) unit can be operated in either chip main power is on or the main power is down but the RTC power is still on. In this case, the RTC power domain consumes only a few micro watts power.

The RTC contains a real time, alarm logic and the power down and wakeup control logic.

25.2 Features

- Embedded 32768Hz oscillator for 32k clock generation with an external 32k crystal
- RTCLK selectable from the oscillator or from the divided clock of EXCLK, so that 32k crystal can be absent if the hibernating mode is not needed
- 32-bits second counter
- Programmable and adjustable counter to generate accurate 1 Hz clock
- Alarm interrupt, 1Hz interrupt
- Stand alone power supply, work in hibernating mode
- Power down controller
- Alarm wakeup
- External pin wakeup with up to 2s glitch filter

25.3 Block Diagram



Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

25.4 Pins Description

RTC has 6 signal IO pins and 1 power pin. They are listed and described in.

Pin Names	Pin Loc	IO	IO Cell Char.	Pin Description	Power
RTCLK		AI	32768Hz	RTCLK: 32768 clock input or OSC input	VDDRTC33
XRTCLK		AO		XRTCLK: OSC output	VDDRTC33
PWRON		O		PWRON: Power on/off control of main power	VDDRTC33
WKUP_		I	Schmitt	WKUP_: Wake signal after main power down	VDDRTC33
PPRST_		I	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDDRTC33
VDDRTC33		P		VDDRTC33: 3.3V power for RTC and hibernating mode controlling that never power down (normally you can use 1.8V instead to reduce power consumption)	-
VDDRTC11		P		VDDRTC11: 1.1V power for RTC logic power	

RTCLK pin. need input 32.768KHz rtc clock. If do not use any clock, hibernate mode will be NOT available any more, and the time will lose if power down.

PWRON pin: this pin is used to control the main power on/off. Output high voltage means on and low voltage means off.

WKUP_ pin: hibernating mode wakeup input. (low active)

PPRST_ pin: This pin should be set to low voltage only in two cases.

- When RTC power is turned on. (so that whole chip is power on)
- A RESET-KEY is pressed.

25.5 Registers Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

5. Register Address = Base + Address offset
6. The registers can be read and written by APB bus
7. Register read/write attribute

   R - Read only

   W - Write only

   RW - read and write

   RCW - read and write, but clear to 0 by read

   RSW - read and write, but set to 1 by read

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

RWC - read and write, clear to 0 by write 1, write 0 has no effect
RWS - read and write, set to 1 by write 1, write 0 has no effect
RC - read only, and clear to 0 by read
RS - read only, and set to 1 by read
SPEC - special access method, relate to its description

8. Reset Value
1 - reset to 1
0 - reset to 0
? - value unknown after reset

Table 25-1 Registers Memory Map-Address Base

Name	Base	Description
RTC	0x10003000	Address base of RTC

Table 25-2 Registers for real time clock

Name	Description	Reset Value	Address offset	Access Size
RTCCR	RTC Control Register	0x000000??*1*2	0x000	32
RTCSR	RTC Second Register	0x????????	0x004	32
RTCSAR	RTC Second Alarm Register	0x????????	0x008	32
RTCGR	RTC Regulator Register	0x0???????	0x00C	32

NOTES:

1 *1: Unless otherwise stated, the reset value is for PPRST_ and Hibernating wakeup reset. WDT reset doesn't change the value.

2 *2: The reset value can be either of 0x00000081, 0x00000091, 0x00000089, 0x00000099.

Table 25-3 Registers for hibernating mode

Name	Description	Reset Value	Address offset	Access Size
HCR	Hibernate Control Register	0x00000000*1	0x020	32
HWFCR	Wakeup filter counter Register in Hibernate mode	0x0000???0	0x024	32
HRCR	Hibernate reset counter Register in Hibernate mode	0x00000??0	0x028	32
HWCR	Wakeup control Register in Hibernate mode	0x2d52d2d0*1	0x02C	32

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

HWRSR	Wakeup Status Register in Hibernate mode	0x00000???*[1]	0x030	32
HSPR	Scratch pattern register	0x????????	0x034	32
WENR	Write enable pattern register	0x00000000	0x03C	32
WKUPPINCR	Configure the extend press WKUP pin to reset chip	0x00050064	0x048	32

NOTE:

*[1]: Unless otherwise stated, the reset value is for PPRST_ and Hibernating wakeup reset. WDT reset doesn't change the value.

All these registers, include those for real time clock and for hibernating mode control, except otherwise stated, are implemented in RTCLK clock domain. When write to these registers, it needs about 1 ~ 2 RTCLK cycles to actually change the register's value and needs another RTCLK cycle to allow the next write access. A bit RTCCR.WRDY is used to indicate it. When RCR.WRDY is 1, it means the previous write is finished, a right value can be read from the target register, and a new write access can be issued. So before any write access, please make sure RCR.WRDY = 1.

25.5.1 RTC Control Register (RTCCR)

RTCCR contains bits to configure the real time clock features. Unless otherwise stated, the reset value is for PPRST_ and Hibernating wakeup reset. WDT reset doesn't change the value.

	RTCCR																													BASE + 0x000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								WRDY	1HZ	1HZIE	AF	AIE	AE	SELEXC	RTCE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1*[1]	0	0*[1]	?	0	?	0*[1]	1

NOTE:

*[1]: These bits are reset in all resets: PPRST_ input pin reset, hibernating reset and WDT reset.

Bits	Name	Description	RW
31:7	Reserved	Writing has no effect, read as zero.	R
7	WRDY	Write ready flag. It is 0 when a write is currently processing and the value has not been written to the writing target register. No write to any RTC registers can be issued in this case, or the result is undefined. The read value from the target register is also undefined. The reading is meaningful and another write can be issued when it is 1. This bit is read only and write to it is ignored.	R
6	1HZ	1Hz flag. This bit is set by hardware once every 1 second through the	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td></td><td></td><td>1Hz pulse if the real time clock is enabled (RTCCR.RTCE = 1). This bit can be cleared by software. Write 1 to this bit is ignored.</td><td></td></tr>
<tr><td>5</td><td>1HZIE</td><td>1Hz interrupt enable. Writing to this bit takes effect immediately without delay.<table><tr><th>1HZIE</th><th>Description</th></tr><tr><td>0</td><td>1Hz interrupt is disabled.</td></tr><tr><td>1</td><td>1Hz interrupt is enabled. RTC issues interrupt when 1HZ bit is set.</td></tr></table></td><td>RW</td></tr>
<tr><td>4</td><td>AF</td><td>Alarm flag. This bit is set by hardware when alarm match (RTCSR = RTCSAR) is found and alarm is enabled (RTCCR.AE = 1) and the real time clock is enabled (RTCCR.RTCE = 1). This bit can be cleared by software. Write 1 to this bit is ignored. Writing to this bit takes effect immediately.</td><td>RW</td></tr>
<tr><td>3</td><td>AIE</td><td>Alarm interrupt enable.<table><tr><th>AIE</th><th>Description</th></tr><tr><td>0</td><td>Alarm interrupt is disabled.</td></tr><tr><td>1</td><td>Alarm interrupt is enabled. RTC issues interrupt when AF is set.</td></tr></table></td><td>RW</td></tr>
<tr><td>2</td><td>AE</td><td>Alarm enable.<table><tr><th>AE</th><th>Description</th></tr><tr><td>0</td><td>Alarm function is disabled.</td></tr><tr><td>1</td><td>Alarm function is enabled.</td></tr></table></td><td>RW</td></tr>
<tr><td>1</td><td>SELEXC</td><td>The divided EXCLK is selected as RTCLK in rtc-hiber module.<table><tr><th>SELEXC</th><th>Description</th></tr><tr><td>0</td><td>OSC32K or RTCLK input clock is selected as RTCLK in rtc-hiber module.</td></tr><tr><td>1</td><td>The divided EXCLK is selected as RTCLK in rtc -hiber module.</td></tr></table>NOTE: If do not use any 32Khz clock (either input clock or using crystal), hibernate mode will be NOT available any more, and the time will lose if power down.
CPM.OPCR.ERCS must be 0, when using SELEXC = 1.
When the main chip power down, SELEXC will be 0 in internal circuit, in this time, RTCLK will use OSC32K clock.</td><td>RW</td></tr>
<tr><td>0</td><td>RTCE</td><td>Real time clock enable.<table><tr><th>RTCE</th><th>Description</th></tr><tr><td>0</td><td>Real time clock function is disabled.</td></tr><tr><td>1</td><td>Real time clock function is enabled.</td></tr></table></td><td>RW</td></tr>
</table>

25.5.2 RTC Second Register (RTCSR)

RTCSR is a 32-bit width second counter. It can be read and write by software. It is increased by 1 at

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

every 1Hz pulse if the real time clock is enabled (RTCCR.RTCE = 1). When read, it should be read continued more than once and take the value if the adjacent results are the same. RTCSR is not initialized by any reset.

	RTCSR																													BASE + 0x004	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RTCSR																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

25.5.3 RTC Second Alarm Register (RTCSAR)

RTCSAR serves as a second alarm register. Alarm flag (RTCCR.AF) is set to 1 when the RTCSR equals the RTCSAR in the condition of alarm is enabled (RTCCR.AE = 1) and the real time clock is enabled (RTCCR.RTCE = 1). RTCSAR can be read and write by software and is not initialized by any reset.

	RTCSAR																													BASE + 0x008	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RTCSAR																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

25.5.4 RTC Regulator Register (RTCGR)

RTCGR is serves as the real time clock regulator, which is used to adjust the interval of the 1Hz pulse.

	RTCGR																													BASE + 0x00C	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LOCK	Reserved					ADJC										NC1HZ															
RST	0*[1]	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

NOTE:

*[1]: This bit is reset in all resets: PPRST_ input pin reset, hibernating reset and WDT reset.

Bits	Name	Description	RW
31	LOCK	Lock bit. This bit is used to safeguard the validity of the data written into the RTCGR register. Once it is set, write to RTCGR is ignored. This bit can only be set by software and cleared by (any type of) resets.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

			LOCK	**Description**		
			0	Write to RTCGR is allowed.		
			1	Write to RTCGR is forbidden.		
30:26	Reserved	Writing has no effect, read as zero.				R
25:16	ADJC	This field specifies how many times it needs to add one 32kHz cycle for the 1Hz pulse interval in every 1024 1Hz pulses. In other words, among every 1024 1Hz pulses, ADJC number of them are trigged in every (NC1HZ + 2) 32kHz clock cycles, (1024 – ADJC) number of them are trigged in every (NC1HZ + 1) 32kHz clock cycles.				RW
15:0	NC1HZ	This field specifies the number plus 1 of the working 32kHz clock cycles are contained in the 1Hz pulse interval. In other words, 1Hz pulse is trigged every (NC1HZ + 1) 32kHz clock cycles, if RTCGR.ADJC = 0.				RW

25.5.5 Hibernate Control Register (HCR)

HCR contains the bit to control the main chip power on/off. Unless otherwise stated, the reset value is for PPRST_ and Hibernating wakeup reset.

	HCR																														BASE + 0x020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															PD
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description			RW
31:1	Reserved	Writing has no effect, read as zero.			R
0	PD	Power down or power on bit. Besides writing by CPU, this bit will be set to 1 if an unknown reason main power supply off is detected. This bit controls the PWRON pin level. When co-working with some external components, this bit is used for power management of this chip. It is supposed when 1 is written to this bit, the main power supply of the chip, except RTC power, will be shut down immediately. After this bit is set to 1, all registers in RTC module, except RTCCR.1HZ and RTCCR.1HZIE, cannot be changed by write access. This bit is cleared by reset pin reset and hibernating reset. The later one is asserted by wakeup procedure.			RW
		PD	**PWRON**	**Description**	
		0	VDDRTC33	No power down, keep power on.	
		1	0 V	Power down enable, turn power off.	

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

25.5.6 HIBERNATE mode Wakeup Filter Counter Register (HWFCR)

The HIBERNATE mode Wakeup Filter Counter Register (HWFCR) is a 32-bit read/write register .It filter the glitch generated by a dedicated wakeup pin. The HWFCR is not initialized by any reset.

	HWFCR																BASE + 0x024														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																HWFCR											Reserved				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:5	HWFCR	Wakeup pin effective minimum time in number of 32 RTCLK cycles, used as glitch filter logic. Maximum of 2 seconds if the RTCLK is 32768Hz If this value is configured to 0, and the WKUP pin keeps low longer than 15 RTCLK periods, it will wakes up RTC from Hibernate. The glitch filter time equals to HWFCR*32 RTCLK period.	RW
4:0	Reserved	Writing has no effect, read as zero.	R

25.5.7 Hibernate Reset Counter Register (HRCR)

The Hibernate Reset Counter Register is a 32-bit read/write register that specifies hibernate reset assertion time. The HRCR is initialized by PPRST_ .

	HRCR																BASE + 0x028														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																HRCR				Reserved											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:15	Reserved	Writing has no effect, read as zero.	R
14:11	HRCR	HIBERNATE Reset asserting time. Number of 2048 RTCLK cycles. Default value 0x1, assert 125 ms. Maximum 1 second if the RTCLK is 32768Hz. If this value is configured to 0, it will generate 2048 RTCLK HIBERNATE Reset, about 62.5 milliseconds.	RW
10:0	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

25.5.8 HIBERNATE Wakeup Control Register (HWCR)

The HIBERNATE Wakeup Control Register is a 32-bit read/write register that controls real time clock alarm wake up enable. The reset value only for PPRST_ .

	HWCR																													BASE + 0x02C	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPDET																													Reserved		EALM
RST	0	0	1	0	1	1	0	1	0	1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0	0	0	0*[1]

NOTE:

*[1]: This bit is reset in PPRST_ input pin reset and hibernating reset .

Bits		Name	Description	RW
31:3		EPDET	Power detect enable. 0x5aa5a5a: enable(default) 0x1a55a5a5: disable Only 0x1a55a5a5 can disable power detect, other values will enable the power detect.	RW
2:1		Reserved	Writing has no effect, read as zero.	R
0		EALM	RTC Alarm wakeup enable. 0: disable 1: enable	RW

25.5.9 HIBERNATE Wakeup Status Register (HWRSR)

The HIBERNATE Wakeup Status Register is a 32-bit read/write register that reflects wakeup status bits.

	HWRSR																													BASE + 0x030	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																							APD	Reserved		HR	PPR	Reserved		PIN	ALM
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	0	0	1*[2]	1*[1]	0	0	?	?

NOTES:

*[1]: This reset value only for PPRST_. It is undefined in case of other resets.

*[2]: This reset value only for HRST_. It is undefined in case of other resets.

Bits	Name	Description	RW
31:9	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td>8</td><td>APD</td><td>Accident power down. When the software has not set to HIBERNATE state, the core power is down, then an accident power down is detected. APD is set and remains set until software clears it. This bit can only be written with 0. Write with 1 is ignored.<table><tr><th>HR</th><th>Description</th></tr><tr><td>0</td><td>Accident power down has not occurred since the last time the software clears this bit.</td></tr><tr><td>1</td><td>Accident power down has occurred since the last time the software clears this bit.</td></tr></table></td><td>RW</td></tr>
<tr><td>7:6</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>5</td><td>HR</td><td>Hibernate Reset. When a Hibernate reset detected, HR is set and remains set until software clears it. This bit can only be written with 0. Write with 1 is ignored.<table><tr><th>HR</th><th>Description</th></tr><tr><td>0</td><td>Hibernate reset has not occurred since the last time the software clears this bit.</td></tr><tr><td>1</td><td>Hibernate reset has occurred since the last time the software clears this bit.</td></tr></table></td><td>RW</td></tr>
<tr><td>4</td><td>PPR</td><td>PAD PIN Reset. When a PPRST_ is detected, PPR is set and remains set until software clears it. This bit can only be written with 0. Write with 1 is ignored.<table><tr><th>PPR</th><th>Description</th></tr><tr><td>0</td><td>PPRST_ reset has not occurred since last time the software clears this bit.</td></tr><tr><td>1</td><td>PPRST_ reset has occurred since last time the software clears this bit.</td></tr></table></td><td>RW</td></tr>
<tr><td>3:2</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>1</td><td>PIN</td><td>Wakeup Pin Status bit. The bit is cleared when chip enters hibernating mode. It is set when exit the hibernating mode by wakeup pin. This bit can only be written with 0. Write with 1 is ignored.</td><td>RW</td></tr>
<tr><td>0</td><td>ALM</td><td>RTC Alarm Status bit. The bit is cleared when chip enters hibernating mode. It is set when exit the hibernating mode by alarm. This bit can only be written with 0. Write with 1 is ignored.</td><td>RW</td></tr>
</table>

25.5.10 Hibernate Scratch Pattern Register (HSPR)

This is a scratch register used to hold a pattern. The software can check the pattern is kept to know whether RTC power has ever been down and whether it is needed to setup the real time clock.

	HSPR																BASE + 0x034													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	PAT																													
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	PAT	The pattern.	RW

25.5.11 Write Enable Pattern Register (WENR)

This is a write protect register to may the rtc registers can write only in certain condition.

	WENR																BASE + 0x03C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WEN	Reserved															WENPAT															
RST	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31	WEN	The write enable flag. If the WENPAT is 0xA55A then this bit will be 1. When the WEN changes to 1, the RTCCR, RTCSR, RTCSAR, RTCGR, HCR, HWFCR, HRCR, HWCR, HWRSR, HSPR registers could be changed. But RTCCR.SELEXC, RTCCR.HZIE, RTCCR.WRDY may change in any time. This bit is read only and write to it is ignored. This bit only reset by PPRST_ and HRST_. There is an exception, when system does NOT have RTC 32Khz crystal. MUST write 1 to RTCCR.SELEXC before write to any value to any other registers. **WEN / Description** 0: Other RTC registers is locked, write these registers will be ignored. 1: Other RTC registers can be changed.	R
30:16	Reserved	Writing has no effect, read as zero.	R
15:0	WENPAT	The write enable pattern. Before writing any value to RTCCR, RTCSR, RTCSAR, RTCGR, HCR, HWFCR, HRCR, HWCR, HWRSR, HSPR registers, write 0xA55A to WENPAT to set these register writable. If this value is ok, WEN will change to 1. But RTCCR.SELEXC and RTCCR.HZIE are writable in any time. These bits are write-only, always read as 0.	W

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

25.5.12 WKUP_PIN_RST control register (WKUPPINCR)

This is a register used to control the enable and set the judge time to reset the chip when extend press the WKUP pin. The are only initialized by PPRST_ and HRST_.

	WKUPPINCR																BASE + 0x048													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									Ramshut	ramsleep	bufferen	fastboot	Driving		Reserved	OSC_EN	Reserved								P_JUD_LEN				P_RST_EN			
RST	0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23	RamShut	Fast boot Ram shut down. 1: shutdown	RW
22	RamSleep	Fast boot Ram sleep. 1: sleep	RW
21	Buffer_en	DDR buffer enable.	RW
20	Fastboot	Fast boot enable. 1: enable	RW
19:18	Driving selector	RTC oscillator Driving selector	RW
17	Reserved	Reserved	RW
16	OSC_EN	RTC internal oscillator enable 1: enable 0: disable	RW
15:5	Reserved	Writing has no effect, read as zero.	R
7:4	P_JUD_LEN	WKUP up pin extend press length judge value The judge time equals to FLT_LEN multiply RTC 1HZ period, and only the active press length equal or greater than judge time, the chip reset can assert.	RW
3: 0	P_RST_EN	Enable reset chip by extend press WKUP pin Others value: disable 4'hB: enable	RW

25.6 Operation Flow

25.6.1 Registers Access

25.6.2 Registers Read

All registers can read directly, but the RTCSR and RTCSAR should be read continued more than once and take the value if the adjacent results are the same. Please check and make sure RTCCR.WRDY equals to 1 before execute a register read.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

25.6.3 Registers Write

Only the RTCCR.SELEXC, RTCCR.HZIE, RTCGR.LOCK, WENR.WENPAT bits can write directly. Others bits need following the below procedure

1) Check RTCCR.WRDY, make sure it equals to 1
2) Write 0xa55a to WENR register to enable other registers write.
3) Waiting WENR.WEN change to 1
4) Check RTCCR.WRDY, make sure it equals to 1
5) Write the target register
6) Waiting RTCCR.WRDY equals to 1 to make sure the current write processing was finished.

25.6.4 Normal Mode

25.6.5 Power Detect

When PPRST_ reset, the HWCR.EPDET set to 0x5aa5a5a, and the power detect is enable. If you want To disable the power detect, you should set HWCR.EPDET to 0x1a55a5a5. If power detect is enable, when CORE power supply was lose, the RTC will into hibernate mode. And if power detect is not enable, the RTC can't enter hibernate mode even CORE power supply was lose.

25.6.6 Power On Timing Diagram

The RTC power on procedure like diagram 1 -1.

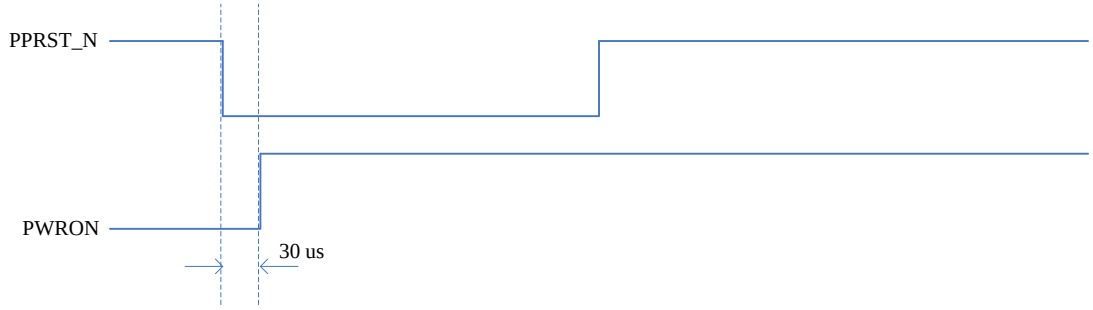


Figure 25-1 Core Power On

25.6.7 HIBERNATE Mode

The purpose of hibernate mode is to save the power. When in hibernate mode, CORE will no power consumption.

If you want to use hibernate mode, please first make sure RTCCR.SELEXC is 0.
When Software writes 1 to PD bit of HCR, the system at once enters HIBERNATE mode. The powers of CORE and IO are disconnected by PWRON pin, no power consumption in core and IO. When a wakeup event occurs, the core enters normal mode through a hibernate reset.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

25.6.8 Procedure to Enter HIBERNATE mode

Before enter HIBERNATE mode, software must complete following steps:

1 Finish the current operation and preserve all data to flash.
2 Configure the wake-up sources properly by configure HWCR.
3 Set HIBERNATE MODE. (Set PD bit in HCR to 1)

25.6.9 Procedure to Wake-up from HIBERNATE mode

1 The internal hibernate reset signal will be asserted if one of the wake-up sources is issued.
2 Check RSR to determine what caused the reset.
3 Check PIN/ALM bits of HWRSR in order to know whether or not the power-up is caused by which wake-up from HIBERNATE mode.
4 Configure the SDRAM memory controller.
5 Recover the data from flash.

25.6.10 Time Regulation

Because of the inherent inaccuracy of crystal and other variables, the time counter may be inaccurate. This requires a slight adjustment. The application processor, through the RTCGR, lets you adjust the 1Hz time base to an error of less than 1ppm. Such that if the Hz clock were set to be 1Hz, there would be an error of less than 5 seconds per month.

To determine the value programmed into the RTCGR, you must first measure the output frequency at the oscillator multiplex (approximately 32 kHz) using an accurate time base, such as a frequency counter. This clock is externally visible by selecting the alternate function of GPIO.
To gain access to the clock, program this pin as an output and then switch to the alternate function.
To trim the clock, divide the output of the oscillator by an integer value and fractional adjust it by periodically deleting clocks from the stream driving this integer divider.

After the true frequency of the oscillator is known, it must be split into integer and fractional portions. The integer portion of the value (minus one) is loaded into the NC1HZ field of the RTCGR.

The fractional part of the adjustment is done by periodically deleting clocks from the clock stream driving the Hz divider. The trim interval period is hardwired to be 1024 1Hz clock cycles (approximately 17 minutes). The number of clocks (represented by ADJC field of RTCGR) are deleted from the input clock stream per trim interval. If ADJC is programmed to be zero, then no trim operations occur and the RTC is clocked with the raw 32 kHz clock. The relationship between the Hz clock frequency and the nominal 32 kHz clock (f1 and f32K, respectively) is shown in the following equation.

$$f1 = \frac{2^{10} \times (NC1HZ + 1)}{2^{10} \times (NC1HZ + 1) + ADJC} \times \frac{f32k}{NC1HZ + 1}$$

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

f1 = actual frequency of 1Hz clock

f32k = frequency of either 32.768KHz crystal output or 3.6864MHz crystal output further divided down to 32.914KHz

25.6.11 Clock select

There could be two clock input to RTC internal clock called rtclk. One is OSC32k clock; the other is EXCLK/512.

The software MUST make sure the RTC run in valid clock configuration.

Table 25-4 Clock select registers

RTCCR.SELEXC	CPM.ERCS	Description	Valid
0	0	RTC use OSC32K clock.	OK
0	1		OK
1	0	RTC use EXCLK/512 clock.	OK
1	1	RTC will lost clock. (Not Valid)	NO

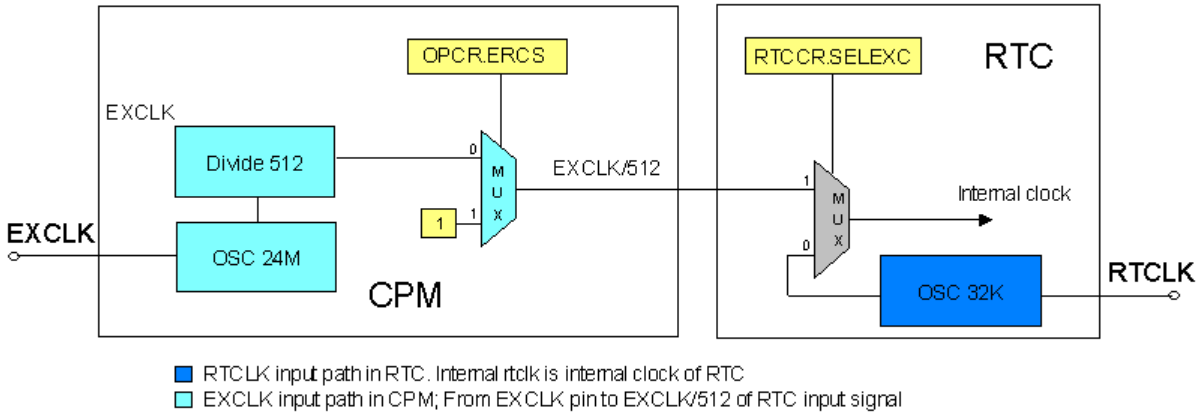


Figure 25-2 RTC clock selection path

Changing RTCLK sequence:

1 There are both 32KHz crystal and 24Mhz EXCLK crystal connected, so RTCLK input path has 32Khz clock.
In this case, there is no need to change internal clock, so do NOT change SELEXC all the time.

2 There is no 32KHz crystal connected but only 24Mhz EXCLK crystal connected, so RTCLK input path has no clock.
In this case, should flow the sequence below to change internal clock:
   a Clear OPCR.ERCS of CPM to 0; open EXCLK/512 to RTC.
   b Set RTCCR.SELEXC to 1 directly; change internal clock to EXCLK/512.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

c Wait 1ms.

d write WENR to 0xa55a.

e wait two rtc clock cycle

f Check RTCCR.WRDY == 1.

g IF YES, finish this sequence; IF NO, do step (c) again.

NOTE: If using HIBERNATE mode, MUST have both 32KHz crystal (or input 32Khz clock) and 24Mhz EXCLK crystal connected, or RTC time will be insignificant.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

26 EFUSE Slave Interface (EFUSE)

26.1 Overview

The EFUSE is provided 2K programmable bit, Total 2K bits are separated into fourteen segments.

Each segment can be programmed separately.
Each segment has a protect bit, which has higher priority than program segment selection.

Programming frequency is wide, and programming time can adjust use the EFUSE register.

Initial value of EFUSE is 0, when programmed to 1, it doesn't able to program back to 0 anymore. Do not attempt to program any bit that already programmed to 1, such action will result unpredictable status to whole EFUSE block.

Programming voltage supply pin AVDEFUSE:

- In program mode, supply AVDEFUSE with 1.8V.
  Maximum accumulative time for AVDEFUSE pin exposed under 1.8V+/-10% should be less than 200 millisecond.
- In read mode, leave AVDEFUSE to 0V.

26.2 Registers

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

26.2.1 Registers Memory Map

Table 26-1 Registers Memory Map-Address Base

Name	Base	Description
EFUSE	0x13540000	Address base of EFUSE

Table 26-2 EFUSE Register Description

Name	Description	Reset Value	Address Offset	Access Size
EFUCTRL	EFUSE Control Register	0x00000000	0x0000	32
EFUCFG	EFUSE Configure Register	0x00000000	0x0004	32
EFUSTATE	EFUSE Status Register	0x00????00	0x0008	32
EFUDATA0	EFUSE Data 0 Register	0x????????	0x000C	32
EFUDATA1	EFUSE Data 1 Register	0x00000000	0x0010	32
EFUDATA2	EFUSE Data 2 Register	0x00000000	0x0014	32
EFUDATA3	EFUSE Data 3 Register	0x00000000	0x0018	32
EFUDATA4	EFUSE Data 4 Register	0x00000000	0x001C	32
EFUDATA5	EFUSE Data 5 Register	0x00000000	0x0020	32
EFUDATA6	EFUSE Data 6 Register	0x00000000	0x0024	32
EFUDATA7	EFUSE Data 7 Register	0x00000000	0x0028	32

26.2.2 Registers and Fields Description

26.2.2.1 EFUSE Control Register (EFUCTRL)

	EFUCTRL																BASE + 0x0000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					Address						Reserved		Length			PG_EN	Reserved			RWL	MR	PS	PD	Reserved						WR_EN	RD_EN	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	Writing has no effect, read as zero.	R
26:21	Address	Indicate the start address wants to program or read Aligned to Word	RW
20:19	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

18:16	Length	Indicate the length wants to program or read, efuse operate length equals to this value add 1. Word number(min: 1word, max: 8world, default: 1world)	RW
15	PG_EN	Programming EFUSE enable 1: Enable 0: Disable	RW
14:12	Reserved	Writing has no effect, read as zero.	RW
11	RWL	Redundancy information row select (active high)	RW
10	MR	Read trip point setting: 0: for normal read mode; 1: for margin read1 mode	RW
9	PS	High to pass 1.8V program voltage to internal for program	RW
8	PD	Power down enable (active high)	RW
7	Reserved	Writing has no effect, read as zero.	RW
1	WR_EN	Write data to EFUSE data buffer enable 1: Enable 0: Disable This bit will change to 0 automatically when write procedure done	RW
0	RD_EN	Read data to EFUSE data buffer enable 1: Enable 0: Disable This bit will change to 0 automatically when read procedure done	RW

26.2.2.2 EFUSE Configure Register (EFUCFG)

	EFUCFG																BASE + 0x0004															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INT_EN	Reserved			RD_ADJ				Reserve			RD_STROBE					WR_ADJ				Reserved	WR_STROBE										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	INT_EN	Interrupt enable when read/write EFUSE done. 1: Enable 0: Disable	RW
30:28	Reserved	Writing has no effect, read as zero.	R
27:24	RD_ADJ	Adjust number of h2clk cycles when EFUSE reading unsigned value, h2clk period multiply (RD_ADJ + 1) should greater than 4 ns.	RW
23:21	Reserved	Writing has no effect, read as zero.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

20:16	RD_STROBE	Adjust number of h2clk cycles when EFUSE reading STROBE Signed value, h2clk period multiply(RD_ADJ +RD_STROBE+30) should greater than 100 ns.	RW
15:12	WR_ADJ	Adjust number of h2clk cycles when EFUSE programming unsigned value, h2clk period multiply (WR_ADJ + 1) should greater than 4 ns.	RW
11	Reserved	Writing has no effect, read as zero.	RW
10:0	WR_STROBE	Adjust number of h2clk cycles when EFUSE programming STROBE Signed value, h2clk period multiply(WR_ADJ + 3000 + WR_STROBE) should between 11us and 13us, typical 12us	RW

26.2.2.3 EFUSE Status Register (EFUSTATE)

	EFUSTATE																BASE + 0x0008													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								NKU1_PRT	NKU0_PRT	USERKEY	CHIPKEY	HIDEBLK	SOCINFO	TRM2_PR	TRM1_PR	TRM0_PR	CUT2_PRT	CUT1_PRT	CUT0_PRT	CHIP_PRT	SEC_PRT	DIS_JTAG	SCBT_EN	Reserved						WR_DONE	RD_DONE
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
30:24	Reserved	Writing has no effect, read as zero.	R
23	NKU_PRT	NKU segment write protect 1: protect, this segment can't write 0: no protect, this segment can write	R
22	USERKEY1	User key 1 segment write protect 1: protect, this segment can't write 0: no protect, this segment can write	R
21	USERKEY0	User key 0 segment write protect 1: protect, this segment can't write 0: no protect, this segment can write	R
20	CHIPKEY	Chip key segment write protect 1: protect, this segment can't write 0: no protect, this segment can write	R
19	HIDEBLK	hideblk segment write protect 1: protect, this segment can't write 0: no protect, this segment can write	R
18	SOCINFO	socinfo segment write protect 1: protect, this segment can't write 0: no protect, this segment can write	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

17	TRIM2_PRT	Trim2 segment write protect bit 1: protect, this segment can't write 0: no protect, this segment can write	R
16	TRIM1_PRT	Trim1 segment write protect bit 1: protect, this segment can't write 0: no protect, this segment can write	R
15	TRIM0_PRT	Trim0 segment write protect bit 1: protect, this segment can't write 0: no protect, this segment can write	R
14	CUSTID2_PRT	Customer ID segment write protect bit 1: protect, this segment can’t write 0: no protect, this segment can write	R
13	CUSTID1_PRT	Customer ID segment write protect bit 1: protect, this segment can’t write 0: no protect, this segment can write	R
12	CUSTID0_PRT	Customer ID segment write protect bit 1: protect, this segment can’t write 0: no protect, this segment can write	R
11	CHIPID_PRT	CHIP ID segment protect bit 1: protect, this segment can’t write 0: no protect, this segment can write	R
10	SECBOOT_PRT	Security boot enable protect bit 1: protect, security boot enable can write 0: no protect, security boot enable can't write	R
9	DIS_JTAG	Disable JTAG 1: disable JTAG 0: enable JTAG	R
8	SECBOOT_EN	Security boot enable 1: enable Security boot 0: Normal boot	R
7:2	Reserved	Writing has no effect, read as zero.	RW
1	WR_DONE	Write data to EFUSE operate done flag 1: done 0: not done *This bit only can write to 0, and write to 0 will clear this flag.	RW
0	RD_DONE	Read EFUSE data operate done flag 1: done 0: not done *This bit only can write to 0, and write to 0 will clear this flag	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

26.2.2.4 EFUSE Data Register (EFUDATAn)

	EFUDATAn (n=0,1,2,3,4,5,6,7)																BASE + 0x000C ~ BASE + 0x0028															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DATA	EFUSE DATA register. *EFUSE DATA0 register mapped low operate address, others mapped increased address.	RW

NOTE:

1. The EFUSE 2K bits are mapped to chip memory address, from 0x13540200 to 0x135402FF.
2. The EFUSE 2K programmable bits are separated into fourteen segments as below table.

The first Segment used to store Ingenic chip id, second to forth segment used to store customer id, fifth to seventh segment reserved to store trim data, eighth segment store ingenic chip information，ninth store segment protect bit, tenth segment store hide block，eleventh used to store chip key, twelfth and thirteenth segment used to store user key, last segment used to store NKU.

Segment	1	2	3	4	5	6	7	8	9
Function	CHIPID	CUTID0	CUTID1	CUTID2	TRIM0	TRIM1	TRIM2	SOC INFO	PRT
Mapped Address	200 | 210	211 | 221	222 | 23E	23F | 25B	25C | 260	261 | 265	266 | 26A	26B | 26F	270 | 273
Aligned (Word)	0 | 4	4 | 8	8 | F	F | 16	17 | 18	18 | 19	19 | 1A	1A | 1B	1C | 1C
Bits	128+8	128+8	216+16	216+16	32+8	32+8	32+8	32+8	16+16

Segment	10	11	12	13	14
Function	HIDEBLK	CHIPKEY	USERKEY0	USERKEY1	NKU
Mapped Address	274 | 277	278 | 299	29A | 2BB	2BC | 2DD	2DE | 2FF
Aligned (Word)	1D | 1D	1E | 26	26 | 2E	2F | 37	37 | 3F
Bits	16+16	256+16	256+16	256+16	256+16

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3. The protect bit segment store others segment write protect bit, if protect bit programmed to 1, corresponding segment can not be able to program. The protect bit map as below table

	Bit	Mapped To EFUSE Status Register
The Protect bit Segment	15	NKU_PRT
	14	USERKEY1_PRT
	13	USERKEY0_PRT
	12	CHIPKEY_PRT
	11	HIDEBLK_PRT
	10	SOCINFO_PRT
	9	TRIM2_PRT
	8	TRIM1_PRT
	7	TRIM0_PRT
	6	CUSTID2_PRT
	5	CUSTID1_PRT
	4	CUSTID0_PRT
	3	CHIPID_PRT
	2	SECBOOT_PRT
	1	DISJTAG
	0	SECBOOT_EN

4. The EFUSE can read or write maximum 256bit in each time, but we strongly recommend operate each segment separately.

5. The segment(Chip key/User key/User key1/NKU) can only read/write by SC-ROM.

6. PS=H, PD=H state is not allowed to avoid unintended program

7. must set PS=L except in program mode.

8. must set PD=L except power-down mode

9. Must enter the redundancy read mode and read the RIR data once prior to the array read mode after power-up(PD rising, 1->0) even if repairing is not needed. Redundancy read requires set EFUCTRL.addr = 0x1F, EFUCTRL.length = 1 to read out the complete repairing information. The data will be stored in registers and will remain there until power-down or power-off. In subsequent array read, when read access the failure bit in the main array, the corresponding output data will be corrected automatically .

26.3 Operation Mode

Mode	RD_EN	WR_EN	PG_EN	RWL	MR	PS	PD
Array Normal Read	1	0	1	0	0	0	0
Array Normal Program	0	1	0	0	0	1	0
Array Margin Read	1	0	1	0	1	0	0
Redundant Margin Read	1	0	1	1	1	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Redundant Read	1	0	1	1	0	0	0
Redundant Program	0	1	0	1	0	1	0
Standby Mode	0	0	X	X	X	0	0
Power-down Mode	0	0	X	X	X	0	1

26.4 Flow

26.4.1 Program EFUSE Flow

1. Set EFUCFG register(reading and programming timing).
2. Write want program data to EFUSE data buffer 0-7 registers.
3. Set control register, indicate want to program address, data length.
4. Write control register PD bit to 0.
5. Write control register PS bit to 1, and set MR/RSB/RWL to correspond mode.
6. Write control register PG_EN bit to 1.
7. Connect AVDEFUSE pin to 1.8V.
8. Write control register WR_EN bit to 1.
9. Wait status register WR_DONE set to 1.
10. Disconnect AVDEFUSE pin from 1.8V.
11. Write control register PG_EN bit to 0.
12. Write control register PS bit to 0.
13. Write control register PD bit to 1.

26.4.2 Program Security Key Flow

1. Set EFUCFG register(reading and programming timing).
2. Write control register PD bit to 0.
3. Write control register PS bit to 1, and set MR/RSB/RWL to correspond mode.
4. Write control register PG_EN bit to 1
5. Connect AVDEFUSE pin to 1.8V
6. Invoke SC-ROM controller to write data to Security key mapped address
7. Wait status register WR_DONE set to 1
8. jump to step 6, program all data like this
9. Disconnect AVDEFUSE pin from 1.8V.
10. Write control register PG_EN bit to 0.
11. Write control register PS bit to 0.
12. Write control register PD bit to 1.

NOTE:

*[1]: Do NOT pre-charge AVDEFUSE too early before EFUSE program started.

The maximum 1.8V supply time to AVDEFUSE must be strictly controlled less than 200 millisecond.

Use on-chip counter and GPIO to coordinate external supply source.

*[2]: Only the 1.4.2 flow can be used to program the User Key and NKU Segment, The Chip key

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Segment will be programmed at CP by Ingenic, other segments only can program use 1.4.1 flow.

*[3]: The SC-ROM Controller can write Key segment 32bits once time.

26.4.3 Read EFUSE Flow

1. Set EFUCFG register(reading and programming timing).
2. Set control register to indicate what to read data address, read data length.
3. Write control register PD bit to 0.
4. Set PS/MR/RSB/RWL to correspond read mode.
5. Set read enable register.
6. Wait status register RD_DONE set to 1 or EFUSE interrupted, software application can read EFUSE data buffer 0 – 7 registers.
7. Write control register PD bit to 1.

26.4.4 Read Security Key Flow

1. Invoke SC-ROM controller to read corresponding map address.

NOTE:

*[1]: EFSUE controller will read EFUSE protect bit segment automatically when chip reset, and update the EFUSE state register.

*[2]: Only 1.4.4 flow can be used to read all Keys, other segments only can read use 1.4.3 flow.

*[3]: The SC-ROM Controller can read Keys value 32bits once time.

*[4]: The Redundancy read must be executed after efuse Power-up(PD rising from 0 to 1), and the simply way is don't set PD to 1, but this may increase power consumption

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Section 7

PERIPHERALS

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

27 General-Purpose I/O Ports

27.1 Overview

General Purpose I/O Ports (GPIO) is used in generating and capturing application-specific input and output signals. Each port can be programmed as an output, an input or function port that serves certain peripheral. As input, pull up/down can be enabled/disabled for the port and the port also can be configured as level or edge tripped interrupt source.

27.2 Features

- Each port can be configured as an input, an output or an alternate function port.
- Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering, and every interrupt source can be masked independently.
- Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled.
- GPIO output 5 interrupts, each group had an interrupt to INTC(Interrupt Controller).

27.3 About GPIO Port Summary Table

1) In the GPIO port summary, different pad type will determine different pad characteristics. such as the types of PDWUWCDGRGM_H and PRWHSWCDGSD_H, it just have pull up/down/hi-Z enable , schmitt trigger enable ,drive strength ,slew rate, power-on-start and receiver enable control port.
2) Each Pad can configured as four module function.
3) GROUP E PE31 it's not GPIO port, but it will used with RTC to realize wakeup operate.

Table 27-1 GPIO port summary table illustration

PAD_ID	PAD_TYPE	PULL_RST	SMT_RST	DS_RST	FUNC0	FUNC1	FUNC2	FUNC3
PA00	TYPEA	HIZ	1	0	sd0(io-0)	msc0_d0(io-0)	(i-0)	(i-0)
PA01	TYPEB	PU	0	0	sd2(io-0)	msc0_d1(io-0)	ssi0_dt(io-0)	sfc_dt(io-0)
PA02	TYPEA	PD	1	0	sd2(io-0)	msc0_d2(io-0)	ssi0_dr(io-0)	sfc_dr(io-0)

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Group number	Instance pad type name (different type will decide GPIO function)	Pad pull enable active value. 00: HIZ 01: pull up(PU) 10: pull down(PD) 11: repeater	Pad schmitt trigger enable: 1: schmitt trigger enable. 0: schmitt trigger disnable..	Pad Drive Strength control (please refer to pad drive strength characteristics)	In table, each function column will expression one module port using relationship. such as the pad PA00, the FUNC0 "sd0_(io-0)", "sd0" means the NEMC module data port 0, "io" means function as I/O, "0" means when configure as other functions, GPIO supply value 0 to this function port.

Pad Drive Strength Characteristics for PDWUWCDGRGM_H(TYPEA)

Parameter		Min.	Nom.	Max.	Units
I_{OL} Low Level Output Current @VOL(max)					
	(DS2,DS1,DS0) = 000	4.0	6.3	8.9	mA
	(DS2,DS1,DS0) = 001	6.0	9.4	13.3	mA
	(DS2,DS1,DS0) = 010	8.0	12.5	17.6	mA
	(DS2,DS1,DS0) = 011	9.9	15.5	21.8	mA
	(DS2,DS1,DS0) = 100	11.9	18.6	26.1	mA
	(DS2,DS1,DS0) = 101	13.9	21.6	30.2	mA
	(DS2,DS1,DS0) = 110	15.8	24.5	34.2	mA
	(DS2,DS1,DS0) = 111	17.7	27.4	38.1	mA
I_{OH} High Level Output Current @VOH(min)					
	(DS2,DS1,DS0) = 000	5.9	9.3	14.2	mA
	(DS2,DS1,DS0) = 001	8.8	13.9	21.2	mA
	(DS2,DS1,DS0) = 010	11.7	18.5	28.2	mA
	(DS2,DS1,DS0) = 011	14.6	23.1	35.2	mA
	(DS2,DS1,DS0) = 100	17.5	27.7	42.2	mA
	(DS2,DS1,DS0) = 101	20.3	32.2	49.1	mA
	(DS2,DS1,DS0) = 110	23.2	36.8	56.0	mA
	(DS2,DS1,DS0) = 111	26.1	41.3	62.8	mA

Pad Drive Strength Characteristics for PRWHSWCDGSD_H(TYPEB)

Parameter	Min.	Nom.	Max.	Units

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

I_{OL} Low Level Output Current @VOL(max)				
(DS2,DS1,DS0) = 000	4.5	7.7	11.3	mA
(DS2,DS1,DS0) = 001	6.7	11.4	16.7	mA
(DS2,DS1,DS0) = 010	9.0	15.2	22.1	mA
(DS2,DS1,DS0) = 011	11.2	18.8	27.3	mA
(DS2,DS1,DS0) = 100	13.4	22.6	32.7	mA
(DS2,DS1,DS0) = 101	15.6	26.2	37.8	mA
(DS2,DS1,DS0) = 110	17.7	29.7	42.8	mA
(DS2,DS1,DS0) = 111	19.9	33.2	47.7	mA
I_{OH} High Level Output Current @VOH(min)				
(DS2,DS1,DS0) = 000	2.6	6.3	11.9	mA
(DS2,DS1,DS0) = 001	3.8	9.4	17.7	mA
(DS2,DS1,DS0) = 010	5.1	12.6	23.7	mA
(DS2,DS1,DS0) = 011	6.4	15.7	29.4	mA
(DS2,DS1,DS0) = 100	7.6	18.8	35.2	mA
(DS2,DS1,DS0) = 101	8.9	21.8	40.9	mA
(DS2,DS1,DS0) = 110	10.1	24.9	46.6	mA
(DS2,DS1,DS0) = 111	11.4	27.9	52.2	mA

Pad Drive Strength Characteristics for PRUW08DGZ_H_G(TYPEC) and PRDW08DGZ_H_G(TPYED)

Parameter	Min.	Nom.	Max.	Units
I_{OL} Low Level Output Current @VOL(max)				
	11.1	18.2	25.6	mA
I_{OH} High Level Output Current @VOH(min)				
	13.1	19.1	26.2	mA

Pad Drive Strength Characteristics for PRWHSWCDGSIM_H(TYPEE)

Parameter	Min.	Nom.	Max.	Units
I_{OL} Low Level Output Current @VOL(max)				
(DS1,DS0) = 00	4.5	7.6	11.2	mA
(DS1,DS0) = 01	6.7	11.4	16.6	mA
(DS1,DS0) = 10	8.9	15.1	22.0	mA
(DS1,DS0) = 11	11.1	18.7	27.2	mA
I_{OH} High Level Output Current @VOH(min)				
(DS1,DS0) = 00	2.6	6.3	11.9	mA
(DS1,DS0) = 01	3.8	9.5	17.8	mA
(DS1,DS0) = 10	5.1	12.6	23.7	mA
(DS1,DS0) = 11	6.4	15.7	29.4	mA

Note: 1.TYPEA = PDWUWCDGRGM_H; TYPEB = PRWHSWCDGSD_H.

2. Feature "PULL_RST" means after reset default pull value.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.3.1 GPIO Port A Summary

Table 27-2 GPIO Port A summary

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<PAD_ID>	PAD_MNAME	PAD_TYPE	PULL_RST	SMT_RST	DS_RST	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
PA00		TYPEE	PU	0	0	cim_vic_d0_i(i-0)	uart4_cts__i(i-1)	i2s3_tx_mclk_o(o)	(i-0)
PA01		TYPEE	PU	0	0	cim_vic_d1_i(i-0)	uart4_rts__o(o)	(i-0)	(i-0)
PA02		TYPEE	PU	0	0	cim_vic_d2_i(i-0)	uart4_rxd_i(i-1)	i2s3_tx_lrck(io-0)	(i-0)
PA03		TYPEE	PU	0	0	cim_vic_d3_i(i-0)	uart4_txd_o(o)	i2s3_tx_data0_o(o)	(i-0)
PA04		TYPEE	PU	0	0	cim_vic_d4_i(i-0)	uart5_rxd_i(i-1)	i2s3_tx_data1_o(o)	(i-0)
PA05		TYPEE	PU	0	0	cim_vic_d5_i(i-0)	uart5_txd_o(o)	i2s3_tx_data2_o(o)	(i-0)
PA06		TYPEE	PU	0	0	cim_vic_d6_i(i-0)	uart6_rxd_i(i-1)	i2s3_tx_data3_o(o)	(i-0)
PA07		TYPEE	PU	0	0	cim_vic_d7_i(i-0)	uart6_txd_o(o)	i2s2_rx_mclk_o(o)	(i-0)
PA08		TYPEE	PU	0	0	vic_d8_i(i-0)	uart7_rxd_i(i-1)	(i-0)	(i-0)
PA09		TYPEE	PU	0	0	vic_d9_i(i-0)	uart7_txd_o(o)	i2s2_rx_lrck(io-0)	(i-0)
PA10		TYPEE	PU	0	0	vic_d10_i(i-0)	(i-0)	i2s2_rx_data0_i(i-1)	(i-0)
PA11		TYPEE	PU	0	0	vic_d11_i(i-0)	(i-0)	i2s2_rx_data1_i(i-1)	(i-0)
PA12		TYPEE	PD	0	0	cim_vic_hsync_i(i-0)	(i-0)	i2s2_rx_data2_i(i-1)	(i-0)
PA13		TYPEE	PD	0	0	cim_vic_vsync_i(i-0)	(i-0)	i2s2_rx_data3_i(i-1)	(i-0)
PA14		TYPEE	PD	0	0	cim_vic_pclk_i(i-0)	(i-0)	(i-0)	(i-0)
PA15		TYPEE	PD	0	0	cim_exposure_o(o)	(i-0)	(i-0)	(i-0)
PA16		TYPEE	PU	0	0	i2c3_sck(io-1)	(i-0)	i2s3_tx_bclk(io-0)	(i-0)
PA17		TYPEE	PU	0	0	i2c3_sda(io-1)	(i-0)	i2s2_rx_bclk(io-0)	(i-0)
PA18			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PA19			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PA20			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PA21			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PA22			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PA23			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PA24			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PA25			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PA26			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PA27			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PA28			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PA29			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PA30			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PA31			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)

Note:

1. TYPEA is equal to PDWUWCDGRGM_H.
2. TYPEB is equal to PRWHSWCDGSD_H.
3. TPYEC is equal to PRUW08DGZ_H_G.
4. TPYED is equal to PRDW08DGZ_H_G.
5. TYPEE is equal to PRWHSWCDGSIM_H.

27.3.2 GPIO Port B Summary

Table 27-3 GPIO Port B summary

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

<PAD_ID>	PAD_MNAME	PAD_TYPE	PULL_RST	SMT_RST	DS_RST	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
PB00		TYPEA	PD	0	0	sa0_o(o)	lcd_d0_o(o)	slcd_d0_o(o)	(i-0)
PB01		TYPEA	PD	0	0	sa1_o(o)	lcd_d1_o(o)	slcd_d1_o(o)	(i-0)
PB02		TYPEA	PD	0	0	sa2_o(o)	lcd_d2_o(o)	slcd_d2_o(o)	(i-0)
PB03		TYPEA	PD	0	0	sa3_o(o)	lcd_d3_o(o)	slcd_d3_o(o)	(i-0)
PB04		TYPEA	PD	0	0	sa4_o(o)	lcd_d4_o(o)	slcd_d4_o(o)	(i-0)
PB05		TYPEA	PD	0	0	sa5_o(o)	lcd_d5_o(o)	slcd_d5_o(o)	(i-0)
PB06		TYPEA	PD	0	0	sa6_o(o)	lcd_d6_o(o)	slcd_d6_o(o)	(i-0)
PB07		TYPEA	PD	0	0	sa7_o(o)	lcd_d7_o(o)	slcd_d7_o(o)	(i-0)
PB08		TYPEA	PD	0	0	sa8_o(o)	lcd_d8_o(o)	slcd_d8_o(o)	rgmac1_txd0_o(o)
PB09		TYPEA	PD	0	0	sa9_o(o)	lcd_d9_o(o)	slcd_d9_o(o)	rgmac1_txd1_o(o)
PB10		TYPEA	PD	0	0	sa10_o(o)	lcd_d10_o(o)	slcd_d10_o(o)	rgmac1_txd2_o(o)
PB11		TYPEA	PD	0	0	sa11_o(o)	lcd_d11_o(o)	slcd_d11_o(o)	rgmac1_txd3_o(o)
PB12		TYPEA	PD	0	0	sa12_o(o)	lcd_d12_o(o)	slcd_d12_o(o)	rgmac1_rxd0_i(i-0)
PB13		TYPEA	PU	0	0	rd__o(o)	lcd_d13_o(o)	slcd_d13_o(o)	rgmac1_rxd1_i(i-0)
PB14		TYPEA	PU	0	0	we__o(o)	lcd_d14_o(o)	slcd_d14_o(o)	rgmac1_rxd2_i(i-0)
PB15		TYPEA	PU	0	0	wait__i(i-1)	lcd_d15_o(o)	slcd_d15_o(o)	rgmac1_rxd3_i(i-0)
PB16		TYPEA	PU	0	0	sd0(io-0)	lcd_d16_o(o)	(i-0)	(i-0)
PB17		TYPEA	PU	0	0	sd1(io-0)	lcd_d17_o(o)	(i-0)	rgmac1_tx_en_o(o)
PB18		TYPEA	PU	0	0	sd2(io-0)	lcd_d18_o(o)	(i-0)	rgmac1_rx_dv_i(i-0)
PB19		TYPEA	PU	0	0	sd3(io-0)	lcd_d19_o(o)	(i-0)	rgmac1_mdc_o(o)
PB20		TYPEA	PU	0	0	sd4(io-0)	lcd_d20_o(o)	(i-0)	rgmac1_mdio(io-0)
PB21		TYPEA	PU	0	0	sd5(io-0)	lcd_d21_o(o)	(i-0)	rgmac1_tx_clk_o(o)
PB22		TYPEA	PU	0	0	sd6(io-0)	lcd_d22_o(o)	i2c2_sck(io-1)	rgmac1_rx_clk_i(i-0)
PB23		TYPEA	PU	0	0	sd7(io-0)	lcd_d23_o(o)	i2c2_sda(io-1)	rgmac1_phy_clk_o(o)
PB24		TYPEA	PU	0	0	sd8(io-0)	lcd_pclk_o(o)	slcd_ce__o(o)	(i-0)
PB25		TYPEA	PU	0	0	sd9(io-0)	lcd_vsync_o(o)	slcd_dc_o(o)	(i-0)
PB26		TYPEA	PU	0	0	sd10(io-0)	lcd_hsync_o(o)	slcd_wr_o(o)	(i-0)
PB27		TYPEA	PU	0	0	sd11(io-0)	lcd_de_o(o)	slcd_te_i(i-1)	(i-0)
PB28		TYPEA	PU	0	0	sd12(io-0)	ssi0_ce0__o(o)	(i-0)	uart8_rxd_i(i-1)
PB29		TYPEA	PU	0	0	sd13(io-0)	ssi0_dr_i(i-0)	(i-0)	uart8_txd_o(o)
PB30		TYPEA	PU	0	0	sd14(io-0)	ssi0_dt_o(o)	(i-0)	uart9_rxd_i(i-1)
PB31		TYPEA	PU	0	0	sd15(io-0)	ssi0_clk_o(o)	(i-0)	uart9_txd_o(o)

Note:

1. TYPEA is equal to PDWUWCDGRGM_H.
2. TYPEB is equal to PRWHSWCDGSD_H.
3. TPYEC is equal to PRUW08DGZ_H_G.
4. TPYED is equal to PRDW08DGZ_H_G..
5. TYPEE is equal to PRWHSWCDGSIM_H.

27.3.3 GPIO Port C Summary

Table 27-4 GPIO Port C summary

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<PAD_ID>	PAD_MNAME	PAD_TYPE	PULL_RST	SMT_RST	DS_RST	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
PC00		TYPEA	PD	0	0	pwm0_tcu0_in0(io-0)	(i-0)	(i-0)	(i-0)
PC01		TYPEA	PU	0	0	pwm1_tcu0_in1(io-0)	rgmac0_phy_clk_o(o)	i2s1_rx_mclk_o(o)	uart7_rxd_i(i-1)
PC02		TYPEA	PU	0	0	pwm2_tcu1_in0(io-0)	rgmac0_txd0_o(o)	i2s1_rx_bclk(io-0)	uart7_txd_o(o)
PC03		TYPEA	PU	0	0	pwm3_tcu1_in1(io-0)	rgmac0_txd1_o(o)	i2s1_rx_lrck(io-0)	scc_sck_o(o)
PC04		TYPEA	PU	0	0	pwm4_tcu2_in0(io-0)	rgmac0_txd2_o(o)	i2s1_rx_data_i(i-0)	scc_sda(io-1)
PC05		TYPEA	PU	0	0	pwm5_tcu2_in1(io-0)	rgmac0_txd3_o(o)	i2s1_tx_bclk(io-0)	uart5_rxd_i(i-1)
PC06		TYPEA	PU	0	0	pwm6_tcu3_in0(io-0)	rgmac0_rxd0_i(i-0)	i2s1_tx_lrck(io-0)	uart5_txd_o(o)
PC07		TYPEA	PU	0	0	pwm7_tcu3_in1(io-0)	rgmac0_rxd1_i(i-0)	i2s1_tx_data_o(o)	uart6_rxd_i(i-1)
PC08		TYPEA	PU	0	0	pwm8_tcu4_in0(io-0)	rgmac0_rxd2_i(i-0)	i2s1_tx_mclk_o(o)	uart6_txd_o(o)
PC09		TYPEA	PU	0	0	pwm9_tcu4_in1(io-0)	rgmac0_rxd3_i(i-0)	ssi1_ce0__o(o)	uart4_cts__i(i-1)
PC10		TYPEA	PU	0	0	pwm10_tcu5_in0(io-0)	rgmac0_tx_en_o(o)	ssi1_dr_i(i-0)	uart4_rts__o(o)
PC11		TYPEA	PU	0	0	pwm11_tcu5_in1(io-0)	rgmac0_rx_dv_i(i-0)	ssi1_dt_o(o)	uart4_rxd_i(i-1)
PC12		TYPEA	PU	0	0	pwm12_tcu6_in0(io-0)	rgmac0_mdc_o(o)	ssi1_clk_o(o)	uart4_txd_o(o)
PC13		TYPEA	PU	0	0	pwm13_tcu6_in1(io-0)	rgmac0_mdio(io-0)	spdif_in_i(i-0)	i2c0_sck(io-1)
PC14		TYPEA	PU	0	0	pwm14_tcu7_in0(io-0)	rgmac0_tx_clk_o(o)	spdif_out_o(o)	i2c0_sda(io-1)
PC15		TYPEA	PU	0	0	pwm15_tcu7_in1(io-0)	rgmac0_rx_clk_i(i-0)	cim_vic_mclk_o(o)	(i-0)
PC16			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PC17			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PC18			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PC19			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PC20		TYPEA	PD	0	0	dmic_clk_o(o)	(i-0)	(i-0)	(i-0)
PC21		TYPEA	PU	0	0	dmic_in0_i(i-0)	uart1_cts__i(i-1)	(i-0)	(i-0)
PC22		TYPEA	PU	0	0	dmic_in1_i(i-0)	uart1_rts__o(o)	(i-0)	(i-0)
PC23		TYPEA	PU	0	0	dmic_in2_i(i-0)	uart1_rxd_i(i-1)	i2c1_sck(io-1)	nemc_cs1__o(o)
PC24		TYPEA	PU	0	0	dmic_in3_i(i-0)	uart1_txd_o(o)	i2c1_sda(io-1)	nemc_cs2__o(o)
PC25		TYPEA	PU	0	0	uart3_rxd_i(i-1)	i2c4_sck(io-1)	(i-0)	(i-0)
PC26		TYPEA	PU	0	0	uart3_txd_o(o)	i2c4_sda(io-1)	(i-0)	(i-0)
PC27		TYPEA	PU	0	0	uart3_cts__i(i-1)	i2c5_sck(io-1)	(i-0)	(i-0)
PC28		TYPEA	PU	0	0	uart3_rts__o(o)	i2c5_sda(io-1)	(i-0)	(i-0)
PC29			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PC30			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PC31			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)

Note:

1. TYPEA is equal to PDWUWCDGRGM_H.
2. TYPEB is equal to PRWHSWCDGSD_H.
3. TPYEC is equal to PRUW08DGZ_H_G.
4. TPYED is equal to PRDW08DGZ_H_G..
5. TYPEE is equal to PRWHSWCDGSIM_H.

27.3.4 GPIO Port D Summary

Table 27-5 GPIO Port D summary

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

<PAD ID>	PAD_M NAME	PAD_TY PE	PULL_ RST	SMT_ RST	DS_RS T	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
PD00		TYPEC	PU	0	0	(i-0)	uart3_cts__i(i-1)	i2c4_sck(io-1)	(i-0)
PD01		TYPEC	PU	0	0	(i-0)	uart3_rts__o(o)	i2c4_sda(io-1)	tdo_o(o)
PD02		TYPEC	PU	0	0	(i-0)	uart3_rxd_i(i-1)	pcm_clk(io-0)	tdi_i(i-0)
PD03		TYPEC	PU	0	0	(i-0)	uart3_txd_o(o)	pcm_do_o(o)	tck_i(i-0)
PD04		TYPEC	PU	0	0	(i-0)	i2c5_sck(io-1)	pcm_di_i(i-0)	tms_i(i-0)
PD05		TYPEC	PU	0	0	(i-0)	i2c5_sda(io-1)	pcm_sync(io-0)	(i-0)
PD06			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PD07			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PD08		TYPEC	PU	0	0	sdio_clk_o(o)	ssi0_clk_o(o)	(i-0)	(i-0)
PD09		TYPEC	PU	0	0	sdio_cmd(io-0)	ssi0_dt_o(o)	(i-0)	(i-0)
PD10		TYPEC	PU	0	0	sdio_d0(io-1)	ssi0_dr_i(i-0)	(i-0)	(i-0)
PD11		TYPEC	PU	0	0	sdio_d1(io-1)	i2c1_sck(io-1)	(i-0)	(i-0)
PD12		TYPEC	PU	0	0	sdio_d2(io-1)	i2c1_sda(io-1)	(i-0)	(i-0)
PD13		TYPEC	PU	0	0	sdio_d3(io-1)	ssi0_ce0__o(o)	(i-0)	(i-0)
PD14			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PD15			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PD16			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PD17		TYPEC	PU	0	0	msc0_clk_o(o)	sfc0_clk_o(o)	ssi1_clk_o(o)	(i-0)
PD18		TYPEC	PU	0	0	msc0_cmd(io-0)	sfc0_ce__o(o)	ssi1_dt_o(o)	(i-0)
PD19		TYPEC	PU	0	0	msc0_d0(io-1)	sfc0_dq0(io-0)	ssi1_dr_i(i-0)	(i-0)
PD20		TYPEC	PU	0	0	msc0_d1(io-1)	sfc0_dq1(io-0)	i2c2_sck(io-1)	(i-0)
PD21		TYPEC	PU	0	0	msc0_d2(io-1)	sfc0_dq2_wp_(io-0)	i2c2_sda(io-1)	(i-0)
PD22		TYPEC	PU	0	0	msc0_d3(io-1)	sfc0_dq3_hold_(io-0)	ssi1_ce0__o(o)	(i-0)
PD23		TYPEC	PU	0	0	msc0_d4(io-1)	sfc1_dq0(io-0)	uart0_rxd_i(i-1)	(i-0)
PD24		TYPEC	PU	0	0	msc0_d5(io-1)	sfc1_dq1(io-0)	uart0_txd_o(o)	(i-0)
PD25		TYPEC	PU	0	0	msc0_d6(io-1)	sfc1_dq2_wp_(io-0)	uart0_cts__i(i-1)	(i-0)
PD26		TYPEC	PU	0	0	msc0_d7(io-1)	sfc1_dq3_hold_(io-0)	uart0_rts__o(o)	(i-0)
PD27			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PD28			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PD29			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PD30		TYPEC	PU	0	0	uart2_rxd_i(i-1)	i2c3_sck(io-1)	pwm0_tcu0_in0(io-0)	(i-0)
PD31		TYPEC	PU	0	0	uart2_txd_o(o)	i2c3_sda(io-1)	pwm1_tcu0_in1(io-0)	(i-0)

Note:

1. TYPEA is equal to PDWUWCDGRGM_H.
2. TYPEB is equal to PRWHSWCDGSD_H.
3. TPYEC is equal to PRUW08DGZ_H_G.
4. TPYED is equal to PRDW08DGZ_H_G..
5. TYPEE is equal to PRWHSWCDGSIM_H.

27.3.5 GPIO Port E Summary

Table 27-6 GPIO Port E summary

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<PAD_ID>	PAD_MNAME	PAD_TYPE	PULL_RST	SMT_RST	DS_RST	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
PE00		TYPEB	PU	0	0	msc1_clk_o(o)	pwm2_tcu1_in0(io-0)	(i-0)	(i-0)
PE01		TYPEB	PU	0	0	msc1_cmd(io-0)	pwm3_tcu1_in1(io-0)	(i-0)	(i-0)
PE02		TYPEB	PU	0	0	msc1_d0(io-1)	pwm4_tcu2_in0(io-0)	(i-0)	(i-0)
PE03		TYPEB	PU	0	0	msc1_d1(io-1)	pwm5_tcu2_in1(io-0)	(i-0)	(i-0)
PE04		TYPEB	PU	0	0	msc1_d2(io-1)	pwm6_tcu3_in0(io-0)	(i-0)	(i-0)
PE05		TYPEB	PU	0	0	msc1_d3(io-1)	pwm7_tcu3_in1(io-0)	(i-0)	(i-0)
PE06			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PE07			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PE08			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PE09			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PE10			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PE11			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PE12			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PE13			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PE14			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PE15			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PE16		TYPEA	PU	0	0	sfc0_clk_o(o)	ssi1_clk_o(o)	(i-0)	(i-0)
PE17		TYPEA	PU	0	0	sfc0_ce__o(o)	ssi1_dt_o(o)	(i-0)	(i-0)
PE18		TYPEA	PU	0	0	sfc0_dq0(io-0)	ssi1_dr_i(i-0)	(i-0)	(i-0)
PE19		TYPEA	PU	0	0	sfc0_dq1(io-0)	i2c2_sck(io-1)	(i-0)	(i-0)
PE20		TYPEA	PU	0	0	sfc0_dq2_wp_(io-0)	i2c2_sda(io-1)	(i-0)	(i-0)
PE21		TYPEA	PU	0	0	sfc0_dq3_hold_(io-0)	ssi1_ce0__o(o)	(i-0)	(i-0)
PE22		TYPED	PD	0	0	drv_vbus_o(o)	(i-0)	(i-0)	(i-0)
PE23		TYPED	PD	0	0	rtc32k_o(o)	(i-0)	(i-0)	(i-0)
PE24		TYPED	PD	0	0	exclk_o(o)	cim_vic_mclk_o(o)	(i-0)	(i-0)
PE25	BOOT_SEL0	TYPED	PD	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PE26	BOOT_SEL1	TYPED	PD	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PE27	BOOT_SEL2	TYPED	PD	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PE28			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PE29			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PE30			HIZ	0	0	(i-0)	(i-0)	(i-0)	(i-0)
PE31		TYPEC	PU	0	0	(i-0)	(i-0)	(i-0)	(i-0)

Note:

1. PE25 used as BOOT_SEL0 input during boot.
2. PE26 used as BOOT_SEL1 input during boot.
3. PE27 used as BOOT_SEL2 input during boot.
4. TYPEA is equal to PDWUWCDGRGM_H.
5. TYPEB is equal to PRWHSWCDGSD_H.
6. TPYEC is equal to PRUW08DGZ_H_G.
7. TPYED is equal to PRDW08DGZ_H_G.
8. TYPEE is equal to PRWHSWCDGSIM_H.
9. PE31 is not a gpio-pad. here only be used the function of the PE31 for WKUP special-pad and it

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

used GPIO's logic to realized wakeup interrupt function with RTC module.

27.3.6 GPIO Port Z - Shadow Group

The group is a dummy group which is not mapping to any on-chip ports. It is used to avoid 3rd (intermittent) state error during configuration. Please refer for detailed information.

27.4 Registers Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   - R - Read only
   - W - Write only
   - RW - read and write
   - RCW - read and write, but clear to 0 by read
   - RSW - read and write, but set to 1 by read
   - RWC - read and write, clear to 0 by write 1, write 0 has no effect
   - RWS - read and write, set to 1 by write 1, write 0 has no effect
   - RC - read only, and clear to 0 by read
   - RS - read only, and set to 1 by read
   - SPEC - special access method, relate to its description
3. Reset Value
   - 1 - reset to 1
   - 0 - reset to 0
   - ? - value unknown after reset
4. Not all the register will be use in this chapter, please review the chapter of "Function Overview" for more detail.

Table 27-85. Table 27-8 summarized all memory-mapped registers, which can be programmed to operate GPIO port and alternate function port sharing configuration.

6. All registers are in 32-bits width. Usually, 1 bit in the register affects a corresponding GPIO port and every GPIO port can be operated independently.
7. Gray bits in the register description indicates that this feature in the GPIO group who did not use, program can be ignored.

27.4.1 Register Memory Map

Table 27-7 Registers Memory Map Base Address

Name	Base	Description

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

PA	0x10010000	Address base of GPIO Port A
PB	0x10010100	Address base of GPIO Port B
PC	0x10010200	Address base of GPIO Port C
PD	0x10010300	Address base of GPIO Port D
PE	0x10010400	Address base of GPIO Port E
PZ	0x10010700	Address base of GPIO Group Z (Shadow group)

Table 27-8 GPIO Registers Group Map

Name	RW	Description	Reset Value	Address Offset	Access Size
GPIO PORT A					
PAPINL	R	PORTA PIN Level Register	0x????_????	0x00	32
PAINT	RW	PORTA Interrupt Register	0x0000_0000	0x10	32
PAINTS	W	PORTA Interrupt Set Register	0x0000_0000	0x14	32
PAINTC	W	PORTA Interrupt Clear Register	0x0000_0000	0x18	32
PAMSK	RW	PORTA Interrupt Mask Register	0x0003_FFFF	0x20	32
PAMSKS	W	PORTA Interrupt Mask Set Register	0x0000_0000	0x24	32
PAMSKC	W	PORTA Interrupt Mask Clear Register	0x0000_0000	0x28	32
PAPAT1	RW	PORTA Pattern 1 Register	0x0003_FFFF	0x30	32
PAPAT1S	W	PORTA Pattern 1 Set Register	0x0000_0000	0x34	32
PAPAT1C	W	PORTA Pattern 1 Clear Register	0x0000_0000	0x38	32
PAPAT0	RW	PORTA Pattern 0 Register	0x0000_0000	0x40	32
PAPAT0S	W	PORTA Pattern 0 Set Register	0x0000_0000	0x44	32
PAPAT0C	W	PORTA Pattern 0 Clear Register	0x0000_0000	0x48	32
PAFLG	R	PORTA FLAG Register	0x0000_0000	0x50	32
PAFLGC	RC	PORTA FLAG Clear Register	0x0000_0000	0x58	32
PAEDG	RW	PORTA Dual-Edge Interrupt Register	0x0000_0000	0x70	32
PAEDGS	W	PORTA Dual-Edge Interrupt Set Register	0x0000_0000	0x74	32
PAEDGC	W	PORT A Dual-Edge Interrupt Clear Register	0x0000_0000	0x78	32
PAPU	RW	PORTA PULL-UP enabled State Register	0x0003_0FFF	0x80	32
PAPUS	W	PORTA PULL-UP enabled State Set Register	0x0000_0000	0x84	32
PAPUC	W	PORTA PULL-UP enabled State Clear Register	0x0000_0000	0x88	32
PAPD	RW	PORTA PULL-Down enabled State Register	0x0000_F000	0x90	32
PAPDS	W	PORTA PULL-Down enabled State Set Register	0x0000_0000	0x94	32
PAPDC	W	PORTA PULL-Down enabled State Clear	0x0000_0000	0x98	32

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Register			
PADS0	RW	PORTA Drive Strength Register0	0x0000_0000	0xA0	32
PADS0S	W	PORTA Drive Strength Set Register0	0x0000_0000	0xA4	32
PADS0C	W	PORTA Drive Strength Clear Register0	0x0000_0000	0xA8	32
PADS1	RW	PORTA Drive Strength Register1	0x0000_0000	0xB0	32
PADS1S	W	PORTA Drive Strength Set Register1	0x0000_0000	0xB4	32
PADS1C	W	PORTA Drive Strength Clear Register1	0x0000_0000	0xB8	32
PASR	RW	PORTA Slew Rate Register	0x0000_0000	0xD0	32
PASRS	W	PORTA Slew Rate Set Register	0x0000_0000	0xD4	32
PASRC	W	PORTA Slew Rate Clear Register	0x0000_0000	0xD8	32
PASMT	RW	PORTA Schmitt Trigger Register	0x0000_0000	0xE0	32
PASMTS	W	PORTA Schmitt Trigger Set Register	0x0000_0000	0xE4	32
PASMTC	W	PORTA Schmitt Trigger Clear Register	0x0000_0000	0xE8	32
GPIO PORT B					
PBPINL	R	PORTB PIN Level Register	0x????_????	0x00	32
PBINT	RW	PORTB Interrupt Register	0x0000_0000	0x10	32
PBINTS	W	PORTB Interrupt Set Register	0x0000_0000	0x14	32
PBINTC	W	PORTB Interrupt Clear Register	0x0000_0000	0x18	32
PBMSK	RW	PORTB Interrupt Mask Register	0xFFFF_FFFF	0x20	32
PBMSKS	W	PORTB Interrupt Mask Set Register	0x0000_0000	0x24	32
PBMSKC	W	PORTB Interrupt Mask Clear Register	0x0000_0000	0x28	32
PBPAT1	RW	PORTB Pattern 1 Register	0xFFFF_FFFF	0x30	32
PBPAT1S	W	PORTB Pattern 1 Set Register	0x0000_0000	0x34	32
PBPAT1C	W	PORTB Pattern 1 Clear Register	0x0000_0000	0x38	32
PBPAT0	RW	PORTB Pattern 0 Register	0x0000_0000	0x40	32
PBPAT0S	W	PORTB Pattern 0 Set Register	0x0000_0000	0x44	32
PBPAT0C	W	PORTB Pattern 0 Clear Register	0x0000_0000	0x48	32
PBFLG	R	PORTB FLAG Register	0x0000_0000	0x50	32
PBFLGC	RC	PORTB FLAG Clear Register	0x0000_0000	0x58	32
PBEDG	RW	PORTB Dual-Edge Interrupt Register	0x0000_0000	0x70	32
PBEDGS	W	PORTB Dual-Edge Interrupt Set Register	0x0000_0000	0x74	32
PBEDGC	W	PORTB Dual-Edge Interrupt Clear Register	0x0000_0000	0x78	32
PBPU	RW	PORTB PULL-UP enabled State Register	0xFFFF_E000	0x80	32
PBPUS	W	PORTB PULL-UP enabled State Set Register	0x0000_0000	0x84	32
PBPUC	W	PORTB PULL-UP enabled State Clear Register	0x0000_0000	0x88	32
PBPD	RW	PORTB PULL-Down enabled State Register	0x0000_1FFF	0x90	32
PBPDS	W	PORTB PULL-Down enabled State Set Register	0x0000_0000	0x94	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

PBPDC	W	PORTB PULL-Down enabled State Clear Register	0x0000_0000	0x98	32
PBDS0	RW	PORTB Drive Strength Register0	0x0000_0000	0xA0	32
PBDS0S	W	PORTB Drive Strength Set Register0	0x0000_0000	0xA4	32
PBDS0C	W	PORTB Drive Strength Clear Register0	0x0000_0000	0xA8	32
PBDS1	RW	PORTB Drive Strength Register1	0x0000_0000	0xB0	32
PBDS1S	W	PORTB Drive Strength Set Register1	0x0000_0000	0xB4	32
PBDS1C	W	PORTB Drive Strength Clear Register1	0x0000_0000	0xB8	32
PBDS2	RW	PORTB Drive Strength Register2	0x0000_0000	0xC0	32
PBDS2S	W	PORTB Drive Strength Set Register2	0x0000_0000	0xC4	32
PBDS2C	W	PORTB Drive Strength Clear Register2	0x0000_0000	0xC8	32
PBSR	RW	PORTB Slew Rate Register	0x0000_0000	0xD0	32
PBSRS	W	PORTB Slew Rate Set Register	0x0000_0000	0xD4	32
PBSRC	W	PORTB Slew Rate Clear Register	0x0000_0000	0xD8	32
PBSMT	RW	PORTB Schmitt Trigger Register	0x0000_0000	0xE0	32
PBSMTS	W	PORTB Schmitt Trigger Set Register	0x0000_0000	0xE4	32
PBSMTC	W	PORTB Schmitt Trigger Clear Register	0x0000_0000	0xE8	32
GPIO PORT C					
PCPINL	R	PORTC PIN Level Register	0x????_????	0x00	32
PCINT	RW	PORTC Interrupt Register	0x0000_0000	0x10	32
PCINTS	W	PORTC Interrupt Set Register	0x0000_0000	0x14	32
PCINTC	W	PORTC Interrupt Clear Register	0x0000_0000	0x18	32
PCMSK	RW	PORTC Interrupt Mask Register	0x1FF0_FFFF	0x20	32
PCMSKS	W	PORTC Interrupt Mask Set Register	0x0000_0000	0x24	32
PCMSKC	W	PORTC Interrupt Mask Clear Register	0x0000_0000	0x28	32
PCPAT1	RW	PORTC Pattern 1 Register	0x1FF0_FFFF	0x30	32
PCPAT1S	W	PORTC Pattern 1 Set Register	0x0000_0000	0x34	32
PCPAT1C	W	PORTC Pattern 1 Clear Register	0x0000_0000	0x38	32
PCPAT0	RW	PORTC Pattern 0 Register	0x0000_0000	0x40	32
PCPAT0S	W	PORTC Pattern 0 Set Register	0x0000_0000	0x44	32
PCPAT0C	W	PORTC Pattern 0 Clear Register	0x0000_0000	0x48	32
PCFLG	R	PORTC FLAG Register	0x0000_0000	0x50	32
PCFLGC	RC	PORTC FLAG Clear Register	0x0000_0000	0x58	32
PCEDG	RW	PORTC Dual-Edge Interrupt Register	0x0000_0000	0x70	32
PCEDGS	W	PORTC Dual-Edge Interrupt Set Register	0x0000_0000	0x74	32
PCEDGC	W	PORTC Dual-Edge Interrupt Clear Register	0x0000_0000	0x78	32
PCPU	RW	PORTC PULL-UP enabled State Register	0x1F10_FFFE	0x80	32
PCPUS	W	PORTC PULL-UP enabled State Set Register	0x0000_0000	0x84	32
PCPUC	W	PORTC PULL-UP enabled State Clear Register	0x0000_0000	0x88	32

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

PCPD	RW	PORTC PULL-Down enabled State Register	0x0010_0001	0x90	32
PCPDS	W	PORTC PULL-Down enabled State Set Register	0x0000_0000	0x94	32
PCPDC	W	PORTC PULL-Down enabled State Clear Register	0x0000_0000	0x98	32
PCDS0	RW	PORTC Drive Strength Register0	0x0000_0000	0xA0	32
PCDS0S	W	PORTC Drive Strength Set Register0	0x0000_0000	0xA4	32
PCDS0C	W	PORTC Drive Strength Clear Register0	0x0000_0000	0xA8	32
PCDS1	RW	PORTC Drive Strength Register1	0x0000_0000	0xB0	32
PCDS1S	W	PORTC Drive Strength Set Register1	0x0000_0000	0xB4	32
PCDS1C	W	PORTC Drive Strength Clear Register1	0x0000_0000	0xB8	32
PCDS2	RW	PORTC Drive Strength Register2	0x0000_0000	0xC0	32
PCDS2S	W	PORTC Drive Strength Set Register2	0x0000_0000	0xC4	32
PCDS2C	W	PORTC Drive Strength Clear Register2	0x0000_0000	0xC8	32
PCSR	RW	PORTC Slew Rate Register	0x0000_0000	0xD0	32
PCSRS	W	PORTC Slew Rate Set Register	0x0000_0000	0xD4	32
PCSRC	W	PORTC Slew Rate Clear Register	0x0000_0000	0xD8	32
PCSMT	RW	PORTC Schmitt Trigger Register	0x0000_0000	0xE0	32
PCSMTS	W	PORTC Schmitt Trigger Set Register	0x0000_0000	0xE4	32
PCSMTC	W	PORTC Schmitt Trigger Clear Register	0x0000_0000	0xE8	32
GPIO PORT D					
PDPINL	R	PORTD PIN Level Register	0x????_????	0x00	32
PDINT	RW	PORTD Interrupt Register	0x0000_0000	0x10	32
PDINTS	W	PORTD Interrupt Set Register	0x0000_0000	0x14	32
PDINTC	W	PORTD Interrupt Clear Register	0x0000_0000	0x18	32
PDMSK	RW	PORTD Interrupt Mask Register	0xC7FE_3F21	0x20	32
PDMSKS	W	PORTD Interrupt Mask Set Register	0x0000_0000	0x24	32
PDMSKC	W	PORTD Interrupt Mask Clear Register	0x0000_0000	0x28	32
PDPAT1	RW	PORTD Pattern 1 Register	0xC7F1_3F3F	0x30	32
PDPAT1S	W	PORTD Pattern 1 Set Register	0x0000_0000	0x34	32
PDPAT1C	W	PORTD Pattern 1 Clear Register	0x0000_0000	0x38	32
PDPAT0	RW	PORTD Pattern 0 Register	0x0000_001E	0x40	32
PDPAT0S	W	PORTD Pattern 0 Set Register	0x0000_0000	0x44	32
PDPAT0C	W	PORTD Pattern 0 Clear Register	0x0000_0000	0x48	32
PDFLG	R	PORTD FLAG Register	0x0000_0000	0x50	32
PDFLGC	RC	PORTD FLAG Clear Register	0x0000_0000	0x58	32
PDEDG	RW	PORTD Dual-Edge Interrupt Register	0x0000_0000	0x70	32
PDEDGS	W	PORTD Dual-Edge Interrupt Set Register	0x0000_0000	0x74	32
PDEDGC	W	PORTD Dual-Edge Interrupt Clear Register	0x0000_0000	0x78	32
PDPU	RW	PORTD PULL-UP-DOWN enabled State	0x0000_0000	0x80	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Register			
PDPUS	W	PORTD PULL-UP-DOWN enabled State Set Register	0x0000_0000	0x84	32
PDPUC	W	PORTD PULL-UP-DOWN enabled State Clear Register	0x0000_0000	0x88	32
GPIO PORT E					
PEPINL	R	PORTE PIN Level Register	0x????_????	0x00	32
PEINT	RW	PORTE Interrupt Register	0x0000_0000	0x10	32
PEINTS	W	PORTE Interrupt Set Register	0x0000_0000	0x14	32
PEINTC	W	PORTE Interrupt Clear Register	0x0000_0000	0x18	32
PEMSK	RW	PORTE Interrupt Mask Register	0x8FFF_003F	0x20	32
PEMSKS	W	PORTE Interrupt Mask Set Register	0x0000_0000	0x24	32
PEMSKC	W	PORTE Interrupt Mask Clear Register	0x0000_0000	0x28	32
PEPAT1	RW	PORTE Pattern 1 Register	0x8FFF_003F	0x30	32
PEPAT1S	W	PORTE Pattern 1 Set Register	0x0000_0000	0x34	32
PEPAT1C	W	PORTE Pattern 1 Clear Register	0x0000_0000	0x38	32
PEPAT0	RW	PORTE Pattern 0 Register	0x0000_0000	0x40	32
PEPAT0S	W	PORTE Pattern 0 Set Register	0x0000_0000	0x44	32
PEPAT0C	W	PORTE Pattern 0 Clear Register	0x0000_0000	0x48	32
PEFLG	R	PORTE FLAG Register	0x0000_0000	0x50	32
PEFLGC	RC	PORTE FLAG Clear Register	0x0000_0000	0x58	32
PEEDG	RW	PORTE Dual-Edge Interrupt Register	0x0000_0000	0x70	32
PEEDGS	W	PORTE Dual-Edge Interrupt Set Register	0x0000_0000	0x74	32
PEEDGC	W	PORTE Dual-Edge Interrupt Clear Register	0x0000_0000	0x78	32
PEPU	RW	PORTE PULL-UP enabled State Register	0x003F_003F	0x80	32
PEPUS	W	PORTE PULL-UP enabled State Set Register	0x0000_0000	0x84	32
PEPUC	W	PORTE PULL-UP enabled State Clear Register	0x0000_0000	0x88	32
PEPD	RW	PORTE PULL-Down enabled State Register	0x0000_0000	0x90	32
PEPDS	W	PORTE PULL-Down enabled State Set Register	0x0000_0000	0x94	32
PEPDC	W	PORTE PULL-Down enabled State Clear Register	0x0000_0000	0x98	32
PEDS0	RW	PORTE Drive Strength Register0	0x0000_0000	0xA0	32
PEDS0S	W	PORTE Drive Strength Set Register0	0x0000_0000	0xA4	32
PEDS0C	W	PORTE Drive Strength Clear Register0	0x0000_0000	0xA8	32
PEDS1	RW	PORTE Drive Strength Register1	0x0000_0000	0xB0	32
PEDS1S	W	PORTE Drive Strength Set Register1	0x0000_0000	0xB4	32
PEDS1C	W	PORTE Drive Strength Clear Register1	0x0000_0000	0xB8	32

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

PEDS2	RW	PORTE Drive Strength Register2	0x0000_0000	0xC0	32
PEDS2S	W	PORTE Drive Strength Set Register2	0x0000_0000	0xC4	32
PEDS2C	W	PORTE Drive Strength Clear Register2	0x0000_0000	0xC8	32
PESR	RW	PORTE Slew Rate Register	0x0000_0000	0xD0	32
PESRS	W	PORTE Slew Rate Set Register	0x0000_0000	0xD4	32
PESRC	W	PORTE Slew Rate Clear Register	0x0000_0000	0xD8	32
PESMT	RW	PORTE Schmitt Trigger Register	0x0000_0000	0xE0	32
PESMTS	W	PORTE Schmitt Trigger Set Register	0x0000_0000	0xE4	32
PESMTC	W	PORTE Schmitt Trigger Clear Register	0x0000_0000	0xE8	32
Shadow Register Group PZ					
PzINTS	W	Shadow Interrupt Set Register	0x0000_0000	0x0014	32
PzINTC	W	Shadow Interrupt Clear Register	0x0000_0000	0x0018	32
PzMSKS	W	Shadow Interrupt Mask Set Register	0x0000_0000	0x0024	32
PzMSKC	W	Shadow Interrupt Mask Clear Register	0x0000_0000	0x0028	32
PzPAT1S	W	Shadow Interrupt Pattern 1 Set Register	0x0000_0000	0x0034	32
PzPAT1C	W	Shadow Interrupt Pattern 1 Clear Register	0x0000_0000	0x0038	32
PzPAT0S	W	Shadow Interrupt Pattern 0 Set Register	0x0000_0000	0x0044	32
PzPAT0C	W	Shadow Interrupt Pattern 0 Clear Register	0x0000_0000	0x0048	32
PzGID2LD	W	PORT Group ID to be load from PZ Register	0x0000_0000	0x00F0	32

Note: 1. Pz* in the description of register is use for shadow operation for other groups, more details will description as follow chapters.

27.4.2 Register and Fields Description

27.4.3 PORT PIN Level Registers (PxPINL,0x0000)

PAPINL,PBPINL,PCPINL,PDPINL and PEPINL are Five 32-bit PORT PIN level registers. They are read-only registers.

	PxPINL																Base + 0x0000													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PINL31	PINL30	PINL29	PINL28	PINL27	PINL26	PINL25	PINL24	PINL23	PINL22	PINL21	PINL20	PINL19	PINL18	PINL17	PINL16	PINL15	PINL14	PINL13	PINL12	PINL11	PINL10	PINL09	PINL08	PINL07	PINL06	PINL05	PINL04	PINL03	PINL02	PINL01	PINL00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	PINL n	Where n = 0 ~ 31 and PBPINL n = PBPINL0 ~ PBPINL31. The PORTB PIN level can be read by reading PINL n bit in register	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		PBPINL.	

Note: 1. In the table, "x" represents the group A,B,C,D and E behind the description of similar.

27.4.4 PORT Interrupt Registers (PxINT,0x0010)

PAINT,PBINT,PCINT,PDINT and PEINT are five 32-bit PORT interrupt registers.

	PxINT																Base + 0x0010													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INT31	INT30	INT29	INT28	INT27	INT26	INT25	INT24	INT23	INT22	INT21	INT20	INT19	INT18	INT17	INT16	INT15	INT14	INT13	INT12	INT11	INT10	INT09	INT08	INT07	INT06	INT05	INT04	INT03	INT02	INT01	INT00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	INT n	Where n = 0 ~ 31 and INT n = INT31 ~ INT00. Interrupt enable. 0: Corresponding pin is used as device functions or normal gpio 1: Corresponding pin is used as interrupt	RW

27.4.5 PORT Interrupt Set Registers (PxINTS,0x0014)

PAINTS,PBINTS,PCINTS,PDINTS and PEINTS are five 32-bit PORT interrupt set registers.

	PxINTS																Base + 0x0014													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTS31	INTS30	INTS29	INTS28	INTS27	INTS26	INTS25	INTS24	INTS23	INTS22	INTS21	INTS20	INTS19	INTS18	INTS17	INTS16	INTS15	INTS14	INTS13	INTS12	INTS11	INTS10	INTS09	INTS08	INTS07	INTS06	INTS05	INTS04	INTS03	INTS02	INTS01	INTS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	INTS n	Writing 1 to INTS n will set INT n to 1 in register PBINT. Writing 0 to INTS n will no use.	W

27.4.6 PORT Interrupt Clear Registers (PxINTC,0x0018)

PAINTC,PBINTC,PCINTC,PDINTC and PEINTC are five 32-bit PORT interrupt clear registers.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	PxINTC																														Base + 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTC31	INTC30	INTC29	INTC28	INTC27	INTC26	INTC25	INTC24	INTC23	INTC22	INTC21	INTC20	INTC19	INTC18	INTC17	INTC16	INTC15	INTC14	INTC13	INTC12	INTC11	INTC10	INTC09	INTC08	INTC07	INTC06	INTC05	INTC04	INTC03	INTC02	INTC01	INTC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	INTC n	Writing 1 to INTC n will set INT n to 0 in register PxINT. Writing 0 to INTC n will no use.	W

27.4.7 PORT Mask Registers (PxMSK,0x0020)

PAMSK,PBMSK,PCMSK,PDMSK and PEMSK are five 32-bit PORT mask registers.

	PxMSK																														Base + 0x0020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSK31	MSK30	MSK29	MSK28	MSK27	MSK26	MSK25	MSK24	MSK23	MSK22	MSK21	MSK20	MSK19	MSK18	MSK17	MSK16	MSK15	MSK14	MSK13	MSK12	MSK11	MSK10	MSK09	MSK08	MSK07	MSK06	MSK05	MSK04	MSK03	MSK02	MSK01	MSK00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	MSK n	Where n = 0 ~ 31 and MSK n = MSK31 ~ MSK0. When INT n = 1: 0: Enable the pin as an interrupt source 1: Disable the pin as an interrupt source When INT n = 0: 0: Corresponding pin will be used as device function 1: Corresponding pin will be used as gpio	RW

Note:

1. Not every PBD support Input Enable Control, please check out Function Overview chapter for details.

27.4.8 PORT Mask Set Registers (PxMSKS,0x0024)

PAMSKS,PBMSKS,PCMSKS,PDMSKS and PEMSKS are five 32-bit PORT mask set registers.

	PxMSKS	Base + 0x0024

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKS31	MSKS30	MSKS29	MSKS28	MSKS27	MSKS26	MSKS25	MSKS24	MSKS23	MSKS22	MSKS21	MSKS20	MSKS19	MSKS18	MSKS17	MSKS16	MSKS15	MSKS14	MSKS13	MSKS12	MSKS11	MSKS10	MSKS09	MSKS08	MSKS07	MSKS06	MSKS05	MSKS04	MSKS03	MSKS02	MSKS01	MSKS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	MSKS n	Writing 1 to MSKS n will set MSK n to 1 in register PxMSK. Writing 0 to MSKS n will no use.	W

27.4.9 PORT Mask Clear Registers (PxMSKC,0x0028)

PAMSKC,PBMSKC,PCMSKC,PDMSKC and PEMSKC are five 32-bit PORT mask clear registers.

	PxMSKC																															Base + 0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKC31	MSKC30	MSKC29	MSKC28	MSKC27	MSKC26	MSKC25	MSKC24	MSKC23	MSKC22	MSKC21	MSKC20	MSKC19	MSKC18	MSKC17	MSKC16	MSKC15	MSKC14	MSKC13	MSKC12	MSKC11	MSKC10	MSKC09	MSKC08	MSKC07	MSKC06	MSKC05	MSKC04	MSKC03	MSKC02	MSKC01	MSKC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	MSKC n	Writing 1 to MSKC n will set MSK n to 0 in register PxMSK. Writing 0 to MSKC n will no use.	W

27.4.10 PORT PAT1/Direction Registers (PxPAT1,0x0030)

PAPAT1,PBPAT1,PCPAT1,PDPAT1 and PEPAT1 are five 32-bit PORT Pattern1/direction registers.

	PxPAT1																															Base + 0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT131	PAT130	PAT129	PAT128	PAT127	PAT126	PAT125	PAT124	PAT123	PAT122	PAT121	PAT120	PAT119	PAT118	PAT117	PAT116	PAT115	PAT114	PAT113	PAT112	PAT111	PAT110	PAT109	PAT108	PAT107	PAT106	PAT105	PAT104	PAT103	PAT102	PAT101	PAT100
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	PAT1 n	Where n = 0 ~ 31 and PAT1 n = PAT131 ~ PAT10. When INT n = 1 (Interrupt function): 0: Level trigger interrupt 1: Edge trigger interrupt When INT n = 0 and MSK = 0 (Device function):	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: Corresponding pin is used as device 0 or device 1 function 1: Corresponding pin is used as device 2 or device 3 function When INT n = 0 and MSK = 1 (GPIO function): 0: Corresponding pin is used as gpio output 1: Corresponding pin is used as gpio input	

Note:

1. Not every PBD support Input Enable Control, please check out Function Overview chapter for details.

27.4.11 PORT PAT1/Direction Set Registers (PxPAT1S,0x0034)

PAPAT1S,PBPAT1S,PCPAT1S,PDPAT1S and PEPAT1S are five 32-bit PORT Pattern1 or direction set registers.

	PxPAT1S																Base + 0x0034													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT1S31	PAT1S30	PAT1S29	PAT1S28	PAT1S27	PAT1S26	PAT1S25	PAT1S24	PAT1S23	PAT1S22	PAT1S21	PAT1S20	PAT1S19	PAT1S18	PAT1S17	PAT1S16	PAT1S15	PAT1S14	PAT1S13	PAT1S12	PAT1S11	PAT1S10	PAT1S09	PAT1S08	PAT1S07	PAT1S06	PAT1S05	PAT1S04	PAT1S03	PAT1S02	PAT1S01	PAT1S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PAT1S n	Writing 1 to PAT1S n will set PAT1 n to 1 in register PxPAT1. Writing 0 to PAT1S n will no use.	W

27.4.12 PORT PAT1/Direction Clear Registers (PxPAT1C,0x0038)

PAPAT1C,PBPAT1C,PCPAT1C,PDPAT1C and PEPAT1C are five 32-bit PORT Pattern1 or direction clear registers.

	PxPAT1S,																Base + 0x0038													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT1C31	PAT1C30	PAT1C29	PAT1C28	PAT1C27	PAT1C26	PAT1C25	PAT1C24	PAT1C23	PAT1C22	PAT1C21	PAT1C20	PAT1C19	PAT1C18	PAT1C17	PAT1C16	PAT1C15	PAT1C14	PAT1C13	PAT1C12	PAT1C11	PAT1C10	PAT1C09	PAT1C08	PAT1C07	PAT1C06	PAT1C05	PAT1C04	PAT1C03	PAT1C02	PAT1C01	PAT1C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PAT1C n	Writing 1 to PAT1C n will set PAT1 n to 0 in register PxPAT1. Writing 0 to PAT1C n will no use.	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.4.13 PORT PAT0/Data Registers (PxPAT0,0x0040)

PAPAT0,PBPAT0,PCPAT0,PDPAT0 and PEPAT0 are five 32-bit PORT Pattern0 or data registers.

	PxPAT0,																Base + 0x0040															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT031	PAT030	PAT029	PAT028	PAT027	PAT026	PAT025	PAT024	PAT023	PAT022	PAT021	PAT020	PAT019	PAT018	PAT017	PAT016	PAT015	PAT014	PAT013	PAT012	PAT011	PAT010	PAT009	PAT008	PAT007	PAT006	PAT005	PAT004	PAT003	PAT002	PAT001	PAT000
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	PAT0 n	Where n = 0 ~ 31 and PAT0 n = PAT00 ~ PAT031. When INTn = 1 and PAT1 = 0: 0: Port is low level triggered interrupt input 1: Port is high level triggered interrupt input When INTn = 1 and PAT1 = 1: 0: Port is falling edge triggered interrupt input 1: Port is rising edge triggered interrupt input When INTn = 0 and MSK = 0 and PAT1 = 0: 0: Port is pin of device 0 1: Port is pin of device 1 When INTn = 0 and MSK = 0 and PAT1 = 1: 0: Port is pin of device 2 1: Port is pin of device 3 When INTn = 0 and MSK = 1 and PAT1 = 0: 0: Port is GPIO output 0 1: Port is GPIO output 1	RW

Note:

1. Not every PBD support Input Enable Control, please check out Function Overview chapter for details.

27.4.14 PORT PAT0/Data Set Registers (PxPAT0S,0x0044)

PAPAT0S,PBPAT0S,PCPAT0S,PDPAT0S and PEPAT0S are five 32-bit PORT Pattern0 or data set registers.

	PxPAT0S																Base + 0x0044															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT0S31	PAT0S30	PAT0S29	PAT0S28	PAT0S27	PAT0S26	PAT0S25	PAT0S24	PAT0S23	PAT0S22	PAT0S21	PAT0S20	PAT0S19	PAT0S18	PAT0S17	PAT0S16	PAT0S15	PAT0S14	PAT0S13	PAT0S12	PAT0S11	PAT0S10	PAT0S09	PAT0S08	PAT0S07	PAT0S06	PAT0S05	PAT0S04	PAT0S03	PAT0S02	PAT0S01	PAT0S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

31:0	PAT0S n	Writing 1 to PAT0S n will set PAT0 n to 1 in register PAT0. Writing 0 to PAT0S n will no use.	W

27.4.15 PORT PAT0/Data Clear Registers (PxPAT0C,0x0048)

PAPAT0C,PBPAT0C,PCPAT0C,PDPAT0C and PEPAT0C are four 32-bit PORT Pattern 0 or data clear registers.

	PxPAT0C																Base + 0x0048													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT0C31	PAT0C30	PAT0C29	PAT0C28	PAT0C27	PAT0C26	PAT0C25	PAT0C24	PAT0C23	PAT0C22	PAT0C21	PAT0C20	PAT0C19	PAT0C18	PAT0C17	PAT0C16	PAT0C15	PAT0C14	PAT0C13	PAT0C12	PAT0C11	PAT0C10	PAT0C09	PAT0C08	PAT0C07	PAT0C06	PAT0C05	PAT0C04	PAT0C03	PAT0C02	PAT0C01	PAT0C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PAT0C n	Writing 1 to PAT0C n will set PAT0 n to 0 in register PAT0. Writing 0 to PAT0C n will no use.	W

27.4.16 PORT FLAG Registers (PxFLG,0x0050)

PAFLG,PBFLG,PCFLG,PDFLG and PEFLG are five 32-bit PORT flag registers. They are read-only registers.

	PxFLG																Base + 0x0050													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FLAG31	FLAG30	FLAG29	FLAG28	FLAG27	FLAG26	FLAG25	FLAG24	FLAG23	FLAG22	FLAG21	FLAG20	FLAG19	FLAG18	FLAG17	FLAG16	FLAG15	FLAG14	FLAG13	FLAG12	FLAG11	FLAG10	FLAG09	FLAG08	FLAG07	FLAG06	FLAG05	FLAG04	FLAG03	FLAG02	FLAG01	FLAG00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	FLAG n	Where n = 0 ~ 31 and FLAG n = FLAG00 ~ FLAG31. FLAG n is interrupt flag bit for checking the interrupt whether to happen. When GPIO is used as interrupt function and the interrupt happened, the FLAG n in PBFLG will be set to 1.	R

Note:

1. Not every PBD support Input Enable Control, please check out Function Overview chapter for details.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.4.17 PORT FLAG Clear Registers (PxFLGC,0x0058)

PAFLGC,PBFLGC,PCFLGC,PDFLGC and PEFLGC are five 32-bit PORT flag clear registers. They are read-only registers.

	PxFLGC																Base + 0x0058													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FLAGC31	FLAGC30	FLAGC29	FLAGC28	FLAGC27	FLAGC26	FLAGC25	FLAGC24	FLAGC23	FLAGC22	FLAGC21	FLAGC20	FLAGC19	FLAGC18	FLAGC17	FLAGC16	FLAGC15	FLAGC14	FLAGC13	FLAGC12	FLAGC11	FLAGC10	FLAGC09	FLAGC08	FLAGC07	FLAGC06	FLAGC05	FLAGC04	FLAGC03	FLAGC02	FLAGC01	FLAGC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	FLAGC n	When GPIO is used as interrupt function and when write 1 to the bit, the bit FLAG n in PxFLG will be cleared.	RC

27.4.18 PORT Dual-Edge Interrupt Register (PxEDG,0x70)

PORT x GROUP dual-edge interrupt register.

	PxEDG																0x70													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EDG31	EDG30	EDG29	EDG28	EDG27	EDG26	EDG25	EDG24	EDG23	EDG22	EDG21	EDG20	EDG19	EDG18	EDG17	EDG16	EDG15	EDG14	EDG13	EDG12	EDG11	EDG10	EDG09	EDG08	EDG07	EDG06	EDG05	EDG04	EDG03	EDG02	EDG01	EDG00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	EDG n	Where n = 0 ~ 31 and EDG n = EDG00 ~ EDG31. EDG n is used to switch active edge of the interrupt from the pad. (please refer to chapter 27.5.1) 0: single-edge interrupt detection (the edge selection bits, PAT0 n enabled) 1: dual-edge interrupt detection (the edge selection bits, PAT0 n ignored)	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.4.19 PORT Dual-Edge Interrupt Set Register (PxEDGS,0x74)

PORT x GROUP dual-edge interrupt set register, WRITE-ONLY.

	PxEDGS																													0x74
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EDGS31	EDGS30	EDGS29	EDGS28	EDGS27	EDGS26	EDGS25	EDGS24	EDGS23	EDGS22	EDGS21	EDGS20	EDGS19	EDGS18	EDGS17	EDGS16	EDGS15	EDGS14	EDGS13	EDGS12	EDGS11	EDGS10	EDGS09	EDGS08	EDGS07	EDGS06	EDGS05	EDGS04	EDGS03	EDGS02	EDGS01	EDGS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	EDGS n	Writing 1 to EDGS n will set EDG n to 1 in register PEEDG. Writing 0 to EDGS n will be ignored.	W

27.4.20 PORT Dual-Edge Interrupt Clear Register (PxEDGC,0x78)

PORT x GROUP dual-edge interrupt clear register, WRITE-ONLY.

	PxEDGC																													0x78
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EDGC31	EDGC30	EDGC29	EDGC28	EDGC27	EDGC26	EDGC25	EDGC24	EDGC23	EDGC22	EDGC21	EDGC20	EDGC19	EDGC18	EDGC17	EDGC16	EDGC15	EDGC14	EDGC13	EDGC12	EDGC11	EDGC10	EDGC09	EDGC08	EDGC07	EDGC06	EDGC05	EDGC04	EDGC03	EDGC02	EDGC01	EDGC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	EDGC n	Writing 1 to EDGC n will clear EDG n to 0 in register PEEDG. Writing 0 to EDGC n will be ignored.	W

27.4.21 PORT PULL-UP State Register (PxPU,0x80)

PORT A GROUP PULL-UP enabled State register.

	PAPU																													0x80
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PU31	PU30	PU29	PU28	PU27	PU26	PU25	PU24	PU23	PU22	PU21	PU20	PU19	PU18	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	PU09	PU08	PU07	PU06	PU05	PU04	PU03	PU02	PU01	PU00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:0	PU n	Where n = 0 ~ 31 and PU n = PU0 ~ PU31. PU n is used to switch pull-up of the corresponding PAPUn. 0: HI-Z 1: PULL-UP Enable	RW

PORT B GROUP PULL-UP enabled State register.

	PBPU																													0x80
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PU31	PU30	PU29	PU28	PU27	PU26	PU25	PU24	PU23	PU22	PU21	PU20	PU19	PU18	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	PU09	PU08	PU07	PU06	PU05	PU04	PU03	PU02	PU01	PU00
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PU n	Where n = 0 ~ 31 and PU n = PU0 ~ PU31. PU n is used to switch pull-up of the corresponding PBPUn. 0: HI-Z 1: PULL-UP Enable	RW

PORT C GROUP PULL-UP enabled State register.

	PCPU																													0x80
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PU31	PU30	PU29	PU28	PU27	PU26	PU25	PU24	PU23	PU22	PU21	PU20	PU19	PU18	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	PU09	PU08	PU07	PU06	PU05	PU04	PU03	PU02	PU01	PU00
RST	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bits	Name	Description	R/W
31:0	PU n	Where n = 0 ~ 31 and PU n = PU0 ~ PU31. PU n is used to switch pull-up of the corresponding PCPUn. 0: HI-Z 1: PULL-UP Enable	RW

PORT D GROUP PULL-UP enabled State register.

	PDPU																													0x80
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PU31	PU30	PU29	PU28	PU27	PU26	PU25	PU24	PU23	PU22	PU21	PU20	PU19	PU18	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	PU09	PU08	PU07	PU06	PU05	PU04	PU03	PU02	PU01	PU00
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:0	PU n	Where n = 0 ~ 31 and PU n = PU0 ~ PU31. PU n is used to switch pull-up of the corresponding PDPUn. 0: HI-Z 1: PULL-UP Enable	RW

PORT E GROUP PULL-UP enabled State register.

	PEPU																													0x80
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PU31	PU30	PU29	PU28	PD27	PD26	PD25	PD24	PD23	PD22	PU21	PU20	PU19	PU18	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	PU09	PU08	PU07	PU06	PU05	PU04	PU03	PU02	PU01	PU00
RST	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bits	Name	Description	R/W
31:0	PU n	Where n = 0 ~ 21, 28 ~ 31 and PU n = PU0 ~ PU21, PU28 ~ PU31. PU n is used to switch pull-up of the corresponding PEPUn. 0: HI-Z 1: PULL-UP Enable Note: Where n = 22 ~ 27 and PU n = PU22 ~ PU27. The register will be used to switch pull-down for TYPED(PORT E22-27). 0: HI-Z 1: PULL-DOWN Enable	RW

27.4.22 PORT PULL-UP State Set Register (PxPUS,0x84)

PORT x GROUP pull-up state set register7, WRITE-ONLY.

	PxPUS																													0x84
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUS31	PUS30	PUS29	PUS28	PUS27	PUS26	PUS25	PUS24	PUS23	PUS22	PUS21	PUS20	PUS19	PUS18	PUS17	PUS16	PUS15	PUS14	PUS13	PUS12	PUS11	PUS10	PUS09	PUS08	PUS07	PUS06	PUS05	PUS04	PUS03	PUS02	PUS01	PUS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PUS n	Writing 1 to PUS n will set PU n to 1 in register PxPUS. Writing 0 to PUS n will be ignored.	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.4.23 PORT PULL-UP State Clear Register (PxPUC,0x88)

PORT x GROUP pull-up state clear register, WRITE-ONLY.

	PxPUC																													0x88
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUC31	PUC30	PUC29	PUC28	PUC27	PUC26	PUC25	PUC24	PUC23	PUC22	PUC21	PUC20	PUC19	PUC18	PUC17	PUC16	PUC15	PUC14	PUC13	PUC12	PUC11	PUC10	PUC09	PUC08	PUC07	PUC06	PUC05	PUC04	PUC03	PUC02	PUC01	PUC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PUC n	Writing 1 to PUC n will clear PU n to 1 in register PxPUC. Writing 0 to PUC n will be ignored.	W

27.4.24 PORT PULL-DOWN State Register (PxPD,0x90)

PORT A GROUP PULL-DOWN enabled State register.

	PxPD																													0x90
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD31	PD30	PD29	PD28	PD27	PD26	PD25	PD24	PD23	PD22	PD21	PD20	PD19	PD18	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	PD09	PD08	PD07	PD06	PD05	PD04	PD03	PD02	PD01	PD00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PD n	Where n = 0 ~ 31 and PD n = PD0 ~ PD31. PD n is used to switch pull-down of the corresponding PAPDn. 0: HI-Z 1: PULL-DOWN Enable	RW

PORT B GROUP PULL-DOWN enabled State register.

	PBPD																													0x90
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD31	PD30	PD29	PD28	PD27	PD26	PD25	PD24	PD23	PD22	PD21	PD20	PD19	PD18	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	PD09	PD08	PD07	PD06	PD05	PD04	PD03	PD02	PD01	PD00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
31:0	PD n	Where n = 0 ~ 31 and PD n = PD0 ~ PD31. PD n is used to switch pull-down of the corresponding PBPDn. 0: HI-Z 1: PULL-DOWN Enable	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

PORT C GROUP PULL-DOWN enabled State register.

	PCPD																														0x90
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD31	PD30	PD29	PD28	PD27	PD26	PD25	PD24	PD23	PD22	PD21	PD20	PD19	PD18	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	PD09	PD08	PD07	PD06	PD05	PD04	PD03	PD02	PD01	PD00
RST	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	R/W
31:0	PD n	Where n = 0 ~ 31 and PD n = PD0 ~ PD31. PD n is used to switch pull-down of the corresponding PCPDn. 0: HI-Z 1: PULL-DOWN Enable	RW

PORT D GROUP PULL-DOWN enabled State register.

	PDPD																														0x90
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD31	PD30	PD29	PD28	PD27	PD26	PD25	PD24	PD23	PD22	PD21	PD20	PD19	PD18	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	PD09	PD08	PD07	PD06	PD05	PD04	PD03	PD02	PD01	PD00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PD n	Note: The register will be ignored for TYPEC(PORT D).	RW

PORT E GROUP PULL-DOWN enabled State register.

	PEPD																														0x90
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD31	PD30	PD29	PD28	PD27	PD26	PD25	PD24	PD23	PD22	PD21	PD20	PD19	PD18	PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	PD09	PD08	PD07	PD06	PD05	PD04	PD03	PD02	PD01	PD00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PD n	Note: The register will be ignored for TYPEC(PORT D).	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.4.25 PORT PULL-DOWN State Set Register (PxPDS,0x94)

PORT x GROUP pull-down state set register, WRITE-ONLY.

	PxPDS																													0x94
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PDS31	PDS30	PDS29	PDS28	PDS27	PDS26	PDS25	PDS24	PDS23	PDS22	PDS21	PDS20	PDS19	PDS18	PDS17	PDS16	PDS15	PDS14	PDS13	PDS12	PDS11	PDS10	PDS09	PDS08	PDS07	PDS06	PDS05	PDS04	PDS03	PDS02	PDS01	PDS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PDS n	Writing 1 to PDS n will set PD n to 1 in register PxPDS. Writing 0 to PDS n will be ignored.	W

27.4.26 PORT PULL-DOWN State Clear Register (PxPDC,0x98)

PORT x GROUP pull-down state clear register, WRITE-ONLY.

	PxPDC																													0x98
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PDC31	PDC30	PDC29	PDC28	PDC27	PDC26	PDC25	PDC24	PDC23	PDC22	PDC21	PDC20	PDC19	PDC18	PDC17	PDC16	PDC15	PDC14	PDC13	PDC12	PDC11	PDC10	PDC09	PDC08	PDC07	PDC06	PDC05	PDC04	PDC03	PDC02	PDC01	PDC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PDC n	Writing 1 to PDC n will clear PD n to 1 in register PxPDC. Writing 0 to PDC n will be ignored.	W

27.4.27 PORT Drive Strength State Register0 (PxDS0,0xA0)

PORT x GROUP Drive Strength register0.

	PxDS0																													0xA0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DS031	DS030	DS029	DS028	DS027	DS026	DS025	DS024	DS023	DS022	DS021	DS020	DS019	DS018	DS017	DS016	DS015	DS014	DS013	DS012	DS011	DS010	DS009	DS008	DS007	DS006	DS005	DS004	DS003	DS002	DS001	DS000
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:0	DS0 n	Where n = 0 ~ 31 and DS0 n = DS00 ~ DS031. DS0 n is used to switch Drive Strength of the corresponding PxDS0n. 1) For TYPEA or TYPEB or TYPEE (Please see chapter 1.3: Pad Drive Strength Characteristics.) 2) For TYPEC or TYPED The register will be ignored	RW

27.4.28 PORT Drive Strength State Set Register0 (PxDS0S,0xA4)

PORT x GROUP Drive Strength state set register, WRITE-ONLY.

	PxDS0S																													0xA4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DS0S31	DS0S30	DS0S29	DS0S28	DS0S27	DS0S26	DS0S25	DS0S24	DS0S23	DS0S22	DS0S21	DS0S20	DS0S19	DS0S18	DS0S17	DS0S16	DS0S15	DS0S14	DS0S13	DS0S12	DS0S11	DS0S10	DS0S09	DS0S08	DS0S07	DS0S06	DS0S05	DS0S04	DS0S03	DS0S02	DS0S01	DS0S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DS0S n	Writing 1 to DS0S n will set DS0 n to 1 in register PxDS0S. Writing 0 to DS0S n will be ignored.	W

27.4.29 PORT Drive Strength State Clear Register0 (PxDS0C,0xA8)

PORT x GROUP Drive Strength state clear register, WRITE-ONLY.

	PxDS0C																													0xA8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DS0C31	DS0C30	DS0C29	DS0C28	DS0C27	DS0C26	DS0C25	DS0C24	DS0C23	DS0C22	DS0C21	DS0C20	DS0C19	DS0C18	DS0C17	DS0C16	DS0C15	DS0C14	DS0C13	DS0C12	DS0C11	DS0C10	DS0C09	DS0C08	DS0C07	DS0C06	DS0C05	DS0C04	DS0C03	DS0C02	DS0C01	DS0C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DS0C n	Writing 1 to DS0C n will clear DS0 n to 1 in register PxDS0C. Writing 0 to DS0C n will be ignored.	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.4.30 PORT Drive Strength State Register1 (PxDS1,0xB0)

PORT x GROUP Drive Strength register1.

	PxDS1																														0xB0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DS131	DS130	DS129	DS128	DS127	DS126	DS125	DS124	DS123	DS122	DS121	DS120	DS119	DS118	DS117	DS116	DS115	DS114	DS113	DS112	DS111	DS110	DS109	DS108	DS107	DS106	DS105	DS104	DS103	DS102	DS101	DS100
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DS1 n	Where n = 0 ~ 31 and DS1 n = DS10 ~ DS131. DS1 n is used to switch Drive Strength of the corresponding PxDS1n. 1) For TYPEA or TYPEB or TYPEE (Please see chapter 1.3: Pad Drive Strength Characteristics.) 2) For TYPEC or TYPED The register will be ignored	

27.4.31 PORT Drive Strength State Set Register1 (PxDS1S,0xB4)

PORT x GROUP Drive Strength state set register, WRITE-ONLY.

	PxDS1S																														0xB4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DS1S31	DS1S30	DS1S29	DS1S28	DS1S27	DS1S26	DS1S25	DS1S24	DS1S23	DS1S22	DS1S21	DS1S20	DS1S19	DS1S18	DS1S17	DS1S16	DS1S15	DS1S14	DS1S13	DS1S12	DS1S11	DS1S10	DS1S09	DS1S08	DS1S07	DS1S06	DS1S05	DS1S04	DS1S03	DS1S02	DS1S01	DS1S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DS1S n	Writing 1 to DS1S n will set DS1 n to 1 in register PxDS1S. Writing 0 to DS1S n will be ignored.	W

27.4.32 PORT Drive Strength State Clear Register1 (PxDS1C,0xB8)

PORT x GROUP Drive Strength state clear register, WRITE-ONLY.

	PxDS1C																														0xB8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DS1C31	DS1C30	DS1C29	DS1C28	DS1C27	DS1C26	DS1C25	DS1C24	DS1C23	DS1C22	DS1C21	DS1C20	DS1C19	DS1C18	DS1C17	DS1C16	DS1C15	DS1C14	DS1C13	DS1C12	DS1C11	DS1C10	DS1C09	DS1C08	DS1C07	DS1C06	DS1C05	DS1C04	DS1C03	DS1C02	DS1C01	DS1C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:0	DS1C n	Writing 1 to DS1C n will clear DS1 n to 1 in register PxDS1C. Writing 0 to DS1C n will be ignored.	W

27.4.33 PORT Drive Strength State Register2 (PxDS2,0xC0)

PORT x GROUP Drive Strength register2.

	PxDS2																														0xC0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DS231	DS230	DS229	DS228	DS227	DS226	DS225	DS224	DS223	DS222	DS221	DS220	DS219	DS218	DS217	DS216	DS215	DS214	DS213	DS212	DS211	DS210	DS209	DS208	DS207	DS206	DS205	DS204	DS203	DS202	DS201	DS200
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DS2 n	Where n = 0 ~ 31 and DS2 n = DS20 ~ DS231. DS2 n is used to switch Drive Strength of the corresponding PxDS2n. 1) For TYPEA or TYPEB (Please see chapter 1.3: Pad Drive Strength Characteristics.) 2) For TYPEC or TYPED or TYPEE The register will be ignored	RW

27.4.34 PORT Drive Strength State Set Register2 (PxDS2S,0xC4)

PORT x GROUP Drive Strength state set register2, WRITE-ONLY.

	PxDS2S																														0xC4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DS2S31	DS2S30	DS2S29	DS2S28	DS2S27	DS2S26	DS2S25	DS2S24	DS2S23	DS2S22	DS2S21	DS2S20	DS2S19	DS2S18	DS2S17	DS2S16	DS2S15	DS2S14	DS2S13	DS2S12	DS2S11	DS2S10	DS2S09	DS2S08	DS2S07	DS2S06	DS2S05	DS2S04	DS2S03	DS2S02	DS2S01	DS2S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DS2S n	Writing 1 to DS2S n will set DS2 n to 1 in register PxDS2S. Writing 0 to DS2S n will be ignored.	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

27.4.35 PORT Drive Strength State Clear Register2 (PxDS2C,0xC8)

PORT x GROUP Drive Strength state clear register2, WRITE-ONLY.

	PxDS2C																													0xC8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DS2C31	DS2C30	DS2C29	DS2C28	DS2C27	DS2C26	DS2C25	DS2C24	DS2C23	DS2C22	DS2C21	DS2C20	DS2C19	DS2C18	DS2C17	DS2C16	DS2C15	DS2C14	DS2C13	DS2C12	DS2C11	DS2C10	DS2C09	DS2C08	DS2C07	DS2C06	DS2C05	DS2C04	DS2C03	DS2C02	DS2C01	DS2C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	DS2C n	Writing 1 to DS2C n will clear DS2 n to 1 in register PxDS2C. Writing 0 to DS2C n will be ignored.	W

27.4.36 PORT Slew Rate Register (PxSR,0xD0)

PORT x GROUP slew rate register.

	PxSR																													0xD0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SR31	SR30	SR29	SR28	SR27	SR26	SR25	SR24	SR23	SR22	SR21	SR20	SR19	SR18	SR17	SR16	SR15	SR14	SR13	SR12	SR11	SR10	SR09	SR08	SR07	SR06	SR05	SR04	SR03	SR02	SR01	SR00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	SR n	Where n = 0 ~ 31 and SR n = SR0 ~ SR31. SR n is used to switch slew rate of the corresponding PxSRn. 0: slow(half frequency) 1: fast Note: The register is valid for TYPEB and TYPEE.	RW

27.4.37 PORT Slew Rate Set Register (PxSRS,0xD4)

PORT x GROUP slew rate set register, WRITE-ONLY.

	PxSRS																													0xD4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRS31	SRS30	SRS29	SRS28	SRS27	SRS26	SRS25	SRS24	SRS23	SRS22	SRS21	SRS20	SRS19	SRS18	SRS17	SRS16	SRS15	SRS14	SRS13	SRS12	SRS11	SRS10	SRS09	SRS08	SRS07	SRS06	SRS05	SRS04	SRS03	SRS02	SRS01	SRS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:0	SRS n	Writing 1 to SRS n will set SR n to 1 in register PxSRS. Writing 0 to SRS n will be ignored.	W

27.4.38 PORT Slew Rate Clear Register (PxSRC,0xD8)

PORT x GROUP slew rate clear register, WRITE-ONLY.

	PxSRC																													0xD8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRC31	SRC30	SRC29	SRC28	SRC27	SRC26	SRC25	SRC24	SRC23	SRC22	SRC21	SRC20	SRC19	SRC18	SRC17	SRC16	SRC15	SRC14	SRC13	SRC12	SRC11	SRC10	SRC09	SRC08	SRC07	SRC06	SRC05	SRC04	SRC03	SRC02	SRC01	SRC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	SRC n	Writing 1 to SRC n will set SR n to 0 in register PxSRC. Writing 0 to SRC n will be ignored.	W

27.4.39 PORT Schmitt Trigger Register (PxSMT,0xE0)

PORT x GROUP schmitt trigger register.

	PxSMT																													0xE0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SMT31	SMT30	SMT29	SMT28	SMT27	SMT26	SMT25	SMT24	SMT23	SMT22	SMT21	SMT20	SMT19	SMT18	SMT17	SMT16	SMT15	SMT14	SMT13	SMT12	SMT11	SMT10	SMT09	SMT08	SMT07	SMT06	SMT05	SMT04	SMT03	SMT02	SMT01	SMT00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	SMT n	Where n = 0 ~ 31 and SMT n = SMT0 ~ SMT31. SMT n is used to enable schmitt trigger of the corresponding PxSMTn. 0: schmitt trigger disabled 1: schmitt trigger enabled Note: The register will be ignored for TYPEC and TYPED	RW

27.4.40 PORT Schmitt Trigger Set Register (PxSMTS,0xE4)

PORT x GROUP schmitt trigger set register, WRITE-ONLY.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	PxSMTS																													0xE4
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SMTS31	SMTS30	SMTS29	SMTS28	SMTS27	SMTS26	SMTS25	SMTS24	SMTS23	SMTS22	SMTS21	SMTS20	SMTS19	SMTS18	SMTS17	SMTS16	SMTS15	SMTS14	SMTS13	SMTS12	SMTS11	SMTS10	SMTS09	SMTS08	SMTS07	SMTS06	SMTS05	SMTS04	SMTS03	SMTS02	SMTS01	SMTS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	SMTS n	Writing 1 to SMTS n will set SMT n to 1 in register PxSMTS. Writing 0 to SMTS n will be ignored.	W

27.4.41 PORT Schmitt Trigger Clear Register (PxSMTC,0xE8)

PORT x GROUP schmitt trigger clear register, WRITE-ONLY.

	PxSMTC																													0xE8
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SMTC31	SMTC30	SMTC29	SMTC28	SMTC27	SMTC26	SMTC25	SMTC24	SMTC23	SMTC22	SMTC21	SMTC20	SMTC19	SMTC18	SMTC17	SMTC16	SMTC15	SMTC14	SMTC13	SMTC12	SMTC11	SMTC10	SMTC09	SMTC08	SMTC07	SMTC06	SMTC05	SMTC04	SMTC03	SMTC02	SMTC01	SMTC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	SMTC n	Writing 1 to SMTC n will set SMT n to 0 in register PxSMTC. Writing 0 to SMTC n will be ignored.	W

27.4.42 PORT Z Shadow Register Group

PORT Z group only have eight registers, PZINTS,PZINTC,PZMSKS,PZMSKC,PZPAT1S,PZPAT1C, PZPAT0S,PZPAT0C. those registers shadow as same as other group registers function which the offset address equal.

	PZINTS																													Base + 0x0014
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTS31	INTS30	INTS29	INTS28	INTS27	INTS26	INTS25	INTS24	INTS23	INTS22	INTS21	INTS20	INTS19	INTS18	INTS17	INTS16	INTS15	INTS14	INTS13	INTS12	INTS11	INTS10	INTS09	INTS08	INTS07	INTS06	INTS05	INTS04	INTS03	INTS02	INTS01	INTS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	PZINTC																															Base + 0x0018
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTC31	INTC30	INTC29	INTC28	INTC27	INTC26	INTC25	INTC24	INTC23	INTC22	INTC21	INTC20	INTC19	INTC18	INTC17	INTC16	INTC15	INTC14	INTC13	INTC12	INTC11	INTC10	INTC09	INTC08	INTC07	INTC06	INTC05	INTC04	INTC03	INTC02	INTC01	INTC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZMSKS																															Base + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKS31	MSKS30	MSKS29	MSKS28	MSKS27	MSKS26	MSKS25	MSKS24	MSKS23	MSKS22	MSKS21	MSKS20	MSKS19	MSKS18	MSKS17	MSKS16	MSKS15	MSKS14	MSKS13	MSKS12	MSKS11	MSKS10	MSKS09	MSKS08	MSKS07	MSKS06	MSKS05	MSKS04	MSKS03	MSKS02	MSKS01	MSKS00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZMSKC																															Base + 0x0028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKC31	MSKC30	MSKC29	MSKC28	MSKC27	MSKC26	MSKC25	MSKC24	MSKC23	MSKC22	MSKC21	MSKC20	MSKC19	MSKC18	MSKC17	MSKC16	MSKC15	MSKC14	MSKC13	MSKC12	MSKC11	MSKC10	MSKC09	MSKC08	MSKC07	MSKC06	MSKC05	MSKC04	MSKC03	MSKC02	MSKC01	MSKC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZPAT1S																															Base + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT1S31	PAT1S30	PAT1S29	PAT1S28	PAT1S27	PAT1S26	PAT1S25	PAT1S24	PAT1S23	PAT1S22	PAT1S21	PAT1S20	PAT1S19	PAT1S18	PAT1S17	PAT1S16	PAT1S15	PAT1S14	PAT1S13	PAT1S12	PAT1S11	PAT1S10	PAT1S09	PAT1S08	PAT1S07	PAT1S06	PAT1S05	PAT1S04	PAT1S03	PAT1S02	PAT1S01	PAT1S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZPAT1S																															Base + 0x0038
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT1C31	PAT1C30	PAT1C29	PAT1C28	PAT1C27	PAT1C26	PAT1C25	PAT1C24	PAT1C23	PAT1C22	PAT1C21	PAT1C20	PAT1C19	PAT1C18	PAT1C17	PAT1C16	PAT1C15	PAT1C14	PAT1C13	PAT1C12	PAT1C11	PAT1C10	PAT1C09	PAT1C08	PAT1C07	PAT1C06	PAT1C05	PAT1C04	PAT1C03	PAT1C02	PAT1C01	PAT1C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	PZPAT0S																													Base + 0x0044
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT0S31	PAT0S30	PAT0S29	PAT0S28	PAT0S27	PAT0S26	PAT0S25	PAT0S24	PAT0S23	PAT0S22	PAT0S21	PAT0S20	PAT0S19	PAT0S18	PAT0S17	PAT0S16	PAT0S15	PAT0S14	PAT0S13	PAT0S12	PAT0S11	PAT0S10	PAT0S09	PAT0S08	PAT0S07	PAT0S06	PAT0S05	PAT0S04	PAT0S03	PAT0S02	PAT0S01	PAT0S00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PZPAT0C																													Base + 0x0048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT0C31	PAT0C30	PAT0C29	PAT0C28	PAT0C27	PAT0C26	PAT0C25	PAT0C24	PAT0C23	PAT0C22	PAT0C21	PAT0C20	PAT0C19	PAT0C18	PAT0C17	PAT0C16	PAT0C15	PAT0C14	PAT0C13	PAT0C12	PAT0C11	PAT0C10	PAT0C09	PAT0C08	PAT0C07	PAT0C06	PAT0C05	PAT0C04	PAT0C03	PAT0C02	PAT0C01	PAT0C00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

27.4.43 GPIOZ Group ID to Load Register (PzGID2LD,0x00F0)

This register controls which Port Group to be load from GPIOZ.

	PzGID2LD																													Base + 0x00F0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													GPID		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOZ Group can shadow four register groups for GPIO Group A to C, when set or clear A to C register groups below four types, it will through shadow register to implement. the GPIOZ ID used for controls which Group to be manipulate.

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, Read as zero	R
2:0	GPID	GPIO Port ID load control register, according the values of GPID to load Shadow register group to the same offset address of group ID meet the GPID. GPID: Shadow register load to work groups 0: Load to GPIO Port A	W

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

			1	Load to GPIO Port B		
			2	Load to GPIO Port C		
			3	Undefine		
			4	Undefine		
			5	Undefine		

27.5 Program Guide

27.5.1 Port Function Guide

EDG	INT	MASK	PAT1	PAT0	Port Description
0	1	0	0	0	Port is low level triggered interrupt input.
0	1	0	0	1	Port is high level triggered interrupt input.
0	1	0	1	0	Port is fall edge triggered interrupt input.
0	1	0	1	1	Port is rise edge triggered interrupt input.
1	1	0	1	x	Port is dual-edge(both rise and fall edge) triggered interrupt input.
0	1	1	0	0	Port is low level triggered interrupt input. Interrupt is masked. Flag is recorded.
0	1	1	0	1	Port is high level triggered interrupt input. Interrupt is masked. Flag is recorded.
0	1	1	1	0	Port is fall edge triggered interrupt input. Interrupt is masked. Flag is recorded.
0	1	1	1	1	Port is rise edge triggered interrupt input. Interrupt is masked. Flag is recorded.
1	1	1	1	x	Port is dual-edge(both rise and fall edge) triggered interrupt input. Interrupt is masked. Flag is recorded.
x	0	0	0	0	Port is pin of device 0.
x	0	0	0	1	Port is pin of device 1.
x	0	0	1	0	Port is pin of device 2.
x	0	0	1	1	Port is pin of device 3.
x	0	1	0	0	Port is GPIO output 0.
x	0	1	0	1	Port is GPIO output 1.
x	0	1	1	x	Port is GPIO input.

27.5.2 Configure without 3rd-unexpected state

Function switching between devices and gpio is controlled by combination of 4 registers: INT/MASK/PAT1/PAT0. As the four register is accessed by soft ware in serial sequence, which posing a risk that third states occur during configuration.

For example:

current state is:

INT = 0x0, MASK = 0x0, PAT0 = 0x0, PAT1 = 0x0;

target state is:

INT = 0x1, MASK = 0x1, PAT0 = 0x1, PAT1 = 0x1;

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

If the first step is to configure INT to 0x1, the 3rd state is:

INT = 0x1, MASK = 0x0, PAT0 = 0x0, PAT1 = 0x0;

This might triggers interrupt if port is low level.

To avoid the unexpected 3-state, the four registers must be updated in the same time.

There is an dummy group GPIOZ, which only used in this purpose. The working mechanism is the information of configure can be temporarily stored in the GPIOZ. When assert GPIOZ.LD, all the four registers will load their content into target group at the same time.

Example:

If the Port B current state is:

INT = 0x0, MASK = 0x0, PAT0 = 0x0, PAT1 = 0x0;

It needs to be configured to state:

INT = 0x1, MASK = 0x1, PAT0 = 0x1, PAT1 = 0x1;

There are two steps to finish:

Step1: put the configuration to temporary buffer: GPIOZ

PzINTS = 0x1;

PzMSKS = 0x1;

PzPAT0S = 0x1;

PzPAT1S = 0x1;

alternatively, PzINT, PzMSK, PzPAT0, PzPAT1 are also can be configured straightly.

Step2: configure PzGID2LD to specify which port group to load

PzGID2LD = 0x1; (0x1 stands for GPIO Port B)

27.5.3 Dual-edge Interrupt Configure Guide

When you want to enable the dual-edge trigger interrupt function, follow the settings below:

1.set the bit of PxEDG(x=A~E) register;

2.set the bit of PxINT and PxPAT1 (x=A~E) register;

3.clear the INT flag bit of PxFLG(x=A~E) register;

4.clear the mask bit of PxMSK(x=A~E) register;

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

28 SMB Controller

28.1 Overview

The SMB bus is a two-wire serial interface, consisting of a serial data line (SDA) and a serial clock (SCL). These wires carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a “transmitter” or “receiver,” depending on the function of the device. Devices can also be considered as masters or slaves when performing data transfers. A master is the device that initializes/terminates a data transfer on the bus and generates clock signals to permit that transfer. During that time, any addressed device is considered as a slave. The SMB controller is software controlled. It behaves as a master or a slave. However, operating as a master and slave simultaneously is not supported.

28.1.1 Features

- Two-wire SMB serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
- Two speeds
  - Standard mode (100 Kb/s)
  - Fast mode (400 Kb/s)
- Device clock is identical with pclk(APB clock)
- Programmable SCL generator
- Master or slave SMB operation
- 7-bit addressing/10-bit addressing whether configure as Master or Slave
- Transmit General Call or START byte
- level transmit and receive FIFOs
- Interrupt operation
- The number of devices that you can connect to the same SMB-bus is limited only by the maximum bus capacitance of 400pF
- APB interface
- 6 independent SMB channels (SMB0, SMB1, SMB2, SMB3, SMB4, SMB5)

28.1.2 Pin Description

Table 28-1 SMB Pin Description

Name	Width	IO	Description
SDA	1-bit	IO	SMB serial data
SCL	1-bit	IO	SMB serial clock

Please note that dedicate pull-up resistors must be introduced on board-level. The low-to-high (rise time) transition is highly dependent on RC time constant of the bus.

Totally speaking, for standard-mode SMB-bus system, the pull up resistor depends on following parameters:

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

- Supply voltage
- Bus capacitance
- Number of connected devices

For fast-mode SMB-bus system, switched pull-up circuit may be essential for strict speed and load requirement. (Please refer NXP Semiconductors, *UM10204: I2C-Bus specification and user manual (Rev.6--4 April 2014)*')

28.2 Registers

28.2.1 Registers Memory Map

A read operation to an address location that contains unused bits results in a 0 value being returned on each of the unused bits.

Registers in SMB controller can be accessed by indicating 24-bit Address Base combined with 8-bit Address Offset.

Table 28-2 Registers Memory Map-Address Base

Name	Addr Base	Description
SMB0	0x10050000	Address base of SMB0
SMB1	0x10051000	Address base of SMB1
SMB2	0x10052000	Address base of SMB2
SMB3	0x10053000	Address base of SMB3
SMB4	0x10054000	Address base of SMB4
SMB5	0x10055000	Address base of SMB5

Table 28-3 Registers Memory Map-Address Offset

Name	Addr Offset	Description	Width	RW	Reset
SMB_CON	0x00	SMB control	8bits	RW	0x7D
SMB_TAR	0x04	SMB target address	13bits	RW	0x1055
SMB_SAR	0x08	SMB slave address	10bits	RW	0x055
SMB_HS_MADDR	0x0C	SMB HS Master Mode Code Address	3bits	RW	0x1
SMB_DC	0x10	SMB data buffer and command	9bits	RW	0x000
SMB_SHCNT	0x14	Standard speed SMB SCL high count	16bits	RW	0x0190
SMB_SLCNT	0x18	Standard speed SMB SCL low count	16bits	RW	0x01D6
SMB_FHCNT	0x1C	Fast speed SMB SCL high count	16bits	RW	0x003C
SMB_FLCNT	0x20	Fast speed SMB SCL low count	16bits	RW	0x0082
SMB_HHCNT	0x24	High speed SMB SCL high count	16bits	RW	0x006
SMB_HLCNT	0x28	High speed SMB SCL low count	16bits	RW	0x0010
SMB_INTST	0x2C	SMB Interrupt Status	12bits	R	0x000
SMB_INTM	0x30	SMB Interrupt Mask	12bits	R/W	12'h8FF
SMB_RINTST	0x34	SMB Raw Interrupt Status	12bits	R	0x0
SMB_RXTL	0x38	SMB RxFIFO Threshold	6bits	RW	0x1F

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

SMB_TXTL	0x3C	SMB TxFIFO Threshold	6bits	RW	0x20
SMB_CINT	0x40	Clear Interrupts	1bit	R	0x0
SMB_CRXUF	0x44	Clear RXUF Interrupt	1bit	R	0x0
SMB_CRXOF	0x48	Clear RX_OVER Interrupt	1bit	R	0x0
SMB_CTXOF	0x4C	Clear TX_OVER Interrupt	1bit	R	0x0
SMB_CRXREQ	0x50	Clear RDREQ Interrupt	1bit	R	0x0
SMB_CTXABT	0x54	Clear TX_ABRT Interrupt	1bit	R	0x0
SMB_CRXDN	0x58	Clear RX_DONE Interrupt	1bit	R	0x0
SMB_CACT	0x5C	Clear ACTIVITY Interrupt	1bit	R	0x0
SMB_CSTP	0x60	Clear STOP Interrupt	1bit	R	0x0
SMB_CSTT	0x64	Clear START Interrupt	1bit	R	0x0
SMB_CGC	0x68	Clear GEN_CALL Interrupt	1bit	R	0x0
SMB_ENABLE	0x6C	SMB Enable	1bit	RW	0x0
SMB_ST	0x70	SMB Status register	7bits	R	0x06
SMB_TXFLR	0x74	TxFIFO Level Register	6bits	R	0x0
SMB_RXFLR	0X78	RxFIFO Level Register	6bits	R	0x0
SMB_SDAHD	0x7C	SMB SDA Hold time Register	16bits	RW	0x55
SMB_ABTSRC	0x80	SMB Transmit Abort Status Register	32bits	R	0x0000
I2CSDNACK	0x84	GenerateSLV_DATA_NACK Register	1bit	R/W	0x0
SMB_DMACR	0x88	DMA Control Register	2bits	R/W	0x0
SMB_DMATDLR	0x8C	DMA Transmit Data Level	6bits	R/W	0x0
SMB_DMARDLR	0x90	DMA Receive Data Level	6bits	R/W	0x0
SMB_SDASU	0x94	SMB SDA Setup Register	8bits	RW	0x64
SMB_ACKGC	0x98	SMB ACK General Call Register	1bit	RW	0x1
SMB_ENBST	0x9C	SMB Enable Status Register	3bits	R	0x0
SMB_FSPKLEN	0xA0	SS and FS Spike Suppression Limit	8bits	RW	0x1
SMB_HSPKLEN	0xA4	HS Spike Suppression Limit	8bits	RW	0x1

28.2.2 Registers and Fields Description

28.2.3 SMB_CON (SMB Control Register)

This register can be written only when SMB is disabled, which corresponds to SMB_ENABLE[0] being set to 0. Writes at other time have on effect.

SMB_CON																BASE + 0x00															
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								SLVDIS	RESTART	MATP	SATP	SPEED		MD
RST																0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
15:7	Reserved	Writing has no effect, read as zero.	R
6	SLVDIS	This bit controls whether SMB has its slave disabled. 0: slave is enabled 1: slave is disabled Note: Software should ensure that if this bit is written with'0', then bit 0 should also be written with '0'.	RW
5	RESTART	Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions. 0: disable 1: enable	RW
4	MATP	This bit is a read-only copy of SMB_TAR.MATP. 0: 7-bit addressing 1: 10-bit addressing	R
3	SATP	When acting as a slave, this bit controls whether the SMB responds to 7-bit or 10-bit addresses. 0: 7-bit addressing 1: 10-bit addressing	RW
2:1	SPEED	These bits control at which speed the SMB operates. 1: standard mode (100 kbps) 2: fast mode (400 kbps) **NOTE:** when these two bits are set to 2'b00 or 2'b11, the speed mode will be automatically set to 2'b10 i.e. fast mode.	RW
0	MD	This bit controls whether the SMB master is enabled. 0: master disabled 1: master enabled Note: Software should ensure that if this bit is written with'1', then bit 6 should also be written with '1'.	RW

28.2.4 SMB_TAR (SMB Target Address Register)

	SMB_TAR																BASE + 0x04													
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved			MATP	SPECIAL	GC_OR_START	SMBTAR									
RST																	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
15:13	Reserved	Writing has no effect, read as zero.	R
12	MATP	This bit controls whether the SMB starts its transfers in 7- or 10-bit addressing mode when acting as a master. 0: 7-bit addressing 1: 10-bit addressing **NOTE:** this bit is initially set to 0.	RW
11	SPECIAL	This bit indicates whether software performs a General Call or START BYTE command. 0: ignore the bit of GC_OR_START and use SMBTAR normally 1: perform special SMB command as specified in GC_OR_START bit **NOTE:** this bit is initially set to 0	RW
10	GC_OR_START	If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call or START byte command is to be performed by the SMB. 0: General Call Address – after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the SMB_INTST register. The SMB remains in General Call mode until the SPECIAL bit value (bit 11) is cleared 1: START BYTE	RW
9:0	SMBTAR	This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the SMB_TAR and SMB_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself, but only to a slave.	RW

NOTE:

(1).It is not necessary to perform any write to this register if SMB is enabled as an SMB slave only.

(2).The meaning of "START byte" in bit 10 is different with the SMB "start condition".

"START byte" can only be applied when a device does not have such an interface, it must constantly monitor the bus via software. For more detail information, please refer *UM10204: I2C-Bus specification and user manual (Rev.6--4 April 2014), '*3.1.15 START byte' section.

"start condition" means A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. please refer *UM10204: I2C-Bus specification and user manual (Rev.6--4 April 2014), '*3.1.4 START and STOP' section for more information.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

28.2.5 SMB_SAR (SMB Slave Address Register)

	SMB_SAR																BASE + 0x08													
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved						SMBSAR									
RST																	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Bits	Name	Description	R/W
15:10	Reserved	Writing has no effect, read as zero.	R
9:0	SMBSAR	The SMBSAR holds the slave address when the SMB is operating as a slave. For 7-bit addressing, only SMBSAR[6:0] is used. This register can be written only when the SMB interface is disabled. Writes at other times have no effect.	RW

NOTE: It is not necessary to perform any write to this register if SMB is enabled as an SMB master only.

28.2.6 SMB_HS_MADDR (SMB High Speed Master Mode Code Address Register)

This register can be written only when the SMB interface is disabled, which corresponds to SMB_ENABLE[0] being set to 0. Writes at other times have no effect.

	SMB_HS_MAR																BASE + 0x0C													
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved													HSMAR		
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description	R/W
15:3	Reserved	Writing has no effect, read as zero.	R
2:0	HSMAR	The HSMAR holds the value of the SMB HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight high speed mode masters can be present on the same SMB bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0's if the SMB_MAX_SPEED_MODE configuration parameter is set to either Standard or Fast.	RW

NOTE: It is not necessary to perform any write to this register if DW_apb_i2c is enabled as an SMB

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

slave only.

28.2.7 SMB_DC (SMB Rx/Tx Data Buffer and Command Register)

This is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO.

	SMB_DC																BASE + 0x10													
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved					RESTART	STOP	CMD	DAT							
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:11	Reserved	Writing has no effect, read as zero.	R
10	RESTART	This bit controls whether a RESTART is issued before the byte is sent or received. 1: If SMB_CON.RESTART is 1, a RESTART is issued before the byte is sent or received, regardless of whether or not the transfer direction is changing from the previous command; if SMB_CON.RESTART is 0, a STOP followed by a START is issued instead. 0: If SMB_CON.RESTART is 1, a RESTERT is issued if the transfer direction is changing from the previous command, if SMB_CON.RESTART is 0, a STOP followed by a START is issued instead.	W
9	STOP	This bit controls whether a STOP is issued after the byte is sent or received. 1: STOP is issued after the byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. 0: STOP is not issued after the byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.	W
8	CMD	This bit controls whether a read or a write is performed. This bit does not control the direction when the SMB acts as a slave. It controls only the direction when it acts as a master. 1: Read 0: Write When programming this bit, you should remember the following:	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		attempting to perform a read operation after a General Call command has been sent results in a *TX_ABRT* interrupt (bit 6 of the *SMB_RAW_INTR_STAT* register), unless bit 11 (*SPECIAL*) in the *SMB_TAR* register has been cleared. If a "1" is written to this bit after receiving a *RD_REQ* interrupt, then a *TX_ABRT* interrupt occurs.	
7:0	DAT	This register contains the data to be transmitted or received on the SMB bus. If you are writing to this register and want to perform a read, bits 7:0 (*DAT*) are ignored by the SMB module. However, when you read this register, these bits return the value of data received on the SMB interface.	RW

NOTE: [1].this command only transfer 8-bit data combined with 1-bit CMD, extra bits on the bus will be eliminated. i.e. only 8-0 bits on the bus are accepted by SMB controller.
[2].For the detail information about what condition could generate START, STOP and RESTART, please refer "*1.3.6 The condition could generate START, STOP and RESTART*".
[3].The differences between *SMB_ENABLE[5]*(RESTART) and *SMB_DC[10]*(RESTART) is that SMB_ENABLE[5] determine whether or not SMB the capability of generating repeat start, but not transmit RESTART when this bit be setted. If this bit set "1", SMB_DC[10] controls whether a RESTART is issued, if set "0", SMB_DC[10] have no meaning.

28.2.8 SMB_SHCNT (SMB Standard Speed SCL High Count Register)

	SMB_SHCNT																BASE + 0x14													
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	SMBSHCNT															
RST																	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Bits	Name	Description	R/W
15:0	SMBSHCNT	This register must be set before any SMB bus transaction can take place to ensure proper I/O timing. The register sets the SCL clock high-period count for standard speed. This register can be written only when the SMB interface is disabled which corresponds to SMB_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 6; hardware prevents values less than this being written, and if attempted results in 6 being set.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

28.2.9 SMB_SLCNT (SMB Standard Speed SCL Low Count Register)

	SMB_SLCNT															BASE + 0x18															
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																SMBSLCNT															
RST																0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	0

Bits	Name	Description	R/W
15:0	SMBSLCNT	This register must be set before any SMB bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for standard speed. This register can be written only when the SMB interface is disabled which corresponds to SMB_ENABLE[0] being set to 0. Writes at other times have no effect. The minimum valid value is 8; hardware prevents values less than this being written, and if attempted, results in 8 being set.	RW

28.2.10 SMB_FHCNT (SMB Fast Speed SCL High Count Register)

	SMB_FHCNT															BASE + 0x1C															
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																SMBFHCNT															
RST																0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

Bits	Name	Description	R/W
15:0	SMBFHCNT	This register must be set before any SMB bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for fast speed. This register can be written only when the SMB interface is disabled which corresponds to SMB_ENABLE[0] being set to 0. Writes at other times have no effect. Minimum value allowed for the SMBSHCNT registers is 6. If the set value was less than 6, it will be automatically set to 6.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

28.2.11 SMB_FLCNT (SMB Fast Speed SCL Low Count Register)

	SMB_FLCNT																BASE + 0x20															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	SMBFLCNT															
RST																	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0

Bits	Name	Description	R/W
15:0	SMBFLCNT	This register must be set before any SMB bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for fast speed. This register can be written only when the SMB interface is disabled which corresponds to SMB_ENABLE[0] being set to 0. Writes at other times have no effect. Minimum value that can be programmed in the SMBSLCNT registers is 8. If the set value was less than 8, it will be automatically set to 8	RW

28.2.12 SMB_HHCNT (SMB High Speed SCL High Count Register)

	SMB_HHCNT																BASE + 0x24															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	SMBHHCNT															
RST																	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Name	Description	R/W
15:0	SMBHHCNT	This register must be set before any SMB bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock high-period count for high speed. This register can be written only when the SMB interface is disabled which corresponds to SMB_ENABLE[0] being set to 0. Writes at other times have no effect. Minimum value allowed for the SMBSHCNT registers is 6. If the set value was less than 6, it will be automatically set to 6.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

28.2.13 SMB_HLCNT (SMB High Speed SCL Low Count Register)

	SMB_HLCNT																BASE + 0x28															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	SMBHLCNT															
RST																	0	0	0	0	0	0	0	0		0	0	1	0	0	0	0

Bits	Name	Description	R/W
15:0	SMBHLCNT	This register must be set before any SMB bus transaction can take place to ensure proper I/O timing. This register sets the SCL clock low period count for high speed. This register can be written only when the SMB interface is disabled which corresponds to SMB_ENABLE[0] being set to 0. Writes at other times have no effect. Minimum value that can be programmed in the SMBSLCNT registers is 8. If the set value was less than 8, it will be automatically set to 8	RW

28.2.14 SMB_INTST (SMB Interrupt Status Register)

Each bit in this register has a corresponding mask bit in the SMBINTM register. These bits are cleared by reading the matching interrupt clear register. The unmasked raw versions of these bits are available in the *SMB_RAW_INTR_STAT* register

	SMB_INTST																BASE + 0x2C															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved				IGC	ISTT	ISTP	IACT	RXDN	TXABT	RDREQ	TXEMP	TXOF	RXFL	RXOF	RXUF
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:12	Reserved	Writing has no effect, read as zero.	R
11	IGC	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling SMB or when the CPU reads bit 0 of the *SMB_CGC* register. SMB stores the received data in the Rx buffer.	R
10	ISTT	Indicates whether a START or RESTART condition has occurred on the SMB interface regardless of whether SMB is operating in slave or master mode.	R
9	ISTP	Indicates whether a STOP condition has occurred on the SMB interface	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		regardless of whether SMB is operating in slave or master mode.	
8	IACT	This bit captures SMB activity and stays set until it is cleared. There are four ways to clear it: 1 Disabling the SMB 2 Reading the SMB_CACT register 3 Reading the SMB_CINT register 4 System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the SMB module is idle, this bit remains set until cleared, indicating that there was activity on the bus.	R
7	RXDN	When the SMB is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.	R
6	TXABT	This bit indicates if SMB, as an SMB transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as an SMB master or an SMB slave, and is referred to as a “transmit abort”. When this bit is set to 1, the SMB_ABTSRC register indicates the reason why the transmit abort takes places. **NOTE:** The SMB flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register SMB_CTXABT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes from the APB interface.	R
5	RDREQ	This bit is set to 1 when SMB is acting as a slave and another SMB master is attempting to read data from SMB. The SMB holds the SMB bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the SMB_DC register. This bit is set to 0 just after the processor reads the SMB_CRREQ register.	R
4	TXEMP	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the SMB_TXTL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When the SMB_ENB bit 0 is 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with SMB_ENB[0]=0.	R
3	TXOF	Set during transmit if the transmit buffer is filled to SMB_TX_BUFFER_DEPTH and the processor attempts to issue another SMB command by writing to the SMB_DC register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when SMB_ENB[0]=0, this interrupt is cleared.	R
2	RXFL	Set when the receive buffer reaches or goes above the SMB_RXTL threshold in the SMB_RXTL register. It is automatically cleared by	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		hardware when buffer level goes below the threshold. If the module is disabled (SMB_ENB[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the SMB_ENB bit 0 is set to 0, regardless of the activity that continues.	
1	RXOF	Set if the receive buffer is completely filled to 64 and an additional byte is received from an external SMB device. The SMB acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (SMB_ENB[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when SMB_ENB[0]=0, this interrupt is cleared.	R
0	RXUF	Set if the processor attempts to read the receive buffer when it is empty by reading from the SMB_DC register. If the module is disabled (SMB_ENB[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when SMB_ENB[0]=0, this interrupt is cleared.	R

NOTE: *1.3.5* summary all the condition could flush TX FIFO.

28.2.15 SMB_INTM (SMB Interrupt Mask Register)

These bits mask their corresponding interrupt status bits. This register is active low; a value of 0 masks the interrupt, whereas a value of 1 unmasks the interrupt.

	SMB_INTM																BASE + 0x30													
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved				MIGC	MISTT	MISTP	MIACT	MRXDN	MTXABT	MRDREQ	MTXEMP	MTXOF	MRXFL	MRXOF	MRXUF
RST																	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
15:12	Reserved	Writing has no effect, read as zero.	R
11	MIGC	These bits mask their corresponding interrupt status bits in the SMBINTST register.	RW
10	MISTT		RW
9	MISTP		RW
8	MIACT		RW
7	MRXDN		RW
6	MTXABT		RW
5	MRDREQ		RW
4	MTXEMP		RW
3	MTXOF		RW
2	MRXFL		RW
1	MRXOF		RW
0	MRXUF		RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

28.2.16 SMB_RAW_INTR_STAT

Unlike the *SMB_INTST* register, these bits are not masked so they always show the true status of the SMB. See *SMB_INTST* for a detailed description of these bits. All bits are only read.

	SMB_RAW_INTM_STAT																BASE + 0x34													
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved				IGC	ISTT	ISTP	IACT	RXDN	TXABT	RDREQ	TXEMP	TXOF	RXFL	RXOF	RXUF
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:12	Reserved	Writing has no effect, read as zero.	R
11	GEN_CALL	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling SMB or when the CPU reads bit 0 of the SMB_CLR_GEN_CALL register. SMB stores the received data in the Rx buffer.	R
10	START_DET	Indicates whether a START or RESTART condition has occurred on the SMB interface regardless of whether SMB is operating in slave or master mode.	R
9	STOP_DET	Indicates whether a STOP condition has occurred on the SMB interface regardless of whether SMB is operating in slave or master mode.	R
8	ACTIVITY	This bit captures SMB activity and stays set until it is cleared. There are four ways to clear it: ■ Disabling the SMB ■ Reading the SMB_CLR_ACTIVITY register ■ Reading the SMB_CLR_INTR register ■ System reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the SMB module is idle, this bit remains set until cleared, indicating that there was activity on the bus.	R
7	RX_DONE	When the SMB is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.	R
6	TX_ABRT	This bit indicates if SMB, as a SMB transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. This situation can occur both as a SMB master or a SMB slave, and is referred to as a “transmit abort”. When this bit is set to 1, the SMB_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. **NOTE:** The SMB flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		SMB_CLR_TX_ABRT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes from the APB interface.	
5	RD_REQ	This bit is set to 1 when SMB is acting as a slave and another SMB master is attempting to read data from SMB. The SMB holds the SMB bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the SMB_DATA_CMD register. This bit is set to 0 just after the processor reads the SMB_CLR_RD_REQ register.	R
4	TX_EMPTY	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the SMB_TX_TL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When SMB_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with smb_en=0, this bit is set to 0.	R
3	TX_OVER	Set during transmit if the transmit buffer is filled to SMB_TX_BUFFER_DEPTH and the processor attempts to issue another SMB command by writing to the SMB_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when smb_en goes to 0, this interrupt is cleared.	R
2	RX_FULL	Set when the receive buffer reaches or goes above the RX_TL threshold in the SMB_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (SMB_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once SMB_ENABLE[0] is set to 0, regardless of the activity that continues.	R
1	RX_OVER	Set if the receive buffer is completely filled to SMB_RX_BUFFER_DEPTH and an additional byte is received from an external SMB device. The SMB acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (SMB_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when smb`_en goes to 0, this interrupt is cleared.	R
0	RX_UNDER	Set if the processor attempts to read the receive buffer when it is empty by reading from the SMB_DATA_CMD register. If the module is disabled (SMB_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when smb_en goes to 0, this interrupt is cleared.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

28.2.17 SMB_RXTL (SMB Receive FIFO Threshold Register)

	SMB_RXTL																BASE + 0x38													
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved										RXTL					
RST																	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Name	Description	R/W
15:6	Reserved	Writing has no effect, read as zero.	R
5:0	RXTL	Receive FIFO Threshold Level. Controls the level of entries that triggers the RxFIFO full interrupt. A value of n sets the threshold for (n+1) entries. For example, a value of 0 sets the threshold for 1 entry, and a value of 255 sets the threshold for 256 entries.	RW

28.2.18 SMB_TXTL (SMB Transmit FIFO Threshold Register)

	SMB_TXTL																BASE + 0x3C													
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved										TXTL					
RST																	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Name	Description	R/W
15:6	Reserved	Writing has no effect, read as zero.	R
5:0	TXTL	Transmit FIFO Threshold Level. Controls the level of entries that trigger the TxFIFO empty interrupt. A value of n sets the threshold for n entries. For example, A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.	RW

28.2.19 SMB_CINT (SMB Clear Combined and Individual Interrupt Register)

	SMB_CINT																BASE + 0x40													
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved															CINT
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CINT	Read this register to clear the combined interrupt, all individual interrupts, and the SMB_ABTSRC register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the SMB_ABTSRC register for an exception to clearing SMB_ABTSRC.	R

28.2.20 SMB_CRXUF (SMB Clear RXUF Interrupt Register)

	SMB_CRXUF															BASE + 0x44														
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														CRXUF
RST																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CRXUF	Read this register to clear the RXUF interrupt (bit 0) of the SMB_INTST register.	R

28.2.21 SMB_CRXOF (SMB Clear RXOF Interrupt Register)

	SMB_CRXOF															BASE + 0x48														
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														CRXOF
RST																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CRXOF	Read this register to clear the RXOF interrupt (bit 1) of the SMBINTST register.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

28.2.22 SMB_CTXOF (SMB Clear TX_OVER Interrupt Register)

	SMB_CTXOF															BASE + 0x4C														
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																Reserved															CTXOF
RST																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CTXOF	Read this register to clear the TX_OVER interrupt (bit 3) of the SMBINTST register.	R

28.2.23 SMB_CRXREQ (SMB Clear RDREQ Interrupt Register)

	SMB_CRXREQ															BASE + 0x50														
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																Reserved															CLRDREQ
RST																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CLRDREQ	Read this register to clear the RDREQ interrupt (bit 5) of the SMBINTST register.	R

28.2.24 SMB_CTXABT (SMB Clear TX_ABRT Interrupt Register)

	SMB_CTXABT															BASE + 0x54														
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																Reserved															CTXABT
RST																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CTXABT	Read this register to clear the TX_ABRT interrupt (bit 6) of the SMB_INTST register, and the SMB_ABTSRC register.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the SMB_ABTSRC register for an exception to clearing SMB_ABTSRC.	

28.2.25 SMB_CRXDN (SMB Clear RX_DONE Interrupt Register)

	SMB_CRXDN															BASE + 0x58															
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														CRXDN
RST																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CRXDN	Read this register to clear the RX_DONE interrupt (bit 7) of the SMB_INTST register.	R

28.2.26 SMB_CACT (SMB Clear ACTIVITY Interrupt Register)

	SMB_CACT															BASE + 0x5C															
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														CACT
RST																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CACT	Reading this register clears the ACTIVITY interrupt if the SMB is not active anymore. If the SMB module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the SMBINTST register.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

28.2.27 SMB_CSTP (SMB Clear STOP Interrupt Register)

	SMB_CSTP															BASE + 0x60													
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													CSTP
RST																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CSTP	Read this register to clear the STOP interrupt (bit 9) of the SMBINTST register.	R

28.2.28 SMB_CSTT (SMB Clear START Interrupt Register)

	SMB_CSTT															BASE + 0x64													
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													CSTT
RST																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CSTT	Read this register to clear the START interrupt (bit 10) of the SMBINTST register.	R

28.2.29 SMB_CGC (SMB Clear GEN_CALL Interrupt Register)

	SMB_CGC															BASE + 0x68													
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													CGC
RST																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	CGC	Read this register to clear the GEN_CALL interrupt (bit 11) of SMBINTST register.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

28.2.30 SMB_ENABLE (SMB Enable Register)

	SMBE_NABLE															BASE + 0x6C															
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																Reserved														ABORT	SMBENB
RST																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:2	Reserved	Writing has no effect, read as zero.	R
1	ABORT	When set, the controller initiates the transfer abort. 0: ABORT not initiated or ABORT done 1: ABORT operation in progress The software can abort the SMB transfer in master mode by setting this bit. The software can set this bit only when ENABLE is already set; otherwise, the controller ignores any write to ABORT bit. The software cannot clear the ABORT bit once set. In response to an ABORT, the controller issues a STOP and flushes the Tx FIFO after completing the current transfer, then sets the TX_ABORT interrupt after the abort operation. The ABORT bit is cleared automatically after the abort operation.	R/W
0	SMBENB	Controls whether the SMB is enabled. 0: Disables SMB (TX and RX FIFOs are held in an erased state) 1: Enables SMB Software can disable SMB while it is active. However, it is important that care be taken to ensure that SMB is disabled properly. When SMB is disabled, the following occurs: – The TX FIFO and RX FIFO get flushed. – Status bits in the SMB_INTST register are still active until SMB goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the SMB stops the current transfer at the end of the current byte and does not acknowledge the transfer.	R/W

28.2.31 SMB_ST(SMB Status Register)

This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt.

When the SMB is disabled by writing 0 in bit 0 of the SMB_ENABLE register:

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

– Bits 1 and 2 are set to 1
– Bits 3 and 4 are set to 0

When the master or slave state machine goes to idle and SMB_ENABLE[0]=0:

– Bits 5 and 6 are set to 0

	SMB_ST																BASE + 0x70													
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved									SLVACT	MSTACT	RFF	RFNE	TFE	TFNF	ACT
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Name	Description	R/W
15:7	Reserved	Writing has no effect, read as zero.	R
6	SLVACT	Slave FSM Activity Status. 0: Slave FSM is in IDLE state so the Slave part of SMB is not Active 1: Slave FSM is not in IDLE state so the Slave part of SMB is Active	R
5	MSTACT	Master FSM Activity Status. 0: Master FSM is in IDLE state so the Master part of SMB is not Active 1: Master FSM is not in IDLE state so the Master part of SMB is Active	R
4	RFF	Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0: Receive FIFO is not full 1: Receive FIFO is full	R
3	RFNE	Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. 0: Receive FIFO is empty 1: Receive FIFO is not empty	R
2	TFE	Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty	R
1	TFNF	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0: Transmit FIFO is full 1: Transmit FIFO is not full	R
0	ACT	SMB Activity Status. The OR of SLVACT and MSTACT bits.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

28.2.32 SMB_TXFLR(SMB Transmit FIFO Level Register)

This register contains the number of valid data entries in the transmit FIFO buffer. It is cleared whenever:

- The SMB is disabled
- There is a transmit abort—that is, TX_ABRT bit is set in the SMB_RAW_INTR_STAT register
- The slave bulk transmit mode is aborted

The register increments whenever data is placed into the transmit FIFO and decrements when data is taken from the transmit FIFO.

		BASE+0X74					
Bit		5	4	3	2	1	0
	Reserved	TXFLR					
RST		0	0	0	0	0	0

Bits	Name	Description	R/W
31:6	Reserved	Reserved.	N/A
5:0	TXFLR	Contains the number of valid data entries in the transmit FIFO	R

28.2.33 SMB_RXFLR(SMB Receive FIFO Level Register)

This register contains the number of valid data entries in the receive FIFO buffer. It is cleared whenever:

- The SMB is disabled
- Whenever there is a transmit abort caused by any of the events tracked in SMB_ABTSRC

The register increments whenever data is placed into the receive FIFO and decrements when data is taken from the receive FIFO.

		BASE+0X78					
Bit		5	4	3	2	1	0
	Reserved	RXFLR					
RST		0	0	0	0	0	0

Bits	Name	Description	R/W
31:6	Reserved	Reserved.	N/A
5:0	RXFLR	Contains the number of valid data entries in the receive FIFO	R

28.2.34 SMB_SDAHD (SMB SDA Hold Time Register)

This register controls the amount of hold time on the SDA signal after a negative edge of SCL

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

in both master and slave mode, in units of APB clock period. The value programmed must be greater than the minimum hold time in each mode for the value to be implemented—one cycle in master mode, seven cycles in slave mode. Writes to this register succeed only when SMB_ENABLE[0]=0.

The programmed SDA hold time cannot exceed at any time the duration of the low part of scl. Therefore the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the scl period measured in APB clock cycles.

	SMB_SDAHD																BASE + 0x7C															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SDAHD															
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	Reserved	Reserved.	N/A
15:0	SDAHD	SMB Hold Time. Sets the required SDA hold time in units of APB clock period.	RW

28.2.35 SMB_ABTSRC (SMB Transmit Abort Source Register)

This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the SMBCTXABT register or the SMBCINT register is read. To clear Bit 9, the source of the SBYTE_NORSTRT must be fixed first; RESTART must be enabled (SMB_CON[5]=1), the SPECIAL bit must be cleared (SMB_TAR[11]), or the GC_OR_START bit must be cleared (SMB_TAR[10]). Once the source of the SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

	SMB_ABTSRC																BASE + 0x80															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TX_FLUSH_CNT								Reserved							USER_ABRT	SLVRD_INTX	SLV_ARBLOST	SLVFLUSH_TXFIFO	ARB_LOST	ABRT_MASTER_DIS	ABRT_10B_RD_NORSTRT	SBYTE_NORSTRT	ABRT_HS_NORSTRT	SBYTE_ACKDET	ABRT_HS_ACKDET	ABRT_GCALL_READ	ABRT_GCALL_NOCK	ABRT_TXDATA_NOACK	ABRT_10ADDR2_NOACK	ABRT_10ADDR1_NOACK	ABRT_7B_ADDR_NOACK
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
31:24	TX_FLUSH_CNT	This field preserves the TXFLR value prior to the last TX_ABRT event. It is cleared whenever SMB is disabled.	R
23:17	Reserved	Read as zero.	
16	USER_ABRT	This is a master-mode-only bit. Master has detected the transfer abort	R
15	SLVRD_INTX	1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of SMB_DC register.	R
14	SLV_ARBLOST	1: Slave lost the bus while transmitting data to a remote master. SMB_ABTSRC[12] is set at the same time. **NOTE:** Even though the slave never “owns” the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then SMB no longer own the bus. Reset value: 0x0.	R
13	SLVFLUSH_TXFIFO	1: Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO. Reset value: 0x0.	R
12	ARB_LOST	1: Master has lost arbitration, or if SMB_ABTSRC[14] is also set, then the slave transmitter has lost arbitration. **NOTE:** SMB can be both master and slave at the same time. Reset value: 0x0.	R
11	ABRT_MASTER_DIS	1: User tries to initiate a Master operation with the Master mode disabled. Reset value: 0x0.	R
10	ABRT_10B_RD_NORSTRT	1: The restart is disabled (RESTART bit (SMB_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode. Reset value: 0x0.	R
9	SBYTE_NORSTRT	To clear Bit 9, the source of the SBYTE_NORSTRT must be fixed first; restart must be enabled (SMB_CON[5]=1), the SPECIAL bit must be cleared (SMB_TAR[11]), or the GC_OR_START bit must be cleared (SMB_TAR[10]). Once the source of the SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted. 1: The restart is disabled (RESTART bit (SMB_CON[5]) = 0) and the user is trying to send a START Byte. Reset value: 0x0.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

8	ABRT_HS_NORSTRT	1: The restart is disabled (RESTART bit (SMB_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode. Reset value: 0x0.	R
7	SBYTE_ACKDET	1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). Reset value: 0x0.	R
6	ABRT_HS_ACKDET	1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). Reset value: 0x0.	R
5	ABRT_GCALL_READ	1: SMB in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (SMBDC[9] is set to 1). Reset value: 0x0.	R
4	ABRT_GCALL_NOACK	1: SMB in master mode sent a General Call and no slave on the bus acknowledged the General Call. Reset value: 0x0.	R
3	ABRT_TXDATA_NOACK	1: This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledgement from the remote slave(s). Reset value: 0x0.	R
2	ABRT_10ADDR2_NOACK	1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave. Reset value: 0x0.	R
1	ABRT_10ADDR1_NOACK	1: Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. Reset value: 0x0.	R
0	ABRT_7B_ADDR_NOACK	1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. Reset value: 0x0.	R

28.2.36 SMB_SLV_DATA_NACK_ONLY (SMB Generate Slave Data NACK Register)

The register is used to generate a NACK for the data part of a transfer when SMB is acting as a slave-receiver. This register only exists when the SMB_SLV_DATA_NACK_ONLY parameter is set to 1. When this parameter disabled, this register does not exist and writing to the register's address has no effect.

A write can occur on this register if either of the following conditions are met:

■ DW_apb_i2c is disabled (SMB_ENABLE[0] = 0)

■ Slave part is inactive (SMB_STATUS[6] = 0)

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	SMB_SLV_DATA_NACK_ONLY															BASE + 0x84														
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													NACK
RST																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	NACK	Generate NACK. This NACK generation only occurs when SMB is a slave receiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. ■ 1 = generate NACK after data byte received ■ 0 = generate NACK/ACK normally	R/W

Note: The SMB_STATUS[6] is a register read-back location for the internal slv_activity signal; the user should poll this before writing the smb_slv_data_nack_only bit.

28.2.37 SMB_DMACR (SMB DMA Control Register)

The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of SMB_ENABLE.

	SMB_DMACR															BASE + 0x88														
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													TDEN	RDEN
RST																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:2	Reserved	Writing has no effect, read as zero.	R
1	TDEN	**Transmit DMA Enable**. This bit enables/disables the transmit DMA channel. 0: Transmit DMA disabled 1: Transmit DMA enabled Reset value: 0x0.	R/W
0	RDEN	**Receive DMA Enable**. This bit enables/disables the receive DMA channel.	R/W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: Receive DMA disabled 1: Receive DMA enabled Reset value: 0x0.	

28.2.38 SMB_DMATDLR (SMB DMA Transmit Data Level Register)

	SMB_DMACR																BASE + 0x8c													
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved										TDLR					
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:5	Reserved	Writing has no effect, read as zero.	R
4:0	TDLR	**DMA Transmit Data Level**. This bit field controls the level at which a DMA request is made by the transmit logic. The dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value.	R/W

28.2.39 SMB_DMARDLR (SMB DMA Transmit Data Level Register)

	SMB_DMACR																BASE + 0x90													
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved										RDLR					
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:5	Reserved	Writing has no effect, read as zero.	R
4:0	RDLR	**DMA Receive Data Level**. This bit field controls the level at which a DMA request is made by the receive logic. The dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1.	R/W

28.2.40 SMB_SDASU (SMB SDA Setup Register)

This register controls the amount of time delay (in terms of number of APB clock periods) introduced in the rising edge of SCL, relative to SDA changing, when SMB services a read request in a

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

slave-transmitter operation. The relevant SMB requirement is $t_{SU:DAT}$(*NOTE 5*)as detailed in the I2C Bus Specification(Please Google "*UM10204 pdf*").

NOTE: The length of setup time is calculated using [(SMB_SDASU - 1) * (apb_clk_period)], so if the user requires 10 apb clock periods of setup time, they should program a value of 11. The SMB_SDA_SETUP register is only used by the SMB when operating as a slave transmitter

NOTE 5: A Fast-mode SMB-bus device can be used in a Standard-mode SMB-bus system, but the requirement $t_{SU;DAT}$ >= 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\ max}$ + $t_{SU;DAT}$ = 1000 +250 =1250 ns (according to the Standard-mode SMB-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time(Please refer NXP Semiconductors, *UM10204: I2C-Bus specification and user manual (Rev.6--4 April 2014), Table 10, Fig 38*)

	SMB_SDASU															BASE + 0x94													
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																							SDASU						
RST																0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Bits	Name	Description	R/W
15:8	Reserved	Writing has no effect, read as zero.	R
7:0	SDASU	SDA Setup. It is recommended that if the required delay is 1000ns, then for an APB clock frequency of 10 MHz, SMBSDASU should be programmed to a value of 11.	R/W

28.2.41 SMB_ACKGC (SMB ACK General Call Register)

The register controls whether SMB responds with an ACK or NACK when it receives an SMB General Call address.

	SMB_ACKGC															BASE + 0x98													
Bit																15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													ACKGC
RST																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	R/W
15:1	Reserved	Writing has no effect, read as zero.	R
0	ACKGC	ACK General Call. When set to 1, SMB responds with an ACK when it receives a General Call. When set to 0, the SMB does not generate General Call interrupts.	R/W

28.2.42 SMB_ENBST (SMB Enable Status)

The register is used to report the SMB hardware status when the SMB_ENABLE[0] is set from 1 to 0; that is, when SMB is disabled.

If SMB_ENABLE[0] has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.

If SMB_ENABLE[0] has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as '0'.

Note: When SMB_ENABLE[0] has been set to 0, a delay occurs for bit 0 to be read as 0 because disabling the SMB depends on SMB bus activities.

	SMB_ENBST																BASE + 0x9C															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													SLVRDLST	SLVDISB	SMBEN
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
15:3	Reserved	Writing has no effect, read as zero.	R
2	SLVRDLST	Slave Received Data Lost. This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an SMB transfer due to the setting of SMB_ENABLE[0] from 1 to 0. When read as 1, SMB is deemed to have been actively engaged in an aborted SMB transfer (with matching address) and the data phase of the SMB transfer has been entered, even though a data byte has been responded with a NACK. **NOTE:** If the remote SMB master terminates the transfer with a STOP condition before the SMB has a chance to NACK a transfer, and SMB_ENABLE[0] has been set to 0, then this bit is also set to 1. When read as 0, SMB is deemed to have been disabled without being actively involved in the data phase of a Slave-Receiver transfer. **NOTE:** The CPU can safely read this bit when SMB_ENABLE[0] is read as 0. Reset value: 0x0.	R
1	SLVDISB	Slave Disabled While Busy (Transmit, Receive). This bit indicates if a potential or active Slave operation has been aborted due to the setting of the SMB_ENABLE register from 1 to 0. This bit is set when the CPU writes a 0 to the SMB_ENABLE register while: (a) SMB is receiving the	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		address byte of the Slave-Transmitter operation from a remote master; OR, (b) address and data bytes of the Slave-Receiver operation from a remote master. When read as 1, SMB is deemed to have forced a NACK during any part of an SMB transfer, irrespective of whether the SMB address matches the slave address set in SMB (SMBSAR register) OR if the transfer is completed before SMBENB is set to 0 but has not taken effect. **NOTES:** 1 If the remote SMB master terminates the transfer with a STOP condition before the SMB has a chance to NACK a transfer, and SMBENB has been set to 0, then this bit will also be set to 1. When read as 0, SMB is deemed to have been disabled when there is master activity, or when the SMB bus is idle. 2 The CPU can safely read this bit when SMB_ENABLE[0] is read as 0. Reset value: 0x0.	
0	SMBEN	When read as 1, SMB is deemed to be in an enabled state. When read as 0, SMB is deemed completely inactive.	R

28.2.43 SMB_FS_SPKLEN (SMB SS and FS Spike Suppression Limit Register)

This register is used to store the duration, measured in APB clock cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes. This register must be programmed with a minimum value of 1.

	SMB_FS_SPKLEN																BASE + 0xA0							
Bit																	7	6	5	4	3	2	1	0
																	FSSPKLEN							
RST																	0	0	0	0	0	0	0	1

Bits	Name	Description	R/W
7:0	FSSPKLEN	This register sets the duration, measured in SMB device clock cycles, of the longest value in the SCL or SDA lines that are filtered out by the spike suppression logic. This register can be written only when the SMB interface is disabled. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted, results in 1 being set.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

28.2.44 SMB_HS_SPKLEN (SMB HS Spike Suppression Limit Register)

This register is used to store the duration, measured in APB clock cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in HS modes. This register must be programmed with a minimum value of 1.

	SMB_HS_SPKLEN															BASE + 0xA4								
Bit																						7	6	5	4	3	2	1	0
																						FSSPKLEN							
RST																						0	0	0	0	0	0	0	1

Bits	Name	Description	R/W
7:0	HSSPKLEN	This register sets the duration, measured in SMB device clock cycles, of the longest value in the SCL or SDA lines that are filtered out by the spike suppression logic. This register can be written only when the SMB interface is disabled. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted, results in 1 being set.	RW

28.3 Operating Flow

This section provides information on the following topics:

- "Slave Mode Operation"
- "Master Mode Operation"
- "Disabling SMB"

NOTE: It is important to note that the SMB should only be set to operate as an SMB Master, or SMB Slave, but not both simultaneously. This is achieved by ensuring that bit 6 (SMBSLAVE_DISABLE) and 0 (SMBMASTER_MODE) of the SMBCON register are never set to 0 and 1, respectively.

28.3.1 SMB Behavior

The SMB can be controlled via software to be either:

- An SMB master only, communicating with other SMB slaves.

OR

- An SMB slave only, communicating with one more SMB masters.

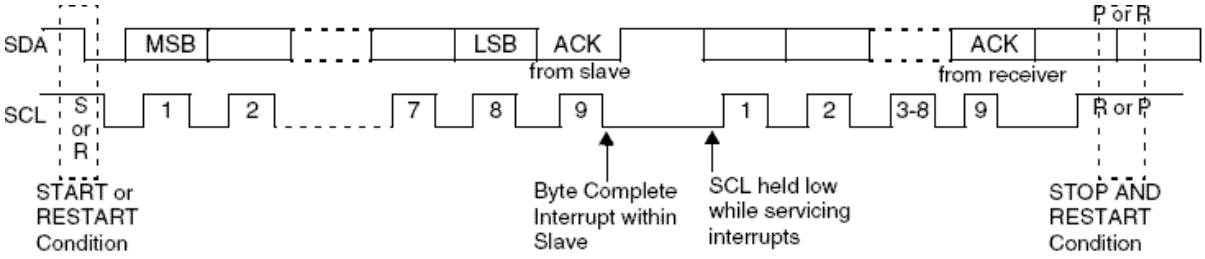
The master is responsible for generating the clock and controlling the transfer of data. The slave is responsible for either transmitting or receiving data to/from the master. The device that is receiving

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

data, which can be either a master or a slave, sends the acknowledgement of data. As mentioned previously, the SMB protocol also allows multiple masters to reside on the SMB bus and uses an arbitration procedure to determine bus ownership.

Each slave has a unique address that is determined by the system designer. When a master wants to communicate with a slave, the master transmits a START/RESTART condition that is then followed by the slave's address and a control bit (R/W) to determine if the master wants to transmit data or receive data from the slave. The slave then sends an acknowledgement (ACK) pulse after the address.

If the master (master-transmitter) is writing to the slave (slave-receiver), the receiver gets one byte of data. This transaction continues until the master terminates the transmission with a STOP condition. If the master is reading from a slave (master-receiver), the slave transmits (slave-transmitter) a byte of data to the master, and the master then acknowledges the transaction with the ACK pulse. This transaction continues until the master terminates the transmission by not acknowledging (NACK) the transaction after the last byte is received, and then the master issues a STOP condition or addresses another slave after issuing a RESTART condition.



28.3.2 Master Mode Operation

This section includes the following topics:

- "Initial Configuration"
- "Dynamic SMBTAR or SMB10BITADDR_MASTER Update"
- "Master Transmit and Master Receive"

28.3.3 Configuration

To use the SMB as a master perform the following steps:

1 Disable the SMB by writing 0 to the SMBENB register. And wait for the SMBENBST.SMBEN = 0.

2 Write to the SMB_CON register to set the speed mode supported (bits 2:1). Please note that the MATP (bit4) is NOT writable. The addressing mode is controlled by Register SMB_TAR.

3 Set the expected SCL frequency. SMB_CON.SPEED = 2'b01, only SMB_SHCNT and SMBSLCNT are needed to be configured; SMB_CON.SPEED = 2'b10, only SMB_FHCNT and SMB_FLCNT are needed to be configured.

Supposed:

T_{scl} : SMB SCL period

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

T_{SMB_clk} : SMB device clock period

$T_{min_scl_l}$: Protocol minimum SCL low time

$T_{min_scl_h}$: Protocol minimum SCL high time

Then can get the equation:

$T_{scl} = T_{SMB_clk} * ((SMB*HCNT + 8) + (SMB*LCNT + 1))$

And the following conditions should be met:

$(SMB*HCNT + 8) * T_{SMB_clk} >= T_{min_scl_h}$

$(SMB*LCNT + 1) * T_{SMB_clk} >= T_{min_scl_l}$

SMB*HCNT >= 6

SMB*LCNT >= 8

4 Write to the SMB_TAR register the address of the SMB device to be addressed. It also indicates whether a General Call or a START BYTE command is going to be performed by SMB. The addressing mode that master starts, either 7-bit or 10-bit addressing, is controlled by the SMB10BITADDR_MASTER bit field (bit 12).

5 Enable the SMB by writing a 1 into SMB_ENABLE register. And wait for the SMB_ENBST.SMBEN = 1.

6 Now write the transfer direction and data to be sent to the SMB_DC register (This can be done by DMA). If the SMB_DC register is written before the SMB is enabled, the data and commands are lost as the buffers are kept cleared when SMB is not enabled.

NOTE: For multiple SMB transfers, perform additional writes to the TX FIFO such that the TX FIFO does not become empty during the SMB transaction. If the TX FIFO is completely emptied at any stage and SMB_CON.STPHLD is 0, then further writes to the TX FIFO results in an independent SMB transaction.

28.3.4 Dynamic SMBTAR or SMB10BITADDR_MASTER Update

The SMB supports dynamic updating of the SMBTAR (bits 9:0) and SMB10BITADDR_MASTER (bit 12) bit fields of the SMBTAR register. You can dynamically write to the SMBTAR register provided the following conditions are met:

1 SMB is not enabled (SMBENB=0);

OR

2 SMB is enabled (SMBENB=1);

AND

SMB is NOT engaged in any Master (tx, rx) operation (SMBST[5]=0);

AND

SMB is enabled to operate in Master mode (SMBCON[0]=1);

AND

there are NO entries in the TX FIFO (SMBST[2]=0).

28.3.5 Master Transmit and Master Receive

The SMB supports switching back and forth between reading and writing dynamically. To transmit data,

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

write the data to be transferred to lower byte of the SMB Rx/Tx Data Buffer and Command Register (SMB_DC). The *CMD* bit (SMB_DC[8]) should be written to 0 for SMB write operations.

Subsequently, a read command may be issued by writing “don’t cares” to the lower byte of the SMBDC register, and a 1 should be written to the *CMD* bit.

28.3.6 Slave Mode Operation

This section includes the following procedures:

- “Initial Configuration”
- “Slave-Transmitter Operation for a Single Byte”
- “Slave-Receiver Operation for a Single Byte”
- “Slave-Transfer Operation For Bulk Transfers”

28.3.7 Initial Configuration

To use the SMB as a slave, perform the following steps:

1 Disable the SMB by writing a ‘0’ to bit 0 of the SMBENB register.

2 Write to the SMB_SAR register (bits 9:0) to set the slave address. This is the address to which the SMB responds.

3 Write to the SMB_CON register to specify which type of addressing is supported (7- or 10-bit by setting bit 3). Enable the SMB in slave-only mode by writing a ‘0’ into bit 6 (SMBSLAVE_DISABLE) and a ‘0’ to bit 0 (MASTER_MODE).

NOTE: Slaves and masters do not have to be programmed with the same type of addressing 7- or 10-bit address. For instance, a slave can be programmed with 7-bit addressing and a master with 10-bit addressing, and vice versa.

4 Enable the SMB by writing a ‘1’ in bit 0 of the SMB_ENB register.

NOTE: Depending on the reset values chosen, steps 2 and 3 may not be necessary because the reset values can be configured. For instance, if the device is only going to be a master, there would be no need to set the slave address because you can configure SMB to have the slave disabled after reset and to enable the master after reset. The values stored are static and do not need to be reprogrammed if the SMB is disabled.

28.3.8 Slave-Transmitter Operation for a Single Byte

When another SMB master device on the bus addresses the SMB and requests data, the SMB acts as a slave-transmitter and the following steps occur:

1 The other SMB master device initiates an SMB transfer with an address that matches the slave address in the SMB_SAR register of the SMB.

2 The SMB acknowledges the sent address and recognizes the direction of the transfer to

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

indicate that it is acting as a slave-transmitter.

3 The SMB asserts the RDREQ interrupt (bit 5 of the SMBINTST register) and holds the SCL line low. It is in a wait state until software responds.
If the RDREQ interrupt has been masked, due to SMB_INTM[5] register (MRDREQ bit field) being set to 0, then it is recommended that a hardware and/or software timing routine be used to instruct the CPU to perform periodic reads of the SMB_INTST register.
   a Reads that indicate SMB_INTST[5] (RDREQ bit field) being set to 1 must be treated as the equivalent of the RDREQ interrupt being asserted.
   b Software must then act to satisfy the SMB transfer.
   c The timing interval used should be in the order of 10 times the fastest SCL clock period the SMB can handle. For example, for 400 kb/s, the timing interval is 25us.

NOTE: The value of 10 is recommended here because this is approximately the amount of time required for a single byte of data transferred on the SMB bus.

4 If there is any data remaining in the TX FIFO before receiving the read request, then the SMB asserts a TX_ABRT interrupt (bit 6 of the SMBINTST register) to flush the old data from the TX FIFO.

NOTE: Because the SMB's TX FIFO is forced into a flushed/reset state whenever a TX_ABRT event occurs, it is necessary for software to release the SMB from this state by reading the SMB_CTXABT register before attempting to write into the TX FIFO. See register SMB_INTST for more details. If the TX_ABRT interrupt has been masked, due to of SMB_INTM[6] register (MTX_ABRT bit field) being set to 0, then it is recommended that re-using the timing routine (described in the previous step), or a similar one, be used to read the SMBINTST register.

   a Reads that indicate bit 6 (TXABT) being set to 1 must be treated as the equivalent of the TX_ABRT interrupt being asserted.
   b There is no further action required from software.
   c The timing interval used should be similar to that described in the previous step for the SMBINTST[5] register.

5 Software writes to the SMB_DC register with the data to be written (by writing a '0' in bit 8).

6 Software must clear the RDREQ and TX_ABRT interrupts (bits 5 and 6, respectively) of the SMBINTST register before proceeding.
If the RDREQ and/or TX_ABRT interrupts have been masked, then clearing of the SMB_INTST register will have already been performed when either the RDREQ or TXABT bit has been read as 1.

7 The SMB releases the SCL and transmits the byte.

8 The master may hold the SMB bus by issuing a RESTART condition or release the bus by issuing a STOP condition.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

28.3.9 Slave-Receiver Operation for a Single Byte

When another SMB master device on the bus addresses the SMB and is sending data, the SMB acts as a slave-receiver and the following steps occur:

1 The other SMB master device initiates an SMB transfer with an address that matches the SMB's slave address in the SMBSAR register.
2 The SMB acknowledges the sent address and recognizes the direction of the transfer to indicate that the SMB is acting as a slave-receiver.
3 SMB receives the transmitted byte and places it in the receive buffer.

NOTE: If the RX FIFO is completely filled with data when a byte is pushed, then an overflow occurs and the SMB continues with subsequent SMB transfers. Because a NACK is not generated, software must recognize the overflow when indicated by the SMB (by the RXOF bit in the SMBINTST register) and take appropriate actions to recover from lost data. Hence, there is a real time constraint on software to service the RX FIFO before the latter overflow as there is no way to re-apply pressure to the remote transmitting master. You must select a deep enough RX FIFO depth to satisfy the interrupt service interval of their system.

4 SMB asserts the RX_FULL interrupt (SMBINTST[2] register).
If the RX_FULL interrupt has been masked, due to setting SMB_INTM[2] register to 0 or setting SMB_TX_TL to a value larger than 0, then it is recommended that a timing routine be implemented for periodic reads of the "SMBST". Reads of the SMB_ST register, with bit 3 (RFNE) set at 1, must then be treated by software as the equivalent of the RX_FULL interrupt being asserted.
5 Software may read the byte from the SMB_DC register (bits 7:0).
6 The other master device may hold the SMB bus by issuing a RESTART condition or release the bus by issuing a STOP condition.

28.3.10 Slave-Transfer Operation For Bulk Transfers

In the standard SMB protocol, all transactions are single byte transactions and the programmer responds to a remote master read request by writing one byte into the slave's TX FIFO.

When a slave (slave-transmitter) is issued with a read request (RDREQ) from the remote master (master-receiver), at a minimum there should be at least one entry placed into the slave-transmitter's TX FIFO.

SMB is designed to handle more data in the TX FIFO so that subsequent read requests can take that data without raising an interrupt to get more data. Ultimately, this eliminates the possibility of significant latencies being incurred between raising the interrupt for data each time had there been a restriction of having only one entry placed in the TX FIFO.

This mode only occurs when SMB is acting as a slave-transmitter. If the remote master acknowledges

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

the data sent by the slave-transmitter and there is no data in the slave's TX FIFO, the SMB holds the SMB SCL line low while it raises the read request interrupt (RDREQ) and waits for data to be written into the TX FIFO before it can be sent to the remote master.

If the RDREQ interrupt is masked, due to bit 5 (MRDREQ) of the SMB_INTST register being set to 0, then it is recommended that a timing routine be used to activate periodic reads of the SMB_INTST register. Reads of SMB_INTST that return bit 5 (RDREQ) set to 1 must be treated as the equivalent of the RDREQ interrupt referred to in this section.

The RDREQ interrupt is raised upon a read request, and like interrupts, must be cleared when exiting the interrupt service handling routine (ISR). The ISR allows you to either write 1 byte or more than 1 byte into the TX FIFO. During the transmission of these bytes to the master, if the master acknowledges the last byte. Then the slave must raise the RDREQ again because the master is requesting for more data.

28.3.11 Disabling SMB

The register SMB_ENBST is added to allow software to unambiguously determine when the hardware has completely shutdown in response to the SMB_ENABLE register being set from 1 to 0.

28.3.12 Procedure

1 Define a timer interval (tSMB_poll) equal to the 10 times the signaling period for the highest SMB transfer speed used in the system and supported by SMB. For example, if the highest SMB transfer mode is 400 kb/s, then this tSMB_poll is 25us.
2 Define a maximum time-out parameter, MAX_T_POLL_COUNT, such that if any repeated polling operation exceeds this maximum value, an error is reported.
3 Execute a blocking thread/process/function that prevents any further SMB master transactions to be started by software, but allows any pending transfers to be completed.
NOTE: This step can be ignored if SMB is programmed to operate as an SMB slave only.
4 The variable POLL_COUNT is initialized to zero.
5 Set SMBENB to 0.
6 Read the SMB_ENBST register and test the SMB_ENABLE[0]. Increment POLL_COUNT by one. If POLL_COUNT >= MAX_T_POLL_COUNT, exit with the relevant error code.
7 If SMB_ENBST[0] is 1, then sleep for tSMB_poll and proceed to the previous step. Otherwise, exit with a relevant success code.

28.3.13 Summary the condition could flush TX FIFO

1. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset.
2. TX_ABRT event occurs. The TX FIFO remains in this flushed state until the register SMB_CTXABT is read. Once this read is performed, the TX FIFO is then ready to

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

accept

more data bytes from the APB interface.

3. When act as a slave, the slave has received a read command and some data exists in the

TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.

28.3.14 The condition could generate START, STOP and RESTART

A STOP condition is generated only when the user specifically requests it by setting bit 9 (Stop bit) of the command written to SMB_DC register. Naturally, if the last byte send out does not set bit 9 (Stop bit), the component does not generate a STOP if the Tx FIFO becomes empty; in this situation the component holds the SCL line low, stalling the bus until a new entry is available in the Tx FIFO

Figure 28-1 illustrates the behavior of the SMB when the Tx FIFO becomes empty while operating as a master transmitter, as well as showing the generation of a STOP condition.

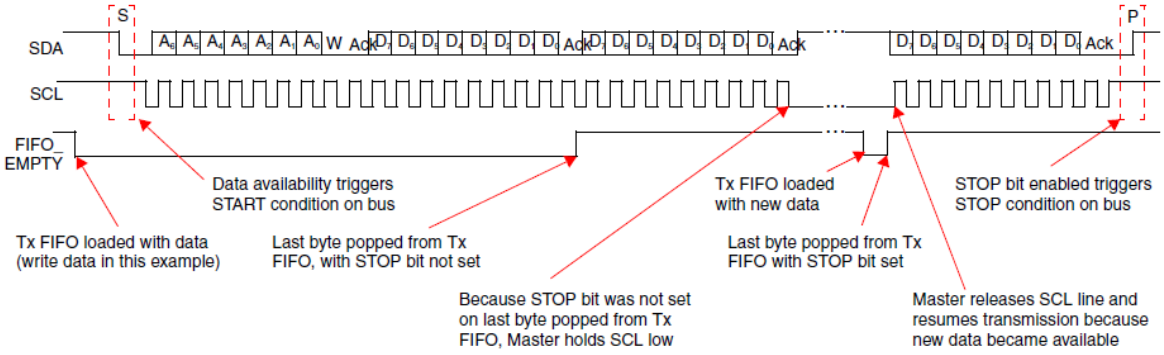


Figure 28-1 Master Transmitter — Tx FIFO Empties/STOP Generation

Figure 28-2 illustrates the behavior of the SMB when the Tx FIFO becomes empty while operating as a master receiver, as well as showing the generation of a STOP condition.

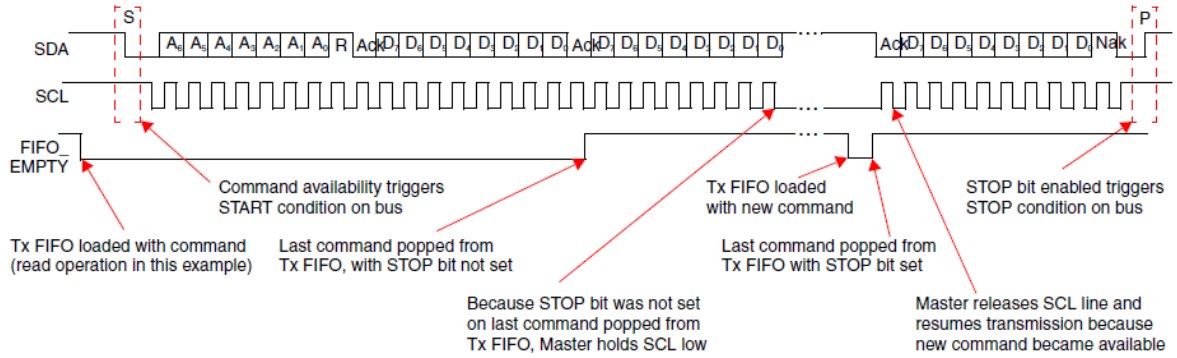


Figure 28-2 Master Receiver — Tx FIFO Empties/STOP Generation

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 28-3 and Figure 28-4 illustrate configurations where the user can control the generation of RESTART conditions on the SMB bus. If bit 10 (Restart) of the SMB_DC register is set and the restart capability is enabled (IC_RESTART_EN=1), a RESTART is generated before the data byte is written to or read from the slave. If the restart capability is not enabled a STOP followed by a START is generated in place of the RESTART. Figure 28-3 illustrates this situation during operation as a master transmitter.

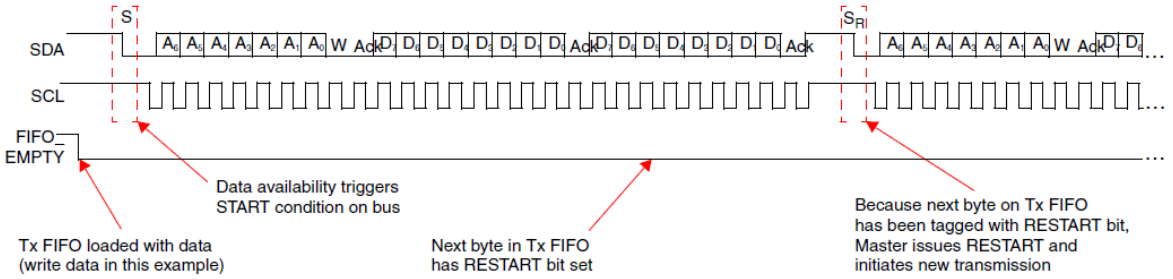


Figure 28-3 Master Transmitter — Restart bit of SMB_DC is set

Figure 28-4 illustrates the same situation, but during operation as a master receiver.

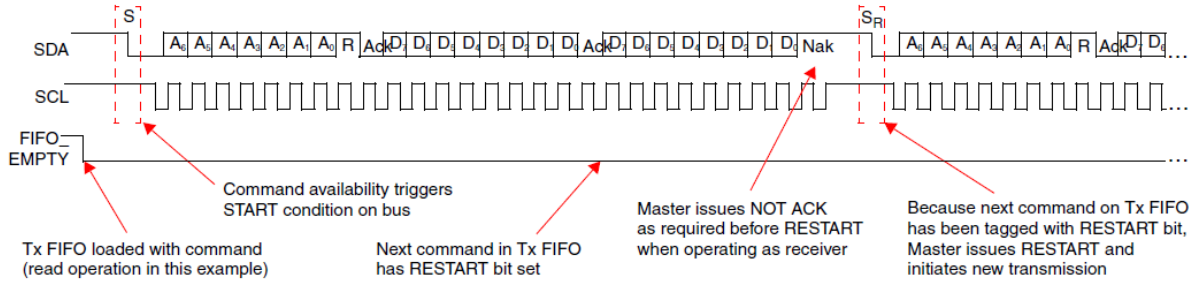


Figure 28-4 Master Receiver — Restart bit of SMB_DC is set

Figure 28-5 illustrates operation as a master transmitter where the Stop bit of the SMB_DC register is set and the Tx FIFO is not empty

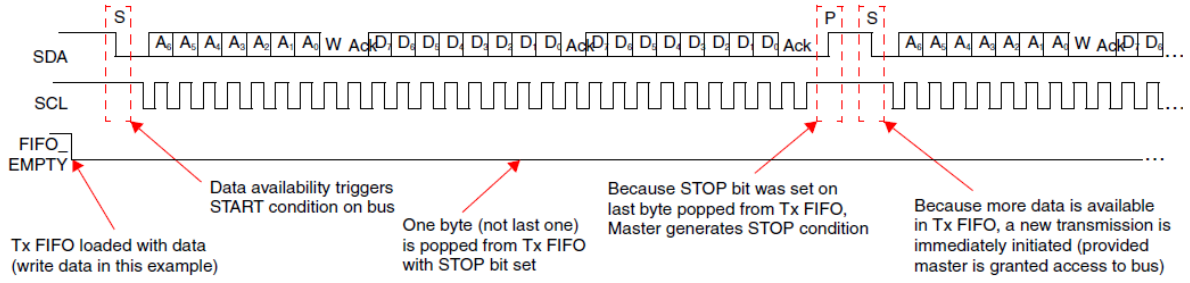


Figure 28-5 Master Transmitter — Stop Bit of SMB_DC Set/Tx FIFO Not Empty

Figure 28-6 illustrates operation as a master transmitter where the first byte loaded into the Tx FIFO is allowed to go empty with the Restart bit set.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

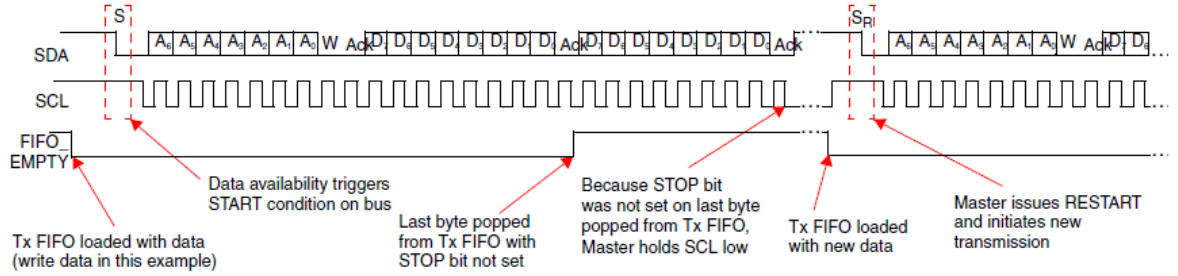


Figure 28-6 Master Transmitter — First Byte Loaded Into Tx FIFO Allowed to Empty, Restart Bit Set

Figure 28-7 illustrates operation as a master receiver where the Stop bit of the SMB_DC register is set and the Tx FIFO is not empty

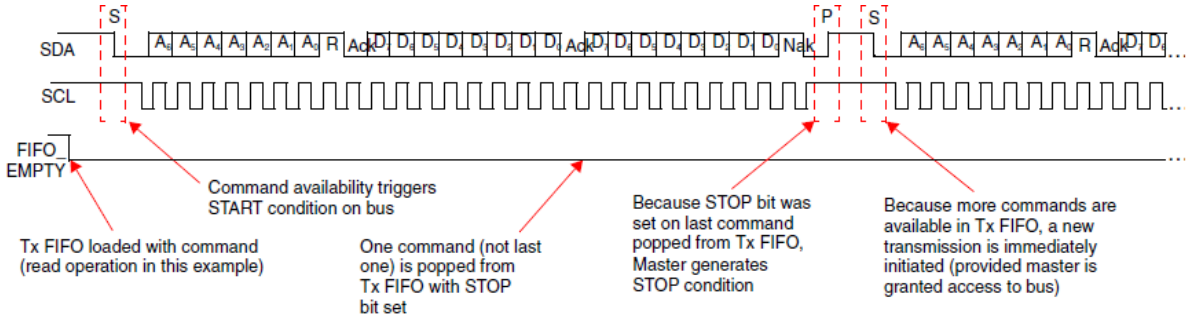


Figure 28-7 Master Receiver — Stop Bit of IC_DATA_CMD Set/Tx FIFO Not Empty

Figure 28-8 illustrates operation as a master receiver where the first command loaded after the Tx FIFO is allowed to empty and the Restart bit is set

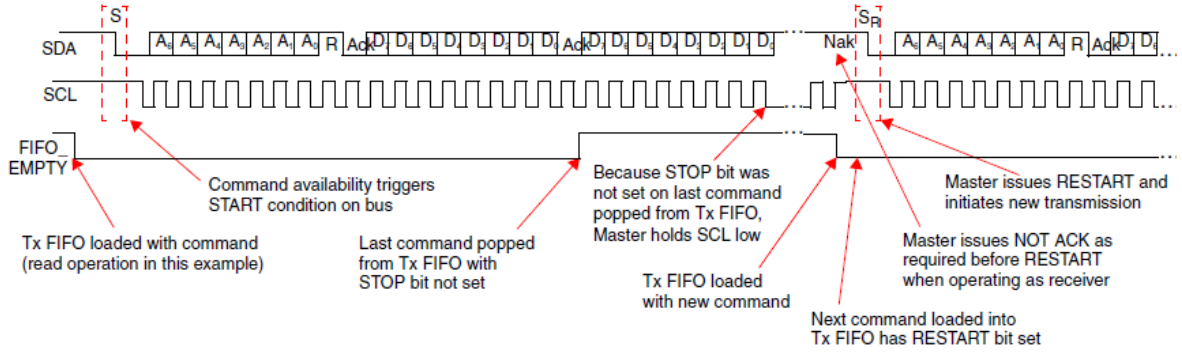


Figure 28-8 Master Receiver — First Command Loaded After Tx FIFO Allowed to Empty/Restart Bit Set

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

29 Smart Card Controller

29.1 Overview

Smart Card Controller (SCC) interface is a primary device and communications interface for kinds of IC cards. The SCC interface supports communication with smart cards as specified in standard ISO7816-3. There are two SCC interfaces integrated in this SOC. And they perform the same functions. The SCC interface supports T=0 and T=1 protocol defined in ISO7816-3.

Software controls the session between the SCC interface and the card by SCC registers. Choosing protocol type and parameters, receiving and sending a byte to/from the card, activating/deactivating the card, and similar operations are accomplished with read/write operations to SCC registers. Transforming byte convention (inverse to direct and vice-versa, according to the session convention) is performed within SCC. Hence, software does not have to perform format inversion before character receipt. The SCC interface provides functionality to support the above standards, but it is the responsibility of software to ensure the standards are met.

Features:

- Supports normal card and UIM card.
- 8-bit, 16-level receive-/transmit- FIFO.
- Supports asynchronous character (T=0) communication modes.
- Supports asynchronous block (T=1) communication modes.
- Supports setting of clock-rate conversion factor F (372, 512, 558, etc.), and bit-rate adjustment factor D (1, 2, 4, 8, 16, 32, 12, 20, etc.).
- Supports extra guard time waiting.
- Auto-error detection in T=0 receive mode.
- Auto-character repeat in T=0 transmit mode.
- Transforms inverted format to regular format and vice versa.
- Support stop clock function in some power consuming sensitive applications.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

29.2 Pin Description

Table 29-1 Smart Card Controller Pins Description

Name	I/O	Description
SCC_CLK	Output	Serial clock connects SCC and the card.
SCC_DAT	Input/Output	Data communication pin.

29.3 Register Description

Conventions:

9. Register Address = Base + Address offset
10. The registers can be read and written by APB bus
11. Register read/write attribute

    R - Read only

    W - Write only

    RW - read and write

    RCW - read and write, but clear to 0 by read

    RSW - read and write, but set to 1 by read

    RWC - read and write, clear to 0 by write 1, write 0 has no effect

    RWS - read and write, set to 1 by write 1, write 0 has no effect

    RC - read only, and clear to 0 by read

    RS - read only, and set to 1 by read

    SPEC - special access method, relate to its description
12. Reset Value

    1 - reset to 1

    0 - reset to 0

    ? - value unknown after reset

Table 29-2 Smart Card Controller Registers Description

Name	RW	Reset Value	Address	Access Size
SCCDR	RW	0x??	0x10040000	8
SCCFDR	R	0x00	0x10040004	8
SCCCR	RW	0x00000000	0x10040008	32
SCCSR	RW	0x8000	0x1004000C	16
SCCTFR	RW	0x0173	0x10040010	16
SCCEGTR	RW	0x00	0x10040014	8
SCCECR	RW	0x00000000	0x10040018	32
SCCRTOR	RW	0x00	0x1004001C	8

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

29.3.1 Transmit/Receive FIFO Data Register (SCCDR)

	SCCDR																													0x10040000
Bit																								7	6	5	4	3	2	1	0
																								DR						
RST																								?	?	?	?	?	?	?	?

Bits	Name	Description	RW
7:0	DR	Data port of HW FIFO.	RW

29.3.2 FIFO Data Count Register (SCCFDR)

	SCCFDR																													0x10040004
Bit																								7	6	5	4	3	2	1	0
																								Reserved			R			
RST																								0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:5	Reserved		R
4:0	R	Characters resisted in FIFO	R

29.3.3 Control Register (SCCCR)

	SCCCR																														0x10040008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCCE	TRS	T2R	Reserved			FDIV		FLUSH	Reserved					TRIG		TP	CONV	TXIE	RXIE	TENDIE	RTOIE	ECIE	EPIE	RETIE	EOIE	Reserved		TSEND	PX		CLKSTP
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	SCCE	Enables or disables SCC. When disable it, the SCC_CLK will be stopped.	RW
30	TRS	Transmit or Receive Select. 0 – Reception mode. 1 – Transmission mode.	RW
29	T2R	Auto-T2R support. T2R means Transmit turn to Reception. 0 – controlled by SW. 1 – controlled by HW.	RW
28:26	Reserved		R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td>25:24</td><td>FDIV</td><td>Frequency Divider Select.<table><tr><th></th><th>SCC_CLK frequency</th></tr><tr><td>00</td><td>Same as device clk</td></tr><tr><td>01</td><td>Half of device clk</td></tr><tr><td>10</td><td>¼ of device clk</td></tr><tr><td>11</td><td>Reserved</td></tr></table></td><td>RW</td></tr>
<tr><td>23</td><td>FLUSH</td><td>Flush FIFO. 0 – Does not empty the Rx/Tx FIFO. 1 – Empty the Rx/Tx FIFO.</td><td>RW</td></tr>
<tr><td>22:18</td><td>Reserved</td><td></td><td>R</td></tr>
<tr><td>17:16</td><td>TRIG</td><td>Receive/Transmit FIFO trigger.<table><tr><th></th><th>Trigger Value</th></tr><tr><td>00</td><td>1</td></tr><tr><td>01</td><td>4</td></tr><tr><td>10</td><td>8</td></tr><tr><td>11</td><td>14</td></tr></table></td><td>RW</td></tr>
<tr><td>15</td><td>TP</td><td>Communicate protocol. 0 – T=0, 1 – T=1</td><td>RW</td></tr>
<tr><td>14</td><td>CONV</td><td>Card data transfer convention. 0 – LSB first. 1 – MSB first and inverted.</td><td>RW</td></tr>
<tr><td>13</td><td>TXIE</td><td>Tx FIFO counter meets the trigger value interrupt enable bit.</td><td>RW</td></tr>
<tr><td>12</td><td>RXIE</td><td>Rx FIFO counter meets the trigger value interrupt enable bit.</td><td>RW</td></tr>
<tr><td>11</td><td>TENDIE</td><td>Transmission finished interrupt enable bit. (Both FIFO and transmitter are empty)</td><td>RW</td></tr>
<tr><td>10</td><td>RTOIE</td><td>Reception timeout interrupt enable bit.</td><td>RW</td></tr>
<tr><td>9</td><td>ECIE</td><td>ETU counter overflow interrupt enable bit.</td><td>RW</td></tr>
<tr><td>8</td><td>EPIE</td><td>Parity error interrupt enable bit.</td><td>RW</td></tr>
<tr><td>7</td><td>RETIE</td><td>Re-transmitting 3 times interrupt enable bit.</td><td>RW</td></tr>
<tr><td>6</td><td>EOIE</td><td>Receive overrun error interrupt enable bit.</td><td>RW</td></tr>
<tr><td>5:4</td><td>Reserved</td><td></td><td>R</td></tr>
<tr><td>3</td><td>TSEND</td><td>Receive TS character stage finished bit. 0 – TS character has not been received. 1 – TS character has been received.</td><td>RW</td></tr>
<tr><td>2:1</td><td>PX</td><td>Parameter X. SCC stop clock mode selection.<table><tr><th></th><th>SCC clock stop</th></tr><tr><td>00</td><td>Does not support SCC clock stop.</td></tr><tr><td>01</td><td>SCC_CLK stops at state low.</td></tr><tr><td>10</td><td>SCC_CLK stops at state high.</td></tr><tr><td>11</td><td>Reserved</td></tr></table></td><td>RW</td></tr>
<tr><td>0</td><td>CLKSTP</td><td>SCC clock stop. 0 – SCC has left or is leaving clock stop mode. 1 – SCC has entered or is entering clock stop mode.</td><td>RW</td></tr>
</table>

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

29.3.4 Status Register (SCCSR)

	SCCSR																0x1004000C															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	TRANS	Reserved		ORER	RTO	PER	TFTG	RFTG	TEND	Reserved		RETR_3	Reserved			ECNTO
RST																	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	TRANS	Transfer status. Specifies whether the transfer is stopped or not.	R
14:13	Reserved		R
12	ORER	Receive overrun error.	RW
11	RTO	Reception timeout.	R
10	PER	Parity error.	RW
9	TFTG	Hit Tx FIFO trigger.	R
8	RFTG	Hit Rx FIFO trigger.	R
7	TEND	Transmission end. Both Tx FIFO and transmitter are empty.	RW
6:5	Reserved		R
4	RETR_3	Re-transmit exceed 3 times.	RW
3:1	Reserved		R
0	ECNTO	ETU counter overflow.	RW

29.3.5 Transmission Factor Register (SCCTFR)

	SCCTFR																0x10040010															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved					FD										
RST																	0	0	0	0	0	0	0	1	0	1	1	1	0	0	1	1

Bits	Name	Description	RW
15:11	Reserved		R
10:0	FD	Value of F/D. The initial value is 0x173(371).	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

29.3.6 Extra Guard Timer Register (SCCEGTR)

	SCCEGTR																												0x10040014							
Bit																									7	6	5	4	3	2	1	0
																									EGTR							
RST																									0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:0	EGTR	The register is corresponding with N value of ISO7816-3. Which indicates the extra-guard time of a transmission.	RW

29.3.7 ETU Counter Value Register (SCCECR)

	SCCECR																															0x10040018							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												EC																			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved		R
19:0	EC	ETU counter. Write operation will clear the internal counter automatically.	RW

29.3.8 Reception Timeout Register (SCCRTOR)

	SCCRTOS																												0x1004001C							
Bit																									7	6	5	4	3	2	1	0
																									RTOR							
RST																									0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:0	RTO	Retry times when parity error detected.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

30 Synchronous Serial Interface(SSI)

30.1 Overview

The SSI is a full-duplex synchronous serial interface and can connect to a variety of external analog-to-digital (A/D) converters, audio and telecom CODECS, and other devices that use serial protocols for transferring data. The SSI supports National's Microwire, Texas Instruments Synchronous Serial Protocol (SSP), and Motorola's Serial Peripheral Interface (SPI) protocol.

The SSI operates in master mode (the attached peripheral functions as a slave) and supports serial bit rates from 7.2 KHz to 50 MHz. Serial data formats may range from 2 to 32 bits in length. The SSI provides 128 entries deep x 32 bits wide transmit and receive data FIFOs.

The FIFOs may be loaded or emptied by the Central Processor Unit (CPU) using programmed I/O, or DMA transfers while receiving or transmitting.

30.2 Features:

- 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
- Full-duplex or transmit-only or receive-only operation
- Programmable transfer order: MSB first or LSB first
- 128 entries deep x 32 bits wide transmit and receive data FIFOs
- Configurable normal transfer mode or Interval transfer mode
- Programmable clock phase and polarity for Motorola's SSI format
- Two slave select signal (SSI_CE0 / SSI_CE1) supporting up to 2 slave devices
- Back-to-back character transmission/reception mode
- Loop back mode for testing

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

30.3 Block Diagram

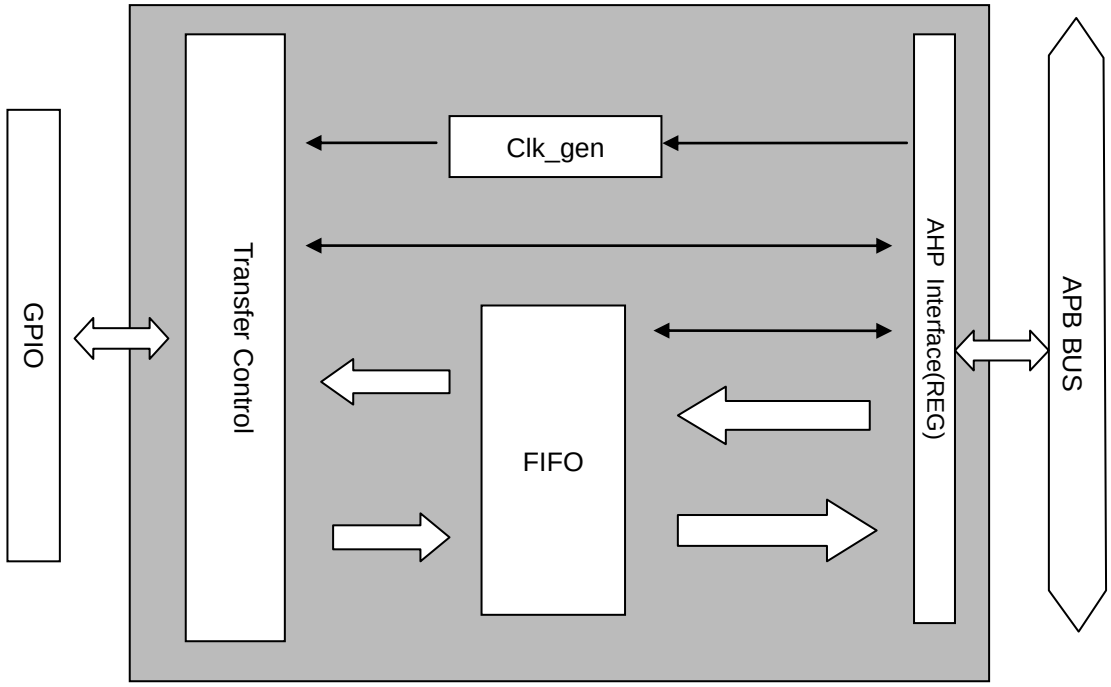


Figure 30-1 SSI Block Diagram

The APB Interface is a slave interface. It is used for register configuration and data transfer.
The FIFO block is bidirectional. There are two 128x32 memory in this block, one used as transmission data buffer, and the other used for data reception.
The Clk_gen module generate the sub-clocks for the Transfer Control module.
The Transfer Control act as the handler of SPI timing generation.

30.4 Functional Description

Serial data is transferred between the processor and external peripheral through FIFO buffers in the SSI. Data transfers to system memory are handled by either the CPU (using programmed I/O) or by DMA. Operation is full duplex - separate buffers and serial data paths permit simultaneous transfers to and from the external peripheral.

Programmed I/O transmits and receives data directly between the CPU and the transmit/receive FIFO's. The DMA controller transfers data during transmit and receive operations between memory and the FIFO's.

Transmit data is written by the CPU or DMA to the SSI's transmit FIFO. The SSI then takes the data from the FIFO, serializes it, and transmits it via the SSI_DT signal to the peripheral. Data from the peripheral is received via the SSI_DR signal, converted to parallel words and is stored in the Receive FIFO. Read operations automatically target the receive FIFO, while write operations write data to the transmit FIFO. Both the transmit and receive FIFO buffers are 128 entries deep by 17 bits wide. As the

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

received data fills the receive FIFO, a programmable threshold triggers an interrupt to the Interrupt Controller. If enabled, an interrupt service routine responds by identifying the source of the interrupt and then performs one or several read operations from the inbound (receive) FIFO buffer.

30.5 Pin Description

Table 30-1 SSI Controller Pins Description

Name	I/O	Description
SSI_CLK	Output	Serial bit-rate clock
SSI_CE0	Output	First slave select enable
SSI_DT	Output	Transmit data (serial data out)
SSI_DR	Input	Receive data (serial data in)

SSI_CLK is the bit-rate clock driven from the SSI to the peripheral. SSI_CLK is toggled only when data is actively being transmitted and received.
SSI_CE0 or SSI_CE1 are the frame signal, indicating the begin and the end of a serialized data word.
SSI_DT and SSI_DR are the Transmit and Receive serial data lines.
SSI_GPC is general-purpose control signal, synchronized with SSI_CLK, can be used for LCD control.

30.6 Data Formats

Four signals are used to transfer data between the processor and external peripheral. The SSI supports three formats: Motorola SPI, Texas Instruments SSP, and National Microwire. Although they have the same basic structure the three formats have significant differences, as described below:

1. SSI_CE0/SSI_CE1 varies for each protocol as follows:
   - For SPI and Microwire formats, SSI_CE0/SSI_CE1 functions as a chip select to enable the external device (target of the transfer), and is held active-low during the data transfer.
   - For SSP format, this signal is pulsed high for one serial bit-clock period at the start of each frame.
2. SSI_CLK varies for each protocol as follows:
   - For Microwire, both transmit and receive data sources switch data on the falling edge of SSI_CLK, and sample incoming data on the rising edge.
   - For SSP, transmit and receive data sources switch data on the rising edge of SSI_CLK, and sample incoming data on the falling edge.
   - For SPI, the user has the choice of which edge of SSI_CLK to use for switching outgoing data, and for sampling incoming data. In addition, the user can move the phase of SSI_CLK, shifting its active state one-half period earlier or later at the start and end of a frame.

While SSP and SPI are full-duplex protocols, Microwire uses a half-duplex master-slave messaging protocol. At the start of a frame, a 1 or 2-byte control message is transmitted from the controller to the peripheral. The peripheral does not send any data. The peripheral interprets the message and, if it is a READ request, responds with requested data, one clock after the last bit of the requesting message.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

The serial clock (SSI_CLK) only toggles during an active frame. At other times it is held in an inactive or idle state, as defined by its specified protocol.

30.6.1 Motorola's SPI Format Details

30.6.1.1 General Single Transfer Formats

The figures below show the timing of general single transfer format.

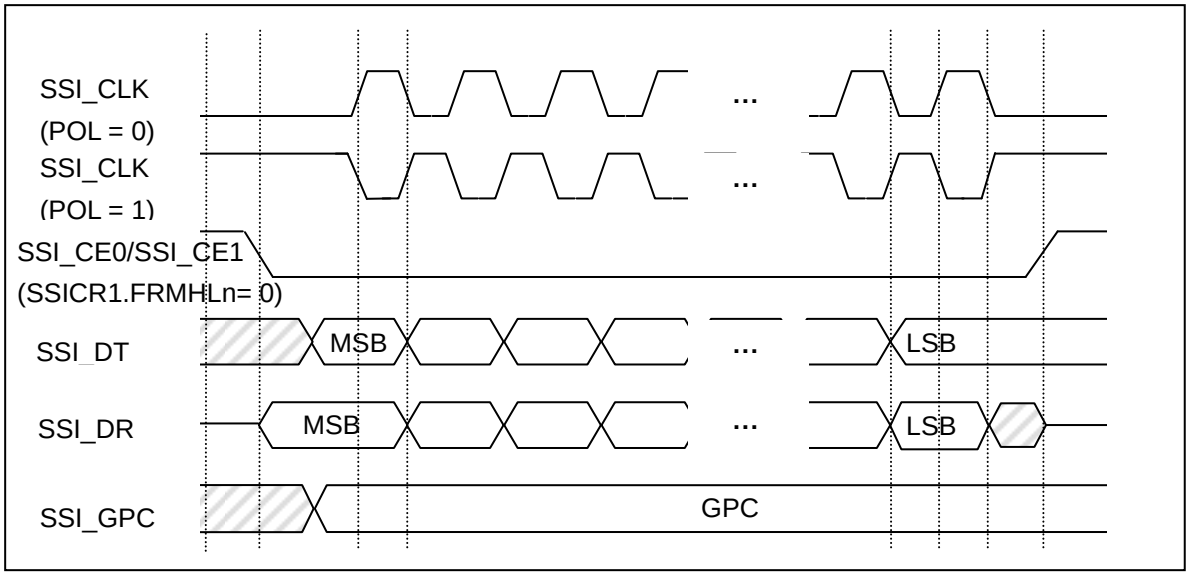


Figure 30-2 SPI Single Character Transfer Format (PHA = 0)

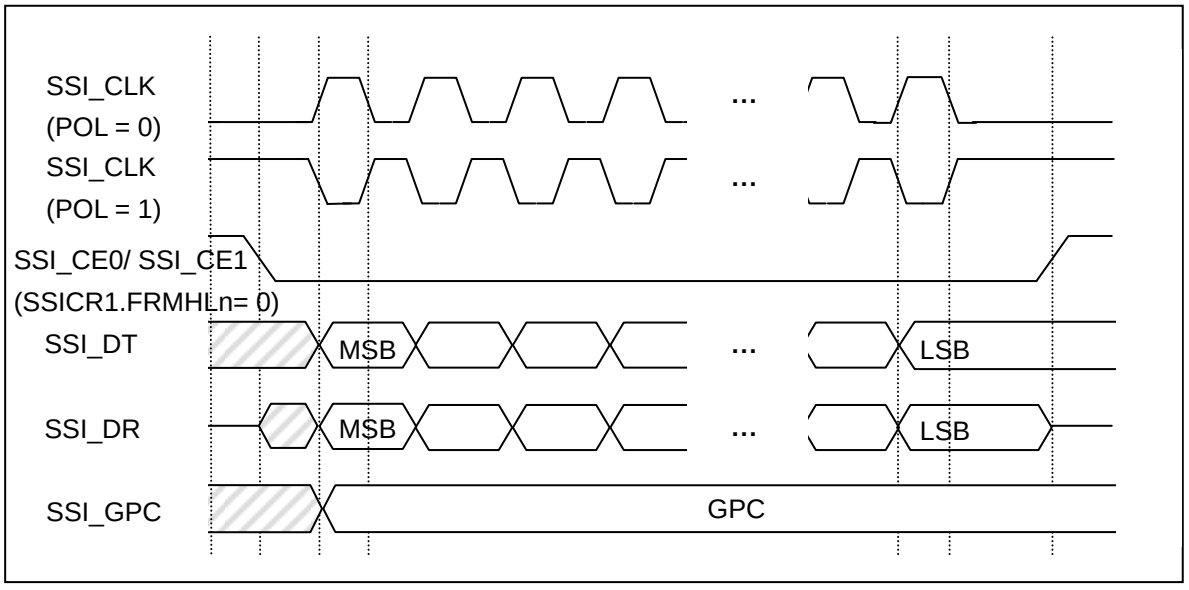


Figure 30-3 SPI Single Character Transfer Format (PHA = 1)

For SSICR1.PHA = 0, when SSICR1.TFVCK = B'00, hardware ensures the first clock edge appears one SSI_CLK period after SSI_CE0 / SSI_CE1 goes valid; when SSICR1.TCKFI = B'00, hardware

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

ensures the SSI_CE0 / SSI_CE1 negated half SSI_CLK period after last clock change edge; when SSICR1.TFVCK ≠ B'00 or SSICR1.TCKFI ≠ B'00, 1/2/3 more clock cycles are inserted.

For SSICR1.PHA = 1, when SSICR1.TFVCK = B'00, hardware ensures the first clock edge appears half SSI_CLK period after SSI_CE0 / SSI_CE1 goes valid; when SSICR1.TCKFI = B'00, hardware ensures the SSI_CE0 / SSI_CE1 negated one SSI_CLK period after last clock change edge; when SSICR1.TFVCK ≠ B'00 or SSICR1.TCKFI ≠ B'00, 1/2/3 more clock cycles are inserted.
Data is sampled from SSI_DR at every rising edge (when PHA = 0, POL = 0 or PHA = 1, POL = 1) or at every falling edge (when PHA = 0, POL = 1 or PHA = 1, POL = 0). According to SPI protocol, input data on SSI_DR should be stable at every sample clock edge.

Drive data onto SSI_DT at every rising edge (when PHA = 0, POL = 1 or PHA = 1, POL = 0) or at every falling edge (when PHA = 0, POL = 0 or PHA = 1, POL = 1).

30.6.1.2 Back-to-Back Transfer Formats

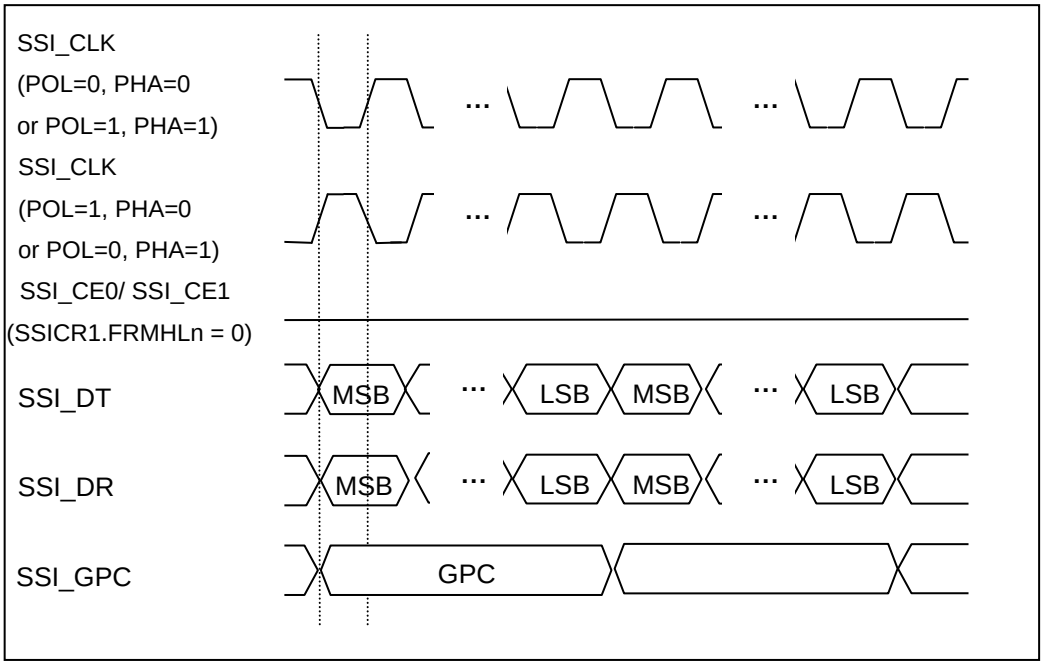


Figure 30-4 SPI Back-to-Back Transfer Format

For Motorola's SPI format transfers those continuous characters are exchanged during SSI_CE0 / SSI_CE1 being valid, the timing is illustrated in the figure (SSICR1.LFST = 0).

Back-to-back transfer is performed as transmit-only/full-duplex operation when transmit-FIFO is not empty before the completion of the last character's transfer or performed as receive-only operation.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

30.6.1.3 Frame Interval Mode Transfer Format

When in interval mode (SSIITR. IVLTM ≠ '0'), SSI always wait for an interval time (SSIITR.IVLTM), transfer fixed number of characters (SSIICR), then repeats the operation.

When SSICR0.RFINE = 1, if transmit-FIFO is still empty after the interval time, receive-only transfer will occur.

During interval-wait time, SSI stops SSI_CLK, and when SSICR1.ITFRM = 0 it negates the SSI_CE0 / SSI_CE1, when SSICR1.ITFRM = 1 it keeps asserting the SSI_CE0 / SSI_CE1.

For transfers finished with transmit-FIFO empty, if the SSI transmit-FIFO is empty before fixed number of characters being loaded to transfer (SSICR1.UNFIN must be 1), then the SSI will set SSISR.UNDR = 1; if enabled, it'll send out a SSI under-run interrupt. At the same time, SSI will hold the SSI_CE0 / SSI_CE1 and SSI_CLK signals at current status and wait for the transmit-FIFO filling. The SSI will continue transfer after transmit-FIFO being filled. The SSI always stops after completion of fixed number of characters' transfer (SSICR1.UNFIN must be 0) with transmit-FIFO empty.

For transfers finished by SSICR0.RFINC being valid set, the SSI will stop after finished current character transfer and needn't wait for a whole completion of fixed number of characters' transfer.

Two Interval transfer mode are illustrated in the following figures. In these timing diagram, SSICR1.PHA = 0, SSICR1.POL = 0 and SSIICR = 0.

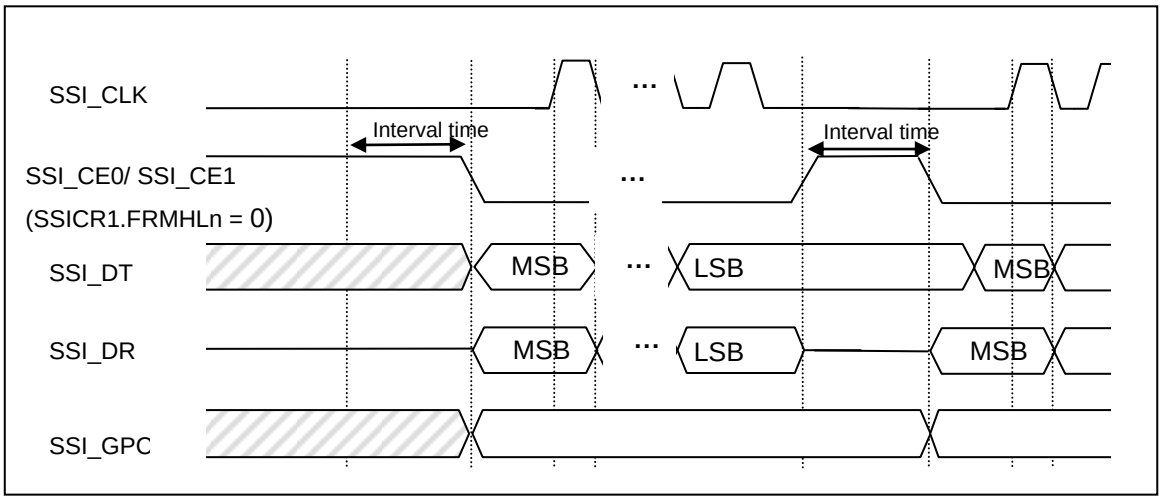


Figure 30-5 SPI Frame Interval Mode Transfer Format (ITFRM = 0, LFST = 0)

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

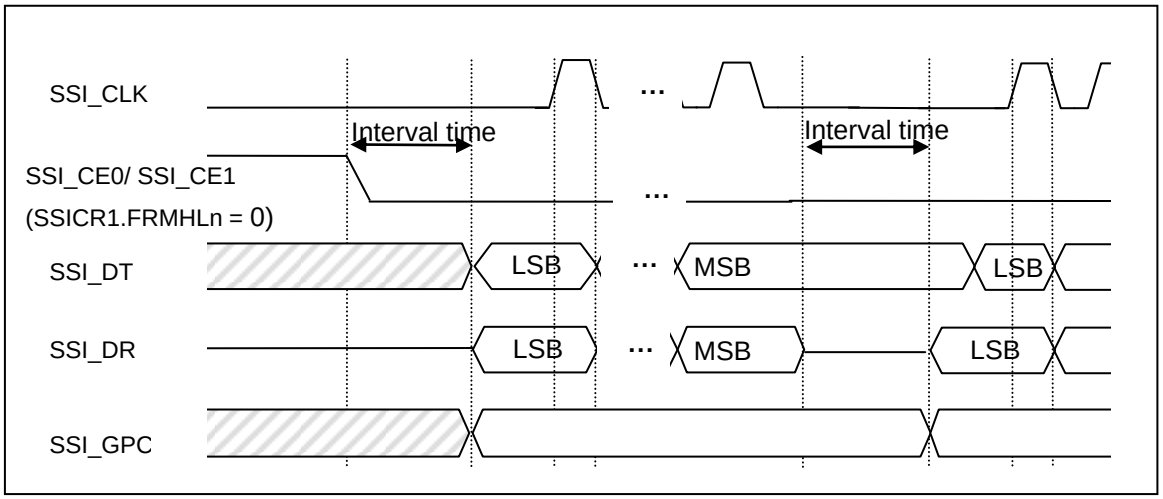


Figure 30-6 SPI Frame Interval Mode Transfer Format (ITFRM = 1, LFST = 1)

30.6.2 TI's SSP Format Details

In this format, each transfer begins with SSI_CE0 pulsed high for one SSI_CLK period. Then both master and slave drive data at SSI_CLK's rising edge and sample data at the falling edge. Data are transferred with MSB first or LSB first. At the end of the transfer, SSI_DT retains the value of the last bit sent through the next idle period.

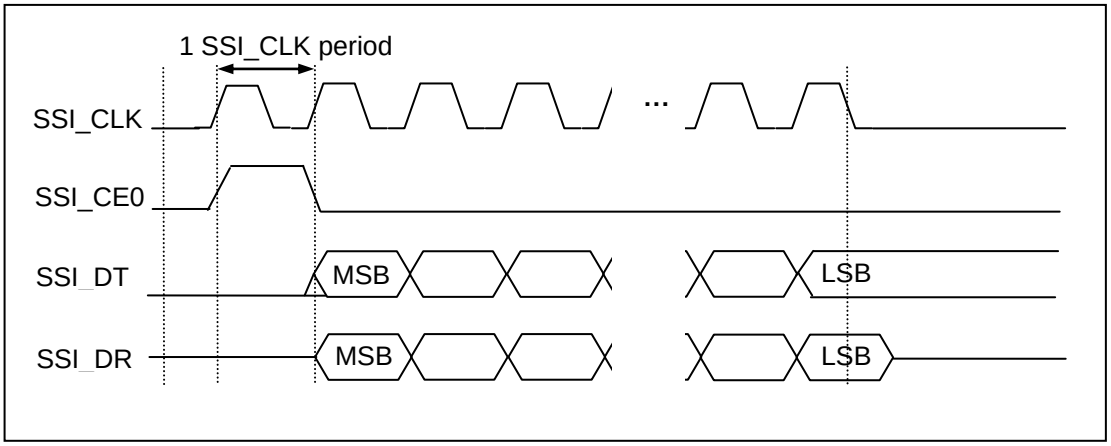


Figure 30-7 TI's SSP Single Transfer Format

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

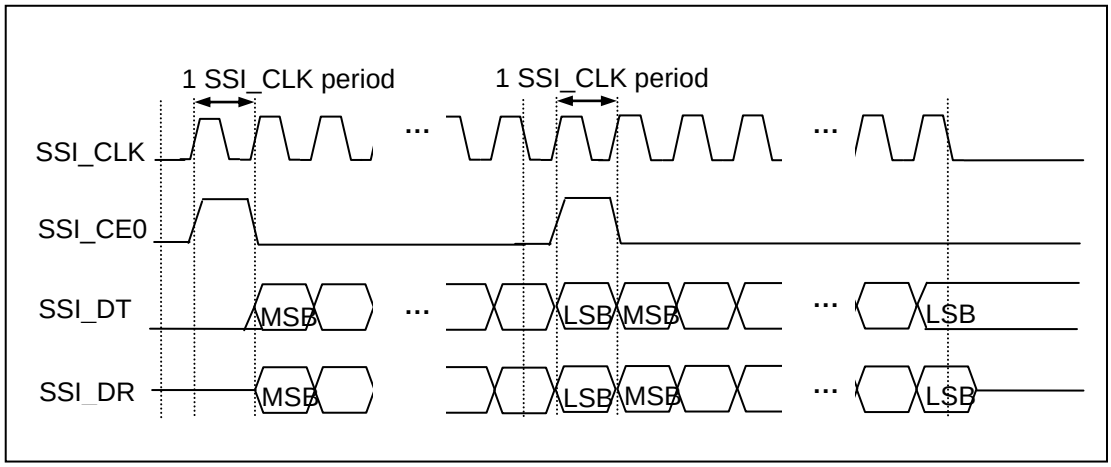


Figure 30-8 TI's SSP Back-to-back Transfer Format

30.6.3 National Microwire Format Details

It supports format 1 and format 2.

Format		Drive Edge	Sample Edge
NM1	Master	↓	↑
	Slave	↓	↑
NM2	Master	↓	↓
	Slave	↑	↑

If format 1 is selected, both master and slave drive data at SSI_CLK falling edge and sample data at the rising edge.

If format 2 is selected, master drive and sample data at SSI_CLK falling edge, slave drive and sample data at SSI_CLK rising edge.

SSI_CLK goes high midway through the command's MSB (or LSB) and continues to toggle at the bit rate. One bit clock (format 1) or half bit clock (format 2) period after the last command bit, the external slave must return the serial data requested, with MSB first (or LSB first) on SSI_DR.

SSI_CE0/SSI_CE2 de-asserts high half clock (SSI_CLK) period (and 1/2/3 additional clock periods) later.

Format 1 support back-to-back transfer, the start and end of back-to-back transfers are similar to those of a single transfer. However, SSI_CE0 / SSI_CE2 remains asserted throughout the transfer. The end of a character data on SSI_DR is immediately followed by the start of the next command byte on SSI_DT.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

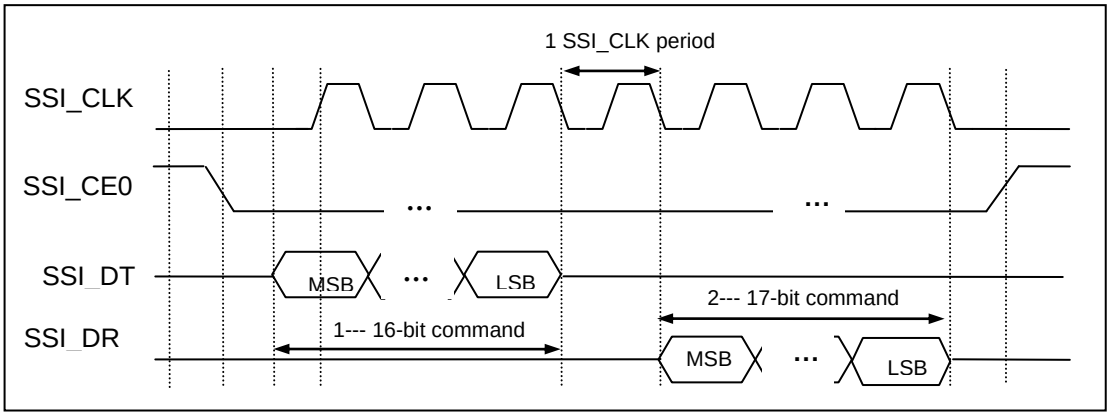


Figure 30-9 National Microwire Format 1 Single Transfer

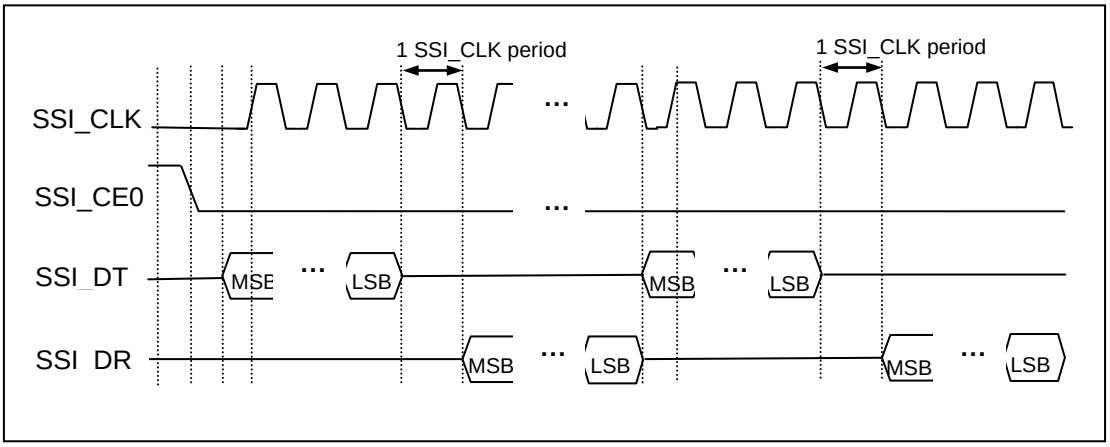


Figure 30-10 National Microwire Format 1 Back-to-back Transfer

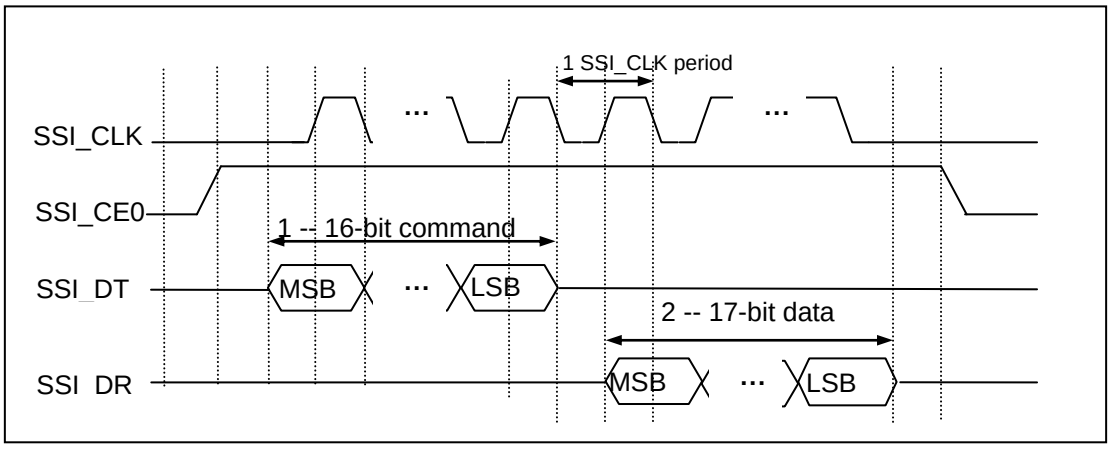


Figure 30-11 National Microwire Format 2 Read Timing

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

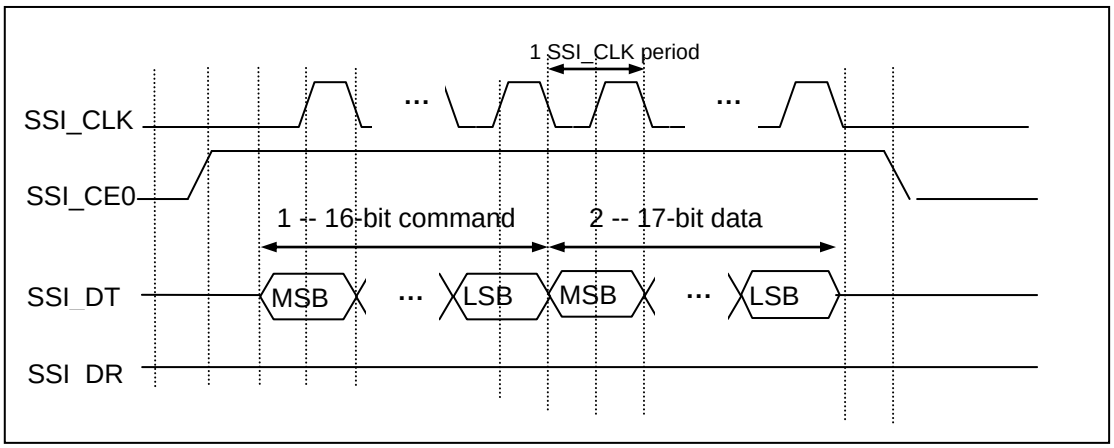


Figure 30-12 National Microwire Format 2 Write Timing

30.7 Register Description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. The registers can be read and written by APB bus
3. Register read/write attribute

   R - Read only

   W - Write only

   RW - read and write

   RCW - read and write, but clear to 0 by read

   RSW - read and write, but set to 1 by read

   RWC - read and write, clear to 0 by write 1, write 0 has no effect

   RWS - read and write, set to 1 by write 1, write 0 has no effect

   RC - read only, and clear to 0 by read

   RS - read only, and set to 1 by read

   SPEC - special access method, relate to its description
4. Reset Value

   1 - reset to 1

   0 - reset to 0

   ? - value unknown after reset

30.7.1 Register Mapping

The SSI0's registers map base address is 0x1004_3000

The SSI1's registers map base address is 0x1004_4000

The SSI has the following registers: one data, two control, one status, one bit-rate control, and two

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

interval control registers. The table lists these registers.

Table 30-2 SSI Serial Port Registers

Name	Description	Reset Value	Address Offset	Access Size
SSI.SSIDR	Date register	0x????_????	0x0000	32
SSI.SSICR0	Controller register 0	0x0000_0000	0x0004	32
SSI.SSICR1	Controller register 1	0x0008_7860	0x0008	32
SSI.SSISR	Status register	0x0000_0098	0x000C	32
SSI.SSIITR	Interval mode controller register	0x????_0000	0x0010	16
SSI.SSIICR	Interval character-per-frame controller register	0x????_??00	0x0014	8
SSI.SSIGR	Bit-rate controller register	0x????_0000	0x0018	16
SSI.SSIRCNT	Receive counter register	0x0000_0000	0x001C	32

30.7.2 SSI Data Register (SSIDR)

	SSIDR																Base + 0x0000															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	D31-D17															GPC/D16	D15-D0															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:17	D31-D17	D31-D17 to be written to/read from Transmit/Receive FIFO.	R
16	GPC/D16	This bit can be used as normal data bus bit 16 or GPC bit alternatively. When it is used as normal data bus bit, it's readable / writable; when SSI_GPC is used, it is GPC bit for SSI_GPC pin output and it's write-only.	RW
15:0	D15-D0	D15-D0 to be written to/read from Transmit/Receive FIFO. When the transfer frame length is less than 17-bit, received data is automatically right justified in the receive-FIFO and the upper unused bits are filled with '0'. For transmission, the upper unused bits of the data written into SSIDR is ignored by the transmit logic. (**NOTE:** "upper unused bits" does not include the SSIDR.GPC bit. National microwire format includes format 1 and format2, when national microwire format 2 is selected, Bit 16 of SSIDR is defined as read/write operation judge bit, if it is 0, bit 15~0 represent one read command; if it is 1, bit 15~0 represent one write command and following is the written data. So the maximum length of one command (is defined in MCOM) is 16, the maximum length of one written or read data (is defined in FLEN)	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		can be 17. Transmit-FIFO only contain one read operation command once, or one write operation command and its data once, after transmit-FIFO is empty, next command can be filled in transmit-FIFO.	

30.7.3 SSI Control Register0 (SSICR0)

	SSICR0																Base + 0x0004													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												TENDIAN		RENDIAN		SSIE	TIE	RIE	TEIE	REIE	LOOP	RFINE	RFINC	EACLRUN	FSEL	Reserved	VRCNT	TFMODE	TFLUSH	RFLUSH	DISREV
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Writing has no effect, read as zero.	R
19:18	TENDIAN	Transfer endian 0: Most significant byte in a word first, most significant bit in a byte first. 1: Most significant byte in a word first, least significant bit in a byte first. 2: Least significant byte in a word first, least significant bit in a byte first. 3: Least significant byte in a word first, most significant bit in a byte first.	
17:16	RENDIAN	Receive endian 0: Most significant byte in a word first, most significant bit in a byte first. 1: Most significant byte in a word first, least significant bit in a byte first. 2: Least significant byte in a word first, least significant bit in a byte first. 3: Least significant byte in a word first, most significant bit in a byte first	RW
15	SSIE	This bit is used to enable/disable SSI module. 0: disable; 1: enable. Clearing SSIE will not reset SSI FIFO, SSICR0, SSICR1, SSIGR, SSIITR and SSIICR automatically. Software should ensure the FIFOs/registers are properly configured and be flush/reset manually when necessary before enabling SSI.	RW
14	TIE	This bit enables/disables the transmit-FIFO half-empty interrupt TXI. 0: disable; 1: enable.	RW
13	RIE	This bit enables/disables the receive-FIFO half-full interrupt RXI. 0: disable; 1: enable.	RW
12	TEIE	This bit enables/disables the transmit-error interrupt TEI. 0: disable; 1: enable.	RW
11	REIE	This bit enables/disables the receive-error interrupt REI. 0: disable; 1: enable.	RW
10	LOOP	Used for test purpose. In loop mode, the output of SSI transmit shift register is connected to input of SSI receive shift register internally. The data received should be the same as the data transmitted. And do not	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td></td><td></td><td colspan="2">output any valid signals on the pins.
0: normal SSI mode; 1: LOOP mode.</td><td></td></tr>
<tr><td>9</td><td>RFINE</td><td>Receive finish control enable.
0: disable; 1: enable.
For SSICR1.FMAT = B’10 (National Microwire format 1 is selected), SSICR0.RFINE must be 0.</td><td rowspan="2">The receive finish condition list below:<table><tr><th>RFINE</th><th>RFINC</th><th>Receive Finish Condition</th></tr><tr><td>0</td><td>x</td><td>Same as transmit completion condition (transmit-fifo is empty and SSICR1.UNFIN = 0)</td></tr><tr><td>1</td><td>0</td><td>Receive continue</td></tr><tr><td>1</td><td>1</td><td>Receive finish</td></tr></table></td><td>RW</td></tr>
<tr><td>8</td><td>RFINC*</td><td>Receive finish control bit.
0: receive continue
1: receive finished</td><td>RW</td></tr>
<tr><td>7</td><td>EACLRUN</td><td colspan="2">0: don’t auto clear under flag, software clear under
1: software auto clear under flag when tfifo don’t empty</td><td>RW</td></tr>
<tr><td>6</td><td>FSEL</td><td colspan="2">This bit sets the frame signal to be used for slave select. The unselected frame signal always output invalid level.
0: SSI_CE0 is selected
1: SSI_CE1 is selected</td><td>RW</td></tr>
<tr><td>5</td><td>Reserved</td><td colspan="2">Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>4</td><td>VRCNT</td><td colspan="2">Receive counter (RCNT) valid flag.
0: SSIRCNT.RCNT will be ignored.
1: SSIRCNT.RCNT will be used.</td><td>RW</td></tr>
<tr><td>3</td><td>TFMODE</td><td colspan="2">0: new fifo empty mode
1: old fifo empty mode</td><td>RW</td></tr>
<tr><td>2</td><td>TFLUSH</td><td colspan="2">Flush the transmit FIFO when set to 1.
Always return 0 when read.</td><td>RW</td></tr>
<tr><td>1</td><td>RFLUSH</td><td colspan="2">Flush the receive FIFO when set to 1.
Always return 0 when read.</td><td>RW</td></tr>
<tr><td>0</td><td>DISREV</td><td colspan="2">Receive function enable.
0: enable.
1: disable.</td><td>RW</td></tr>
</table>

NOTE:

***:** When transmitting finished or for receive-only operation, transmit function can be disabled and this bit is used to control receiving completion, and the SSI will consume less power.

When the finish condition is set, the receiving will complete after present character is completely shifted in, then the SSI will stop the SSI_CLK and negate the SSI_CE0 / SSI_CE1 if necessary. To make sure present transfer is completed, user must read and get SSISR.END = 1 (or SSISR.BUSY = 0).

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

30.7.4 SSI Control Register1 (SSICR1)

	SSICR1																												Base + 0x0008	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRMHL		TFVCK		TCKFI		Reserved	ITFRM	UNFIN	Reserved	FMAT		TTRG				MCOM				RTRG				FLEN					Reserved	PHA	POL
RST	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	0	0	0	0	1	1	0	0	0	0

Bits	Name	Description	RW
31:30	FRMHL	Frame valid level select, FRMHL [1: 0] correspond to SSI_CE1 and SSI_CE0 respectively.	RW

FRMHL[1:0]	Description	
00	SSI_CE0 is low level valid and SSI_CE1 is low level valid	Initial value
01	SSI_CE0 is high level valid and SSI_CE1 is low level valid	
10	SSI_CE0 is low level valid and SSI_CE1 is high level valid	
11	SSI_CE0 is high level valid and SSI_CE1 is high level valid	

Bits	Name	Description	RW
29:28	TFVCK	Time from frame valid to clock start. When TFVCK = B'00, the time is fixed half or one SSI_CLK cycle according to SSICR1.POL and SSICR1.PHA configuration. For SSICR1.FMAT = B'01, SSICR1.TFVCK is ignored.	RW

TFVCK[1:0]	Description	
00	half or one SSI_CLK cycle delay time	Initial value
01	1 more SSI_CLK cycle delay is added	
10	2 more SSI_CLK cycle delay is added	
11	3 more SSI_CLK cycle delay is added	

Bits	Name	Description	RW
27:26	TCKFI	Time from clock stop to frame invalid. When TCKFI = B'00, the time is fixed one SSI_CLK or half SSI_CLK cycle according to SSICR1.POL and SSICR1.PHA configuration. For SSICR1.FMAT = B'01, SSICR1.TFVCK is ignored.	RW

TCKFI[1:0]	Description	
00	half or one SSI_CLK cycle delay	Initial value
01	1 more SSI_CLK cycle delay is added	
10	2 more SSI_CLK cycle delay is added	
11	3 more SSI_CLK cycle delay is added	

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

<table>
<tr><td>25</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>24</td><td>ITFRM</td><td>Frame during interval, selects if the Frame (SSI_CE0 /SSI_CE1) signal is negated or not during interval time at Interval Mode (SSICR1.FMAT = B’00 and SSIITR.IVLTM ≠ H’0000). It’s ignored at Normal Mode.
0: SSI_CE0 /SSI_CE1 de-asserts during interval time at Interval Mode
1: SSI_CE0 /SSI_CE1 keeps asserted during interval time at Interval Mode</td><td>RW</td></tr>
<tr><td>23</td><td>UNFIN</td><td>This bit controls whether the SSI finishes transmission or wait for data filling (underrun happen) after all data in transmit-FIFO are sent out during transfer. This bit must be cleared to 0 when SSICR1.FMAT = B’01. (TI’s SSP format)
0: TxFIFO empty means end of transmission
1: Transmission didn’t finish when transmit-FIFO is empty, SSI underrun error would occur and SSI waits for data filling; SSI_CLK and SSI_CE0 /SSI_CE1 keeps asserted, SSI_CLK stop at the current level
NOTE: For TxFIFO empty before any transfer after SSI enabled, if SSICR1.UNFIN = 1 or SSICR0.RFINE = 0, SSI will wait till TxFIFO isn’t empty then start to transfer and no underrun error will occur; if SSICR1.UNFIN = 0 and SSICR0.RFINE = 1, after transmit-FIFO become empty, SSI will start a receive-only transfer.</td><td>RW</td></tr>
<tr><td>22</td><td>Reserved</td><td>Writing has no effect, read as zero.</td><td>R</td></tr>
<tr><td>21:20</td><td>FMAT</td><td>These bits set the operating transfer format.
<table>
<tr><th>FMAT</th><th>Description</th><th></th></tr>
<tr><td>00</td><td>Motorola’s SPI format</td><td>Initial value</td></tr>
<tr><td>01</td><td>TI’s SSP format</td><td></td></tr>
<tr><td>10</td><td>National Microwire 1 format</td><td></td></tr>
<tr><td>11</td><td>National Microwire 2 format</td><td></td></tr>
</table></td><td>RW</td></tr>
<tr><td>19:16</td><td>TTRG</td><td>These bits define the transmit-FIFO half-empty threshold value, which when equal or less characters left in transmit-FIFO, the SSISR.TFHE will be set to ‘1’.
0000: less than or equal to 1
n: less than or equal to nx8</td><td>RW</td></tr>
<tr><td>15:12</td><td>MCOM</td><td>Defines the length of command.
Only used when SSICR1.FMAT = b’10 or b’11 (National Microwire format 1 or 2 is selected).
The command length is (MCOM + 1).
Initial value is b’0111.</td><td>RW</td></tr>
<tr><td>11:8</td><td>RTRG</td><td>These bits define the receive-FIFO half-full threshold value, which when equal or more characters received in receive-FIFO, the SSISR.RFHF will be set to ‘1’.
0000: more than or equal to 1</td><td>RW</td></tr>
</table>

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		n: more than or equal to nx8	
7:3	FLEN	These bits set the bit length of every character to be transmitted/received. The maximum data length can be configured is 32 bits. For data length longer than 17 bits (multiples of the SSICR1.FLEN configured length), the software should ensure properly processing. When SSI_GPC pin is used, the FLEN shouldn't be configured as B'01111 (17-bit data). When TI SSP mode is selected (FMAT = 2'b01), 2-bit data length (FLEN = 0) isn't supported. The bit length of one data = FLEN + 2	RW
2	Reserved	Writing has no effect, read as zero.	R
1	PHA	This bit sets the phase of the SSI_CLK from the beginning of a data frame for Motorola's SPI format (SSICR1.FMAT = B'00). 0: The leading edge of SSI_CLK is used to sample data from SSI_DR after the SSI_CE0 /SSI_CE1 goes valid, it is initial value 1: The leading edge of SSI_CLK is used to drive data onto SSI_DT after the SSI_CE0 /SSI_CE1 goes valid	RW
0	POL	SSI_CLK polarity for Motorola's SPI format during idle state. (SSICR1.FMAT = B'00). 0: SSI_CLK keeps low level when idle 1: SSI_CLK keeps high level when idle	RW

30.7.5 SSI Status Register (SSISR)

	SSISR																Base + 0x000C											
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								TFIFO-NUM								RFIFO-NUM								END	BUSY	TFF	RFE	TFHE	RFHF	UNDR	OVER
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Writing has no effect, read as zero.	R
23:16	TFIFO-NUM	These bits indicate the Characters Number in Transmit-FIFO.	R
15:8	RFIFO-NUM	These bits indicate the Characters Number in Transmit-FIFO.	R
7	END	This bit indicates transfer end status. It is the inverse of SSISR.BUSY when transfer is in process, but it'll keep cleared at interval time before transfer is completed. It'll be set when transfer finished.	R
6	BUSY	This bit indicates SSI's working status. 0: SSI is idle or at interval time 1: Transmission and/or reception is in process	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

5	TFF	This bit denotes transmit-FIFO is full or not. 0: Transmit-FIFO is not full 1: Transmit-FIFO is full	R
4	RFE	This bit denotes receive-FIFO is empty or not. 0: Receive-FIFO is not empty 1: Receive-FIFO is empty	R
3	TFHE	This bit denotes whether the characters number in transmit-FIFO being less or equal to SSICR1.TTRG. 0: The data in transmit-FIFO is more than the condition set by SSICR1.TTRG 1: The data in transmit-FIFO meets the condition set by SSICR1.TTRG, If SSICR0.TIE = 1, it will generate SSI TXI interrupt	R
2	RFHF	This bit denotes whether the characters number in receive-FIFO being more or equal to the number set by SSICR1.RTRG. 0: The data in receive-FIFO is less than the condition set by SSICR1.RTRG 1: The data in receive-FIFO meets the condition set by SSICR1.RTRG, If SSICR0.RIE = 1, it will generate SSI RXI interrupt	R
1	UNDR	Transmit-FIFO underrun status. When underrun happens, SSI set this bit and keeps the current status of SSI_CLK and SSI_CE0/SSI_CE1, waiting for transmit-FIFO filling. 0: Underrun has not occurred 1: Underrun has occurred, when SSICR0.TEIE is set, it will generate SSI TEI interrupt. Write '0' to clear this bit, writing '1' has no effect	RW
0	OVER	Receive-FIFO overrun status, new received data will lose. 0: Overrun has not occurred 1: Overrun has occurred; When SSICR0.REIE is set, it will generate SSI REI interrupt. Write '0' to clear this bit, writing '1' has no effect	RW

30.7.6 SSI Interval Time Control Register (SSIITR)

	SSIITR																Base + 0x0010															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	CNTCLK	IVLTM														
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	CNTCLK	Counting clock source select.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0: Use SSI bit clock (SSI_CLK) as the interval counter clock source 1: Use 32K clock as the interval counter clock source	
14:0	IVLTM	Interval time set, set the cycle number of counting clock source for desired interval time. When SSIITR.IVLTM = 0x0000, normal mode is selected, and SSIITR.CNTCLK and SSIICR are ignored. When SSIITR.IVLTM ≠ 0x0000, interval mode is selected. The interval time is calculated as follows: *Interval time ≈ [CNTCLK clock period] * [Value of IVLTM]* The actual interval time is as follow: When SSIITR.CNTCLK = 0: *Interval time = [CNTCLK clock period] * [Value of IVLTM] + 3 * device_clock period* When SSIITR.CNTCLK = 1: *Interval time ≥ [CNTCLK clock period] * [Value of IVLTM + 1] + 1 * device_clock period;* *Interval time ≤ [CNTCLK clock period] * [Value of IVLTM + 2] + 2 * device_clock period*	RW

30.7.7 SSI Interval Character-per-frame Control Register (SSIICR)

	SSIICR																						Base + 0x0014							
Bit																							7	6	5	4	3	2	1	0
																							Reserved					ICC		
RST																							0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:3	Reserved	Writing has no effect, read as zero.	R
2:0	ICC	Sets the fixed number of characters to be transmitted / received each time during SSI_CLK changing (and SSI_CE0 / SSI_CE1 asserting) in interval mode for SSICR1.FMAT = B'00 (Motorola's SPI format is selected). SSIICR is ignored for SSICR1.FMAT ≠ B'00. The desired transfer number of characters-per-frame is (SSIICR set value + 1).	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

30.7.8 SSI Clock Generator Register (SSIGR)

	SSIGR																Base + 0x0018															
Bit																	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																Reserved								CGV							
RST																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7:0	CGV	Sets the frequency of serial bit clock (SSI_CLK). The serial bit clock (SSI_CLK) is generated by dividing device-clock as follows: F_{SSI_CLK} = [Frequency of device clock] / (2 * (CGV + 1)) Device clock is generated in CPM module. The value in SSIGR can be set from 0 to 255, and initialized to 0x0000 on power-on reset.	RW

30.7.9 SSI Receive Counter Register (SSIRCNT)

	SSIRCNT																Base + 0x001C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																RCNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	RCNT	Number of data to be received. If SSICR1.UNFIN = 0 and SSICR0.RFINE = 1, after transmit-FIFO become empty, SSI will start a receive-only transfer. If SSICR0.VRCNT = 1, a special internal counter will be increased automatically. When the value of the internal counter equals to the RCNT, the receiving operation will be stopped automatically.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

30.8 Software Guideline

30.8.1 Common flow

The initial steps are:

1) set GPIO
2) disable interrupt (or not) by setting SSICR0
3) clear SSISR (write 0x0, clear interrupt, FIFO state and working condition)
4) flush FIFO (write SSICR0.xFLUSH once for each FIFO)
5) select the counting clock by configuring SSIITR
6) configure SSIGR (set the frequency of serial bit clock)
7) configure SSICR1 (set valid level of CE signals, set head and end delay of the transfer, set state of CE signals in interval time, select protocols, set threshold of FIFO, set bit length, etc.)
8) configure SSIICR (set the fixed number of characters to be transmit/received each time during SSI_CLK changing in interval mode)
9) configure SSIRCNT (number of data to be received)
10) configure SSICR0 (the start trigger is in this register)

NOTE: the frequency of dev_clk should not be 4 times or more higher than PCLK

30.8.2 Interrupt Operation

In SSI, there are TXI, RXI, TEI and REI total 4 interrupts, all these interrupts are combined together to make one SSI interrupt, which can be masked by writing '1' into corresponding mask bit in INTC interrupt mask register (IMR).

Table 30-3 SSI Interrupts

Operation	Condition	Flag Bit	Mask Bit	Interrupt	DMAC Activation
Transmit	T-FIFO is half-empty or less	SSISR.TFHE	SSICR0.TIE	**TXI**	Possible
	Transmit underrun error	SSISR.UNDR	SSICR0.TEIE	**TEI**	Impossible
Receive	R-FIFO is half-full or more	SSISR.RFHF	SSICR0.RIE	**RXI**	Possible
	Receive overrun error	SSISR.OVER	SSICR0.REIE	**REI**	Impossible

Either SSISR.TFHE or SSISR.RFHF can activate DMA transferring when corresponding individual interrupt mask bit in SSICR0 is cleared (masked) and DMA is enabled and configured.

30.9 Index

Name	Description
APB	Advanced Microcontroller Bus Architecture
Dual SPI	See SPI

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

CPU	Central Processing Unit
Endian	The convention used to interpret the bytes making up a data word when those bytes are stored in computer memory. See Endianness at Wikipedia
FIFO	First In, First Out, a method for organizing and manipulating a data buffer
LSB	See Endian
MSB	See Endian
Quad SPI	See SPI
SPI	Serial Peripheral Interface
Standard SPI	See SPI

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

31 UART Interface

31.1 Overview

This chapter describes the universal asynchronous receiver/transmitter (UART) serial ports. There are ten UARTs: All UARTs use the same programming model. Each of the serial ports can operate in interrupt based mode or DMA-based mode.

The Universal asynchronous receiver/transmitter (UART) is compatible with the 16550-industry standard and can be used as slow infrared asynchronous interface that conforms to the Infrared Data Association (IrDA) serial infrared specification 1.1.

31.1.1 Features

- Full-duplex operation
- 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
- 64x8 bit transmit FIFO and 64x11bit receive FIFO
- Independently controlled transmit, receive (data ready or timeout), line status interrupts
- Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
- Separate DMA requests for transmit and receive data services in FIFO mode
- Supports modem flow control by software or hardware
- Slow infrared asynchronous interface that conforms to IrDA specification

31.1.2 Pin Description

Table 31-1 UART Pins Description

Name	Type	Description
RxD	Input	Receive data input
TxD	Output	Transmit data output
CTS_	Input	Clear to Send — Modem Transmission enabled
RTS_	Output	Request to Send — UART Transmission request

NOTE: UART4, UART3, UART1, UART0 support RxD, TxD, RTS_, CTS_.
UART9, UART8, UART7, UART6, UART5, UART2 support RxD, TxD.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

31.2 Register Descriptions

All UART register 32-bit access address is physical address. When ULCR.DLAB is 0, URBR, UTHR and UIER can be accessed; When ULCR.DLAB is 1, UDLLR and UDLHR can be accessed.

31.2.1 Register Mapping

There are 10 UART controllers in chip, name UART0, UART1, UART2, UART3, UART4, UART5, UART6, UART7, UART8, UART9 respectively.
The base address of UART0 is 0x10030000.
The base address of UART1 is 0x10031000.
The base address of UART2 is 0x10032000.
The base address of UART3 is 0x10033000.
The base address of UART4 is 0x10034000.
The base address of UART5 is 0x10035000.
The base address of UART6 is 0x10036000.
The base address of UART7 is 0x10037000.
The base address of UART8 is 0x10038000.
The base address of UART9 is 0x10039000.

Table 31-2 UART Registers Description

Name	Description	RW	Reset Value	Offset Address	Access Size
URBR	UART Receive Buffer Register	R	0x??	0x000	8
UTHR	UART Transmit Hold Register	W	0x??	0x000	8
UDLLR	UART Divisor Latch Low Register	RW	0x00	0x000	8
UDLHR	UART Divisor Latch High Register	RW	0x00	0x004	8
UIER	UART Interrupt Enable Register	RW	0x00	0x004	8
UIIR	UART Interrupt Identification Register	R	0x01	0x008	8
UFCR	UART FIFO Control Register	W	0x00	0x008	8
ULCR	UART Line Control Register	RW	0x00	0x00c	8
UMCR	UART Modem Control Register	RW	0x00	0x010	8
ULSR	UART Line Status Register	R	0x00	0x014	8
UMSR	UART Modem Status Register	R	0x00	0x018	8
USPR	UART Scratchpad Register	RW	0x00	0x01c	8
ISR	Infrared Selection Register	RW	0x00	0x020	8
UMR	UART M Register	RW	0x00	0x024	8
UACR	UART Add Cycle Register	RW	0x00	0x028	16
URCR	UART RXFIFO Counter Register	R	0x00	0x040	8
UTCR	UART TXFIFO Counter Register	R	0x00	0x044	8
URTDCR	UART Separate RX/TX DMA Register	RW	0x00	0x050	8

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

31.2.2 UART Receive Buffer Register (URBR)

The read-only URBR is corresponded to one level 11bit buffer in non-FIFO mode and a 32x11bit FIFO that holds the character(s) received by the UART. Bits in URBR are right justified when being configured to use fewer than eight bits, and the rest of most significant data bits are zeroed and the most significant three bits of each buffer are the status for the character in the buffer. If ULSR.DRY is 0, don't read URBR, otherwise wrong operation may occur.

	URBR																0x000 (DLAB = 0)							
Bit																	7	6	5	4	3	2	1	0
																	URBR							
RST																	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
7:0	URBR	8-bit UART receive read data.	R

31.2.3 UART Transmit Hold Register (UTHR)

The write-only UTHR is corresponded to one leve 8 bit buffer in non-FIFO mode and a 32x8bit FIFO in FIFO mode that holds the data byte(s) to be transmitted next.

	UTHR																0x000 (DLAB = 0)							
Bit																	7	6	5	4	3	2	1	0
																	UTHR							
RST																	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
7:0	UTHR	8-bit UART transmit write hold data.	W

31.2.4 UART Divisor Latch Low/High Register (UDLLR / UDLHR)

UART Divisor Latch registers, UDLLR/UDLHR together compose the divisor for the programmable baud rate generator that can take the UART device clock and divide it by 1 to (2^{16} – 1).

The UART device source clock is EXCLK or EXCLK/2 that is determined by CPCCR.ECS. UDLHR/UDLLR stores the high/low 8-bit of the divisor respectively. Load these divisor latches during initialization to ensure that the baud rate generator operates properly. If both Divisor Latch registers are 0, the 16X clock stops.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

If you don't set UMR and UACR, UART will work at normal mode with the specified frequency. The relationship between baud rate and the value of Divisor is shown by the formula when UMR and UACR are not set:

Baud Rate = (UART device clock) / (16 * **Divisor**)

	UDLLR																						0x000 (DLAB = 1)							
Bit																							7	6	5	4	3	2	1	0
																							Divisor Latch Low 8-bit							
RST																							0	0	0	0	0	0	0	0

	UDLHR																						0x004 (DLAB = 1)							
Bit																							7	6	5	4	3	2	1	0
																							Divisor Latch High 8-bit							
RST																							0	0	0	0	0	0	0	0

31.2.5 UART Interrupt Enable Register (UIER)

The UART Interrupt Enable Register (UIER) contains the interrupt enable bits for the five types of interrupts (receive data ready, timeout, line status, and transmit data request, and modem status) that set a value in UIIR.

	UIER																						0x004 (DLAB = 0)							
Bit																							7	6	5	4	3	2	1	0
																							Reserved			RTOIE	MSIE	RLSIE	TDRIE	RDRIE
RST																							0	0	0	0	0	0	0	0

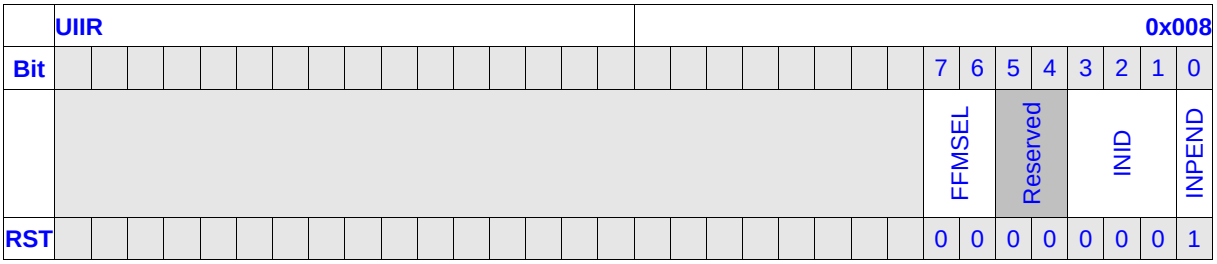
Bits	Name	Description	RW
7:5	Reserved	Writing has no effect, read as zero.	R
4	RTOIE	**Receive Timeout Interrupt Enable.** 0: Disable the receive timeout interrupt 1: Enable the receive timeout interrupt Timeout means the URDR (FIFO mode) is not empty but no character has	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		received for a period of time T: T (bits) = 4 X Word length + 12.	
3	MSIE	**Modem Status Interrupt Enable.** 0: Disable the modem status interrupt 1: Enable the modem status interrupt	RW
2	RLSIE	**Receive Line Status Interrupt Enable.** 0: Disable receive line status interrupt 1: Enable receive line status interrupt	RW
1	TDRIE	**Transmit Data Request Interrupt Enable.** 0: Disable the transmit data request interrupt 1: Enable the transmit data request interrupt	RW
0	RDRIE	**Receive Data Ready Interrupt Enable.** 0: Disable the receive data ready interrupt 1: Enable the receive data ready interrupt	RW

31.2.6 UART Interrupt Identification Register (UIIR)

The read-only UART Interrupt Identification Register (UIIR) records the prioritized pending interrupt source information. Its initial value after power-on reset is 0x01.



Bits	Name	Description	RW
7:6	FFMSEL	**FIFO Mode Select.** 0b00: Non-FIFO mode 0b01: Reserved 0b10: Reserved 0b11: FIFO mode	R
5:4	Reserved	Writing has no effect, read as zero.	R
3:1	INID	**Interrupt Identifier.** These bits identify the current highest priority pending interrupt.	R

INID	Description
0b000	Modem Status
0b001	Transmit Data Request
0b010	Receive Data Ready
0b011	Receive Line Status
0b100	Reserved
0b101	Reserved

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		0b110 Receive Time Out 0b111 Reserved See Table 31-3 for details.	
0	INPEND	**Interrupt Pending.** 0: interrupt is pending 1: No interrupt pending	R

Table 31-3 UART Interrupt Identification Register Description

UIIR.INID	Interrupt Set/Clear Cause			
	Priority	Type	Source	Clear Condition
0b0001	—	None	No pending interrupt	—
0b0110	1st Highest	Receive Line Status	Overrun, Parity, Frame Error, Break Interrupt, and FIFO Error (DMA mode only)	Reading ULSR or empty all the error characters in DMA mode
0b0100	2nd Highest	Receive Data Ready	FIFO mode: Trigger threshold was reached Non-FIFO mode: URBR full	FIFO mode: Reading URBR till below trigger threshold. Non-FIFO mode: Empty URBR
0b1100	2nd Highest	Receive Timeout	FIFO mode only: URBR not empty but no data read in for a period of time	Reset receive buffer by setting UFCR.RFRT to 1 or Reading URBR
0b0010	3rd Highest	Transmit Data Request	FIFO mode: Empty location in UTHR equal to half or more than half Non-FIFO mode: UTHR empty	FIFO mode: Data number in UTHR more than half Non-FIFO mode: Writing UTHR
0b0000	4th Highest	Modem Status	Modem CTS_ pin status change	Reading UMSR

31.2.7 UART FIFO Control Register (UFCR)

The write-only register UFCR contains the control bits for receive and transmit FIFO.

	UFCR																												0x008	
Bit																									7	6	5	4	3	2	1	0
																									RDTR		Reserved	UME	DME	TFRT	RFRT	FME
RST																									0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
7:6	RDTR	**Receive Buffer Data Number Trigger.** These bits are used to select the trigger level for the receive data ready interrupt in FIFO mode. 0b00: 1 0b01: 8 0b10: 16 0b11: 32	W
5	Reserved	Writing has no effect, read as zero.	R
4	UME	**UART Module Enable.** 0: Disable UART 1: Enable UART	W
3	DME	**DMA Mode Enable.** 0: Disable DMA mode 1: Enable DMA mode	W
2	TFRT	**Transmit Holding Register Reset.** 0: Not reset 1: Reset transmit FIFO	W
1	RFRT	**Receive Buffer Reset.** 0: Not reset 1: Reset receive FIFO	W
0	FME	**FIFO Mode Enable.** Set this bit before the trigger levels. 0: non-FIFO mode 1: FIFO mode	W

31.2.8 UART Line Control Register (ULCR)

The ULCR defines the format for UART data transmission.

	ULCR																								0x00C	
Bit																									7	6	5	4	3	2	1	0
																									DLAB	SBK	STPAR	PARM	PARE	SBLS	WLS	
RST																									0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7	DLAB	**Divisor Latch Access Bit.** 0: Enable to access URBR, UTHR or UIER 1: Enable to access UDLLR or UDLHR	W
6	SBK	**Set Break.**	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Causes a break condition (at least one 0x00 data) to be transmitted to the receiving UART. Acts only on the TXD pin and has no effect on the transmit logic. 0: No effect on TXD output 1: Forces TXD output to 0	
5	STPAR	**Sticky Parity.** Setting this bit forces parity location to be opposite of PARM bit when PARE is 1 (it is ignored when PARE is 0). 0: Disable Sticky parity 1: Enable Sticky parity (opposite o f PARM bit)	W
4	PARM	**Parity Odd/Even Mode Select.** If PARE = 0, PARM is ignored. 0: Odd parity 1: Even parity	W
3	PARE	**Parity Enable.** Enables a parity bit to be generated on transmission or checked on reception. 0: No parity 1: Parity	W
2	SBLS	**Stop Bit Length Select.** Specifies the number of stop bits transmitted and received in each character. When receiving, the receiver checks only the first stop bit. 0: 1 stop bit 1: 2 stop bits, except for 5-bit character then 1-1/2 bits	W
1:0	WLS	**Word Length Select.** 0b00: 5-bit character 0b01: 6-bit character 0b10: 7-bit character 0b11: 8-bit character	W

31.2.9 UART Line Status Register (ULSR)

The read-only ULSR indicates status information during the data transfer. Receive error information in ULSR[4:1] remains set until software reads ULSR and it must be read before the error character is read.

	ULSR																								0x014							
Bit																									7	6	5	4	3	2	1	0
																									FIFOE	TEMP	TDRQ	BI	FMER	PARER	OVER	DRY
RST																									0	1	1	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
7	FIFOE	**FIFO Error Status. (FIFO mode only)** FIFOE is set when there is at least one kind of receive error (parity, frame, overrun, break) for any of the characters in receive buffer. FIFOE is reset when all error characters are read out of the buffer. During DMA transfer, the error interrupt generates when FIFOE is 1, and no receive DMA request generates even when data in receive buffer reaches the trigger threshold until all the error characters are read out. In non-DMA mode, FIFOE set does not generate error interrupt. 0: No error data in receive buffer or non-FIFO mode 1: One or more error character in receive buffer	R
6	TEMP	**Transmit Holding Register Empty.** Set when both UTHR and shift register are empty. It is cleared when either the UTHR or the shift register contains a data character. 0: There is data in the transmit shifter and UTHR 1: All the data in the transmit shifter and UTHR has been shifted out	R
5	TDRQ	**Transmit Data Request.** Set when UTHR has half or more empty location (FIFO mode) or empty (non-FIFO mode). When both UIER.TDRIE and TDRQ are 1, transmit data request interrupt generates or during DMA transfer, DMA request to the DMA controller generates when UIER.TDRIE is 0 and TDRQ is 1. 0: There is one (non-FIFO mode) or more than half data (FIFO mode) in UTHR 1: None data (non-FIFO mode) or half or less than half data (FIFO mode) in UTHR	R
4	BI	**Break Interrupt.** BI is set when the received data input is held low for longer than a full-word transmission time (the total time of start bit + data bits + parity bit + stop bits). BI is cleared when the processor reads the ULSR. In FIFO mode, only one character equal to 0x00 is loaded into the FIFO regardless of the length of the break condition. BI shows the break condition for the character at the front of the FIFO, not the most recently received character. 0: No break signal has been received 1: Break signal received	R
3	FMER	**Framing Error.** Set when the bit following the last data bit or parity bit is detected to be 0. If the ULCR had been set for two or one and half stop bits, the other stop	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		bits are not checked except the first one. In FIFO mode, FMER shows a framing error for the character at the front of the receive buffer, not for the most recently received character. Cleared when the processor reads the ULSR. 0: No framing error 1: Invalid stop bit has been detected	
2	PARER	**Parity Error.** Indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. PARER is set upon detection if a parity error and is cleared when the processor reads the ULSR. In FIFO mode, PARER shows a parity error for the character at the front of the FIFO, not the most recently received character. 0: No parity error 1: Parity error has occurred	R
1	OVER	**Overrun Error.** Set when both receive buffer and shifter are full and new data is received which will be lost. Cleared when the processor reads the ULSR. 0: No data has been lost 1: Receive data has been lost	R
0	DRY	**Data Ready.** Set when a complete incoming character has been received into the Receive Buffer registers. DRY is cleared when the receive buffer is read (non-FIFO mode) or when the buffer is empty or when the buffer is reset by setting UFCR.RFRT to 1. 0: No data has been received 1: Data is available in URBR	R

31.2.10 UART Modem Control Register (UMCR)

The UMCR uses the modem control pins RTS_ and CTS_ to control the interface with a modem or data set. UMCR also controls the loopback mode. Loopback mode must be enabled before the UART is enabled.

UMCR																									0x010							
Bit																									7	6	5	4	3	2	1	0
																									MDCE	FCM	Reserved	LOOP	Reserved		RTS	Reserved
RST																									0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7	MDCE	**Modem Control Enable.** 0: Modem function is disabled	W

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1: Modem function is enabled	
6	FCM	**Flow Control Mode.** 0: Flow control by software 1: Flow control by hardware	
5	Reserved	Writing has no effect, read as zero.	R
4	LOOP	**Loop Back.** This bit is used for diagnostic testing of the UART. When LOOP is 1, TXD output pin is set to a logic 1 state, RXD is disconnected from the pin, and the output of the transmitter shifter register is looped back into the receiver shift register input internally, similar to CTS_ and RTS_ pins and the RTS bit of the UMCR is connected to CTS bit of UMSR respectively. Loopback mode must be selected before the UART is enabled. 0: Normal operation mode 1: Loopback-mode UART operation	W
3:2	Reserved	Writing has no effect, read as zero.	R
1	RTS	**Request To Send.** This bit can control the RTS_ output state. 0: RTS_ force to high 1: RTS_ force to low	W
0	Reserved	Writing has no effect, read as zero.	R

31.2.11 UART Modem Status Register (UMSR)

The read-only UMSR provides the current state of the control lines from the modem to the processor. They are cleared when the processor reads UMSR.

	UMSR																								0x018							
Bit																									7	6	5	4	3	2	1	0
																									Reserved			CTS	Reserved			CCTS
RST																									0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:5	Reserved	Writing has no effect, read as zero.	R
4	CTS	**Status of Clear To Send.** When MDCE bit is 1, this bit is the complement of CTS_ input. If Loop bit of UMCR is 1, this bit is equivalent to RTS bit of UMCR. 0: CTS_ pin is 1 1: CTS_ pin is 0	R
3:1	Reserved	Writing has no effect, read as zero.	R
0	CCTS	**Change status of CTS_.**	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		When MDCE bit is 1, this bit indicates the state change on CTS_ pin. 0: No state change on CTS_ pin since last read of UMSR 1: A change occurs on the state of CTS_ pin	

31.2.12 UART Scratchpad Register

This Scratchpad register is used as a scratch register for the programmer and has no effect on the UART.

	USPR																												0x01C	
Bit																									7	6	5	4	3	2	1	0
																									Scratch Data							
RST																									?	?	?	?	?	?	?	?

31.2.13 Infrared Selection Register (ISR)

The ISR is used to configure the slow-infrared (SIR) interface that is provided in each UART to support two-way wireless communication using infrared transmission that conforms to the IrDA serial infrared specification 1.1. The maximum frequency is up to 115.2kbps.

	ISR																												0x020	
Bit																									7	6	5	4	3	2	1	0
																									Reserved			RDPL	TDPL	XMODE	RCVEIR	XMITIR
RST																									0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:5	Reserved	Writing has no effect, read as zero.	R
4	RDPL	**Receive Data Polarity.** 0: Slow-infrared (SIR) interface decoder takes positive pulses as zeros 1: SIR decoder takes negative pulses as zeros	W
3	TDPL	**Transmit Data Polarity.** 0: SIR encoder generates a positive pulse for a data bit of zero 1: SIR encoder generates a negative pulse for a data bit of zero	W
2	XMODE	**Transmit Pulse Width Mode.** Set when the transmit encoder needs to generate 1.6us pulses (that are 3/16 of a bit-time at 115.2 kbps). Cleared when the transmit encoder needs to generate 3/16 of a bit-time wide according to current baud rate. 0: Transmit pulse width is 3/16 of a bit-time wide 1: Transmit pulse width is 1.6 us	W

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	RCVEIR	**Receiver SIR Enable.** This bit is used to select the signal from the RXD pin is processed by the IrDA decoder before it is fed to the UART (RCVEIR = 1) or bypass IrDA decoder and is fed directly to the UART (RCVEIR = 0). 0: Receiver is in UART mode 1: Receiver is in SIR mode	W
0	XMITIR	**Transmitter SIR Enable.** This bit is used to select TXD output pin is processed by the IrDA encoder before it is fed to the device pin (XMITIR = 1) or bypass IrDA encoder and is fed directly to the device pin (XMITIR = 0). **NOTE:** disable infrared LED before XMITIR is set, otherwise a false start bit may occur. 0: Transmitter is in UART mode 1: Transmitter is in SIR mode	W

31.2.14 UART M Register (UMR)

	UMR																												0x024
Bit																							7	6	5	4	3	2	1	0
																							Reserved			M				
RST																							0	0	0	0	0	0	0	0

M is the value of UMR register.

It will take UART at least M cycles to transmit or receive one bit.

It will take UART at most M+1 cycles to transmit or receive one bit.

31.2.15 UART Add Cycle Register (UACR)

	UACR																												0x028
Bit																					11	10	9	8	7	6	5	4	3	2	1	0
																	Reserved				AC										
RST																					0	0	0	0	0	0	0	0	0	0	0	0

If nth bit of the register is 1, it will take UART M+1 cycles to transmit or receive the bit of date.

If the register is 12'h0, UART will receive or transmit a bit by M cycle(s).

If the register is 12'hfff, UART will receive or transmit a bit by M+1 cycle(s).

For the detail to see For any frequency clock to use the Uart.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

31.2.16 UART RXFIFO Counter Register (URCR)

	URCR																												0x040	
Bit																													7	6	5	4	3	2	1	0
																													Reserved	RCNT						
RST																													0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7	Reserved	Writing has no effect, read as zero.	R
6:0	RCNT	RXFIFO Counter. Indicates there are n data in RXFIFO when this field is n.	R

31.2.17 UART TXFIFO Counter Register (UTCR)

	UTCR																												0x044	
Bit																													7	6	5	4	3	2	1	0
																													Reserved	TCNT						
RST																													0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7	Reserved	Writing has no effect, read as zero.	R
6:0	TCNT	TXFIFO Counter. Indicates there are n data in TXFIFO when this field is n.	R

31.2.18 UART Separate RX/TX DMA Register (URTDCR)

	URTDCR																												0x050	
Bit																													7	6	5	4	3	2	1	0
																													RTD_EN	Reserved					RTD_R	RTD_T
RST																													0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7	RTD_EN	Separate receive and transmit dma control enable.	RW
6:2	Reserved	Writing has no effect, read as zero.	R
1	RTD_R	Enable receive dma.	RW
0	RTD_T	Enable transmit dma.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

31.3 Operation

The following sections describe the UART operations that include flow of configuration, data transmission, data reception, and Infrared mode.

31.3.1 UART Configuration

Before UART starts to transfer data or changing transfer format, configuration must be done to define the transfer format. The sample flow is as the following:

In FIFO mode, set FME bit of UFCR to 1, reset receive and transmit FIFO, then initialize the UART as described below:

1 Clear UFCR.UME to 0.
2 Set value in UDLL/UDHR to generate the baud rate clock.
3 Set data format in ULCR.
4 If it is in FIFO MODE, set FME bit and other FIFO control in UFCR, reset receive and transmit FIFO, otherwise skip item 4.
5 Set each interrupt enable bit in UIER in interrupt-based transfer or set UFCR.DME in DMA-based transfer (DMA transfer is FIFO mode only), then set UFCR.UME.

31.3.2 Data Transmission

After configuration, UART is ready for data transfer. For data transmission, refer to the following procedure:

1 Read ULSR.TDRQ (interrupt disable) or wait for transmit data request interrupt (interrupt enable), if TDRQ = 1 or transmit data request interrupt generates, that means there is enough empty location in UTHR for new data.
2 If ULSR.TDRQ is 1 or get the transmit data request interrupt, write transmit data to UTHR to start transmission.
3 Do item 1 and item 2 if there are more data waiting for transmit.
4 After all necessary data are written to UTHR, wait ULSR.TEMP = 1, that means all data completely transmitted.
5 If it is necessary to send break, set ULCR.SBK and at least wait for 1-bit interval time to send a valid break, then clear ULCR.SBK.
6 Clear UME bit to finish UART transmission.

31.3.3 Data Reception

After configuration, UART is ready for data transfer. For data reception, refer to the following sample procedure:

1 Read ULSR.DRY (interrupt disable) or wait for receive data request interrupt (interrupt enable), if ULSR.DRY =1 or receive data request interrupt generates, that means URBR has

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

one data (non-FIFO mode) or data in URBR reaches the trigger value. (FIFO mode)

2 If ULSR.DRY = 1 or receive data request interrupt generates, then read ULSR.FIFOE or see if there is error interrupt, if FIFOE = 1, it means received data has receive error, then go to error handler, other wise go to item 3.

3 Read one received data in URBR (non-FIFO mode) or data equal to trigger value in URBR. (FIFO mode)

4 Check whether all data received: check whether ULSR.DRY = 0, in FIFO mode and interrupt is enabled, timeout interrupt may generate, when timeout interrupt generates, read URBR till ULSR.DRY = 0.

5 Clear UFCR.UME to end data reception when all data are received and ULSR.DRY = 0.

31.3.4 Receive Error Handling

A sample error handling flow is as the following:

1 If ULSR.FIFOE = 1, it means there is receive error in received data, then check what error it is.

2 If ULSR.OVER = 1, go to OVER error handling.

3 If ULSR.BI = 1, go to Break handling.

4 If ULSR.FMER = 1, go to Frame error handling.

5 If PARER = 1, go to PARER error handling.

31.3.5 Modem Transfer

When UMCR.MDCE = 1, modem control is enabled. Transfer flow can be stopped and restarted by software through RTS_ and CTS_ pin. When UART transmitter detects low level on CTS_ pin, it stops transmission and TxD pin goes to mark state after finishing transmitting the current character until it detects CTS_ pin goes back to high level. RTS_ pin is output to receiving UART and its state can be controlled by setting UMCR.RTS bit, that is, setting UMCR.RTS to 1, RTS_ pin is low level output that means UART is ready to receive data, on the contrary, it means UART currently can't receive more data.

31.3.6 DMA Transfer

UART can operate in DMA-based (UFCR.DME = 1, FIFO mode only), that is, dma request initiated by UART takes the place of interrupt request and transmission/reception is carried out using DMA instead of CPU. Be sure that software guarantee to disable transmit and receive interrupt except timeout and error interrupts.

During DMA transfer, if an interrupt occurs, software must first read the ULSR to see if an error interrupt exists, then check the UIIR for the source of the interrupt and if DMA channel is already halt because of the error indicator from UART, then disable DMA channel and read out all the error data from receive FIFO. Software re-set and re-enable DMA and data transfer by DMA will re-start.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

31.3.7 Slow IrDA Asynchronous Interface

Each UART supports slow infra-red (SIR) transmission and reception by setting ISR.XMITIR and ISR.RCVEIR to 1 (make sure the two bits are not set to 1 at the same time because SIR can't operate full-duplex). According to the IrDA 1.1, data rate is limited at a maximum value of 115.2Kbps.

In SIR transmit mode, the transmit pulse comes out at a rate of 3/16 (when the transmit data bit is zero); in SIR receive mode, the receiver must detect the 3/16 pulsed period to recognize a zero value (an active high or low pulse is demodulation to 0, and no pulse is demodulation to 1).

Compared to normal UART, there are some limitations to SIR, that is, each character is fixed to 8-bit data width, no parity and 1 stop bit and modem function is ignored. The IrDA 1.1 specifies a minimum 10ms latency after an optical node ceases transmitting before its receiver recovers its receiving function and software must guarantee this delay.

In the IrDA 1.1 specification, communication must start up at the rate of 9600bps, but then allows the link to negotiate higher (or lower) data rates if supported by both ends. However, the communication rate will not automatically change. Change, if necessary, is performed by software.

31.3.8 For any frequency clock to use the UART

NOTE: if you don't set M register and UACR the UART work at normal mode with the specified frequencies. To use other frequency you should to set M register and UACR to right value.

1 The Improving

Following changes are made:

a One bit is composed by M CLK_{BR} cycles, which can be 4~1024.

b Some extra CLK_{BR} cycles can be inserted in some bits in one frame, so that like M has fraction.

For instance:

$CLK_{BR} = CLK_{DEV} / N$ N = 1, 2, …

$CLK_{BR} = CLK_{DEV}$ = 4MHz

Band rate = 460800

In accurate

$M_a = 8.681$

We take

M = 8, with 8 extra cycles in every frame

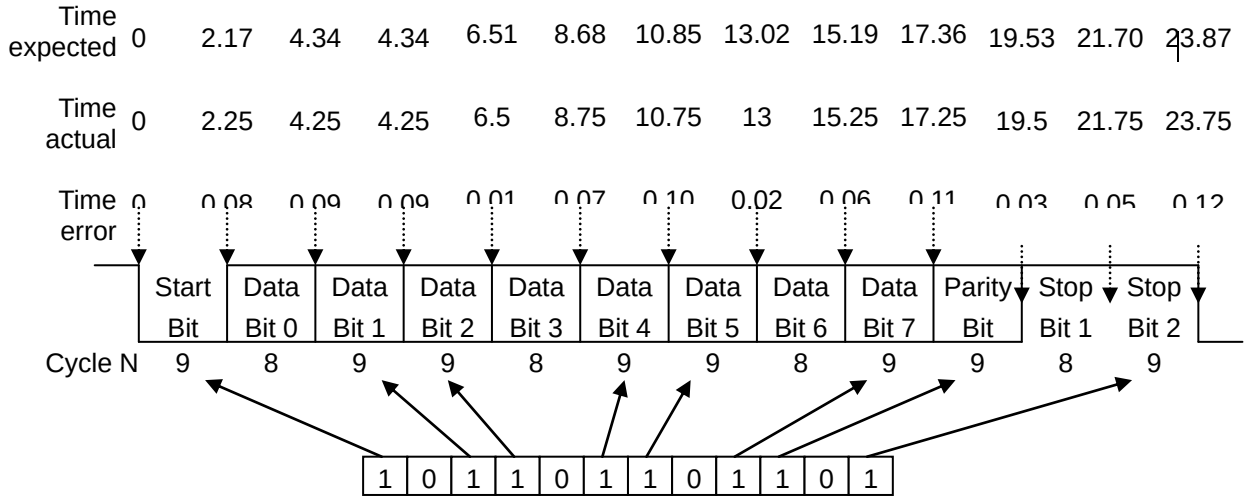
A 12-bit register is used to indicate where to insert the extra cycles.

The first line is the time expected

The second line is the time actual

The third line is the time error

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.



For transmission, in theory, the biggest error is half of CLK_{BR} cycle, which is 0.125us here.

2 To set UMR register

$CLK_{BR} = CLK_{DEV} / N$

$M_a = CLK_{BR}$/band rate

M is modem of M_a.

Write M to Mregister.

Considering the power and the robust quality, for M form 6 to 32 is you better select by set the UDLR.

The max error

$$\frac{0.5/CLK_{BR}}{M_a/CLK_{BR}} = 0.5/M_a < 0.5/M$$

M	4	8	16	32	64
error/W_{bit}	12.5%	6.25%	3.125%	1.56%	0.78%

3 To set UACR value

For each bit of it means:

0: means not to add additional cycle to the bit that UART is prepare to transmit or receive, in another word, you will to use M cycles to transmit or receive the bit

1: means to add additional cycle to the bit that UART is prepare to transmit or receive, in another word, you will to use M+1 cycles to transmit or receive the bit

To set UACR value you must ensure that the max error of each bit should be less than $0.5P_{BR}$.

For example：M_a-M =0.15; M+1-M_a=0.85;

Write 8 to UMR,

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Write 0x408 to UACR

cycle/bit	:	M，	M，	M，	M+1，	M，	M，	M，	M，	M，	M，	M+1，	M
UACR	:	0	0	0	1	0	0	0	0	0	0	1	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32 eMMC/SD Controller（MSC）

32.1 Overview

The embedded Multi Media Card (eMMC) is a universal low cost mass storage and communication media that is designed to cover a wide area of applications such as electronic toys, organizers, PDAs, smart phones, and so on.

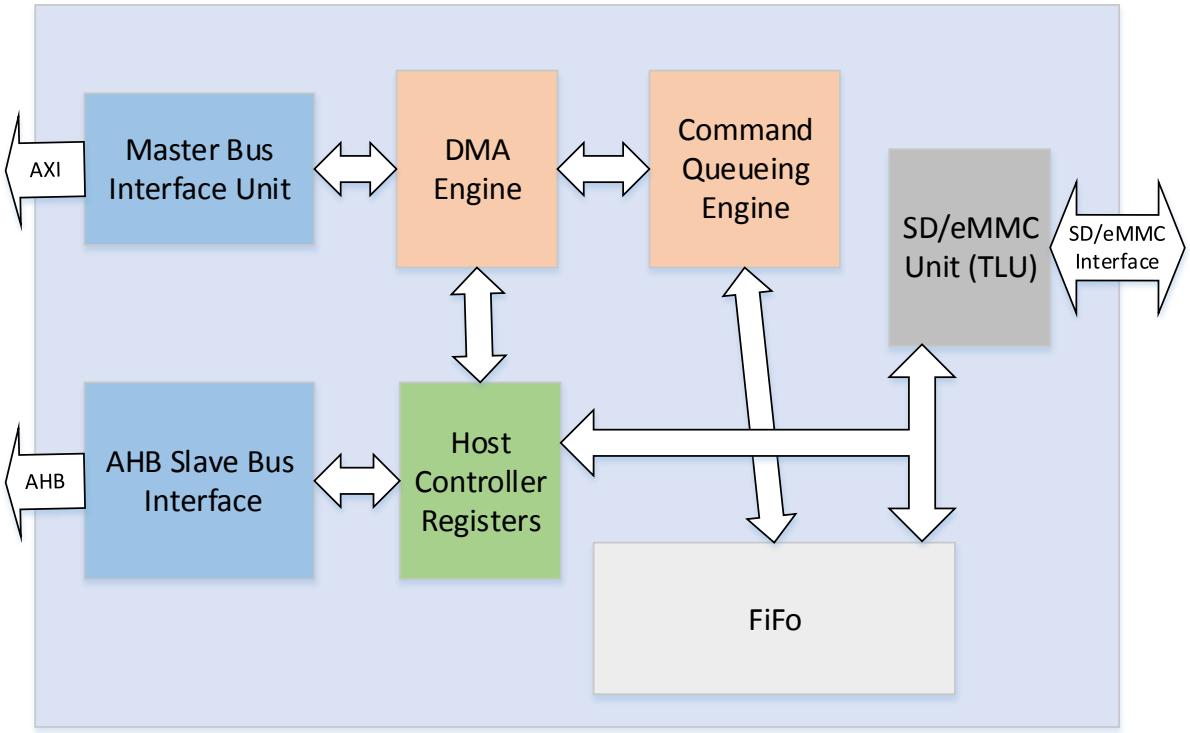
The Secure Digital (SD) card is an evolution of eMMC. It is specifically designed to meet the security, capacity, performance, and environmental requirements inherent in newly emerging audio and video consumer electronic devices. The physical form factor, pin assignment, and data transfer protocol are forward compatible with the Multi Media Card with some additions. An SD card can be categorized as SD memory or SD I/O card, commonly known as SDIO. A memory card invokes a copyright protection mechanism that complies with the security of the SDMI standard and is faster and capable of higher memory capacity. The SDIO card provides high-speed data I/O with low-power consumption for mobile electronic devices.

32.2 Features

- Supports SD memory and SD Input/Output (SDIO) digital interface protocol, and compliant with SD HCI specification
- Supports eMMC Command Queuing Engine (CQE), Compliant with CQ HCI specification
- Supports Host Version 4
- Support eMMC Specification 5.1
- Support SD Specification 4.1
- Support SD I/O Specification 2.0
- Maximum data rate is 100MBps
- Support data width 1/4/8 bit
- Built-in programmable frequency divider for eMMC/SD bus
- Multi-DMA mode including SDMA, ADMA2 and ADMA3
- Multi-SD function support including multiple I/O and combined I/O and memory
- IRQ supported enable card to interrupt eMMC/SD controller
- Single or multi block access to the card including erase operation
- Stream access to the eMMC card
- Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
- Support Command Completion Signal and interrupt to CPU
- Command Completion Signal disable feature
- The maximum block length is 4KB(4096 bytes)

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.3 Block Diagram

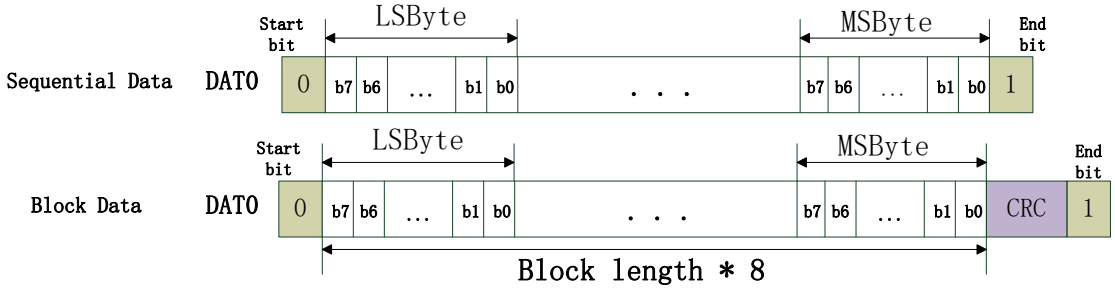


32.4 Data Format Description

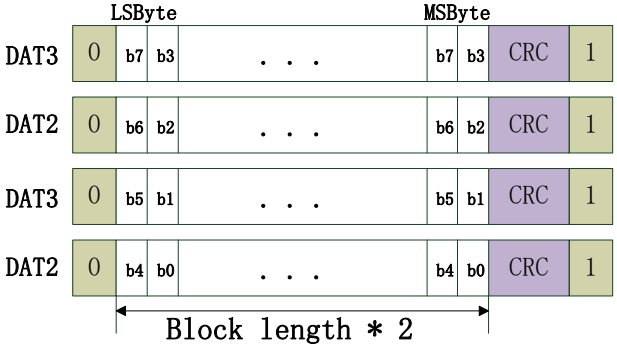
MSC0 supports three kinds of data bits width:1bits, 4bits, 8bits. MSC1 and MSC2 only support 1bits and 4bits.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

1 bit bus(only DAT0 used):



4 bits bus(DAT3 to DAT0 used):



8 bits bus(DAT7 to DAT0 used):

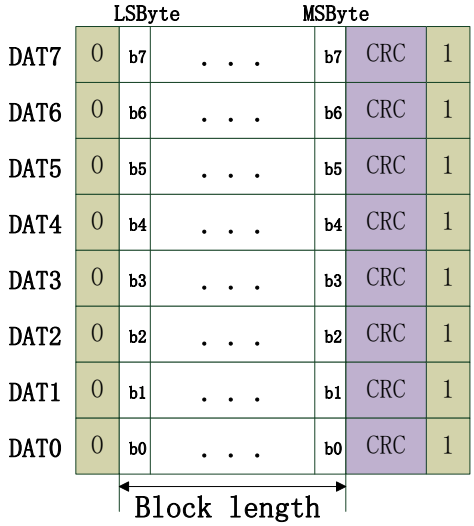


Figure 32-1 msc data format

32.5 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute

   R- Read only

   W- Write only

   RW- Read and Write

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

RCW- Read and Write, but Clear to 0 by Read
RSW- Read and Write, but Set to 1 by Read
RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
RC- Read only, and Clear to 0 by read
RS- Read only, and Set to 1 by read

3. Reset Value
1 - reset to 1
0 - reset to 0
? - value unknown after reset

The MSC implements all the registers defined by the SD Host Controller Specification that defines registers for SD modes. Some of these registers are reused in the eMMC mode. Additionally, MSC implements registers defined in the Host Controller Interface for Command Queuing section of the eMMC Specification.
For accessing an unused address within the memory space of MSC, a read completes successfully with all-zero read data, and a write completes successfully with write data being discarded.

MSC supports different types of card interfaces namely SD and eMMC. To support the SD card interface, MSC implements all registers defined in SD host controller specification. These registers can be used in Legacy SD bus interface mode. Most of the registers used for Legacy SD bus interface mode are reused for the eMMC bus interface mode. In addition to the Command Queuing registers defined by eMMC specification, MSC provides defines additional registers to control eMMC-specific operations. Table 32-1 shows usage of registers for appropriate card interface modes.

Table 32-1 Card Interfaces Supported for Different Register Types

Register Type	Available Registers for a Specific Register Type	Support in Legacy SD Mode?	Supported in eMMC Mode?
SD/eMMC Generation Registers	BLOCKSIZE_R BLOCKCOUNT_R ARGUMENT_R XFER_MODE_R CMD_R	yes	yes
Response Registers	RESP01_R RESP45_R RESP67_R	yes	yes
	RESP23_R	yes	yes
Slave Mode Memory Access Register	BUF_DATA_R	yes	yes
Host Setting and Capabilities Registers	PSTATE_REG HOST_CTRL1_R BGAP_CTRL_R	yes	yes

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	CLK_CTRL_R SW_RST_R NORMAL_INT_STAT_R ERROR_INT_STAT_R NORMAL_INT_STAT_EN_R ERROR_INT_STAT_EN_R NORMAL_INT_SIGNAL_EN_R ERROR_INT_SIGNAL_EN_R HOST_CTRL2_R CAPABILITIES1_R CAPABILITIES2_R CURR_CAPABILITIES1_R CURR_CAPABILITIES2_R		
	TOUT_CTRL_R AUTO_CMD_STAT_R FORCE_AUTO_CMD_STAT_R FORCE_ERROR_INT_STAT_R	yes	yes
DMA registers	SDMASA_R ADMA_ERR_STAT_R ADMA_SA_LOW_R ADMA_SA_HIGH_R ADMA_ID_LOW_R ADMA_ID_HIGH_R	yes	yes
Pointer Registers	P_VENDOR_SPECIFIC_AREA	yes	Yes
	P_VENDOR2_SPECIFIC_ARE	no	yes
Vendor Specific Registers	MSHC_VER_ID_R MSHC_VER_TYPE_R	yes	yes
	EMMC_CTRL_R	no	Yes
Command Queuing Registers	CQVER CQCAP CQCFG CQCTL CQIS CQISE CQISGE CQIC CQTDLBA CQTDLBAU CQTDBR CQTCN CQDQS CQDPT CQTCLR	no	yes

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	CQSSC1 CQSSC2 CQCRDCT CQRMEM CQTERRI CQCRI CQCRA		

32.5.1 Register Memory Map

Table 32-2 Registers Memory Map Base Address

Name	Base	Description
MSC0	0x13450000	Address base of MSC0
MSC1	0x13460000	Address base of MSC1
MSC2	0x13490000	Address base of MSC2

Table 32-3 lists all the MSC registers:

Table 32-3 MSC Registers Map

Name	Reset Value	Offset	Description	Mask
SDMASA_R	0x0000_0000	0x00	configure 32-bit Block Count or SDMA System Address based on the Host...	0xFFFF_FFFF
BLOCKSIZE_R	0x0000	0x04	configure SDMA buffer boundary and number of bytes in a data block	0x7FFF
BLOCKCOUNT_R	0x0000	0x06	configure the number of data blocks	0xFFFF
ARGUMENT_R	0x0000_0000	0x08	configure the SD/eMMC command argument	0xFFFF_FFFF
XFER_MODE_R	0x0000	0x0c	control the operation of data transfers for an SD/eMMC mode	0x01FF
CMD_R	0x0000	0x0e	provide the information related to command and response packet	0x3FFF
RESP01_R	0x0000_0000	0x10	store the response from the cards	0xFFFF_FFFF
RESP23_R	0x0000_0000	0x14	store the response from the cards	0xFFFF_FFFF
RESP45_R	0x0000_0000	0x18	store the response from the cards	0xFFFF_FFFF
RESP67_R	0x0000_0000	0x1c	store the response from the cards	0xFFFF_FFFF
BUF_DATA_R	0x0000_0000	0x20	access the packet buffer	0xFFFF_FFFF
PSTATE_REG	0x0000_0000	0x24	indicates the present status of the Host Controller	0x1BFF_0FFF
HOST_CTRL1_R	0x00	0x28	control the operation of Host Controller	0xFF
BGAP_CTRL_R	0x00	0x2a	control any operation related to Block Gap	0x0F
CLK_CTRL_R	0x0000	0x2c	controls SDCLK (card clock) in an SD/eMMC mode	0xFFEF
TOUT_CTRL_R	0x00	0x2e	At the initialization of the Host Controller, the Host Driver shall set the Data Timeout Counter...	0x0F

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

SW_RST_R	0x00	0x2f	A reset pulse is generated when writing 1 to each bit of this register	0x07
NORMAL_INT_STAT_R	0x0000	0x30	reflects the status of Normal Interrupt	0xFFFF
ERROR_INT_STAT_R	0x0000	0x32	Signals defined in this register can be enabled by the Error Interrupt Status Enable register	0xFFFF
NORMAL_INT_STAT_EN_R	0x0000	0x34	enables the Interrupt Status for Normal Interrupt Status register	0x7FFF
ERROR_INT_STAT_EN_R	0x0000	0x36	sets the Interrupt Status for Error Interrupt Status register	0xFFFF
NORMAL_INT_SIGNAL_EN_R	0x0000	0x38	select the interrupt status that is indicated to the Host System as the...	0x7FFF
ERROR_INT_SIGNAL_EN_R	0x0000	0x3a	select the interrupt status that is notified to the Host System as an...	0xFFFF
AUTO_CMD_STAT_R	0x0000	0x3c	indicate the CMD12 response error of Auto CMD12, and the CMD23 response...	0x00BF
HOST_CTRL2_R	0x0000_0000	0x3e	control how the Host Controller operates	0x007F_007F
CAPABILITIES1_R	0x0000_0000	0x40	provides the Host Driver with information specific to the Host Controller implementation	0x276D_C898
CAPABILITIES2_R	0x0000_0000	0x44	provides the Host Driver with information specific to the Host Controller implementation	0x0800_2077
FORCE_AUTO_CMD_STAT_R	0x0000	0x50	The register is not a physically implemented but is an address at which the Auto CMD Error Status...	0x00BF
FORCE_ERROR_INT_STAT_R	0x0000	0x52	This register is not a physically implemented but is an address at which the Error Interrupt Status...	0xFFFF
ADMA_ERR_STAT_R	0x00	0x54	holds the ADMA state during ADMA error	0x07
ADMA_SA_LOW_R	0x0000_0000	0x58	holds the lower 32-bit system address for DMA transfer	0xFFFF_FFFF
ADMA_SA_HIGH_R	0x0000_0000	0x5c	holds the upper 32-bit system address for DMA transfer	0xFFFF_FFFF
ADMA_ID_LOW_R	0x0000_0000	0x78	holds the lower 32-bit Integrated Descriptor address	0xFFFF_FFFF
ADMA_ID_HIGH_R	0x0000_0000	0x7c	holds the upper 32-bit Integrated Descriptor address	0xFFFF_FFFF
SLOT_INTR_STATUS_R	0x0000	0xfc	This register indicate the Interrupt status of each slot.	0x00FF
CQVER	0x0000_0510	0x180	provides information about the version of the eMMC Command Queueing standard, which...	0x0000_0FFF
CQCAP	0x0000_3018	0x180 + 0x4	indicates the capabilities of the command queuing engine	0x0000_F3FF

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

CQCFG	0x0000_0000	0x180 + 0x8	controls CQE behavior affecting the general operation of command queuing...	0x0000_1101
CQCTL	0x0000_0000	0x180 + 0xc	controls CQE behavior affecting the general operation of command queuing module or...	0x0000_0101
CQIS	0x0000_0000	0x180 + 0x10	indicates pending interrupts that require service	0x0000_0000F
CQISE	0x0000_0000	0x180 + 0x14	enables and disables the reporting of the corresponding interrupt to host software...	0x0000_0000F
CQISGE	0x0000_0000	0x180 + 0x18	enables and disables the generation of interrupts to host software	0x0000_0000F
CQIC		0x180 + 0x1c	controls and configures interrupt coalescing feature	
CQTDLBA		0x180 + 0x20	configuring the lower 32 bits of the byte address of the head of the Task...	
CQTDLBAU		0x180 + 0x24	configuring the upper 32 bits of the byte address of the head of the Task...	
CQTDBR		0x180 + 0x28	Using this register, software triggers CQE to process a new task	
CQTCN		0x180 + 0x2c	used by CQE to notify software about completed tasks	
CQDQS		0x180 + 0x30	stores the most recent value of the device's queue status	
CQDPT		0x180 + 0x34	Maintains the list of tasks that are queued into device and are awaiting execution...	
CQTCLR		0x180 + 0x38	removing an outstanding task in the CQE	
CQSSC1		0x180 + 0x40	removing an outstanding task in the CQE	
CQSSC2		0x180 + 0x44	removing an outstanding task in the CQE	
CQCRDCT		0x180 + 0x48	stores the response of last executed DCMD	
CQRMEM		0x180 + 0x50	controls the generation of response error detect (RED) interrupt	
CQTERRI		0x180 + 0x54	updated by CQE when an error occurs on data or command related to a task activity....	
CQCRI		0x180 + 0x58	stores the index of the last received command response	
CQCRA		0x180 + 0x5c	stores the argument of the last received command response	
MSC_VER_ID_R		0x500	reflects the current release number of MSC	

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

MSC_VER_TYPE_R		0x500 + 0x4	reflects the current release type of MSC	
EMMC_CTRL_R		0x500 + 0x2c	control the eMMC operation	

32.5.2 Register and Fields Description

32.5.2.1 SDMA System Address register (SDMASA_R, 0x00)

	SDMASA_R																															BASE + 0x00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BLK_CNT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	BLK_CNT	32-bit Block Count (SDMA System Address) ■ SDMA System Address (Host Version 4 Enable = 0) - This register contains the system memory address for SDMA transfer in the 32-bit addressing mode. When the Host Controller stops an SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing. Reading this register during data transfers may return invalid value. ■ 32-bit Block Count (Host Version 4 Enable = 1) - From Host Controller Version 4.10, this register is redefined as 32-bit Block Count. The Host Controller decrements the block count of this register for every block transfer and the data transfer stops when the count reaches zero. This register should be accessed when no transaction is executing. Reading this register during data transfers may return invalid value. ■ FFFF_FFFFh - 4G - 1 block ■ ... - ... ■ 0000_0002h - 2 blocks ■ 0000_0001h - 1 block ■ 0000_0000h - Stop Count Note: ■ For Host Version 4 Enable = 0, Host driver shall not program system address in this register while operating in ADMA mode. It should be programmed in ADMA System Address register. ■ For Host Version 4 Enable = 0, Host driver shall program 32-bit block count in this register when Auto CMD23 is enabled for non-DMA and ADMA mode. Volatile: true	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.5.2.2 Block Size register (BLOCKSIZE_R, 0x04)

	BLOCKSIZE_R								BASE + 0x04							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	SDMA_BUF_BDRY			XFER_BLK_SIZE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	Reserved	Writing has no effect, read as zero.	R
14:12	SDMA_BUF_BDRY	SDMA Buffer Boundary These bits specify the size of contiguous buffer in system memory. The SDMA transfer shall wait at every boundary specified by these fields and the Host Controller generates the DMA interrupt to request the Host Driver to update the SDMA System Address register. ■ 000b - 4K bytes ■ 001b - 8K bytes ■ 010b - 16K bytes ■ 011b - 32K bytes ■ 100b - 64K bytes ■ 101b - 128K bytes ■ 110b - 256K bytes ■ 111b - 512K bytes Values: ■ 0x0 (BYTES_4K): 4K Bytes SDMA Buffer Boundary ■ 0x1 (BYTES_8K): 8K Bytes SDMA Buffer Boundary ■ 0x2 (BYTES_16K): 16K Bytes SDMA Buffer Boundary ■ 0x3 (BYTES_32K): 32K Bytes SDMA Buffer Boundary ■ 0x4 (BYTES_64K): 64K Bytes SDMA Buffer Boundary ■ 0x5 (BYTES_128K): 128K Bytes SDMA Buffer Boundary ■ 0x6 (BYTES_256K): 256K Bytes SDMA Buffer Boundary ■ 0x7 (BYTES_512K): 512K Bytes SDMA Buffer Boundary	RW
11:0	XFER_BLK_SIZE	Transfer Block Size This register specifies the block size of data transfers. In case of memory, it shall be set up to 512 bytes. It can be accessed only if no transaction is executing. Read operations during transfers may return an invalid value, and write operations shall be ignored.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 0x0 - No Data Transfer ■ 0x1 - 1 Byte ■ 0x2 - 2 Bytes ■ 0x3 - 3 Bytes ■ ... - ... ■ 0x1FF - 511 Byte ■ 0x200 - 512 Bytes ■ ... - ... ■ 0x800 - 2048 Bytes	

32.5.2.3 16-bit Block Count register (BLOCKCOUNT_R, 0x06)

	BLOCKCOUNT_R															BASE + 0x06
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BLK_CNT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:0	BLK_CNT	16-bit Block Count ■ If Host Version 4 Enable is set 0 or 16-bit Block Count register is set to non-zero, 16-bit Block Count register is selected. ■ If Host Version 4 Enable is set 1 and 16-bit Block Count register is set to zero, 32-bit Block Count register is selected. ■ 0x0 - Stop Count ■ 0x1 - 1 Block ■ 0x2 - 2 Blocks ■ ... - ... ■ 0xFFFF - 65535 Blocks Note: For Host Version 4 Enable = 0, this register should be set to 0000h before programming 32-bit block count register when Auto CMD23 is enabled for non-DMA and ADMA mode. Volatile: true	RW

32.5.2.4 Argument register (ARGUMENT_R, 0x08)

	ARGUMENT_R																													BASE + 0x08
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ARGUMENT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	ARGUMENT	Command Argument The SD/eMMC command argument is specified as bit 39-8 of the command format.	RW

32.5.2.5 Transfer Mode register (XFER_MODE_R, 0x0c)

	XFER_MODE_R								BASE + 0x0c							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							RESP_INT_DIS	RESP_ERR_CHK_EN	RESP_TYPE	MULTI_BLK_SEL	DATA_XFER_DIR	AUTO_CMD_EN		BLK_CNT_EN	DMA_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:9	Reserved	Writing has no effect, read as zero.	R
8	RESP_INT_DIS	Response Interrupt Disable Host Controller supports response check function to avoid overhead of response error check by Host driver. Only R1 and R5 can be checked by the controller. If Host Driver checks response error, set this bit to 0 and wait for Command Complete Interrupt and then check the response register. If Host Controller checks response error, set this bit to 1 and set Response Error Check Enable to 1. Command Complete Interrupt is disabled by this bit regardless of Command Complete Signal Enable. ■ 0 - Response Interrupt enabled ■ 1 - Response Interrupt is disabled Note: While carrying out tuning (When Execute Tuning bit in Host Control2 register is set), command complete interrupt is not generated irrespective of Response Interrupt Disable setting. Values: ■ 0x0 (ENABLED): Response Interrupt enabled ■ 0x1 (DISABLED): Response Interrupt is disabled	RW
7	RESP_ERR_CHK_EN	Response Error Check Enable Host Controller supports response check function to avoid overhead of response error check by Host driver. Only R1	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		and R5 can be checked by the controller. If Host Controller checks the response error, set this bit to 1 and set Response Interrupt Disable to 1. If an error is detected, Response Error interrupt is generated in the Error Interrupt Status register. ■ 1 - Response Error Check is enabled ■ 0 - Response Error Check is disabled Note: ■ Response error check should not be enabled for any reponse type other than R1 and R5. ■ Response check should not be enabled for tuning command. Values: ■ 0x1 (ENABLED): Response Error Check is enabled ■ 0x1 (DISABLED): Response Error Check is disabled	
6	RESP_TYPE	Response Type R1/R5 When response error check is enabled, this bit selects either R1 or R5 response types. Error statuses checked in R1: ■ OUT_OF_RANGE ■ ADDRESS_ERROR ■ BLOCK_LEN_ERROR ■ WP_VIOLATION ■ CARD_IS_LOCKED ■ COM_CRC_ERROR ■ CARD_ECC_FAILED ■ CC_ERROR ■ ERROR Response Flags checked in R5: ■ COM_CRC_ERROR ■ ERROR ■ FUNCTION_NUMBER ■ OUT_OF_RANGE ■ 1 - R5 (SDIO) ■ 0 - R1 (Memory) Values: ■ 0x0 (RESP_R1): R1 (Memory) ■ 0x1 (RESP_R5): R5 (SDIO)	RW
5	MULTI_BLK_SEL	Multi/Single Block Select This bit is set when issuing multiple-block transfer commands using DAT line. If this bit is set to 0, it is not necessary to set Block Count register. ■ 1 - Multiple Block ■ 0 - Single Block	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Values: ■ 0x1 (MULTI): Read (Multiple Block) ■ 0x0 (SINGLE): Write (Single Block)	
4	DATA_XFER_DIR	Data Transfer Direction Select This bit defines the direction of DAT line data transfers. This bit is set to 1 by the Host Driver to transfer data from the SD/eMMC card to the Host Controller and it is set to 0 for all other commands. ■ 1 - Card to Host ■ 0 - Host to Card Values: ■ 0x1 (READ): Read (Card to Host) ■ 0x0 (WRITE): Write (Host to Card)	RW
3:2	AUTO_CMD_EN	Auto Command Enable This field determines use of auto command functions. ■ 00b - Auto Command Disabled ■ 01b - Auto CMD12 Enable ■ 10b - Auto CMD23 Enable ■ 11b - Auto CMD Auto Select Note: In SDIO, this field should be set as 00b (Auto Command Disabled). Values: ■ 0x0 (AUTO_CMD_DISABLED): Auto Command Disabled ■ 0x1 (AUTO_CMD12_ENABLED): Auto CMD12 Enable ■ 0x2 (AUTO_CMD23_ENABLED): Auto CMD23 Enable ■ 0x3 (AUTO_CMD_AUTO_SEL): Auto CMD Auto Select	RW
1	BLK_CNT_EN	Block Count Enable This bit is used to enable the Block Count register, which is relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. Host Driver should set this bit to 0 when ADMA is used. ■ 1 - Enable ■ 0 - Disable Values: ■ 0x1 (ENABLED): Enable ■ 0x0 (DISABLED): Disable	RW
0	DMA_EN	DMA Enable This bit enables the DMA functionality. If this bit is set to 1, a DMA operation begins when Host Driver writes to Command register. You can select one of the DMA modes by using DMA Select in the HostControl 1 register. ■ 1 - DMA Data transfer	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 0 - No data transfer or Non-DMA data transfer Values: ■ 0x1 (ENABLED): DMA Data transfer ■ 0x0 (DISABLED): No data transfer or Non DMA data transfer	

32.5.2.6 Command register (CMD_R, 0x0e)

	CMD_R								BASE + 0x0e							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		CMD_INDEX						CMD_TYPE		DATA_PRES_SEL	CMD_IDX_CHK_EN	CMD_CRC_CHK_EN	SUB_CMD_FLAG	RESP_TYPE_SEL	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:14	Reserved	Writing has no effect, read as zero.	R
13:8	CMD_INDEX	Command Index These bits shall be set to the command number that is specified in bits 45-40 of the Command Format.	RW
7:6	CMD_TYPE	Command Type These bits indicate the command type. ■ 00b - Normal command ■ 01b - Suspend command ■ 10b - Resume command ■ 11b - Abort command Values: ■ 0x3 (ABORT_CMD): Abort ■ 0x2 (RESUME_CMD): Resume ■ 0x1 (SUSPEND_CMD): Suspend ■ 0x0 (NORMAL_CMD): Normal	RW
5	DATA_PRES_SEL	Data Present Select This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. ■ 0 - No Data Present ■ 1 - Data Present This bit is set to 0 in the following instances: ■ Command using CMD line	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ Command with no data transfer but using busy signal on DAT[0] line ■ Resume Command Values: ■ 0x0 (NO_DATA): No Data Present ■ 0x1 (DATA): Data Present	
4	CMD_IDX_CHK_EN	Command Index Check Enable If this bit is set, Host Controller shall check the index field in the response to verify if it has the same value as the command index. If it is not, it is reported as a Command Index error. ■ 0 - Disable ■ 1 - Enable Note: ■ Index Check enable should be set to 0 for the command with no response, R2 response, R3 response and R4 response. ■ For tuning command, this bit should always be set to enable the index check. Values: ■ 0x0 (DISABLED): Disable ■ 0x1 (ENABLED): Enable	RW
3	CMD_CRC_CHK_EN	Command CRC Check Enable If this bit is set, Host Controller shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC error. ■ 0 - Disable ■ 1 - Enable Note: - CRC Check enable should be set to 0 for the command with no response, R3 response and R4 response. - For tuning command, this bit should always be set to 1 to enable the CRC check. Values: ■ 0x0 (DISABLED): Disable ■ 0x1 (ENABLED): Enable	RW
2	SUB_CMD_FLAG	Sub Command Flag This bit distinguishes a main command or a sub command. ■ 0 - Main Command ■ 1 - Sub Command Values: ■ 0x0 (MAIN): Main Command ■ 0x1 (SUB): Sub Command	RW
1:0	RESP_TYPE_SEL	Response Type Select	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		This bit indicates the type of response expected from the card. ■ 00b - No Response ■ 01b - Response Length 136 ■ 10b - Response Length 48 ■ 11b - Response Length 48 check (Busy after response) Values: ■ 0x0 (NO_RESP): No Response ■ 0x1 (RESP_LEN_136): Response Length 136 ■ 0x2 (RESP_LEN_48): Response Length 48 ■ 0x3 (RESP_LEN_48B): Response Length 48 check Busy after response	

32.5.2.7 Response Register 0/1 (RESP01_R, 0x10)

	RESP01_R																														BASE + 0x10	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RESP01																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	RESP01	Command Response These bits reflect bits 39-8 of the Response Field. **Note:** For Auto CMD, the 32-bit response (bits 39-8 of the Response Field) is updated in RESP67_R register. Volatile: true	R

32.5.2.8 Response Register 2/3 (RESP23_R, 0x14)

	RESP23_R																														BASE + 0x14	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RESP23																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	RESP23	Command Response These bits reflect bits 71-40 of the Response Field. Volatile: true	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.5.2.9 Response Register 4/5 (RESP45_R, 0x18)

	RESP45_R																													BASE + 0x18	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RESP45																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	RESP45	Command Response These bits reflect bits 103-72 of the Response Field. Volatile: true	R

32.5.2.10 Response Register 6/7 (RESP67_R, 0x1c)

	RESP67_R																													BASE + 0x1c	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RESP67																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	RESP67	Command Response These bits reflect bits 135-104 of the Response Field. **Note:** For Auto CMD, this register also reflects the 32-bit response (bits 39-8 of the Response Field). Volatile: true	R

32.5.2.11 Buffer Data Port Register (BUF_DATA_R, 0x20)

	BUF_DATA_R																													BASE + 0x20	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BUF_DATA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	BUF_DATA	Buffer Data The Host Controller packet buffer can be accessed through this 32-bit Buffer Data Port register. Volatile: true	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.5.2.12 Present State Register (PSTATE_REG, 0x24)

	PSTATE_REG																												Base + 0x0024	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			SUB_CMD_STAT	CMD_ISSU_ERR	Reserved	HOST_REG_VOL	CMD_LINE_L	DAT_3_0				Reserved								BUF_RD_EN	BUF_WR_EN	RD_XFER_ACT	WR_XFER_ACT	DAT_7_4				RE_TUNE_REQ	DAT_LINE_ACT	CMD_INH_DAT	CMD_INH
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:29	Reserved	Writing has no effect, read as zero.	R
28	SUB_CMD_STAT	Sub Command Status This status is used to distinguish main command and sub command status. ■ 0 - Main Command Status ■ 1 - Sub Command Status Values: ■ 0x0 (FALSE): Main Command Status ■ 0x1 (TRUE): Sub Command Status Volatile: true	R
27	CMD_ISSU_ERR	Command Not Issued by Error This bit is set if a command cannot be issued after setting the command register due to error except Auto CMD12 error ■ 0 - No error for issuing a command ■ 1 - Command cannot be issued Values: ■ 0x0 (FALSE): No error for issuing a command ■ 0x1 (TRUE): Command cannot be issued Volatile: true	R
26	Reserved	Writing has no effect, read as zero.	R
25	HOST_REG_VOL	Host Regulator Voltage Stable This status is used to check whether the host regulator voltage is stable for switching the voltage of UHS-I mode. This bit reflects the synchronized value of host_reg_vol_stablepin. ■ 0 - Host Regulator Voltage is not stable ■ 1 - Host Regulator Voltage is stable	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Values: ■ 0x0 (FALSE): Host Regulator Voltage is not stable ■ 0x1 (TRUE): Host Regulator Voltage is stable Volatile: true	
24	CMD_LINE_L	Command Line Signal Level (SD/eMMC Mode only) This status is used to check the CMD line level to recover from errors and for debugging. These bits reflect the value of sd_cmd_in pin. It is irrelevant for UHS-II mode and always return 0. Volatile: true	R
23:20	DAT_3_0	DAT[3:0] Line Signal Level (SD/eMMC Mode only) This status is used to check the DAT line level to recover from errors and for debugging. These bits reflect the value of sd_dat_in(lower nibble) pin. Volatile: true	R
19:12	Reserved	Reading has no effect	R
11	BUF_RD_EN	Buffer Read Enable This status is used for non-DMA transfers. This bit is set if valid data exists in Host buffer. ■ 0 - Read disable ■ 1 - Read enable Values: ■ 0x0 (DISABLED): Read disable ■ 0x1 (ENABLED): Read enable Volatile: true	R
10	BUF_WR_EN	Buffer Write Enable This status is used for non-DMA transfers. This bit is set if space is available for writing data. ■ 0 - Write disable ■ 1 - Write enable Values: ■ 0x0 (DISABLED): Write disable ■ 0x1 (ENABLED): Write enable Volatile: true	R
9	RD_XFER_ACT	Read Transfer Active (SD/eMMC Mode only) This status indicates whether a read transfer is active. It is irrelevant for UHS-II mode and always returns 0. ■ 0 - No valid data ■ 1 - Transferring data Values: ■ 0x0 (INACTIVE): No valid data ■ 0x1 (ACTIVE): Transferring data Volatile: true	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

8	WR_XFER_ACT	Write Transfer Active (SD/eMMC Mode only) This status indicates whether a write transfer is active. ■ 0 - No valid data ■ 1 - Transferring data Values: ■ 0x0 (INACTIVE): No valid data ■ 0x1 (ACTIVE): Transferring data Volatile: true	R
7:4	DAT_7_4	DAT[7:4] Line Signal Level (Embedded only) This status is used to check the DAT line level to recover from errors and for debugging. These bits reflect the value of sd_dat_in(upper nibble) pin. Volatile: true	R
3	RE_TUNE_REQ	Re-Tuning Request (UHS-I only) Host Controller may request Host Driver to execute re-tuning sequence by setting this bit when the data window is shifted. This bit is cleared when a command is issued with setting Execute Tuning in Host Control 2 register. ■ 0 - Fixed or well-tuned sampling clock ■ 1 - Sampling clock needs re-tuning Values: ■ 0x0 (FIXED): Fixed or well-tuned sampling clock ■ 0x1 (RE_TUNE): Sampling clock need re-tuning Volatile: true	R
2	DAT_LINE_ACT	DAT Line Active (SD/eMMC Mode only) This bit indicates whether one of the DAT lines on the SD/eMMC bus is in use. This bit is irrelevant for UHS-II mode. In the case of read transactions, this status indicates whether a read transfer is executing on the SD/eMMC bus. In the case of write transactions, this status indicates whether a write transfer is executing on the SD/eMMC bus. For command with busy, this status indicates whether command executing busy is executing on the SD/eMMC bus. ■ 0 - DAT Line Inactive ■ 1 - DAT Line Active Values: ■ 0x0 (INACTICE): DAT Line Inactive ■ 0x1 (ACTIVE): DAT Line Active	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Volatile: true	
1	CMD_INH_DAT	Command Inhibit (DAT)(SD/eMMC Mode only) This status bit is generated if either DAT line active or Read transfer active is set to 1. If this bit is 0, it indicates that Host Controller can issue subsequent SD/eMMC commands. ■ 0 - Can issue command that used DAT line ■ 1 - Cannot issue command that used DAT line Values: ■ 0x0 (READY): Can issue command which used DAT line ■ 0x1 (NOT_READY): Cannot issue command which used DAT line Volatile: true	R
0	CMD_INH	Command Inhibit (CMD) In an SD/eMMC mode, if this bit is 0, it indicates that the CMD line is not in use and the Host controller can issue an SD/eMMC command using the CMD line. This bit is set when the command register is written. This bit is cleared when the command response is received. This bit is not cleared by the response of auto CMD12/23 but cleared by the response of read/write command. ■ 0 - Host Controller is not ready to issue a command ■ 1 - Host Controller is ready to issue a command Values: ■ 0x0 (READY): Host Controller is not ready to issue a command ■ 0x1 (NOT_READY): Host Controller is ready to issue a command Volatile: true	R

32.5.2.13 Host Control 1 Register (HOST_CTRL1_R, 0x28)

	HOST_CTRL1_R						BASE + 0x28	
Bit	7	6	5	4	3	2	1	0
	Reserved		EXT_DAT_XFER	DMA_SEL		HS_EN	DAT_XFER_W	Reserved
RST	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
7:6	Reserved	Keep default	RW
5	EXT_DAT_XFER	Extended Data Transfer Width (Embedded and an SD/eMMC Mode only) This bit controls 8-bit bus width mode of embedded device. This bit is not applicable for UHS-II mode. ■ 0 - Bus Width is selected by Data Transfer Width ■ 1 - 8-bit Bus Width Values: ■ 0x1 (EIGHT_BIT): 8-bit Bus Width ■ 0x0 (DEFAULT): Bus Width is selected by Data ransfer Width	RW
4:3	DMA_SEL	DMA Select This field is used to select the DMA type. When Host Version 4 Enable is 1 in Host Control 2 register: ■ 00b - SDMA is selected ■ 01b - Reserved ■ 10b - ADMA2 is selected ■ 11b - ADMA2 or ADMA3 is selected When Host Version 4 Enable is 0 in Host Control 2 register: ■ 00b - SDMA is selected ■ 01b - Reserved ■ 10b - 32-bit Address ADMA2 is selected ■ 11b - 64-bit Address ADMA2 is selected Values: ■ 0x0 (SDMA): SDMA is selected ■ 0x1 (RSVD_BIT): Reserved ■ 0x2 (ADMA2): ADMA2 is selected ■ 0x3 (ADMA2_3): ADMA2 or ADMA3 is selected	RW
2	HS_EN	High Speed Enable (SD/eMMC Mode only) Before setting this bit, the Host Driver shall check the High Speed Support in the Capabilities register. This bit is used to determine the selection of preset value for High Speed mode. This bit is not effective for UHS-II mode. ■ 0 - Normal Speed mode ■ 1 - High Speed mode Note: MSC always outputs the sd_cmd_outand sd_dat_outlines at the rising edge of cclk_txclock irrespective of this bit.Please refer the section Connecting the Clock IO interface in the Mobile Storage Host Controller user guide on clocking requirement for an SD/eMMC card Values:	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 0x1 (HIGH_SPEED): High Speed mode ■ 0x0 (NORMAL_SPEED): Normal Speed mode	
1	DAT_XFER_W	Data Transfer Width (SD/eMMC Mode only) This bit selects the data width of the Host Controller. The Host Driver shall set it to match the data width of the SD/eMMC card. ■ 0 - 1-bit mode ■ 1 - 4-bit mode Values: ■ 0x1 (FOUR_BIT): 4-bit mode ■ 0x0 (ONE_BIT): 1-bit mode	RW
0	Reserved	Keep default	RW

32.5.2.14 Block Gap Control Register (BGAP_CTRL_R, 0x2a)

	BGAP_CTRL_R				BASE + 0x2a			
Bit	7	6	5	4	3	2	1	0
	Reserved				INT_AT_BGAP	RD_WAIT_CTRL	CONT_REQ	STOP_BG_REQ
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:4	Reserved	Writing has no effect, read as zero.	R
3	INT_AT_BGAP	Interrupt At Block Gap (SD Mode only) This bit is valid only in 4-bit mode of SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. ■ 0 - Disabled ■ 1 - Enabled Values: ■ 0x0 (DISABLE): Disabled ■ 0x1 (ENABLE): Enabled	RW
2	RD_WAIT_CTRL	Read Wait Control (SD Mode only) This bit is used to enable the read wait protocol to stop read data using DAT[2] line if the card supports read wait. Otherwise, the Host Controller has to stop the card clock to hold the read data. In UHS-II mode, Read Wait is disabled. ■ 0 - Disable Read Wait Control	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 1 - Enable Read Wait Control Values: ■ 0x0 (DISABLE): Disable Read Wait Control ■ 0x1 (ENABLE): Enable Read Wait Control	
1	CONT_REQ	Continue Request This bit is used to restart the transaction, which was stopped using the Stop At Block Gap Request. The Host Controller automatically clears this bit when the transaction re-starts. If stop at block gap request is set to 1, any write to this bit is ignored. ■ 0 - Not affect ■ 1 - Restart Values: ■ 0x0 (NOT_AFFECT): Not Affect ■ 0x1 (RESTART): Restart Volatile: true	RW
0	STOP_BG_REQ	Stop At Block Gap Request This bit is used to stop executing read and write transaction at the next block gap for non-DMA, SDMA and ADMA transfers. ■ 0 - Transfer ■ 1 - Stop Values: ■ 0x0 (XFER): Transfer ■ 0x1 (STOP): Stop	RW

32.5.2.15 Clock Control Register (CLK_CTRL_R, 0x2c)

	CLK_CTRL_R								BASE + 0x2c							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												PLL_EN	SD_CLK_EN	Reserved	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:4	Reserved	Reading has no effect	R
3	PLL_ENABLE	PLL Enable This bit is used to activate the PLL (applicable when Host Version 4 Enable = 1). The value is reflected on the card_clk_en pin. ■ 0 - PLL is in low power mode	

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 1 - PLL is enabled Values: ■ 0x0 (FALSE): PLL is in low power mode ■ 0x1 (TRUE): PLL is enabled	
2	SD_CLK_EN	SD/eMMC Clock Enable This bit stops the SDCLK or RCLK when this bit is set to 0. SDCLK/RCLK Frequency Select can be changed when this bit is 0. The value is reflected on the clk2card_on pin. ■ 0 - Disable providing SDCLK/RCLK ■ 1 - Enable providing SDCLK/RCLK Values: ■ 0x0 (FALSE): Disable ■ 0x1 (TRUE): Enable	
1:0	Reserved	Keep default	

32.5.2.16 Timeout Control Register (TOUT_CTRL_R, 0x2e)

	TOUT_CTRL_R				BASE + 0x2e			
Bit	7	6	5	4	3	2	1	0
	Reserved				TOUT_CNT			
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:4	Reserved	Writing has no effect, read as zero.	R
3:0	TOUT_CNT	Data Timeout Counter Value. This value determines the interval by which DAT line timeouts are detected. Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Data Timeout Error Status Enable (in the Error Interrupt Status Enable register) ■ 1111b - Reserved ■ 1110b - TMCLK x 2^27 ■ ..... - ..... ■ 0001b - TMCLK x 2^14 ■ 0000b - TMCLK x 2^13 Note: During a boot operating in an eMMC mode, an application should configure the boot data timeout value (approximately 1 sec) in this field.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.5.2.17 Software Reset Register (SW_RST_R, 0x2f)

	SW_RST_R				BASE + 0x2f			
Bit	7	6	5	4	3	2	1	0
	Reserved					SW_RST_DAT	SW_RST_CMD	SW_RST_ALL
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:3	Reserved	Writing has no effect, read as zero.	R
2	SW_RST_DAT	Software Reset For DAT line (SD/eMMC Mode only) This bit resets only a part of the data circuit and the DMA circuit is also reset. ■ 1 - Reset ■ 0 - Work The following registers and bits are cleared by this bit: ■ Buffer Data Port register - Buffer is cleared and initialized. ■ Present state register - Buffer Read Enable - Buffer Write Enable - Read Transfer Active - Write Transfer Active - DAT Line Active - Command Inhibit (DAT) ■ Block Gap Control register - Continue Request - Stop At Block Gap Request ■ Normal Interrupt status register - Buffer Read Ready - Buffer Write Ready - DMA Interrupt - Block Gap Event -Transfer Complete Values: ■ 0x0 (FALSE): Work ■ 0x1 (TRUE): Reset Volatile: true	RW
1	SW_RST_CMD	Software Reset For CMD line Only part of command circuit is reset to be able to issue a	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		command. It is also used toinitialize a UHS-II command circuit. This reset is effective only for a command issuing circuit (including response error statuses related to Command Inhibit (CMD) control) and does not affect the data transfer circuit. Host Controller can continue data transfer even after this reset is executed during handling of subcommand response errors. The following registers and bits are cleared by this bit: - Present State register Command Inhibit (CMD) - Normal Interrupt Status register Command Complete - Error Interrupt Status Response error statuses related to Command Inhibit (CMD) ■ 1 - Reset ■ 0 - Work Values: ■ 0x0 (FALSE): Work ■ 0x1 (TRUE): Reset Volatile: true	
0	SW_RST_ALL	Software Reset For All This reset affects the entire Host Controller except for the card detection circuit. During its initialization, the Host Driver shall set this bit to 1 to reset the Host Controller. All registers are reset except the capabilities register. If this bit is set to 1, the Host Driver should issue reset command and reinitialize the SD/eMMC card. ■ 1 - Reset ■ 0 - Work Values: ■ 0x0 (FALSE): Work ■ 0x1 (TRUE): Reset Volatile: true	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.5.2.18 Normal Interrupt Status Register (NORMAL_INT_STAT_R, 0x30)

	NORMAL_INT_STAT_R															BASE + 0x30
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERR_INT	CQE_EVNT	FX_EVNT	RE_TUNE_EVNT	Reserved						BUF_RD_RDY	BUF_WR_RDY	DMA_INT	BGAP_EVNT	XFER_CMPLT	CMD_CMPLT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	Reserved	Writing has no effect, read as zero.	R
15	ERR_INT	Error Interrupt If any of the bits in the Error Interrupt Status register are set, then this bit is set. ■ 0 - No Error ■ 1 - Error Values: ■ 0x0 (FALSE): No Error ■ 0x1 (TRUE): Error Volatile: true	R
14	CQE_EVNT	Command Queuing Event This status is set if Command Queuing engine related event occurred. Read CQHCI's CQISregister for more details ■ 0 - No Event ■ 1 - Command Queuing Event is detected Values: ■ 0x0 (FALSE): No Event ■ 0x1 (TRUE): Command Queuing Event is detected Volatile: true	R/W1C
13	FX_EVNT	FX Event This status is set when R[14] of response register is set to 1 and Response Type R1/R5 is set to 0 in Transfer Mode register. This interrupt is used with response check function. ■ 0 - No Event ■ 1 - FX Event is detected Values: ■ 0x0 (FALSE): No Event ■ 0x1 (TRUE): FX Event is detected Volatile: true	R
12	RE_TUNE_EVNT	Re-tuning Event (UHS-I only) This bit is set if Re-Tuning Request changes from 0 to 1.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 0 - Re-Tuning is not required ■ 1 - Re-Tuning should be performed Values: ■ 0x0 (FALSE): Re-Tuning is not required ■ 0x1 (TRUE): Re-Tuning should be performed Volatile: true	
11:6	Reserved	Keep default	
5	BUF_RD_RDY	Buffer Read Ready This bit is set if the Buffer Read Enable changes from 0 to 1. ■ 0 - Not ready to read buffer ■ 1 - Ready to read buffer Values: ■ 0x0 (FALSE): Not ready to read buffer ■ 0x1 (TRUE): Ready to read buffer Volatile: true	R/W1C
4	BUF_WR_RDY	Buffer Write Ready This bit is set if the Buffer Write Enable changes from 0 to 1. ■ 0 - Not ready to write buffer ■ 1 - Ready to write buffer Values: ■ 0x0 (FALSE): Not ready to write buffer ■ 0x1 (TRUE): Ready to write buffer Volatile: true	R/W1C
3	DMA_INT	DMA Interrupt This bit is set if the Host Controller detects the SDMA Buffer Boundary during transfer. In case of ADMA, by setting Int field in the descriptor table, Host controller generates this interrupt. This interrupt shall not be generated after Transfer Complete. ■ 0 - No DMA Interrupt ■ 1 - DMA Interrupt is generated Values: ■ 0x0 (FALSE): No DMA Interrupt ■ 0x1 (TRUE): DMA Interrupt is generated Volatile: true	R/W1C
2	BGAP_EVNT	Block Gap Event This bit is set when both read/write transaction is stopped at block gap due to Stop at Block Gap Request. ■ 0 - No block gap event ■ 1 - Transaction stopped Values: ■ 0x0 (FALSE): No Block Gap Event ■ 0x1 (TRUE): Transaction stopped Volatile: true	R/W1C

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	XFER_CMPLT	Transfer Complete This bit is set when a read/write transfer and a command with status busy is completed. ■ 0 - Not complete ■ 1 - Command execution is completed Values: ■ 0x0 (FALSE): Not complete ■ 0x1 (TRUE): Command execution is completed Volatile: true	R/W1C
0	CMD_CMPLT	Command Complete In an SD/eMMC Mode, this bit is set when the end bit of a response except for Auto CMD12 and Auto CMD23. This interrupt is not generated when the Response Interrupt Disable in Transfer Mode Register is set to 1. ■ 0 - No command complete ■ 1 - Command complete Values: ■ 0x0 (FALSE): No command complete ■ 0x1 (TRUE): Command Complete Volatile: true	R/W1C

32.5.2.19 Error Interrupt Status Register (ERROR_INT_STAT_R, 0x32)

	ERROR_INT_STAT_R															BASE + 0x32
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VENDOR_ERR3	VENDOR_ERR2	VENDOR_ERR1	BOOT_ACK_ERR	RESP_ERR	TUNING_ERR	ADMA_ERR	AUTO_CMD_ERR	CUR_LMT_ERR	DAT_END_BIT_ERR	DATA_CRC_ERR	DATA_TOUT_ERR	CMD_IDX_ERR	CMD_END_BIT_ERR	CMD_CRC_ERR	CMD_TOUT_ERR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	VENDOR_ERR3	This 16th register field of Error interrupt status register is reserved. It will always return 0. Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): Error Volatile: true	R/W1C
14	VENDOR_ERR2	This 15th register field of Error interrupt status register is reserved. It will always return 0.	R/W1C

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): Error Volatile: true	
13	VENDOR_ERR1	This 14th register field of Error interrupt status register is reserved. It will always return 0. Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): Error Volatile: true	R/W1C
12	BOOT_ACK_ERR	Boot Acknowledgement Error (eMMC Mode only) This bit is set when there is a timeout for boot acknowledgement or when detecting boot ack status having a value other than 010. This is applicable only when boot acknowledgement is expected and boot feature in MSC is enabled with DWC_MSHC_EMMC_BOOT_EN = 1. Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): Error Volatile: true	R/W1C
11	RESP_ERR	Response Error (SD Mode only) Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If Response Error Check Enable is set to 1 in the Transfer Mode register, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1. ■ 1 - Error ■ 0 - No Error Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): Error Volatile: true	R/W1C
10	TUNING_ERR	Tuning Error (UHS-I Mode only) This bit is set when an unrecoverable error is detected in a tuning circuit except during the tuning procedure (occurrence of an error during tuning procedure is indicated by Sampling Clock Select in the Host Control 2 register). By detecting Tuning Error, Host Driver needs to abort a command executing and perform tuning. To reset tuning circuit, Sampling Clock Select shall be set to 0 before executing tuning procedure. The Tuning Error is higher priority than the other error interrupts generated during data	R/W1C

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		transfer. By detecting Tuning Error, the Host Driver should discard data transferred by a current read/write command and retry data transfer after the Host Controller retrieved from the tuning circuit error. ■ 1 - Error ■ 0 - No Error Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): Error Volatile: true	
9	ADMA_ERR	ADMA Error This bit is set when the Host Controller detects error during ADMA-based data transfer. The error could be due to following reasons: ■ Error response received from System bus (Master I/F) ■ ADMA3,ADMA2 Descriptors invalid ■ CQE Task or Transfer descriptors invalid When the error occurs, the state of the ADMA is saved in the ADMA Error Status register. In eMMC CQE mode: The Host Controller generates this Interrupt when it detects an invalid descriptor data (Valid=0) at the ST_FDS state. ADMA Error State in the ADMA Error Status indicates that an error has occurred in ST_FDS state. The Host Driver may find that Valid bit is not set at the error descriptor. ■ 1 - Error ■ 0 - No Error Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): Error Volatile: true	R/W1C
8	AUTO_CMD_ERR	Auto CMD Error (SD/eMMC Mode only) This error status is used by Auto CMD12 and Auto CMD23. This bit is set when detecting that any of the bits D00 to D05 in Auto CMD Error Status register has changed from 0 to 1. D07 is effective in case of Auto CMD12. Auto CMD Error Status register is valid while this bit is set to 1 and may be cleared by clearing of this bit (another implementation is also allowed). ■ 1 - Error ■ 0 - No Error Values: ■ 0x0 (FALSE): No error	R/W1C

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 0x1 (TRUE): Error Volatile: true	
7	CUR_LMT_ERR	Current Limit Error By setting the SD Bus Power bit in the Power Control register, the Host Controller is requested to supply power for the SD Bus. If the Host Controller supports the Current Limit function, it can be protected from an illegal card by stopping power supply to the card in which case this bit indicates a failure status. A reading of 1 for this bit means that the Host Controller is not supplying power to the SD card due to some failure. A reading of 0 for this bit means that the Host Controller is supplying power and no error has occurred. The Host Controller may require some sampling time to detect the current limit. If the Host Controller does not support this function, this bit shall always be set to 0. ■ 1 - Power fail ■ 0 - No Error Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): Power Fail Volatile: true	R/W1C
6	DAT_END_BIT_ERR	Data End Bit Error (SD/eMMC Mode only) This error occurs either when detecting 0 at the end bit position of read data that uses the DAT line or at the end bit position of the CRC status. ■ 1 - Error ■ 0 - No Error Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): Error Volatile: true	R/W1C
5	DATA_CRC_ERR	Data CRC Error (SD/eMMC Mode only). This error occurs when detecting CRC error when transferring read data which uses the DAT line, when detecting the Write CRC status having a value of other than 010 or when write CRC status timeout. ■ 1 - Error ■ 0 - No Error Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): Error Volatile: true	R/W1C
4	DATA_TOUT_ERR	Data Timeout Error (SD/eMMC Mode only)	R/W1C

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		This bit is set when detecting one of the following timeout conditions: - Busy timeout for R1b, R5b type - Busy timeout after Write CRC status - Write CRC Status timeout - Read Data timeout ■ 1 - Timeout ■ 0 - No Error Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): Time out Volatile: true	
3	CMD_IDX_ERR	Command Index Error (SD/eMMC Mode only) This bit is set if a Command Index error occurs in the command response. ■ 1 - Error ■ 0 - No Error Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): Error Volatile: true	R/W1C
2	CMD_END_BIT_ERR	Command End Bit Error (SD/eMMC Mode only) This bit is set when detecting that the end bit of a command response is 0. ■ 1 - End Bit Error Generated ■ 0 - No Error Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): End Bit error generated Volatile: true	R/W1C
1	CMD_CRC_ERR	Command CRC Error (SD/eMMC Mode only) Command CRC Error is generated in two cases. If a response is returned and the Command Timeout Error is set to 0 (indicating no timeout), this bit is set to 1 when detecting a CRC error in the command response. The Host Controller detects a CMD line conflict by monitoring the CMD line when a command is issued. If the Host Controller drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SD clock edge, then the Host Controller shall abort the command (stop driving CMD line) and set this bit to 1. The Command Timeout Error shall also be set to 1 to distinguish CMD line conflict. ■ 1 - CRC Error Generated	R/W1C

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 0 - No Error Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): CRC error generated Volatile: true	
0	CMD_TOUT_ERR	Command Timeout Error (SD/eMMC Mode only) This bit is set only if no response is returned within 64 SD clock cycles from the end bit of the command. If the Host Controller detects a CMD line conflict, along with Command CRC Error bit, this bit is set to1, without waiting for 64 SD/eMMC card clock cycles. ■ 1 - Time out ■ 0 - No Error Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): Time out Volatile: true	R/W1C

32.5.2.20 Normal Interrupt Status Enable Register (NORMAL_INT_STAT_EN_R, 0x34)

	NORMAL_INT_STAT_EN_R										BASE + 0x34					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	CQE_EVNT_ST_EN	FX_EVNT_ST_EN	RE_TUNE_EVNT_ST_EN	Reserved						BUF_RD_RDY_ST_EN	BUF_WR_RDY_ST_EN	DMA_INT_ST_EN	BGAP_EVNT_ST_EN	XFER_CMPLT_ST_EN	CMD_CMPLT_ST_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	Reserved	Writing has no effect, read as zero.	R
14	CQE_EVNT_ST_EN	CQE Event Status Enable. ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
13	FX_EVNT_ST_EN	FX Event Status Enable. This bit is added from Version 4.10. ■ 1 - Enabled	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	
12	RE_TUNE_EVNT_ST_EN	Re-Tuning Event (UHS-I only) Status Enable ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
11:6	Reserved	Keep default	RW
5	BUF_RD_RDY_ST_EN	Buffer Read Ready Status Enable ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
4	BUF_WR_RDY_ST_EN	Buffer Write Ready Status Enable ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
3	DMA_INT_ST_EN	DMA Interrupt Status Enable ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
2	BGAP_EVNT_ST_EN	Block Gap Event Status Enable ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
1	XFER_CMPLT_ST_EN	Transfer Complete Status Enable ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
0	CMD_CMPLT_ST_EN	Command Complete Status Enable ■ 1 - Enabled	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	

32.5.2.21 Error Interrupt Status Enable Register (ERROR_INT_STAT_EN_R, 0x36)

	ERROR_INT_STAT_EN_R															BASE + 0x36
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VENDOR_ERR_ST_EN3	VENDOR_ERR_ST_EN2	VENDOR_ERR_ST_EN1	BOOT_ACK_ERR_ST_EN	RESP_ERR_ST_EN	TUNING_ERR_ST_EN	ADMA_ERR_ST_EN	AUTO_CMD_ERR_ST_EN	CUR_LMT_ERR_ST_EN	DAT_END_BIT_ERR_ST_EN	DAT_CRC_ERR_ST_EN	DAT_TOUT_ERR_ST_EN	CMD_IDX_ERR_ST_EN	CMD_END_BIT_ERR_ST_EN	CMD_CRC_ERR_ST_EN	CMD_TOUT_ERR_ST_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	VENDOR_ERR_ST_EN3	This 15th bit of Error Interrupt Status Enable register is reserved. It will always return 0. Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
14	VENDOR_ERR_ST_EN2	This 14th bit of Error Interrupt Status Enable register is reserved. It will always return 0. Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
13	VENDOR_ERR_ST_EN1	This 13th bit of Error Interrupt Status Enable register is reserved. It will always return 0. Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
12	BOOT_ACK_ERR_ST_EN	Boot Acknowledgment Error (eMMC Mode only). Setting this bit to 1 enables setting of Boot Acknowledgment Error in Error Interrupt Status register (ERROR_INT_STAT_R). ■ 1 - Enabled ■ 0 - Masked Values:	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	
11	RESP_ERR_ST_EN	Response Error Status Enable (SD Mode only) ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
10	TUNING_ERR_ST_EN	Tuning Error Status Enable (UHS-I Mode only). ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
9	ADMA_ERR_ST_EN	ADMA Error Status Enable. ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
8	AUTO_CMD_ERR_ST_EN	Auto CMD Error Status Enable (SD/eMMC Mode only). ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
7	CUR_LMT_ERR_ST_EN	Current Limit Error Status Enable ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
6	DAT_END_BIT_ERR_ST_EN	Data End Bit Error Status Enable (SD/eMMC Mode only). ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
5	DAT_CRC_ERR_ST_EN	Data CRC Error Status Enable (SD/eMMC Mode only) ■ 1 - Enabled	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	
4	DAT_TOUT_ERR_ST_EN	Data Timeout Error Status Enable (SD/eMMC Mode only) ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
3	CMD_IDX_ERR_ST_EN	Command Index Error Status Enable (SD/eMMC Mode only) ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): Error	RW
2	CMD_END_BIT_ERR_ST_EN	Command End Bit Error Status Enable (SD/eMMC Mode only) ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
1	CMD_CRC_ERR_ST_EN	Command CRC Error Status Enable (SD/eMMC Mode only) ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
0	CMD_TOUT_ERR_ST_EN	Command Timeout Error Status Enable (SD/eMMC Mode only). ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.5.2.22 Normal Interrupt Signal Enable Register (NORMAL_INT_SIGNAL_EN_R, 0x38)

	NORMAL_INT_SIGNAL_EN_R															BASE + 0x38
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	CQE_EVNT_SIG_EN	FX_EVNT_SIG_EN	RE_TUNE_EVNT_SIG_EN	Reserved						BUF_RD_RDY_SIG_EN	BUF_WR_RDY_SIG_EN	DMA_INT_SIG_EN	BGAP_EVNT_SIG_EN	XFER_CMPLT_SIG_EN	CMD_CMPLT_SIG_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	Reserved	Writing has no effect, read as zero.	R
14	CQE_EVNT_SIG_EN	Command Queuing Engine Event Signal Enable ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
13	FX_EVNT_SIG_EN	FX Event Signal Enable ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
12	RE_TUNE_EVNT_SIG_EN	Re-Tuning Event (UHS-I only) Signal Enable. Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
11:6	Reserved	Keep default	RW
5	BUF_RD_RDY_SIG_EN	Buffer Read Ready Signal Enable ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
4	BUF_WR_RDY_SIG_EN	Buffer Write Ready Signal Enable ■ 1 - Enabled ■ 0 - Masked Values:	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	
3	DMA_INT_SIG_EN	DMA Interrupt Signal Enable ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
2	BGAP_EVNT_SIG_EN	Block Gap Event Signal Enable ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
1	XFER_CMPLT_SIG_EN	Transfer Complete Signal Enable ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
0	CMD_CMPLT_SIG_EN	Command Complete Signal Enable ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW

32.5.2.23 Error Interrupt Signal Enable Register (ERROR_INT_SIGNAL_EN_R, 0x3a)

	ERROR_INT_SIGNAL_EN_R															BASE + 0x3a
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VENDOR_ERR_SIG_EN3	VENDOR_ERR_SIG_EN2	VENDOR_ERR_SIG_EN1	BOOT_ACK_ERR_SIG_EN	RESP_ERR_SIG_EN	TUNING_ERR_SIG_EN	ADMA_ERR_SIG_EN	AUTO_CMD_ERR_SIG_EN	CUR_LMT_ERR_SIG_EN	DAT_END_BIT_ERR_SIG_EN	DAT_CRC_ERR_SIG_EN	DAT_TOUT_ERR_SIG_EN	CMD_IDX_ERR_SIG_EN	CMD_END_BIT_ERR_SIG_EN	CMD_CRC_ERR_SIG_EN	CMD_TOUT_ERR_SIG_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
15	VENDOR_ERR_SIG_EN3	This 16th bit of Error Interrupt Signal Enable is reserved. It will always return 0. Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
14	VENDOR_ERR_SIG_EN2	This 15th bit of Error Interrupt Signal Enable is reserved. It will always return 0. Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
13	VENDOR_ERR_SIG_EN1	This 14th bit of Error Interrupt Signal Enable is reserved. It will always return 0. Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
12	BOOT_ACK_ERR_SIG_EN	Boot Acknowledgment Error (eMMC Mode only). Setting this bit to 1 enables generating interrupt signal when Boot Acknowledgement Error in Error Interrupt Status register is set. ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
11	RESP_ERR_SIG_EN	Response Error Signal Enable (SD Mode only) ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
10	TUNING_ERR_SIG_EN	Tuning Error Signal Enable (UHS-I Mode only) ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
9	ADMA_ERR_SIG_EN	ADMA Error Signal Enable ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

8	AUTO_CMD_ERR_SIG_EN	Auto CMD Error Signal Enable (SD/eMMC Mode only) ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
7	CUR_LMT_ERR_SIG_EN	Current Limit Error Signal Enable ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
6	DAT_END_BIT_ERR_SIG_EN	Data End Bit Error Signal Enable (SD/eMMC Mode only) ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
5	DAT_CRC_ERR_SIG_EN	Data CRC Error Signal Enable (SD/eMMC Mode only) ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
4	DAT_TOUT_ERR_SIG_EN	Data Timeout Error Signal Enable (SD/eMMC Mode only) ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
3	CMD_IDX_ERR_SIG_EN	Command Index Error Signal Enable (SD/eMMC Mode only) ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): No error ■ 0x1 (TRUE): Error	RW
2	CMD_END_BIT_ERR_SIG_EN	Command End Bit Error Signal Enable (SD/eMMC Mode only) ■ 1 - Enabled	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	
1	CMD_CRC_ERR_SIG_EN	Command CRC Error Signal Enable (SD/eMMC Mode only) ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW
0	CMD_TOUT_ERR_SIG_EN	Command Timeout Error Signal Enable (SD/eMMC Mode only) ■ 1 - Enabled ■ 0 - Masked Values: ■ 0x0 (FALSE): Masked ■ 0x1 (TRUE): Enabled	RW

32.5.2.24 Auto CMD Status Register (AUTO_CMD_STAT_R, 0x3c)

	AUTO_CMD_STAT_R								BASE + 0x3c							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								C_NOT_A_C12	Reserved	A_C_RESP_ERR	A_C_IDX_ERR	A_C_EBIT_ERR	A_C_CRC_ERR	A_C_TOUT_ERR	A_C12_NOT_EXEC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7	C_NOT_A_C12	Command Not Issued By Auto CMD12 Error If this bit is set to 1, CMD_wo_DAT is not executed due to an Auto CMD12 Error (D04-D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. ■ 1 - Not issued ■ 0 - No error Values:	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 0x1 (TRUE): Not Issued ■ 0x0 (FALSE): No Error Volatile: true	
6	Reserved	Writing has no effect, read as zero.	R
5	A_C_RESP_ERR	Auto CMD Response Error This bit is set when ResponseError Check Enable in the Transfer Mode register is set to 1 and an error is detected in R1 response of either Auto CMD12 or CMD13. This status is ignored if any bit between D00 to D04 is set to 1. ■ 1 - Error ■ 0 - No error Values: ■ 0x1 (TRUE): Error ■ 0x0 (FALSE): No Error Volatile: true	R
4	A_C_IDX_ERR	Auto CMD Index Error This bit is set if the command index error occurs in response to a command. ■ 1 - Error ■ 0 - No error Values: ■ 0x1 (TRUE): Error ■ 0x0 (FALSE): No Error Volatile: true	R
3	A_C_EBIT_ERR	Auto CMD End Bit Error This bit is set when detecting that the end bit of command response is 0. ■ 1 - End Bit Error Generated ■ 0 - No error Values: ■ 0x1 (TRUE): End Bit Error Generated ■ 0x0 (FALSE): No Error Volatile: true	R
2	A_C_CRC_ERR	Auto CMD CRC Error This bit is set when detecting a CRC error in the command response. ■ 1 - CRC Error Generated ■ 0 - No error Values: ■ 0x1 (TRUE): CRC Error Generated ■ 0x0 (FALSE): No Error Volatile: true	R
1	A_C_TOUT_ERR	Auto CMD Timeout Error	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		This bit is set if no response is returned with 64 SDCLK cycles from the end bit of the command. If this bit is set to 1, error status bits (D04-D01) are meaningless. ■ 1 - Time out ■ 0 - No error Values: ■ 0x1 (TRUE): Time out ■ 0x0 (FALSE): No Error Volatile: true	
0	A_C12_NOT_EXEC	Auto CMD12 Not Executed If multiple memory block data transfer is not started due to a command error, this bit is not set because it is not necessary to issue an Auto CMD12. Setting this bit to 1 means that the Host Controller cannot issue Auto CMD12 to stop multiple memory block data transfer, due to some error. If this bit is set to 1, error status bits (D04-D01) is meaningless. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. ■ 1 - Not executed ■ 0 - Executed Values: ■ 0x1 (TRUE): Not Executed ■ 0x0 (FALSE): Executed Volatile: true	R

32.5.2.25 Host Control 2 Register (HOST_CTRL2_R, 0x3e)

	HOST_CTRL2_R								BASE + 0x3e							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	ASYNC_INT_EN	ADDRESSING	HOST_V4_EN	CMD23_EN	ADMA2_LEN_MD	Reserved	Keep0	SMP_CLK_SEL	EXEC_TUNING	Reserved			UHS_MODE_SEL		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	Reserved	Keep default	RW
14	ASYNC_INT_EN	Asynchronous Interrupt Enable This bit can be set if a card supports asynchronous interrupts and Asynchronous Interrupt Support is set to 1 in the Capabilities	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		register. ■ 0 - Disabled ■ 1 - Enabled Values: ■ 0x0 (FALSE): Disabled ■ 0x1 (TRUE): Enabled	
13	ADDRESSING	64-bit Addressing This bit is effective when Host Version 4 Enable is set to 1. ■ 0 - 32 bits addressing ■ 1 - 64 bits addressing Values: ■ 0x0 (FALSE): 32 bits addressing ■ 0x1 (TRUE): 64 bits addressing	RW
12	HOST_V4_EN	Host Version 4 Enable This bit selects either Version 3.00 compatible mode or Version 4 mode. Functions of following fields are modified for Host Version 4 mode: ■ SDMA Address: SDMA uses ADMA System Address (05Fh-058h) instead of SDMA System Address register (003h-000h) ■ ADMA2/ADMA3 selection: ADMA3 is selected by DMA select in Host Control 1 register ■ 64-bit ADMA Descriptor Size: 128-bit descriptor is used instead of 96-bit descriptor when 64-bit Addressing is set to 1 ■ Selection of 32-bit/64-bit System Addressing: Either 32-bit or 64-bit system addressing is selected by 64-bit Addressing bit in this register ■ 32-bit Block Count: SDMA System Address register (003h-000h) is modified to 32-bit Block Count register ■ 0 - Version 3.00 compatible mode ■ 1 - Version 4 mode **Note:** It is recommended not to program ADMA3 Integrated Descriptor Address registers and Command Queuing registers (if applicable) while operating in Host version less than 4 mode (Host Version 4 Enable = 0). Values: ■ 0x0 (FALSE): Version 3.00 compatible mode ■ 0x1 (TRUE): Version 4 mode	RW
11	CMD23_EN	CMD23 Enable If the card supports CMD23, this bit is set to 1. This bit is used to select Auto CMD23 or Auto CMD12 for ADMA3 data transfer. ■ 0 - Auto CMD23 is disabled ■ 1 - Auto CMD23 is enabled Values: ■ 0x0 (FALSE): Auto CMD23 is disabled	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 0x1 (TRUE): Auto CMD23 is enabled	
10	ADMA2_LEN_MD	ADMA2 Length Mode This bit selects ADMA2 Length mode to be either 16-bit or 26-bit. ■ 0 - 16-bit Data Length Mode ■ 1 - 26-bit Data Length Mode Values: ■ 0x0 (FALSE): 16-bit Data Length Mode ■ 0x1 (TRUE): 26-bit Data Length Mode	RW
9	Reserved	Writing has no effect, read as zero.	R
8	Keep0	Please keep this bit 0.	RW
7	SMP_CLK_SEL	Sampling Clock Select (UHS-I only) This bit is used by the Host Controller to select the sampling clock to receive CMD and DAT. This bit is set by the tuning procedure and is valid after the completion of tuning (when Execute Tuning is cleared). Setting this bit to 1 means that tuning is completed successfully and setting this bit to 0 means that tuning has failed. The value is reflected on the sample_cclk_sel pin. ■ 0 - Fixed clock is used to sample data ■ 1 - Tuned clock is used to sample data Values: ■ 0x0 (FALSE): Fixed clock is used to sample data ■ 0x1 (TRUE): Tuned clock is used to sample data Volatile: true	RW
6	EXEC_TUNING	Execute Tuning (UHS-I only) This bit is set to 1 to start the tuning procedure and this bit is automatically cleared when tuning procedure is completed. ■ 0 - Not Tuned or Tuning completed ■ 1 - Execute Tuning Values: ■ 0x0 (FALSE): Not Tuned or Tuning completed ■ 0x1 (TRUE): Execute Tuning Volatile: true	RW
5:3	Reserved	Keep default	RW
2:0	UHS_MODE_SEL	UHS Mode/eMMC Speed Mode Select This field is used to select UHS mode in SD mode of operation. In eMMC mode, this field is used to select eMMC Speed mode. UHS Mode (SD mode only): ■ 000b - SDR12 ■ 001b - SDR25 ■ 010b - SDR50 ■ 011b - SDR104 ■ 100b - DDR50 ■ 101b - Rsvd	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 110b - Rsvd ■ 111b - Rsvd eMMC Speed Mode (eMMC mode only): ■ 000b - Legacy ■ 001b - High Speed SDR ■ 010b - Rsvd ■ 011b - HS200 ■ 100b - High Speed DDR ■ 101b - Rsvd ■ 110b - Rsvd ■ 111b - HS400 Values: ■ 0x0 (SDR12): SDR12 ■ 0x1 (SDR25): SDR25 ■ 0x2 (SDR50): SDR50 ■ 0x3 (SDR104): SDR104 ■ 0x4 (DDR50): DDR50 ■ 0x5 (RSVD5): Reserved ■ 0x6 (RSVD6): Reserved ■ 0x7 (UHS2): Reserved	

32.5.2.26 Capabilites 1 Register (CAPABILITES1_R, 0x40)

	CAPABILITES1_R																BASE + 0x40															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSVD		ASYNC_INT_SUPPORT	SYS_ADDR_64_V3	SYS_ADDR_64_V4				SUS_RES_SUPPORT	SDMA_SUPPORT	HIGH_SPEED_SUPPORT	RSVD	ADMA2_SU{PPORT	Embedded_8_BIT	MAX_BLK_LEN		Reserved															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:30	Resverd		
29	ASYNC_INT_SUPPORT	Asynchronous Interrupt Support (SD Mode only) ■ 1 - Asynchronous Interrupt Supported ■ 0 - Asynchronous Interrupt Not Supported Values: ■ 0x0 (FALSE): Asynchronous Interrupt Not Supported	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 0x1 (TRUE): Asynchronous Interrupt Supported	
28	SYS_ADDR_64_V3	64-bit System Address Support for V3 This bit sets Host Controller to support 64-bit System Addressing of V3 mode. SDMA cannot be used in 64-bit Addressing in Version 3 Mode. If this bit is set to 1, 64-bit ADMA2 with using 96-bit Descriptor can be enabled by setting Host Version 4 Enable (HOST_VER4_ENABLE = 0) and DMA select (DMA_SEL = 11b). ■ 1 - 64-bit System Address for V3 is Supported ■ 0 - 64-bit System Address for V3 is not Supported Values: ■ 0x0 (FALSE): 64-bit System Address for V3 is Not Supported ■ 0x1 (TRUE): 64-bit System Address for V3 is Supported	R
27	SYS_ADDR_64_V4	64-bit System Address Support for V4 This bit sets the Host Controller to support 64-bit System Addressing of V4 mode. When this bit is set to 1, full or part of 64-bit address should be used to decode the Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller registers is effective regardless of setting to 64-bit Addressing in Host Control 2. If this bit is set to 1, 64-bit DMA Addressing for version 4 is enabled by setting Host Version 4 Enable (HOST_VER4_ENABLE = 1) and by setting 64-bit Addressing (ADDRESSING =1) in the Host Control 2 register. SDMA can be used and ADMA2 uses 128-bit Descriptor. - 1 - 64-bit System Address for V4 is Supported ■ 0 - 64-bit System Address for V4 is not Supported Values: ■ 0x0 (FALSE): 64-bit System Address for V4 is Not Supported ■ 0x1 (TRUE): 64-bit System Address for V4 is Supported	R
26:24	Resverd		
23	SUS_RES_SUPPORT	Suspense/Resume Support This bit indicates whether the Host Controller supports Suspend/Resume functionality. If this bit is 0, the Host Driver shall not issue either Suspend or Resume commands because the Suspend and Resume mechanism is not	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		supported. ■ 1 - Supported ■ 0 - Not Supported Values: ■ 0x0 (FALSE): Not Supported ■ 0x1 (TRUE): Supported	
22	SDMA_SUPPORT	SDMA Support This bit indicates whether the Host Controller is capable of using SDMA to transfer data between the system memory and the Host Controller directly. ■ 1 - SDMA Supported ■ 0 - SDMA not Supported Values: ■ 0x0 (FALSE): SDMA not Supported ■ 0x1 (TRUE): SDMA Supported	R
21	HIGH_SPEED_SUPPORT	High Speed Support This bit indicates whether the Host Controller and the Host System supports High Speed mode and they can supply the SD Clock frequency from 25 MHz to 50 MHz. ■ 1 - High Speed Supported ■ 0 - High Speed not Supported Values: ■ 0x0 (FALSE): High Speed not Supported ■ 0x1 (TRUE): High Speed Supported	R
20	Resverd		
19	ADMA2_SUPPORT	ADMA2 Support This bit indicates whether the Host Controller is capable of using ADMA2. ■ 1 - ADMA2 Supported ■ 0 - ADMA2 not Supported Values: ■ 0x0 (FALSE): ADMA2 not Supported ■ 0x1 (TRUE): ADMA2 Supported	R
18	Embedded_8_BIT	8-bit Support for Embedded Device This bit indicates whether the Host Controller is capable of using an 8-bit bus width mode. This bit is not effective when the Slot Type is set to 10b. ■ 1 - 8-bit Bus Width Supported ■ 0 - 8-bit Bus Width not Supported Values: ■ 0x0 (FALSE): 8-bit Bus Width not Supported ■ 0x1 (TRUE): 8-bit Bus Width Supported	R
17:16	MAX_BLK_LEN	Maximum Block Length	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		This bit indicates the maximum block size that the Host driver can read and write to the buffer in the Host Controller. The buffer transfers this block size without wait cycles. The transfer block length is always 512 bytes for the SD Memory irrespective of this bit ■ 00 - 512 Byte ■ 01 - 1024 ■ 10 - 2048 ■ 11 - Reserved Values: ■ 0x0 (ZERO): 512 Byte ■ 0x1 (ONE): 1024 Byte ■ 0x2 (TWO): 2048 Byte ■ 0x3 (THREE): Reserved	
15:0	Resverd		

32.5.2.27 Capabilites 2 Register (CAPABILITES1_R, 0x44)

	CAPABILITES2_R																												BASE + 0x44	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSVD				ADMA3_SUPPORT	RSVD											RE_TUNING_MODES		USE_TUNING_SDR50	RSVD	RETUNE_CNT				RSVD						DDR50_SUPPORT	SDR104_SUPPORT	SDR50_SUPPORT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	Resverd		R
27	ADMA3_SUPPORT	ADMA3 Support This bit indicates whether the Host Controller is capable of using ADMA3. ■ 0 - ADMA3 is not supported ■ 1 - ADMA3 is supported Values: ■ 0x0 (FALSE): ADMA3 not Supported ■ 0x1 (TRUE): ADMA3 Supported	R
26:16	Resverd		R
15:14	RE_TUNING_MODES	Re-Tuning Modes (UHS-I only) This field selects re-tuning method and limits the maximum	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		data length. ■ 00b - Mode 1 - Timer ■ 01b - Mode 2 - Timer and Re-Tuning Request ■ 10b - Mode 3 - Auto Re-Tuning (for transfer) ■ 11b - Reserved Values: ■ 0x0 (MODE1): Timer ■ 0x1 (MODE2): Timer and Re-Tuning Request ■ 0x2 (MODE3): Auto Re-Tuning (for transfer) Timer and Re-Tuning Request ■ 0x3 (RSVD_MODE): Reserved	
13	USE_TUNING_SDR50	Use Tuning for SDR50(UHS-I only) ■ 1 - SDR50 requires tuning ■ 0 - SDR50 does not require tuning Values: ■ 0x0 (ZERO): SDR50 does not require tuning ■ 0x1 (ONE): SDR50 requires tuning	R
12	Resverd		R
11:8	RETUNE_CNT	Timer Count for Re-Tuning (UHS-I only) ■ 0x0 - Re-Tuning Timer disabled; ■ 0x1 - 1 seconds; ■ 0x2 - 2 seconds; ■ 0x3 - 4 seconds; ■ 0xB - 1024 seconds; ■ 0xC - Reserved; ■ 0xD - Reserved; ■ 0xE - Reserved; ■ 0xF - Get information from other source;	R
7:3	Resverd		R
2	DDR50_SUPPORT	DDR50 Support (UHS-I only) ■ 1 - DDR50 is Supported ■ 0 - DDR50 is Not Supported Values: ■ 0x0 (FALSE): DDR50 is not supported ■ 0x1 (TRUE): DDR50 is supported	R
1	SDR104_SUPPORT	SDR104 Support (UHS-I only) SDR104 requires tuning. ■ 1 - SDR104 is Supported ■ 0 - SDR104 is Not Supported Values: ■ 0x0 (FALSE): SDR104 is not supported ■ 0x1 (TRUE): SDR104 is supported	R
0	SDR50_SUPPORT	SDR50 Support (UHS-I only)	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		If SDR104 is supported, this bit shall be set to 1. Bit 45 indicates whether SDR50 requires tuning or not. ■ 1 - SDR50 is Supported ■ 0 - SDR50 is Not Supported Values: ■ 0x0 (FALSE): SDR50 is not supported ■ 0x1 (TRUE): SDR50 is supported	

32.5.2.28 Force Event Register for Auto CMD Error Status register (FORCE_AUTO_CMD_STAT_R, 0x50)

	FORCE_AUTO_CMD_STAT_R								BASE + 0x50							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								FC_CMD_NOT_ISS_AC12	Reserved	FC_AC_RESP_ERR	FC_AC_IDX_ERR	FC_AC_EBIT_ERR	FC_AC_CRC_ERR	FC_AC_TOUT_ERR	FC_AC12_NOT_EXEC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:8	Reserved	Write has no effect. Read as zero.	R
7	FC_CMD_NOT_ISS_AC12	Force Event for Command Not Issued By Auto CMD12 Error ■ 1 - Command not issued by Auto CMD12 Error Status is set ■ 0 - Not Affected Values: ■ 0x1 (TRUE): Command Not Issued By Auto CMD12 Error Status is set ■ 0x0 (FALSE): Not Affected	W
6	Reserved	Write has no effect. Read as zero.	R
5	FC_AC_RESP_ERR	Force Event for Auto CMD Response Error ■ 1 - Auto CMD Response Error Status is set ■ 0 - Not Affected Values: ■ 0x1 (TRUE): Force Event for Auto CMD Response Error	W

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Status is set ■ 0x0 (FALSE): Not Affected	
4	FC_AC_IDX_ERR	Force Event for Auto CMD Index Error ■ 1 - Auto CMD Index Error Status is set ■ 0 - Not Affected Values: ■ 0x1 (TRUE): Force Event for Auto CMD Index Error Status is set ■ 0x0 (FALSE): Not Affected	W
3	FC_AC_EBIT_ERR	Force Event for Auto CMD End Bit Error ■ 1 - Auto CMD End Bit Error Status is set ■ 0 - Not Affected Values: ■ 0x1 (TRUE): Force Event for Auto CMD End Bit Error Status is set ■ 0x0 (FALSE): Not Affected	W
2	FC_AC_CRC_ERR	Force Event for Auto CMD CRC Error ■ 1 - Auto CMD CRC Error Status is set ■ 0 - Not Affected Values: ■ 0x1 (TRUE): Force Event for Auto CMD CRC Error Status is set ■ 0x0 (FALSE): Not Affected	W
1	FC_AC_TOUT_ERR	Force Event for Auto CMD Timeout Error ■ 1 - Auto CMD Timeout Error Status is set ■ 0 - Not Affected Values: ■ 0x1 (TRUE): Force Event for Auto CMD Timeout Error Status is set ■ 0x0 (FALSE): Not Affected	W
0	FC_AC12_NOT_EXEC	Force Event for Auto CMD12 Not Executed ■ 1 - Auto CMD12 Not Executed Status is set ■ 0 - Not Affected Values: ■ 0x1 (TRUE): Auto CMD12 Not Executed Status is set ■ 0x0 (FALSE): Not Affected	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.5.2.29 Force Event Register for Error Interrupt Status (FORCE_ERROR_INT_STAT_R, 0x52)

	FORCE_ERROR_INT_STAT_R															BASE + 0x52
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FC_VENDOR_ERR3	FC_VENDOR_ERR2	FC_VENDOR_ERR1	FC_BOOT_ACK_ERR	FC_RESP_ERR	FC_TUNING_ERR	FC_ADMA_ERR	FC_AUTO_C_ERR	FC_CUR_LMT_ERR	FC_D_END_BIT_ERR	FC_D_CRC_ERR	FC_D_TOUT_ERR	FC_C_IDX_ERR	FC_C_END_BIT_ERR	FC_C_CRC_ERR	FC_C_TOUT_ERR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15	FC_VENDOR_ERR3	This 16th bit of Force Error Interrupt Status register is reserved. It will always return 0. Values: ■ 0x0 (FALSE): Not Affected ■ 0x1 (TRUE): Vendor Specific Error Status is set	W
14	FC_VENDOR_ERR2	This 15th bit of Force Error Interrupt Status register is reserved. It will always return 0. Values: ■ 0x0 (FALSE): Not Affected ■ 0x1 (TRUE): Vendor Specific Error Status is set	W
13	FC_VENDOR_ERR1	This 14th bit of Force Error Interrupt Status register is reserved. It will always return 0. Values: ■ 0x0 (FALSE): Not Affected ■ 0x1 (TRUE): Vendor Specific Error Status is set	W
12	FC_BOOT_ACK_ERR	Force Event for Boot Ack error. Values: ■ 0x0 (FALSE): Not Affected ■ 0x1 (TRUE): Vendor Specific Error Status is set	W
11	FC_RESP_ERR	Force Event for Response Error (SD Mode only) ■ 1 - Response Error Status is set ■ 0 - Not Affected Values: ■ 0x0 (FALSE): Not Affected ■ 0x1 (TRUE): Response Error Status is set	W
10	FC_TUNING_ERR	Force Event for Tuning Error (UHS-I Mode only) ■ 1 - Tuning Error Status is set ■ 0 - Not Affected	W

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Values: ■ 0x0 (FALSE): Not Affected ■ 0x1 (TRUE): Tuning Error Status is set	
9	FC_ADMA_ERR	Force Event for ADMA Error ■ 1 - ADMA Error Status is set ■ 0 - Not Affected Values: ■ 0x0 (FALSE): Not Affected ■ 0x1 (TRUE): ADMA Error Status is set	W
8	FC_AUTO_C_ERR	Force Event for Auto CMD Error (SD/eMMC Mode only) ■ 1 - Auto CMD Error Status is set ■ 0 - Not Affected Values: ■ 0x0 (FALSE): Not Affected ■ 0x1 (TRUE): Auto CMD Error Status is set	W
7	FC_CUR_LMT_ERR	Force Event for Current Limit Error ■ 1 - Current Limit Error Status is set ■ 0 - Not Affected Values: ■ 0x0 (FALSE): Not Affected ■ 0x1 (TRUE): Current Limit Error Status is set	W
6	FC_D_END_BIT_ERR	Force Event for Data End Bit Error (SD/eMMC Mode only) ■ 1 - Data End Bit Error Status is set ■ 0 - Not Affected Values: ■ 0x0 (FALSE): Not Affected ■ 0x1 (TRUE): Data End Bit Error Status is set	W
5	FC_D_CRC_ERR	Force Event for Data CRC Error (SD/eMMC Mode only) ■ 1 - CRC Error Status is set ■ 0 - Not Affected Values: ■ 0x0 (FALSE): Not Affected ■ 0x1 (TRUE): Data CRC Error Status is set	W
4	FC_D_TOUT_ERR	Force Event for Data Timeout Error (SD/eMMC Mode only) ■ 1 - Timeout Error Status is set ■ 0 - Not Affected Values: ■ 0x0 (FALSE): Not Affected ■ 0x1 (TRUE): Data Timeout Error Status is set	W
3	FC_C_IDX_ERR	Force Event for Command Index Error (SD/eMMC Mode only) ■ 1 - Command Index Error Status is set ■ 0 - Not Affected	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Values: ■ 0x0 (FALSE): Not Affected ■ 0x1 (TRUE): Command Index Error Status is set	
2	FC_C_END_BIT_ERR	Force Event for Command End Bit Error (SD/eMMC Mode only) ■ 1 - Command End Bit Error Status is set ■ 0 - Not Affected Values: ■ 0x0 (FALSE): Not Affected ■ 0x1 (TRUE): Command End Bit Error Status is set	W
1	FC_C_CRC_ERR	Force Event for Command CRC Error (SD/eMMC Mode only) ■ 1 - Command CRC Error Status is set ■ 0 - Not Affected Values: ■ 0x0 (FALSE): Not Affected ■ 0x1 (TRUE): Command CRC Error Status is set	W
0	FC_C_TOUT_ERR	Force Event for Command Timeout Error (SD/eMMC Mode only) ■ 1 - Command Timeout Error Status is set ■ 0 - Not Affected Values: ■ 0x0 (FALSE): Not Affected ■ 0x1 (TRUE): Command Timeout Error Status is set	W

32.5.2.30 ADMA Error Status Register (ADMA_ERR_STAT_R, 0x54)

	ADMA_ERR_STAT_R					BASE + 0x54		
Bit	7	6	5	4	3	2	1	0
	Reserved					ADMA_LEN_ERR	ADMA_ERR_STA	
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7:3	Reserved	Write has no effect. Read as zero.	R
2	ADMA_LEN_ERR	ADMA Length Mismatch Error States This error occurs in the following instances: ■ While Block Count Enable is being set, the total data length specified by the Descriptor table is different from that specified by	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		the Block Count and Block Length ■ Total data length cannot be divided by the block length ■ 0 - No Error ■ 1 - Error Values: ■ 0x0 (NO_ERR): No Error ■ 0x1 (ERROR): Error Volatile: true	
1:0	ADMA_ERR_STA	ADMA Error States These bits indicate the state of ADMA when an error occurs during ADMA data transfer. ■ 00b - Stop DMA - SYS_ADR register points to a location next to the error descriptor ■ 01b - Fetch Descriptor - SYS_ADR register points to the error descriptor ■ 10b - Never set this state - Not used ■ 11b - Transfer Data - SYS_ADR register points to a location next to the error descriptor Values: ■ 0x0 (ST_STOP): Stop DMA ■ 0x1 (ST_FDS): Fetch Descriptor ■ 0x2 (UNUSED): Never set this state ■ 0x3 (ST_TFR): Transfer Data Volatile: true	R

32.5.2.31 ADMA System Address Register - Low (ADMA_SA_LOW_R, 0x58)

	ADMA_SA_LOW_R																															Base + 0x58
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADMA_SA_LOW																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	ADMA_SA_LOW	ADMA System Address These bits indicate the lower 32 bits of the ADMA system address. ■ SDMA If Host Version 4 Enable is set to 1, this register holds the system address of the data location ■ ADMA2 This register holds byte address of executing command of the descriptor table	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ ADMA3 This register is set by ADMA3. ADMA2 increments the address of this register that points to the next line, every time a Descriptor line is fetched. Volatile: true	

32.5.2.32 ADMA System Address Register - High (ADMA_SA_HIGH_R, 0x5c)

	ADMA_SA_HIGH_R																															Base + 0x5c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADMA_SA_HIGH																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	ADMA_SA_HIGH	ADMA System Address These bits indicate the higher 32-bit of the ADMA system address. Volatile: true	RW

32.5.2.33 ADMA3 Integrated Descriptor Address Register - Low (ADMA_ID_LOW_R, 0x78)

	ADMA_ID_LOW_R																															Base + 0x78
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADMA_ID_LOW																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	ADMA_ID_LOW	ADMA Integrated Descriptor Address This bit indicates the lower 32-bit of the ADMA Integrated Descriptor address. The start address of Integrated Descriptor is set to this register. The ADMA3 fetches one Descriptor Address and increments this field to indicate the next Descriptor address. Volatile: true	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.5.2.34 ADMA3 Integrated Descriptor Address Register - High (ADMA_ID_ HIGH_R, 0x7c)

	ADMA_ID_ HIGH_R																														Base + 0x7c
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADMA_ID_ HIGH																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	ADMA_ID_ HIGH	ADMA Integrated Descriptor Address These bits indicate the higher 32 bit of the ADMA Integrated Descriptor address. Volatile: true	RW

32.5.2.35 Slot Interrupt Status Register (SLOT_INTR_STATUS_R, 0xfc)

	SLOT_INTR_STATUS_R								BASE + 0xfc							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								INTR_SLOT							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:8	Reserved	Write has no effect. Read as zero.	R
7:0	INTR_SLOT	Interrupt signal for each Slot These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot. A maximum of 8 slots can be defined. If one interrupt signal is associated with multiple slots, the Host Driver can know which interrupt is generated by reading these status bits. By a power on reset or by setting Software Reset For All, the interrupt signal are de-asserted and this status reads 00h. ■ Bit 00 - Slot 1 ■ Bit 01 - Slot 2 ■ Bit 02 - Slot 3 ■ . . ■ . . ■ Bit 07 - Slot 8 Volatile: true	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.5.2.36 Command Queuing Version register (CQVER, 0x180)

	CQVER																												Base + 0x180	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reversed																				EMMC_VER_MJR				EMMC_VER_MIN				EMMC_VER_SUF			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0

Bits	Name	Description	RW
31:12	Reserved	Write has no effect. Read as zero.	R
11:8	EMMC_VER_MJR	This bit indicates the eMMC major version (1st digit left of decimal point) in BCD format.	R
7:4	EMMC_VER_MIN	This bit indicates the eMMC minor version (1st digit right of decimal point) in BCD format.	R
3:0	EMMC_VER_SUF	This bit indicates the eMMC version suffix (2nd digit right of decimal point) in BCD format.	R

32.5.2.37 Command Queuing Capabilities register (CQCAP, 0x180+0x04)

	CQCAP																												Base + 0x180 + 0x04	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reversed																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0

Bits	Name	Description	RW
31:0	Reserved	Write has no effect. Read as zero.	R

32.5.2.38 Command Queuing Configuration register (CQCFG, 0x180+0x08)

	CQCFG																												Base + 0x180 + 0x08	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reversed																			DCMD_EN	Reversed			TASK_DESC_SIZE	Reversed							CQ_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:13	Reserved	Write has no effect. Read as zero.	R
12	DCMD_EN	This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a data transfer descriptor or a direct-command descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor ■ 1 - Task descriptor in slot #31 is a DCMD Task Descriptor ■ 0 - Task descriptor in slot #31 is a data Transfer Task Descriptor	RW
11:9	Reserved	Write has no effect. Read as zero.	R
8	TASK_DESC_SIZE	Bit Value Description This bit indicates the size of task descriptor used in host memory. This bit can only be configured when Command Queuing Enable bit is 0 (command queuing is disabled). ■ 1 - Task descriptor size is 128 bits ■ 0 - Task descriptor size is 64 bits	RW
7:1	Reserved	Write has no effect. Read as zero.	R
0	CQ_EN	Enable command queuing engine (CQE) ■ 1 - Enable CQE ■ 0 - Disable CQE When CQE is disable, the software controls the eMMC bus using the registers between the addresses 0x000 to 0x1FF. Before the software writes to this bit, software shall verify that the eMMC host controller is in idle state and there are no ongoing commands or data transfers. When software wants to exit command queuing mode, it shall clear all previous tasks (if any) before setting this bit to 0. Testable: restore	RW

32.5.2.39 Command Queuing Control register (CQCTL, 0x180+0x0c)

	CQCTL																Base + 0x180 + 0x0c													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reversed																							CLR_ALL_TASKS	Reversed							HALT
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:9	Reserved	Write has no effect. Read as zero.	R
8	CLR_ALL_TASKS	Clear all tasks	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		This bit can only be written whenthe controller is halted. This bit does not clear tasks in the device. The software has to use the CMDQ_TASK_MGMT command to clear device's queue. ■ 1 - Clears all the tasks in the controller ■ 0 - No effect Volatile: true	
7:1	Reserved	Write has no effect. Read as zero.	R
0	HALT	Halt state ■ 1 - Software writes 1 to this bit when it wants to acquire software control over the eMMC bus and to disable CQE from issuing command on the bus. For example, issuing a Discard Task command (CMDQ_TASK_MGMT). When the software writes 1, CQE shall complete the ongoing task (if any in progress). After the task is completed and the CQE is in idle state, CQE shall not issue new commands and shall indicate to the software by setting this bit to 1. The software can poll on this bit until it is set to 1 and only then send commands on the eMMC bus. ■ 0 - Software writes 0 to this bit to exit from the halt state and resume CQE activity. Volatile: true	RW

32.5.2.40 Command Queuing Interrupt Status register (CQIS, 0x180+0x10)

	CQIS																Base + 0x180 + 0x10															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reversed																												TCL	RED	TCC	HAC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Write has no effect. Read as zero.	R
3	TCL	Task cleared interrupt This status bit is asserted (if CQISTE.TCL_STE=1) when a task clear operation is completed by CQE. The completed task clear operation is either an individual task clear (by writing CQTCLR) or clearing of all tasks (by writing CQCTL). A value of 1 clears this status bit. Volatile: true	R/W1C
2	RED	Response error detected interrupt This status bit is asserted (if CQISTE.RED_STE=1) when a response is received with an error bit set in the device status field.	R/W1C

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Configure the CQRMEM register to identify device status bit fields that may trigger an interrupt and that are masked. A value of 1 clears this status bit. Volatile: true	
1	TCC	Task complete interrupt This status bit is asserted (if CQISTE.TCC_STE=1) when at least one of the following conditions are met: ■ A task is completed and the INT bit is set in its Task Descriptor ■ Interrupt caused by Interrupt Coalescing logic due to timeout ■ Interrupt Coalescing logic reached the configured threshold A value of 1 clears this status bit Volatile: true	R/W1C
0	HAC	Halt complete interrupt This status bit is asserted (only if CQISTE.HAC_STE=1) when halt bit in the CQCTL register transitions from 0 to 1 indicating that the host controller has completed its current ongoing task and has entered halt state. A value of 1 clears this status bit. Volatile: true	R/W1C

32.5.2.41 Command Queuing Interrupt Status Enable register (CQISE, 0x180+0x14)

	CQISE																Base + 0x180 + 0x14															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reversed																												TCL_STE	RED_STE	TCC_STE	HAC_STE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Write has no effect. Read as zero.	R
3	TCL_STE	Task cleared interrupt status enable ■ 1 - CQIS.TCL will be set when its interrupt condition is active ■ 0 - CQIS.TCL is disabled	RW
2	RED_STE	Response error detected interrupt status enable ■ 1 - CQIS.RED will be set when its interrupt condition is active ■ 0 - CQIS.RED is disabled	RW
1	TCC_STE	Task complete interrupt status enable ■ 1 - CQIS.TCC field will be set when its interrupt condition is active ■ 0 - CQIS.TCC field is disabled	RW
0	HAC_STE	Halt complete interrupt status enable ■ 1 - CQIS.HAC will be set when its interrupt condition is active ■ 0 - CQIS.HAC is disabled	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.5.2.42 Command Queuing Interrupt signal enable register (CQISGE, 0x180+0x18)

	CQISGE																Base + 0x180 + 0x18															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reversed																												TCL_SGE	RED_SGE	TCC_SGE	HAC_SGE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:4	Reserved	Write has no effect. Read as zero.	R
3	TCL_SGE	Task cleared interrupt signal enable ■ 1 - CQIS.TCL interrupt generation is active ■ 0 - CQIS.TCL interrupt generation is disabled	RW
2	RED_SGE	Response error detected interrupt signal enable ■ 1 - CQIS.RED interrupt generation is active ■ 0 - CQIS.RED interrupt generation is disabled	RW
1	TCC_SGE	Task complete interrupt signal enable ■ 1 - CQIS.TCC interrupt generation is active ■ 0 - CQIS.TCC interrupt generation is disabled	RW
0	HAC_SGE	Halt complete interrupt signal enable ■ 1 - CQIS.HAC interrupt generation is active ■ 0 - CQIS.HAC interrupt generation is disabled	RW

32.5.2.43 Command Queuing Interrupt Coalescing register (CQIC, 0x180+0x1c)

	CQIC																Base + 0x180 + 0x1c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTC_EN	Reversed										INTC_STAT	Reversed			INTC_RST	INTC_TH_WEN	Reversed		INTC_TH					TOUT_VAL_WEN	TOUT_VAL							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	INTC_EN	Interrupt Coalescing Enable Bit ■ 1 - Interrupt coalescing mechanism is active. Interrupts are counted and timed, and coalesced interrupts are generated. ■ 0 - Interrupt coalescing mechanism is disabled (Default)	RW
30:21	Reserved	Write has no effect. Read as zero.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

20	INTC_STAT	Interrupt Coalescing Status Bit This bit indicates to the software whether any tasks (with INT=0) have completed and counted towards interrupt coalescing (that is, this is set if and only if INTC counter > 0). ■ 1 - At least one task completion has been counted (INTC counter > 0) ■ 0 - Task completions have not occurred since last counter reset (INTC counter == 0)	R
19:17	Reserved	Write has no effect. Read as zero.	R
16	INTC_RST	Counter and Timer Reset When host driver writes 1, the interrupt coalescing timer and counter are reset.	W
15	INTC_TH_WEN	When software writes 1 to this bit, the value INTC_TH is updated with the contents written on the same cycle.	W
14:13	Reserved	Write has no effect. Read as zero.	R
12:8	INTC_TH	Interrupt Coalescing Counter Threshold filed Software uses this field to configure the number of task completions (only tasks with INT=0 in the Task Descriptor), which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT=0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in INTC_TH, and generates interrupt. ■ 0x0 - Interrupt coalescing feature disabled ■ 0x0 - Interrupt coalescing interrupt generated after 1 task when INT=0 completes ■ 0x1 - Interrupt coalescing interrupt generated after 2 tasks when INT=0 completes ■ ... ■ 0x0 - Interrupt coalescing interrupt generated after 31 tasks when INT=0 completes To write to this field, the INTC_TH_WEN bit must be set during the same write operation. Testable: untestable	W
7	TOUT_VAL_WEN	When software writes 1 to this bit, the value TOUT_VAL is updated with the contents written on the same cycle.	W
6:0	TOUT_VAL	Interrupt Coalescing Timeout Value Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when the first data	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		transfer task with INT=0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field, it generates an interrupt and stops. The timer's unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. ■ 0x0 - Timer is disabled. Timeout-based interrupt is not generated. ■ 0x1 - Timeout on 01x1024 cycles of timer clock frequency. ■ 0x2 - Timeout on 02x1024 cycles of timer clock frequency. ■ .... ■ 0x7f - Timeout on 127x1024 cycles of timer clock frequency. In order to write to this field, the TOUT_VAL_WEN bit must be set at the same write operation. Testable: untestable	

32.5.2.44 Command Queuing Task Descriptor List Base Address register (CQTDLBA, 0x180+0x20)

	CQTDLBA																Base + 0x180 + 0x20															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TDLBA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	TDLBA	This register stores the LSB bits (31:0) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * (Task Descriptor size + Transfer Descriptor size) as configured by the host driver. This address shall be set on 1 KB boundary. The lower 10 bits of this register shall be set to 0 by software and shall be ignored by CQE.	RW

32.5.2.45 Command Queuing Task Descriptor List Base Address Upper register (CQTDLBAU, 0x180+0x24)

	CQTDLBAU																Base + 0x180 + 0x24															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TDLBAU																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	TDLBAU	This register stores the MSB bits (63:32) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This address shall be set on 1 KB boundary. The lower 10 bits of this register shall be set to 0 by software and shall be ignored by CQE. This register is reserved when using 32-bit addressing mode.	RW

32.5.2.46 Command Queuing DoorBell register (CQTDLBR, 0x180+0x28)

	CQTDLBR																Base + 0x180 + 0x28															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TDLBR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	TDLBR	Software shall configure TDLBA and TDLBAU, and enable CQE in CQCFG before using this register. Writing 1 to bit n of this register triggers CQE to start processing the task encoded in slot n of the TDL. Writing 0 by software shall have no impact on the hardware, and will not change the value of the register bit. CQE always processes tasks according to the order submitted to the list by CQTDBR write transactions. CQE processes Data Transfer tasks by reading the Task Descriptor and sending QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) commands to the device. CQE processes DCMD tasks (in slot #31, when enabled) by reading the Task Descriptor, and generating the command encoded by its index and argument. The corresponding bit is cleared to 0 by CQE in one of the following events: ■ A task execution is completed (with success or error). ■ The task is cleared using CQTCLR register. ■ All tasks are cleared using CQCTL register. ■ CQE is disabled using CQCFG register. Software may initiate multiple tasks at the same time (batch submission) by writing 1 to multiple bits of this register in the same transaction. In the case of batch submission, CQE shall process the	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		tasks in order of the task index, starting with the lowest index. If one or more tasks in the batch are marked with QBR, the ordering of execution will be based on said processing order.	

32.5.2.47 Command Queuing TaskClear Notification register (CQTCN, 0x180+0x2c)

	CQTCN																															
																	Base + 0x180 + 0x2c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCN																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	TCN	Task Completion Notification Each of the 32 bits are bit mapped to the 32 tasks ■ Bit-N(1) - Task-N has completed execution (with success or errors) ■ Bit-N(0) - Task-N has not completed, could be pending or not submitted. On task completion, software may read this register to know tasks that have completed. After reading this register, software may clear the relevant bit fields by writing 1 to the corresponding bits.	R/ W1C

32.5.2.48 Device queue status register (CQDQS, 0x180+0x30)

	CQDQS																															
																	Base + 0x180 + 0x30															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DQS																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DQS	Device Queue Status Each of the 32 bits are bit mapped to the 32 tasks. ■ Bit-N(1) - Device has marked task N as ready for execution ■ Bit-N(0) - Task-N is not ready for execution. This task could be pending in device or not submitted. Host controller updates this register with response of the Device Queue Status command.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.5.2.49 Device pending tasks register (CQDPT, 0x180+0x34)

	CQDPT																															
																	Base + 0x180 + 0x34															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DPT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DPT	Device-Pending Tasks Each of the 32 bits are bit mapped to the 32 tasks. ■ Bit-N(1) - Task-N has been successfully queued into the device and is awaiting execution ■ Bit-N(0) - Task-N is not yet queued. Bit n of this register is set if and only if QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) were sent for this specific task and if this task has not been executed. The controller sets this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution. Software reads this register in the task-discard procedure to determine if the task is queued in the device.	R

32.5.2.50 Command Queuing DoorBell register (CQTCLR, 0x180+0x38)

	CQTCLR																															
																	Base + 0x180 + 0x38															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCLR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	TCLR	Writing 1 to bit n of this register orders CQE to clear a task that the software has previously issued. This bit can only be written when CQE is in Halt state as indicated in CQCFG register Halt bit. When software writes 1 to a bit in this register, CQE updates the value to 1, and starts clearing the data structures related to the task. CQE clears the bit fields (sets a value of 0) in CQTCLR and in CQTDBR once the clear operation is complete. Software should poll on the CQTCLR until itis cleared to verify that a clear operation was done.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.5.2.51 CQ Send Status Configuration 1 register (CQSSC1, 0x180+0x40)

	CQSSC1																Base + 0x180 + 0x40															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												SQSCMD_BLK_CNT				SQSCMD_IDLE_TMR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:20	Reserved	Write has no effect. Read as zero.	R
19:16	SQSCMD_BLK_CNT	This field indicates when SQS CMD is sent while data transfer is in progress. A value of 'n' indicates that CQE shall send status command on the CMD line, during the transfer of data block BLOCK_CNT-n, on the data lines, where BLOCK_CNT is the number of blocks in the current transaction. ■ 0 - SEND_QUEUE_STATUS (CMD13) command shall not be sent during the transaction. Instead it will be sent only when the data lines are idle. ■ 1 - SEND_QUEUE_STATUS command is to be sent during the last block of the transaction.	RW
19:16	SQSCMD_IDLE_TMR	This field configures the polling period to be used when using periodic SEND_QUEUE_STATUS (CMD13) polling.Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicates that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS. Timer units are clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. The minimum value is 0001h (1 clock period) and the maximum value is FFFFh (65535 clock periods). For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in CQSSC1.CIT is 1000h, the calculated polling period is 4096*52.08 ns= 213.33 ns.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.5.2.52 CQ Send Status Configuration 2 register (CQSSC2, 0x180+0x44)

	CQSSC2																Base + 0x180 + 0x44															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																SQSCMD_RCA																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Write has no effect. Read as zero.	R
15:0	SQSCMD_RCA	This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_STATUS (CMD13) command argument. CQE will copy this field to bits31:16 of the argument when transmitting SEND_ QUEUE_STATUS (CMD13) command.	RW

32.5.2.53 Command response for direct command register (CQCRDCT, 0x180+0x48)

	CQCRDCT																Base + 0x180 + 0x48															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCMD_RESP																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DCMD_RESP	This register contains the response of the command generated by the last direct command (DCMD) task that was sent. Contents of this register are valid only after bit 31 of CQTDBR register is cleared by the controller.	R

32.5.2.54 Command response mode error mask register (CQRMEM, 0x180+0x50)

	CQRMEM																Base + 0x180 + 0x50															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RESP_ERR_MASK																															
RST	1	1	1	1	1	1	0	1	1	1	1	1	1	0	0	1	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	RESP_ERR_MASK	The bits of this field are bit mapped to the device response. This bit is used as an interrupt mask on the device status filed that is received in R1/R1b responses. ■ 1 - When a R1/R1b response is received, with a bit i in the device status set, a RED interrupt is generated. ■ 0 - When a R1/R1b response is received, bit i in the device status is ignored. The reset value of this register is set to trigger an interrupt on all "Error" type bits in the device status. **Note**: Responses to CMD13 (SQS) encode the QSR so that they are ignored by this logic. Value After Reset: 0xfdf9a080	RW

32.5.2.55 CQ Task Error Information register (CQTERRI, 0x180+0x54)

	CQTERRI																Base + 0x180 + 0x54													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRANS_ERR_FIELDS_VALID	Reserved		TRANS_ERR_TASKID					Reserved		TRANS_ERR_CMD_INDX						RESP_ERR_FIELDS_VALID	Reserved		RESP_ERR_TASKID					Reserved		RESP_ERR_CMD_INDX					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	TRANS_ERR_FIELDS_VALID	This bit is updated when an error is detected when a command transaction was in progress. ■ 0 - Ignore contents of TRANS_ERR_TASKID and TRANS_ERR_CMD_INDX ■ 1 - Response-related error detected. Check contents of TRANS_ERR_TASKID and TRANS_ERR_CMD_INDX fields	R
30:29	Reserved	Write has no effect. Read as zero.	R
28:24	TRANS_ERR_TASKID	This field captures the ID of the task that was executed and whose data transfer has errors.	
23:22	Reserved	Write has no effect. Read as zero.	R
21:16	TRANS_ERR_CMD_INDX	This field captures the index of the command that was executed and whose data transfer has errors.	R
15	RESP_ERR_FIELDS_VALID	This bit is updated when an error is detected while a command transaction was in progress.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		■ 0 - Ignore contents of RESP_ERR_TASKID and RESP_ERR_CMD_INDX ■ 1 - Response-related error is detected. Check contents of RESP_ERR_TASKID and RESP_ERR_CMD_INDX fields	
14:13	Reserved	Write has no effect. Read as zero.	R
12:8	RESP_ERR_TASKID	This field captures the ID of the task which was executed on the command line when the error occurred.	R
14:13	Reserved	Write has no effect. Read as zero.	R
5:0	RESP_ERR_CMD_INDX	This field captures the index of the command that was executed on the command line when the error occurred.	R

32.5.2.56 CQ Command response index (CQCRI, 0x180+0x58)

	CQCRI																Base + 0x180 + 0x58													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										CMD_RESP_INDX					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Write has no effect. Read as zero.	R
5:0	CMD_RESP_INDX	Last Command Response index This field stores the index of the last received command response. Controller updates the value every time a command response is received.	R

32.5.2.57 CQ Command response argument register (CQCRA, 0x180+0x5c)

	CQCRA																Base + 0x180 + 0x5c													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMD_RESP_ARG																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	CMD_RESP_ARG	Last Command Response argument This field stores the argument of the last received command response. Controller updates the value every time a command response is received.	R

32.5.2.58 eMMC Control register (EMMC_CTRL_R, 0x500+0x2c)

	EMMC_CTRL_R								BASE + 0x500 + 0x2c							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					CQE_PREFETCH_DISABLE	CQE_ALGO_SEL	ENH_STROBE_ENABLE	Reserved						DISABLE_DATA_CRC_CHK	CARD_IS_EMMC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:11	Reserved	Write has no effect. Read as zero.	R
10	CQE_PREFETCH_DISABLE	Enable or Disable CQE's PREFETCH feature This field allows Software to disable CQE's data prefetch feature when set to 1. ■ 0 - Data Prefetch ENABLED ■ 1 - Data prefetch DISABLED Values: ■ 0x0 (PREFETCH_ENABLE): CQE can Prefetch data for sucessive WRITE transfers and pipeline sucessive READ transfers ■ 0x1 (PREFETCH_DISABLE): Prefetch for WRITE and Pipeline for READ are disabled	RW
9	CQE_ALGO_SEL	Scheduler algorithm selected for execution This bit selects the Algorithm used for selecting one of the many ready tasks for execution. ■ 0 - High-Priority Tasks preferred over Normal-Priority Tasks. Order of DBR rings (First come First served) is used to resolve contention among equal priority tasks ■ 1 - First come First served, The order of DBR rings decide a Task's preference for execution Values: ■ 0x0 (PRI_REORDER_PLUS_FCFS): Priority based reordering with FCFS to resolve equal priority tasks ■ 0x1 (FCFS_ONLY): First come First serve, in the order of DBR	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		rings	
8	ENH_STROBE_ENABLE	Enhanced Strobe Enable This bit instructs MSC to sample the CMD line using data strobe for HS400 mode. ■ 1 - CMD line is sampled using data strobe for HS400 mode ■ 0 - CMD line is sampled using cclk_rx for HS400 mode Values: ■ 0x1 (ENH_STB_FOR_CMD): CMD line is sampled using data strobe for HS400 mode ■ 0x0 (NO_STB_FOR_CMD): CMD line is sampled using cclk_rx for HS400 mode	RW
7:2	Reserved	Write has no effect. Read as zero.	R
1	DISABLE_DATA_CRC_CHK	Disable Data CRC Check This bit controls masking of CRC16 error for Card Write in eMMC mode. This is useful in bus testing (CMD19) for an eMMC device. In bus testing, an eMMC card does not send CRC status for a block, which may generate CRC error. This CRC error can be masked using this bit during bus testing. ■ 1 - DATA CRC check is disabled ■ 0 - DATA CRC check is enabled Values: ■ 0x1 (DISABLE): DATA CRC check is disabled ■ 0x0 (ENABLE): DATA CRC check is enabled	RW
0	CARD_IS_EMMC	eMMC Card present This bit indicates the type of card connected. An application program this bit based on the card connected to MSHC. ■ 1 - eMMC card ■ 0 - Non-eMMC card Values: ■ 0x1 (EMMC_CARD): Card connected to MSHC is eMMC card ■ 0x0 (NON_EMMC_CARD): Card connected to MSHC is non eMMC card	RW

32.6 Data Flow

The host controller communicates to the software driver using the system bus interface and to the card using the SD Bus interface. Figure 32-2 depicts the high level data flow through the Host controller.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

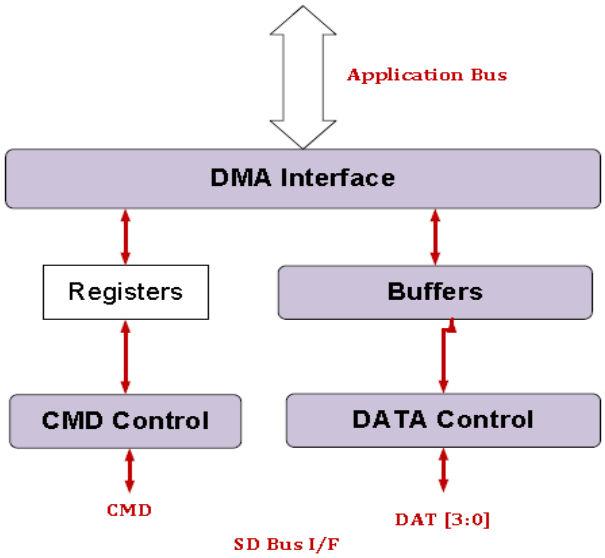


Figure 32-2 Host Controller Data Flow

The host driver can transfer data using either a programmed I/O method or using any of the defined DMA methods. In the Programmed Input/Output (PIO) method of data transfer, data is transferred to the system memory by the host driver. It is done either on the basis of block (SD/eMMC). In a card write, the controller provides Buffer Write ready interrupt when it has space for one block. Based on this interrupt, the host driver must transfer one block of data from system memory to the Msc buffer through the Buffer data port. After that block is sent to card by controller, the same mechanism is used in the reverse direction in the case of card read using the Buffer read ready interrupt. PIO mode is much slower and burdens the processor. It is recommended not to use the PIO mode for large transfers.

Following are different DMA methods described in SD standards:

- Single operation DMA (SDMA)
- Advanced DMA-2 (ADMA2)
- Advanced DMA-3 (ADMA3)

The capabilities register defined by the standard provides the information of type of DMA support provided by the particular controller.

DMA supports both single block and multi-block transfers. The control bits in the Block Gap Control register is used to Stop and Restart a DMA operation. SDMA mode is used for short data transfer as it generates interrupts at page boundaries. ADMA2 and ADMA3 are used for long data transfers and use scatter-gather algorithms. ADMA2 supports single READ/WRITE SD operation at a time while ADMA3 supports multiple READ/WRITE SD operation at a time.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

SD mode command generation is done by writing into the following registers:

- System address
- Block Size
- Block count
- Transfer mode
- Command

32.6.1 ADMA2 Operation

Figure 32-3 shows the ADMA2 data transfer between the host controller and the system memory and it shows the descriptor table that is created by the host driver. A 32-bit address descriptor table is used for a system with 32-bit addressing. In the descriptor table, ach line contains information about the address, its length and an attributes that specifies the operation of the descriptor line. ADMA2 uses the 64-bit ADMA address register for the descriptor pointer. An ADMA2 transfer is triggered by writing to the command register and ADMA2 processes each line in the descriptor table.

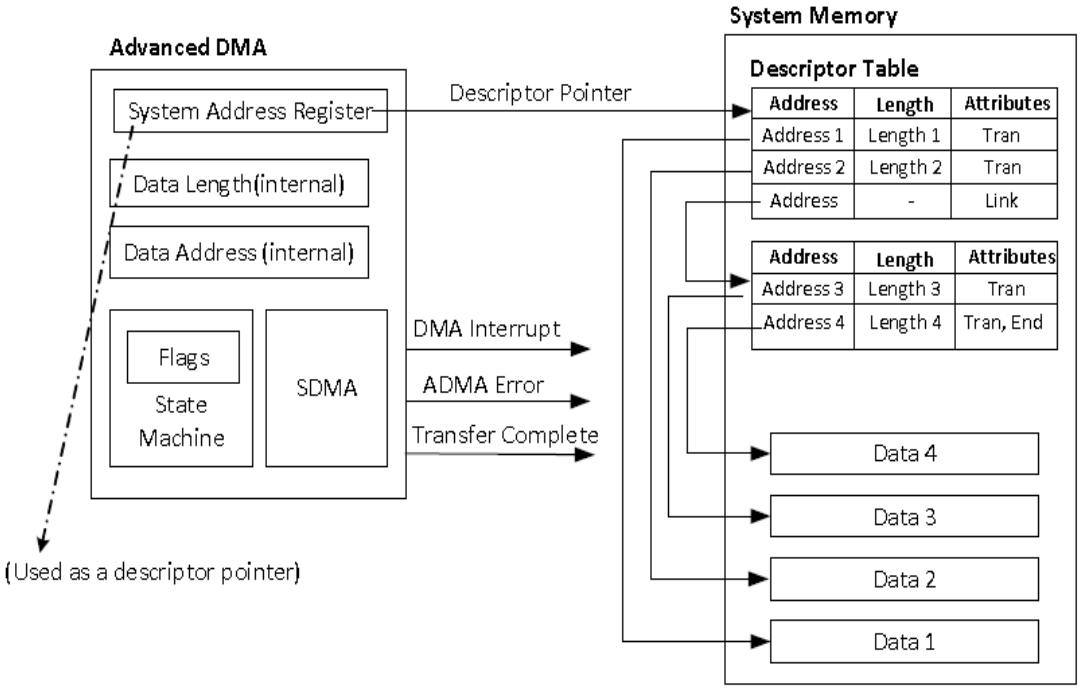


Figure 32-3 ADMA2 Block Diagram

The descriptor table is created in the system memory by the Host driver. ADMA2 fetches one descriptor line and executes it until the end of descriptor denoted by (End = 1 in attribute) is found.

Figure 32-4 shows the ADMA2 descriptor format.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

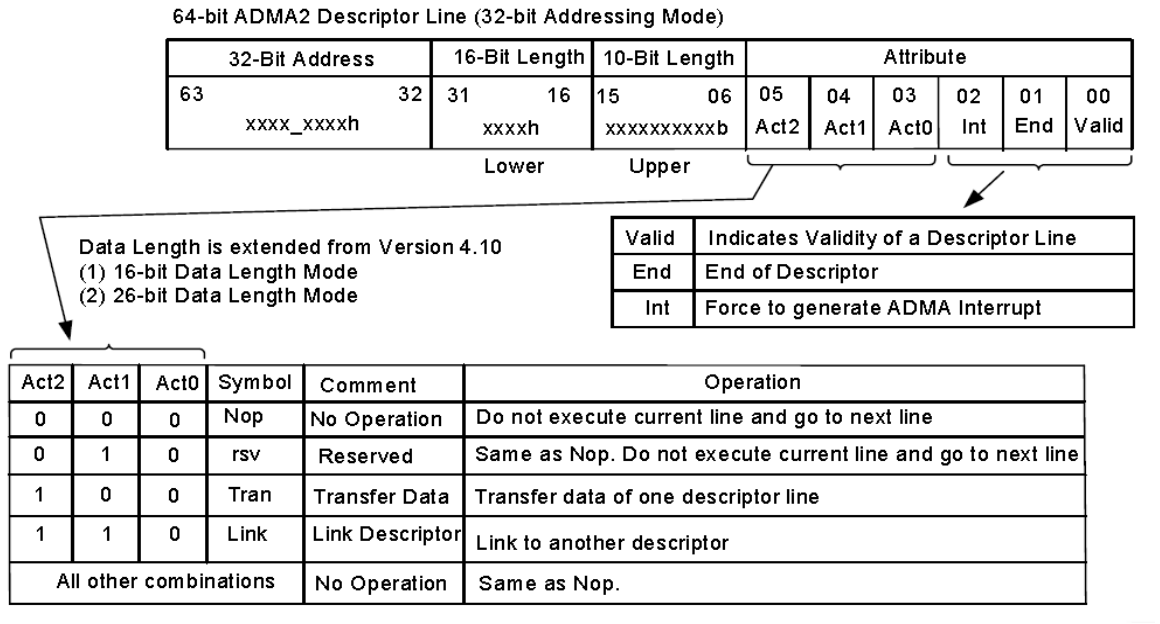


Figure 32-4 ADMA2 Descriptor Table

32.6.2 ADMA3 Operation

ADMA3 can be considered as multiple ADMA2 operations. This is achieved by using an integrated descriptor structure which in turn consists of a pair of Command Descriptor and ADMA2 descriptor. This pair is programmed for a multi-block data transfer from the system memory to the SD card. In ADMA2, the host driver issues an SD command using the Host Control registers, whereas ADMA3 uses the Command Descriptors to issue an SD command. The different command descriptor types available in Msc are SD command descriptor types.

shows a sample ADMA3 data transfer to write three data blocks (Data A, Data B, and Data C) to different areas of an SD card.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

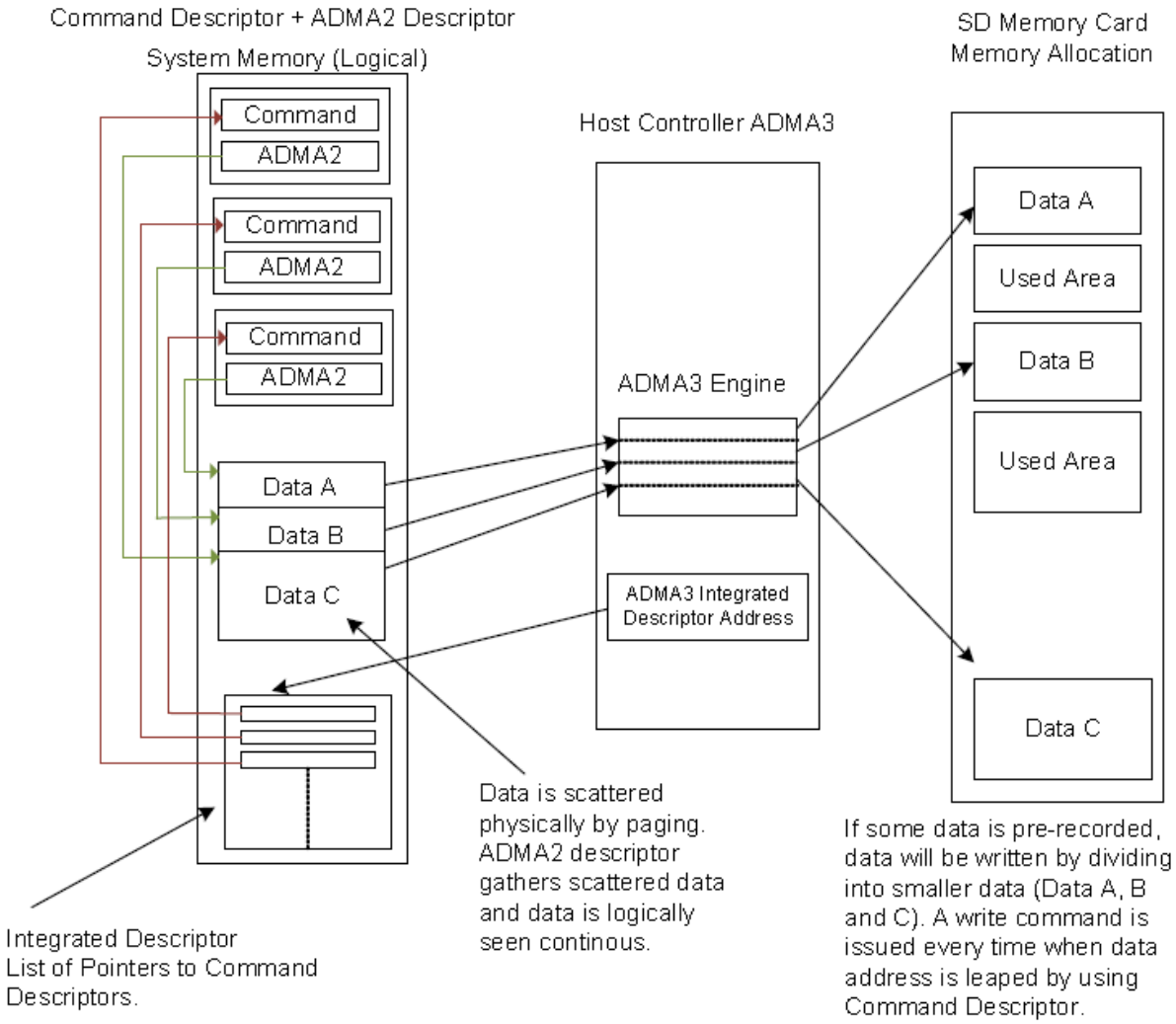


Figure 32-5 ADMA3 Integrated Descriptor Pair(Command Descriptor + ADMA2 Descriptor)

system memory to the SD memory card. Similarly, the second pair is programmed to transfer Data B, and the third pair is programmed to transfer Data C. After processing all descriptors pointed by the integrated descriptors are completed, ADMA3 generates the Transfer Complete interrupt to indicate completion of data transfer to the host driver.

Figure 32-6 shows the ADMA3 command descriptor format, 32-bit register fields are written to the host controller registers from 000h to 00Fh. An SD command is issued when 00Fh is written.

The host controller register contains a pointer to a descriptor line for the command descriptor and ADMA2 descriptor. This pointer is incremented after reading each descriptor line. When the last line in the command descriptor is read, the pointer points to the top of the ADMA2 descriptor, which is placed after the command

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

descriptor.

Command Descriptor (for 32-bit/64-bit Addressing Mode)

32-bit Register	Reserved	Reserved	Attribute					
63 32	31 16	15 06	05	04	03	02	01	00
xxxx_xxxxh	0000h	000000b	Act2	Act1	Act0	Int	End	Valid

32-bit register fields are written to the Host Control Registers from 000h to 00Fh to issue an SD command.

(1) Command Descriptor for SD Mode

32-Bit Address	Reserved	Attribute	
32-bit Block Count	All 0	001001b	→ Set to 003h – 000h
(16-bit Block Count) + Block Size	All 0	001001b	→ Set to 007h – 004h
Argument	All 0	001001b	→ Set to 00Bh – 008h
Command + Transfer Mode	All 0	001011b	→ Set to 00Fh – 00Ch

Figure 32-6 ADMA3 Command Descriptor Format

Figure 32-7 shows the ADMA3 integrated descriptor format. Each row in the integrated descriptor table. The pointer of 32-bit address is set to bit 63-32 in the 64-bit Integrated Descriptor and the controller ignores "Int" of attribute in this descriptor.

64-bit Integrated Descriptor (32-bit Addressing)

32-bit Pointer	Reserved	Reserved	Attribute					
63 32	31 16	15 06	05	04	03	02	01	00
xxxx_xxxxh	0000h	000000b	Act2	Act1	Act0	Int	End	Valid

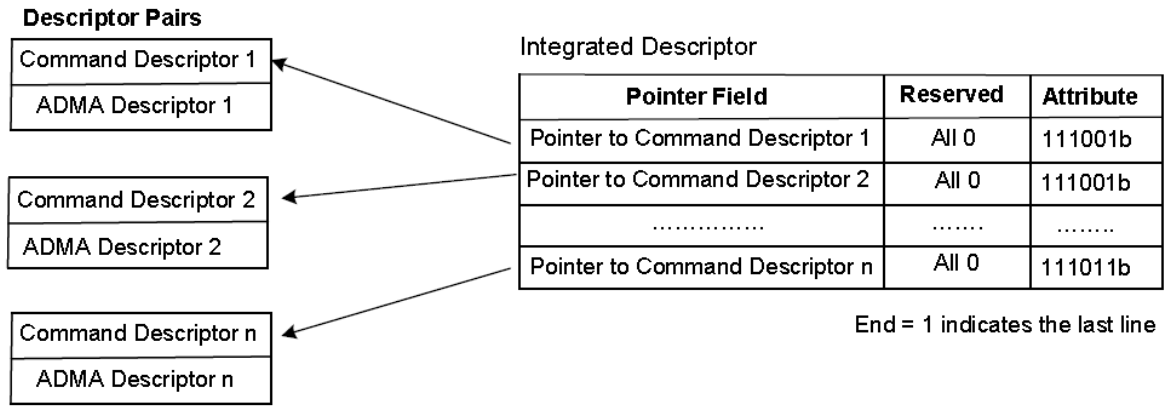


Figure 32-7 ADMA3 Integrated Descriptor Format

For more information about these descriptor formats, see *SD Specifications Part A2 SD*

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Host Controller Standard Specification Version 4.10, Sep 2013.

32.6.3 Command Queueing Task Descriptor

The Command Queueing Engine (CQE) denotes the hardware unit executing the Command Queueing (CQ) activities. The CEQ manages the interface between the host software and the eMMC device, and the data transfers. CQE receives tasks from the software though a Task Descriptor List (TDL) in the host memory and the doorbell register. The CQE issues CQ commands, CMD44 and CMD45, to the eMMC device and also stores the task information. CQE also reads the queue status register of the device and decides the task to execute, and issues the EXECUTE commands

In order to implement queueing of tasks in the eMMC device, the host asynchronously issues tasks using the TDL, which is located in a memory location known to the CQE, and contains up to 32 fixed-size slots. Each slot contains one Task Descriptor and one Transfer Descriptor. To issue a task, the software selects an available TDL slot and constructs the following two descriptors in it:

- Task Descriptor – This encodes all information that defines the Task. For instance, the Address, Block Count, and Priority. This information is later passed to the device. The Task Descriptor can alternatively encode any arbitrary command that is sent directly to the device.
- Transfer Descriptor – This points either to one continuous data buffer to/from which data is transferred (TRAN Descriptor) or to a scatter/gather list of any length (LINK Descriptor).

Figure 32-8 shows the structure of the TDL in the host memory and the slot numbers in the TDL. The slot numbers in Figure 32-8 store the following information:

0 – Stores a Data Transfer Task with a TRAN descriptor.

1 – Stores a Data Transfer Task with a LINK descriptor, pointing to a scatter/gather list.

31 – Stores a DCMD descriptor.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

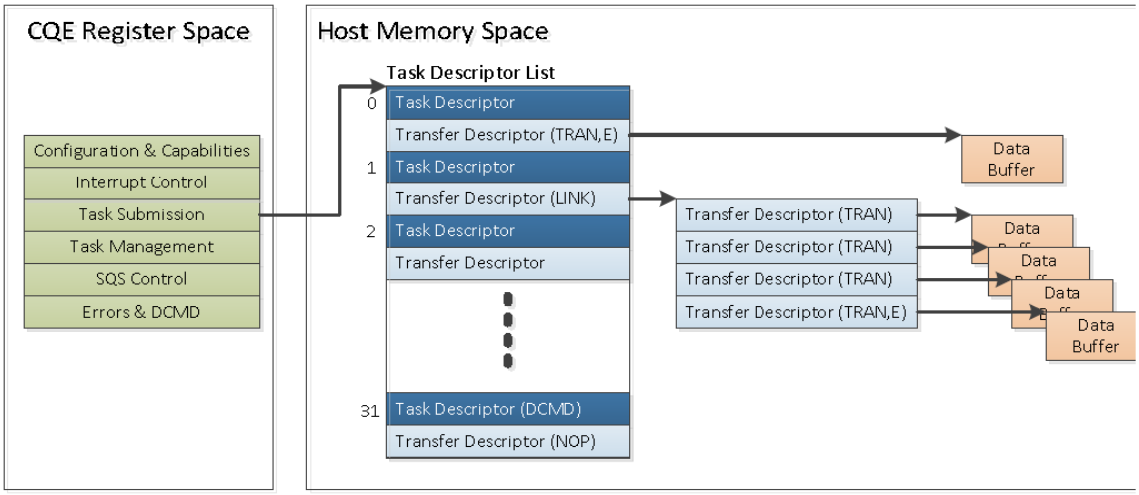


Figure 32-8 Command Queuing Host Controller Interface (HCI) Structure

32.6.4 eMMC Data Structures

This section describes the descriptor structures used in eMMC Command Queuing. As mentioned in "Command Queueing Task Descriptor", the host writes a pair of descriptors namely Task Descriptor and Transfer Descriptor, which are organized in the host memory in the Task Descriptor List.

This section discusses the following structures:

- "Task Descriptor Structure"
- "Transfer Descriptor Structure"
- "Task Descriptor for Direct-Command (DCMD) Tasks"

32.6.4.1Task Descriptor Structure

Table 32-4 summarize the Task Descriptor structure, and Table 32-5 describes task descriptor fields

Table 32-4 Task Descriptor Structure; Lower 64 bits (Data Transfer tasks)

Block Address	Block Count	Task Parameters Field							Attribute			
63:32	31:16	15	14	13	12	11	10:7	6	5:3	2	1	0
xxxx_xxxxh	xxxxh	Reliable Write	QBR	Priority	Data Direction	Tag request	Context	Forced program	Act=101	Int	End=1	Valid=1

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Table 32-5 Task Descriptor Fields

Field Name	Bit Location	Description	Encoded in CMD
Valid	0	1 – The descriptor is effective and must be processed by hardware. 0 – The descriptor line must not be used.	
End	1	Must always be set to 1. Every Task Descriptor is standalone.	
Int	2	Indicates the interrupt generation policy required for this task. 1 – Hardware generates an interrupt upon the task completion. 0 – Hardware counts task completion for interrupt coalescing.	
Act	5:3	Must be set to b101 to indicate that this is a Task Descriptor.	
Forced Programming (FP)	6	If 1, FP is enabled. Data is forcefully programmed to a non-volatile storage instead of volatile cache while cache is turned ON	CMD44
Context ID	10:7	A context is an active session, configured for a specific read/write pattern. A device may support one or more concurrent contexts, defined by a Context ID. Each context ID	CMD44
Tag Request	11	Indicates request to receive information (about specific data types) from the host.	CMD44
Data Direction	12	Indicates the direction of data transfer. 1 – Device to Host (Read) 0 – Host to Device (Write)	CMD44
Priority	13	1 – high 0 – simple	CMD44
Queue Barrier (QBR)	14	Indicates the control of the host on the ordering between tasks.	
Reliable Write	15	Indicates multiple block write with pre-defined block count and Reliable	CMD44
Block Count	31:16	Number of blocks to be read/written.	CMD44
Block Address	63:32	Data block address	CMD45

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.6.4.2Transfer Descriptor Structure

Table 32-6 summarize the Transfer Descriptor structure for 32-bit addressing. Table 32-7 describes transfer descriptor fields.

Table 32-6 Transfer Descriptor Structure (32-Bit Addressing)

Address	Length	Rsvd	Attribute			
63:32	31:16	15 6	5:3	2	1	0
xxxx_xxxxh	xxxxh	0000000	Act	Int	End	Valid

Table 32-7 Transfer Descriptor Fields

Field Name	Bit Location	Description
Valid	0	1 – The descriptor is effective and must be processed by hardware. 0 – The descriptor line must not be used.
End	1	1 – The descriptor is the last descriptor in a descriptor list. 0 – Additional descriptors follow this descriptor. In the case of a TRAN descriptor, the value of this bit is 1.
Int	2	The value of this bit is set to 0 in command queuing.
Act	5:3	100: TRAN – Address field of descriptor points to a data buffer. 110: LINK – Address field of descriptor points to a another descriptor. 000: NOP – no operation.
Reserved	15:6	Reserved
Length	31:16	Length of data buffer in bytes. A value of 0000 means 64 KB.
Address (32-bit)	63:32	Data buffer address in host memory, in 32-bit addressing mode. Address must be set on 32-bit boundary (Lower 2 bits set to 0)
Address (64-bit)	95:32	Data buffer address in host memory, in 64-bit addressing mode. Address must be set on 64-bit boundary (Lower 3 bits set to 0)

32.6.4.3Task Descriptor for Direct-Command (DCMD) Tasks

Table 32-8 summarizes the Transfer Descriptor structure for the lower 64 bits for DCMD tasks and
Table 32-9 describes transfer descriptor fields.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Table 32-8 Task Descriptor Structure: Lower 64 bits (for Direct-Command (DCMD) tasks)

Command Argument	Command Parameters				Task Parameters Field			Attribute			
63:32	31 25	24 23	22	21 16	15	14	13 6	5 3	2	1	0
xxxx_xxxxh	Reserved (0000000)	Response Type	CMD timing	CMD Index	Rsvd (0)	QBR	Reserved (0000000)	Act=101	Int	End=1	Valid =1

Table 32-9 Transfer Descriptor Fields

Field Name	Bit Location	Description
Valid	0	1 – The descriptor is effective and must be processed by hardware. 0 – The descriptor line must not be used.
End	1	Must always be set to 1. Every Task Descriptor is standalone.
Int	2	Indicates the interrupt generation policy required for this task. 1 – Hardware generates an interrupt upon the task completion. 0 – Hardware does not generate an interrupt upon the task completion.
Act	5:3	Shall be set to b101 to indicate that this is a Task Descriptor.
Reserved	13:6	Reserved
Queue Barrier (QBR)	14	Indicates the control of the host on the ordering between tasks.
Reserved	15	
CMD Index	21:16	The index of the command to be sent to the device.
CMD Timing	22	1 – Command may be sent to device during data activity or busy time. 0 – Command may not be sent to device during data activity or busy time.
Response Type	24:23	This field indicates to the host controller the response expected to be received from the device. b00 – No Response Expected b01 – Reserved b10 – R1, R4, R5 b11 – R1b
Reserved	31:25	
CMD Argument	63:32	The argument of the command to be sent to the device.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.7 SDIO Read Wait

A host device controls the SDCLK (card clock) to stop the read data block output from a card executing a multiple read commands when the host cannot accept more data. The duration of time when the host has stopped the SDCLK, a CMD52 cannot be issued. This limitation causes a problem in that a host device cannot perform the I/O command during a multiple read cycle.

In order to overcome this limitation, Msc supports the read wait feature to signal a card that is executing multiple read (CMD53) operations to temporarily pause data transfer while allowing the host to send commands to any other function within the card. The read wait function is optional for SDIO cards.

If the card supports read wait, then the Msc controller can stall the read data from the card by issuing read wait using the sd_dat_out[2] line at the block boundary instead of stopping the card clock. The Msc controller asserts read wait during the NAC period of the data block if:

- The controller is configured to stop at block gap and read wait is enabled.
- If the packet buffer of the controller does not have sufficient space to contain the next block of data and if read wait is enabled.

While the read wait feature is optional for SDIO cards. This feature is defined only for the SD 1 and 4-bit modes, and it does not apply to SPI transfers.

32.8 SDIO Card Interrupt

An SD interface supports the interrupt function to allow an SDIO card to interrupt the host. An SDIO card provides level-sensitive interrupt Msc using the sd_dat_in[1] Interrupt Input in SD mode. This interrupt is used to inform the host about error status and also about normal information, such as function ready. This interrupt is also used as a source of wakeup event to inform the host to resume from standby mode. The card interrupt is cleared when the card/device stops asserting the interrupt, that is, when the application services the interrupt condition.

For SD 1-bit mode, there are no timing constraints for interrupt.

For 4-bit mode, the Msc samples the card interrupt only during the interrupt period that is defined as follows:

- Interrupt period ends from the end bit of a command that transfers the data block (1 to 3 clocks for SDR50, SDR104, and DDR50 modes).
- Resume two clocks after the completion of last data block transfer (2 to 4 for SDR50, SDR104, and DDR50 modes)

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

- Within the data block gap, 2-clock Interrupt period begins 2 clocks after the end bit of data blocks (Block Gap card interrupt is disabled in SDR50, SDR104, and DDR 50 as recommended by the device specification)
- While the specification defines that the asynchronous interrupt period starts 4 clocks from the start of synchronous interrupt period and ends 1 to 3 clocks from the beginning of end bit of data command, the Msc does not distinguish between synchronous and asynchronous interrupt periods.
- In case of abort CMD, the interrupt period ends 2 clocks after the end bit of abort CMD and resumes 2 clocks after the end bit of the response

An asynchronous interrupt is effective in SD 4-bit mode. The asynchronous interrupt generated from the device while the card clock is stopped to save the power is dehvered to the host system

32.9 Operation Flow

This chapter discusses the following sections:

- "Overview"
- "Host Controller Setup Sequence"
- "Clock Control"
- "Card Interface Setup Sequence"
- "Timeout Setting"
- "Abort Transaction"
- "SD/SDIO Transaction Mode"
- "eMMC Transaction Mode"
- "Error Recovery"

32.9.1 Overview

This section explains the programming steps required for Msc and the card subsystem before starting data transfer with a connected card. Initially, both the host controller and the card needs to be initialized.

Following is the programming sequence required before starting the data transfer with the card:

1. Setup basic settings for Msc controller as described in "Host Controller Setup Sequence". Different setup sequences for SD card ("SD Interface") and eMMC card ("eMMC Device") are provided.
2. Enable input clocks that are available in Msc. Internal clocks (aclk, bclk, tmclk and cqetmclk) are enabled followed by the card clocks (cclk_tx/cclk_rx) as discussed in the programming sequence in "Host Controller Clock Setup Sequence". At this stage, Msc is ready to communicate with the card.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

3. Executing the programming sequence described in "Card Interface Setup", provide clock to the card.
4. Appropriate sequence as shown in Table 32-10 must to be executed based on type of the connected card.

Table 32-10 Card Initialization Sequence for Different Cards

Type of Card	Card Initialization Sequences
SD	SD Card Initialization and Identification ("SD Card Initialization and Identification")
eMMC	Initializing and Identifying an eMMC Card ("Initializing and Identifying an eMMC Device")

5. As both host controller and card are initialized, the host can start sending commands to the card to perform the data transfer. Control and data commands are two types of commands that can be issued to the card. The control command is used to read or write any register in the card. The data command is used for writing or reading data to or from the card. Table 32-11 lists the control and data command sequences for SD, eMMC cards.

Table 32-11 Command Sequence for Different Cards

Type of Card	Command Sequence	
SD/eMMC	Control CMD	Issuing CMD without Data Transfer ("Issuing CMD without Data Transfer")
	Data CMD	Issuing CMD with Data Transfer ("Issuing CMD with Data Transfer")

a. Data transfer can be aborted using Abort command ("Abort Command Sequence").
b. If errors are detected during the transfer, recovery should be done using sequence described in "Error Recovery".

32.9.2 Host Controller Setup Sequence

This section discusses the host controller setup sequence for SD interfaces, and an eMMC device.

This section discusses the following sequences:

- "SD Interface"
- "eMMC Device"

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.9.2.1 SD Interface

Figure 32-9 shows the host controller setup sequence. The register parameters set in this sequence retain their values irrespective of bus speed mode changes.

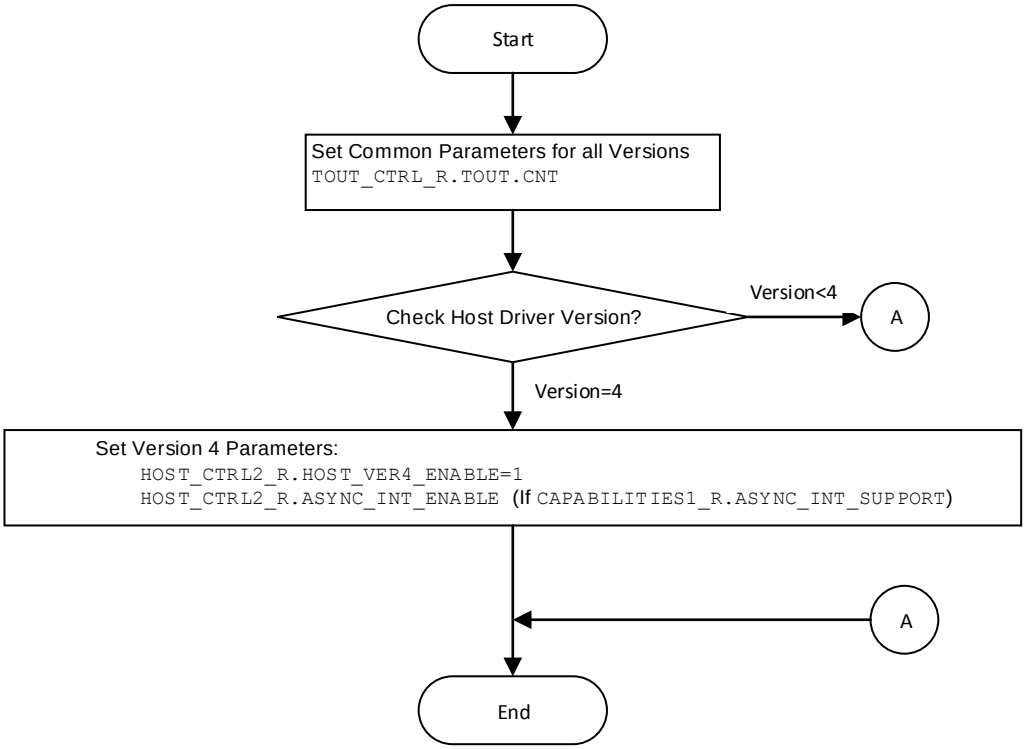


Figure 32-9 Host Controller Setup Sequence for SD

32.9.2.2 eMMC Device

Figure 32-10 shows the host controller setup sequence for an eMMC device. In addition to completing the programming sequence in Figure 32-10, you must set the parameter EMMC_CRTL_R.CARD_IS_EMMC = 1.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

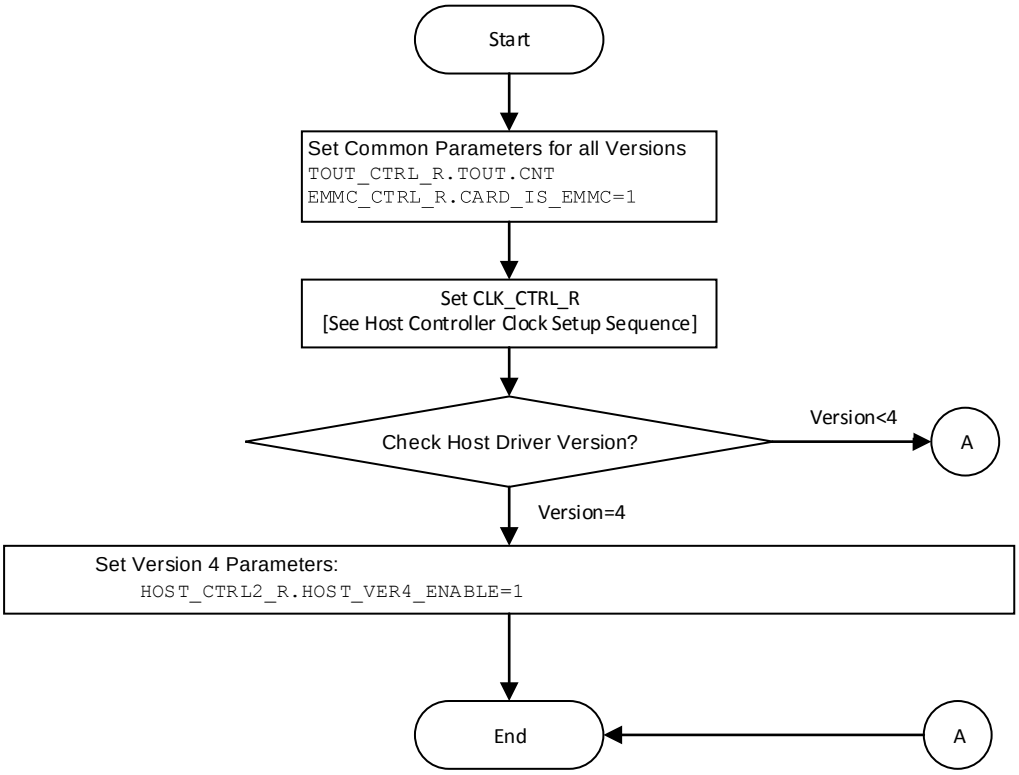


Figure 32-10 Host Controller Setup Sequence for eMMC Interface

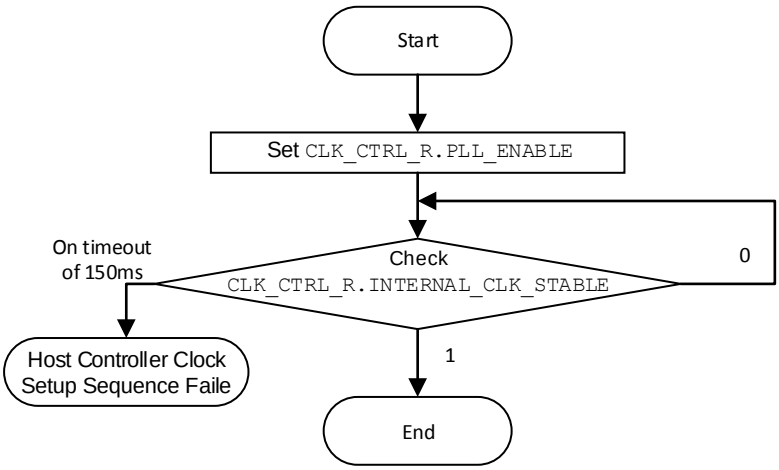
32.9.3 Clock Control

This section discusses the programming sequence for setting up internal clocks and card clock provided Msc and for supplying and setting up a clock provided to the card.

This section includes the following sequences:

- "Host Controller Clock Setup Sequence"
- "Card Clock Supply and Stop Sequence"

32.9.3.1 Host Controller Clock Setup Sequence



Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 32-11 Host Controller Clock Supply Sequence

32.9.3.2 Card Clock Supply and Stop Sequence



Figure 32-12 Card Clock Supply and Stop Sequence

32.9.4 Card Interface Setup Sequence

This section discusses the programming sequence for setting up the card interface for an SD, eMMC cards.

This section discusses the following topics:

- "Card Interface Setup"

32.9.4.1 Card Interface Setup

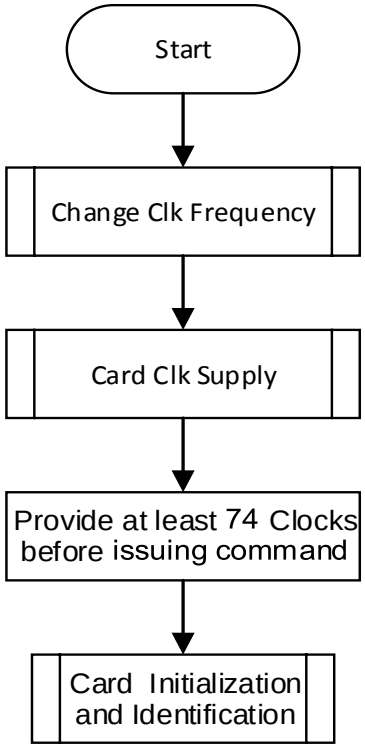


Figure 32-13 Card Interface Setup Sequence

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.9.5 Timeout Setting

This section discusses the timeout setting on the SD, eMMC data lines.

This section discusses the following sequences:

- "Timeout Setting for an SD/eMMC Bus"

32.9.5.1 Timeout Setting for an SD/eMMC Bus

Figure 32-14 shows the timeout setting for an SD/eMMC bus.

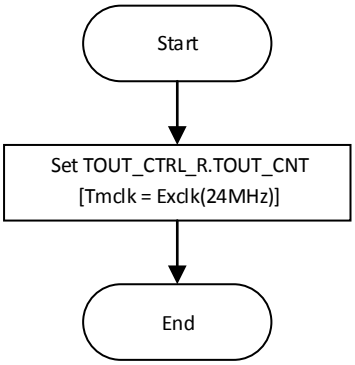


Figure 32-14 SD/eMMC Bus Timeout Setting

32.9.6 Abort Transaction

An abort command to the card is issued to abort an ongoing data transaction. To abort a transaction on an SD/eMMC card, CMD12 is issued, whereas to abort a transaction on an SDIO card, CMD52 is issued.

Following are the instances when an abort command must be issued:

- To stop an infinite block transfer
- To stop transfer due to a request from an application
- To stop a transfer due to an error detection

The sequence to issue an abort command is shown in "Abort Command Sequence". An abort command can be issued synchronously or asynchronously during data transfer. In asynchronous abort, abort command is issued at any time irrespective of the state of data transfer as a subcommand. Synchronous abort ensures that the data transfer is stopped (at block gap) before issuing an abort command. Both methods are explained in "Asynchronous Abort" and "Synchronous Abort" respectively

This section discusses the following sequences:

- "Abort Command Sequence"
- "Asynchronous Abort"
- "Synchronous Abort"

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.9.6.1 Abort Command Sequence

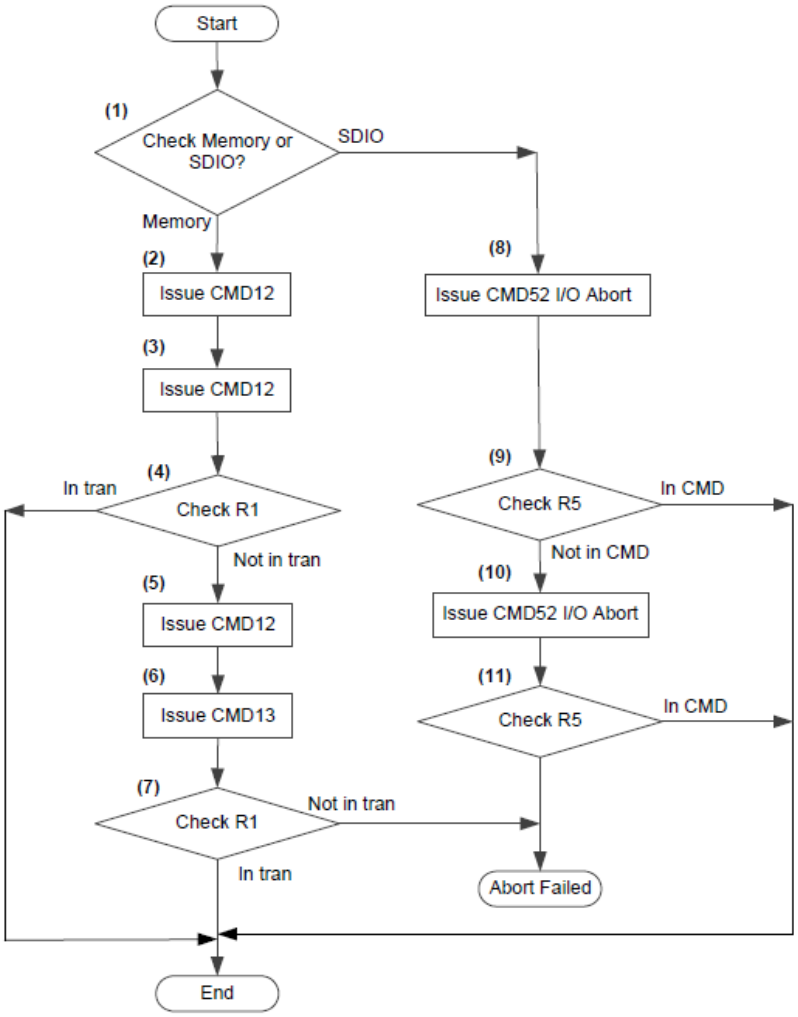


Figure 32-15 Abort Command Sequence

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.9.6.2 Asynchronous Abort

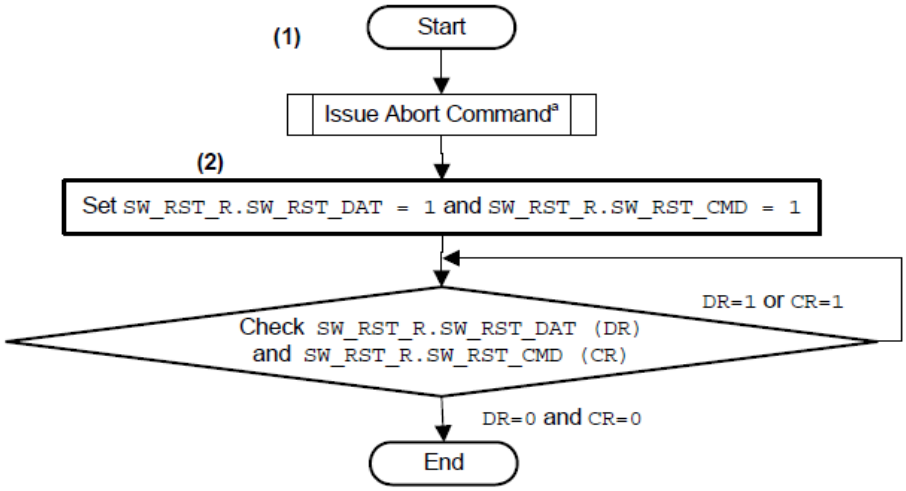


Figure 32-16 Asynchronous Abort Sequence

32.9.6.3 Synchronous Abort

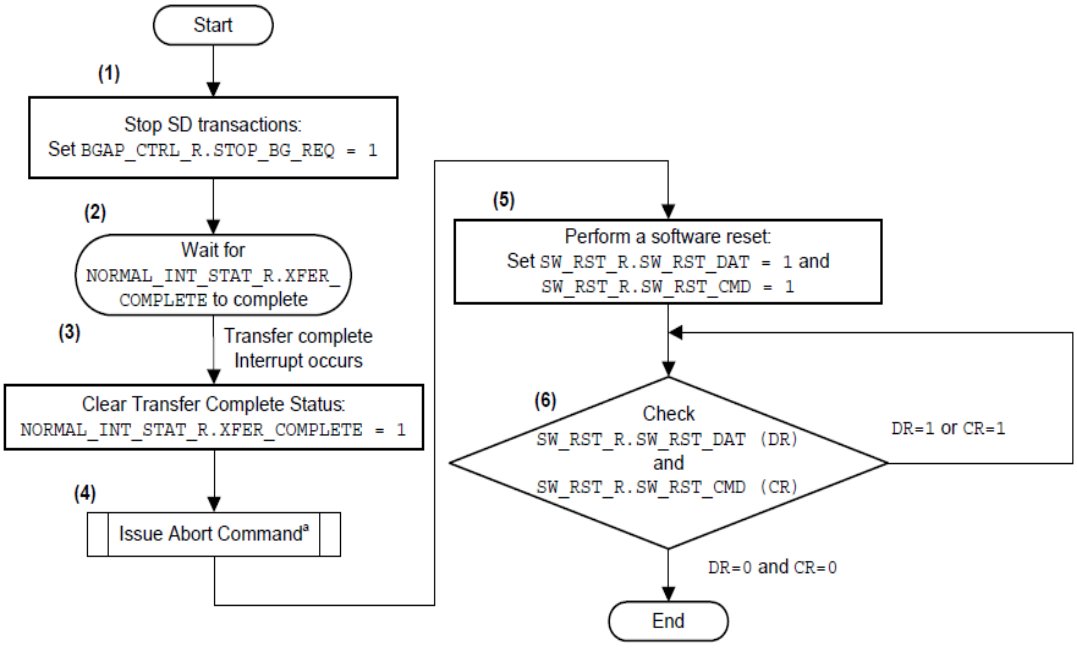


Figure 32-17 Synchronous Abort Sequence

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.9.7 SD/SDIO Transaction Mode

This section includes the sequences to generate and control different types of SD/SDIO transactions that can be classified as transactions without data transfer using the DAT line and transactions with data transfer using the DAT line. This section also discusses the sequence for tuning the flow, changing the bus width and speed mode, setting the timeout on a DAT line, initializing and identifying an SD card, and the aborting sequence.

This section discusses the following programming sequences:

- "SD Card Initialization and Identification"
- "SD Changing Bus Width"
- "SD Mode Tuning Flow Sequence"
- "Issuing CMD without Data Transfer"
- "Issuing CMD with Data Transfer"
- "SD Changing Bus Speed Mode"

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.9.7.1 SD Card Initialization and Identification

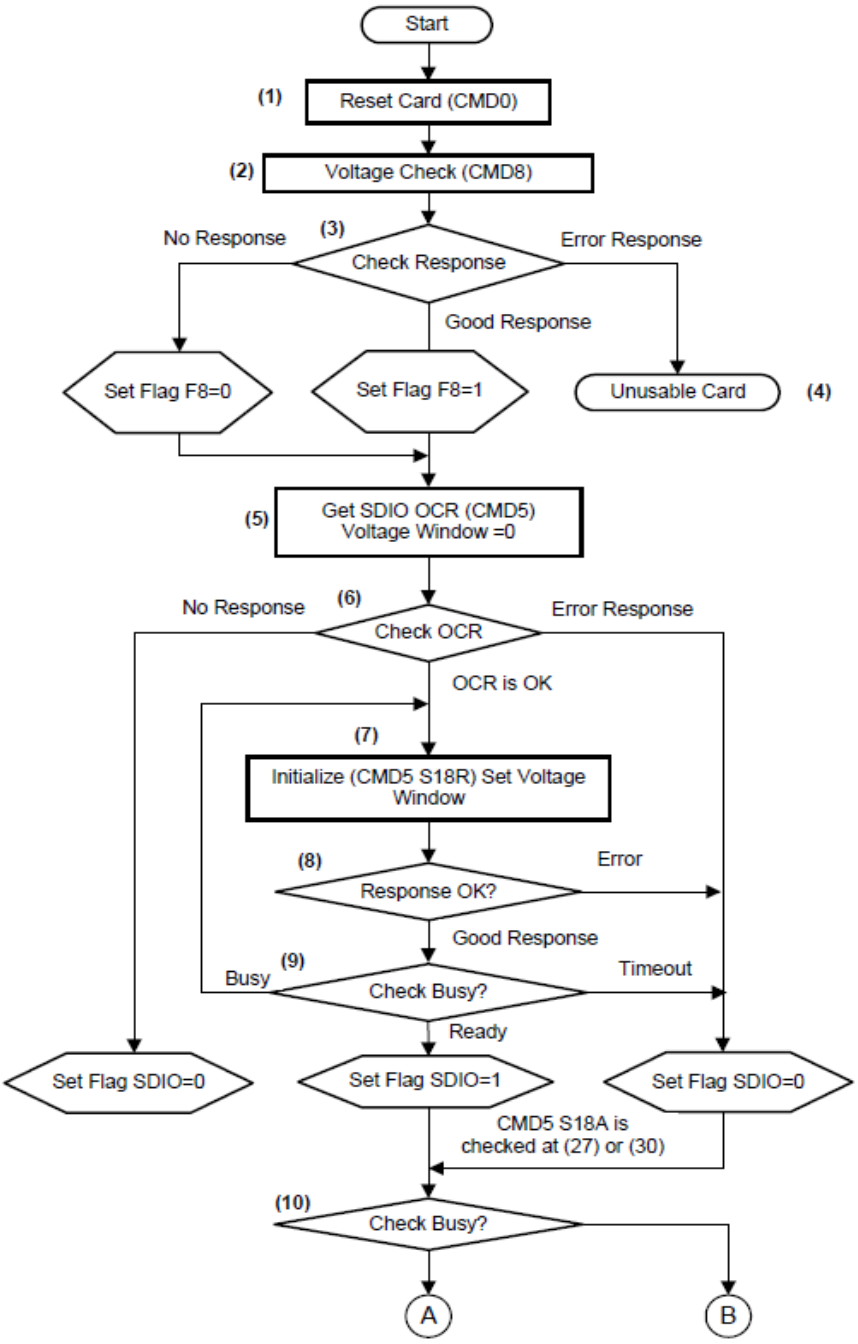


Figure 32-18 SD Card Initialization and Identification

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

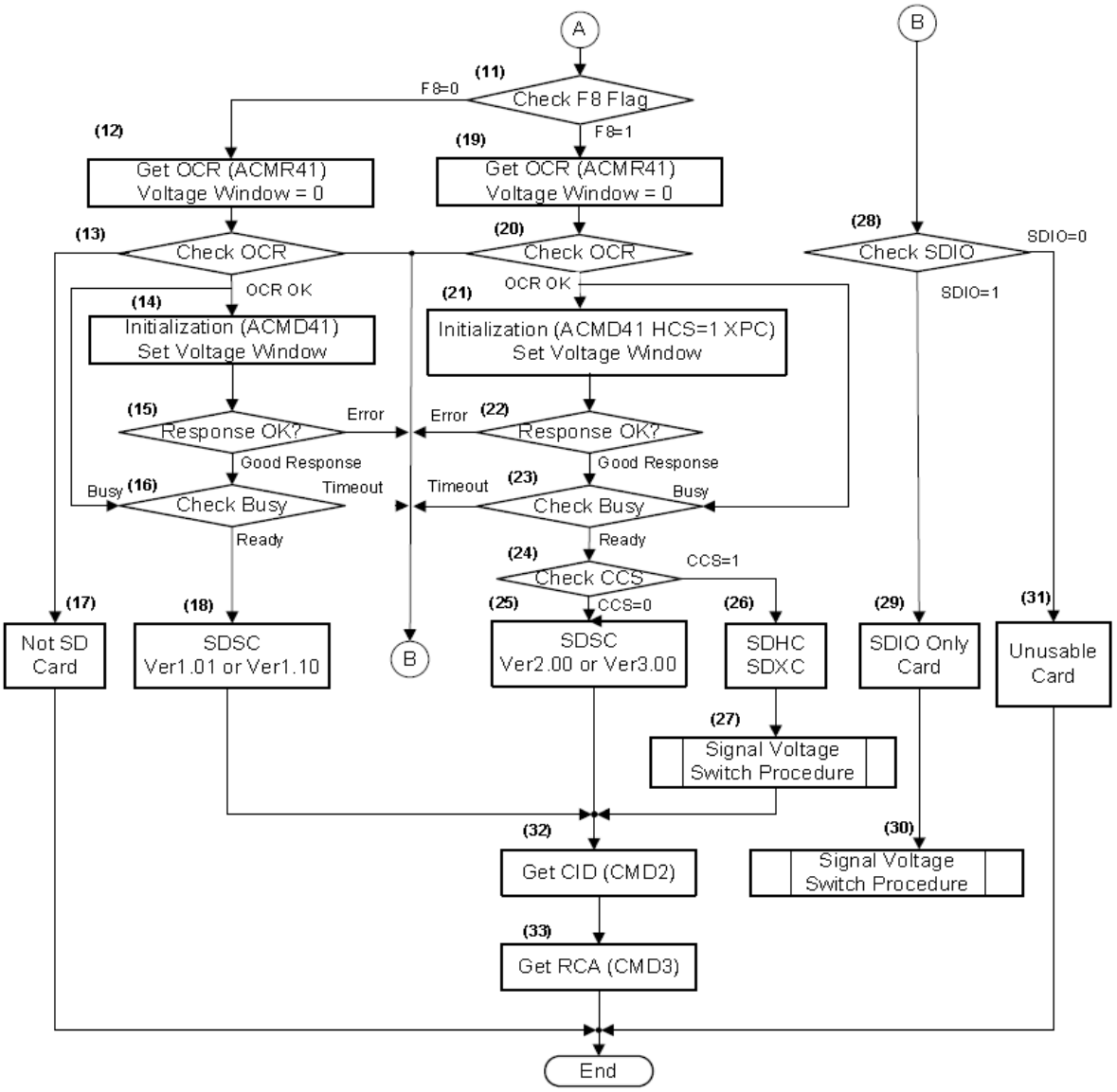


Figure 32-19 SD Card Initialization and Identification (contd)

32.9.7.2 SD Changing Bus Width

Figure 32-20 shows the sequence for changing bit mode on SD Bus

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

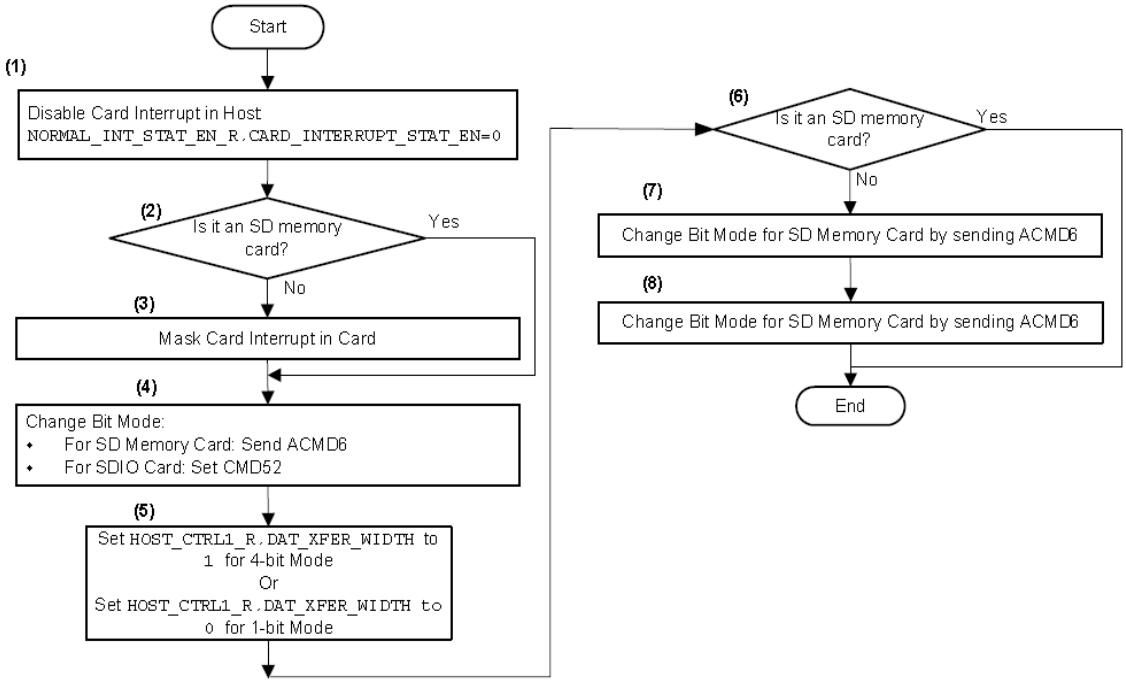


Figure 32-20 Change Bus Width Sequence

32.9.7.3 SD Mode Tuning Flow Sequence

Figure 32-21 shows how to perform tuning in an SD mode.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

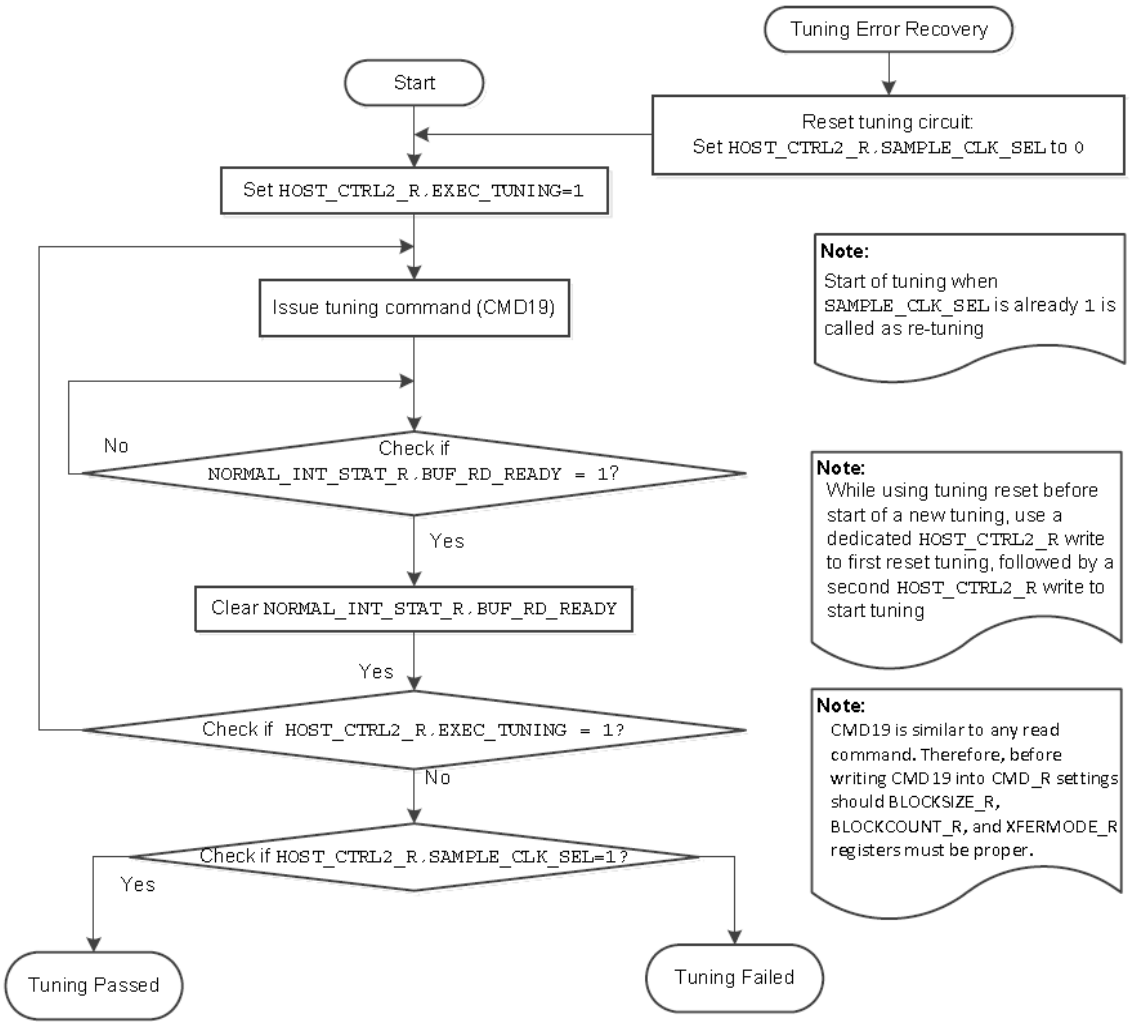


Figure 32-21 Tuning Sequence

32.9.7.4 Issuing CMD without Data Transfer

Figure 32-22 shows the sequence on how to issue and complete an SD command. An SD command may or may not use a data line (DAT) (which is used for busy signaling).

Figure 32-22 shows the procedure to issue commands for both scenarios.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

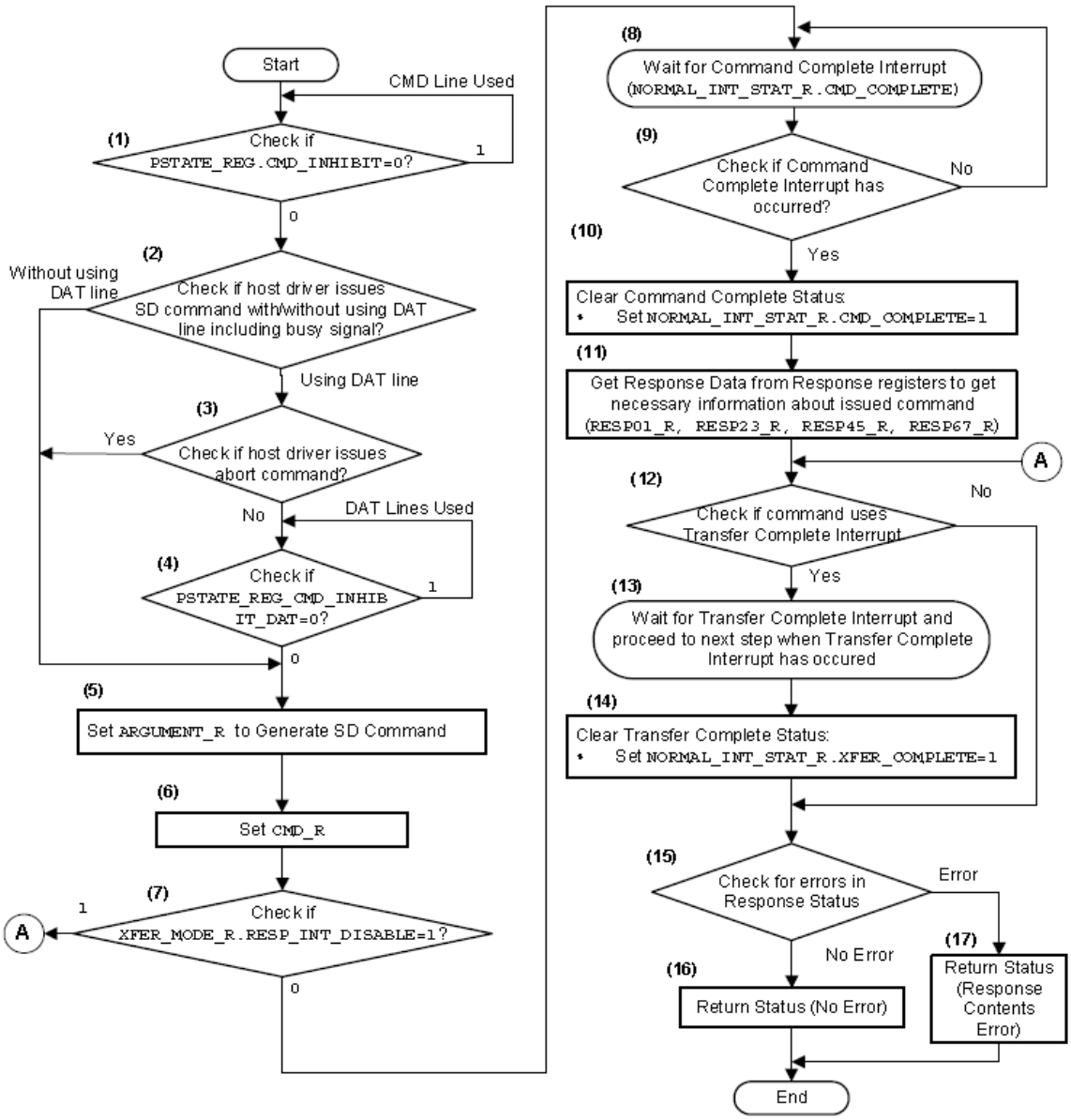


Figure 32-22 SD Command Issue and Complete

32.9.7.5 Issuing CMD with Data Transfer

This section includes the sequence to issues a command with data transfer without using DMA and by using SDMA, ADMA, and ADMA3 modes.

This section discusses the following programming sequences:

- "Issuing CMD with Data Transfer (Not Using DMA/PIO)"
- "Issuing CMD with Data Transfer (Using SDMA)"
- "Issuing CMD with Data Transfer (Using ADMA2)"
- "Issuing CMD with Data Transfer (Using ADMA3)"

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.9.7.5.1 Issuing CMD with Data Transfer (Not Using DMA/PIO)

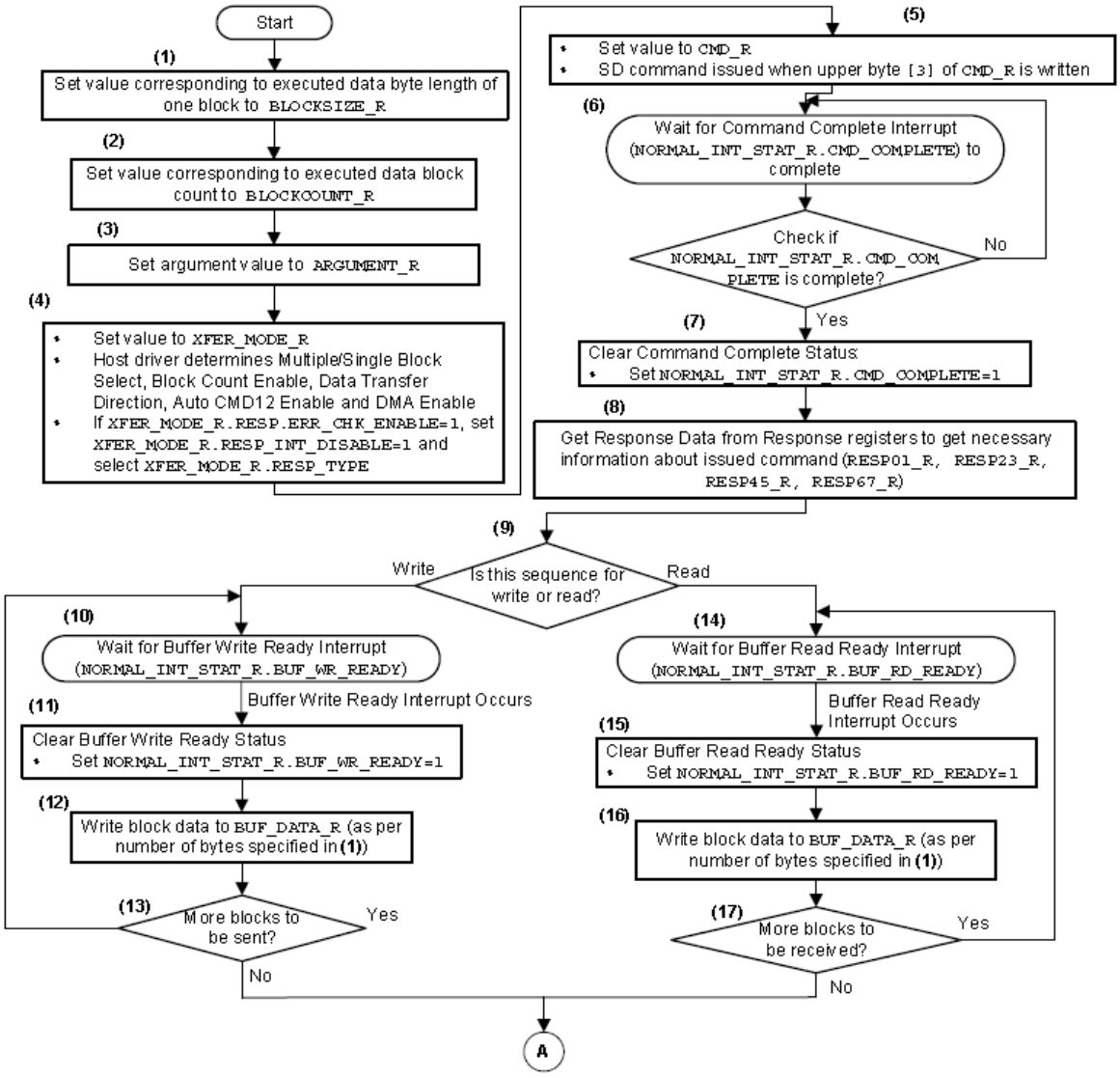


Figure 32-23 Transaction Not Using DMA for Data Transfer

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

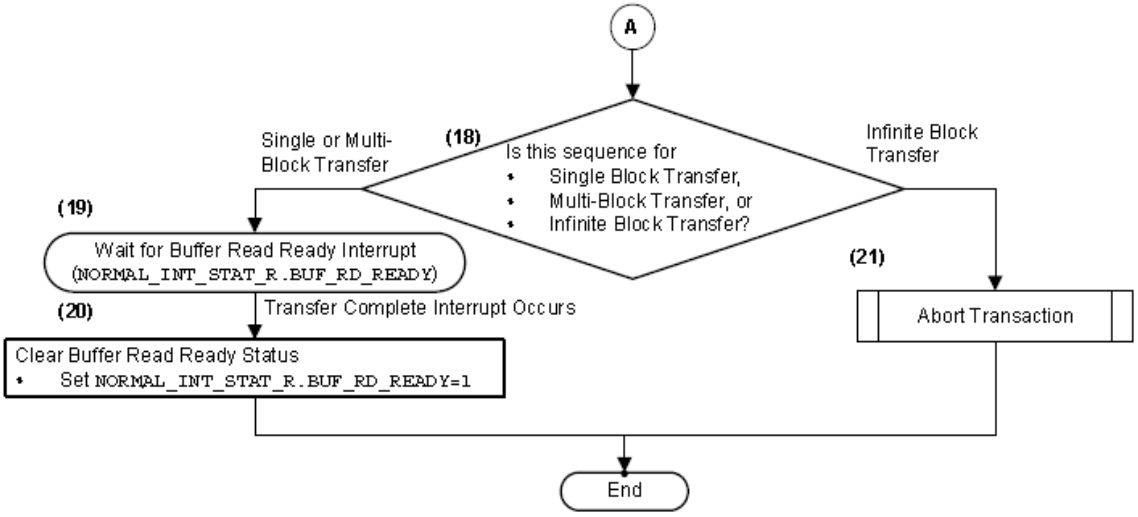


Figure 32-24 Transaction Control with Data Transfer Using DAT Line (Not Using DMA)

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.9.7.5.2 Issuing CMD with Data Transfer (Using SDMA)

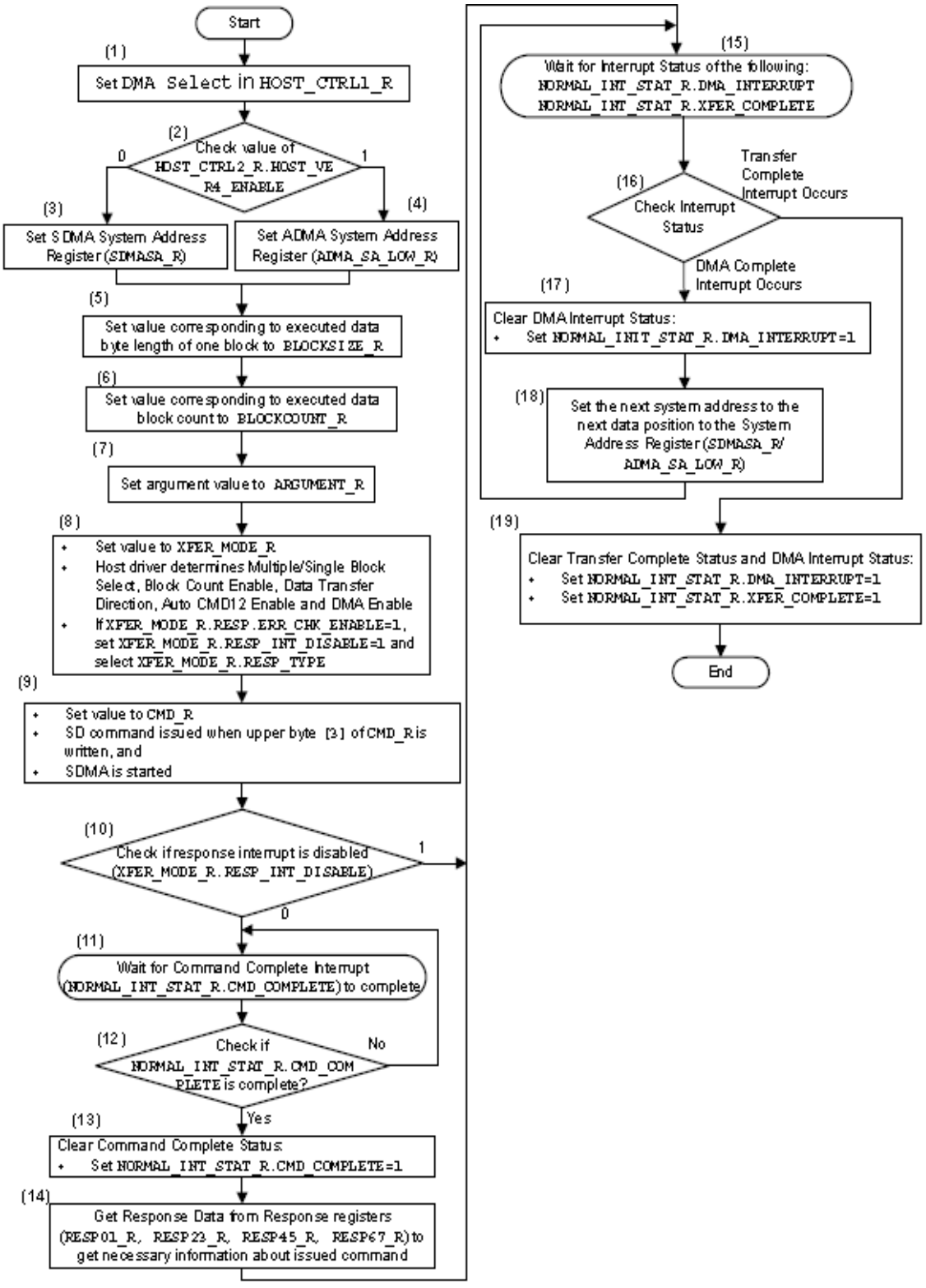


Figure 32-25 Transaction Using SDMA for Data Transfer

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.9.7.5.3 Issuing CMD with Data Transfer (Using ADMA2)

Figure 32-26 and Figure 32-27 show the transaction that uses ADMA2 for data transfer using the DAT line.

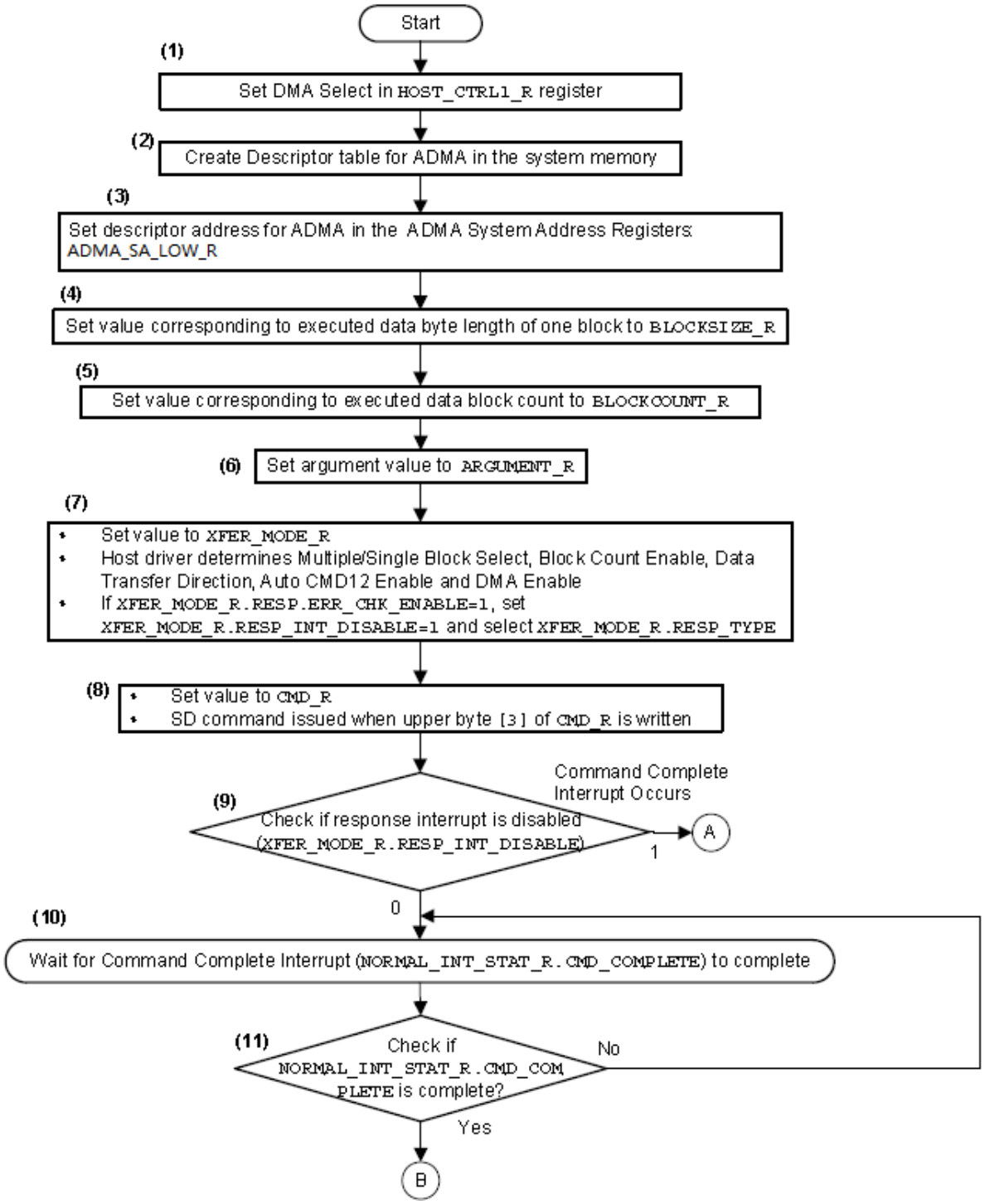


Figure 32-26 Transaction Control with Data Transfer Using DAT Line (Using ADMA2)

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

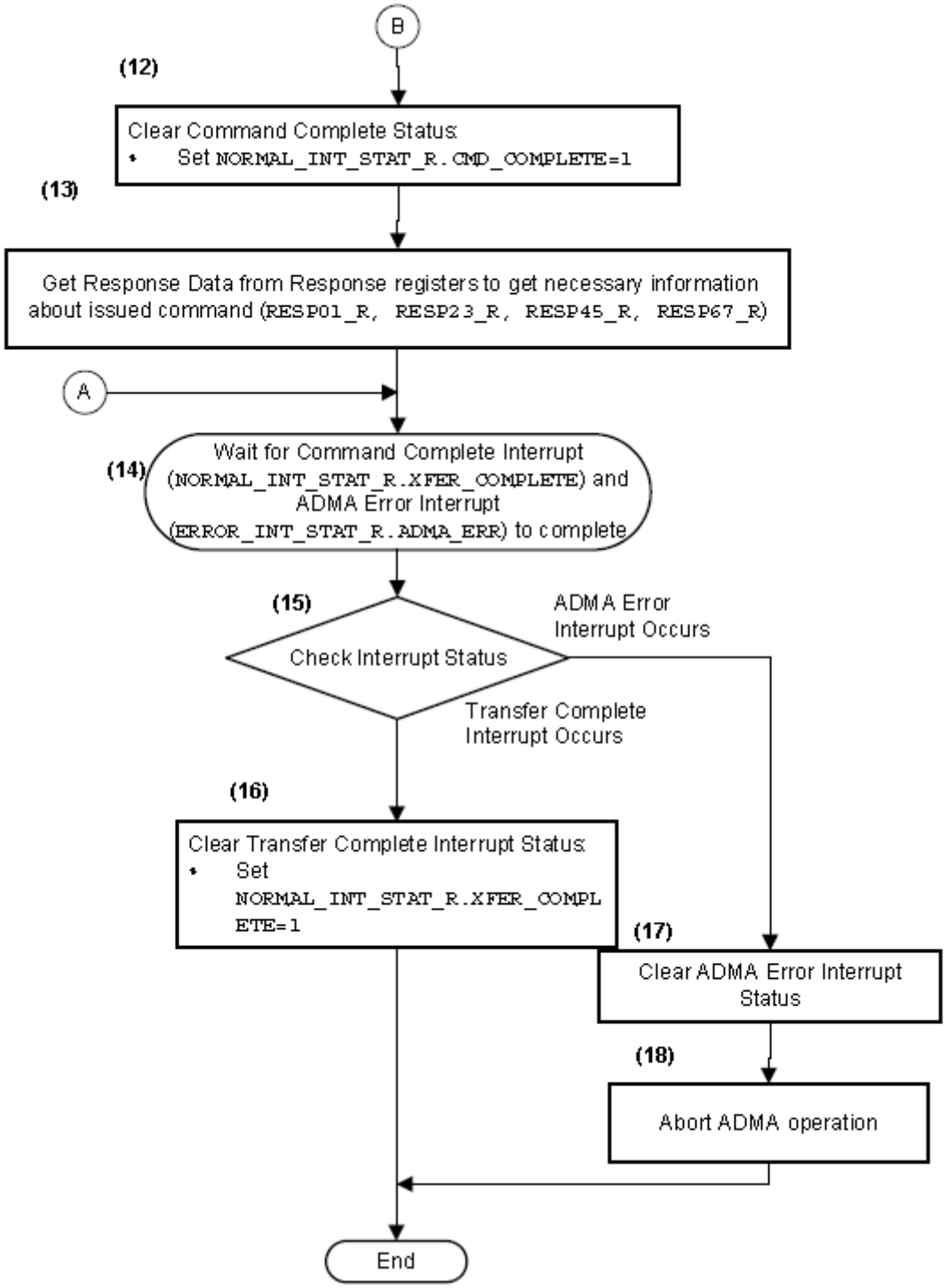


Figure 32-27 Transaction Control with Data Transfer Using DAT Line (Using ADMA) (Contd)

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.9.7.5.4 Issuing CMD with Data Transfer (Using ADMA3)

Figure 32-28 shows the transaction that uses ADMA3 for data transfer using the DAT line.

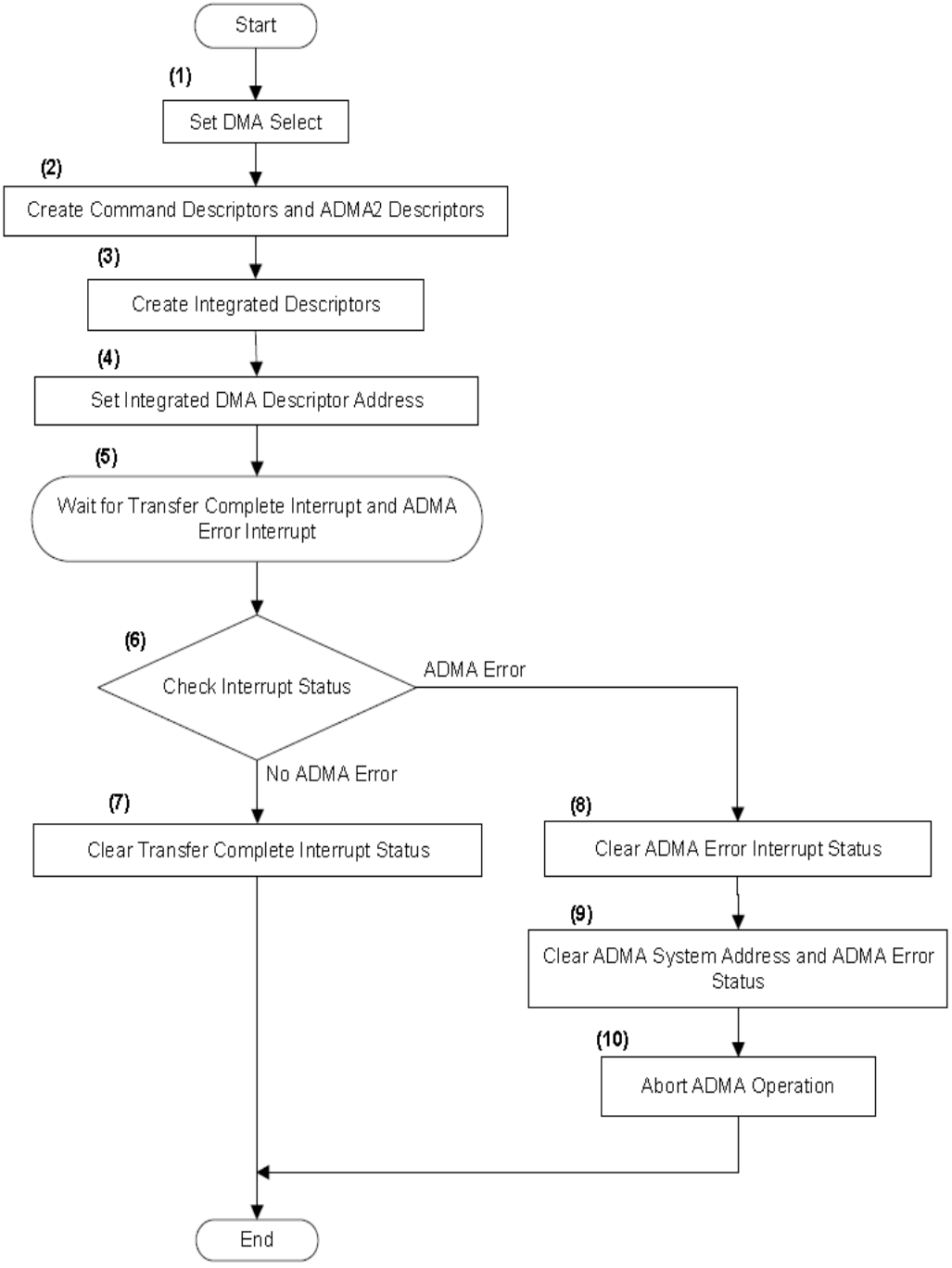


Figure 32-28 Transaction Control with Data Transfer Using DAT Line (Using ADMA3)

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.9.7.6 SD Changing Bus Speed Mode

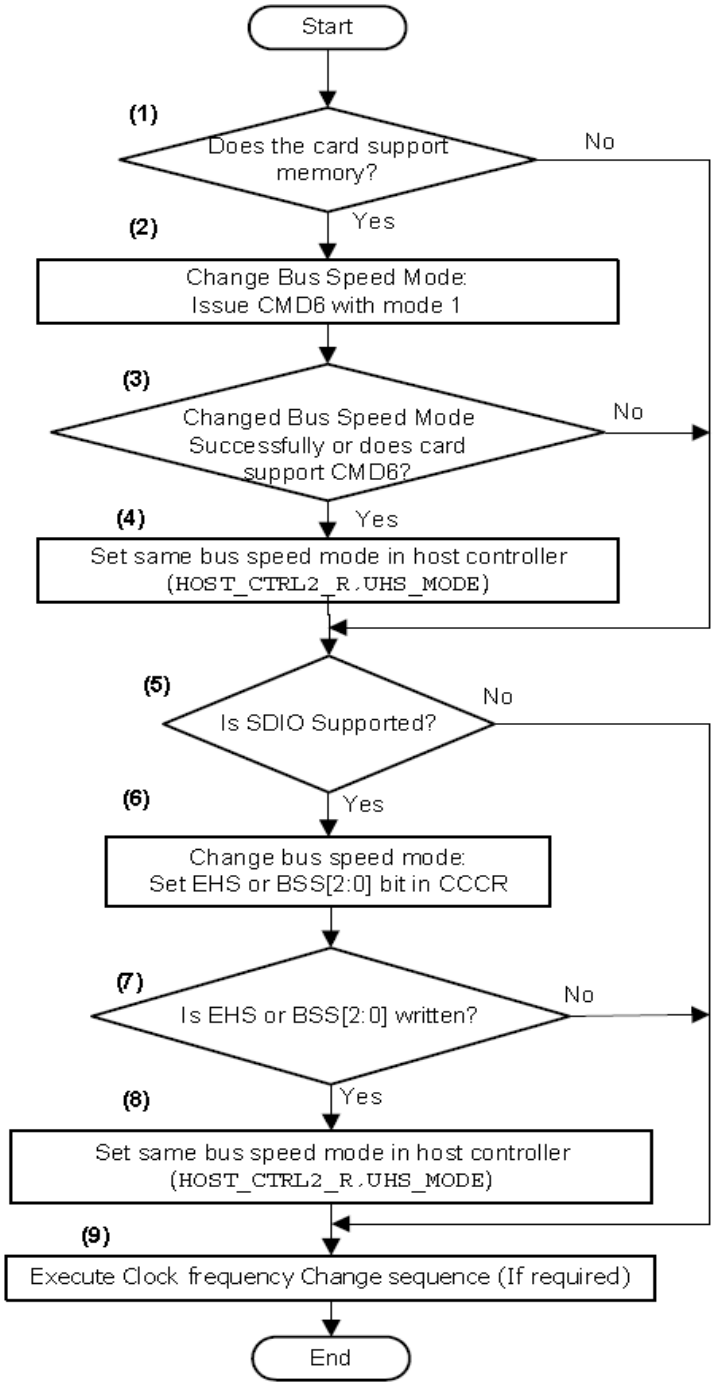


Figure 32-29 SD Changing Bus Speed Mode

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.9.8 eMMC Transaction Mode

This section discusses the programming sequence for setting the host controller for an eMMC interface, initializing and identify the card, issuing a command with/without data transfer using or not using a DAT line, switching to various speed modes and to change the data bus width. This section also discusses how to program, initiate, and abort different boot speed modes.

This section discusses the following programming sequences:

- "Initializing and Identifying an eMMC Device"
- "Issue CMD without Data Transfer for an eMMC Device"
- "Issue CMD with Data Transfer for an eMMC Device"
- "Switch to Various Speed Modes in an eMMC Device"
- "Changing the Data Bus Width for an eMMC Device"
- "Tuning Sequence for an eMMC Device"
- "Command Queueing"

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.9.8.1 Initializing and Identifying an eMMC Device

Figure 32-30 shows the programming sequence to initialize and identify an eMMC device.

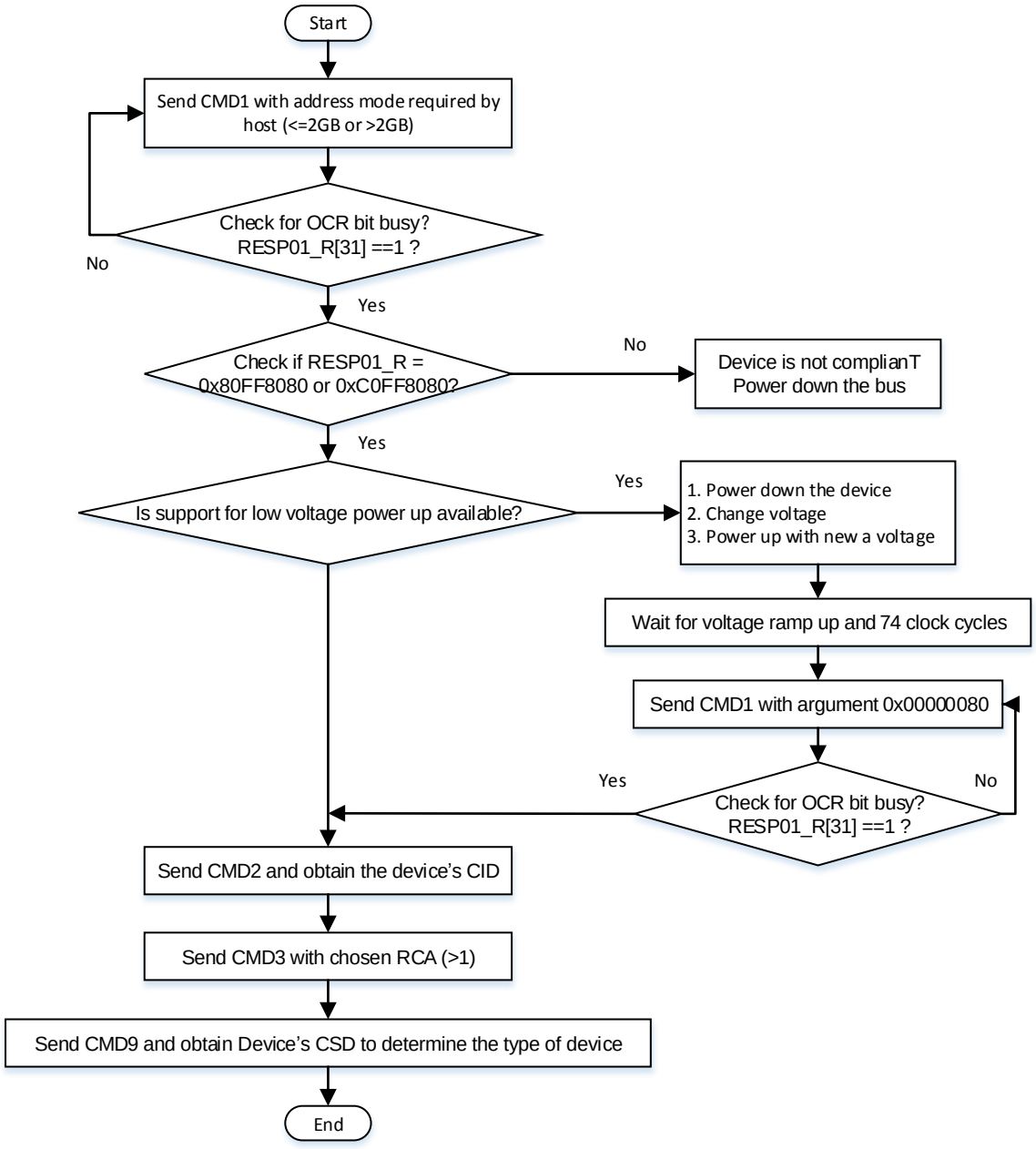


Figure 32-30 Card Initialization and Identification Programming Sequence

32.9.8.2 Issue CMD without Data Transfer for an eMMC Device

The programming sequence for issuing a command without data transfer for an eMMC device is similar to the sequence mentioned in "Issuing CMD without Data

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Transfer"

32.9.8.3 Issue CMD with Data Transfer for an eMMC Device

The programming sequence for issuing a command with data transfer for an eMMC device is similar to the programming sequence mentioned in "Issuing CMD with Data Transfer". Data transfer can be done with or without using DMA. The supported DMA modes are SDMA, ADMA2, and ADMA3.

32.9.8.4 Switch to Various Speed Modes in an eMMC Device

Figure 32-31 shows the programming sequence to switch to various speed modes in an eMMC device. In Figure 32-31, note that CMD6 is effective only during the transfer state.

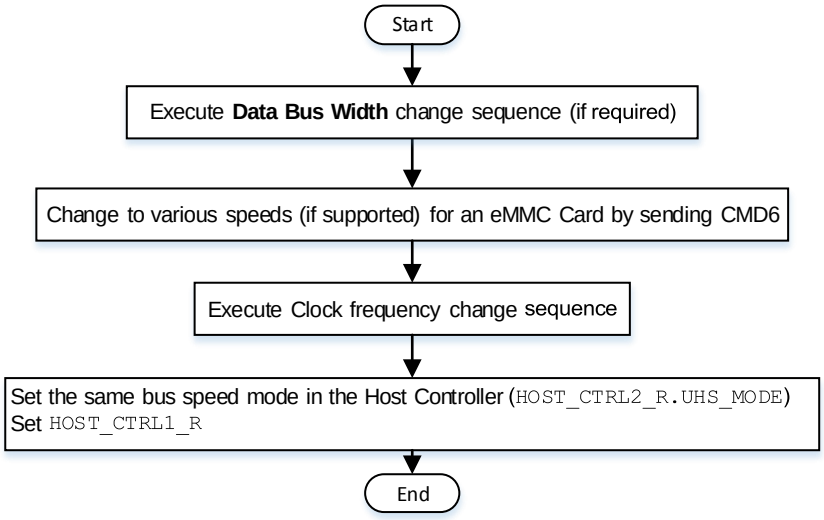
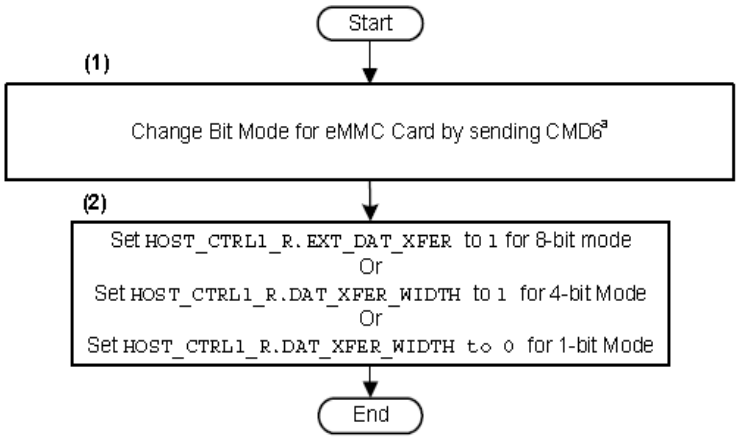


Figure 32-31 Programming Sequence to Switch to Various Speed Modes in an eMMC Device

32.9.8.5 Changing the Data Bus Width for an eMMC Device

Figure 32-32 shows the programming sequence to change the data bus width for an eMMC device. In Figure 32-32, note that CMD6 is effective only during transfer state.



Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Figure 32-32 Programming Sequence to Change Data Bus Width for an eMMC Device

32.9.8.6 Tuning Sequence for an eMMC Device

The tuning sequence for an eMMC device is similar to the programming sequence shown in Figure 32-21 except that for an eMMC device CMD21 is sent for tuning instead of CMD19 as mentioned in Figure 32-21. For eMMC, CMD21 shall be sent for tuning instead of CMD19 as defined in flow diagram.

32.9.8.7 Command Queueing

32.9.8.7.1 Command Queuing Engine Initialization

Figure 32-33 shows the programming sequence to initialize the command queuing engine.

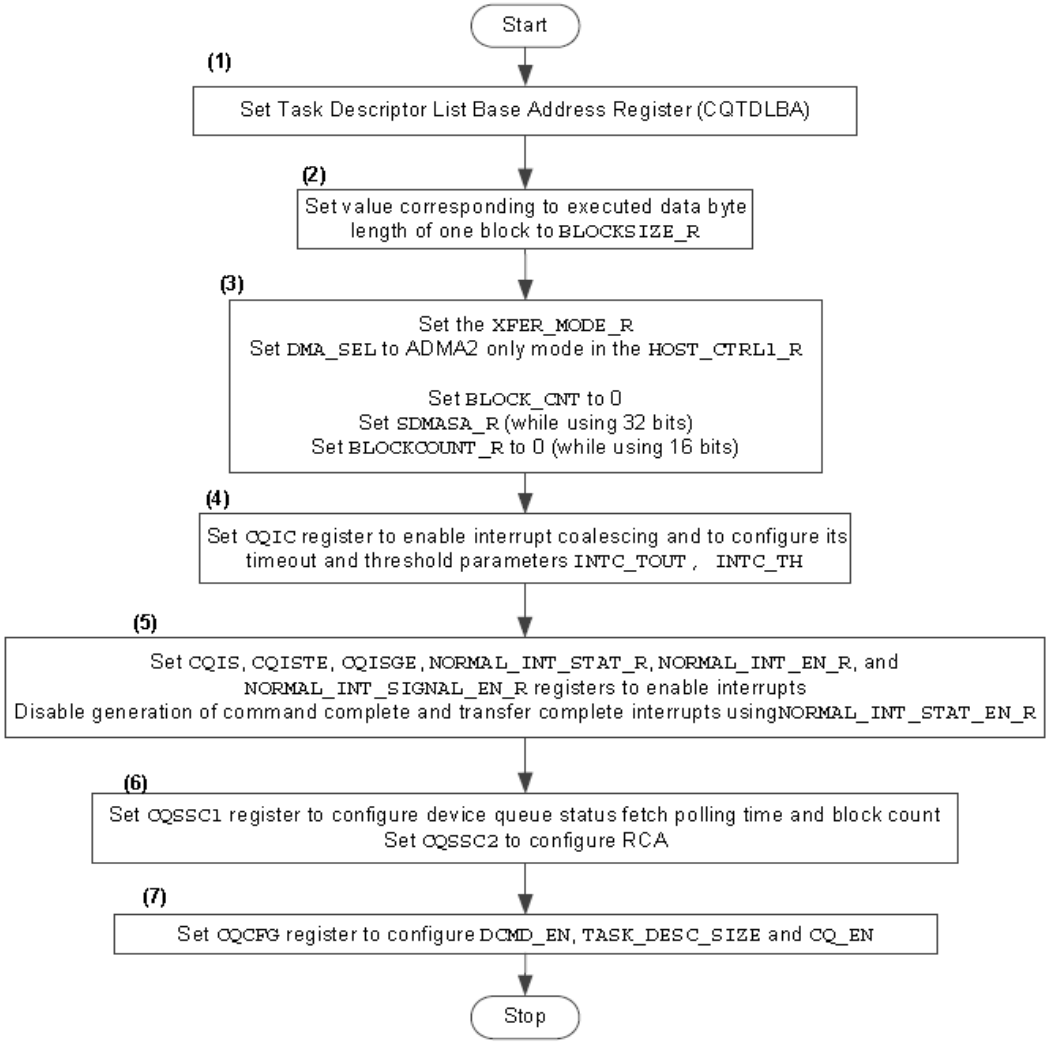


Figure 32-33 Initializing the Command Queuing Engine

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.9.8.7.2 Task Submission and Completion in a Command Queuing Engine

Figure 32-34 shows the sequence to submit and complete a task in a command queuing engine.

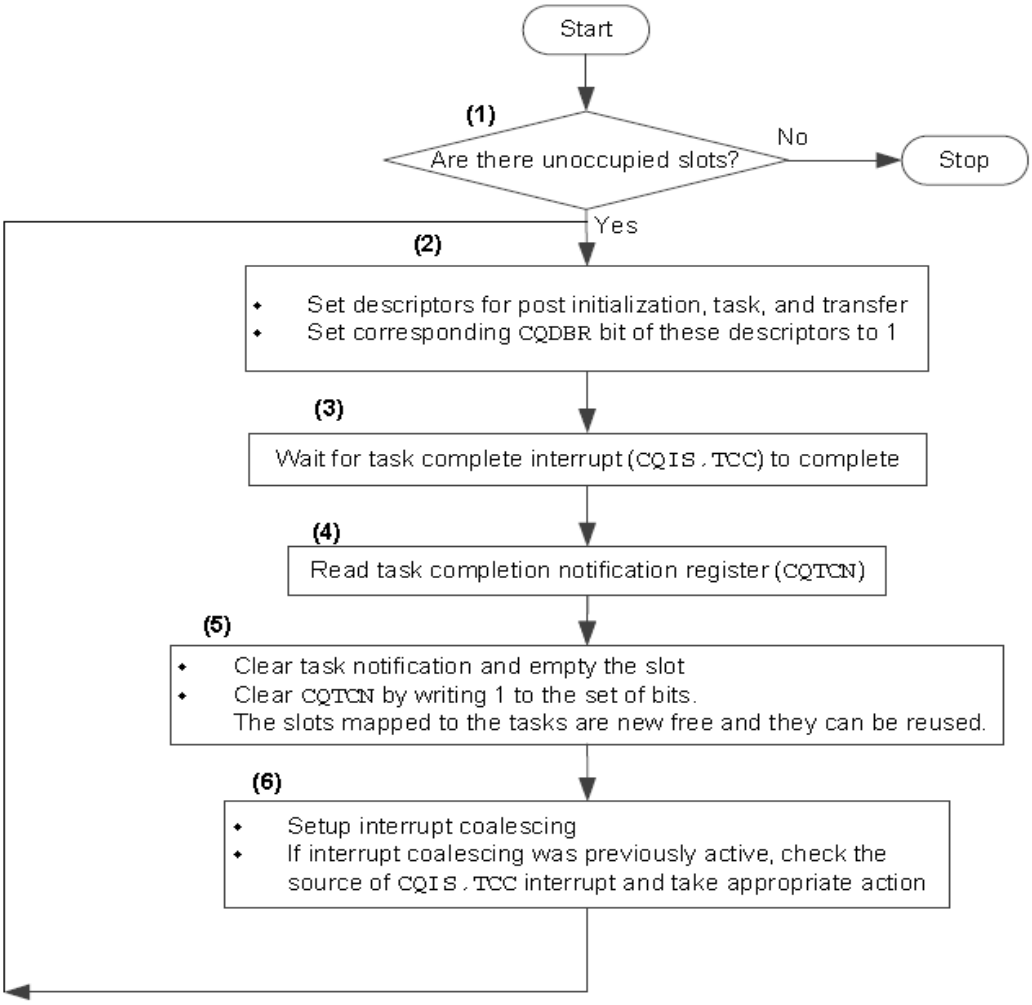


Figure 32-34 Submitting and Completing a Task

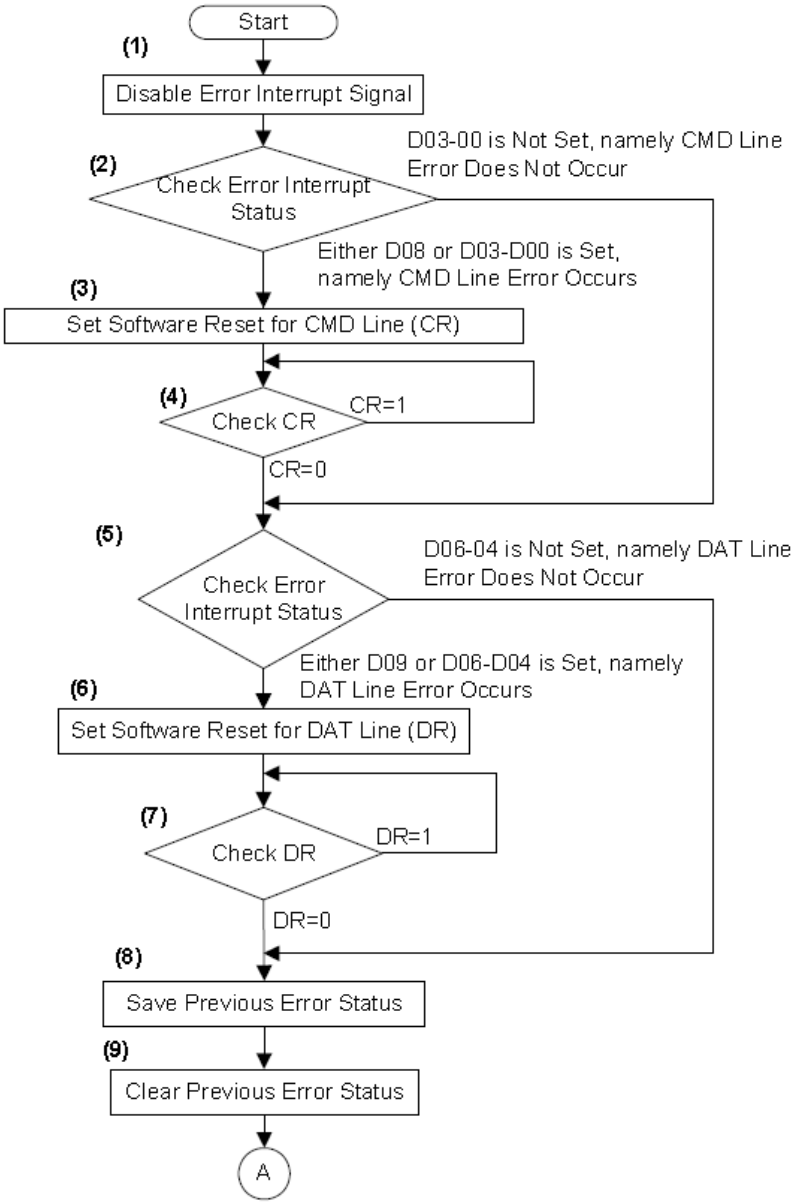
32.9.9 Error Recovery

This section includes the sequence for error recovery in SD, eMMC and SD-TRAN modes. This section discusses the following programming sequences:

- "SD/eMMC Mode"

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

32.9.9.1 SD/eMMC Mode



Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

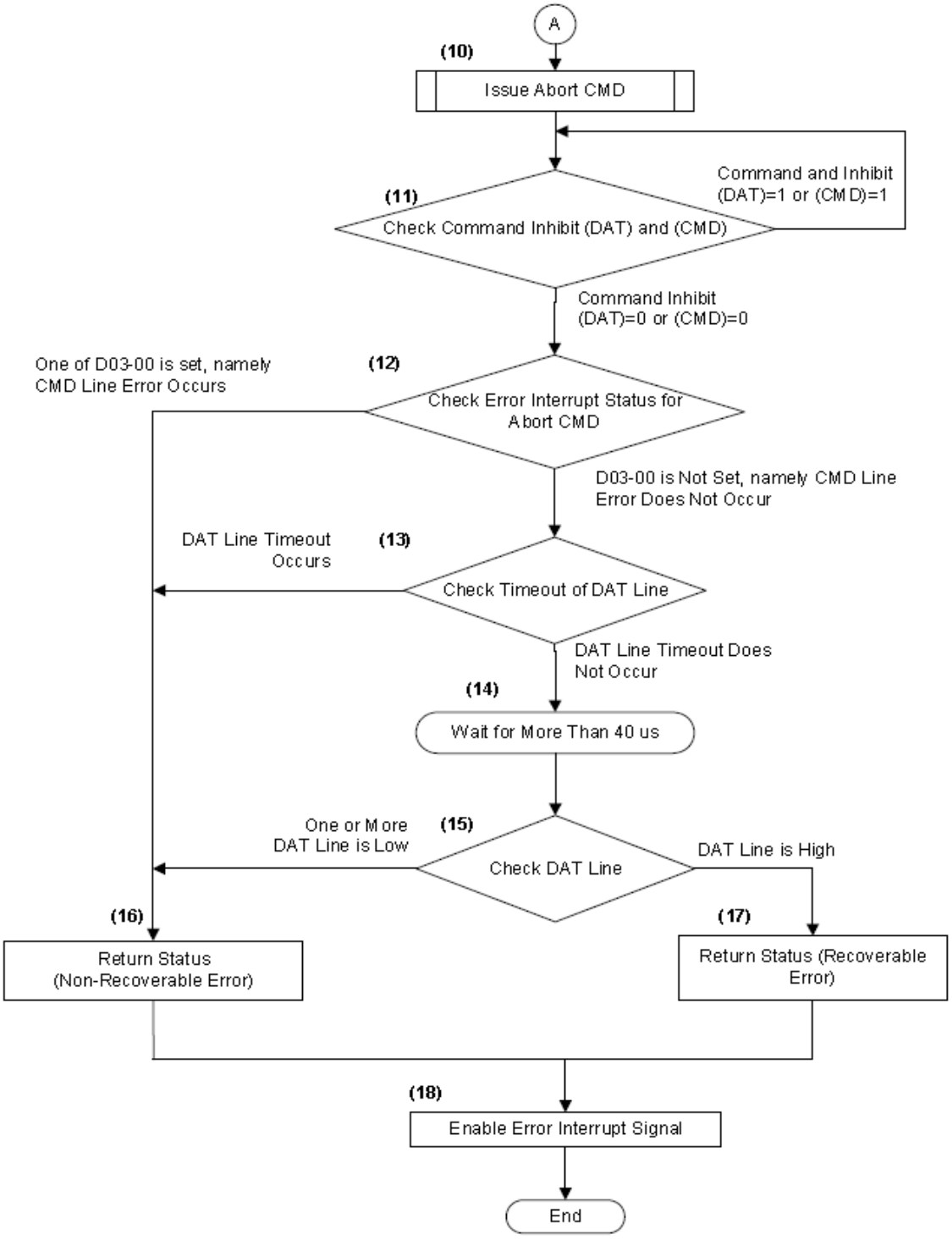


Figure 32-35 Error Recovery in SD/eMMC Mode

Note:

▪ The Error recovery sequence returns either "Recoverable Error" or "Non-Recoverable Error" status. When "Recoverable Error" is returned, error is recovered fully. If "Non- Recoverable Error" status is returned, both controller and card must be re-initialized after performing power cycle for the card.

▪ It is recommended to issue abort command in step 10 synchronously (in Figure 32-35), when DMA is

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

enabled

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

33 ON-THE-GO Controller(OTG)

33.1 Overview

This chapter describes the USB On-The-Go (OTG) implemented in the processor.
The Universal Serial Bus (USB) supports serial data exchanges between a host computer and a variety of simultaneously accessible portable peripherals. Many of these portable devices would benefit a lot from being able to communicate to each other over the USB interface. And OTG make this possible. An OTG device can plays the role of both host and device.
Familiarity with the Universal Serial Bus Specification, Revision 1.1 and OTG supplement are necessary to fully understand the material contained in this section.

33.2 Features

- Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the *On-The-Go* supplement to the USB 2.0 specification
- Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
- UTMI+ Level 3 Transceiver Interface
- Soft connect/disconnect
- 16 Endpoints
- Supports control, interrupt, ISO and bulk transfer

33.3 Functional Description

The OTG is a Dual-Role Device(DRD) controller that supports both device and host functions and complies fully with the On-The-Go Supplement to the USB 2.0 Specification ,Revision 1.3a and Revision 2.0.It can also be configured as a host-only or device-only controller , fully compliant with the USB 2.0 Specification.

33.4 Pins Description

DRV_VBUS：PC17,USB 5-V Signal.
Function: This is the USB 5-V supply. A charge pump external to USB2.0 picoPHY must provide power to this pin. The nominal voltage for this pin is 5V. If VBUS is not used ,leave it floating.

33.5 Data Format Description

Support UTMI 8/16 for the USB-Phy Interface.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

33.6 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R- Read only
   W- Write only
   RW- Read and Write
   RCW- Read and Write, but Clear to 0 by Read
   RSW- Read and Write, but Set to 1 by Read
   RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
   RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
   RC- Read only, and Clear to 0 by read
   RS- Read only, and Set to 1 by read
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

33.6.1 Register Memory Map

Table 33-1 Registers Memory Map Base Address

Name	Base	Description
OTG	0x13500000	Address base of OTG

The On-The-Go Controller is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 33-2 On-The-Go（OTG） Registers Map

Name	RW	Reset Value	Address Offset	Access Size
GOTGCTL	RW	0x0???_0000	0x000	32
GOTGINT	RW	0x0000_0000	0x004	32
GAHBCFG	RW	0x0000_0000	0x008	32
GUSBCFG	RW	0x0?00_140?	0x00C	32
GRSTCTL	RW	0x8000_0000	0x010	32
GINTSTS	RW	0x0400_0020	0x014	32
GINTMSK	RW	0x0000_0000	0x018	32
GRXSTSR	R	0x0000_0000	0x01C	32
GRXSTSP	R	0x0000_0000	0x020	32
GRXFSIZ	RW	0x0000_????	0x024	32
GNPTXFSIZ	RW	0x????_????	0x028	32
GNPTXSTS	RW	0x00??_????	0x02C	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

GHWCFG1	R	0x????_????	0x044	32
GHWCFG2	R	0x????_????	0x048	32
GHWCFG3	R	0x????_????	0x04C	32
GHWCFG4	R	0x????_?0??	0x050	32
GDFIFOCFG	RW	0x????_????	0x05C	32
HPTXFSIZ	RW	0x????_????	0x100	32
DIEPTXFn	RW	0x????_????	0x104+n*0x4	32
HCFG	RW	0x0000_0200	0x400	32
HFIR	RW	0x0000_EA60	0x404	32
HFNUM	R	0x0000_3FFF	0x408	32
HPTXSTS	R	0x00??_????	0x410	32
HAINT	R	0x0000_0000	0x414	32
HAINTMAK	RW	0x0000_0000	0x418	32
HPRT	RW	0x0000_0000	0x440	32
HCCHARn	RW	0x0000_0000	0x500+n*0x20	32
HCSPLTn	RW	0x0000_0000	0x504+n*0x20	32
HCINTn	RW	0x0000_0000	0x508+n*0x20	32
HCINTMSKn	RW	0x0000_0000	0x50c+n*0x20	32
HCTSIZn	RW	0x0000_0000	0x510+n*0x20	32
HCDMAn	RW	0x0000_0000	0x514+n*0x20	32
HCDMABn	R	0x????_????	0x51C+n*0x20	32
DCFG	RW	0x0820_0000	0x800	32
DCTL	RW	0x0000_0002	0x804	32
DSTS	R	0x0000_0002	0x808	32
DIEPMSK	RW	0x0000_0000	0x810	32
DOEPMSK	RW	0x0000_0000	0x814	32
DAINT	R	0x0000_0000	0x818	32
DAINTMSK	RW	0x0000_0000	0x81C	32
DTKNQR1	R	0x0000_0000	0x820	32
DTKNQR2	R	0x0000_0000	0x824	32
DTKNQR3	R	0x0000_0000	0x830	32
DTKNQR4	R	0x0000_0000	0x834	32
DVBUSDIS	RW	0x0000_????	0x828	32
DVBUSPULSE	RW	0x0000_0???	0x82C	32
DTHRCTL	RW	0x0810_0020	0x830	32
DIEPEMPMSK	RW	0x0000_0000	0x834	32
DEACHINT	R	0x0000_0000	0x838	32
DEACHINTMSK	RW	0x0000_0000	0x83C	32
DIEPEACHMSKn	RW	0x0000_0000	0x840	32
DOEPEACHMSKn	RW	0x0000_0000	0x844	32
DIEPCTL0	RW	0x0000_8000	0x900	32
DOEPCTL0	RW	0x0000_8000	0xB00	32

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

DIEPCTLn/DOEPCTLn	RW	0x0000_0000	0x900/0xB00+n*0x20	32
DIEPINTn/DOEPINTn	RW	0x0000_0080	0x908/0xB08+n*0x20	32
DIEPTSIZ0/DOEPTSIZ0	RW	0x0000_0000	0x910/0xB10	32
DIEPTSIZn/DOEPTSIZn	RW	0x0000_0000	0x910/0xB10+n*0x20	32
DIEPDMAn/DOEPDMAn	RW	0x????_????	0x914/0xB14+n*0x20	32
DIEPDMABn/DOEPDMABn	R	0x????_????	0x91C/0xB1C+n*0x20	32
DTXFSTSn	R	0x0000_0000	0x918	32

33.6.2 Register and Fields Description

33.6.2.1 Control and Status Register (GOTGCTL,0x000)

	GOTGCTL																Base + 0x000													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				chirpen	MultValIdBc					Reserved	OTGVer	BSesVld	ASesVld	DbncTime	ConIDSts	Reserved				DevHNPEn	HstSetHNPEn	HNPReq	HstNegScs	BvalidOvVa	BvalidOvEn	AvalidOvVal	AvalidOvEn	VbvalidOvVal	VbvalidOvEn	SesReq	SesReqScs
RST	0	0	0	0	0	?	?	?	?	?	0	0	?	?	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	Mode	R/W
31:26	Reserved	Host and Device	R
27	Chirp On Enable (ChirpEn) This bit when programmed to 1'b1 results in the core asserting chirp_on before sending an actual Chirp "K" signal on USB. This bit is present only if OTG_BC_SUPPORT = 1.If OTG_BC_SUPPORT!=1, this bit is a reserved bit.	Device only	RW
26:22[1]	Multi Valued ID pin (MultValIdBc) Battery Charger ACA inputs in the following order: Bit 26 - rid_float. Bit 25 - rid_gnd Bit 24 - rid_a Bit 23 - rid_b Bit 22 - rid_c These bits are valid only if OTG_BC_SUPPORT=1, otherwise they are reserved.	Host and Device	R
21	Reserved	Host and Device	R
20	OTG Version (OTGVer) Indicates the OTG revision. 1'b0: OTG Version 1.3. In this version the core supports Data line pulsing and VBus pulsing for SRP. 1'b1: OTG Version 2.0. In this version the core supports only	Host and Device	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Data line pulsing for SRP.		
19	B-Session Valid (BSesVld) Indicates the Device mode transceiver status. 1'b0: B-session is not valid. 1'b1: B-session is valid. In OTG mode, you can use this bit to determine if the device is connected or disconnected. **Note:** If you do not enable OTG features (such as SRP and HNP), the read reset value will be 1.The vbus assigns the values internally for non- SRP or non-HNP configurations. In case of OTG_MODE=0, the reset value of this bit is 1'b0.	Device only	R
18	A-Session Valid (ASesVld) Indicates the Host mode transceiver status. 1'b0: A-session is not valid 1'b1: A-session is valid **Note:** If you do not enable OTG features (such as SRP and HNP), the read reset value will be 1.The vbus assigns the values internally for non- SRP or non-HNP configurations. In device mode, this bit is reserved.	Host only	R
17	Long/Short Debounce Time (DbncTime) Indicates the debounce time of a detected connection. 1'b0: Long debounce time, used for physical connections (100 ms + 2.5 μs) 1'b1: Short debounce time, used for soft connections (2.5 μs)	Host only	R
16	Connector ID Status (ConIDSts) Indicates the connector ID status on a connect event. 1'b0: The DWC_otg core is in A-Device mode 1'b1: The DWC_otg core is in B-Device mode	Host and Device	R
15:12	Reserved	Host and Device	R
11	Device HNP Enabled (DevHNPEn) The application sets this bit when it successfully receives a SetFeature.SetHNPEnable command from the connected USB host. 1'b0: HNP is not enabled in the application 1'b1: HNP is enabled in the application	Device Only OTG configurations	RW
10	Host Set HNP Enable (HstSetHNPEn) The application sets this bit when it has successfully enabled HNP (using the SetFeature.SetHNPEnable command) on the connected device. 1'b0: Host Set HNP is not enabled 1'b1: Host Set HNP is enabled	Device Only OTG configurations	RW
9	HNP Request (HNPReq)	Device Only	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	The application sets this bit to initiate an HNP request to the connected USB host. The application can clear this bit by writing a 0 when the Host Negotiation Success Status Change bit in the OTG Interrupt register (GOTGINT.HstNegSucStsChng) is set. The core clears this bit when the HstNegSucStsChng bit is cleared. 1'b0: No HNP request 1'b1: HNP request	OTG configurations	
8	Host Negotiation Success (HstNegScs) The core sets this bit when host negotiation is successful. The core clears this bit when the HNP Request (HNPReq) bit in this register is set. 1'b0: Host negotiation failure 1'b1: Host negotiation success	Device only	R
7	B-Peripheral Session Valid OverrideValue (BvalidOvVal) This bit is used to set the Override value for Bvalid signal when GOTGCTL.BvalidOvEn is set. 1'b0: Bvalid value is 1'b0 when GOTGCTL.BvalidOvEn = 1. 1'b1: Bvalid value is 1'b1 when GOTGCTL.BvalidOvEn = 1.	Device only	RW
6	B-Peripheral Session Valid Override Enable (BvalidOvEn) This bit is used to enable/disable the software to override the Bvalid signal using the GOTGCTL.BvalidOvVal. 1'b1: Internally Bvalid received from the PHY is overridden with GOTGCTL.BvalidOvVal. 1'b0: Override is disabled and Bvalid signal from the respective PHY selected is used internally by the core.	Device only	RW
5	A-Peripheral Session Valid OverrideValue (AvalidOvVal) This bit is used to set the Override value for Avalid signal when GOTGCTL.AvalidOvEn is set. 1'b0: Avalid value is 1'b0 when GOTGCTL.AvalidOvEn = 1. 1'b1: Avalid value is 1'b1 when GOTGCTL.AvalidOvEn = 1.	Host only	RW
4	A-Peripheral Session Valid Override Enable (AvalidOvEn) This bit is used to enable/disable the software to override the Avalid signal using the GOTGCTL.AvalidOvVal. 1'b1: Internally Avalid received from the PHY is overridden with GOTGCTL.AvalidOvVal. 1'b0: Override is disabled and Avalid signal from the respective PHY is used internally by the core.	Host only	RW
3	VBUS Valid OverrideValue (VbvalidOvVal) This bit is used to set the Override value for vbus valid signal when GOTGCTL.VbusvalidOvEn is set. 1'b0: vbusvalid value is 1'b0 when GOTGCTL.VbvalidOvEn = 1.	Host only	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	1'b1: vbusvalid value is 1'b1 when GOTGCTL.VbvalidOvEn = 1.		
2	VBUS Valid Override Enable (VbvalidOvEn) This bit is used to enable/disable the software to override the vbus-valid signal using the GOTGCTL.vbvalidOvVal. 1'b1: The vbus-valid signal received from the PHY is overridden with GOTGCTL.vbvalidOvVal. 1'b0: Override is disabled and avalid signal from the respective PHY is used internally by the core.	Host only	RW
1	Session Request (SesReq) The application sets this bit to initiate a session request on the USB. The application can clear this bit by writing a 0 when the Host Negotiation Success Status Change bit in the OTG Interrupt register (GOTGINT.HstNegSucStsChng) is set. The core clears this bit when the HstNegSucStsChng bit is cleared. If you use the USB 1.1 Full-Speed Serial Transceiver interface to initiate the session request, the application must wait until the VBUS discharges to 0.2 V, after the B-Session Valid bit in this register (GOTGCTL.BSesVld) is cleared. This discharge time varies between different PHYs and can be obtained from the PHY vendor. 1'b0: No session request 1'b1: Session request	Device only	RW
0	Session Request Success (SesReqScs) The core sets this bit when a session request initiation is successful. 1'b0: Session request failure 1'b1: Session request success	Device only	R

Note:

[1]. bits [26:22]: configurable. The reset value is unknown if OTG_BC_ SUPPORT=1 and 0 otherwise.

33.6.2.2 Interrupt Register (GOTGINT,0x004)

	GOTGINT																														Base + 0x004	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												MVIC	DbnceDone	ADevTOUTCh	Reserved							HstNegSucStsChng	SesReqSucStsChng	Reserved					SesEndDet	Reserved	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	Mode	R/W
31:21	Reserved	Host and Device	R
20	Multi-Valued input changed (MVIC) This bit when set indicates that there is a change in the value of at least one ACA pin value. This bit is present only if OTG_BC_SUPPORT = 1, otherwise it is reserved.	Host and Device	RW[1]
19	Debounce Done (DbnceDone) The core sets this bit when the debounce is completed after the device connect. The application can start driving USB reset after seeing this interrupt. This bit is only valid when the HNP Capable or SRP Capable bit is set in the Core USB Configuration register (GUSBCFG.HNPCap or GUSBCFG.SRPCap, respectively).	Host Only	RW[2]
18	A-Device Timeout Change (ADevTOUTChg) The core sets this bit to indicate that the A-device has timed out while waiting for the B-device to connect.	Host and Device	RW[3]
17	Host Negotiation Detected (HstNegDet) The core sets this bit when it detects a host negotiation request on the USB.	Host and Device	RW[4]
16:10	Reserved	Host and Device	R
9	Host Negotiation Success Status Change (HstNegSucStsChng) The core sets this bit on the success or failure of a USB host negotiation request. The application must read the Host Negotiation Success bit of the OTG Control and Status register (GOTGCTL.HstNegScs) to check for success or failure.	Host and Device	RW[5]
8	Session Request Success Status Change (SesReqSucStsChng) The core sets this bit on the success or failure of a session request. The application must read the Session Request Success bit in the OTG Control and Status register (GOTGCTL.SesReqScs) to check for success or failure.	Host and Device	RW[6]
7:3	Reserved	Host and Device	R
2	Session End Detected (SesEndDet) The core sets this bit when the utmisrp_bvalid signal is deasserted.	Device only	RW[7]
1:0	Reserved	Host and Device	R

Note:

[1]~[7]: This bits will operate with Self set , Write clear function.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

33.6.2.3 AHB Configuration Register (GAHBCFG,0x008)

	GAHBCFG																Base + 0x008															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								AHBSingle	NotiAllDmaWrit	RemMemSupp	Reserved												PTxFEmpLvl	NPTxFEmpLvl	Reserved	DMAEn	HBstLen				GlbIntrMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	Mode	R/W
31:24	Reserved	Host and Device	R
23	AHB Single Support (AHBSingle) This bit when programmed supports Single transfers for the remaining data in a transfer when the DWC_otg core is operating in DMA mode. 1'b0: This is the default mode. When this bit is set to 1'b0, the remaining data in the transfer is sent using INCR burst size. 1'b1: When set to 1'b1, the remaining data in a transfer is sent using Single burst size. Note: if this feature is enabled, the AHB RETRY and SPLIT transfers still have INCR burst type. Enable this feature when the AHB Slave connected to the DWC_otg core does not support INCR burst (and when Split, and Retry transactions are not being used in the bus).	Host and Device	RW
22	Notify All Dma Write Transactions (NotiAllDmaWrit) This bit is programmed to enable the System DMA Done functionality for all the DMA write Transactions corresponding to the Channel/Endpoint. This bit is valid only when GAHBCFG.RemMemSupp is set to 1. GAHBCFG.NotiAllDmaWrit = 1 HS OTG core asserts int_dma_req for all the DMA write transactions on the AHB interface along with int_dma_done, chep_last_transact and chep_number signal informations. The core waits for sys_dma_done signal for all the DMA write transactions in order to complete the transfer of a particular Channel/Endpoint. GAHBCFG.NotiAllDmaWrit = 0 HS OTG core asserts int_dma_req signal only for the last transaction of DMA write transfer corresponding to a particular Channel/Endpoint. Similarly, the core waits for	Host and Device	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	sys_dma_done signal only for that transaction of DMA write to complete the transfer of a particular Channel/Endpoint.		
21	Remote Memory Support (RemMemSupp) This bit is programmed to enable the functionality to wait for the system DMA Done Signal for the DMA Write Transfers. GAHBCFG.RemMemSupp=1 The int_dma_req output signal is asserted when HS OTG DMA starts write transfer to the external memory. When the core is done with the Transfers it asserts int_dma_done signal to flag the completion of DMA writes from HS OTG. The core then waits for sys_dma_done signal from the system to proceed further and complete the Data Transfer corresponding to a particular Channel/Endpoint. GAHBCFG.RemMemSupp=0 The int_dma_req and int_dma_done signals are not asserted and the core proceeds with the assertion of the XferComp interrupt as soon as the DMA write transfer is done at the HS OTG Core Boundary and it doesn't wait for the sys_dma_done signal to complete the DATA transfers.	Host and Device	RW
20:9	Reserved	Host and Device	R
8	Periodic TxFIFO Empty Level (PTxFEmpLvl) Indicates when the Periodic TxFIFO Empty Interrupt bit in the Core Interrupt register (GINTSTS.PTxFEmp) is triggered. This bit is used only in Slave mode. 1'b0: GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is half empty 1'b1: GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is completely empty	Host only	RW
7	Non-Periodic TxFIFO Empty Level (NPTxFEmpLvl) This bit is used only in Slave mode. In host mode and with Shared FIFO with device mode, this bit indicates when the Non-Periodic TxFIFO Empty Interrupt bit in the Core Interrupt register (GINTSTS.NPTxFEmp) is triggered. With dedicated FIFO in device mode, this bit indicates when IN endpoint Transmit FIFO empty interrupt (DIEPINTn.TxFEmp) is triggered. Host mode and with Shared FIFO with device mode: 1'b0: GINTSTS.NPTxFEmp interrupt indicates that the Non-Periodic TxFIFO is half empty 1'b1: GINTSTS.NPTxFEmp interrupt indicates that the Non-Periodic TxFIFO is completely empty Dedicated FIFO in device mode:	Host and Device	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	1'b0: DIEPINTn.TxFEmp interrupt indicates that the IN Endpoint TxFIFO is half empty 1'b1: DIEPINTn.TxFEmp interrupt indicates that the IN Endpoint TxFIFO is completely empty		
6	Reserved	Host and Device	R
5	DMA Enable (DMAEn) 1'b0: Core operates in Slave mode 1'b1: Core operates in a DMA mode	Host and Device	RW
4:1	Burst Length/Type (HBstLen) This Bits is used in both External and Internal DMA modes. In External DMA mode, these bits appear on dma_burst[3:0] ports, which can be used by an external wrapper to interface the External DMA Controller interface to Synopsys DW_ahb_dmac or ARM PrimeCell. External DMA Mode — defines the DMA burst length in terms of 32-bit words: 4'b0000: 1 word 4'b0001: 4 words 4'b0010: 8 words 4'b0011: 16 words 4'b0100: 32 words 4'b0101: 64 words 4'b0110: 128 words 4'b0111: 256 words Others: Reserved Internal DMA Mode — AHB Master burst type: 4'b0000 Single 4'b0001 INCR 4'b0011 INCR4 4'b0101 INCR8 4'b0111 INCR16 Others: Reserved Slave Mode: Only single burst is supported.	Host and Device	RW
0	Global Interrupt Mask (GlblIntrMsk) The application uses this bit to mask or unmask the interrupt line assertion to itself. Irrespective of this bit's setting, the interrupt status registers are updated by the core. 1'b0: Mask the interrupt assertion to the application. 1'b1: Unmask the interrupt assertion to the application.	Host and Device	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

33.6.2.4 USB Configuration Register (GUSBCFG,0x00C)

	GUSBCFG																Base + 0x00C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Txpacket	ForceDevMode	ForceHstMode	TxEndDelay	IC_USBTrafCtl	C_USBCap	ULIPPectDis	IndiPass	IndiComp	TermSelDLPulse	ULPIExtVbusIndicator	ULPIExtVbusDrv	ULPIClkSusM	ULPIAutoRes	ULPIFsLs	Otgl2CSel	PhyLPwrClkSel	Reserved	USBTrdTim				HNPCap	SRPCap	DDRSel	PHYSel	FSIntf	ULPI_UTMI_Sel	PHYIf	TOutCal		
RST	0	0	0	0	0	?	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	?	0	0	0

Bits	Description	Mode	R/W
31	Corrupt Tx packet(Txpacket) This bit is for debug purposes only. Never set this bit to 1.	Host and Device	W
30	Force Device Mode (ForceDevMode) Writing a 1 to this bit forces the core to device mode irrespective of utmiotg_iddig input pin. 1'b0: Normal Mode 1'b1: Force Device Mode After setting the force bit, the application must wait at least 25 ms before the change to take effect. When the simulation is in scale down mode, waiting for 500 µs is sufficient.	Host and Device	RW
29	Force Host Mode (ForceHstMode) Writing a 1 to this bit forces the core to host mode irrespective of utmiotg_iddig input pin. 1'b0: Normal Mode 1'b1: Force Host Mode After setting the force bit, the application must wait at least 25 ms before the change to take effect. When the simulation is in scale down mode, waiting for 500 µs is sufficient.	Host and Device	RW
28	Tx End Delay (TxEndDelay) Writing a 1 to this bit enables the TxEndDelay timers in the core as per the section 4.1.5 on Opmode of the USB 2.0 Transceiver Macrocell Interface (UTMI) version 1.05. 1'b0: Normal mode 1'b1: Introduce Tx end delay timers	Device Only	RW
27	IC_USB TrafficPullRemove Control (IC_USBTrafCtl) When this bit is set, pullup/pulldown resistors are detached from the USB during traffic signaling, per section 6.3.4 of the IC_USB specification. This bit is invalid.	Device	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

26	IC_USB-Capable (IC_USBCap) The application uses this bit to control the DWC_otg core's IC_USB capabilities. 1'b0: IC_USB PHY Interface is not selected. 1'b1: IC_USB PHY Interface is selected. This bit is set to 1'b0 and the bit is read only.	Host and Device	R
25	ULPI Interface Protect Disable (ULIPPectDis) Controls circuitry built into the PHY for protecting the ULPI interface when the link tri-states STP and data. Any pull-ups or pull-downs employed by this feature can be disabled. 1'b0: Enables the interface protect circuit 1'b1: Disables the interface protect circuit This bit is reserved and read-only.	Host only	R
24	Indicator Pass Through(IndiPass) Controls wether the Complement Output is qualified with the Internal Vbus Valid comparator before being used in the Vbus State in the RX CMD. Please refer to the ULPI Specification for more detail. 1'b0: Complement Output signal is qualified with the Internal VbusValid comparator. 1'b1: Complement Output signal is not qualified with the Internal VbusValid comparator. This bit is reserved and read-only.	Host Only	R
23	Indicator Complement(IndiComp) Controls the PHY to invert the ExternalVbusIndicator input signal, generating the Complement Output. Please refer to the ULPI Specification for more detail 1'b0: PHY does not invert ExternalVbusIndicator signal 1'b1: PHY does invert ExternalVbusIndicator signal This bit is reserved and read-only.	Host Only	R
22	TermSel DLine Pulsing Selection (TermSelDLPulse) This bit selects utmi_termselect to drive data line pulse during SRP. 1'b0: Data line pulsing using utmi_txvalid (default). 1'b1: Data line pulsing using utmi_termsel.	Device Only	RW
21	ULPI External VBUS Indicator (ULPIExtVbusIndicator) This bit indicates to the ULPI PHY to use an external VBUS over-current indicator. 1'b0: PHY uses internal VBUS valid comparator.	Host Only	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	1'b1: PHY uses external VBUS valid comparator. This bit is invalid.		
20	ULPI External VBUS Drive (ULPIExtVbusDrv) This bit selects between internal or external supply to drive 5V on VBUS, in ULPI PHY. 1'b0: PHY drives VBUS using internal charge pump (default). 1'b1: PHY drives VBUS using external supply. This bit is invalid.	Host Only	RW
19	ULPI Clock SuspendM (ULPIClkSusM) This bit sets the ClockSuspendM bit in the Interface Control register on ULPI PHY. 1'b0: PHY powers down internal clock during suspend. 1'b1: PHY does not power down internal clock. This bit is invalid.	Host and Device	RW
18	ULPI Auto Resume (ULPIAutoRes) This bit sets the AutoResume bit in the Interface Control register on the ULPIPHY. 1'b0: PHY does not use AutoResume feature. 1'b1: PHY uses AutoResume feature. This bit is invalid.	Host and Device	RW
17	ULPI FS/LS Select (ULPIFsLs) The application uses this bit to select the FS/LS serial interface for the ULPI PHY. This bit is valid only when the FS serial transceiver is selected on the ULPI PHY. 1'b0: ULPI interface 1'b1: ULPI FS/LS serial interface	Host and Device	RW
16	UTMIFS or I2C Interface Select (OtgI2CSel) The application uses this bit to select the I2C interface. 1'b0: UTMI USB 1.1 Full-Speed interface for OTG signals 1'b1: I 2C interface for OTG signals This bit is writable only if I 2C and UTMIFS were specified for Enable I2C Interface	Host and Device	R/RW
15	PHY Low-Power Clock Select (PhyLPwrClkSel) Selects either 480-MHz or 48-MHz (low-power) PHY mode. In FS and LS modes, the PHY can usually operate on a 48-MHz clock to save power. 1'b0: 480-MHz Internal PLL clock 1'b1: 48-MHz External Clock In 480 MHz mode, the UTMI interface operates at either 60 or 30-MHz, depending upon whether 8- or 16-bit data width is selected. In 48-MHz mode, the UTMI interface operates at 48 MHz in FS and LS modes. This bit drives the utmi_fsls_low_power core output signal,	Host and Device	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	and is valid only for UTMI+ PHYs.		
14	Reserved	Host and Device	R
13:10	USB Turnaround Time (USBTrdTim) Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIFO (SPRAM). This must be programmed to 4'h5: When the MAC interface is 16-bit UTMI+. 4'h9: When the MAC interface is 8-bit UTMI+. Note: The values above are calculated for the minimum AHB frequency of 30 MHz. USB turnaround time is critical for certification where long cables and 5-Hubs are used, so if you need the AHB to run at less than 30 MHz, and if USB turnaround time is not critical, these bits can be programmed to a larger value.	Device Only	RW
9	HNP-Capable (HNPCap) The application uses this bit to control the DWC_otg core's HNP capabilities. 1'b0: HNP capability is not enabled. 1'b1: HNP capability is enabled. This bit is writable only if an HNP mode was specified for Mode of operation in coreConsultant (parameter OTG_MODE). Otherwise, reads return 0. If HNP functionality is disabled by the software, the OTG signals on the PHY domain must be tied to the appropriate values.	Host and Device	R/RW
8	SRP-Capable (SRPCap) The application uses this bit to control the DWC_otg core SRP capabilities. If the core operates as a non-SRP-capable B-device, it cannot request the connected A-device (host) to activate VBUS and start a session. 1'b0: SRP capability is not enabled. 1'b1: SRP capability is enabled. If SRP functionality is disabled by the software, the OTG signals on the PHY domain must be tied to the appropriate values.	Host and Device	RW
7	ULPI DDR Select (DDRSel) The application uses this bit to select a Single Data Rate (SDR) or Double Data Rate (DDR) or ULPI interface. 1'b0: Single Data Rate ULPI Interface, with 8-bit-wide data bus 1'b1: Double Data Rate ULPI Interface, with 4-bit-wide data	Host and Device	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	bus This bit is invalid.		
6	USB 2.0 High-Speed PHY or USB 1.1 Full-Speed Serial Transceiver Select (PHYSel) The application uses this bit to select either a high-speed UTMI+ or ULPI PHY, or a full-speed transceiver. 1'b0: USB 2.0 high-speed UTMI+ or ULPI PHY 1'b1: USB 1.1 full-speed serial transceiver This bit is always 0, with Read Only access.	Host and Device	R/RW
5	Full-Speed Serial Interface Select (FSIntf) The application uses this bit to select either a unidirectional or bidirectional USB 1.1 full-speed serial transceiver interface. 1'b0: 6-pin unidirectional full-speed serial interface 1'b1: 3-pin bidirectional full-speed serial interface This bit is always 0, with Read Only access.	Host and Device	R/RW
4	ULPI or UTMI+ Select (ULPI_UTMI_Sel) The application uses this bit to select either a UTMI+ interface or ULPI Interface. 1'b0: UTMI+ Interface 1'b1: ULPI Interface This bit takes effect only if GUSBCFG.PHYSel = 1'b0.	Host and Device	R/RW
3	PHY Interface (PHYIf) The application uses this bit to configure the core to support a UTMI+ PHY with an 8- or 16-bit interface. When a ULPI PHY is chosen, this must be set to 8-bit mode. 1'b0: 8 bits 1'b1: 16 bits This bit is writable only if UTMI+ and ULPI were selected in coreConsultant configuration (parameter = 2). Otherwise, this bit returns the value for the power-on interface selected during configuration.	Host and Device	R/RW
2:0	HS/FS Timeout Calibration (TOutCal) The number of PHY clocks that the application programs in this Bits is added to the high-speed/full-speed interpacket timeout duration in the core to account for any additional delays introduced by the PHY. This can be required, because the delay introduced by the PHY in generating the line state condition can vary from one PHY to another. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value for full-speed operation is 16 to 18 (inclusive) bit times. The application must program this Bits based on the speed of enumeration. The number of bit times added per PHY clock	Host and Device	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	are: High-speed operation: One 30-MHz PHY clock = 16 bit times One 60-MHz PHY clock = 8 bit times Full-speed operation: One 30-MHz PHY clock = 0.4 bit times One 60-MHz PHY clock = 0.2 bit times One 48-MHz PHY clock = 0.25 bit times Using the HS as an example, if you set ToutCal to '001' you add one 30MHz PHY clock or 16 bit times. If you set ToutCal to '010' you add two 30MHz PHY clocks or 32 bit times, and so on. The 3 bits allow you to add up to 7 PHY clocks, and the number of bit times depend on the speed, and the PHY clock you are using.		

33.6.2.5 Reset Register (GRSTCTL,0x010)

	GRSTCTL																					Base + 0x010										
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AHBIdle	DMAReq	Reserved																			DMAReq					TxFFIsh	RxFFIsh	INTknQFIsh	FrmCntrRst	Reserved	CSftRst
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	Mode	R/W
31	AHB Master Idle (AHBIdle) Indicates that the AHB Master State Machine is in the IDLE condition.	Host and Device	R
30	DMA Request Signal (DMAReq) Indicates that the DMA request is in progress. Used for debug.	Host and Device	R
29:11	Reserved	Host and Device	R
10:6	TxFIFO Number (TxFNum) This is the FIFO number that must be flushed using the TxFIFO Flush bit. This Bits must not be changed until the core clears the TxFIFO Flush bit. 5'h0: Non-periodic TxFIFO flush in Host mode Non-periodic TxFIFO flush in device mode when in shared	Host and Device	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	FIFO operation Tx FIFO 0 flush in device mode when in dedicated FIFO mode 5'h1: Periodic TxFIFO flush in Host mode Periodic TxFIFO 1 flush in Device mode when in shared FIFO operation TXFIFO 1 flush in device mode when in dedicated FIFO mode 5'h2: Periodic TxFIFO 2 flush in Device mode when in shared FIFO operation TXFIFO 2 flush in device mode when in dedicated FIFO mode ... 5'hF: Periodic TxFIFO 15 flush in Device mode when in shared FIFO operation TXFIFO 15 flush in device mode when in dedicated FIFO mode 5'h10: Flush all the transmit FIFOs in device or host mode.		
5	TxFIFO Flush (TxFFlsh) This bit selectively flushes a single or all transmit FIFOs, but cannot do so if the core is in the midst of a transaction. The application must write this bit only after checking that the core is neither writing to the TxFIFO nor reading from the TxFIFO. Verify using these registers: Read—NAK Effective Interrupt ensures the core is not reading from the FIFO. Write—GRSTCTL.AHBIdle ensures the core is not writing anything to the FIFO. Flushing is normally recommended when FIFOs are re-configured or when switching between Shared FIFO and Dedicated Transmit FIFO operation. FIFO flushing is also recommended during device endpoint disable. The application must wait until the core clears this bit before performing any operations. This bit takes eight clocks to clear, using the slower clock of phy_clk or hclk.	Host and Device	RW[1]
4	RxFIFO Flush (RxFFlsh) The application can flush the entire RxFIFO using this bit, but must first ensure that the core is not in the middle of a	Host and Device	RW[2]

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	transaction. The application must only write to this bit after checking that the core is neither reading from the RxFIFO nor writing to the RxFIFO. The application must wait until the bit is cleared before performing any other operations. This bit requires 8 clocks (slowest of PHY or AHB clock) to clear.		
3	IN Token Sequence Learning Queue Flush (INTknQFlsh) This bit is valid only if OTG_EN_DED_TX_FIFO = 0. The application writes this bit to flush the IN Token Sequence Learning Queue.	Device Only	RW[3]
2	Host Frame Counter Reset (FrmCntrRst) The application writes this bit to reset the (micro)frame number counter inside the core. When the (micro)frame counter is reset, the subsequent SOF sent out by the core has a (micro)frame number of 0.	Host Only	RW[4]
1	Reserved	Host and Device	R
0	Core Soft Reset (CSftRst) Resets the hclk and phy_clock domains as follows: Clears the interrupts and all the CSR registers except the following register bits: PCGCCTL.RstPdwnModule PCGCCTL.GateHclk PCGCCTL.PwrClmp GUSBCFG.DDRSel GUSBCFG.PHYSel GUSBCFG.FSIntf GUSBCFG.ULPI_UTMI_Sel GUSBCFG.PHYIf HCFG.FSLSPclkSel DCFG.DevSpd DCTL.SftDiscon GGPIO GUSBCFG.TxEndDelay GUSBCFG.TermSelDLPulse GUSBCFG.ULPIClkSusM GUSBCFG.ULPIAutoRes GUSBCFG.ULPIFsLs GPWRDN GADPCTL All module state machines (except the AHB Slave Unit) are reset to the IDLE state, and all the transmit FIFOs and the receive FIFO are flushed.	Host and Device	RW[5]

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Any transactions on the AHB Master are terminated as soon as possible, after gracefully completing the last data phase of an AHB transfer. Any transactions on the USB are terminated immediately. When Hibernation or ADP feature is enabled, the PMU module is not reset by the Core Soft Reset. The application can write to this bit any time it wants to reset the core. This is a self-clearing bit and the core clears this bit after all the necessary logic is reset in the core, which can take several clocks, depending on the current state of the core. Once this bit is cleared software must wait at least 3 PHY clocks before doing any access to the PHY domain (synchronization delay). Software must also must check that bit 31 of this register is 1 (AHB Master is IDLE) before starting any operation. Typically software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain has to be reset for proper operation.		

***Notes*:**

[1]~[5]: This bits will operate with Write set , self clear function.

33.6.2.6 Interrupt Register (GINTSTS,0x014)

	GINTSTS																														
																														Base + 0x014	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WkUpInt	SessReqInt	DisconnInt	ConIDStsChng	LPM_Int	PTxFEmp	HCInt	PrtInt	ResetDet	FetSusp	incompIP	incompISOIN	OEPInt	IEPInt	EPMis	RstrDoneInt	EOPF	ISOOutDrop	EnumDone	USBRst	USBSusp	ErlySusp	I2CINT	ULPICKINT	GOUTNakEff	GINNakEff	NPTxFEmp	RxFLvl	Sof	OTGInt	ModeMis	CurMod
RST	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Description	Mode	R/W
31	Resume/Remote Wakeup Detected Interrupt (WkUpInt) Wakeup Interrupt during Suspend(L2) or LPM(L1) state. During Suspend(L2): Device Mode - This interrupt is asserted only when Host Initiated Resume is detected on USB.	Host and Device	RW[1]

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Host Mode - This interrupt is asserted only when Device Initiated Remote Wakeup is detected on USB. During LPM(L1): Device Mode - This interrupt is asserted for either Host Initiated Resume or Device Initiated Remote Wakeup on USB. Host Mode - This interrupt is asserted for either Host Initiated Resume or Device Initiated Remote Wakeup on USB.		
30	Session Request/New Session Detected Interrupt (SessReqInt) In Host mode, this interrupt is asserted when a session request is detected from the device. In Host mode, this interrupt is asserted when a session request is detected from the device. In Device mode, this interrupt is asserted when the utmisrp_bvalid signal goes high. For more information on how to use this interrupt, see "FIFO RAM Allocation" in the Programming Guide.	Host and Device	RW[2]
29	Disconnect Detected Interrupt (DisconnInt) This interrupt is asserted when a device disconnect is detected.	Host Only	RW[3]
28	Connector ID Status Change (ConIDStsChng) This interrupt is asserted when there is a change in connector ID status.	Host and Device	RW[4]
27	LPM Transaction Received Interrupt (LPM_Int) Device Mode - This interrupt is asserted when the device receives an LPM transaction and responds with a non-ERROREd response. Host Mode - This interrupt is asserted when the device responds to an LPM transaction with a non-ERROREd response or when the host core has completed LPM transactions for the programmed number of times (GLPMCFG.RetryCnt). This Bits is valid only if the Core LPM Configuration register's LPM- Capable (LPMCap) Bits is set to 1 and the User HW Config3 register's OTG_ENABLE_LPM bit is set to 1.	Host and Device	RW[5]
26	Periodic TxFIFO Empty (PTxFEmp) This interrupt is asserted when the Periodic Transmit FIFO is either half or completely empty and there is space for at least one entry to be written in the Periodic Request Queue. The half or completely empty status is determined by the Periodic TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.PTxFEmpLvl).	Host Only	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

25	Host Channels Interrupt (HChInt) The core sets this bit to indicate that an interrupt is pending on one of the channels of the core (in Host mode). The application must read the Host All Channels Interrupt (HAINT) register to determine the exact number of the channel on which the interrupt occurred, and then read the corresponding Host Channel-n Interrupt (HCINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the HCINTn register to clear this bit.	Host Only	R
24	Host Port Interrupt (PrtInt) The core sets this bit to indicate a change in port status of one of the DWC_otg core ports in Host mode. The application must read the Host Port Control and Status (HPRT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the Host Port Control and Status register to clear this bit.	Host Only	R
23	Reset Detected Interrupt (ResetDet) The core sets this status bit in device mode when reset is detected on the USB in L2 Suspend state. This bit is valid only when the core is Device Mode and is operating in Partial Power-Down, or Clock Gating modes of Suspend. This bit is not valid when device is in Hibernation mode of Suspend.	Device Only	RW[6]
22	Data Fetch Suspended (FetSusp) This interrupt is valid only in DMA mode. This interrupt indicates that the core has stopped fetching data for IN endpoints due to the unavailability of TxFIFO space or Request Queue space. This interrupt is used by the application for an endpoint mismatch algorithm. For example, after detecting an endpoint mismatch, the application: Sets a global non-periodic IN NAK handshake Disables In endpoints Flushes the FIFO Determines the token sequence from the IN Token Sequence Learning Queue Re-enables the endpoints Clears the global non-periodic IN NAK handshake If the global non-periodic IN NAK is cleared, the core has not yet fetched data for the IN endpoint, and the IN token is	Device Only	RW[7]

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	received: the core generates an "IN token received when FIFO empty" interrupt. The OTG then sends the host a NAK response. To avoid this scenario, the application can check the GINTSTS.FetSusp interrupt, which ensures that the FIFO is full before clearing a global NAK handshake. Alternatively, the application can mask the "IN token received when FIFO empty" interrupt when clearing a global IN NAK handshake.		
21	Incomplete Periodic Transfer (incomplP) In Host mode, the core sets this interrupt bit when there are incomplete periodic transactions still pending which are scheduled for the current microframe. Incomplete Isochronous OUT Transfer (incompISOOUT) The Device mode, the core sets this interrupt to indicate that there is at least one isochronous OUT endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register.	Host only Device only	RW[8]
20	Incomplete Isochronous IN Transfer (incompISOIN) The core sets this interrupt to indicate that there is at least one isochronousIN endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register. Note: This interrupt is not asserted in Scatter/Gather DMA mode.	Device only	RW[9]
19	OUT Endpoints Interrupt (OEPInt) The core sets this bit to indicate that an interrupt is pending on one of the OUT endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the OUT endpoint on which the interrupt occurred, and then read the corresponding Device OUT Endpoint-*n* Interrupt (DOEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DOEPINTn register to clear this bit.	Device only	R
18	IN Endpoints Interrupt (IEPInt) The core sets this bit to indicate that an interrupt is pending on one of the IN endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the IN	Device only	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	endpoint on which the interrupt occurred, and then read the corresponding Device IN Endpoint-*n* Interrupt (DIEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DIEPINTn register to clear this bit.		
17	Endpoint Mismatch Interrupt (EPMis) Note: This interrupt is valid only in shared FIFO operation. ndicates that an IN token has been received for a non-periodic endpoint, but the data for another endpoint is present in the top of the Non-periodic Transmit FIFO and the IN endpoint mismatch count programmed by the application has expired.	Device only	RW[10]
16	Restore Done Interrupt (RstrDoneInt) The core sets this bit to indicate that the restore command after Hibernation was completed by the core. The core continues from Suspended state into the mode dictated by PCGCCTL.RestoreMode bits. This bit is valid only when Hibernation feature is enabled (OTG_EN_PWROPT=2)	Host and Device mode	RW[11]
15	End of Periodic Frame Interrupt (EOPF) Indicates that the period specified in the Periodic Frame Interval bits of the Device Configuration register (DCFG.PerFrInt) has been reached in the current microframe.	Device only	RW[12]
14	Isochronous OUT Packet Dropped Interrupt (ISOOutDrop) The core sets this bit when it fails to write an isochronous OUT packet into the RxFIFO because the RxFIFO does not have enough space to accommodate a maximum packet size packet for the isochronous OUT endpoint.	Device only	RW[13]
13	Enumeration Done (EnumDone) The core sets this bit to indicate that speed enumeration is complete. The application must read the Device Status (DSTS) register to obtain the enumerated speed.	Device only	RW[14]
12	USB Reset (USBRst) The core sets this bit to indicate that a reset is detected on the USB.	Device only	RW[15]
11	USB Suspend (USBSusp) The core sets this bit to indicate that a suspend was detected on the USB. The core enters the Suspended state when there is no activity on the utmi_linestate signal for an extended period of time.	Device only	RW[16]
10	Early Suspend (ErlySusp) The core sets this bit to indicate that an Idle state has been detected on the USB for 3 ms.	Device only	RW[17]

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9	I2C Interrupt (I2CINT) The core sets this interrupt when I2C access is completed on the I 2C interface. This Bits is used only if the I2C interface was enabled. Otherwise, reads return 0.	Host and Device	RW[18]
8	ULPI Carkit Interrupt (ULPICKINT) This Bits is used only if the Carkit interface was enabled. Otherwise, reads return 0.	Host and Device	RW[19]
7	Global OUT NAK Effective (GOUTNakEff) Indicates that the Set Global OUT NAK bit in the Device Control register (DCTL.SGOUTNak), set by the application, has taken effect in the core. This bit can be cleared by writing the Clear Global OUT NAK bit in the Device Control register (DCTL.CGOUTNak).	Device only	R
6	Global IN Non-Periodic NAK Effective (GINNakEff) Indicates that the Set Global Non-periodic IN NAK bit in the Device Control register (DCTL.SGNPInNak), set by the application, has taken effect in the core. That is, the core has sampled the Global IN NAK bit set by the application. This bit can be cleared by clearing the Clear Global Non- periodic IN NAK bit in the Device Control register (DCTL.CGNPInNak). This interrupt does not necessarily mean that a NAK handshake is sent out on the USB. The STALL bit takes precedence over the NAK bit.	Device only	R
5	Non-Periodic TxFIFO Empty (NPTxFEmp) This interrupt is valid only when OTG_EN_DED_TX_FIFO = 0. This interrupt is asserted when the Non-periodic TxFIFO is either half or completely empty, and there is space for at least one entry to be written to the Non-periodic Transmit Request Queue. The half or completely empty status is determined by the Non-periodic TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl).	Host and Device	R
4	RxFIFO Non-Empty (RxFLvl) Indicates that there is at least one packet pending to be read from the RxFIFO.	Host and Device	R
3	Start of (micro)Frame (Sof) In Host mode, the core sets this bit to indicate that an SOF (FS), micro-SOF (HS), or Keep-Alive (LS) is transmitted on the USB. The application must write a 1 to this bit to clear the interrupt. In Device mode, in the core sets this bit to indicate that an SOF token has been received on the USB. The application can read the Device Status register to get the current	Host and Device	RW[20]

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	(micro)frame number. This interrupt is seen only when the core is operating at either HS or FS. Note: This register may return 1'b1 if read immediately after power on reset. If the register bit reads 1'b1 immediately after power on reset it does not indicate that an SOF has been sent (in case of host mode) or SOF has been received (in case of device mode). The read value of this interrupt is valid only after a valid connection between host and device is established. If the bit is set after power on reset the application can clear the bit.		
2	OTG Interrupt (OTGInt) The core sets this bit to indicate an OTG protocol event. The application must read the OTG Interrupt Status (GOTGINT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the GOTGINT register to clear this bit.	Host and Device	R
1	Mode Mismatch Interrupt (ModeMis) The core sets this bit when the application is trying to access: A Host mode register, when the core is operating in Device mode A Device mode register, when the core is operating in Host mode The register access is completed on the AHB with an OKAY response, but is ignored by the core internally and does not affect the operation of the core.	Host and Device	RW[21]
0	Current Mode of Operation (CurMod) Indicates the current mode. 1'b0: Device mode 1'b1: Host mode	Host and Device	R

Note:

[1]_[21]: This bits will operate with Write set , self clear function.

33.6.2.7 Interrupt Mask Register (GINTMSK,0x018)

	GINTMSK																Base + 0x018															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WkUpInt	SessReqInt	DisconnInt	ConIDStsChng	LPM_Int	PTxFEmp	HChInt	PrtInt	ResetDet	FetSusp	incomplP	incomplSOIN	OEPInt	IEPInt	EPMis	RstrDoneInt	EOPF	ISOOutDrop	EnumDone	USBRst	USBSusp	ErlySusp	I2CINT	ULPICKINT	GOUTNakEff	GINNakEff	NPTxFEmp	RxFLvl	Sof	OTGInt	ModeMis	CurMod
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	Mode	R/W
31	Resume/Remote Wakeup Detected Interrupt Mask (WkUpIntMsk)	Host and Device	RW
30	Session Request/New Session Detected Interrupt Mask (SessReqIntMsk)	Host and Device	RW
29	Disconnect Detected Interrupt Mask (DisconnIntMsk)	Host Only	RW
28	Connector ID Status Change Mask (ConIDStsChngMsk)	Host and Device	RW
27	LPM Transaction Received Interrupt Mask (LPM_IntMsk)	Host and Device	RW
26	Periodic TxFIFO Empty Mask (PTxFEmpMsk)	Host Only	RW
25	Host Channels Interrupt Mask (HChIntMsk)	Host Only	RW
24	Host Port Interrupt Mask (PrtIntMsk)	Host Only	RW
23	Reset Detected Interrupt Mask (ResetDetMsk)	Device Only	RW
22	Data Fetch Suspended Mask (FetSuspMsk)	Device Only	RW
21	Incomplete Periodic Transfer Mask (incomplPMsk) Incomplete Isochronous OUT Transfer Mask (incompISOOUTMsk)	Host only Device only	RW
20	Incomplete Isochronous IN Transfer Mask (incompISOINMsk) This bit is enabled only when device periodic endpoints are enabled in Dedicated TxFIFO mode.	Device only	RW
19	OUT Endpoints Interrupt Mask (OEPIntMsk)	Device only	RW
18	IN Endpoints Interrupt Mask (IEPIntMsk)	Device only	RW
17	Endpoint Mismatch Interrupt Mask (EPMisMsk)	Device only	RW
16	Restore Done Interrupt Mask (RstrDoneIntMsk) This Bits is valid only when Hibernation feature is enabled (OTG_EN_PWROPT=2).	Host and Device mode	RW
15	End of Periodic Frame Interrupt Mask (EOPFMsk)	Device only	RW
14	Isochronous OUT Packet Dropped Interrupt Mask (ISOOutDropMsk)	Device only	RW
13	Enumeration Done Mask (EnumDoneMsk)	Device only	RW
12	USB Reset Mask (USBRstMsk)	Device only	RW
11	USB Suspend Mask (USBSuspMsk)	Device only	RW
10	Early Suspend Mask (ErlySuspMsk)	Device only	RW
9	I^2C Interrupt Mask (I2CIntMsk)	Host and Device	RW
8	ULPI Carkit Interrupt Mask (ULPICKINTMsk) I^2C Carkit Interrupt Mask (I2CCKINTMsk)	Host and Device	RW
7	Global OUT NAK Effective Mask (GOUTNakEffMsk)	Device only	RW
6	Global Non-periodic IN NAK Effective Mask (GINNakEffMsk)	Device only	RW
5	Non-periodic TxFIFO Empty Mask (NPTxFEmpMsk)	Host and Device	RW
4	Receive FIFO Non-Empty Mask (RxFLvlMsk)	Host and Device	RW
3	Start of (micro)Frame Mask (SofMsk)	Host and Device	RW
2	OTG Interrupt Mask (OTGIntMsk)	Host and Device	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	Mode Mismatch Interrupt Mask (ModeMisMsk)	Host and Device	RW
0	Reserved	Host and Device	R

33.6.2.8 Receive Status Debug Read/Status Read and Pop Registers (GRXSTSR/GRXSTSP)

when host mode:

	GRXSTSR/GRXSTSP																Base + 0x01C/Base + 0x020															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											PktSts				DPID	BCnt												ChNum			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:21	Reserved	R
20:17	Packet Status (PktSts) 4'b0010: IN data packet received 4'b0011: IN transfer completed (triggers an interrupt) 4'b0101: Data toggle error (triggers an interrupt) 4'b0111: Channel halted (triggers an interrupt) Others: Reserved	R
16:15	Data PID (DPID) Indicates the Data PID of the received packet	R
14:4	Byte Count (BCnt) Indicates the byte count of the received IN data packet.	R
3:0	Channel Number (ChNum) Indicates the channel number to which the current received packet belongs.	R

when device mode:

	GRXSTSR/GRXSTSP																Base + 0x01C/Base + 0x020															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							FN				PktSts				DPID	BCnt												EPNum			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	R/W
31:25	Reserved	R
24:21	Frame Number (FN) This is the least significant 4 bits of the (micro)frame number in which the packet is received on the USB. This Bits is supported only when isochronous OUT endpoints are supported.	R
20:17	Packet Status (PktSts) Indicates the status of the received packet 4'b0001: Global OUT NAK (triggers an interrupt) 4'b0010: OUT data packet received 4'b0011: OUT transfer completed (triggers an interrupt) 4'b0100: SETUP transaction completed (triggers an interrupt) 4'b0110: SETUP data packet received Others: Reserved	R
16:15	Data PID (DPID) Indicates the Data PID of the received OUT data packet 2'b00: DATA0 2'b10: DATA1 2'b01: DATA2 2'b11: MDATA	R
14:4	Byte Count (BCnt) Indicates the byte count of the received data packet.	R
3:0	Endpoint Number (EPNum) Indicates the endpoint number to which the current received packet belongs.	R

33.6.2.9 Receive FIFO Size Register (GRXFSIZ,0x024)

	GRXFSIZ																													Base + 0x024	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																RxFDep															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	Reserved	R
15:0	RxFIFO Depth (RxFDep) This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 3648.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

33.6.2.10 Non-Periodic Transmit FIFO Size Register (GNPTXFSIZ,0x028)

	GNPTXFSIZ																Base + 0x028															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NPTxFDep																NPTxFStAddr															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	Non-periodic TxFIFO Depth (NPTxFDep) For host mode, this Bits is always valid. For Device mode, this Bits is invalid. This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 3648	R/RW
15:0	Non-periodic Transmit RAM Start Address (NPTxFStAddr) For host mode, this Bits is always valid. This Bits contains the memory start address for Non-periodic Transmit FIFO RAM. The application can write a new value in this Bits. Programmed values must not exceed the power-on value set	RW

33.6.2.11 Non-Periodic Transmit FIFO/Queue Status Register (GNPTXSTS,0x02C)

	GNPTXSTS																Base + 0x02C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NPTxQTop								NPTxQSpcAvail								NPTxFSpcAvail															
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:24	Top of the Non-periodic Transmit Request Queue (NPTxQTop) Entry in the Non-periodic Tx Request Queue that is currently being processed by the MAC. Bits [30:27]: Channel/endpoint number Bits [26:25]: 2'b00: IN/OUT token 2'b01: Zero-length transmit packet (device IN/host OUT) 2'b10: PING/CSPLIT token	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	2'b11: Channel halt command Bit [24]: Terminate (last entry for selected channel/endpoint)	
23:16	Non-periodic Transmit Request Queue Space Available (NPTxQSpcAvail) Indicates the amount of free space available in the Non-periodic Transmit Request Queue. This queue holds both IN and OUT requests in Host mode. Device mode has only IN requests. 8'h0: Non-periodic Transmit Request Queue is full 8'h1: 1 location available 8'h2: 2 locations available n : n locations available (0≤n≤8) Others: Reserved	R
15:0	Non-periodic TxFIFO Space Avail (NPTxFSpcAvail) Indicates the amount of free space available in the Non-periodic TxFIFO. Values are in terms of 32-bit words. 16'h0: Non-periodic TxFIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'h*n*: *n* words available (where 0≤n≤32,768) 16'h8000: 32,768 words available Others: Reserved	R

33.6.2.12 User HW Config1 Register (GHWCFG1,0x044)

	GHWCFG1																Base + 0x044															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	epdir																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:0	Endpoint Direction (epdir) This 32-bit Bits uses two bits per endpoint to determine the endpoint direction. Endpoint Bits [31:30]: Endpoint 15 direction Bits [29:28]: Endpoint 14 direction ... Bits [3:2]: Endpoint 1 direction Bits[1:0]: Endpoint 0 direction (always BIDIR) Direction 2'b00: BIDIR (IN and OUT) endpoint	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	2'b01: IN endpoint 2'b10: OUT endpoint 2'b11: Reserved This Bits is configured using "Name: OTG_EP_DIR_1(n)".	

33.6.2.13 User HW Config2 Register (GHWCFG2,0x048)

	GHWCFG2																Base + 0x048													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	otgenicusb	TknQDepth					PTxQDepth		NPTxQDepth		Reserved	MultiProcIntrpt	DynFifoSizing	PerioSupport	NumHstChnl		NumDevEps						FSPhyType		HSPhyType		SingPnt	OtgArch		OtgMode		
RST	?	?	?	?	?	?	?	?	?	?	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31	OTG_ENABLE_IC_USB(otgenicusb) IC_USB mode specified for mode of operation (parameter OTG_ENABLE _IC_USB) in coreConsultant. To choose IC_USB_MODE, both OTG_FSPHY_INTERFACE and OTG_ENABLE_IC_USB must be 1.	R
30:26	Device Mode IN Token Sequence Learning Queue Depth (TknQDepth) Range: 0-30 This Bits is configured using "Name: OTG_TOKEN_QUEUE_DEPTH".	R
25:24	Host Mode Periodic Request Queue Depth (PTxQDepth) 2'b00: 2 2'b01: 4 2'b10: 8 2'b11: 16 This Bits is configured using parameter "Name: OTG_PERIO_TX_QUEUE_DEPTH"	R
23:22	Non-periodic Request Queue Depth (NPTxQDepth) 2'b00: 2 2'b01: 4 2'b10: 8 Others: Reserved This Bits is configured using parameter "Name: OTG_NPERIO_TX_QUEUE_DEPTH".	R
21	Reserved	R
20	Multi Processor Interrupt Enabled (MultiProcIntrpt) 1'b0: No	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	1'b1: Yes This Bits is configured using parameter "Name: OTG_MULTI_PROC_INTRPT".	
19	Dynamic FIFO Sizing Enabled (DynFifoSizing) 1'b0: No 1'b1: Yes This Bits is configured using parameter "Name: OTG_DFIFO_DYNAMIC".	R
18	Periodic OUT Channels Supported in Host Mode (PerioSupport) 1'b0: No 1'b1: Yes This Bits is configured using parameter "Name: OTG_EN_PERIO_HOST".	R
17:14	Number of Host Channels (NumHstChnl) Indicates the number of host channels supported by the core in Host mode. The range of this Bits is 0-15: 0 specifies 1 channel, 15 specifies 16 channels. This Bits is configured using parameter "Name: OTG_NUM_HOST_CHAN".	R
13:10	Number of Device Endpoints (NumDevEps) Indicates the number of device endpoints supported by the core in Device mode in addition to control endpoint 0. The range of this Bits is 1-15. This Bits is configured using parameter "Name: OTG_NUM_EPS".	R
9:8	Full-Speed PHY Interface Type (FSPhyType) 2'b00: Full-speed interface not supported 2'b01: Dedicated full-speed interface 2'b10: FS pins shared with UTMI+ pins 2'b11: FS pins shared with ULPI pins This Bits is configured using parameter "Name: OTG_FSPHY_INTERFACE".	R
7:6	High-Speed PHY Interface Type (HSPhyType) 2'b00: High-Speed interface not supported 2'b01: UTMI+ 2'b10: ULPI 2'b11: UTMI+and ULPI This Bits is configured using parameter "Name: OTG_HSPHY_INTERFACE".	R
5	Point-to-Point (SingPnt) 1'b0: Multi-point application (hub and split support) 1'b1: Single-point application (no hub and no split support) This Bits is configured using parameter "Name: OTG_SINGLE_POINT".	R
4:3	Architecture (OtgArch) 2'b00: Slave-Only 2'b01: External DMA 2'b10: Internal DMA Others: Reserved This Bits is configured using parameter "Name: OTG_ARCHITECTURE".	R
2:0	Mode of Operation (OtgMode) 3'b000: HNP- and SRP-Capable OTG (Host and Device) 3'b001: SRP-Capable OTG (Host and Device)	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	3'b010: Non-HNP and Non-SRP Capable OTG (Host and Device) 3'b011: SRP-Capable Device 3'b100: Non-OTG Device 3'b101: SRP-Capable Host 3'b110: Non-OTG Host Others: Reserved This Bits is configured using parameter "Name: OTG_MODE".	

33.6.2.14 User HW Config3 Register (GHWCFG3,0x04C)

																													Base + 0x04C	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DfifoDepth																OTG_ENABLE_LPM	OTG_BC_SUPPORT	OTG_ENABLE_HSIC	OTG_ADP_SUPPORT	RstType	OptFeature	VndctlSupt	I2CIntSel	OtgEn	PktSizeWidth			XferSizeWidth			
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	DFIFO Depth (DfifoDepth minus EP_LOC_CNT) This value is in terms of 32-bit words. Minimum value is 32 Maximum value is 32,768 This Bits is configured using parameter "Name: OTG_DFIFO_DEPTH" and EP_LOC_CNT. For more information on EP_LOC_CNT, see "Endpoint Information Controller (EPINFO_CTL)".	R
15	OTG_ENABLE_LPM LPM mode specified for Mode of Operation (parameter OTG_ENABLE_LPM) in coreConsultant configuration.	R
14	OTG_BC_SUPPORT This bit indicates the HS OTG controller support for Battery Charger. 0 - No Battery Charger Support 1 - Battery Charger support present.	R
13	OTG_ENABLE_HSIC HSIC mode specified for Mode of Operation in coreConsultant configuration (parameter OTG_ENABLE_HSIC). Value Range: 0-1 1: HSIC-capable with shared UTMI PHY interface 0: Non-HSIC-capable Parameter Name: OTG_ENABLE_HSIC	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Dependencies: OTG_HSPHY_INTERFACE Default: Non-HSIC-capable	
12	OTG_ADP_SUPPORT This bit indicates whether ADP logic is present within or external to the HS OTG controller 0 - No ADP logic present with HS OTG controller 1- ADP logic is present along with HS OTG controller.	R
11	Reset Style for Clocked always Blocks in RTL (RstType) 1'b0: Asynchronous reset is used in the core 1'b1: Synchronous reset is used in the core This Bits is configured using parameter "Name: OTG_SYNC_RESET_TYPE".	R
10	Optional Features Removed (OptFeature) Indicates whether the User ID register, GPIO interface ports, and SOF toggle and counter ports were removed for gate count optimization by enabling Remove Optional Features? during coreConsultant configuration. 1'b0: No 1'b1: Yes This Bits is configured using parameter "Name: OTG_RM_OPT_FEATURES".	R
9	Vendor Control Interface Support (VndctlSupt) 1'b0: Vendor Control Interface is not available on the core. 1'b1: Vendor Control Interface is available. This Bits is configured using parameter "Name: OTG_VENDOR_CTL_INTERFACE".	R
8	I^2C Selection (I2CIntSel) 1'b0: I 2C Interface is not available on the core. 1'b1: I 2C Interface is available on the core. This Bits is configured using parameter "Name: OTG_I2C_INTERFACE".	R
7	OTG Function Enabled (OtgEn) The application uses this bit to indicate the DWC_otg core's OTG capabilities. 1'b0: Not OTG capable 1'b1: OTG Capable This Bits is configured using parameter "Name: OTG_MODE".	R
6:4	Width of Packet Size Counters (PktSizeWidth) 3'b000: 4 bits 3'b001: 5 bits 3'b010: 6 bits 3'b011: 7 bits 3'b100: 8 bits 3'b101: 9 bits 3'b110: 10 bits Others: Reserved This Bits is configured using parameter "Name: OTG_PACKET_COUNT_WIDTH".	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

3:0	Width of Transfer Size Counters (XferSizeWidth) 4'b0000: 11 bits 4'b0001: 12 bits ... 4'b1000: 19 bits Others: Reserved This Bits is configured using parameter "Name: OTG_TRANS_COUNT_WIDTH".	R

33.6.2.15 User HW Config4 Register (GHWCFG4,0x050)

	GHWCFG4																Base + 0x050													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SGDMA	SGDMACFG	INEps				DedFifoMode	SessEndFltr	BValidFltr	AValidFltr	VBusValidFltr	IddgFltr	NumCtlEps				PhyDataWidth		Reserved								AhbFreq	enPartPwrDn	NumDevPerioEps			
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0	0	0	0	?	?	?	?	?	?

Bits	Description	R/W
31	Scatter/Gather DMA(SGDMA) 1'b1: Dynamic configuration This Bits is configured using parameter "Name: OTG_EN_DESC_DMA" .	R
30	Scatter/Gather DMA configuration(SGDMACFG) 1'b0: Non-Scatter/Gather DMA configuration 1'b1: Scatter/Gather DMA configuration This Bits is configured using parameter "Name: OTG_EN_DESC_DMA".	R
29:26	Number of Device Mode IN Endpoints Including Control Endpoints (INEps) Range 0 -15 0:1 IN Endpoint 1:2 IN Endpoints .... 15:16 IN Endpoints This Bits is configured using parameter "Name: OTG_NUM_IN_EPS".	R
25	Enable Dedicated Transmit FIFO for device IN Endpoints (DedFifoMode) 1'b0: Dedicated Transmit FIFO Operation not enabled. 1'b1: Dedicated Transmit FIFO Operation enabled. This Bits is configured using parameter "Name: OTG_EN_DED_TX_FIFO".	R
24	session_end Filter Enabled (SessEndFltr) 1'b0: No filter 1'b1: Filter This Bits is configured using parameter "Name:	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	OTG_EN_SESSIONEND_FILTER"	
23	"b_valid" Filter Enabled (BValidFltr) 1'b0: No filter 1'b1: Filter This Bits is configured using parameter "Name: OTG_EN_B_VALID_FILTER".	R
22	"a_valid" Filter Enabled (AValidFltr) 1'b0: No filter 1'b1: Filter This Bits is configured using parameter "Name: OTG_EN_A_VALID_FILTER".	R
21	"vbus_valid" Filter Enabled (VBusValidFltr) 1'b0: No filter 1'b1: Filter This Bits is configured using parameter "Name: OTG_EN_VBUSVALID_FILTER".	R
20	"iddig" Filter Enable (IddgFltr) 1'b0: No filter 1'b1: Filter This Bits is configured using parameter "Name: OTG_EN_IDDIG_FILTER".	R
19:16	Number of Device Mode Control Endpoints in Addition to Endpoint 0 (NumCtlEps) Range: 0-15 This Bits is configured using parameter "Name: OTG_NUM_CRL_EPS".	R
15:14	UTMI+ PHY/ULPI-to-Internal UTMI+ Wrapper Data Width (PhyDataWidth) When a ULPI PHY is used, an internal wrapper converts ULPI to UTMI+. 2'b00: 8 bits 2'b01: 16 bits 2'b10: 8/16 bits, software selectable Others: Reserved This Bits is configured using parameter "Name: OTG_HSPHY_DWIDTH".	R
13:6	Reserved	R
6	Enable Hibernation 1'b0: Hibernation feature not enabled 1'b1: Hibernation feature enabled This Bits is configured using parameter "Name: OTG_EN_PWROPT".	R
5	Minimum AHB Frequency Less Than 60 MHz (AhbFreq) 1'b0: No 1'b1: Yes This Bits is configured using parameter "Name: OTG_MIN_AHB_FREQ_LESSTHAN_60".	R
4	Enable Partial Power Down(enPartPwrDn) 1'b0: Partial Power Down Not Enabled 1'b1: Partial Power Down Enabled This Bits is configured using parameter "Name: OTG_EN_PWROPT".	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

3:0	Number of Device Mode Periodic IN Endpoints (NumDevPerioEps) Range: 0-15 This Bits is configured using parameter "Name: OTG_NUM_PERIO_EPS".	R

33.6.2.16 DFIFO Software Config Register (GDFIFOCFG,0x05C)

	GDFIFOCFG																Base + 0x05C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPInfoBaseAddr																GDFIFOCfg															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	Mode	R/W
31:16	EPInfoBaseAddr This Bits provides the start address of the EP info controller.	Host and Device	RW
15:0	GDFIFOCfg This Bits is for dynamic programming of the DFIFO Size. This value takes effect only when the application programs a non zero value to this register. The value programmed must conform to the guidelines described in "FIFO RAM Allocation" in the Programming Guide. The DWC_otg core does not have any corrective logic if the FIFO sizes are programmed incorrectly.	Host and Device	RW

33.6.2.17 Host Periodic Transmit FIFO Size Register (HPTXFSIZ,0x100)

	HPTXFSIZ																Base + 0x100															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PTxFSize																PTxFStAddr															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	Host Periodic TxFIFO Depth (PTxFSize) This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 3648	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

15:0	Host Periodic TxFIFO Start Address (PTxFStAddr) The power-on reset value of this register is the sum of the Largest Rx Data FIFO Depth and Largest Non-periodic Tx Data FIFO Depth specified .These parameters are: In shared FIFO operation:- OTG_RX_DFIFO_DEPTH(3648) + OTG_TX_NPERIO_DFIFO_DEPTH(1024) In dedicated FIFO mode:- OTG_RX_DFIFO_DEPTH(3648) + OTG_TX_HNPERIO_DFIFO_DEPTH(3648)	R/RW

33.6.2.18 Device IN Endpoint Transmit FIFO Size Register: (DIEPTXFn,0x104+(FIFO_num - 1)*0x04)

	DIEPTXFn																Base + 0x104+(FIFO_num - 1)*0x4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INEPnTxFDep																INEPnTxFStAddr															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	IN Endpoint TxFIFO Depth (INEPnTxFDep) This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 3648	RW
15:0	IN Endpoint FIFO*n* Transmit RAM Start Address (INEPnTxFStAddr) This Bits contains the memory start address for IN endpoint Transmit FIFOn (0 < n <= 15). The power-on reset value of this register is calculated according to the following formula: OTG_RX_DFIFO_DEPTH + SUM of OTG_TX_DINEP_DFIFO_DEPTH_'x' (where x = 0 to n - 1) If at POR the calculated value (C) exceeds 65535, then the Reset value becomes Reset Value(A) = (C - 65536). Example: If start address of IN endpoint FIFO 1 is OTG_RX_DFIFO_DEPTH + OTG_TX_DINEP_DFIFO_DEPTH_ 0 and start address of IN endpoint FIFO 2 is OTG_RX_DFIFO_DEPTH + OTG_TX_DINEP_DFIFO_DEPTH_ 0 + OTG_TX_DINEP_DFIFO_DEPTH_ 1.	R/RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

33.6.2.19 Host Configuration Register (HCFG,0x400)

	HCFG																Base + 0x400													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ModeChTimEn	Reserved				PerSchedEna	FrListEn		DescDMA	Reserved							ResValid								Ena32KHzS	Reserved				FSLSSupp	FSLSPclkSel	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Mode Change Ready Timer Enable (ModeChTimEn) This bit is used to enable or disable the host core to wait for 200 PHY clock cycles at the end of Resume to change the opmode signal to the PHY to 00 after Suspend or LPM. 1'b0: The Host core waits for either 200 PHY clock cycles or a linestate of SE0 at the end of resume to change the opmode from 2'b10 to 2'b00. 1'b1: The Host core waits only for a linestate of SE0 at the end of resume to change the opmode from 2'b10 to 2'b00.	RW
30:27	Reserved	R
26	Enable Periodic Scheduling (PerSchedEna) Applicable in Scatter/Gather DMA mode only. Enables periodic scheduling within the core. Initially, the bit is reset. The core will not process any periodic channels. As soon as this bit is set, the core will get ready to start scheduling periodic channels. In non Scatter/Gather DMA mode, this bit is reserved.	RW
25:24	Frame List Entries (FrListEn). The value in the register specifies the number of entries in the Frame list. This Bits is valid only in Scatter/Gather DMA mode. 2'b00: 8 Entries 2'b01:16 Entries 2'b10: 32 Entries 2'b11: 64 Entries In modes other than Scatter/Gather DMA mode, these bits are reserved.	RW
23	Enable Scatter/gather DMA in Host mode (DescDMA) When the Scatter/Gather DMA option selected during configuration of the RTL, the application can set this bit during initialization to enable the Scatter/Gather DMA operation. NOTE: This bit must be modified only once after a reset. The following combinations are available for programming: GAHBCFG.DMAEn=0, HCFG.DescDMA=0 => Slave mode GAHBCFG.DMAEn=0, HCFG.DescDMA=1 => Invalid GAHBCFG.DMAEn=1, HCFG.DescDMA=0 => Buffered DMA mode GAHBCFG.DMAEn=1, HCFG.DescDMA=1 => Scatter/Gather DMA mode	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	In non Scatter/Gather DMA mode, this bit is reserved.	
22:16	Reserved	RW
15:8	Resume Validation Period (ResValid) This Bits is effective only when HCFG.Ena32KHzS is set. It controls the resume period when the core resumes from suspend. The core counts the ResValid number of clock cycles to detect a valid resume when this is set.	RW
7	Enable 32-KHz Suspend Mode (Ena32KHzS) This bit can only be set if the USB 1.1 Full-Speed Serial Transceiver Interface has been selected. If USB 1.1 Full-Speed Serial Transceiver Interface has not been selected, this bit must be zero. When the USB 1.1 Full-Speed Serial Transceiver Interface is chosen and this bit is set, the core expects the 48-MHz PHY clock to be switched to 32 KHz during a suspend.	RW
6:3	Reserved	R
2	FS- and LS-Only Support (FSLSSupp) The application uses this bit to control the core's enumeration speed. Using this bit, the application can make the core enumerate as a FS host, even if the connected device supports HS traffic. Do not make changes to this Bits after initial programming. 1'b0: HS/FS/LS, based on the maximum speed supported by the connected device 1'b1: FS/LS-only, even if the connected device can support HS	RW
1:0	FS/LS PHY Clock Select (FSLSPclkSel) When the core is in FS Host mode 2'b00: Internal PHY clock is running at 30/60 MHZ (For UTMI+/ULPI PHY Interfaces) 2'b01: Internal PHY clock is running at 48MHZ (For 1.1 FS transceiver Interface) Others: Reserved When the core is in LS Host mode 2'b00: Internal PHY clock is running at 30/60 MHZ (For UTMI+/ULPI PHY Interfaces) 2'b10: Internal PHY clock is running at 6 MHZ and the external clock is running at 48MHZ. When you select a 6 MHz clock during LS Mode, you must do a soft reset (for 1.1 FS transceiver Interface) Others: Reserved Notes: When Core in FS mode, the internal and external clocks have the same frequency. When Core in LS mode, If FSLSPclkSel = 2'b00: Internal and external clocks have the same frequency If FSLSPclkSel = 2'b10: Internal clock is divided by eight version of external 48 MHz clock (utmifs_clk).	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

33.6.2.20 Host Frame Interval Register (HFIR,0x404)

	HFIR																													Base + 0x404	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															HFIRRldCtrl	FrInt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0	0	0

Bits	Description	R/W
31:17	Reserved	R
16	Reload Control (HFIRRldCtrl) This bit allows dynamic reloading of the HFIR register during runtime. 1'b0: The HFIR cannot be reloaded dynamically 1'b1: the HFIR can be dynamically reloaded during runtime. This bit needs to be programmed during initial configuration and its value must not be changed during runtime.	RW
15:0	Frame Interval (FrInt) The value that the application programs to this Bits specifies the interval between two consecutive SOFs (FS) or micro-SOFs (HS) or Keep-Alive tokens (LS). This Bits contains the number of PHY clocks that constitute the required frame interval. The default value set in this Bits for a FS operation when the PHY clock frequency is 60 MHz. The application can write a value to this register only after the Port Enable bit of the Host Port Control and Status register (HPRT.PrtEnaPort) has been set. If no value is programmed, the core calculates the value based on the PHY clock specified in the FS/LS PHY Clock Select Bits of the Host Configuration register (HCFG.FSLSPclkSel). 125 μs * (PHY clock frequency for HS) 1 ms * (PHY clock frequency for FS/LS)	RW

33.6.2.21 Host Frame Number/Frame Time Remaining Register (HFNUM,0x408)

	HFNUM																													Base + 0x408	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FrRem																FrNum															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	R/W
31:16	Frame Time Remaining (FrRem) Indicates the amount of time remaining in the current microframe (HS) or frame (FS/LS), in terms of PHY clocks. This Bits decrements on each PHY clock. When it reaches zero, this Bits is reloaded with the value in the Frame Interval register and a new SOF is transmitted on the USB.	R
15:0	Frame Number (FrNum) This Bits increments when a new SOF is transmitted on the USB, and is reset to 0 when it reaches 16'h3FFF.	R

33.6.2.22 Host Periodic Transmit FIFO/Queue Status Register (HPTXSTS,0x410)

	HPTXSTS																Base + 0x410													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PTxQTop								PTxQSpcAvail								PTxFSpcAvail															
RST	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:24	Top of the Periodic Transmit Request Queue (PTxQTop) This indicates the entry in the Periodic Tx Request Queue that is currently being processes by the MAC. This register is used for debugging. Bit [31]: Odd/Even (micro)frame 1'b0: send in even (micro)frame 1'b1: send in odd (micro)frame Bits [30:27]: Channel/endpoint number Bits [26:25]: Type 2'b00: IN/OUT 2'b01: Zero-length packet 2'b10: CSPLIT 2'b11: Disable channel command Bit [24]: Terminate (last entry for the selected channel/endpoint)	R
23:16	Periodic Transmit Request Queue Space Available (PTxQSpcAvail) Indicates the number of free locations available to be written in the Periodic Transmit Request Queue. This queue holds both IN and OUT requests. 8'h0: Periodic Transmit Request Queue is full 8'h1: 1 location available 8'h2: 2 locations available n : n locations available (0 ≤n ≤16)	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Others: Reserved	
15:0	Periodic Transmit Data FIFO Space Available (PTxFSpcAvail) Indicates the number of free locations available to be written to in the Periodic TxFIFO. Values are in terms of 32-bit words 16'h0: Periodic TxFIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'hn: n words available (where 0 ≤n ≤32,768) 16'h8000: 32,768 words available Others: Reserved	R

33.6.2.23 Host All Channels Interrupt Register (HAINT,0x414)

	HAINT																Base + 0x414													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																HAINT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	Reserved	R
15:0	Channel Interrupts (HAINT) One bit per channel: Bit 0 for Channel 0, bit 15 for Channel 15	R

33.6.2.24 Host All Channels Interrupt Mask Register (HAINTMSK,0x418)

	HAINTMSK																Base + 0x418													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																HAINTMsk															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	Reserved	R
15:0	Channel Interrupt Mask (HAINTMsk) One bit per channel: Bit 0 for channel 0, bit 15 for channel 15	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

33.6.2.25 Host Port Control and Status Register (HPRT,0x440)

	HPRT																Base + 0x440															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													PrtSpd		PrtTstCtl				PrtPwr	PrtLnSts		Reserved	PrtRst	PrtSusp	PrtRes	PrtOvrCurrChng	PrtOvrCurrAct	PrtEnChng	PrtEna	PrtConnDet	PrtConnSts
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:19	Reserved	R
18:17	Port Speed (PrtSpd) Indicates the speed of the device attached to this port. 2'b00: High speed 2'b01: Full speed 2'b10: Low speed 2'b11: Reserved	R
16:13	Port Test Control (PrtTstCtl) The application writes a nonzero value to this Bits to put the port into a Test mode, and the corresponding pattern is signaled on the port. 4'b0000: Test mode disabled 4'b0001: Test_J mode 4'b0010: Test_K mode 4'b0011: Test_SE0_NAK mode 4'b0100: Test_Packet mode 4'b0101: Test_Force_Enable Others: Reserved For more information on moving the DWC_otg host core into test mode, see "Moving the Host Core to Test Mode" on page 89.	RW
12	Port Power (PrtPwr) The application uses this Bits to control power to this port (write 1'b1 to set to 1'b1 and write 1'b0 to set to 1'b0), and the core can clear this bit on an over current condition. 1'b0: Power off 1'b1: Power on	R
11:10	Port Line Status (PrtLnSts) Indicates the current logic level USB data lines Bit [10]: Logic level of D+ Bit [11]: Logic level of D-	R
9	Reserved	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

8	Port Reset (PrtRst) When the application sets this bit, a reset sequence is started on this port. The application must time the reset period and clear this bit after the reset sequence is complete. 1'b0: Port not in reset 1'b1: Port in reset To start a reset on the port, the application must leave this bit set for at least the minimum duration mentioned below, as specified in the USB 2.0 specification, Section 7.1.7.5. The application can leave it set for another 10 ms in addition to the required minimum duration, before clearing the bit, even though there is no maximum limit set by the USB standard. High speed: 50 ms Full speed/Low speed: 10 ms	RW
7	Port Suspend (PrtSusp) The application sets this bit to put this port in Suspend mode. The core only stops sending SOFs when this is set. To stop the PHY clock, the application must set the Port Clock Stop bit, which asserts the suspend input pin of the PHY. The read value of this bit reflects the current suspend status of the port. This bit is cleared by the core after a remote wakeup signal is detected or the application sets the Port Reset bit or Port Resume bit in this register or the Resume/Remote Wakeup Detected Interrupt bit or Disconnect Detected Interrupt bit in the Core Interrupt register (GINTSTS.WkUpInt or GINTSTS.DisconnInt, respectively). 1'b0: Port not in Suspend mode 1'b1: Port in Suspend mode	RW[1]
6	Port Resume (PrtRes) The application sets this bit to drive resume signaling on the port. The core continues to drive the resume signal until the application clears this bit. If the core detects a USB remote wakeup sequence, as indicated by the Port Resume/Remote Wakeup Detected Interrupt bit of the Core Interrupt register (GINTSTS.WkUpInt), the core starts driving resume signaling without application intervention and clears this bit when it detects a disconnect condition. The read value of this bit indicates whether the core is currently driving resume signaling. 1'b0: No resume driven 1'b1: Resume driven When LPM is enabled and the core is in the L1 (Sleep) state, setting this bit results in the following behavior: The core continues to drive the resume signal until a pre-determined time specified in the GLPMCFG.HIRD_Thres[3:0] Bits.	RW[2]

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	If the core detects a USB remote wakeup sequence, as indicated by the Port L1 Resume/Remote L1 Wakeup Detected Interrupt bit of the Core Interrupt register (GINTSTS.L1WkUpInt), the core starts driving resume signaling without application intervention and clears this bit at the end of the resume. The read value of this bit indicates whether the core is currently driving resume signaling. 1'b0: No resume driven 1'b1: Resume driven	
5	Port Overcurrent Change (PrtOvrCurrChng) The core sets this bit when the status of the Port Overcurrent Active bit (bit 4) in this register changes.	RW[3]
4	Port Overcurrent Active (PrtOvrCurrAct) Indicates the overcurrent condition of the port. 1'b0: No overcurrent condition 1'b1: Overcurrent condition	R
3	Port Enable/Disable Change (PrtEnChng) The core sets this bit when the status of the Port Enable bit [2] of this register changes.	RW[4]
2	Port Enable (PrtEna) A port is enabled only by the core after a reset sequence, and is disabled by an overcurrent condition, a disconnect condition, or by the application clearing this bit. The application cannot set this bit by a register write. It can only clear it to disable the port. This bit does not trigger any interrupt to the application. 1'b0: Port disabled 1'b1: Port enabled	RW[5]
1	Port Connect Detected (PrtConnDet) The core sets this bit when a device connection is detected to trigger an interrupt to the application using the Host Port Interrupt bit of the Core Interrupt register (GINTSTS.PrtInt). The application must write a 1 to this bit to clear the interrupt.	RW[6]
0	Port Connect Status (PrtConnSts) 0: No device is attached to the port. 1: A device is attached to the port.	R

Note:

[1] ,[2]: This bits will operate with Write set , self clear function.

[3] ,[4] ,[6]: This bits will operate with Self set , Write clear function.

[5]: This bits will operate with Write clear or read clear function.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

33.6.2.26 Host Channel-n Characteristics Register (HCCHARn,0x500+n*0x20)

	HCCHARn																Base + 0x500+n*0x20													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ChEna	ChDis	OddFrm	DevAddr	DevAddr						EC		EPType		LSpdDev	Reserved	EPDir	EPNum				MPS										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Channel Enable (ChEna) When Scatter/Gather mode is enabled 1'b0: Indicates that the descriptor structure is not yet ready. 1'b1: Indicates that the descriptor structure and data buffer with data is setup and this channel can access the descriptor. When Scatter/Gather mode is disabled This Bits is set by the application and cleared by the OTG host. 1'b0: Channel disabled 1'b1: Channel enabled	RW[1]
30	Channel Disable (ChDis) The application sets this bit to stop transmitting/receiving data on a channel, even before the transfer for that channel is complete. The application must wait for the Channel Disabled interrupt before treating the channel as disabled.	RW[2]
29	Odd Frame (OddFrm) This Bits is set (reset) by the application to indicate that the OTG host must perform a transfer in an odd (micro)frame. This Bits is applicable for only periodic (isochronous and interrupt) transactions. 1'b0: Even (micro)frame 1'b1: Odd (micro)frame This Bits is not applicable for Scatter/Gather DMA mode and need not be programmed by the application and is ignored by the core.	RW
28:22	Device Address (DevAddr) This Bits selects the specific device serving as the data source or sink.	RW
21:20	Multi Count (MC) / Error Count (EC) When the Split Enable bit of the Host Channel-n Split Control register (HCSPLTn.SpltEna) is reset (1'b0), this Bits indicates to the host the number of transactions that must be executed per microframe for this periodic endpoint. For non periodic transfers, this Bits is used only in DMA mode, and specifies the number packets to be fetched for this channel before the internal DMA engine changes aubitration. 2'b00: Reserved This Bits yields undefined results.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	2'b01: 1 transaction 2'b10: 2 transactions to be issued for this endpoint per microframe 2'b11: 3 transactions to be issued for this endpoint per microframe When HCSPLTn.SpltEna is set (1'b1), this Bits indicates the number of immediate retries to be performed for a periodic split transactions on transaction errors. This Bits must be set to at least 2'b01.	
19:18	Endpoint Type (EPType) Indicates the transfer type selected. 2'b00: Control 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt	RW
17	Low-Speed Device (LSpdDev) This Bits is set by the application to indicate that this channel is communicating to a low-speed device. The application must program this bit when a low speed device is connected to the host through an FS HUB. The HS OTG Host core uses this Bits to drive the XCVR_SELECT signal to 2'b11 while communicating to the LS Device through the FS hub. **Note:** In a peer to peer setup, the HS OTG Host core ignores this bit even if it is set by the application software.	RW
16	Reserved	R
15	Endpoint Direction (EPDir) Indicates whether the transaction is IN or OUT. 1'b0: OUT 1'b1: IN	RW
14:11	Endpoint Number (EPNum) Indicates the endpoint number on the device serving as the data source or sink.	RW
10:0	Maximum Packet Size (MPS) Indicates the maximum packet size of the associated endpoint.	RW

Note:

[1], [2]: This bits will operate with Write set , self clear function.

33.6.2.27 Host Channel-n Split Control Register (HCSPLTn,0x504+n*0x20)

	HCSPLTn																Base + 0x504+n*0x20															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SpltEna	Reserved														CompSplt	XactPos	HubAddr								PrtAddr						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	R/W
31	Split Enable (SpltEna) The application sets this Bits to indicate that this channel is enabled to perform split transactions.	RW
30:17	Reserved	R
16	Do Complete Split (CompSplt) The application sets this Bits to request the OTG host to perform a complete split trsnsaction.	RW
15:14	Transaction Position (XactPos) This Bits is used to determine whether to send all, first, middle, or last payloads with each OUT transaction. 2'b11: All. This is the entire data payload is of this transaction (which is less than or equal to 188 bytes). 2'b10: Begin. This is the first data payload of this transaction (which is larger than 188 bytes). 2'b00: Mid. This is the middle payload of this transaction (which is larger than 188 bytes). 2'b01: End. This is the last payload of this transaction (which is larger than 188 bytes).	RW
13:7	Hub Address (HubAddr) This Bits holds the device address of the transaction translator's hub.	RW
6:0	Port Address (PrtAddr) This Bits is the port number of the recipient transaction translator.	RW

33.6.2.28 Host Channel-n Interrupt Register (HCINTn,0x508+n*0x20)

	HCINTn																		Base + 0x508+n*0x20													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		DESC_LST_ROLLIntr	XCS_XACT_ERR	BNAIntr	DataTglErr	FrmOvrun	BblErr	XactErr	NYET	ACK	NAK	STALL	AHBErr	ChHltd	XferCompl
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:14	Reserved	R
13	Descriptor rollover interrupt (DESC_LST_ROLLIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core sets this bit when the corresponding channel's descriptor list rolls	RW[1]

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	over. For non Scatter/Gather DMA mode, this bit is reserved.	
12	Excessive Transaction Error (XCS_XACT_ERR) This bit is valid only when Scatter/Gather DMA mode is enabled. The core sets this bit when 3 consecutive transaction errors occurred on the USB bus. XCS_XACT_ERR will not be generated for Isochronous channels. For non Scatter/Gather DMA mode, this bit is reserved.	RW[2]
11	BNA (Buffer Not Available) Interrupt (BNAIntr) This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process. BNA will not be generated for Isochronous channels. For non Scatter/Gather DMA mode, this bit is reserved.	RW[3]
10	Data Toggle Error (DataTglErr) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[4]
9	Frame Overrun (FrmOvrun) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core	RW[5]
8	Babble Error (BblErr) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[6]
7	Transaction Error (XactErr) Indicates one of the following errors occurred on the USB. CRC check failure Timeout Bit stuff error False EOP In Scatter/Gather DMA mode, the interrupt due to this bit is not set.	RW[7]
6	NYET Response Received Interrupt (NYET) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[8]
5	ACK Response Received/Transmitted Interrupt (ACK) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[9]
4	NAK Response Received Interrupt (NAK) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[10]
3	STALL Response Received Interrupt (STALL) In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.	RW[11]
2	AHB Error (AHBErr)	RW[12]

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	This is generated only in DMA mode when there is an AHB error during AHB read/write. The application can read the corresponding channel's DMA address register to get the error address.	
1	Channel Halted (ChHltd) In non Scatter/Gather DMA mode, it indicates the transfer completed abnormally either because of any USB transaction error or in response to disable request by the application or because of a completed transfer. In Scatter/Gather DMA mode, this indicates that transfer completed due to any of the following EOL being set in descriptor AHB error Excessive transaction errors In response to disable request by the application Babble Stall	RW[13]
0	Transfer Completed (XferCompl) For Scatter/Gather DMA mode, it indicates that current descriptor processing got completed with IOC bit set in its descriptor. In non Scatter/Gather DMA mode, it indicates that Transfer completed normally without any errors.	RW[14]

Note:

[1],[2]: This bits will operate with Self set , write clear function.

33.6.2.29 Host Channel-n Interrupt Mask Register (HCINTMSKn,0x50C+n*0x20)

	HCINTMSKn																		Base + 0x50C+n*0x20											
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		ROLLIntrMsk	Reserved	BNAIntrMsk	DataTglErrMsk	DataTglErrMsk	BblErrMsk	XactErrMsk	NyetMsk	AckMsk	NakMsk	StallMsk	AHBErrMsk	ChHltdMsk	XferComplMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:14	Reserved	R
13	Descriptor rollover interrupt Mask register (DESC_LST_ROLLIntrMsk) This bit is valid only when Scatter/Gather DMA mode is enabled. In non Scatter/Gather DMA mode, this bit is reserved.	RW
12	Reserved	R
11	BNA (Buffer Not Available) Interrupt mask register (BNAIntrMsk) This bit is valid only when Scatter/Gather DMA mode is enabled.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	In non Scatter/Gather DMA mode, this bit is reserved	
10	Data Toggle Error Mask (DataTglErrMsk) This bit is not applicable in Scatter/Gather DMA mode.	R
9	Frame Overrun Mask (FrmOvrunMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
8	Babble Error Mask (BblErrMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
7	Transaction Error Mask (XactErrMsk) This bit is not applicable in Scatter/Gather DMA mode	RW
6	NYET Response Received Interrupt Mask (NyetMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
5	ACK Response Received/Transmitted Interrupt Mask (AckMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
4	NAK Response Received Interrupt Mask (NakMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
3	STALL Response Received Interrupt Mask (StallMsk) This bit is not applicable in Scatter/Gather DMA mode.	RW
2	AHB Error Mask (AHBErrMsk) Note: This bit is only accessible when OTG_ARCHITECTURE = 2	RW
1	Channel Halted Mask (ChHltdMsk)	RW
0	Transfer Completed Mask (XferComplMsk)	RW

33.6.2.30 Host Channel-n Transfer Size Register (HCTSIZn,0x510+n*0x20)

	HCTSIZn																Base + 0x510+n*0x20													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	Pid		Reserved													NTD								SCHED_INFO							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Reserved	R
30:29	PID (Pid) The application programs this Bits with the type of PID to use for the initial transaction. The host maintains this Bits for the rest of the transfer. 2'b00: DATA0 2'b01: DATA2 2'b10: DATA1 2'b11: MDATA (non-control)	RW
28:16	Reserved	R
15:8	NTD (Number of Transfer Descriptors)	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	(Non Isochronous) This value is in terms of number of descriptors. Maximum number of descriptor that can be present in the list is 64. The values can be from 0 to 63. 0 - 1 descriptor. 63 - 64 descriptors This Bits indicates the total number of descriptors present in that list. The core will wrap around after servicing NTD number of descriptors for that list. (Isochronous) This Bits indicates the number of descriptors present in that list.µframe The possible values for FS are 1 - 2 descriptors 3 - 4 descriptors 7 - 8 descriptors 15 - 16 descriptors 31 - 32 descriptors 63 - 64 descriptors The possible values for HS are 7 - 8 descriptors 15 - 16 descriptors 31 - 32 descriptors 63 - 64 descriptors 127 - 128 descriptors 255 - 256 descriptors	
7:0	SCHED_INFO (Schedule information) Every bit in this 8 bit register indicates scheduling for that microframe. Bit 0 indicates scheduling for 1st microframe and bit 7 indicates scheduling for 8th microframe in that frame. A value of 8'b11111111 indicates that the corresponding interrupt channel is scheduled to issue a token every microframe in that frame. A value of 8'b10101010 indicates that the corresponding interrupt channel is scheduled to issue a token every alternate microframe starting with second microframe. Note that this Bits is applicable only for periodic (Isochronous and Interrupt) channels.	RW

In Non-Scatter/Gather mode, HCTSIZn is defined as follows:

	HCTSIZn																Base + 0x510+n*0x20															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DoPng	Pid		PktCnt										XferSize																		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	R/W
31	Do Ping (DoPng) This bit is used only for OUT transfers. Setting this Bits to 1 directs the host to do PING protocol. Note: Do not set this bit for IN transfers. If this bit is set for IN transfers it disables the	RW
30:29	PID (Pid) The application programs this Bits with the type of PID to use for the initial transaction. The host maintains this Bits for the rest of the transfer. 2'b00: DATA0 2'b01: DATA2 2'b10: DATA1 2'b11: MDATA (non-control)/SETUP (control)	RW
28:19	Packet Count (PktCnt) This Bits is programmed by the application with the expected number of packets to be transmitted (OUT) or received (IN). The host decrements this count on every successful transmission or reception of an OUT/IN packet. Once this count reaches zero, the application is interrupted to indicate normal completion.	RW
18:0	Transfer Size (XferSize) For an OUT, this Bits is the number of data bytes the host sends during the transfer. For an IN, this Bits is the buffer size that the application has Reserved for the transfer. The application is expected to program this Bits as an integer multiple of the maximum packet size for IN transactions (periodic and non-periodic).	RW

33.6.2.31 Host Channel-n DMA Address Register (HCDMAn, ,0x514+n*0x20)

Buffer DMA Mode:

	HCDMAn																Base + 0x514+n*0x20															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMAAddr																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	R/W
31:0	DMA Address (DMAAddr) This Bits holds the start address in the external memory from which the data for the endpoint must be fetched or to which it must be stored. This register is incremented on every AHB transaction.	RW

Descriptor DMA Mode：

	HCDMAn																Base +0x514+n*0x20													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMAAddr																							CTD						Reserved		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:9 (Non Isoc)	DMA Address (DMAAddr) Non-Isochronous: This Bits holds the start address of the 512 bytes page. The first descriptor in the list should be located in this address. The first descriptor may be or may not be ready. The core starts processing the list from the CTD value. Isochronous: This Bits holds the address of the 2*(nTD+1) bytes of locations in which the isochronous descriptors are present where N is based on nTD as per Table below	RW
8:3 (Non Isoc)	Current Transfer Desc (CTD): Non Isochronous: This value is in terms of number of descriptors. The values can be from 0 to 63.	RW

31:N	N-1:3	2:0
Base Address	Offset	000

HS ISOC	
nTD	N
7	6
15	7
31	8
63	9
127	10
255	11

FS ISOC	
nTD	N
1	4
3	5
7	6
15	7
31	8
63	9

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	0 - 1 descriptor. 63- 64 descriptors. This Bits indicates the current descriptor processed in the list. This Bits is updated both by application and the core. For example, if the application enables the channel after programming CTD=5, then the core will start processing the 6th descriptor. The address is obtained by adding a value of (8bytes*5=) 40(decimal) to DMAAddr. Isochronous: CTD for isochronous is based on the current frame/μframe value. Need to be set to zero by application.	
2:0	Reserved	R

33.6.2.32 Host Channel-n DMA Buffer Address Register (HCDMABn,0x51C+n*0x20)

	HCDMABn																Base + 0x51C+n*0x20													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	buffer_address																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:0	Holds the current buffer address. This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this Bits is reserved.	R

33.6.2.33 Host Frame List Base Address Register (HFLBAddr,0x51C+n*0x20)

	HFLBAddr																Base + 0x41C+n*0x20													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	flarm_list																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:0	The starting address of the Frame list. This register is used only for Isochronous and Interrupt Channels.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

33.6.2.34 Device Configuration Register (DCFG,0x800)

	DCFG																Base + 0x800															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ResValid						PerSchIntvl		DescDMA	EPMisCnt					Reserved				EnDevOutNak	PerFrInt		DevAddr							Ena32KHzS	NZStsOUTHShk	DevSpd	
RST	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:26	Resume Validation Period (ResValid) This Bits controls the period when the core resumes from a suspend. When this bit is set, the core counts for the ResValid number of clock cycles to detect a valid resume. This Bits is effective only when DCFG.Ena32KHzSusp is set.	RW
25:24	Periodic Scheduling Interval (PerSchIntvl) PerSchIntvl must be programmed only for Scatter/Gather DMA mode. Description: This Bits specifies the amount of time the Internal DMA engine must allocate for fetching periodic IN endpoint data. Based on the number of periodic endpoints, this value must be specified as 25,50 or 75% of (micro)frame. When any periodic endpoints are active, the internal DMA engine allocates the specified amount of time in fetching periodic IN endpoint data. When no periodic endpoints are active, then the internal DMA engine services non- periodic endpoints, ignoring this Bits. After the specified time within a (micro)frame, the DMA switches to fetching for non- periodic endpoints. 2'b00: 25% of (micro)frame. 2'b01: 50% of (micro)frame. 2'b10: 75% of (micro)frame. 2'b11: Reserved.	RW
23	Enable Scatter/Gather DMA in Device mode (DescDMA). When the Scatter/Gather DMA option selected during configuration of the RTL, the application can set this bit during initialization to enable the Scatter/Gather DMA operation. NOTE: This bit must be modified only once after a reset. The following combinations are available for programming: GAHBCFG.DMAEn=0,DCFG.DescDMA=0 => Slave mode GAHBCFG.DMAEn=0,DCFG.DescDMA=1 => Invalid GAHBCFG.DMAEn=1,DCFG.DescDMA=0 => Buffered DMA mode	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	GAHBCFG.DMAEn=1,DCFG.DescDMA=1 => Scatter/Gather DMA mode	
22:18	IN Endpoint Mismatch Count (EPMisCnt) This Bits is valid only in shared FIFO operation. The application programs this filed with a count that determines when the core generates an Endpoint Mismatch interrupt (GINTSTS.EPMis). The core loads this value into an internal counter and decrements it. The counter is reloaded whenever there is a match or when the counter expires. The width of this counter depends on the depth of the Token Queue.	RW
17:14	Reserved	R
13	Enable Device OUT NAK (EnDevOutNak) This bit enables setting NAK for Bulk OUT endpoints after the transfer is completed when the core is operating in Device Descriptor DMA mode. 1'b0: The core does not set NAK after Bulk OUT transfer complete 1'b1: The core sets NAK after Bulk OUT transfer complete This bit is valid only when OTG_EN_DESC_DMA == 1'b1	RW
12:11	Periodic Frame Interval (PerFrInt) Indicates the time within a (micro)frame at which the application must be notified using the End Of Periodic Frame Interrupt. This can be used to determine if all the isochronous traffic for that (micro)frame is complete. 2'b00: 80% of the (micro)frame interval 2'b01: 85% 2'b10: 90% 2'b11: 95%	RW
10:4	Device Address (DevAddr) The application must program this Bits after every SetAddress control command.	RW
3	Enable 32-KHz Suspend Mode (Ena32KHzS) When the USB 1.1 Full-Speed Serial Transceiver Interface is chosen and this bit is set, the core expects the 48-MHz PHY clock to be switched to 32 KHz during a suspend. This bit can only be set if USB 1.1 Full-Speed Serial Transceiver Interface has been selected. If USB 1.1 Full-Speed Serial Transceiver Interface has not been selected, this bit must be zero.	RW
2	Non-Zero-Length Status OUT Handshake (NZStsOUTHShk) The application can use this Bits to select the handshake the core sends on receiving a nonzero-length data packet during the OUT transaction of a control transfer's Status stage. 1'b1: Send a STALL handshake on a nonzero-length status OUT transaction and do not send the received OUT packet to the application. 1'b0: Send the received OUT packet to the application (zero-length or nonzero-length) and send a handshake based on the NAK and STALL bits for the endpoint in the Device Endpoint Control register.	RW
1:0	Device Speed (DevSpd) Indicates the speed at which the application requires the core to enumerate, or	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the core is connected. 2'b00: High speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 2'b01: Full speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 2'b10: Low speed (USB 1.1 FS transceiver clock is 48 MHz) 2'b11: Full speed (USB 1.1 FS transceiver clock is 48 MHz)	

33.6.2.35 Device Control Register (DCTL,0x804)

	DCTL																															Base + 0x804
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														EnContOnBNA	NakOnBble	IgnrFrmNum	GMC		Reserved	PWROnPrgDone	CGOUTNak	SGOUTNak	CGNPInNak	SGNPInNak	TstCtl			GOUTNakSts	GNPINNakSts	SftDiscon	RmtWkUpSig
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Description	R/W
31:18	Reserved	R
17	Enable Continue on BNA (EnContOnBNA) This bit enables the DWC_otg core to continue on BNA for Bulk OUT endpoints. With this feature enabled, when a Bulk OUT endpoint receives a BNA interrupt the core starts processing the descriptor that caused the BNA interrupt after the endpoint re-enables the endpoint. 1'b0: After receiving BNA interrupt, the core disables the endpoint. When the endpoint is re-enabled by the application, the core starts processing from the DOEPDMA descriptor. 1'b1: After receiving BNA interrupt, the core disables the endpoint. When the endpoint is re-enabled by the application, the core starts processing from the descriptor that received the BNA interrupt. This bit is valid only when OTG_EN_DESC_DMA == 1'b1. It is a one-time programmable after reset bit like any other DCTL register bits.	RW
16	Set NAK automatically on babble (NakOnBble). The core sets NAK automatically for the endpoint on which babble is received.	RW
15	Ignore frame number for isochronous endpoints (IgnrFrmNum) Slave Mode (GAHBCFG.DMAEn=0): This bit is not valid in Slave mode and should not be programmed to 1.Non-Scatter/Gather DMA mode (GAHBCFG.DMAEn=1,DCFG.DescDMA=0): This bit is not used when Threshold mode is enabled and should not be programmed to 1.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	In non-Scatter/Gather DMA mode, the application receives transfer complete interrupt after transfers for multiple (micro)frames are completed. When Scatter/Gather DMA mode is disabled, this Bits is used by the application to enable periodic transfer interrupt. The application can program periodic endpoint transfers for multiple (micro)frames. 0: Periodic transfer interrupt feature is disabled; the application must program transfers for periodic endpoints every (micro)frame 1: Packets are not flushed when an ISOC IN token is received for an elapsed frame. The core ignores the frame number, sending packets as soon as the packets are ready, and the corresponding token is received. This Bits is also used by the application to enable periodic transfer interrupts. Scatter/Gather DMA Mode (GAHBCFG.DMAEn=1,DCFG.DescDMA=1): This bit is not applicable to high-speed, high-bandwidth transfers and should not be programmed to 1. In addition, this bit is not used when Threshold mode is enabled and should not be programmed to 1. 0: The core transmits the packets only in the frame number in which they are intended to be transmitted. 1: Packets are not flushed when an ISOC IN token is received for an elapsed frame. The core ignores the frame number, sending packets as soon as the packets are ready, and the corresponding token is received. When this bit is set, there must be only one packet per descriptor.	
14:13	Global Multi Count (GMC) GMC must be programmed only once after initialization. Applicable only for Scatter/Gather DMA mode. This indicates the number of packets to be serviced for that end point before moving to the next end point. It is only for non- periodic end points. 2'b00: Invalid. 2'b01: 1 packet. 2'b10: 2 packets. 2'b11: 3 packets. The value of this Bits automatically changes to 2'h1 when DCFG.DescDMA is set to 1. When Scatter/Gather DMA mode is disabled, this Bits is reserved and reads 2'b00.	RW
12	Reserved	R
11	Power-On Programming Done (PWROnPrgDone) The application uses this bit to indicate that register programming is completed after a wake-up from Power Down mode.	W
10	Clear Global OUT NAK (CGOUTNak) A write to this Bits clears the Global OUT NAK.	W
9	Set Global OUT NAK (SGOUTNak) A write to this Bits sets the Global OUT NAK.	W

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	The application uses this bit to send a NAK handshake on all OUT endpoints. The application must set the this bit only after making sure that the Global OUT NAK Effective bit in the Core Interrupt Register (GINTSTS.GOUTNakEff) is cleared.	
8	Clear Global Non-periodic IN NAK (CGNPInNak) A write to this Bits clears the Global Non-periodic IN NAK.	W
7	Set Global Non-periodic IN NAK (SGNPInNak) A write to this Bits sets the Global Non-periodic IN NAK.The application uses this bit to send a NAK handshake on all non-periodic IN endpoints. The core can also set this bit when a timeout condition is detected on a non-periodic endpoint in shared FIFO operation. The application must set this bit only after making sure that the Global IN NAK Effective bit in the Core Interrupt Register (GINTSTS.GINNakEff) is cleared.	W
6:4	Test Control (TstCtl) 3'b000: Test mode disabled 3'b001: Test_J mode 3'b010: Test_K mode 3'b011: Test_SE0_NAK mode 3'b100: Test_Packet mode 3'b101: Test_Force_Enable Others: Reserved	RW
3	Global OUT NAK Status (GOUTNakSts) 1'b0: A handshake is sent based on the FIFO Status and the NAK and STALL bit settings. 1'b1: No data is written to the RxFIFO, irrespective of space availability. Sends a NAK handshake on all packets, except on SETUP transactions. All isochronous OUT packets are dropped.	W
2	Global Non-periodic IN NAK Status (GNPINNakSts) 1'b0: A handshake is sent out based on the data availability in the transmit FIFO. 1'b1: A NAK handshake is sent out on all non-periodic IN endpoints, irrespective of the data availability in the transmit FIFO.	W
1	Soft Disconnect (SftDiscon) The application uses this bit to signal the DWC_otg core to do a soft disconnect. As long as this bit is set, the host does not see that the device is connected, and the device does not receive signals on the USB. The core stays in the disconnected state until the application clears this bit. The minimum duration for which the core must keep this bit set is specified in Table 33-3. 1'b0: Normal operation. When this bit is cleared after a soft disconnect, the core drives the phy_opmode_o signal on the UTMI+ to 2'b00, which generates a device connect event to the USB host. When the device is reconnected, the USB host restarts device enumeration. 1'b1: The core drives the phy_opmode_o signal on the UTMI+ to 2'b01, which	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	generates a device disconnect event to the USB host. Note: This bit can be also used for ULPI/FS Serial interfaces. Note: This bit is not impacted by a soft reset.	
0	Remote Wakeup Signaling (RmtWkUpSig) When the application sets this bit, the core initiates remote signaling to wake the USB host. The application must set this bit to instruct the core to exit the Suspend state. As specified in the USB 2.0 specification, the application must clear this bit 1-15 ms after setting it.If LPM is enabled and the core is in the L1 (Sleep) state, when the application sets this bit, the core initiates L1 remote signaling to wake up the USB host. The application must set this bit to instruct the core to exit the Sleep state. As specified in the LPM specification, the hardware automatically clears this bit 50 µs ($T_{L1DevDrvResume}$) after being set by the application. The application must not set this bit when GLPMCFG bRemoteWake from the previous LPM transaction is zero.	RW

Table 33-3 Minimum Duration for Soft Disconnect

Operating Speed	Device state	Minimum Duration
High Speed	Suspend	1ms+2.5us
High Speed	Idle	3ms+2.5us
High Speed	Not Idle or Suspend	125us
Full Speed/Low Speed	Suspend	1ms+2.5us
Full Speed/Low Speed	Idle	2.5us
Full Speed/Low Speed	Not Idle or Suspend	2.5us

33.6.2.36 Device Status Register (DSTS,0x808)

	DSTS																														Base + 0x808
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										SOFFN														Reserved				ErrticErr	EnumSpd		SuspSts
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Description	R/W
31:22	Reserved	R
21:8	Frame or Microframe Number of the Received SOF (SOFFN) When the core is operating at high speed, this Bits contains a microframe number. When the core is operating at full or low speed, this Bits contains a frame number. Note: This register may return a non zero value if read immediately after power	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	on reset. In case the register bit reads non zero immediately after power on reset it does not indicate that SOF has been received from the host. The read value of this interrupt is valid only after a valid connection between host and device is established.	
7:4	Reserved	R
3	Erratic Error (ErrticErr) The core sets this bit to report any erratic errors (phy_rxvalid_i/phy_rxvldh_i or phy_rxactive_i is asserted for at least 2 ms, due to PHY error) seen on the UTMI+. Due to erratic errors, the DWC_otg core goes into Suspended state and an interrupt is generated to the application with Early Suspend bit of the Core Interrupt register (GINTSTS.ErlySusp). If the early suspend is asserted due to an erratic error, the application can only perform a soft disconnect recover.	R
2:1	Enumerated Speed (EnumSpd) Indicates the speed at which the DWC_otg core has come up after speed detection through a chirp sequence. 2'b00: High speed (PHY clock is running at 30 or 60 MHz) 2'b01: Full speed (PHY clock is running at 30 or 60 MHz) 2'b10: Low speed (PHY clock is running at 48 MHz, internal phy_clk at 6 MHz) 2'b11: Full speed (PHY clock is running at 48 MHz) Low speed is not supported for devices using a UTMI+ PHY.	R
0	Suspend Status (SuspSts) In Device mode, this bit is set as long as a Suspend condition is detected on the USB. The core enters the Suspended state when there is no activity on the utmi_linestate signal for an extended period of time. The core comes out of the suspend: When there is any activity on the utmi_linestate signal When the application writes to the Remote Wakeup Signaling bit in the Device Control register (DCTL.RmtWkUpSig).	R

33.6.2.37 Device IN Endpoint Common Interrupt Mask Register (DIEPMSK,0x810)

	DIEPMSK																														
																														Base + 0x810	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		NAKMsk	NAKMsk			BNAInIntrMsk	TxfifoUndrnMsk	Reserved	INEPNakEffMsk	INTknEPMisMsk	INTknTXFEmpMsk	TimeOUTMsk	AHBErrMsk	EPDisbldMsk	XferComplMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	R/W
31:14	Reserved	R
13	NAK interrupt Mask (NAKMsk)	RW
12:10	Reserved	R
9	BNA Interrupt Mask (BNAInIntrMsk) This bit is valid only when Device Descriptor DMA is enabled.	RW
8	Fifo Underrun Mask (TxfifoUndrnMsk)	RW
7	Reserved	R
6	IN Endpoint NAK Effective Mask (INEPNakEffMsk)	RW
5	IN Token received with EP Mismatch Mask (INTknEPMisMsk)	RW
4	IN Token Received When TxFIFO Empty Mask (INTknTXFEmpMsk)	RW
3	Timeout Condition Mask (TimeOUTMsk) (Non-isochronous endpoints)	RW
2	AHB Error Mask (AHBErrMsk)	RW
1	Endpoint Disabled Interrupt Mask (EPDisbldMsk)	RW
0	Transfer Completed Interrupt Mask (XferComplMsk)	RW

33.6.2.38 Device OUT Endpoint Common Interrupt Mask Register (DOEPMSK,0x814)

	DOEPMSK																Base + 0x814															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	NYETMsk	NAKMsk	BbleErrMsk	Reserved		BnaOutIntrMsk	OutPktErrMsk	Reserved	Back2BackSETup	Reserved	OUTTknEPdisMsk	SetUPMsk	AHBErrMsk	EPDisbldMsk	XferComplMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:15	Reserved	R
14	NYET Interrupt Mask (NYETMsk)	RW
13	NAK Interrupt Mask (NAKMsk)	RW
12	Babble Interrupt Mask (BbleErrMsk)	RW
11:10	Reserved	R
9	BNA interrupt Mask (BnaOutIntrMsk)	RW
8	OUT Packet Error Mask (OutPktErrMsk)	RW
7	Reserved	R
6	Back-to-Back SETUP Packets Received Mask (Back2BackSETup) Applies to control OUT endpoints only.	RW
5	Reserved	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

4	OUT Token Received when Endpoint Disabled Mask (OUTTknEPdisMsk) Applies to control OUT endpoints only.	RW
3	SETUP Phase Done Mask (SetUPMsk) Applies to control endpoints only.	RW
2	AHB Error (AHBErrMsk)	RW
1	Endpoint Disabled Interrupt Mask (EPDisbldMsk)	RW
0	Transfer Completed Interrupt Mask (XferComplMsk)	RW

33.6.2.39 Device All Endpoints Interrupt Register (DAINT,0x818)

	DAINT																Base + 0x818															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OutEPInt																InEpInt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	OUT Endpoint Interrupt Bits (OutEPInt) One bit per OUT endpoint: Bit 16 for OUT endpoint 0, bit 31 for OUT endpoint 15	R
15:0	IN Endpoint Interrupt Bits (InEpInt) One bit per IN Endpoint: Bit 0 for IN endpoint 0, bit 15 for endpoint 15	R

33.6.2.40 Device All Endpoints Interrupt Mask Register (DAINTMSK,0x81C)

	DAINTMSK																Base + 0x81C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OutEpMsk																InEpMsk															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	OUT EP Interrupt Mask Bits (OutEpMsk) One per OUT Endpoint: Bit 16 for OUT EP 0, bit 31 for OUT EP 15 The value of this Bits depends on the number of OUT endpoints that are	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	configured.	
15:0	IN EP Interrupt Mask Bits (InEpMsk) One bit per IN Endpoint: Bit 0 for IN EP 0, bit 15 for IN EP 15 The value of this Bits depends on the number of IN endpoints that are configured.	RW

33.6.2.41 Device IN Token Sequence Learning Queue Read Register 1 (DTKNQR1,0x820)

	DTKNQP1																Base + 0x820													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPTkn																								WrapBit	Reserved		INTknWPtr				
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:8	Endpoint Token (EPTkn) Four bits per token represent the endpoint number of the token: Bits [31:28]: Endpoint number of Token 5 Bits [27:24]: Endpoint number of Token 4 ..... Bits [15:12]: Endpoint number of Token 1 Bits [11:8]: Endpoint number of Token 0	R
7	Wrap Bit (WrapBit) This bit is set when the write pointer wraps. It is cleared when the learning queue is cleared.	R
6:5	Reserved	R
4:0	IN Token Queue Write Pointer (INTknWPtr)	R

33.6.2.42 Device IN Token Sequence Learning Queue Read Register 2 (DTKNQR2,0x824)

	DTKNQR2																Base + 0x824													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPTkn																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	R/W
31:0	Endpoint Token (EPTkn) Four bits per token represent the endpoint number of the token: Bits [31:28]: Endpoint number of Token 13 Bits [27:24]: Endpoint number of Token 12 ..... Bits [7:4]: Endpoint number of Token 7 Bits [3:0]: Endpoint number of Token 6	R

33.6.2.43 Device IN Token Sequence Learning Queue Read Register 3 (DTKNQR3,0x830)

	DTKNQR3																Base + 0x830															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPTkn																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:0	Endpoint Token (EPTkn) Four bits per token represent the endpoint number of the token: Bits [31:28]: Endpoint number of Token 21 Bits [27:24]: Endpoint number of Token 20 ..... Bits [7:4]: Endpoint number of Token 15 Bits [3:0]: Endpoint number of Token 14	R

33.6.2.44 Device IN Token Sequence Learning Queue Read Register 4 (DTKNQR4,0x834)

	DTKNQR4																Base + 0x834															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPTkn																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	R/W
31:0	Endpoint Token (EPTkn) Four bits per token represent the endpoint number of the token: Bits [31:28]: Endpoint number of Token 29 Bits [27:24]: Endpoint number of Token 28 ..... Bits [7:4]: Endpoint number of Token 23 Bits [3:0]: Endpoint number of Token 22	R

33.6.2.45 Device VBUS Discharge Time Register (DVBUSDIS,0x828)

	DVBUSDIS																Base + 0x828													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																DVBUSDis															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:16	Reserved	R
15:0	Device VBUS Discharge Time (DVBUSDis) Specifies the VBUS discharge time after VBUS pulsing during SRP. This value equals: VBUS discharge time in PHY clocks / 1,024 The value you use depends whether the PHY is operating at 30 MHz (16-bit data width) or 60 MHz (8-bit data width). Depending on your VBUS load, this value can need adjustment. The reset value is : PHY CLK 30MHz :0x0B8F PHY CLK 60MHz :0x17D7	RW

33.6.2.46 Device VBUS Pulsing Time Register (DVBUSPULSE,0x82C)

	DVBUSPULSE																Base + 0x82C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				DVBUSPulse											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	R/W
31:12	Reserved	R
11:0	Device VBUS Pulsing Time (DVBUSPulse) Specifies the VBUS pulsing time during SRP. This value equals: VBUS pulsing time in PHY clocks / 1,024 The value you use depends whether the PHY is operating at 30 MHz (16-bit data width) or 60 MHz (8-bit data width). The reset value is : PHY CLK 30MHz :0x2C6 PHY CLK 60MHz :0x5B8	RW

33.6.2.47 Device Threshold Control Register (DTHRCTL,0x830)

	DTHRCTL																													Base + 0x830
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				ArbPrkEn	Reserved	RxThrLen									RxThrEn	Reserved			AHBThrRatio		TxThrLen									ISOThrEn	NonISOThrEn
RST	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Description	R/W
31:28	Reserved	R
27	Arbiter Parking Enable (ArbPrkEn) This bit controls internal DMA arbiter parking for IN endpoints. When thresholding is enabled and this bit is set to one, then the arbiter parks on the IN endpoint for which there is a token received on the USB. This is done to avoid getting into underrun conditions. By default the parking is enabled.	RW
26	Reserved	R
25:17	Receive Threshold Length (RxThrLen) This Bits specifies Receive thresholding size in DWORDS. This Bits also specifies the amount of data received on the USB before the core can start transmitting on the AHB. The threshold length has to be at least eight DWORDS. The recommended value for ThrLen is to be the same as the programmed AHB Burst Length (GAHBCFG.HBstLen).	RW
16	Receive Threshold Enable (RxThrEn) When this bit is set, the core enables thresholding in the receive direction. Note: Synopsys recommends that you do not enable RxThrEn, because it may cause issues in the RxFIFO especially during error conditions such as RxError and	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Babble.	
15:13	Reserved	R
12:11	AHB Threshold Ratio (AHBThrRatio) These bits define the ratio between the AHB threshold and the MAC threshold for the transmit path only. The AHB threshold always remains less than or equal to the USB threshold, because this does not increase overhead. Both the AHB and the MAC threshold must be DWORD-aligned. The application needs to program TxThrLen and the AHBThrRatio to make the AHB Threshold value DWORD aligned. If the AHB threshold value is not DWORD aligned, the core might not behave correctly. When programming the TxThrLen and AHBThrRatio, the application must ensure that the minimum AHB threshold value does not go below 8 DWORDS to meet the USB turnaround time requirements.	RW
10:2	Transmit Threshold Length (TxThrLen) This Bits specifies Transmit thresholding size in DWORDS. This Bits also forms the MAC threshold and specifies the amount of data, in bytes, to be in the corresponding endpoint transmit FIFO before the core can start a transmit on the USB. When the value of AHBThrRatio is 2'h00, the threshold length must be at least 8 DWORDS. If the AHBThrRatio is nonzero, the application must ensure that the AHB threshold value does not go below the recommended 8 DWORDs. This Bits controls both isochronous and non-isochronous IN endpoint thresholds. The recommended value for ThrLen is to be the same as the programmed AHB Burst Length (GAHBCFG.HBstLen).	RW
1	ISO IN Endpoints Threshold Enable. (ISOThrEn) When this bit is set, the core enables thresholding for isochronous IN endpoints.	RW
0	Non-ISO IN Endpoints Threshold Enable. (NonISOThrEn) When this bit is set, the core enables thresholding for Non Isochronous IN endpoints.	RW

33.6.2.48 Device IN Endpoint FIFO Empty Interrupt Mask Register(DIEPEMPMSK,0x834)

	DIEPEMPMSK																Base + 0x834															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																InEpTxfEmpMsk															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	R/W
31:16	Reserved	R
15:0	IN EP Tx FIFO Empty Interrupt Mask Bits (InEpTxfEmpMsk) These bits acts as mask bits for DIEPINTn. TxFEmp interrupt One bit per IN Endpoint: Bit 0 for IN endpoint 0 ... Bit 15 for endpoint 15	RW

33.6.2.49 Device Each Endpoint Interrupt Register (DEACHINT,0x838)

	DEACHINT																														Base + 0x838
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EchOutEPInt																EchInEpInt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	OUT Endpoint Interrupt Bits (EchOutEPInt) One bit per OUT endpoint: Bit 16 for OUT endpoint 0 ... Bit 31 for OUT endpoint 15	R
15:0	IN Endpoint Interrupt Bits (EchInEpInt) One bit per IN Endpoint: Bit 0 for IN endpoint 0 ... Bit 15 for IN endpoint 15	R

33.6.2.50 Device Each Endpoint Interrupt Register Mask (DEACHINTMSK,0x83C)

	DEACHINTMSK																														Base + 0x83C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EchOutEPInt																EchInEpInt															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	R/W
31:16	OUT EP Interrupt Mask Bits (EchOutEpMsk) One per OUT Endpoint: Bit 16 for IN endpoint 0 ... Bit 31 for IN endpoint 15	RW
15:0	IN EP Interrupt Mask Bits (EchInEpMsk) One bit per IN Endpoint: Bit 0 for IN endpoint 0 ... Bit 15 for IN endpoint 15	RW

33.6.2.51 Device Each In Endpoint-n Interrupt Register (DIEPEACHMSKn,0x840)

	DIEPEACHMSKn																														
	Base + 0x840																														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		NAKMsk	Reserved			BNAInIntrMsk	TxfifoUndrnMsk	Reserved	INEPNakEffMsk	INTknEPMisMsk	INTknTXFEmpMsk	TimeOUTMsk	AHBErrMsk	EPDisbldMsk	XferComplMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:14	Reserved	R
13	NAK interrupt Mask (NAKMsk)	RW
12:10	Reserved	R
9	BNA interrupt Mask (BNAInIntrMsk)	RW
8	Fifo Under run Mask (TxfifoUndrnMsk)	RW
7	Reserved	R
6	IN Endpoint NAK Effective Mask (INEPNakEffMsk)	RW
5	IN Token received with EP Mismatch Mask (INTknEPMisMsk)	RW
4	IN Token Received When TxFIFO Empty Mask (INTknTXFEmpMsk)	RW
3	Timeout Condition Mask (TimeOUTMsk) (Non-isochronous endpoints)	RW
2	AHB Error Mask (AHBErrMsk)	RW
1	Endpoint Disabled Interrupt Mask (EPDisbldMsk)	RW
0	Transfer Completed Interrupt Mask (XferComplMsk)	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

33.6.2.52 Device Each Out Endpoint-n Interrupt Register (DOEPEACHMSKn,0x880+n*0x4)

	DOEPEACHMSKn																Base + 0x880+n*0x4													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	NYETMsk	NAKMsk	BbleErrMsk	Reserved		BnaOutIntrMsk	OutPktErrMsk	Reserved	Back2BackSETup	Reserved	OUTTknEPdisMsk	SetUPMsk	AHBErrMsk	EPDisbldMsk	XferComplMsk
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:15	Reserved	R
14	NYET interrupt Mask (NYETMsk)	RW
13	NAK interrupt Mask (NAKMsk)	RW
12	Babble interrupt Mask (BbleErrMsk)	RW
11:10	Reserved	R
9	BNA interrupt Mask (BnaOutIntrMsk)	RW
8	OUT Packet Error Mask (OutPktErrMsk)	RW
7	Reserved	R
6	Back-to-Back SETUP Packets Received Mask (Back2BackSETup) Applies to control OUT endpoints only.	RW
5	Reserved	R
4	OUT Token Received when Endpoint Disabled Mask (OUTTknEPdisMsk) Applies to control OUT endpoints only.	RW
3	SETUP Phase Done Mask (SetUPMsk) Applies to control endpoints only.	RW
2	AHB Error (AHBErrMsk)	RW
1	Endpoint Disabled Interrupt Mask (EPDisbldMsk)	RW
0	Transfer Completed Interrupt Mask (XferComplMsk)	RW

33.6.2.53 Device Control IN Endpoint 0 Control Register (DIEPCTL0,0x900)

	DIEPCTL0																Base + 0x900													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPEna	EPDis	Reserved		SNAK	CNAK	TxFNum				Stall	Reserved	EPType		NAKSts	Reserved	USBActEP	NextEp				Reserved									MPS	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	R/W
31	Endpoint Enable (EPEna) When Scatter/Gather DMA mode is enabled, for IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. When Scatter/Gather DMA mode is disabled—such as in buffer-pointer based DMA mode—this bit indicates that data is ready to be transmitted on the endpoint. The core clears this bit before setting the following interrupts on this endpoint: Endpoint Disabled Transfer Completed	RW[1]
30	Endpoint Disable (EPDis) The application sets this bit to stop transmitting data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled Interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint. This bit is valid only when DMA mode is enabled.	RW[2]
29:28	Reserved	R
27	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint.	W
26	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint.	W
25:22	TxFIFO Number (TxFNum) For Shared FIFO operation, this value is always set to 0, indicating that control IN endpoint 0 data is always written in the Non-Periodic Transmit FIFO. For Dedicated FIFO operation, this value is set to the FIFO number that is assigned to IN Endpoint 0.	RW
21	STALL Handshake (Stall) The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority.	RW[3]
20	Reserved	R
19:18	Endpoint Type (EPType) Hardcoded to 00 for control.	R
17	NAK Status (NAKSts) Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status 1'b1: The core is transmitting NAK handshakes on this endpoint. When this bit is set, either by the application or core, the core stops transmitting data, even if there is data available in the TxFIFO. Irrespective of this bit's setting, the	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	core always responds to SETUP data packets with an ACK handshake.	
16	Reserved	R
15	USB Active Endpoint (USBActEP) This bit is always set to 1, indicating that control endpoint 0 is always active in all configurations and interfaces.	R
14:11	Next Endpoint (NextEp) Applies to non-periodic IN endpoints only. Indicates the endpoint number to be fetched after the data for the current endpoint is fetched. The core can access this Bits, even when the Endpoint Enable (EPEna) bit is not set. This Bits is not valid in Slave mode. Note: This Bits is valid only for Shared FIFO operations.	RW
10:2	Reserved	R
1:0	Maximum Packet Size (MPS) Applies to IN and OUT endpoints. The application must program this Bits with the maximum packet size for the current logical endpoint.	RW

Note:

[1],[2],[3]: This bits will operate with Write set , self clear function.

33.6.2.54 Device Control OUT Endpoint 0 Control Register (DOEPCTL0,0xB00)

	DOEPCTL																Base + 0xB00															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPEna	EPDis	Reserved		SNAK	CNAK	Reserved				Stall	Snp	EPType		NAKSts	Reserved	USBActEP	Reserved													MPS	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Endpoint Enable (EPEna) When Scatter/Gather DMA mode is enabled, for OUT endpoints this bit indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is disabled—(such as for buffer-pointer based DMA mode)—this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint:	RW[1]

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	SETUP Phase Done Endpoint Disabled Transfer Completed Note: In DMA mode, this bit must be set for the core to transfer SETUP data packets into memory.	
30	Endpoint Disable (EPDis) The application cannot disable control OUT endpoint 0.	R
29:28	Reserved	R
27	Set NAK (SNAK) A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set bit on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.	W
26	Clear NAK (CNAK) A write to this bit clears the NAK bit for the endpoint.	W
25:22	Reserved	R
21	STALL Handshake (Stall) The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	RW[2]
20	Snoop Mode (Snp) This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.	RW
19:18	Endpoint Type (EPType) Hardcoded to 2'b00 for control.	R
17	NAK Status (NAKSts) Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit, the core stops receiving data, even if there is space in the RxFIFO to accommodate the incoming packet. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	R
16	Reserved	R
15	USB Active Endpoint (USBActEP) This bit is always set to 1, indicating that a control endpoint 0 is always active in all configurations and interfaces.	R
14:2	Reserved	R
1:0	Maximum Packet Size (MPS) The maximum packet size for control OUT endpoint 0 is the same as what is	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	programmed in control IN Endpoint 0. 2'b00: 64 bytes 2'b01: 32 bytes 2'b10: 16 bytes 2'b11: 8 bytes	

Note:

[1],[2]: This bits will operate with Write set , self clear function.

33.6.2.55 Device Endpoint-n Control Register (DIEPCTLn/DOEPCTLn, 0x900/0xB00+n*0x20)

	DIEPCTLn/DOEPCTLn																Base + 0x900/0xB00+n*0x20													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EPEna	EPDis	SetD1PID	SetD0PID	SNAK	CNAK	TxFNum				Stall	Snp	EPType		NAKSts	DPID	USBActEP	NextEp				MPS										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31	Endpoint Enable (EPEna) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is enabled—such as for buffer-pointer based DMA mode: For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint. SETUP Phase Done Endpoint Disabled Transfer Completed Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory.	RW[1]
30	Endpoint Disable (EPDis) Applies to IN and OUT endpoints.	RW[2]

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.	
29	Set DATA1 PID (SetD1PID) Applies to interrupt/bulk IN and OUT endpoints only. Writing to this Bits sets the Endpoint Data PID (DPID) Bits in this register to DATA1. This Bits is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Set Odd (micro)frame (SetOddFr) Applies to isochronous IN and OUT endpoints only. Writing to this Bits sets the Even/Odd (micro)frame (EO_FrNum) Bits to odd (micro)frame. This Bits is not applicable for Scatter/Gather DMA mode.	W W
28	Set DATA0 PID (SetD0PID) Applies to interrupt/bulk IN and OUT endpoints only. Writing to this Bits sets the Endpoint Data PID (DPID) Bits in this register to DATA0. This Bits is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. In non-Scatter/Gather DMA mode: Set Even (micro)frame (SetEvenFr) Applies to isochronous IN and OUT endpoints only. Writing to this Bits sets the Even/Odd (micro)frame (EO_FrNum) Bits to even (micro) frame. When Scatter/Gather DMA mode is enabled, this Bits is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure.	W
27	Set NAK (SNAK) Applies to IN and OUT endpoints. A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for OUT endpoints on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.	W
26	Clear NAK (CNAK) Applies to IN and OUT endpoints. A write to this bit clears the NAK bit for the endpoint.	W
25:22	TxFIFO Number (TxFNum) *Shared FIFO Operation*—non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. 4'h0: Non-Periodic TxFIFO	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Others: Specified Periodic TxFIFO.number Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum Bits is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint, and the number of this FIFO must be programmed into the TxFNum Bits. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. *Dedicated FIFO Operation*—these bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This Bits is valid only for IN endpoints.	
21	STALL Handshake (Stall) Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	RW RW[3]
20	Snoop Mode (Snp) Applies to OUT endpoints only. This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.	RW
19:18	Endpoint Type (EPType) Applies to IN and OUT endpoints. This is the transfer type supported by this logical endpoint. 2'b00: Control 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt	RW
17	NAK Status (NAKSts) Applies to IN and OUT endpoints. Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. For non-isochronous IN endpoints: The core stops transmitting any data on an IN	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	endpoint, even if there data is available in the TxFIFO. For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	
16	Endpoint Data PID (DPID) Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID Bitss of this register to program either DATA0 or DATA1 PID. 1'b0: DATA0 1'b1: DATA1 This Bits is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro) frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr Bitss in this register. 1'b0: Even (micro)frame 1'b1: Odd (micro)frame When Scatter/Gather DMA mode is enabled, this Bits is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure.	R
15	USB Active Endpoint (USBActEP) Applies to IN and OUT endpoints. Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit.	RW[4]
14:11	Next Endpoint (NextEp) Applies to non-periodic IN endpoints only. Indicates the endpoint number to be fetched after the data for the current endpoint is fetched. The core can access this Bits, even when the Endpoint Enable (EPEna) bit is low. This Bits is not valid in Slave mode operation. Note: This Bits is valid only for Shared FIFO operations.	RW
10:0	Maximum Packet Size (MPS) Applies to IN and OUT endpoints. The application must program this Bits with the maximum packet size for the current	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Note:[1]~[2]: This bits will operate with Write set , self clear function.

33.6.2.56 Device Endpoint-n Interrupt Register (DIEPINTn/DOEPINTn, 0x908/0xB08+n*0x20)

	DIEPINTn/DOEPINTn																Base + 0x908/0xB08+n*0x20													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																	NYETIntrpt	NAKIntrpt	BbleErrIntrpt	PktDrpSts	Reserved	BNAIntr	TxfifoUndrn	TxFEmp	INEPNakEff	INTknEPMis	INTknTXFEmp	TimeOUT	AHBErr	EPDisbld	XferCompl
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:15	Reserved	R
14	NYET interrupt (NYETIntrpt) The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint.	RW[1]
13	NAK interrupt (NAKIntrpt) The core generates this interrupt when a NAK is transmitted. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to unavailability of data in the TXFifo.	RW[2]
12	BbleErr (Babble Error) interrupt (BbleErrIntrpt) The core generates this interrupt when babble is received for the endpoint.	RW[3]
11	PktDrpSts (Packet Dropped Status) This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. **Dependency**: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.	RW[4]
10	Reserved	R
9	BNA (Buffer Not Available) Interrupt (BNAIntr) The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done. **Dependency**: This bit is valid only when Scatter/Gather DMA mode is enabled.	RW[5]
8	FIFO Underrun (TxfifoUndrn) Applies to IN endpoints only The core generates this interrupt when it detects a transmit FIFO underrun condition for this endpoint. **Dependency**: This interrupt is valid only when both of the following conditions are true: Parameter OTG_EN_DED_TX_FIFO=1	RW[6]

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Thresholding is enabled OUT Packet Error (OutPktErr) Applies to OUT endpoints only This interrupt is asserted when the core detects an overflow or a CRC error for an OUT packet. **Dependency**: This interrupt is valid only when both of the following conditions are true: Parameter OTG_EN_DED_TX_FIFO=1 Thresholding is enabled.	RW[7]
7	Transmit FIFO Empty (TxFEmp) This bit is valid only for IN Endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)).	R
6	N Endpoint NAK Effective (INEPNakEff) This bit should be cleared by writing a 1'b1 before writing a 1'b1 to corresponding DIEPCTLn.CNAK. The interrupt indicates that the IN endpoint NAK bit set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. This bit is applicable only when the endpoint is enabled. Back-to-Back SETUP Packets Received (Back2BackSETup) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint. This bit is not valid in Slave mode.	RW[8] RW[9]
5	IN Token Received with EP Mismatch (INTknEPMis) Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received. Status Phase Received For Control Write (StsPhseRcvd) This interrupt is valid only for Control OUT endpoints and only in Scatter Gather DMA mode. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is	RW[10]

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	applicable only in case of Scatter Gather DMA mode.	
4	IN Token Received When TxFIFO is Empty (INTknTXFEmp) Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received. OUT Token Received When Endpoint Disabled (OUTTknEPdis) Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received.	RW[11]
3	Timeout Condition (TimeOUT) In shared TX FIFO mode, applies to non-isochronous IN endpoints only. In dedicated FIFO mode, applies only to Control IN endpoints. In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint. SETUP Phase Done (SetUp) Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet.	RW[12]
2	AHB Error (AHBErr) Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address.	RW[13]
1	Endpoint Disabled Interrupt (EPDisbld) Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.	RW[14]
0	Transfer Completed Interrupt (XferCompl) Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled For IN endpoint this Bits indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. For OUT endpoint this Bits indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. When Scatter/Gather DMA mode is disabled, this Bits indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint.	RW[15]

Note:

[1]~[15]: This bits will operate with Self set , Write clear function.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

33.6.2.57 Device Endpoint 0 Transfer Size Register (DIEPTSIZ0/DOEPTSIZ0,0x910/0xB10)

	DIEPTSIZ0/DOEPTSIZ0																Base + 0x910/0xB10															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											PktCnt		Reserved													XferSize						
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:21	Reserved	R
20:19	Packet Count (PktCnt) Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. This Bits is decremented every time a packet (maximum size or short packet) is read from the TxFIFO.	RW
18:7	Reserved	R
6:0	Transfer Size (XferSize) Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this Bits every time a packet from the external memory is written to the TxFIFO.	RW

33.6.2.58 Device Endpoint-n Transfer Size Register (DIEPTSIZn/DOEPTSIZn, 0x910/0xB10+n*0x20)

	DIEPTSIZn/DOEPTSIZn																Base + 0x910/0xB10+n*0x20															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	MC		PktCnt										XferSize																		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	R/W
31	Reserved	R
30:29	Multi Count (MC) Applies to IN endpoints only. For periodic IN endpoints, this Bits indicates the number of packets that must be transmitted per microframe on the USB. The core uses this Bits to calculate the data PID for isochronous IN endpoints. 2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets For non-periodic IN endpoints, this Bits is valid only in Internal DMA mode. It specifies the number of packets the core must fetch for an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint Bits of the Device Endpoint-*n* Control register (DIEPCTLn.NextEp). Received Data PID (RxDPID) Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint. 2'b00: DATA0 2'b01: DATA2 2'b10: DATA1 2'b11: MDATA SETUP Packet Count (SUPCnt) Applies to control OUT Endpoints only. This Bits specifies the number of back-to-back SETUP data packets the endpoint can receive. 2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets	RW R R RW
28:19	Packet Count (PktCnt) Indicates the total number of USB packets that constitute the Transfer Size amount of data for this endpoint (PktCnt = XferSize / MPS). IN Endpoints: This Bits is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. OUT Endpoints: This Bits is decremented every time a packet (maximum size or short packet) is written to the RxFIFO.	RW
18:0	Transfer Size (XferSize) This Bits contains the transfer size in bytes for the current endpoint. The transfer size (XferSize) = Sum of buffer sizes across all descriptors in the list for the endpoint. In Buffer DMA, the core only interrupts the application after it has exhausted the	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. IN Endpoints: The core decrements this Bits every time a packet from the external memory is written to the TxFIFO. OUT Endpoints: The core decrements this Bits every time a packet is read from the RxFIFO and written to the external memory.	

33.6.2.59 Device Endpoint-n DMA Address Register (DIEPDMAn/DOEPDMAn, 0x914/0xB14+n*0x20)

	DIEPDMAnDOEPDMAn																Base + 0x914/0xB14+n*0x20													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMAAddr																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Description	R/W
31:0	DMA Address (DMAAddr) Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this Bits stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this Bits. When Scatter/Gather DMA mode is enabled, this Bits indicates the base pointer for the descriptor list.	RW

33.6.2.60 Device Endpoint-n DMA Buffer Address Register (DIEPDMABn/DOEPDMABn, 0x91C/0xB1C+n*0x20)

	DIEPDMABn/DOEPDMABn																Base + 0x91C/0xB1C+n*0x20													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMABufferAddr																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Description	R/W
31:0	DMA Buffer Address (DMABufferAddr) Holds the current buffer address.This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this Bits is reserved.	R

33.6.2.61 Device IN Endpoint Transmit FIFO Status Register (DTXFSTSn,0x918)

	DTXFSTSn																Base + 0x918															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																INEPTxFSpcAvail																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Description	R/W
31:16	Reserved.	R
15:0	IN Endpoint TxFIFO Space Avail (INEPTxFSpcAvail) Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. 16'h0: Endpoint TxFIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'hn: n words available (where 0≤n≤32,768) 16'h8000: 32,768 words available Others: Reserved	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

34 Gigabit Ethernet Media Access Controller (GMAC)

34.1 Overview

The processor contains one Ethernet media access controller (GMAC), each capable of supporting 10/100/1000Mbps Ethernet. The MAC provides the interface between the host application and the PHY layer through RMII/RGMII. The PHY layer device is external to the processor.

34.2 Features

- 10, 100,1000Mbps data transfer rates with the following PHY interfaces:
  - RMII/RGMII interface to communicate with an external Fast Ethernet PHY
- Full-duplex operation:
  - IEEE 802.3x flow control automatic transmission of zero-quanta Pause frame on flow control input de-assertion
  - forwarding of received Pause frames to the user application
- Half-duplex operation:
  - CSMA/CD Protocol support
  - Frame bursting and frame extension in 100 Mbps half-duplex operation
- Preamble and start of frame data (SFD) insertion in Transmit path
- Preamble and SFD deletion in the Receive path
- Automatic CRC and pad generation controllable on a per-frame basis
- Automatic Pad and CRC Stripping options for receive frames
- Flexible address filtering modes, such as:
  - Up to 31 additional 48-bit perfect (DA) address filters with masks for each byte
  - 64-bit Hash filter for multicast and unicast (DA) addresses
  - Option to pass all multicast addressed frames
  - Promiscuous mode to pass all frames without any filtering for network monitoring
  - Pass all incoming packets (as per filter) with a status report
- Support Standard or Jumbo Ethernet frames with up to 2 KB of size
- IEEE 802.1Q VLAN tag detection for reception frames
- MDIO master interface for PHY device configuration and management
- CRC replacement, Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted frames with per-frame control
- Programmable watchdog timeout limit in the receive path
- Detect remote wake-up frames and AMD magic packets

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

34.3 Block Diagram

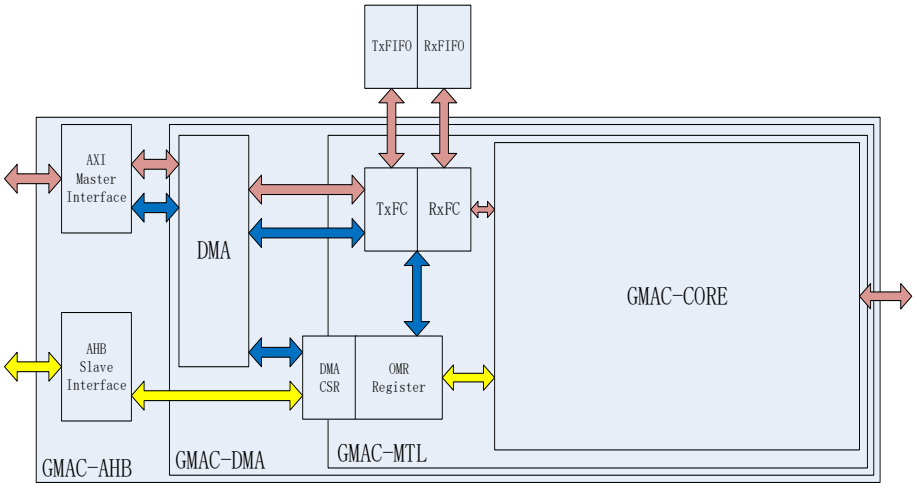


Figure 34-1 GMAC Block Diagram

34.4 Functional Description

The GMAC enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard. The GMAC is a configurable product that can be optimized for gate count and latency to meet the application requirements. You can use the GMAC in number of applications such as switches and network interface cards.

34.5 Pins Description

Table 34-1 GMAC pin description

Pin	I/O	Description
PHY_CLK	Output	External PHY clock Function: The PHY_CLK is provide for External GMAC PHY, and the frequency is 50MHz
RX_DV	Input	PHY Receive Data Valid Function: This signal is driven by PHY and has multiple functions depending on which PHY interface is selected: RMII: Contains the crs and data valid information of the receive interface. Synchronous to: RX_CLK
RX_CLK	Input	RX Transmission Clock
RXD [3:0]	Input	PHY Receive Data Function: This is a bundle of two data signals received from the PHY: RMII: Bits [1:0] provide the RMII receive data. The validity of the data is qualified with phy_rxdv_o. Synchronous to: RX_CLK

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

TX_CLK	Output	TX Transmission Clock
TX_EN	Output	PHY Transmit Data Enable Function: This signal is driven by the MAC and has multiple functions depending on which PHY interface is selected: RMII: When high, indicates that valid data is being transmitted on the phy_txd bus. Synchronous to: TX_CLK
TXD [3:0]	Output	PHY Transmit Data Function: This is a group of two transmit data signals driven by the MAC. RMII: Bits [1:0] provide the RMII transmit data. The validity of the data is qualified with phy_txen_o. Synchronous to: TX_CLK
MDC	Output	Management Data Clock Function: The maximum frequency of this clock is 2.5 MHz. This clock is generated from the GMAC HCLK through a clock divider.
MDIO	I/O	MDIO is the bidirectional data signal between the MAC and the PHY that is clocked by MDC.

34.6 Data Format Description

For RMII mode , the data width is 2bits,

34.7 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   - R- Read only
   - W- Write only
   - RW- Read and Write
   - RCW- Read and Write, but Clear to 0 by Read
   - RSW- Read and Write, but Set to 1 by Read
   - RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
   - RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
   - RC- Read only, and Clear to 0 by read
   - RS- Read only, and Set to 1 by read
3. Reset Value
   - 1 - reset to 1
   - 0 - reset to 0
   - ? - value unknown after reset

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

34.7.1 Register Memory Map

Table 34-2 Registers Memory Map Base Address

Name	Base	Description
GMAC	0x134B0000	Address base of GMAC

The GMAC is controlled by a set of registers that the application configures before every operation. The following table lists all the registers.

Table 34-3 GMAC Registers Map

Name	RW	Reset Value	Address Offset	Access Size
DMA_BMR	RW	0x0002_0101	0x1000	32
DMA_TPDR	RW	0x0000_0000	0x1004	32
DMA_RPDR	RW	0x0000_0000	0x1008	32
DMA_RDLAR	RW	0x0000_0000	0x100C	32
DMA_TDLAR	RW	0x0000_0000	0x1010	32
DMA_SR	RW	0x0000_0000	0x1014	32
DMA_OMR	RW	0x0000_0000	0x1018	32
DMA_IER	RW	0x0000_0000	0x101C	32
DMA_MFOCR	RC	0x0000_0000	0x1020	32
DMA_RIWTR	RW	0x0000_0000	0x1024	32
DMA_AHBSR	R	0x0000_0000	0x102C	32
MAC_CR	RW	0x0000_0000	0x0000	32
MAC_FFR	RW	0x0000_0000	0x0004	32
MAC_HTHR	RW	0x0000_0000	0x0008	32
MAC_HTLR	RW	0x0000_0000	0x000C	32
GMII_AR	RW	0x0000_0000	0x0010	32
GMII_DR	RW	0x0000_0000	0x0014	32
MAC_FCR	RW	0x0000_0000	0x0018	32
MAC_VTR	RW	0x0000_0000	0x001C	32
MAC_DR	R	0x0000_0000	0x0024	32
LPI_CSR	RW	0x0000_0000	0x0030	32
LPI_TCR	RW	0x03E8_0000	0x0034	32
MAC_ISR	R	0x0000_0000	0x0038	32
MAC_IMR	RW	0x0000_0000	0x003C	32
MAC_A0HR	RW	0x8000_FFFF	0x0040	32
MAC_A0LR	RW	0xFFFF_FFFF	0x0044	32
MAC_A1HR	RW	0x0000_FFFF	0x0048	32
MAC_A1LR	RW	0xFFFF_FFFF	0x004C	32
MAC_WTR	RW	0x0000_0000	0x00DC	32
MAC_TCR	RW	0x0000_2000	0x0700	32
MAC_SSIR	RW	0x0000_0000	0x0704	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

MAC_STSR	R	0x0000_0000	0x0708	32
MAC_STNR	R	0x0000_0000	0x070C	32
MAC_STSUR	RW	0x0000_0000	0x0710	32
MAC_STNUR	RW	0x0000_0000	0x0714	32
MAC_TAR	RW	0x0000_0000	0x0718	32
MAC_TTSR	RW	0x0000_0000	0x071C	32
MAC_TTNR	RW	0x0000_0000	0x0720	32
MAC_STHWSR	RW	0x0000_0000	0x0724	32
MAC_TSR	RW	0x0000_0000	0x0728	32
MAR_PPSCR	RW	0x0000_0000	0x072C	32
MAR_ATNR	R	0x0000_0000	0x0730	32
MAR_ATSR	R	0x0000_0000	0x0734	32
MAR_AVCR	RW	0x0000_0000	0x0738	32
MAR_PPS0IR	RW	0x0000_0000	0x0760	32
MAR_PPS0WR	RW	0x0000_0000	0x0764	32
MAR_PPS1TTSR	RW	0x0000_0000	0x0780	32
MAR_PPS1TTNR	RW	0x0000_0000	0x0784	32

34.7.2 Register and Fields Description

34.7.2.1 DMA Bus Mode Register(DMA_BMR,0x1000)

	DMA_BMR																Base + 0x1000													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RIB	Reserved	PRWG	TXPR	MB	AAL	PLBx8	USP	RPBL							FB	PR	PBL							ATDS	DSL					DA	SWR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Name	Description	R/W
31	RIB	Rebuild INCRx Burst When this bit is set high and the AHB master gets an EBT (Retry, Split, or Losing bus grant), the AHB master interface rebuilds the pending beats of any burst transfer initiated with INCRx. The AHB master interface rebuilds the beats with a combination of specified bursts with INCRx and SINGLE. By default, the AHB master interface rebuilds pending beats of an EBT with an unspecified (INCR) burst.	RW
30	Reserved	Writing has no effect. Read as zero.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

29:28	PRWG	Channel Priority Weights This Bits sets the priority weights for Channel 0 during the round-robin arbitration between the DMA channels for the system bus. 00: The priority weight is 1. 01: The priority weight is 2. 10: The priority weight is 3. 11: The priority weight is 4	RW
27	TXPR	Transmit Priority When set, this bit indicates that the transmit DMA has higher priority than the receive DMA during arbitration for the system-side bus.	RW
26	MB	Mixed Burst When this bit is set high and the FB bit is low, the AHB master interface starts all bursts of length more than 16 with INCR (undefined burst), whereas it reverts to fixed burst transfers (INCRx and SINGLE) for burst length of 16 and less.	RW
25	AAL	Address-Aligned Beats When this bit is set high and the FB bit is equal to 1, the AHB interface generates all bursts aligned to the start address LS bits. If the FB bit is equal to 0, the first burst (accessing the start address of data buffer) is not aligned, but subsequent bursts are aligned to the address.	RW
24	PBLx8	PBLx8 Mode When set high, this bit multiplies the programmed PBL value (Bits [22:17] and Bits[13:8]) eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value.	RW
23	USP	Use Separate PBL When set high, this bit configures the Rx DMA to use the value configured in Bits [22:17] as PBL. The PBL value in Bits [13:8] is applicable only to the Tx DMA operations. When reset to low, the PBL value in Bits [13:8] is applicable for both DMA engines.	RW
22:17	RPBL	Rx DMA PBL This Bits indicates the maximum number of beats to be transferred in one Rx DMA transaction. This is the maximum value that is used in a single block Read or Write. The Rx DMA always attempts to burst as specified in the RPBL bit each time it starts a Burst transfer on the host bus. You can program RPBL with values of 1, 2, 4, 8, 16, and 32. Any other value results in undefined behavior. This Bits is valid and applicable only when USP is set high.	RW
16	FB	Fixed Burst	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		This bit controls the AHB master interface performs fixed burst transfers or not. When set, the AHB interface uses only SINGLE, INCR4, INCR8, or INCR16 during start of the normal burst transfers. When reset, the AHB interface uses SINGLE and INCR burst transfer operations.	
15:14	PR	Priority Ratio These bits control the priority ratio in the weighted round-robin arbitration between the Rx DMA and Tx DMA. These bits are valid only when Bit 1 (DA) is reset. The priority ratio is Rx:Tx or Tx:Rx depending on whether Bit 27 (TXPR) is reset or set. 00: The Priority Ratio is 1:1. 01: The Priority Ratio is 2:1. 10: The Priority Ratio is 3:1. 11: The Priority Ratio is 4:1.	RW
13:8	PBL	Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA transaction. This is the maximum value that is used in a single block Read or Write. The DMA always attempts to burst as specified in PBL each time it starts a Burst transfer on the host bus. PBL can be programmed with permissible values of 1, 2, 4, 8, 16, and 32. Any other value results in undefined behavior. When USP is set high, this PBL value is applicable only for Tx DMA transactions. If the number of beats to be transferred is more than 32, then perform the following steps: 1. Set the PBLx8 mode. 2. Set the PBL. For example, if the maximum number of beats to be transferred is 64, then first set PBLx8 to 1 and then set PBL to 8. The PBL values have the following limitation: The maximum number of possible beats (PBL) is limited by the size of the Tx FIFO and Rx FIFO in the MTL layer and the data bus width on the DMA. The FIFO has a constraint that the maximum beat supported is half the depth of the FIFO, except when specified.	RW
7	ATDS	Alternate Descriptor Size When set, the size of the alternate descriptor increases to 32 bytes (8 DWORDS). This is required when the IPC Full Checksum Offload Engine (Type 2) is enabled in the receiver. The enhanced descriptor is not required if the IPC Full Checksum Offload Engine (Type 2) features are not enabled. In such case, you can use the 16 bytes descriptor to save 4 bytes of memory. IPC Full Checksum Offload Engine (Type 2) feature Otherwise, this bit is reserved and is read-only. When reset, the descriptor size reverts back to 4 DWORDs (16	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		bytes). This bit preserves the backward compatibility for the descriptor size. In versions prior to 3.50a, the descriptor size is 16 bytes for both normal and enhanced descriptors.	
6:2	DSL	Descriptor Skip Length This bit specifies the number of Word, Dword, or Lword (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of current descriptor to the start of next descriptor. When the DSL value is equal to zero, the descriptor table is taken as contiguous by the DMA in Ring mode.	RW
1	DA	DMA Arbitration Scheme This bit specifies the arbitration scheme between the transmit and receive paths of Channel 0. 0: Weighted round-robin with Rx:Tx or Tx:Rx The priority between the paths is according to the priority specified in Bits [15:14] (PR) and priority weights specified in Bit 27 (TXPR). 1: Fixed priority The transmit path has priority over receive path when Bit 27 (TXPR) is set. Otherwise, receive path has priority over the transmit path.	RW
0	SWR	Software Reset When this bit is set, the MAC DMA Controller resets the logic and all internal registers of the MAC. It is cleared automatically after the reset operation is complete in all of the GMAC clock domains. Before reprogramming any register of the GMAC, you should read a zero (0) value in this bit. Note: The Software reset function is driven only by this bit. Bit 0 of Register 64 (Channel 1 Bus Mode Register) or Register 128 (Channel 2 Bus Mode Register) has no impact on the Software reset function. The reset operation is completed only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for the software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock.	RW[1]

Note:

1. Only support RMII mode
2. [1]:Write Set, self clear

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

34.7.2.2 DMA Transmit Poll Demand Register(DMA_TPDR,0x1004)

	DMA_TPDR																Base+ 0x1004															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TPD																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	TPD	Transmit Poll Demand When these bits are written with any value, the DMA reads the current descriptor to which the Register 18 (Current Host Transmit Descriptor Register) is pointing. If that descriptor is not available (owned by the Host), the transmission returns to the Suspend state and Bit 2 (TU) of Register 5 (Status Register) is asserted. If the descriptor is available, the transmission resumes.	RW

Note:

Only support RMII mode

34.7.2.3 DMA Receive Poll Demand Register(DMA_RPDR,0x1008)

	DMA_RPDR																Base + 0x1008															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RPD																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	RPD	Receive Poll Demand When these bits are written with any value, the DMA reads the current descriptor to which the Register 19 (Current Host Receive Descriptor Register) is pointing. If that descriptor is not available (owned by the Host), the reception returns to the Suspended state and Bit 7 (RU) of Register 5 (Status Register) is asserted. If the descriptor is available, the Rx DMA returns to the active state.	RW

Note:

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Only support RMII mode

34.7.2.4 DMA Receive Descriptor List Address Register(DMA_RDLAR,0x100C)

	DMA_RDLAR																Base + 0x100C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDESLA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	RDESLA	Start of Receive List This Bits contains the base address of the first descriptor in the Receive Descriptor list. The LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width are ignored and internally taken as all-zero by the DMA. Therefore, these LSB bits are read-only (RO).	RW

Note:

Only support RMII mode

34.7.2.5 DMA Transmit Descriptor List Address Register(DMA_TDLAR,0x1010)

	DMA_TDLAR																Base + 0x1010															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TDESLA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	TDESLA	Start of Transmit List This Bits contains the base address of the first descriptor in the Transmit Descriptor list. The LSB bits (1:0, 2:0, 3:0) for 32-bit, 64-bit, or 128-bit bus width are ignored and are internally taken as all-zero by the DMA. Therefore, these LSB bits are read-only (RO).	RW

Note:

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Only support RMII mode

34.7.2.6 DMA Status Register(DMA_SR,0x1014)

	DMA_BMR																														
																	Base + 0x1014														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	GLPLL/GTMSI	TTI	GPI	GMI	GLI	EB			TS			RS			NIS	AIS	ERI	FBI	Reserved		ETI	RWT	RPS	RU	RI	UNF	OVF	TJT	TU	TPS	TI
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	Reserved	Writing has no effect, read as zero.	R
30	GLPII OR GTMSI	GLPII: GMAC LPI Interrupt (for Channel 0) This bit indicates an interrupt event in the LPI logic of the GMAC. To reset this bit to 1'b0, the software must read the corresponding registers in the gmac to get the exact cause of the interrupt and clear its source. **Note:** GLPII status is given only in Channel 0 DMA register and is applicable only when the Energy Efficient Ethernet feature is enabled. GTMSI: GMAC TMS Interrupt (for Channel 1 and Channel 2) This bit indicates an interrupt event in the traffic manager and scheduler logic of gmac. To reset this bit, the software must read the corresponding registers (Channel Status Register) to get the exact cause of the interrupt and clear its source.	R
29	TTI	Reserved	R
28	GPI	GMAC PMT Interrupt This bit indicates an interrupt event in the PMT module of the gmac. The software must read the PMT Control and Status Register in the MAC to get the exact cause of interrupt and clear its source to reset this bit to 1'b0. The interrupt signal from the gmac subsystem is high when this bit is high.	R
27	GMI	GMAC MMC Interrupt This bit reflects an interrupt event in the MMC module of the GMAC. The software must read the corresponding registers in the GMAC to get the exact cause of the interrupt and clear the source of interrupt to make this bit as 1'b0. The interrupt signal from the gmac subsystem is high when this bit is high.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		This bit is applicable only when the MAC Management Counters (MMC) are enabled. Otherwise, this bit is reserved.	
26	GLI	GMAC Line Interface Interrupt When set, this bit reflects any of the following interrupt events in the GMAC interfaces: RGMII: Link change event To identify the exact cause of the interrupt, the software must first read Bit 11 and Bits[2:0] of Register 14 (Interrupt Status Register) and then to clear the source of interrupt (which also clears the GLI interrupt), read any of the following corresponding registers: PCS (TBI, RTBI, or SGMII): Register 49 (AN Status Register) RGMII: Register 54 (RGMII Control and Status Register) General Purpose Input (GPI): Register 56 (General Purpose IO Register)	R
25:23	EB	Error Bits This Bits indicates the type of error that caused a Bus Error, for example, error response on the AHB interface. This Bits is valid only when Bit 13 (FBI) is set. This Bits does not generate an interrupt. 0 0 0: Error during Rx DMA Write Data Transfer 0 1 1: Error during Tx DMA Read Data Transfer 1 0 0: Error during Rx DMA Descriptor Write Access 1 0 1: Error during Tx DMA Descriptor Write Access 1 1 0: Error during Rx DMA Descriptor Read Access 1 1 1: Error during Tx DMA Descriptor Read Access **Note:** 001 and 010 are reserved.	R
22:20	TS	Transmit Process State This Bits indicates the Transmit DMA FSM state. This Bits does not generate an interrupt. 3'b000: Stopped; Reset or Stop Transmit Command issued 3'b001: Running; Fetching Transmit Transfer Descriptor 3'b010: Running; Waiting for status 3'b011: Running; Reading Data from host memory buffer and queuing it to transmit buffer (Tx FIFO) 3'b100: Reserved for future use 3'b101: Reserved for future use 3'b110: Suspended; Transmit Descriptor Unavailable or Transmit Buffer Underflow 3'b111: Running; Closing Transmit Descriptor	R
19:17	RS	Receive Process State This Bits indicates the Receive DMA FSM state. This Bits does not generate an interrupt. 3'b000: Stopped: Reset or Stop Receive Command issued	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		3'b001: Running: Fetching Receive Transfer Descriptor 3'b010: Reserved for future use 3'b011: Running: Waiting for receive packet 3'b100: Suspended: Receive Descriptor Unavailable 3'b101: Running: Closing Receive Descriptor 3'b110: TIME_STAMP write state 3'b111: Running: Transferring the receive packet data from receive buffer to host memory	
16	NIS	Normal Interrupt Summary Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in Register 7 (Interrupt Enable Register): Register 5[0]: Transmit Interrupt Register 5[2]: Transmit Buffer Unavailable Register 5[6]: Receive Interrupt Register 5[14]: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in Register 7) affect the Normal Interrupt Summary bit. This is a sticky bit and must be cleared (by writing 1 to this bit) each time a corresponding bit, which causes NIS to be set, is cleared.	RW[1]
15	AIS	Abnormal Interrupt Summary Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in Register 7 (Interrupt Enable Register): Register 5[1]: Transmit Process Stopped Register 5[3]: Transmit Jabber Timeout Register 5[4]: Receive FIFO Overflow Register 5[5]: Transmit Underflow Register 5[7]: Receive Buffer Unavailable Register 5[8]: Receive Process Stopped Register 5[9]: Receive Watchdog Timeout Register 5[10]: Early Transmit Interrupt Register 5[13]: Fatal Bus Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit and must be cleared (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared.	RW[2]
14	ERI	Early Receive Interrupt This bit indicates that the DMA filled the first data buffer of the packet. This bit is cleared when the software writes 1 to this bit or Bit 6 (RI) of this register is set (whichever occurs earlier).	RW[3]
13	FBI	Fatal Bus Error Interrupt	RW[4]

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		This bit indicates that a bus error occurred, as described in Bits [25:23]. When this bit is set, the corresponding DMA engine disables all of its bus accesses.	
12:11	Reserved	Writing has no effect, read as zero.	R
10	ETI	Early Transmit Interrupt This bit indicates that the frame to be transmitted is fully transferred to the MTL Transmit FIFO.	RW[5]
9	RWT	Receive Watchdog Timeout When set, this bit indicates that the Receive Watchdog Timer expired while receiving the current frame and the current frame is truncated after the watchdog timeout.	RW[6]
8	RPS	Receive Process Stopped This bit is asserted when the Receive Process enters the Stopped state.	RW[7]
7	RU	Receive Buffer Unavailable This bit indicates that the host owns the Next Descriptor in the Receive List and the DMA cannot acquire it. The Receive Process is suspended. To resume processing Receive descriptors, the host should change the ownership of the descriptor and issue a Receive Poll Demand command. If no Receive Poll Demand is issued, the Receive Process resumes when the next recognized incoming frame is received. This bit is set only when the previous Receive Descriptor is owned by the DMA.	RW[8]
6	RI	Receive Interrupt This bit indicates that the frame reception is complete. When reception is complete, the Bit 31 of RDES1 (Disable Interrupt on Completion) is reset in the last Descriptor, and the specific frame status information is updated in the descriptor. The reception remains in the Running state.	RW[9]
5	UNF	Transmit Underflow This bit indicates that the Transmit Buffer had an Underflow during frame transmission. Transmission is suspended and an Underflow Error TDES0[1] is set.	RW[10]
4	OVF	Receive Overflow This bit indicates that the Receive Buffer had an Overflow during frame reception. If the partial frame is transferred to the application, the overflow status is set in RDES0[11].	RW[11]
3	TJT	Transmit Jabber Timeout This bit indicates that the Transmit Jabber Timer expired, which happens when the frame size exceeds 2,048 (10,240 bytes when the Jumbo frame is enabled).	RW[12]

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		When the Jabber Timeout occurs, the transmission process is aborted and placed in the Stopped state. This causes the Transmit Jabber Timeout TDES0[14] flag to assert.	
2	TU	Transmit Buffer Unavailable This bit indicates that the host owns the Next Descriptor in the Transmit List and the DMA cannot acquire it. Transmission is suspended. Bits[22:20] explain the Transmit Process state transitions. To resume processing Transmit descriptors, the host should change the ownership of the descriptor by setting TDES0[31] and then issue a Transmit Poll Demand command.	RW[13]
1	TPS	Transmit Process Stopped This bit is set when the transmission is stopped.	RW[14]
0	TI	Transmit Interrupt This bit indicates that the frame transmission is complete. When transmission is complete, Bit 31 (OWN) of TDES0 is reset, and the specific frame status information is updated in the descriptor.	RW[15]

Note:

1. Only support RMII mode
2. [1]~[15]:This bits will operate with Self set, read clear function.

34.7.2.7 DMA Operation Mode Register(DMA_OMR,0x1018)

	DMA_OMR																Base + 0x1018													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					DT	RSF	DFF	Reserved		TSF	FTF	Reserved				TTC		ST	RFD		RFA		EFC	FEF	FUF	DGF	RTC		OSF	SR	Reserved
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:27	Reserved	Writing has no effect, read as zero.	R
26	DT	Disable Dropping of TCP/IP Checksum Error Frames When this bit is set, the MAC does not drop the frames which only have errors detected by the Receive Checksum Offload engine. Such frames do not have any errors (including FCS error) in the Ethernet frame received by the MAC but have errors only in the encapsulated payload. When this bit is reset, all error frames are dropped if the FEF bit is reset. If the IPC Full Checksum Offload Engine (Type 2) is disabled, this	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		bit is reserved (RO with value 1'b0).	
25	RSF	Receive Store and Forward When this bit is set, the MTL reads a frame from the Rx FIFO only after the complete frame has been written to it, ignoring the RTC bits. When this bit is reset, the Rx FIFO operates in the cut-through mode, subject to the threshold specified by the RTC bits.	RW
24	DFF	Disable Flushing of Received Frames When this bit is set, the Rx DMA does not flush any frames because of the unavailability of receive descriptors or buffers as it does normally when this bit is reset.	RW
23:22	Reserved	Writing has no effect, read as zero.	R
21	TSF	Transmit Store and Forward When this bit is set, transmission starts when a full frame resides in the MTL Transmit FIFO. When this bit is set, the TTC values specified in Bits [16:14] are ignored. This bit should be changed only when the transmission is stopped.	RW
20	FTF	Flush Transmit FIFO When this bit is set, the transmit FIFO controller logic is reset to its default values and thus all data in the Tx FIFO is lost or flushed. This bit is cleared internally when the flushing operation is complete. The Operation Mode register should not be written to until this bit is cleared. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt frame transmission. Note: The flush operation is complete only when the Tx FIFO is emptied of its contents and all the pending Transmit Status of the transmitted frames are accepted by the host. In order to complete this flush operation, the PHY transmit clock is required to be active.	RW[1]
19:17	Reserved	Writing has no effect, read as zero.	R
16:14	TTC	Transmit Threshold Control These bits control the threshold level of the MTL Transmit FIFO. Transmission starts when the frame size within the MTL Transmit FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are also transmitted. These bits are used only when Bit 21 (TSF) is reset. ▪ 000: 64 ▪ 001: 128 ▪ 010: 192 ▪ 011: 256 ▪ 100: 40 ▪ 101: 32	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		▪ 110: 24 ▪ 111: 16	
13	ST	Start or Stop Transmission Command When this bit is set, transmission is placed in the Running state, and the DMA checks the Transmit List at the current position for a frame to be transmitted. Descriptor acquisition is attempted either from the current position in the list, which is the Transmit List Base Address set by Register 4 (Transmit Descriptor List Address Register), or from the position retained when transmission was stopped previously. If the DMA does not own the current descriptor, transmission enters the Suspended state and Bit 2 (Transmit Buffer Unavailable) of Register 5 (Status Register) is set. The Start Transmission command is effective only when transmission is stopped. If the command is issued before setting Register 4 (Transmit Descriptor List Address Register), then the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current frame. The Next Descriptor position in the Transmit List is saved, and it becomes the current position when transmission is restarted. To change the list address, you need to program Register 4 (Transmit Descriptor List Address Register) with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current frame is complete or the transmission is in the Suspended state.	RW
12:11	RFD	Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (Fill-level of Rx FIFO) at which the flow control is de-asserted after activation. ▪ 00: Full minus 1 KB, that is, FULL — 1 KB ▪ 01: Full minus 2 KB, that is, FULL — 2 KB ▪ 10: Full minus 3 KB, that is, FULL — 3 KB ▪ 11: Full minus 4 KB, that is, FULL — 4 KB The de-assertion is effective only after flow control is asserted. If the Rx FIFO is 8 KB or more, an additional Bit (RFD_2) is used for more threshold levels as described in Bit 22. These bits are reserved and read-only when the Rx FIFO depth is less than 4 KB.	RW
10:9	RFA	Threshold for Activating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (Fill level of Rx FIFO) at which the flow control is activated. ▪ 00: Full minus 1 KB, that is, FULL—1KB. ▪ 01: Full minus 2 KB, that is, FULL—2KB. ▪ 10: Full minus 3 KB, that is, FULL—3KB. ▪ 11: Full minus 4 KB, that is, FULL—4KB. These values are applicable only to Rx FIFOs of 4 KB or more and when Bit 8 (EFC) is set high. If the Rx FIFO is 8 KB or	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		more, an additional Bit (RFA_2) is used for more threshold levels as described in Bit 23. These bits are reserved and read-only when the depth of Rx FIFO is less than 4 KB.	
8	EFC	Enable HW Flow Control When this bit is set, the flow control signal operation based on the fill-level of Rx FIFO is enabled. When reset, the flow control operation is disabled. This bit is not used (reserved and always reset) when the Rx FIFO is less than 4 KB.	RW
7	FEF	Forward Error Frames When this bit is reset, the Rx FIFO drops frames with error status (CRC error, collision error, GMII_ER, giant frame, watchdog timeout, or overflow). However, if the start byte (write) pointer of a frame is already transferred to the read controller side (in Threshold mode), then the frame is not dropped. When the FEF bit is set, all frames except runt error frames are forwarded to the DMA. If the Bit 25 (RSF) is set and the Rx FIFO overflows when a partial frame is written, then the frame is dropped irrespective of the FEF bit setting. However, if the Bit 25 (RSF) is reset and the Rx FIFO overflows when a partial frame is written, then a partial frame may be forwarded to the DMA. **Note:** When FEF bit is reset, the giant frames are dropped if the giant frame status is given in Rx Status in the following configurations: The IP checksum engine (Type 1) and full checksum offload engine (Type 2) are not selected.	RW
6	FUF	Forward Undersized Good Frames When set, the Rx FIFO forwards Undersized frames (that is, frames with no Error and length less than 64 bytes) including pad-bytes and CRC. When reset, the Rx FIFO drops all frames of less than 64 bytes, unless a frame is already transferred because of the lower value of Receive Threshold, for example, RTC = 01.	RW
5	DGF	Drop Giant Frames When set, the MAC drops the received giant frames in the Rx FIFO, that is, frames that are larger than the computed giant frame limit. When reset, the MAC does not drop the giant frames in the Rx FIFO.	RW
4:3	RTC	Receive Threshold Control These two bits control the threshold level of the MTL Receive FIFO. Transfer (request) to DMA starts when the frame size within the MTL Receive FIFO is larger than the threshold. In addition, full frames with length less than the threshold are automatically transferred. The value of 11 is not applicable if the configured Receive FIFO size is 128 bytes.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		These bits are valid only when the RSF bit is zero, and are ignored when the RSF bit is set to 1. ▪ 00: 64 ▪ 01: 32 ▪ 10: 96 ▪ 11: 128	
2	OSF	Operate on Second Frame When this bit is set, it instructs the DMA to process the second frame of the Transmit data even before the status for the first frame is obtained.	RW
1	SR	Start or Stop Receive When this bit is set, the Receive process is placed in the Running state. The DMA attempts to acquire the descriptor from the Receive list and processes the incoming frames. The descriptor acquisition is attempted from the current position in the list, which is the address set by the Register 3 (Receive Descriptor List Address Register) or the position retained when the Receive process was previously stopped. If the DMA does not own the descriptor, reception is suspended and Bit 7 (Receive Buffer Unavailable) of Register 5 (Status Register) is set. The Start Receive command is effective only when the reception has stopped. If the command is issued before setting Register 3 (Receive Descriptor List Address Register), the DMA behavior is unpredictable. When this bit is cleared, the Rx DMA operation is stopped after the transfer of the current frame. The next descriptor position in the Receive list is saved and becomes the current position after the Receive process is restarted. The Stop Receive command is effective only when the Receive process is in either the Running (waiting for receive packet) or in the Suspended state. **Note:** For information about how to pause the transmission, see "Stopping and Starting Transmission".	RW
0	-	Reserved	R

Note:

Only support RMII mode

34.7.2.8 DMA Interrupt Enable Register(DMA_IER,0x101C)

	DMA_IER																Base + 0x101C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	Reserved															NIE	AIE	ERE	FBEE	Reserved		ETE	RWE	RSE	RUE	RIE	UNE	OVE	TJE	TUE	TSE	TIE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:17	Reserved	Writing has no effect, read as zero.	R
16	NIE	Normal Interrupt Summary Enable When this bit is set, normal interrupt summary is enabled. When this bit is reset, normal interrupt summary is disabled. This bit enables the following interrupts in Register 5 (Status Register): ▪ Register 5[0]: Transmit Interrupt ▪ Register 5[2]: Transmit Buffer Unavailable ▪ Register 5[6]: Receive Interrupt ▪ Register 5[14]: Early Receive Interrupt	RW
15	AIE	Abnormal Interrupt Summary Enable When this bit is set, abnormal interrupt summary is enabled. When this bit is reset, the abnormal interrupt summary is disabled. This bit enables the following interrupts in Register 5 (Status Register): ▪ Register 5[1]: Transmit Process Stopped ▪ Register 5[3]: Transmit Jabber Timeout ▪ Register 5[4]: Receive Overflow ▪ Register 5[5]: Transmit Underflow ▪ Register 5[7]: Receive Buffer Unavailable ▪ Register 5[8]: Receive Process Stopped ▪ Register 5[9]: Receive Watchdog Timeout ▪ Register 5[10]: Early Transmit Interrupt ▪ Register 5[13]: Fatal Bus Error	RW
14	ERE	Early Receive Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Early Receive Interrupt is enabled. When this bit is reset, the Early Receive Interrupt is disabled.	RW
13	FBEE	Fatal Bus Error Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Fatal Bus Error Interrupt is enabled. When this bit is reset, the Fatal Bus Error Enable Interrupt is disabled.	RW
12:11	Reserved	Writing has no effect, read as zero.	R
10	ETE	Early Transmit Interrupt Enable When this bit is set with an Abnormal Interrupt Summary Enable (Bit 15), the Early Transmit Interrupt is enabled. When this bit is reset, the Early Transmit Interrupt is disabled.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

9	RWE	Receive Watchdog Timeout Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Watchdog Timeout Interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout Interrupt is disabled.	RW
8	RSE	Receive Stopped Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped Interrupt is disabled.	RW
7	RUE	Receive Buffer Unavailable Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Buffer Unavailable Interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable Interrupt is disabled.	RW
6	RIE	Receive Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled.	RW
5	UNE	Underflow Interrupt Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Transmit Underflow Interrupt is enabled. When this bit is reset, the Underflow Interrupt is disabled.	RW
4	OVE	Overflow Interrupt Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Overflow Interrupt is enabled. When this bit is reset, the Overflow Interrupt is disabled.	RW
3	TJE	Transmit Jabber Timeout Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Transmit Jabber Timeout Interrupt is enabled. When this bit is reset, the Transmit Jabber Timeout Interrupt is disabled.	RW
2	TUE	Transmit Buffer Unavailable Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Transmit Buffer Unavailable Interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable Interrupt is disabled.	RW
1	TSE	Transmit Stopped Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Transmission Stopped Interrupt is enabled. When this bit is reset, the Transmission Stopped Interrupt is disabled.	RW
0	TIE	Transmit Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled.	RW

Note:

Only support RMII mode

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

34.7.2.9 DMA Missed Frame and Buffer Overflow Counter Register(DMA_MFOCR,0x1020)

	DMA_MFOCR																														Base + 0x1020	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			OVFCNTOVF	MISCNTOVF											MISCNTOVF	MISFRMCNT																	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:29	Reserved	Writing has no effect, read as zero.	R
28	OVFCNTOVF	Overflow Bit for FIFO Overflow Counter This bit is set every time the Overflow Frame Counter (Bits[27:17]) overflows, that is, the Rx FIFO overflows with the overflow frame counter at maximum value. In such a scenario, the overflow frame counter is reset to all-zeros and this bit indicates that the rollover happened.	RC[1]
27:17	OVFFRMCNT	Overflow Frame Counter This Bits indicates the number of frames missed by the application. This counter is incremented each time the MTL FIFO overflows. The counter is cleared when this register is read with mci_be_i[2] at 1'b1.	RC[2]
16	MISCNTOVF	Overflow Bit for Missed Frame Counter This bit is set every time Missed Frame Counter (Bits[15:0]) overflows, that is, the DMA discards an incoming frame because of the Host Receive Buffer being unavailable with the missed frame counter at maximum value. In such a scenario, the Missed frame counter is reset to all-zeros and this bit indicates that the rollover happened.	RC[3]
15:0	MISFRMCNT	Missed Frame Counter This Bits indicates the number of frames missed by the controller because of the Host Receive Buffer being unavailable. This counter is incremented each time the DMA discards an incoming frame. The counter is cleared when this register is read with mci_be_i[0] at 1'b1.	RC[4]

Note:1. Only support RMII mode

2. [1]~[4]:This bits will operate with Self set, read clear function.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

34.7.2.10 DMA Receive Interrupt Watchdog Timer Register(DMA_RIWTR,0x1024)

	DMA_BMR																Base + 0x1024															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								RIWT							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:8	Reserved	Writing has no effect, read as zero.	R
7:0	RIWT	RI Watchdog Timer Count This bit indicates the number of system clock cycles multiplied by 256 for which the watchdog timer is set. The watchdog timer gets triggered with the programmed value after the Rx DMA completes the transfer of a frame for which the RI status bit is not set because of the setting in the corresponding descriptor RDES1[31]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per RDES1[31] of any received frame.	RW

Note:Only support RMII mode

34.7.2.11 DMA AHB State Register(DMA_AHBSR,0x102C)

	DMA_AHBSR																Base + 0x102C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															AXWHSTS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:1	Reserved	Writing has no effect, read as zero.	R
0	AXWHSTS	AHB Master Status	R

Note:Only support RMII mode

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

34.7.2.12 MAC Configuration Register(MAC_CR,0x0000)

	MAC_CR																														Base + 0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	SARC			TWOKPE	Reserved	CST	TC	WD	JD	BE	JE	IFG			DCRS	PS	FES	DO	LM	DM	IPC	DR	LUD	ACS	BL		DC	TE	RE	PRELEN	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	Reserved	Writing has no effect, read as zero.	R
30:28	SARC	Source Address Insertion or Replacement Control This Bits controls the source address insertion or replacement for all transmitted frames. Bit 30 specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits [29:28]: 2'b0*x*: The input signals mti_sa_ctrl_i and ati_sa_ctrl_i control the SA Bits generation. 2'b10: If Bit 30 is set to 0, the MAC inserts the content of the MAC Address 0 registers (registers 16 and 17) in the SA Bits of all transmitted frames. If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected during core configuration, the MAC inserts the content of the MAC Address 1 registers (registers 18 and 19) in the SA Bits of all transmitted frames. 2'b11: If Bit 30 is set to 0, the MAC replaces the content of the MAC Address 0 registers (registers 16 and 17) in the SA Bits of all transmitted frames. If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected during core configuration, the MAC replaces the content of the MAC Address 1 registers (registers 18 and 19) in the SA Bits of all transmitted frames. **Note:** Changes to this Bits take effect only on the start of a frame. If you write this register Bits when a frame is being transmitted, only the subsequent frame can use the updated value, that is, the current frame does not use the updated value. These bits are reserved and RO when the Enable SA, VLAN, and CRC Insertion on TX feature is not selected during core configuration.	RW
27	TWOKPE	IEEE 802.3as Support for 2K Packets	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		When set, the MAC considers all frames, with up to 2,000 bytes length, as normal packets. When Bit 20 (JE) is not set, the MAC considers all received frames of size more than 2K bytes as Giant frames. When this bit is reset and Bit 20 (JE) is not set, the MAC considers all received frames of size more than 1,518 bytes (1,522 bytes for tagged) as Giant frames. When Bit 20 is set, setting this bit has no effect on Giant Frame status. For more information about how the setting of this bit and Bit 20 impact the Giant frame status.	
26	Reserved	Writing has no effect, read as zero.	RW
25	CST	CRC Stripping for Type Frames When this bit is set, the last 4 bytes (FCS) of all frames of Ether type (Length/Type Bits greater than or equal to 1,536) are stripped and dropped before forwarding the frame to the application. This function is not valid when the IP Checksum Engine (Type 1) is enabled in the MAC receiver. This function is valid when Type 2 Checksum Offload Engine is enabled. **Note:** For information about how the settings of Bit 7 (ACS) and this bit impact the frame length.	RW
24	TC	Transmit Configuration in RGMII When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMI port. When this bit is reset, no such information is driven to the PHY.	RW
23	WD	Watchdog Disable When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive frames of up to 16,384 bytes. When this bit is reset, the MAC does not allow a receive frame which more than 2,048 bytes (10,240 if JE is set high) or the value programmed in Register 55 (Watchdog Timeout Register). The MAC cuts off any bytes received after the watchdog limit number of bytes.	RW
22	JD	Jabber Disable When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer frames of up to 16,384 bytes. When this bit is reset, the MAC cuts off the transmitter if the application sends out more than 2,048 bytes of data (10,240 if JE is set high) during transmission.	RW
21	BE	Frame Burst Enable When this bit is set, the MAC allows frame bursting during transmission in the GMII half-duplex mode. This bit is reserved (and RO) in the 10/100 Mbps only or full-duplex-only configurations.	RW
20	JE	Jumbo Frame Enable When this bit is set, the MAC allows Jumbo frames of 9,018 bytes	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		(9,022 bytes for VLAN tagged frames) without reporting a giant frame error in the receive frame status.	
19:17	IFG	Inter-Frame Gap These bits control the minimum IFG between frames during transmission. 000: 96 bit times 001: 88 bit times 010: 80 bit times ... 111: 40 bit times In the half-duplex mode, the minimum IFG can be configured only for 64 bit times (IFG = 100). Lower values are not considered. In the 1000-Mbps mode, the minimum IFG supported is 80 bit times.	RW
16	DCRS	Disable Carrier Sense During Transmission When set high, this bit makes the MAC transmitter ignore the (G)MII CRS signal during frame transmission in the half-duplex mode. This request results in no errors generated because of Loss of Carrier or No Carrier during such transmission. When this bit is low, the MAC transmitter generates such errors because of Carrier Sense and can even abort the transmissions. This bit is reserved (and RO) in the full-duplex-only configurations.	RW
15	PS	Port Select This bit selects the Ethernet line speed. 0: For 1000 Mbps operations 1: For 10 or 100 Mbps operations In 10 or 100 Mbps operations, this bit, along with FES bit, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only with the appropriate value. In default 10/100/1000 Mbps configuration, this bit is R_W.	RW
14	FES	Speed This bit selects the speed in the MII, RMII, RGMII or GMII interface: 0: 10 Mbps 1: 100 Mbps	RW
13	DO	Disable Receive Own When this bit is set, the MAC disables the reception of frames when the TXEN is asserted in the half-duplex mode. When this bit is reset, the MAC receives all packets that are given by the PHY while transmitting. This bit is not applicable if the MAC is operating in the full-duplex mode. This bit is reserved (RO with default value) if the MAC is configured for the full-duplex-only operation.	RW
12	LM	Loopback Mode	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Receive clock input (RX_CLK) is required for the loopback to work properly, because the Transmit clock is not looped-back internally.	
11	DM	Duplex Mode When this bit is set, the MAC operates in the full-duplex mode where it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configuration.	RW
10	IPC	Checksum Offload When this bit is set, the MAC calculates the 16-bit one's complement of the one's complement sum of all received Ethernet frame payloads. It also checks whether the IPv4 Header checksum (assumed to be bytes 25-26 or 29-30 (VLAN- tagged) of the received Ethernet frame) is correct for the received frame and gives the status in the receive status word. The MAC also appends the 16-bit checksum calculated for the IP header datagram payload (bytes after the IPv4 header) and appends it to the Ethernet frame transferred to the application (when Type 2 COE is deselected). When this bit is reset, this function is disabled. When Type 2 COE is selected, this bit, when set, enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled and the corresponding PCE and IP HCE status bits are always cleared.	RW
9	DR	Disable Retry When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current frame transmission and reports a Frame Abort with excessive collision error in the transmit frame status. When this bit is reset, the MAC attempts retries based on the settings of the BL Bits (Bits [6:5]). This bit is applicable only in the half-duplex mode and is reserved (RO with default value) in the full-duplex-only configuration.	RW
8	LUD	Link Up or Down This bit indicates whether the link is up or down during the transmission of configuration in the RGMI: 0: Link Down 1: Link Up	RW
7	ACS	Automatic Pad or CRC Stripping When this bit is set, the MAC strips the Pad or FCS Bits on the incoming frames only if the value of the length Bits is less than 1,536 bytes. All received frames with length Bits greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		FCS Bits. When this bit is reset, the MAC passes all incoming frames, without modifying them, to the Host. **Note:** For information about how the settings of Bit 23 (CST) and this bit impact the frame length.	
6:5	BL	Back-Off Limit The Back-Off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000 Mbps and 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. This bit is applicable only in the half-duplex mode and is reserved (RO) in the full-duplex-only configuration. 00: k= min (*n*, 10) 01: k = min (*n*, 8) 10: k = min (*n*, 4) 11: k = min (*n*, 1) where *n* = retransmission attempt. The random integer *r* takes the value in the range $0 \leq r < 2^k$	RW
4	DC	Deferral Check When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Frame Abort status, along with the excessive deferral error bit set in the transmit frame status, when the transmit state machine is deferred for more than 24,288 bit times in the 10 or 100 Mbps mode. If the MAC is configured for 1000 Mbps operation or if the Jumbo frame mode is enabled in the 10 or 100 Mbps mode, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and then the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0 and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode and is reserved (RO) in the full-duplex-only configuration.	RW
3	TE	Transmitter Enable When this bit is set, the transmit state machine of the MAC is enabled for transmission on the GMII or MII. When this bit is reset, the MAC transmit state machine is disabled after the completion of the	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		transmission of the current frame, and does not transmit any further frames.	
2	RE	Receiver Enable When this bit is set, the receiver state machine of the MAC is enabled for receiving frames from the GMII or MII. When this bit is reset, the MAC receive state machine is disabled after the completion of the reception of the current frame, and does not receive any further frames from the GMII or MII.	RW
1:0	PRELEN	Preamble Length for Transmit frames These bits control the number of preamble bytes that are added to the beginning of every Transmit frame. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. 2'b00: 7 bytes of preamble 2'b01: 5 bytes of preamble 2'b10: 3 bytes of preamble 2'b11: Reserved	RW

Note:Only support RMII mode

34.7.2.13 MAC Frame Filter Register(MAC_FFR,0x0004)

	MAC_FFR																Base + 0x0004											
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RA	Reserved														VTFE	Reserved					HPF	SAF	SAIF	PCF		DBF	PM	DAIF	HMC	HUC	PR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	RA	Receive All When this bit is set, the MAC Receiver module passes all received frames, irrespective of whether they pass the address filter or not, to the Application. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bits in the Receive Status Word. When this bit is reset, the Receiver module passes only those frames to the Application that pass the SA or DA address filter.	RW
30:17	Reserved	Writing has no effect, read as zero.	R
16	VTFE	VLAN Tag Filter Enable When set, this bit enables the MAC to drop VLAN tagged frames that do not match the VLAN Tag comparison. When reset, the MAC forwards all frames irrespective of the match status of the VLAN Tag.	RW
15:11	Reserved	Writing has no effect, read as zero.	RW
10	HPF	Hash or Perfect Filter	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		When this bit is set, it configures the address filter to pass a frame if it matches either the perfect filtering or the hash filtering as set by the HMC or HUC bits. When this bit is low and the HUC or HMC bit is set, the frame is passed only if it matches the Hash filter.	
9	SAF	Source Address Filter Enable When this bit is set, the MAC compares the SA Bits of the received frames with the values programmed in the enabled SA registers. If the comparison fails, the MAC drops the frame. When this bit is reset, the MAC forwards the received frame to the application with updated SAF bit of the Rx Status depending on the SA address comparison. **Note:** According to the IEEE specification, Bit 47 of the SA is reserved and set to 0. However, in gmac, the MAC compares all 48 bits. The software driver should take this into consideration while programming the MAC address registers for SA.	RW
8	SAIF	SA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the SA address comparison. The frames whose SA matches the SA registers are marked as failing the SA Address filter. When this bit is reset, frames whose SA does not match the SA registers are marked as failing the SA Address filter.	RW
7:6	PCF	Pass Control Frames These bits control the forwarding of all control frames (including unicast and multicast Pause frames). 00: MAC filters all control frames from reaching the application. 01: MAC forwards all control frames except Pause frames to application even if they fail the Address filter. 10: MAC forwards all control frames to application even if they fail the Address Filter. 11: MAC forwards control frames that pass the Address Filter. The following conditions should be true for the Pause frames processing: Condition 1: The MAC is in the full-duplex mode and flow control is enabled by setting Bit 2 (RFE) of Register 6 (Flow Control Register) to 1. Condition 2: The destination address (DA) of the received frame matches the special multicast address or the MAC Address 0 when Bit 3 (UP) of the Register 6 (Flow Control Register) is set. Condition 3: The Type Bits of the received frame is 0x8808 and the OPCODE Bits is 0x0001. **Note:** This Bits should be set to 01 only when the Condition 1 is true,	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		that is, the MAC is programmed to operate in the full-duplex mode and the RFE bit is enabled. Otherwise, the Pause frame filtering may be inconsistent. When Condition 1 is false, the Pause frames are considered as generic control frames. Therefore, to pass all control frames (including Pause frames) when the full-duplex mode and flow control is not enabled, you should set the PCF Bits to 10 or 11 (as required by the application).	
5	DBF	Disable Broadcast Frames When this bit is set, the AFM module blocks all incoming broadcast frames. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast frames.	RW
4	PM	Pass All Multicast When set, this bit indicates that all received frames with a multicast destination address (first bit in the destination address Bits is '1') are passed. When reset, filtering of multicast frame depends on HMC bit.	RW
3	DAIF	DA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast frames. When reset, normal filtering of frames is performed.	RW
2	HMC	Hash Multicast When set, MAC performs destination address filtering of received multicast frames according to the hash table. When reset, the MAC performs a perfect destination address filtering for multicast frames, that is, it compares the DA Bits with the values programmed in DA registers.	RW
1	HUC	Hash Unicast When set, MAC performs destination address filtering of unicast frames according to the hash table. When reset, the MAC performs a perfect destination address filtering for unicast frames, that is, it compares the DA Bits with the values programmed in DA registers.	RW
0	PR	Promiscuous Mode When this bit is set, the Address Filter module passes all incoming frames irrespective of the destination or source address. The SA or DA Filter Fails status bits of the Receive Status Word are always cleared when PR is set.	RW

Note:

Only support RMII mode

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

34.7.2.14 MAC Hash Table High Register(MAC_HTHR,0x0008)

	MAC_HTHR																															Base + 0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HTH																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	HTH	Hash Table High This Bits contains the upper 32 bits of the Hash table.	RW

Note:

Only support RMII mode

34.7.2.15 MAC Hash Table Low Register(MAC_HTLR,0x000C)

	MAC_HTLR																															Base + 0x000C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HTL																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	HTL	Hash Table Low This Bits contains the lower 32 bits of the Hash table.	RW

Note:

Only support RMII mode

34.7.2.16 GMII Address Register(GMII_AR,0x0010)

	GMII_AR																															Base + 0x0010
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PA					GR					CR				GW	GB	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

31:16	Reserved	Writing has no effect, read as zero.	R
15:11	PA	Physical Layer Address This Bits indicates which of the 32 possible PHY devices are being accessed.	RW
10:6	GR	GMII Register These bits select the desired GMII register in the selected PHY device.	RW
5:2	CR	CSR Clock Range The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design. The suggested range of CSR clock frequency applicable for each value (when Bit[5] = 0) ensures that the MDC clock is approximately between the frequency range 1.0 MHz-2.5 MHz. 0000: The CSR clock frequency is 60-100 MHz and the MDC clock frequency is CSR clock/42. 0001: The CSR clock frequency is 100-150 MHz and the MDC clock frequency is CSR clock/62. 0010: The CSR clock frequency is 20-35 MHz and the MDC clock frequency is CSR clock/16. 0011: The CSR clock frequency is 35-60 MHz and the MDC clock frequency is CSR clock/26. 0100: The CSR clock frequency is 150-250 MHz and the MDC clock frequency is CSR clock/102. 0101: The CSR clock frequency is 250-300 MHz and the MDC clock is CSR clock/124. 0110, 0111: Reserved When Bit 5 is set, you can achieve higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE Std 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, then the resultant MDC clock is of 12.5 MHz which is outside the limit of IEEE 802.3 specified range. Program the following values only if the interfacing chips support faster MDC clocks. 1000: CSR clock/4 1001: CSR clock/6 1010: CSR clock/8 1011: CSR clock/10 1100: CSR clock/12 1101: CSR clock/14 1110: CSR clock/16	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		1111: CSR clock/18	
1	GW	GMII Write When set, this bit indicates to the PHY that this is a Write operation using the GMII Data register. If this bit is not set, it indicates that this is a Read operation, that is, placing the data in the GMII Data register.	RW
0	GB	GMII Busy This bit should read logic 0 before writing to Register 4 and Register 5. During a PHY or RevMII register access, the software sets this bit to 1'b1 to indicate that a Read or Write access is in progress. Register 5 is invalid until this bit is cleared by the MAC. Therefore, Register 5 (GMII Data) should be kept valid until the MAC clears this bit during a PHY Write operation. Similarly for a read operation, the contents of Register 5 are not valid until this bit is cleared. The subsequent read or write operation should happen only after the previous operation is complete. Because there is no acknowledgment from the PHY to MAC after a read or write operation is completed, there is no change in the functionality of this bit even when the PHY is not present.	RW[1]

Note:1. Only support RMII mode

2. [1]:This bits will operate with Write set, read clear function.

34.7.2.17 GMII Data Register(GMII_DR,0x0014)

	GNII_DR																Base + 0x0014															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																GD															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	GD	GMII Data This Bits contains the 16-bit data value read from the PHY after a Management Read operation or the 16-bit data value to be written to the PHY before a Management Write operation.	RW

Note:

Only support RMII mode

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

34.7.2.18 MAC Flow Control Register(MAC_FCR,0x0018)

	MAC_FCR																Base+ 0x0018													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PT																Reserved								DZPQ	Reserved	PLT		UP	RFE	TFE	FCP/PBA
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16	PT	Pause Time This Bits holds the value to be used in the Pause Time Bits in the transmit control frame. If the Pause Time bits is configured to be double-synchronized to the (G)MII clock domain, then consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.	RW
15:8	Reserved	Writing has no effect, read as zero.	R
7	DZPQ	Disable Zero-Quanta Pause When this bit is set, it disables the automatic generation of the Zero-Quanta Pause frames on the de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i/mti_flowctrl_i). When this bit is reset, normal operation with automatic Zero-Quanta Pause frame generation is enabled.	RW
6	Reserved	Writing has no effect, read as zero.	R
5:4	PLT	Pause Low Threshold This Bits configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause frame. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot-times), and PLT = 01, then a second Pause frame is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256 - 28) slot times after the first Pause frame is transmitted. The following list provides the threshold values for different values: 00: The threshold is Pause time minus 4 slot times (PT - 4 slot times). 01: The threshold is Pause time minus 28 slot times (PT - 28 slot times).	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		10: The threshold is Pause time minus 144 slot times (PT - 144 slot times). 11: The threshold is Pause time minus 256 slot times (PT - 256 slot times). The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface.	
3	UP	Unicast Pause Frame Detect A pause frame is processed when it has the unique multicast address specified in the IEEE Std 802.3. When this bit is set, the MAC can also detect Pause frames with unicast address of the station. This unicast address should be as specified in the MAC Address0 High Register and MAC Address0 Low Register. When this bit is reset, the MAC only detects Pause frames with unique multicast address. **Note:** The MAC does not process a Pause frame if the multicast address of received frame is different from the unique multicast address.	RW
2	RFE	Receive Flow Control Enable When this bit is set, the MAC decodes the received Pause frame and disables its transmitter for a specified (Pause) time. When this bit is reset, the decode function of the Pause frame is disabled.	RW
1	TFE	Transmit Flow Control Enable In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to transmit Pause frames. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause frames. In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled.	RW
0	FCB_BPA	Flow Control Busy or Backpressure Activate This bit initiates a Pause frame in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. In the full-duplex mode, this bit should be read as 1'b0 before writing to the Flow Control register. To initiate a Pause frame, the Application must set this bit to 1'b1. During a transfer of the Control Frame, this bit continues to be set to signify that a frame transmission is in progress. After the completion of Pause frame transmission, the MAC resets this bit to 1'b0. The Flow Control register should not be written to until this bit is cleared.	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		In the half-duplex mode, when this bit is set (and TFE is set), then backpressure is asserted by the MAC. During backpressure, when the MAC receives a new frame, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled.	

Note:

Only support RMII mode

34.7.2.19 MAC VLAN Tag Register(MAC_VTR,0x001C)

	MAC_VTR																Base + 0x001C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												VTHM	ESVL	VTIM	ETV	VL															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:20	Reserved	Writing has no effect, read as zero.	R
19	VTHM	VLAN Tag Hash Table Match Enable When set, the most significant four bits of the VLAN tag's CRC are used to index the content of Register 354 (VLAN Hash Table Register). A value of 1 in the VLAN Hash Table register, corresponding to the index, indicates that the frame matched the VLAN hash table. When Bit 16 (ETV) is set, the CRC of the 12-bit VLAN Identifier (VID) is used for comparison whereas when ETV is reset, the CRC of the 16-bit VLAN tag is used for comparison. When reset, the VLAN Hash Match operation is not performed.	RW
18	ESVL	nable S-VLAN When this bit is set, the MAC transmitter and receiver also consider the S-VLAN (Type = 0x88A8) frames as valid VLAN tagged frames.	RW
17	VTIM	VLAN Tag Inverse Match Enable When set, this bit enables the VLAN Tag inverse matching. The frames that do not have matching VLAN Tag are marked as matched.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		When reset, this bit enables the VLAN Tag perfect matching. The frames with matched VLAN Tag are marked as matched.	
16	ETV	Enable 12-Bit VLAN Tag Comparison When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding Bits in the received VLAN-tagged frame. Similarly, when enabled, only 12 bits of the VLAN tag in the received frame are used for hash-based VLAN filtering. When this bit is reset, all 16 bits of the 15th and 16th bytes of the received VLAN frame are used for comparison and VLAN hash filtering.	RW
15:0	VL	VLAN Tag Identifier for Receive Frames This Bits contains the 802.1Q VLAN tag to identify the VLAN frames and is compared to the 15th and 16th bytes of the frames being received for VLAN frames. The following list describes the bits of this Bits: Bits [15:13]: User Priority Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) Bits[11:0]: VLAN tag's VLAN Identifier (VID) Bits When the ETV bit is set, only the VID (Bits[11:0]) is used for comparison. If VL (VL[11:0] if ETV is set) is all zeros, the MAC does not check the fifteenth and 16th bytes for VLAN tag comparison, and declares all frames with a Type Bits value of 0x8100 or 0x88a8 as VLAN frames.	RW

Note:Only support RMII mode

34.7.2.20 MAC Debug Register(MAC_DR,0x0024)

	MAC_DR																														Base + 0x0024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							TXFSTS	Reserved	TWCST	TRCSTS		TXPAUSED	TFCSTS		TPESTS	Reserved						RXFSTS		Reserved	RPCSTS		RWCSTS	Reserved	RFCFCSTS	RPESTS	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:25	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

24	TXFSTS	MTL Tx FIFO Not Empty Status When high, this bit indicates that the MTL Tx FIFO is not empty and some data is left for transmission.	R
23	Reserved	Writing has no effect, read as zero.	R
22	TWCSTS	MTL Tx FIFO Write Controller Status When high, this bit indicates that the MTL Tx FIFO Write Controller is active and is transferring data to the Tx FIFO.	R
21:20	TRCSTS	MTL Tx FIFO Read Controller Status This Bits indicates the state of the Tx FIFO Read Controller: ▪ 00: IDLE state ▪ 01: READ state (transferring data to the MAC transmitter) ▪ 10: Waiting for Tx Status from the MAC transmitter ▪ 11: Writing the received Tx Status or flushing the Tx FIFO	R
19	TXPAUSED	MAC Transmitter in Pause When high, this bit indicates that the MAC transmitter is in the Pause condition (in the full-duplex-only mode) and hence does not schedule any frame for transmission.	R
18:17	TFCSTS	MAC Transmit Frame Controller Status This Bits indicates the state of the MAC Transmit Frame Controller module: 00: IDLE state 01: Waiting for status of previous frame or IFG or backoff period to be over 10: Generating and transmitting a Pause frame (in the full-duplex mode) 11: Transferring input frame for transmission	R
16	TPESTS	MAC GMII or MII Transmit Protocol Engine Status When high, this bit indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data and is not in the IDLE state.	R
15:10	Reserved	Writing has no effect, read as zero.	R
9:8	RXFSTS	MTL Rx FIFO Fill-Level Status This Bits gives the status of the fill-level of the Rx FIFO: ▪ 00: Rx FIFO Empty ▪ 01: Rx FIFO fill-level below flow-control deactivate threshold ▪ 10: Rx FIFO fill-level above flow-control activate threshold ▪ 11: Rx FIFO Full	R
7	Reserved	Writing has no effect, read as zero.	R
6:5	RRCSTS	MTL Rx FIFO Read Controller State This Bits gives the state of the Rx FIFO read Controller: ▪ 00: IDLE state ▪ 01: Reading frame data ▪ 10: Reading frame status	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		▪ 11: Flushing the frame data and status	
4	RWCSTS	MTL Rx FIFO Write Controller Active Status When high, this bit indicates that the MTL Rx FIFO Write Controller is active and is transferring a received frame to the FIFO.	R
3	Reserved	Writing has no effect, read as zero.	R
2:1	RFCFCSTS	MAC Receive Frame FIFO Controller Status When high, this Bits indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Frame Controller Module.	R
0	RPESTS	MAC GMII or MII Receive Protocol Engine Status When high, this bit indicates that the MAC GMII or MII receive protocol engine is actively receiving data and not in IDLE state.	R

Note:

Only support RMII mode

34.7.2.21 LPI Control and Status Register(LPI_CSR,0x0030)

	LPI_CSR																															Base + 0x0030
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												LPITXA	PLSEN	PLS	LPIEN	Reserved						RLPIST	TLPIST	Reserved				RLPIES	RLPIEN	TLPIES	TLPIEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:20	Reserved	Writing has no effect, read as zero.	R
19	LPITXA	LPI TX Automate This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the transmit side. If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding frames (in the core) and pending frames (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any frame for transmission or the application issues a TX FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If TX FIFO Flush is set in Bit 20 of Register 6 (Operation Mode Register), when the MAC is in the LPI mode, the MAC exits the LPI mode. When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

18	PLSEN	PHY Link Status Enable This bit enables the link status received on the RGMII receive paths to be used for activating the LPILS TIMER. When set, the MAC uses the link-status bits of Register 54 (RGMII Control and Status Register) and Bit 17 (PLS) for the LPI LS Timer trigger. When cleared, the MAC ignores the link-status bits of Register 54 and takes only the PLS bit.	RW
17	PLS	PHY Link Status This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (okay) at least for the time indicated by the LPI LS TIMER. When set, the link is considered to be okay (up) and when reset, the link is considered to be down.	RW
16	LPIEN	LPI Enable When set, this bit instructs the MAC Transmitter to enter the LPI state. When reset, this bit instructs the MAC to exit the LPI state and resume normal transmission. This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission.	RW[1]
15:10	Reserved	Writing has no effect, read as zero.	R
9	RLPIST	Receive LPI State When set, this bit indicates that the MAC is receiving the LPI pattern on the GMII or MII interface.	R
8	TLPIST	Transmit LPI State When set, this bit indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface.	R
7:4	Reserved	Writing has no effect, read as zero.	R
3	RLPIEX	Receive LPI Exit When set, this bit indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register. **Note:** This bit may not get set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than 3 clock cycles of HCLK clock.	R[2]
2	RLPIEN	Receive LPI Entry When set, this bit indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this register. **Note:** This bit may not get set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than 3 clock cycles of HCLK clock.	R[3]

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	TLPIEX	Transmit LPI Exit When set, this bit indicates that the MAC transmitter has exited the LPI state after the user has cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register.	R[4]
0	TLPIEN	Transmit LPI Entry When set, this bit indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register.	R[5]

Note:

1. Only support RMII mode
2. [1]:This bits will operate with Self clear function.
3. [2]~[5]: This bits will operate with Self set , read clear function.

34.7.2.22 LPI Timers Control Register(LPI_TCR,0x0034)

	LPI_TCR																															Base + 0x0034
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						LST										TWT															
RST	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:26	Reserved	Writing has no effect, read as zero.	R
25:16	LST	LPI LS TIMER This Bits specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard.	RW
15:0	TWT	LPI TW TIMER This Bits specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer.	RW

Note:

Only support RMII mode

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

34.7.2.23 MAC Interrupt Status Register(MAC_ISR,0x0038)

	MAC_ISR																															
																	Base + 0x0038															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				GPIIS	LPIIS	Reserved		MMCRXIPIS	MMCTXIS	MMCRXIS	MMCIS	PMTIS	Reserved		RGMII
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:12	Reserved	Writing has no effect, read as zero.	R
11	GPIIS	GPI Interrupt Status When the GPIO feature is enabled, this bit is set when any active event (LL or LH) occurs on the GPIS Bits (Bits [3:0]) of Register 56 (General Purpose IO Register) and the corresponding GPIE bit is enabled. This bit is cleared on reading lane 0 (GPIS) of Register 56 (General Purpose IO Register). When the GPIO feature is not enabled, this bit is reserved.	R
10	LPIIS	LPI Interrupt Status When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared on reading Bit 0 of Register 12 (LPI Control and Status Register). In all other modes, this bit is reserved.	R
9:8	Reserved	Writing has no effect, read as zero.	R
7	MMCRXIPIS	MMC Receive Checksum Offload Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared.	R
6	MMCTXIS	MMC Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared.	R
5	MMCRXIS	MMC Receive Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared.	R
4	MMCIS	MMC Interrupt Status This bit is set high when any of the Bits [7:5] is set high and	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		cleared only when all of these bits are low.	
3	PMTIS	PMT Interrupt Status This bit is set when a magic packet or remote wake-up frame is received in the power-down mode (see Bits 5 and 6 in the PMT Control and Status Register). This bit is cleared when both Bits[6:5] are cleared because of a read operation to the PMT Control and Status register.	R
2:1	Reserved	Writing has no effect, read as zero.	R
0	RGMII	RGMII Interrupt Status This bit is set because of any change in value of the Link Status of RGMII interface.	R

Note:

Only support RMII mode

34.7.2.24 MAC Interrupt Mask Register(MAC_IMR,0x003C)

	MAC_IMR																														
	Base + 0x003C																														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																					LPIIM	Reserved						PMTIM	PCSANCIM	PCSLCHGIM	RGMII
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:11	Reserved	Writing has no effect, read as zero.	R
10	LPIIM	LPI Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of the LPI Interrupt Status bit in Register 14 (Interrupt Status Register).	RW
9:4	Reserved	Writing has no effect, read as zero.	R
3	PMTIM	PMT Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of PMT Interrupt Status bit in Register 14 (Interrupt Status Register).	RW
2	PCSANCIM	PCS AN Completion Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of PCS Auto-negotiation complete bit in Register 14 (Interrupt Status Register).	RW
1	PCSLCHGIM	PCS Link Status Interrupt Mask When set, this bit disables the assertion of the interrupt signal	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		because of the setting of the PCS Link-status changed bit in Register 14 (Interrupt Status Register).	
0	RGMII	RGMII Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of the RGMII Interrupt Status bit in Register 14 (Interrupt Status Register).	RW

34.7.2.25 MAC Address0 High Register(MAC_A0HR,0x0040)

	MAC_A0HR																Base + 0x0040															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AE	Reserved															ADDRHI															
RST	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
31	AE	Address Enable This bit is always set to 1.	R
30:16	Reserved	Writing has no effect, read as zero.	R
15:0	ADDRHI	MAC Address0 [47:32] This Bits contains the upper 16 bits (47:32) of the first 6-byte MAC address. The MAC uses this Bits for filtering the received frames and inserting the MAC address in the Transmit Flow Control (Pause) Frames.	RW

Note:

Only support RMII mode

34.7.2.26 MAC Address0 LOW Register(MAC_A0LR,0x0044)

	MAC_A0LR																Base + 0x0044															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADDRLO																															
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
31:0	ADDRLO	MAC Address0 [31:0] This Bits contains the lower 32 bits of the first 6-byte MAC address.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		This is used by the MAC for filtering the received frames and inserting the MAC address in the Transmit Flow Control (Pause) Frames.	

Note:

Only support RMII mode

34.7.2.27 MAC Address1 High Register(MAC_A1HR,0x0048)

	MAC_A1HR																														Base + 0x0048
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AE	SA	MBC						Reserved								ADDRHI															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
31	AE	Address Enable When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering.	RW
30	SA	Source Address When this bit is set, the MAC Address1[47:0] is used to compare with the SA bits of the received frame. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA Bits of the received frame.	RW
29:24	MBC	Mask Byte Control These bits are mask control bits for comparison of each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: Bit 29: Register 18[15:8] Bit 28: Register 18[7:0] Bit 27: Register 19[31:24] ... Bit 24: Register 19[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.	RW
23:16	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

15:0	ADDRHI	MAC Address1 [47:32] This Bits contains the upper 16 bits (47:32) of the second 6-byte MAC address.	RW

Note:

Only support RMII mode

34.7.2.28 MAC Address1 LOW Register(MAC_A1LR,0x004C)

	MAC_A1LR																Base + 0x004C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADDRLO																															
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
31:0	ADDRLO	MAC Address1 [31:0] This Bits contains the lower 32 bits of the second 6-byte MAC address. The content of this Bits is undefined until loaded by the Application after the initialization process.	RW

Note: Only support RMII mode

34.7.2.29 MAC Watchdog Timeout Register(MAC_WTR,0x00DC)

	MAC_WTR																Base + 0x00DC															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															PWE	Reserved		WTO													
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:17	Reserved	Writing has no effect, read as zero.	R
16	PWE	Programmable Watchdog Enable When this bit is set and Bit 23 (WD) of Register 0 (MAC Configuration Register) is reset, the WTO Bits (Bits[13:0]) is used as watchdog timeout for a received frame.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		When this bit is cleared, the watchdog timeout for a received frame is controlled by the setting of Bit 23 (WD) and Bit 20 (JE) in Register 0 (MAC Configuration Register).	
15:14	Reserved	Writing has no effect, read as zero.	R
13:0	WTO	Watchdog Timeout When Bit 16 (PWE) is set and Bit 23 (WD) of Register 0 (MAC Configuration Register) is reset, this Bits is used as watchdog timeout for a received frame. If the length of a received frame exceeds the value of this Bits, such frame is terminated and declared as an error frame. **Note:** When Bit 16 (PWE) is set, the value in this Bits should be more than 1,522 (0x05F2). Otherwise, the IEEE Std 802.3-specified valid tagged frames are declared as error frames and are dropped.	RW

Note:

Only support RMII mode

34.7.2.30 MAC Timestamp Control Register (MAC_TCR, 0x0700)

	MAC_TCT																Base + 0x0700													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				ATSEN3	ATSEN2	ATSEN1	ATSEN0	ATSFC						TSENMACADDR	SNAPTYPSEL		TSMSTRENA	TSEVNTENA	TSIPV4ENA	TSIPV6ENA	TSIPENA	TSVER2ENA	TSCTRLSSR	TSENALL			TSADDREG	TSTRIG	TSUPDT	TSINIT	TSCFUPDT	TSENA
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:29		Reserved	
28	ATSEN3	Auxiliary Snapshot 3 Enable This Field controls capturing the Auxiliary Snapshot Trigger 3. When this bit is set, the Auxiliary snapshot of event on ptp_aux_trig_i[3] input is enable	RW
27	ATSEN2	Auxiliary Snapshot 2 Enable This Field controls capturing the Auxiliary Snapshot Trigger 3. When this bit is set, the Auxiliary snapshot of event on ptp_aux_trig_i[2] input is enable	RW
26	ATSEN1	Auxiliary Snapshot 1 Enable This Field controls capturing the Auxiliary Snapshot Trigger 3. When this bit is set, the Auxiliary snapshot of event on ptp_aux_trig_i[1] input is enable	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

25	ATSEN0	Auxiliary Snapshot 0 Enable This Field controls capturing the Auxiliary Snapshot Trigger 3. When this bit is set, the Auxiliary snapshot of event on ptp_aux_trig_i[0] input is enable	RW
24	ATSFV	Auxiliary Snapshot FIFO Clear When set, it resets the pointer of Auxiliary Snapshot FIFO	RWS_SC
23:19			
18	TSEBNACADDR	Enable MAC address for PTP Frame Filtering When set the DA MAC address is used to filter the PTP frames when PTP is directly sent over Ethernet	RW
17:16	SNAPTYPSEL	Select PTP packets for Taking Snapshots	RW
15	TSMSTRENA	Enable Snapshot for Messages Relevant to Master When set, the snapshot is taken only for the messages relevant the master node.	RW
14	TSEVENTENA	Enable Timestamp Snapshot for Event Messages When set, the timestamp snapshot is taken only for event messages.	RW
13	TSIPV4ENAV	Enable Processing of PTP Frames Send over IPV4-UDP When set, the MAC receiver processes PTP packets encapsulated in UDP over IPv4 packets	RW
12	TSIPV6ENAV	Enable Processing of PTP Frames Send over IPV6-UDP When set, the MAC receiver processes PTP packets encapsulated in UDP over IPv6 packets	RW
11	TSIPENA	Enable Processing of PTP over Ethernet Frames When set, the MAC receiver processes the PTP packets encapsulated directly in the Ethernet frames.	RW
10	TSVER2ENA	Enable PTP packet Processing for Version 2 Format When set, the PTP packets are processed using the 1588 version 2 format	RW
9	TSCTRLSSR	Timestamp Digital or Binary Rollover Control When set, the Timestamp Low register rolls over after 0x3B9A_C9FF value	RW
8	TSENALL	Enable Timestamp for All Frames When set, the timestamp snapshot is enabled for all frames received by the MAC	RW
7:6		Reserved	
5	TSADDREG	Addend Reg Update When set, the content of the Timestamp Addend register is updated in the PTP block for fine correction.	RWS_SC
4	TSTRIG	Timestamp Interrupt Trigger Enable When set, the timestamp interrupt is generated when the system	RW_S_SC

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		Time becomes greater than the value written in the Target Time register. The bit is reset after the generation of the Timestamp Trigger Interrupt	
3	TSUPDT	Timestamp Update The bit should be read zero before updating it. The bit is reset when the update is completed in hardware	RW_S_SC
2	TSINIT	Timestamp initialize The bit should be read zero before updating it. This bit is reset when the initialization is complete	RW_S_SC
1	TSCFUPDT	Timestamp Fine or Coarse Update When set, this bit indicates that the system times update should be done using the fine update method. When reset, it indicates the system timestamp update should be done using the coarse method	RW
0	TSENA	Timestamp Enable When set, the timestamp is added for the transmit and receive frames. When disabled, timestamp is not added for the transmit and receive frames and the Timestamp Generator is also suspend. You need to initialize the Timestamp after enabling this mode. On the receive side, the Mac process the 1588 frames only if this bit is set	RW

34.7.2.31 MAC Sub-Second Increment Register (MAC_SSIR,0x0704)

	MAC_SSIR																													Base + 0x0704
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																									SSINC							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:8		Reserved	
7:0	SSINC	Sub-second Increment Value The value programmed in this filed is accumulated every clock cycle	RW

34.7.2.32 MAC System Time - Second Register (MAC_STSR, 0x0708)

	MAC_SSIR																													Base + 0x0708
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	TSS
RST	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Name	Description	R/W
31:0	TSS	Timestamp Second The value in this field indicates the current value in seconds of the system Time maintained by the MAC	R

34.7.2.33 MAC System Time - Nanosecond Register (MAC_STNR, 0x070C)

	MAC_STNR																Base + 0x070C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		TSSS																														
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	TSSS	Timestamp Sub Second The value in this field has the sub second representation of time, with an accuracy of 0.46ns	R

34.7.2.34 MAC System Time – Second Update Register (MAC_STSUR, 0x0710)

	MAC_STSUR																Base + 0x0710													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSS																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	TSS	Timestamp Second The value in this field indicates the time in seconds to be initialized or added to the system time	RW

34.7.2.35 MAC System Time – Nanosecond Update Register (MAC_STNUR, 0x0714)

	MAC_STNUR																Base + 0x0714													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

	ADDSUB	TSSSS																													
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	ADDSUB	Add or Subtract Time When this bit is set, the time value is subtracted with the contents of the update register	RW
30:0	TSSS	Timestamp Sub Second The value in this field has the sub second representation of time	RW

34.7.2.36 MAC Timestamp Addend Register (MAC_TAR, 0x0718)

	MAC_STNUR																														Base + 0x0718
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSAR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	TSAR	Timestamp Addend Register The field indicates the 32-bits time value to be added to the Accumulator register to achieve time synchronization.	RW

34.7.2.37 MAC Target Time Seconds Register (MAC_TTSR, 0x071C)

	MAC_TTSR																														Base + 0x071C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSTR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	TSTR	Target Time Seconds Register This register stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp register	RW

34.7.2.38 MAC Target Time Nanoseconds Register (MAC_TTNR, 0x0720)

	MAC_TTNR	Base + 0x0720

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRGTBUSY	TTSLO																														
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	TRGTBUSY	Target Time Register Busy	R_W S_SC
30:0	TTSLO	Target Timestamp Low Register This register stores the time in nanoseconds. When the value of the timestamp matches the both Target Timestamp, then based on the TRGTMODSEL0.	RW

34.7.2.39 MAC System Time – Higher Word Seconds Register (MAC_STHWSR, 0x0724)

	MAC_STHWSR																														Base + 0x0724	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																	TSHWR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:16		reserved	
15:0	TTSLO	Timestamp Higher Word Register This field contains the most significant 16-bits of the timestamp seconds value	RW_ SU

34.7.2.40 MAC Timestamp Status Register (MAC_TSR, 0x0728)

	MAC_TSR																														Base + 0x0728	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		ATSNS						ATSSTM					ATSSTN										TSTRGTEER3	TSTARGT3	TSTRGTEER2	TSTARGT2	TSTRGTEER1	TSTARGT1	TSTRGTEER	AUXTSTRIG	TSTART	TSSOVF
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	*Description*	R/W

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

31:30		Reserved	
29:25	ATSNS	Number of Auxiliary Timestamp Snapshots The field indicates the number of Snapshot available in the FIFO. A value equal to the selected depth of FIFO indicates that the Auxiliary Snapshot FIFO is full	R
24	ATSSTM	Auxiliary Timestamp Snapshot Trigger Missed This bit is set when the Auxiliary timestamp snapshot FIFO is full and external trigger was set. This indicates that the latest snapshot is not stored in the FIFO.	R
23:20		Reserved	
19:16	ATSSTN	Auxiliary Timestamp Snapshot Trigger Identifier These bits identify the Auxiliary trigger input s for which the timestamp available in the Auxiliary Snapshot Register is applicable. Bit 16: Auxiliary trigger 0 Bit 17: Auxiliary trigger 1 Bit 18: Auxiliary trigger 2 Bit 19: Auxiliary trigger 3	R_SS_RC
15:10		Reserved	
9	TSTRGTERR3	Timestamp Target Time Error	R_SS_RC
8	TSTARGT3	Timestamp Target Time Reached for Target Time PPS3	R_SS_RC
7	TSTRGTERR2	Timestamp Target Time Error	R_SS_RC
6	TSTARGT2	Timestamp Target Time Reached for Target Time PPS2	R_SS_RC
5	TSTRGTERR1	Timestamp Target Time Error	R_SS_RC
4	TSTARGT1	Timestamp Target Time Reached for Target Time PPS1	R_SS_RC
3	TSTRGTERR	Timestamp Target Time Error	R_SS_RC
2	AUTSTRIG	Auxiliary Timestamp Trigger Snapshot This bit is set high when the auxiliary snapshot is written to the FIFO.	R_SS_RC
1	TSTARGT	Timestamp Target Time Reached When set, this bit indicates that the value of system time is greater than or equal to the value specified in Target Time Seconds Register and Target Time Nanoseconds Register.	R_SS_RC
0	TSSOVF	Timestamp Seconds Overflow When set, this bit indicates that the seconds value of the	R_SS_RC

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		timestamp has overflowed beyond 32'hFFFFFFFF.	

34.7.2.41 MAC PPS Control Register (MAC_PPSCR, 0x072C)

	MAC_PPSCR																Base + 0x072C															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		TRGTMODSEL3				PPSCMD3				TRGTMODSEL2				PPSCMD1				TRGTMODSEL1				PPSCMD1				TRGTMODSEL0		PPSEN0	PPSCTRL0_CMD0			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	*Description*	R/W
31		Reserved	
30:29	TRGTMODSEL3	Target Time Register Mode for PPS3 Output	RW
28:27		Reserved	
26:24	PPSCMD3	Flexible PPS3 Output Control	R_WS_SC
23		Reserved	
22:21	TRGTMODSEL2	Target Time Register Mode for PPS2 Output	RW
20:19		Reserved	
18:16	PPSCMD2	Flexible PPS2 Output Control	R_WS_SC
15		Reserved	
14:13	TRGTMODSEL1	Target Time Register Mode for PPS1 Output	RW
12:11		Reserved	
10:8	PPSCMD1	Flexible PPS1 Output Control	R_WS_SC
7		Reserved	
6:5	TRGTMODSEL0	Target Time Register Mode for PPS0 Output 00: indicates that the Target Time register are programmed only for generating the interrupt event 01: Reserved 10: indicates that the Target Time register are programmed for generating the interrupt event and starting or stopping the generation if the PPS0 output single. 11: indicates that the Target Time register are programmed only for	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		starting or stopping the generation of the PPS0 output signal. No interrupt is asserted	
4	PPSEN0	Flexible PPS Output Mode Enable When set low, Bits[3:0] function as PPSCTRL When set high, Bits[3:0] function as PPSCMD	RW
3:0	PPSCTRL0 PPSCMD0	PPS Output Frequency Control This field controls the frequency of the PPS0 output signal. 0001: The binary rollover is 2Hz, the digital rollover is 1Hz 0010: The binary rollover is 4Hz, the digital rollover is 2Hz 0011: The binary rollover is 8Hz, the digital rollover is 4Hz 0100: The binary rollover is 16Hz, the digital rollover is 32Hz 1111: The binary rollover is 32.768Hz, the digital rollover is 16.384Hz Flexible PPS0 Output Control 0000: No command 0001: Start Single Pulse 0010: Start Pulse Train 0011:Cancel START 0100:STOP Pulse train at time 0101:STOP Pulse Train immediately 0110: Cancel Stop Pulse Train 0111-1111: reserved	RW

34.7.2.42 MAC Auxiliary Timestamp - Nanoseconds Register (MAC_ATNR, 0x0730)

	MAC_ATNR																Base + 0x0730													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		AUXTSLO																														
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31		reserved	
30:0	AUXTSLO	Contains the lower 31 bits nanoseconds field of the auxiliary timestamp	R

34.7.2.43 MAC Auxiliary Timestamp - Seconds Register (MAC_ATSR, 0x0734)

	MAC_ATSR																Base + 0x0734													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	AUXTSHI
RST	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bits	Name	Description	R/W
31:0	AUXTSHI	Contains the lower 31 bits seconds field of the auxiliary timestamp	R

34.7.2.44 MAC AV Control Register (MAC_AVCR, 0x0738)

	MAC_ATSR																Base + 0x0738															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							PTPCH			AVCH		AVCD	VQE	AVP			AVT															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	*Description*	R/W
31:26		Reserved	
25:24	PTPCH	Channel for Queuing the PTP Packets The field specifies the channel on which the untagged PTP packet, sent over the Ethernet payload and not over IPV4 or IPV6, are queued 00: Channel 0 01: Channel 1 10: Channel 2 11: Reserved	RW
23		Reserved	
22:21	AVCH	Channel for Queuing the AV Control Packets The field specifies the channel on which the received untagged AV control packet, are queued 00: Channel 0 01: Channel 1 10: Channel 2 11: Reserved	RW
20	AVCD	AV Channel Disable	RW
19	VQE	VLAN Tagged Non-AV Packets Queuing Enable	RW
18:16	AVP	AV Priority for Queuing	RW
15:0	AVT	AV Ether Type Value	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

34.7.2.45 MAC PPS0 Interval Register (MAC_PPS0IR 0x0760)

	MAC_PPS0IR																															Base + 0x0760
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PPSINT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	PPSINT	PPS0 Output Signal Interval These bits store the interval between the rising edges of PPS0 signal output in terms of units of sub-second increment value	RW

34.7.2.46 MAC PPS1 Target Time Second Register (MAC_PPS1TTSR 0x0780)

	MAC_PPS1SSTR																															xBase + 0x0780
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSTRH																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31:0	TSTRTH1	PPS1 Target Time Seconds Register This register stores the time in seconds.	RW

34.7.2.47 MAC PPS1 Target Time Nanoseconds Register (MAC_PPS1TTNR 0x0784)

	MAC_PPS1SSNR																															Base + 0x0784
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRGTBUSY1	TTSL1																														
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
31	TRGTBUSY1	PPS1 Target Time Register Busy The MAC sets this bits when the PPSCMD1 filed is programmed to	R_WS_SS

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		010 or 011	
30:0	TTSL1	Target Time Low for PPS1 Register This register stores the time in nanoseconds.	RW

34.8 Operation Flow

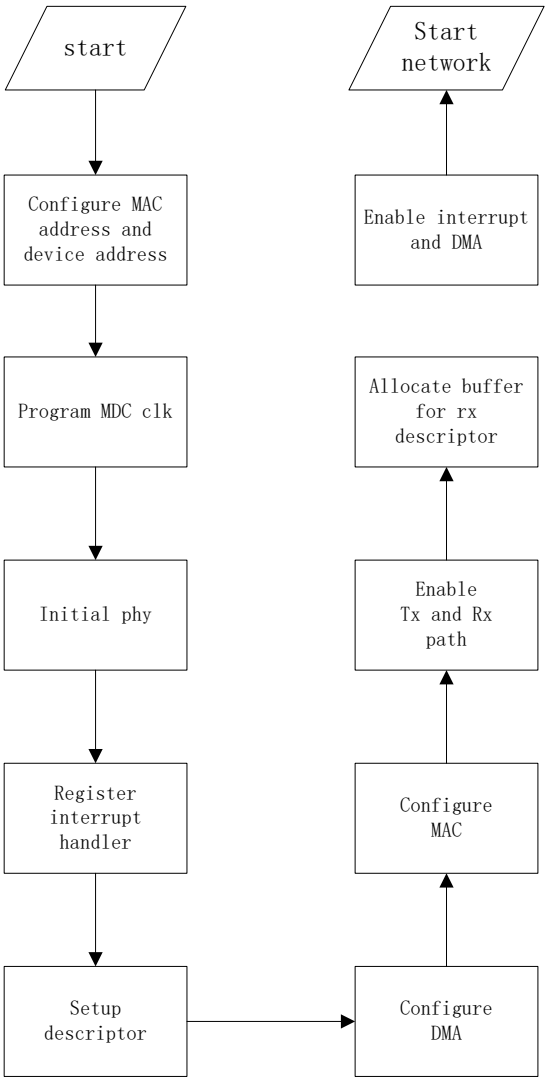


Figure 34-2 GMAC configure flow

Note: Only support RMII mode

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

35 AES

35.1 Overview

- Advanced Encryption Standard
- Fully referring to *Rijdael_fips_197* standard
- AES Engine: AES-128/192/256
- 128/192/256 bits key for AES Encryption and Decryption supported
- ECB and CBC mode supported
- Internal DMA mode supported
- Clear bit supported to clear keys, data and IV for security concern

35.2 AES engine

- 128 bits data for Encryption and Decryption
- 128/192/256 bits Key
- 128 bits IV (initial vector) for CBC mode
- ECB and CBC mode

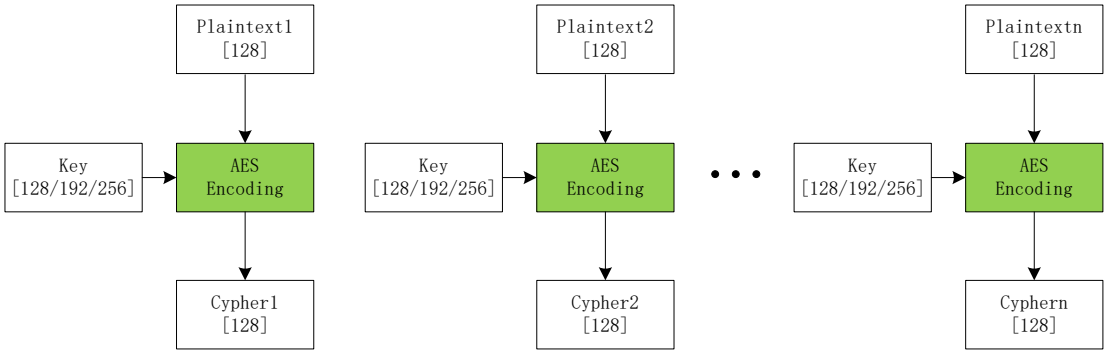


Figure 35-1 ECB mode encoding

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

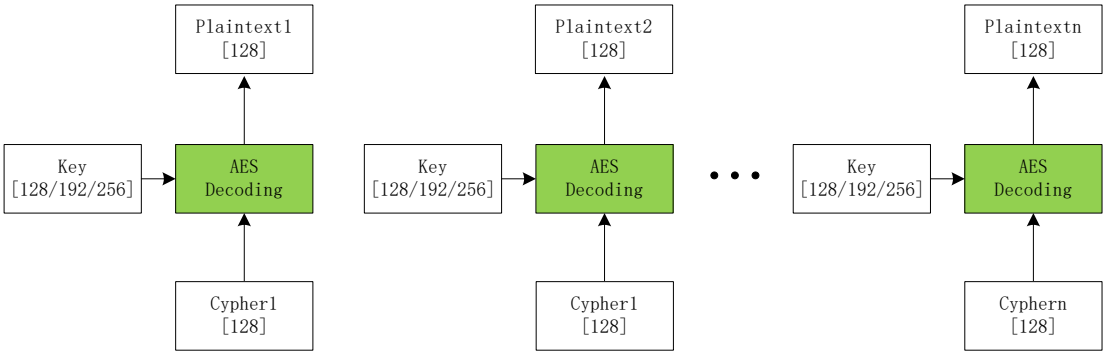


Figure 35-2 ECB mode decoding

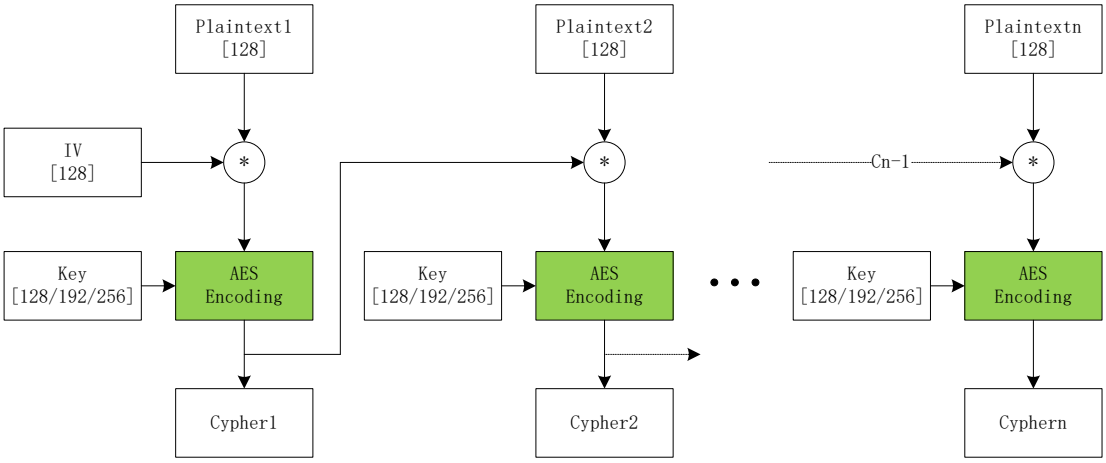


Figure 35-3 CBC mode encoding

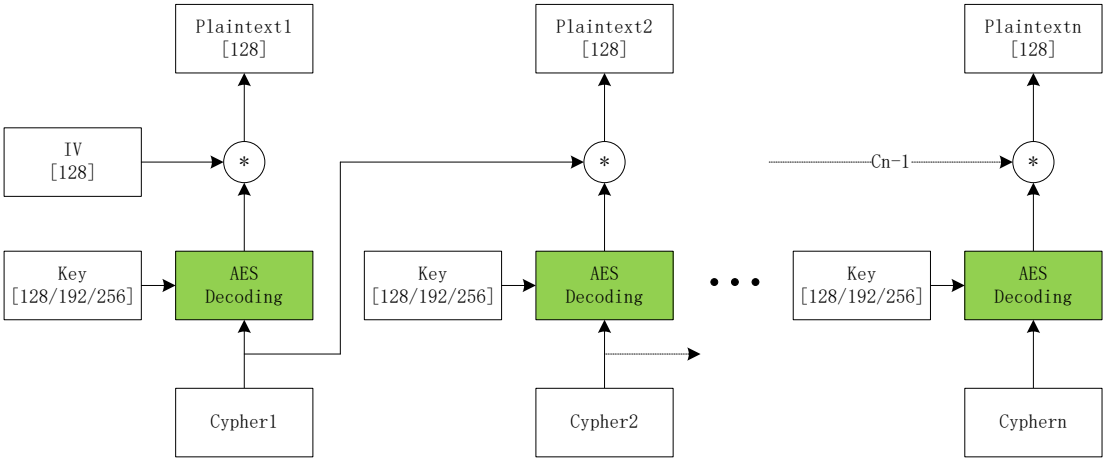


Figure 35-4 CBC mode decoding

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

35.3 Registers

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clears to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - Reset to 1
   0 - reset to 0
   ? - Value unknown after reset

35.3.1 Register Memory Map

Table 35-1 Registers Memory Map-Address Base

Name	Base	Description
AES	0x13430000	AES registers memory map address

Table 35-2 AES registers description

Name	Description	Reset Value	Address offset	Access Size
ASCR	AES control register	0x00000000	0x0000	32
ASSR	AES status register	0x00000000	0x0004	32
ASINTM	AES interrupt mask register	0x00000000	0x0008	32
ASSA	AES DMA source address	0x00000000	0x000c	32
ASDA	AES DMA destine address	0x00000000	0x0010	32
ASTC	AES DMA transfer count	0x00000000	0x0014	32
ASDI	AES data input	0x00000000	0x0018	32
ASDO	AES data output	0x00000000	0x001c	32
ASKY	AES key input	0x00000000	0x0020	32
ASIV	AES IV input	0x00000000	0x0024	32

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

35.3.2 AES Control Register (ASCR)

	ASCR																BASE+0x0000											
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PS				RESERVED																ENDIAN	CLR	DMAS	DMAE	KEYL		MODE	DECE	AESS	KEYS	INIT_IV	EN
RST	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	PS	Page Size, don't set these bits, and keep them default value. 0: don't care 1: 1 KB 2: 2 KB 3: 4 KB(default) 4: 8 KB 5: 16 KB	RW
27:12	Reserved	Writes to these bits have no effect and always read as 0.	R
11	ENDIAN	0: little-endian data input 1: big-endian data input	RW
10	CLR	Clear the IV & KEYs: This bit MUST be set by two reasons : (1)After CBC mode decoding; (2)Clear IV/KEYs/Input Data/Output Data for security concern ;	RWS
9	DMAS	DMA Start	RWS
8	DMAE	DMA Enable	RW
7:6	KEYL	Selects the key size mode according to the following list: • 2'b00 value selects 128 bit key length, • 2'b01 value selects 192 bit key length, • 2'b10 value selects 256 bit key length This value should not change during operation of the core unless the key mode is changed and key expansion is restarted.	RW
5	MODE	AES mode select bit 0: ECB mode selected 1: CBC mode selected	RW
4	DECE	AES encrypts/decrypts select bit 0: Encrypts input data 1: Decrypts input data	RW
3	AESS	AES Start ONLY valid when DMAE==0, Means a round of AES process start. After ASIV and ASDI write, set AESS by software.	RWS
2	KEYS	Key Expansion Start: Key expansion start command.	RWS
1	INIT_IV	AES IV Initial	RWS

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		After a new ASIV be written, INIT MUST be set by software to indicate a new round of CBC mode process will be start.	
0	EN	AES enable 0: Disable AES 1: Enable AES	WR

35.3.3 AES Status Register (ASSR)

	ASSR																BASE+0x0004															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													DMAD	AESD	KEYD
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Security

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
2	DMAD	**1: DMA mode encryption/decryption done** **0: DMA mode encryption/decryption not done** Set 1 to clear after reading this bit, writing 0 has no effect	RWC
1	AESD	**1: CPU mode encryption/decryption Done** **0: CPU mode encryption/decryption not done** Set 1 to clear after reading this bit, writing 0 has no effect	RWC
0	KEYD	**1: Key Expansion done** **0: Key Expansion not done** Set 1 to clear after reading this bit, writing 0 has no effect	RWC

35.3.4 AES Interrupt Mask Register (ASINTM)

	ASINTM																BASE+0x0008															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																													DMA_INT_M	AES_INT_M	KEY_INT_M
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:3	Reserved	Writing has no effect, read as zero.	R
2	DMA_INT_M	**DMA Done Interrupt Mask** 1: Interrupt Enable 0: Interrupt Mask(default)	WR

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	AES_INT_M	**AES Done Interrupt Mask** 1: Interrupt Enable 0: Interrupt Mask(default)	WR
0	KEY_INT_M	**KEY Expansion Done Interrupt Mask** 1: Interrupt Enable 0: Interrupt Mask(default)	WR

35.3.5 AES DMA Source Address (ASSA)

	ASSA																BASE+0x000c															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	SA	**Source physical address for DMA mode**	WR

35.3.6 AES DMA Destination Address (ASDA)

	ASDA																BASE+0x0010															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DA	**Destination Physical Address for DMA mode**	WR

35.3.7 AES Transfer Count (ASTC)

	ASTC																BASE+0x0014															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TC																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	TC	**Transfer Count:** Number of Blocks(**1Block == 128bit**)	WR

35.3.8 AES Data Input Register (ASDI)

	ASDI																BASE+0x0018														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIN																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DIN	**Data Input:** Only support Word write The minimum data unit of AES algorithms is 128-bit. Software should ensure that the number of data to process is **n*128** (bit). The write data flow is {DIN_1st, DIN_2ed, DIN_3rd, DIN_4th}; ASDI can ONLY be acceded by word-write.	W

35.3.9 AES Data Output Register (ASDO)

	ASDO																BASE+0x001C														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DOUT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DOUT	**Data Output FIFO** The minimum data unit of AES algorithms is 128-bit. Software should ensure that the number of data to process is **n*128** (bit). The read data flow is { DOUT_1st, DOUT_2ed, DOUT_3rd , DOUT_4th}; DOUT can **ONLY** be acceded by word-read, writing has no effect.	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

35.3.10 AES KEY FIFO (ASKY)

	ASKY																BASE+0x0020															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ASKY																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	ASKY	AES Key register The key(AES128) data flow is { KEY_1st, KEY_2ed, KEY_3rd , KEY_4th }; The key(AES192) data flow is { KEY_1st, KEY_2ed, KEY_3rd , KEY_4th, KEY_5th, KEY_6th }; The key(AES256) data flow is { KEY_1st, KEY_2ed, KEY_3rd , KEY_4th, KEY_5th, KEY_6th, KEY_7th, KEY_8th }; ASKY can **ONLY** be acceded by word-write, read as 0	W

35.3.11 AES IV FIFO (ASIV)

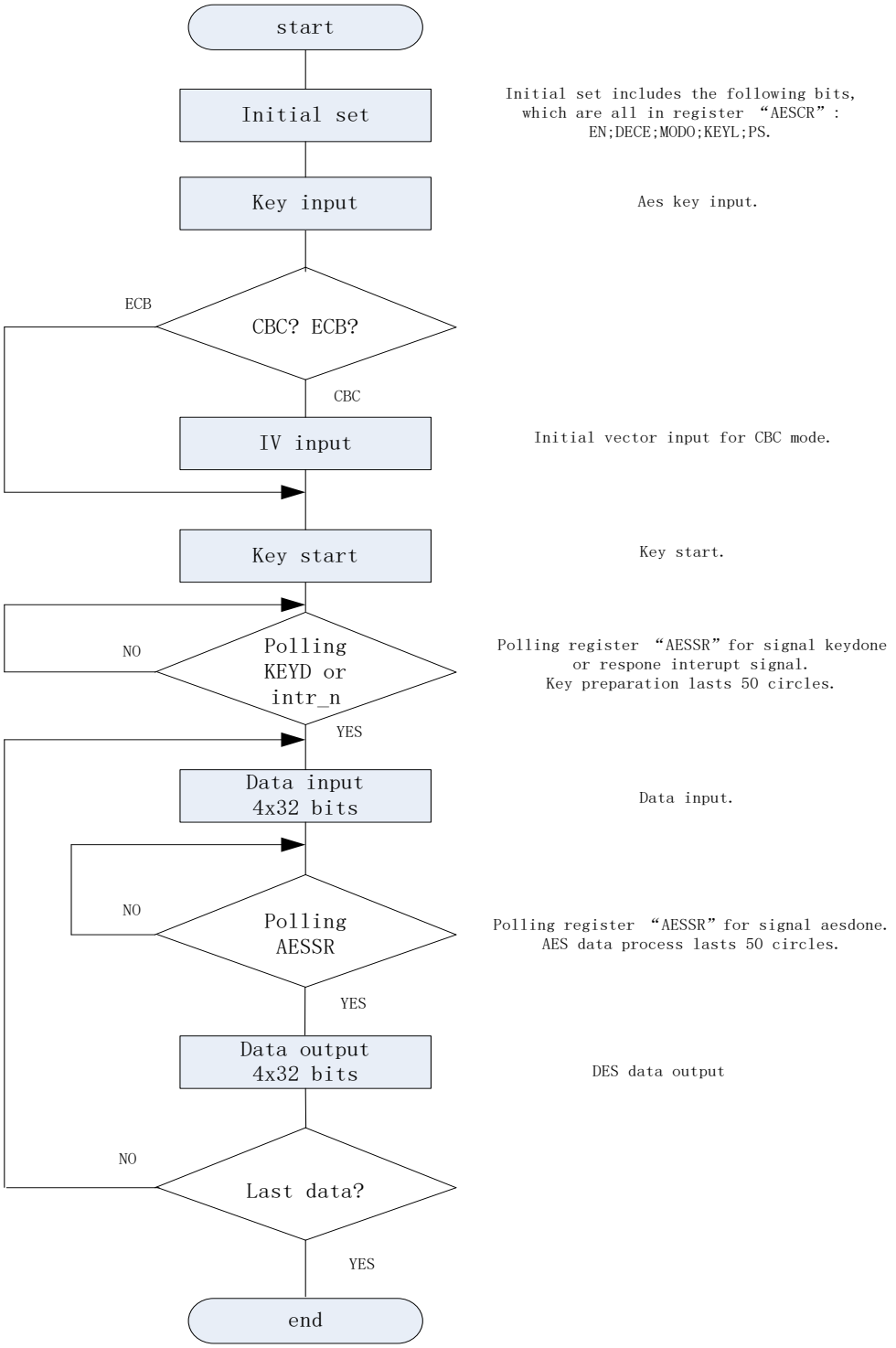
	ASIV																BASE+0x0024															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ASIV																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	ASIV	Initial Vector register The IV data flow is { IV_1st, IV_2ed, IV_3rd, IV_4th }; ASIV can **ONLY** be acceded by word-write, read as 0	W

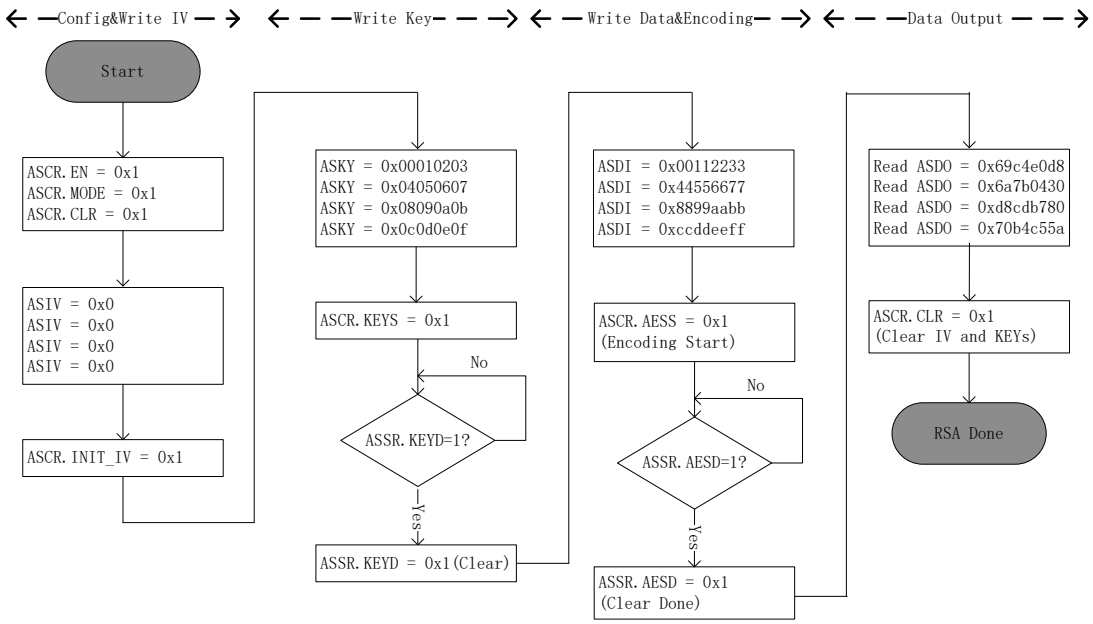
Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

35.4 Software User Guide

Running flow:



Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.



Example for software

Test Vectors:

128bit Key: 0x2b7e1516 28aed2a6 abf71588 09cf4f3c

IV: NULL

Data Input: 0x3243f6a8 885a308d 313198a2 e0370734

Encoding Output: 0x3925841d 02dc09fb dc118597 196a0b32

128bit Key: 0x2b7e1516 28aed2a6 abf71588 09cf4f3c

IV: 0x00010203 04050607 08090a0b 0c0d0e0f

Data Input: 0x6bc1bee2 2e409f96 e93d7e11 7393172a

Encoding Output: 0x7649abac 8119b246 cee98e9b 12e9197d

192bit Key: 0x00010203 04050607 08090a0b 0c0d0e0f 10111213 14151617

IV: NULL

Data Input: 0x00112233 44556677 8899aabb ccddeeff

Encoding Output: 0xdda97ca4 864cdfe0 6eaf70a0 0ec07191

256bit Key: 0x00010203 04050607 08090a0b 0c0d0e0f 10111213 14151617
18191a1b 1c1d1e1f

IV: NULL

Data Input: 0x00112233 44556677 8899aabb ccddeeff

Encoding Output: 0x8ea2b7ca 516745bf eafc4990 4b496089

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

36 SC_RSA

36.1 Overview

- RSA encrypt algorithm supporting 1k/2k key length

36.2 Feature

- RSA core:

Name	Input Data Lenth	Output Data Lenth	Run time @300MHz	BPS
RSA-1024	E(1024bit) N(1024bit) M(1024bit)	P(1024bit)	0.06s	2Kbyte/s
RSA-2048	E(2048bit) N(2048bit) M(2048bit)	P(2048bit)	0.5s	0.5Kbyte/s

36.3 Registers

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 1, write 0 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clears to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - Reset to 1
   0 - reset to 0
   ? - Value unknown after reset

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

36.3.1 Register Memory Map

Table 36-1 Registers Memory Map-Address Base

Name	Base	Description
RSA	0x13480000	RSA registers memory map address

Table 36-2 RSA registers description

Name	Description	Reset Value	Address offset	Access Size
RSAC	RSA control register	0x00030000	0x0000	32
RSAE	RSA E-key register	0x00000000	0x0004	32
RSAN	RSA N-key register	0x00000000	0x0008	32
RSAM	RSA M-message register	0x00000000	0x000c	32
RSAP	RSA P-output register	0x00000000	0x0010	32

36.3.2 RSA Ctrl Register (RSAC)

	RSAC																BASE+0x0000													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														RSA_INT_M	PER_INT_M	Reserved								RSA_SEL	Reserved	RSAD	RSAS	Reserved	PRED	PRES	EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
17	RSA_INT_M	**RSA Interrupt Mask** 1: Interrupt Mask 0: Interrupt Enable	WR
16	PER_INT_M	**PER Interrupt Mask** 1: Per Interrupt Mask 0: Per Interrupt Enable	WR
7	RSA_SEL	**RSA Mode Select:** 1: RSA-2048 0: RSA-1024	WR
5	RSAD	**RSA Main Process Done:** Write 1 to clear this bit.	W1R
4	RSAS	**RSA Main Process Start:** RSA Main Process Start. This bit is cleared automatically by hardware and always read as 0.	W1

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		$P = M^E \ (mod\ N)$	
2	PERD	**RSA Per-Process Done:** Write 1 to clear this bit. $R = 2^{2(n+2)} (\mathrm{mod}\ N)$ process done	W1R
1	PERS	**RSA Per-Process Start:** $R = 2^{2(n+2)} (\mathrm{mod}\ N)$	W1
0	EN	**RSA Enable:** 1: RSA Enable 0: RSA Disable NOTE: set this bit to 0 can clear RSAE、RSAN、RSAM、RSAP;	WR

36.3.3 RSA E-key Register (RSAE)

	RSAE																BASE+0x0004															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSAE																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	RSAE	**RSA E-key:** RSA2048: The write data for core is { RSAE_1st, RSAE_2ed,..., RSAE_63th, RSAE_64th}; RSA1024: The write data for core is { RSAE_1st, RSAE_2ed,..., RSAE_31th, RSAE_32th}; RSAE can ONLY be acceded by word-write(REG32). **NOTE:** Set RSAC.EN to 0 will clear this register to 0;	RWC

36.3.4 RSA N-key Register (RSAN)

	RSAN																BASE+0x0008															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSAN																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	RSAN	**RSA N-key:** RSA2048: The write data for core is { RSAE_1st, RSAE_2ed,..., RSAE_63th, RSAE_64th}; RSA1024: The write data for core is { RSAE_1st, RSAE_2ed,..., RSAE_31th, RSAE_32th}; RSAE can ONLY be acceded by word-write(REG32). **NOTE:** Set RSAC.EN to 0 will clear this register to 0;	RWC

36.3.5 RSA M-message Register (RSAM)

	RSAM																BASE+0x000C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSAM																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	RSAM	**RSA M-message:** RSA2048: The write data for core is { RSAM_1st, RSAM_2ed,..., RSAM_63th, RSAM_64th};(NOTE. the RSAM_1st's left-most byte MUST be 8'h00) RSA1024: The write data for core is { RSAM_1st, RSAM_2ed,..., RSAM_31th, RSAE_32th};(NOTE. the RSAM_1st's left-most byte MUST be 8'h00) RSAM can ONLY be acceded by word-write(REG32). **NOTE:** (1)Set RSAC.EN to 0 will clear this register to 0; (2)the RSAM_1st's left-most byte MUST be 8'h00;	RWC

36.3.6 RSA P-output Register (RSAP)

	RSAP																BASE+0x0010													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSAP																															

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

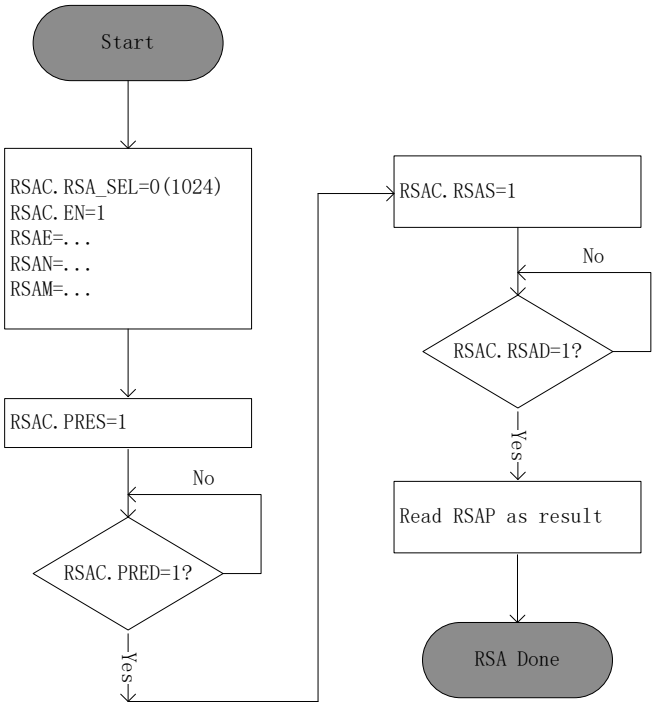
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	RSAP	**RSA P-output:** RSA2048: { RSAP_1st, RSAP_2ed,..., RSAP_63th, RSAP_64th}; RSA1024: { RSAP_1st, RSAP_2ed,..., RSAP_31th, RSAP_32th}; RSAP can ONLY be acceded by word-write(REG32). **NOTE:** Set RSAC.EN to 0 will clear this register to 0;	R

36.4 Software User Guide

Example:

$P = M^E \ (mod\ N)$



Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

37 SC_HASH HDL

37.1 Overview

- HASH digest algorithm
- HASH engine: SHA and MD5
- SHA1 fully referring to *RFC-3174* standard
- MD5 fully referring to *RFC-1321* standard

37.2 Feature

- AHB2 slave interface;
- AHB2 master interface;
- SHA core: support SHA 160/224/256/384/512bit digest;

Name	Vertion	Input Data Lenth	Output Data Lenth	Cycle	BPS
SHA1	160	512*n	160	88	73Mbyte/ (200MHz)
SHA2	224	512*n	224	64	
	256	512*n	256	64	
	384	1024*n	384	97	
	512	1024*n	512	97	
MD5		512*n	128	79	81Mbyte/ (200MHz)

37.3 Registers

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute

   R - Read only

   W - Write only

   RW - read and write

   RCW - read and write, but clear to 0 by read

   RSW - read and write, but set to 1 by read

   RWC - read and write, clear to 0 by write 1, write 0 has no effect

   RWS - read and write, set to 1 by write 1, write 0 has no effect

   RC - read only, and clears to 0 by read

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

RS - read only, and set to 1 by read

SPEC - special access method, relate to its description

3. Reset Value

1 - Reset to 1

0 - reset to 0

? - Value unknown after reset

37.3.1 Register Memory Map

Table 37-1 Registers Memory Map-Address Base

Name	Base	Description
HASH	0x13420000	HASH registers memory map address

Table 37-2 HASH registers description

Name	Description	Reset Value	Address offset	Access Size
HSCR	HASH control register	0x00000000	0x0000	32
HSSR	HASH status register	0x00000000	0x0004	32
HSINTM	HASH interrupt mask register	0x00000000	0x0008	32
HSSA	HASH DMA source address	0x00000000	0x000c	32
HSTC	HASH DMA transfer count	0x00000000	0x0010	32
HSDI	HASH data input	0x00000000	0x0014	32
HSDO	HASH data output	0x00000000	0x0018	32

37.3.2 Hash Ctrl Register (HSCR)

	HSCR																BASE+0x0000													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PS				Reserved																			DORVS	DIRVS	DMAS	DMAE	INIT	SEL			EN
RST	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:28	PS	Page Size, don't set these bits, and keep them default value. 0: don’t care 1: 1 KB 2: 2 KB	RW

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

		3: 4 KB(default) 4: 8 KB 5: 16 KB	
27:7	Reserved	Writing has no effect, read as zero.	R
8	DORVS	**Data output reveres**: big-end <> little-end If output data is odata[31:0] 0: the result is odata[31:0]; 1:the result is {odata[7:0],odata[15:8],odata[23:16],odata[31:24]}; In MD5 mode, this bit should set to 1 before data input.	WR
7	DIRVS	**Data input reveres**: big-end ~ little-end If input data is idata[31:0] 0: the result is idata[31:0]; 1:the result is {idata[7:0],idata[15:8],idata[23:16],idata[31:24]}; In SHA mode, this bit should be set to 1 before data input.	WR
6	DMAS	**DMA Start** This bit is cleared automatically by hardware and always read as 0.	RWS
5	DMAE	**DMA Enable**	WR
4	INIT	**Initial module for a New Round:** HASH Process Initial. This bit is cleared automatically by hardware and always read as 0. **NOTE:** ONLY a new round of hash begin this bit may set to 1.	RWS
3:1	SEL	**Hash Algorithm Selection :** 000: MD5 001: SHA1 010: SHA224 011: SHA256 100: SHA384 101: SHA512 110: Reserved 111: Reserved	WR
0	EN	**Hash Enable:** 1: Hash Enable 0: Hash Disable	WR

37.3.3 Hash Status Register (HSSR)

	HSCR																BASE+0x0004															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														MRD	ORD
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	MRD	**Multi Hash Round Done: the HSDO is valid** MRD ONLY for DMA read access done ; Set 1 to clear	RWC
0	ORD	**ONE Hash Round Done: the HSDO is valid** ORD for CPU read access done as usual ; Set 1 to clear	RWC

37.3.4 Hash Interrupt Mask Register (HSINTM)

	HSCR																BASE+0x0008													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														MR_INT_M	OR_INT_M
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writing has no effect, read as zero.	R
1	MR_INT_M	**MRD Interrupt Mask** 1: Interrupt Enable 0: Interrupt Mask(default)	WR
0	OR_INT_M	**ORD Interrupt Mask** 1: Interrupt Enable 0: Interrupt Mask(default)	WR

37.3.5 Hash DMA Source Address (HSSA)

	HSSA																BASE+0x000C													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	SA	**Source physical address for DMA use.**	WR

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

37.3.6 Hash Transfer Count (HSTC)

	HSTC																														BASE+0x0010	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TC																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	TC	**Transfer Count:** Number of Blocks(**1Block == 512bit**)	WR

37.3.7 Hash Data Input Register (HSDI)

	HSDI																														BASE+0x0014	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIN																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DIN	**Data Input:** Only support Word write	W

37.3.8 Hash Data Output Register (HSDO)

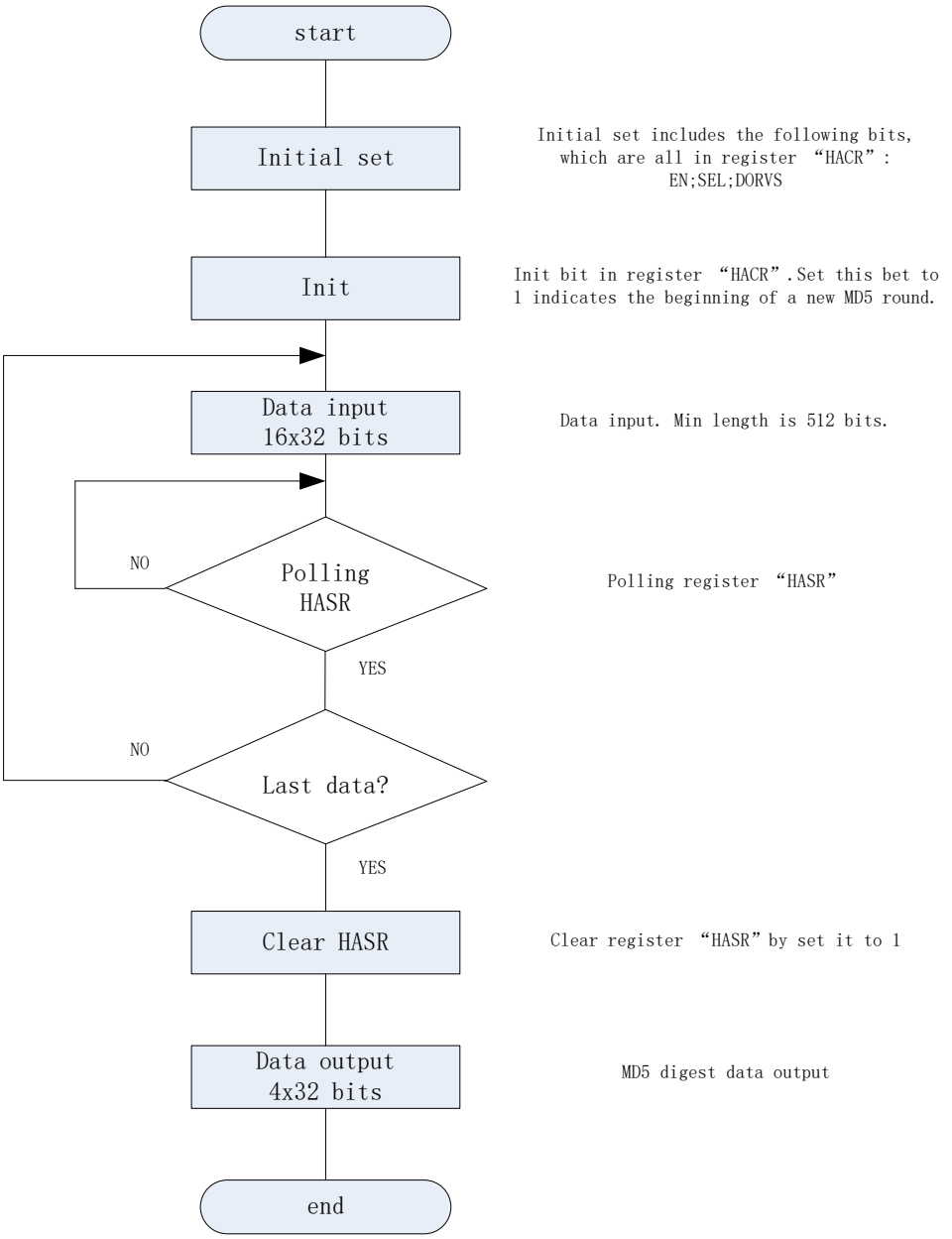
	HSDO																														BASE+0x0018	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DOUT																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DOUT	Data Output : Only support word read MD5: 128bit SHA1:160bit SHA224:224bit SHA256:256bit SHA384:384bit SHA512:512bit	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

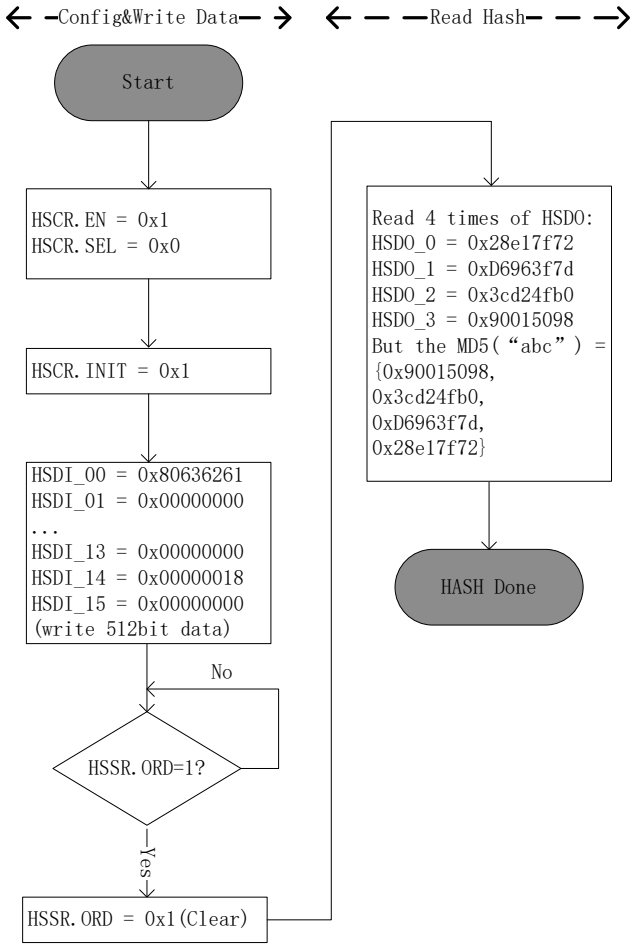
37.4 Software User Guide

37.4.1 HASH running flow:



Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

37.4.2 Example of MD5



MD5("abc") = 0x900150983cd24fb0d6963f7d28e17f72;
MD5 ("") = d41d8cd98f00b204e9800998ecf8427e
MD5 ("a") = 0cc175b9c0f1b6a831c399e269772661
MD5 ("abc") = 900150983cd24fb0d6963f7d28e17f72
MD5 ("message digest") = f96b697d7cb7938d525a2f31aaf161d0
MD5 ("abcdefghijklmnopqrstuvwxyz") = c3fcd3d76192e4007dfb496cca67e13b
MD5 ("ABCDEFGHIJKLMNOPQRSTUVWXYZabcdefghijklmnopqrstuvwxyz0123456789") = d174ab98d277d9f5a5611c2c9f419d9f
MD5 ("12345678901234567890123456789012345678901234567890123456789012345678901234567890") = 57edf4a22be3c955ac49da2e2107b67a
use Linux command md5sum

```
> md5sum -t file.txt
Note: if the original text is "abc" the actual text is "abc<LF>";
<LF> = 0x0a;
```

file.txt

```
abc
```


Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

37.4.3 Example of SHA1

SHA1("abc") = a9993e36 47068 16a ba3e2571 7850c26c 9cd0d89d

SHA1("abcdbcdecdefdefgefghfghighijhijkijkljklmklmnlmnomnopnopq") = 84983e44 1c3bd26e baae4aa1 f95129e5 e54670f1

SHA1 consists of 1,000,000 repetitions of the character " a " = 34aa973c d4c4daa4 f61eeb2b dbad2731 6534016f

37.4.4 Test Vectors

SHA1

Text: "abc"

Input: 80636261 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 18000000

output: a9993e36 4706816a ba3e2571 7850c26c 9cd0d89d

MD5

Text: "abc"

Input: 80636261 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000018 00000000

output: 90015098 3cd24fb0 d6963f7d 28e17f72

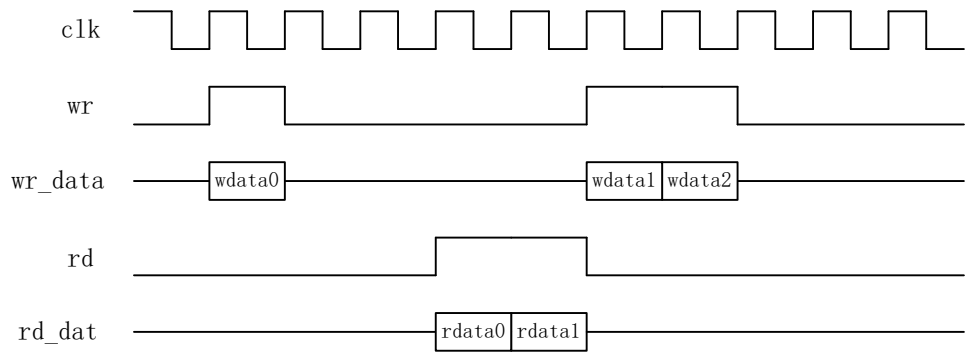
37.5 AHB Interface

37.5.1 AHB Slave Interface

System Signal			
Port Name	**IO**	**Width**	**Note**
clk	Input	1	Clock input
rst_n	Intput	1	Reset, active low
For Internal Module			
Port Name	**IO**	**Width**	**Note**
wr	output	1	Ahb bus write enable for internal module
wr_addr	output	5	Ahb bus write addr for internal module
wr_dat	output	32	Write 32bit data to internal module
rd	output	1	Ahb bus read enable for internal module
rd_addr	output	5	Ahb bus read addr for internal module
rd_data	input	32	Read 32bit data from internal module
For AHB Slave Interface			
Port Name	**IO**	**Width**	**Note**
haddr	input	32	

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

htran	input	2	
hwrite	input	1	
hburst	input	3	Single access ONLY
hsize	input	3	Word access ONLY
hsel	input	1	
hwdata	input	32	
hready	input	1	
hready_local	output	1	
hresp_local	output	2	MUST be AHB_OKAY = 2'b00
hrdata_local	output	32	

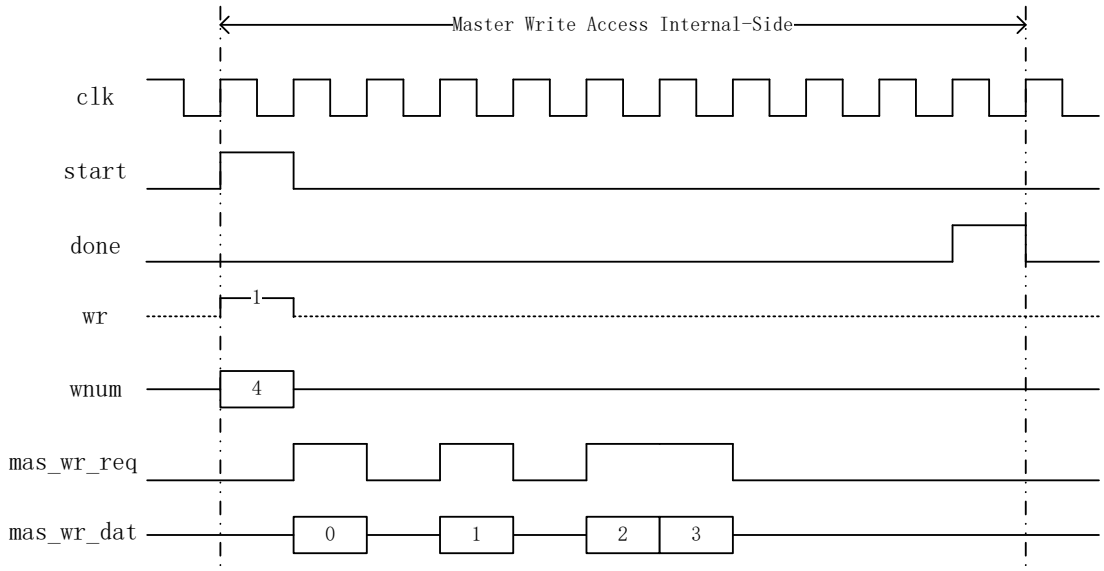


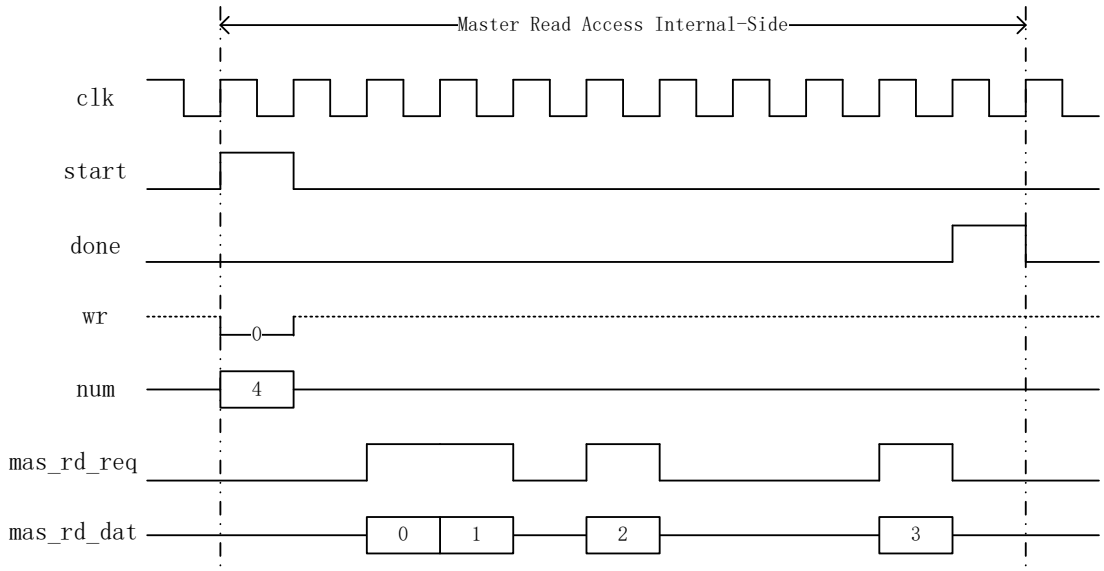
37.5.2 AHB Master Interface

System Signal			
Port Name	**IO**	**Width**	**Note**
clk	Input	1	Clock input
rst_n	Input	1	Reset, active low
For Internal Module			
Port Name	**IO**	**Width**	**Note**
start	Input	1	Start signal
done	output	1	Current access done
wr_rd	input	1	1: write data 0: read data
cmd	Input	2	Number of Words 00:INCR4 01:INCR16 10:INCR16x2
mas_wr_req	output	1	Master read data valid, combination logic output
mas_wr_dat	input	32	Master trans 32bit internal data to AHB, register input
mas_rd_req	output	1	Master read data valid, register output
mas_rd_dat	output	32	Master read 32bit data, and trans to internal module, register output

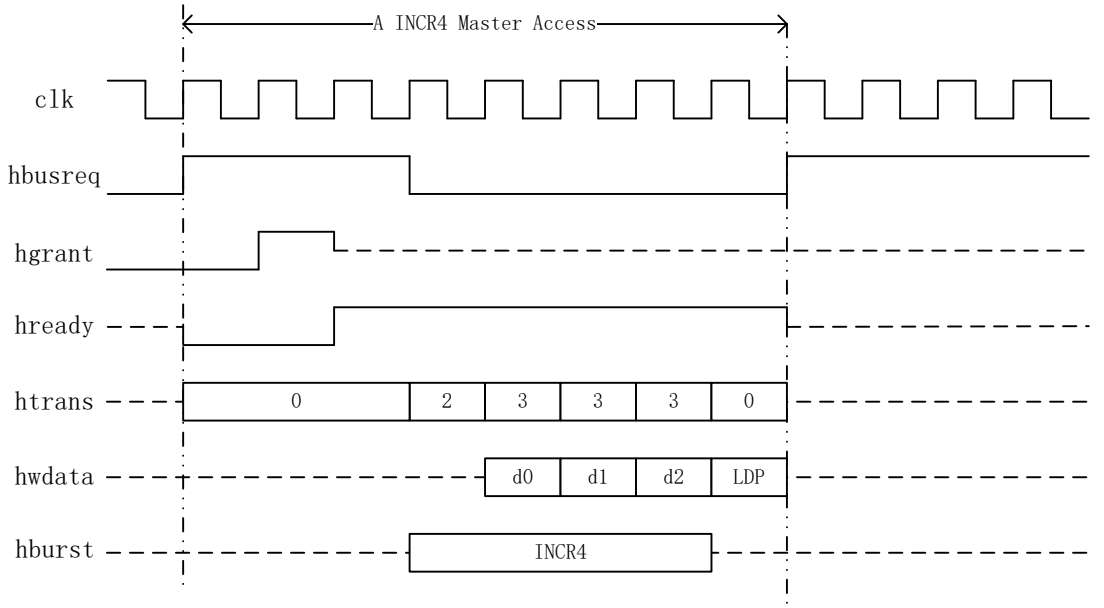
Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

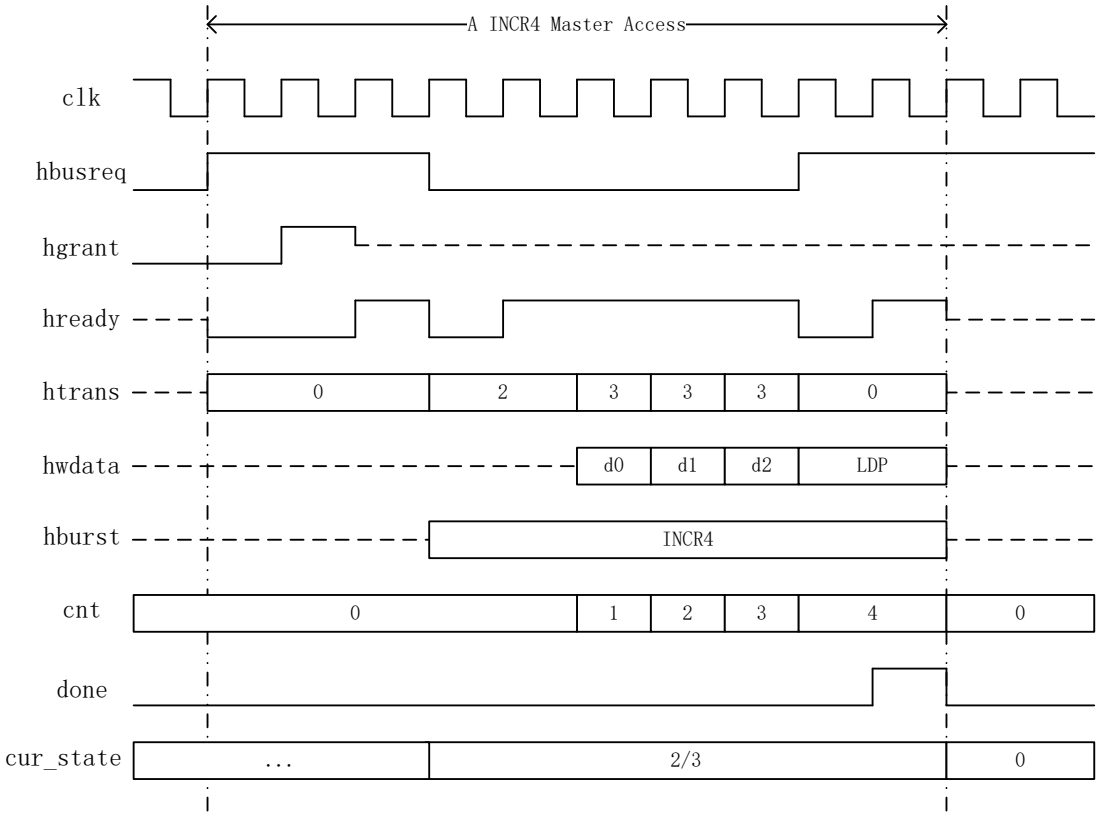
For AHB Master Interface			
Port Name	**IO**	**Width**	**Note**
haddr	Output	10	
htran	Output	2	
hwrite	Output	1	
hburst	Output	3	Support INCR4,INCR16
hsize	Output	3	Word access ONLY
hsel	Output	1	
hwdata	Output	32	
hready	Input	1	





Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.



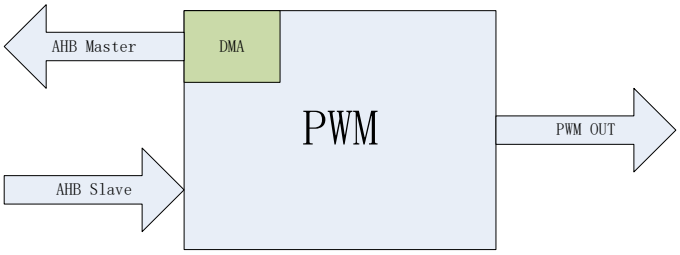


Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

38 Pulse Modulator Module

38.1 overview

This chapter describes the pluse modulator module, explains its modes of operation, and defines its registers.This module can produce PWM according to the configuration.



38.2 Features

- This module include 16 channels, the counter's clock is up to 500MHz. Each channel can be independently enabled.
- Two modes to update the PWM configuration: common update mode and DMA update mode.

38.3 Block Diagram

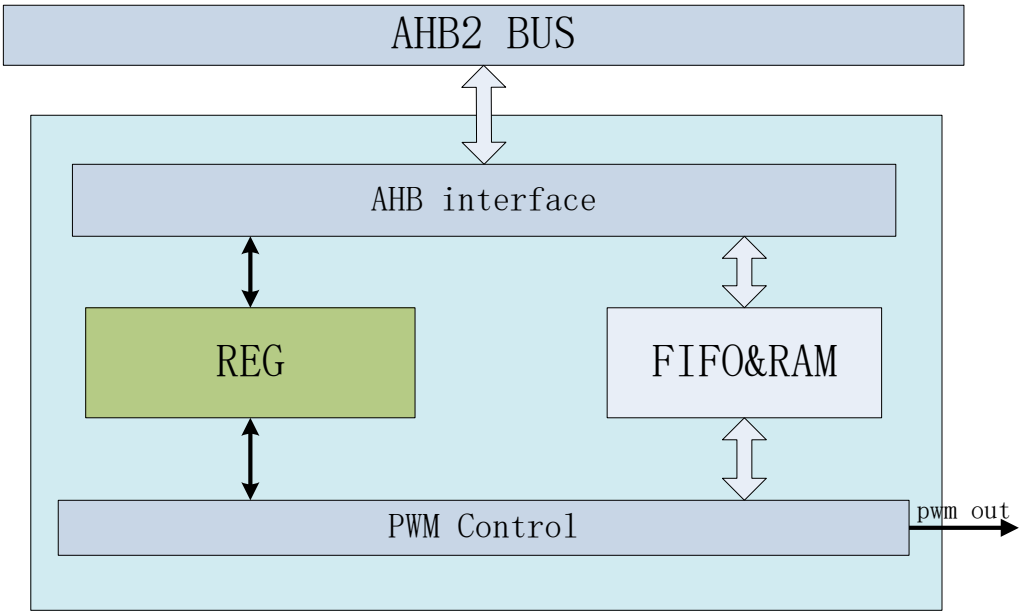


Figure 38-1 PWM Block Diagram

The AHB Interface includes one slave interface and one master interface. The slave interface is used for register configuration, and the master interface is used to DMA mode.

The FIFO is used as storing the PWM wave configuration information from AHB.

The PWM Control acts as a role to produce the PWM wave.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

38.4 register description

Following chapter will descript the functions of all software accessible registers.

Conventions:

1. Register Address = Base + Address offset
2. Register read/write attribute
   R - Read only
   W - Write only
   RW - read and write
   RCW - read and write, but clear to 0 by read
   RSW - read and write, but set to 1 by read
   RWC - read and write, clear to 0 by write 0, write 1 has no effect
   RWS - read and write, set to 1 by write 1, write 0 has no effect
   RC - read only, and clear to 0 by read
   RS - read only, and set to 1 by read
   SPEC - special access method, relate to its description
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

Table 38-1 Registers Memory Map-Address Base

Name	Base	Description
PWM	0x134C0000	Address base of PWM

Table 38-2 SYS_OST Registers Configuration

Name	Description	RW	Reset Value	Address offset	Access Size
PWMCCFG0	PWM Clock Configure Register	RW	0x00000000	0x0000	32
PWMCCFG1	PWM Clock Configure Register	RW	0x00000000	0x0004	32
PWMENS	PWM enable set register	W	-	0x0010	32
PWMENC	PWM enable clear register	W	-	0x0014	32
PWMEN	PWM enable status register	R	0x00000000	0x0018	32
PWMUPDATE	PWM update register	W	0x00000000	0x0020	32
PWMBUSYR	PWM update process busy status register	R	0x00000000	0x0024	32
PWMLVL	PWM channel n init/idle level configure register	RW	0x00000000	0x0030	32

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

PWMWCFG0~15	PWM channel n waveform configure	RW	0x00000000	0x00B0+n*4	32
PWMDES	PWM DMA enable Set register	W	0x00000000	0x100	32
PWMDEC	PWM DMA enable clear register	W	0x00000000	0x104	32
PWMDE	PWM DMA enable Status register	R	0x00000000	0x108	32
PWMDCR0	PWM DMA mode select control register	RW	0x00000000	0x110	32
PWMDCR1	PWM DMA mode loop control register	RW	0x00000000	0x114	32
PWMDTRIG	PWM DMA trigger register	W	0x00000000	0x120	32
PWMDFER	PWM DMA fifo empty register	R	0x0000FFFF	0x124	32
PWMDFSM	PWM DMA FSM register	R	0x00000000	0x128	32
PWMDSR	PWM DMA status register	R	0x00000000	0x130	32
PWMDSCR	PWM DMA status Clear register	W	0x00000000	0x134	32
PWMDINTC	PWM DMA Interrupt Control register	RW	0x0000FFFF	0x138	32
PWMnDAR	PWMn DMA memory address register	RW	0x00000000	0x0140+n*4	32
PWMnDTLR	PWMn DMA transfer length register	RW	0x00000000	0x0190+n*4	32
PWMOEN	PWMn output enable (X2000-V12 PWM/TCU func0)	RW	0x00000000	0x300	32

38.4.1 PWM Counter Clock Configure Register (PWMCFG0,1)

	PWMCCFG0																BASE+0x0000													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PRESCALE7				PRESCALE6				PRESCALE5				PRESCALE4				PRESCALE3				PRESCALE2				PRESCALE1				PRESCALE0			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	PWMCCFG1																BASE+0x0004													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PRESCALE15				PRESCALE14				PRESCALE13				PRESCALE12				PRESCALE11				PRESCALE10				PRESCALE9				PRESCALE8			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	PRESCALEn (n=0~15)	These bits select the PWM count clock frequency for each channel. Don't change this field when the channel is running. For PRESCALEn <8:Freq= input counter clock/(2^PRESCALEn) For PRESCALEn >=8:Reserved	RW

38.4.2 PWM Counter Enable Register (PWMEN, PWMENS, PWMENC)

The PWMEN is a 32-bit read-only register. It contains the counter enable control bits for each channels. It is initialized to 0x00000000 by any reset. It can only be set/clear by the register PWMENS and PWMENC. Since the enable control bits are located in the same addresses, different channel can be started at the same time. (Default: disable)

	PWMENS																BASE+0x0010													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PWM15ENS	PWM14ENS	PWM13ENS	PWM12ENS	PWM11ENS	PWM10ENS	PWM9ENS	PWM8ENS	PWM7ENS	PWM6ENS	PWM5ENS	PWM4ENS	PWM3ENS	PWM2ENS	PWM1ENS	PWM0ENS
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	PWMnENS	Enable the counter in PWM channeln's timer. 0: no effect 1: set PWNEN.PWMnEN to 1	W

	PWMENC																BASE+0x0014													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PWM15ENC	PWM14ENC	PWM13ENC	PWM12ENC	PWM11ENC	PWM10ENC	PWM9ENC	PWM8ENC	PWM7ENC	PWM6ENC	PWM5ENC	PWM4ENC	PWM3ENC	PWM2ENC	PWM1ENC	PWM0ENC
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	PWMnENC	Disable the counter in channel2's timer. 0: no effect 1: clear PWNEN.PWMnEN to 0	W

	PWMEN																BASE+0x0018													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PWM15EN	PWM14EN	PWM13EN	PWM12EN	PWM11EN	PWM10EN	PWM9EN	PWM8EN	PWM7EN	PWM6EN	PWM5EN	PWM4EN	PWM3EN	PWM2EN	PWM1EN	PWM0EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	PWMnEN	Enable the counter in channeln's timer. 0: The PWM is disable 1: The PWM is enable	R

38.4.3 PWM Update Register (PWMUPDATE)

Write 1 to each bit to update related PWM channel's counter period and pulse start/end position. Only set in common mode.

	PWMUPDATE																BASE+0x0020													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PWM15UP	PWM14UP	PWM13UP	PWM12UP	PWM11UP	PWM10UP	PWM9UP	PWM8UP	PWM7UP	PWM6UP	PWM5UP	PWM4UP	PWM3UP	PWM2UP	PWM1UP	PWM0UP
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	PWMnUP	Update the PWM's waveform configuration. Write 0 has no effect. Write 1 to update.	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

38.4.4 PWM Update Process Busy Status Register (PWMBUSYR)

After setting update bit for one channel, the related PWMnBUSY bit will keep 1 until the update takes effection. Only used in common mode.

	PWMBUSYR																BASE+0x0024													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PWM15BUSY	PWM14BUSY	PWM13BUSY	PWM12BUSY	PWM11BUSY	PWM10BUSY	PWM9BUSY	PWM8BUSY	PWM7BUSY	PWM6BUSY	PWM5BUSY	PWM4BUSY	PWM3BUSY	PWM2BUSY	PWM1BUSY	PWM0BUSY
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

38.4.5 PWM LEVEL Register (PWMLVL)

Channel n wave level configuration(n represents the PWM channel n).

	PWMLVL																BASE+0x0030													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ch15_idle_lvl	ch14_idle_lvl	ch13_idle_lvl	ch12_idle_lvl	ch11_idle_lvl	ch10_idle_lvl	Ch9_idle_lvl	Ch8_idle_lvl	Ch7_idle_lvl	Ch6_idle_lvl	Ch5_idle_lvl	Ch4_idle_lvl	Ch3_idle_lvl	Ch2_idle_lvl	ch1_idle_lvl	Ch0_idle_lvl	ch15_init_lvl	ch14_init_lvl	ch13_init_lvl	ch12_init_lvl	ch11_init_lvl	ch10_init_lvl	ch9_init_lvl	ch8_init_lvl	ch7_init_lvl	ch6_init_lvl	ch5_init_lvl	ch4_init_lvl	ch3_init_lvl	ch2_init_lvl	ch1_init_lvl	ch0_init_lvl
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	chn_idle_lvl	Channel n wave idle level configuration	RW
15:0	chn_init_lvl	Channel n wave init level configuration	RW

38.4.6 PWM Waveform Configuration(PWMWCFGn)

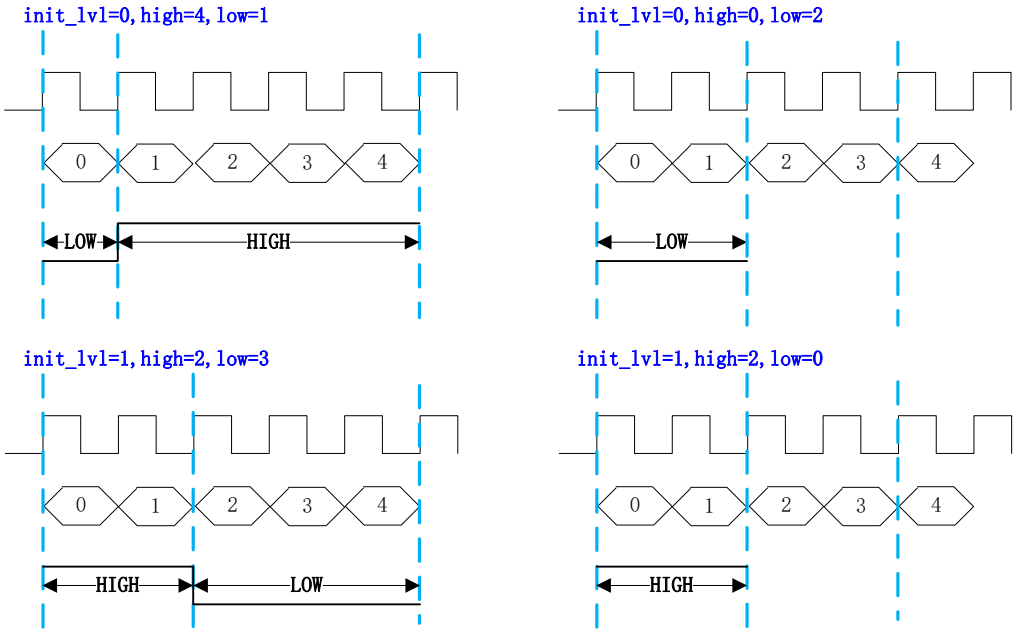
Only set in common mode.

	PWMWCFGn																BASE+0x00B0+n*4													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HIGH																LOW															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	HIGH	Waveform high level cycle number.	RW
15:0	LOW	Waveform low level cycle number.	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

The PWM's waveform show in figure below:



Note : dma mode high+low must >=2.

38.4.7 PWM DMA Enable Register (PWMDE, PWMDES, PWMDEC)

The PWMDE is a 32-bit read-only register. It contains the enable control bits for each channels. It is initialized to 0x00000000 by any reset. It can only be set/clear by the register PWMDES and PWMDEC.

	PWMDES																BASE+0x0100													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PWM15DES	PWM14DES	PWM13DES	PWM12DES	PWM11DES	PWM10DES	PWM9DES	PWM8DES	PWM7DES	PWM6DES	PWM5DES	PWM4DES	PWM3DES	PWM2DES	PWM1DES	PWM0DES
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	PWMnDES	Enable the DMA in PWM channeln's 0: no effect 1: set PWNDE.PWMnDE to 1	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

	PWMDEC																BASE+0x0104															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PWM15DEC	PWM14DEC	PWM13DEC	PWM12DEC	PWM11DEC	PWM10DEC	PWM9DEC	PWM8DEC	PWM7DEC	PWM6DEC	PWM5DEC	PWM4DEC	PWM3DEC	PWM2DEC	PWM1DEC	PWM0DEC		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	PWMnDEC	Disable the DMA in channel2's 0: no effect 1: clear PWNDE.PWMnDE to 0	W

	PWMDE																BASE+0x0108															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PWM15DEN	PWM14DEN	PWM13DEN	PWM12DEN	PWM11DEN	PWM10DEN	PWM9DEN	PWM8DEN	PWM7DEN	PWM6DEN	PWM5DEN	PWM4DEN	PWM3DEN	PWM2DEN	PWM1DEN	PWM0DEN		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	PWMnDE	Enable the counter in channeln's. 0: The PWM DMA is disable 1: The PWM DMA is enable	R

38.4.8 PWM DMA Control Register0(PWMDCR0)

	PWMDCR0																BASE+0x0110															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CH15_DMA_MODE	CH14_DMA_MODE	CH13_DMA_MODE	CH12_DMA_MODE	CH11_DMA_MODE	CH10_DMA_MODE	CH9_DMA_MODE	CH8_DMA_MODE	CH7_DMA_MODE	CH6_DMA_MODE	CH5_DMA_MODE	CH4_DMA_MODE	CH3_DMA_MODE	CH2_DMA_MODE	CH1_DMA_MODE	CH0_DMA_MODE		
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

15:0	CHn_DMA_MODE	0: Register mode 1: DMA mode	RW

38.4.9 WM DMA Control Register1(PWMDCR1)

	PWMDCR1																BASE+0x0114													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CH15_DMA_LOOP	CH14_DMA_LOOP	CH13_DMA_LOOP	CH12_DMA_LOOP	CH11_DMA_LOOP	CH10_DMA_LOOP	CH9_DMA_LOOP	CH8_DMA_LOOP	CH7_DMA_LOOP	CH6_DMA_CLOOP	CH5_DMA_LOOP	CH4_DMA_LOOP	CH3_DMA_LOOP	CH2_DMA_LOOP	CH1_DMA_LOOP	CH0_DMA_LOOP
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	CHn_DMA_LOOP	Write 1 to enable channel n loop DMA transmission Write 0 to disable channel n loop DMA transmission	RW

38.4.10 PWM DMA Transfer Trigger Register(PWMDTRIG)

	PWMDTRIG																BASE+0x0120													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CH15_DMA_START	CH14_DMA_START	CH13_DMA_START	CH12_DMA_START	CH11_DMA_START	CH10_DMA_START	CH9_DMA_START	CH8_DMA_START	CH7_DMA_START	CH6_DMA_START	CH5_DMA_START	CH4_DMA_START	CH3_DMA_START	CH2_DMA_START	CH1_DMA_START	CH0_DMA_START
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	CHn_DMA_START	Write 1 to start dma transmission Auto clear 0 next cycle	W

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

38.4.11 PWM DMA Fifo Empty Status Register(PWMDFER)

	PWMDFER																BASE+0x0124													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CH15_DFE	CH14_DFE	CH13_DFE	CH12_DFE	CH11_DFE	CH10_DFE	CH9_DFE	CH8_DFE	CH7_DFE	CH6_DFE	CH5_DFE	CH4_DFE	CH3_DFE	CH2_DFE	CH1_DFE	CH0_DFE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	CHn_DFE	1: FIFO empty 0: FIFO not empty	R

38.4.12 PWM DMA FSM Register(PWMDFSM)

	PWMDFSM																BASE+0x0128													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CH15_DFSM	CH14_DFSM	CH13_DFSM	CH12_DFSM	CH11_DFSM	CH10_DFSM	CH9_DFSM	CH8_DFSM	CH7_DFSM	CH6_DFSM	CH5_DFSM	CH4_DFSM	CH3_DFSM	CH2_DFSM	CH1_DFSM	CH0_DFSM
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	CHn_DFSM	1: DMA working 0: DMA idle	R

38.4.13 PWM DMA Status Register(PWMDSR)

	PWMDSR																BASE+0x0130													
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																DMA_END15	DMA_END14	DMA_END13	DMA_END12	DMA_END11	DMA_END10	DMA_END9	DMA_END8	DMA_END7	DMA_END6	DMA_END5	DMA_END4	DMA_END3	DMA_END2	DMA_END1	DMA_END0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	DMA_ENDn	1: DMA Trans End	R

38.4.14 PWM DMA Status Clear Register(PWMDSCR)

	PWMDSCR																BASE+0x0134															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																DMA_END_CLR15	DMA_END_CLR14	DMA_END_CLR13	DMA_END_CLR12	DMA_END_CLR11	DMA_END_CLR10	DMA_END_CLR9	DMA_END_CLR8	DMA_END_CLR7	DMA_END_CLR6	DMA_END_CLR5	DMA_END_CLR4	DMA_END_CLR3	DMA_END_CLR2	DMA_END_CLR1	DMA_END_CLR0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	DMA _END_CLRn	Write 1 to clear DMA Trans End Status	W

38.4.15 PWM DMA INTERRUPT Control Register(PWMDINTC)

	PWMDINTC																BASE+0x0138															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																DMA_INT_MASK15	DMA_INT_MASK14	DMA_INT_MASK13	DMA_INT_MASK12	DMA_INT_MASK11	DMA_INT_MASK10	DMA_INT_MASK9	DMA_INT_MASK8	DMA_INT_MASK7	DMA_INT_MASK6	DMA_INT_MASK5	DMA_INT_MASK4	DMA_INT_MASK3	DMA_INT_MASK2	DMA_INT_MASK1	DMA_INT_MASK0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	DMA _INT_MASKn	1: MASK (Default) 0: UNMASK	RW

38.4.16 PWM n DMA Memory Address Register (PWMnDMADDR)

	PWMnDMADDR																BASE+0x0140+n*4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MEM_ADDR																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:0	MEM_ADDR	Memory address	RW

38.4.17 PWM n DMA Transfer Length Register (PWMnDTLR)

	PWMnDTLR																BASE+0x0190+n*4															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																TRAN_LEN															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:0	TRAN_LEN	Transfer length	RW

38.4.18 PWM n Output Enable Register (PWMOEN)

The PWMOEN is a 32-bit register. It contains the ouput enable control bits for each channels (only X2000-V12). It is initialized to 0x00000000 by any reset.

	PWMOEN																BASE+0x300															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PWM15OEN	PWM14OEN	PWM13OEN	PWM12OEN	PWM11OEN	PWM10OEN	PWM9OEN	PWM8OEN	PWM7OEN	PWM6OEN	PWM5OEN	PWM4OEN	PWM3OEN	PWM2OEN	PWM1OEN	PWM0OEN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writing has no effect, read as zero.	R
15:0	PWMnOEN	IO Output Enable 0: disable 1: enable	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

38.5 Basic Operation

38.5.1 Register update mode

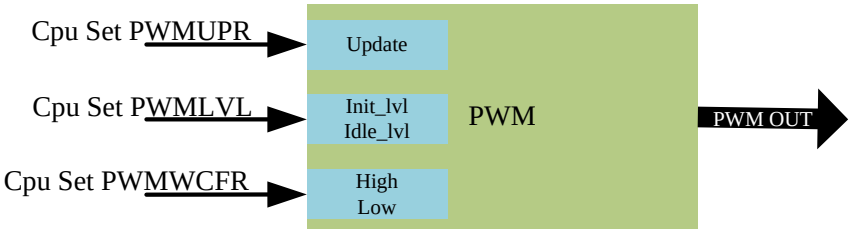
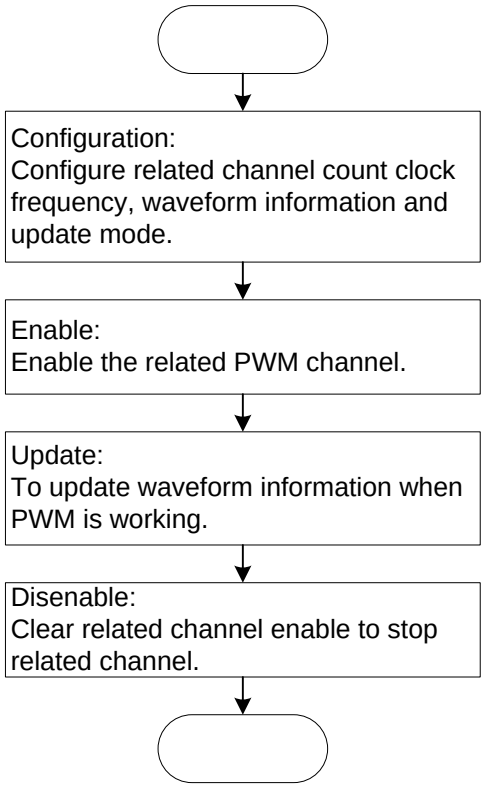


Figure 38-2 Register update mode



1. Configuration.
   a) Write PWMCCFG to set related channel count clock frequency.
   b) Write PWMLVL & PWMWCFG to set the related PWM channel's waveform.
   c) Write 0 to PWMDCR0.CHn_DMA_MODE to select the register mode.
2. Enable

   Set the PWMENS.PWMENSn bit to 1 to enable the related PWM channels. You can enable different channels at same time, and the related PWM channels will keep synchronized.
3. Update

   During PWM is working, if you want to change the waveform, you can set related registers as follows:

   Set PWMLVL & PWMWCFG, and set PWMUP.PWMnUP for related channel. Then polling related PWMBUSY.PWMnBUSY bit, after it is cleared to 0, the update information will take effection.
4. Disable

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Set PWMENC.PWMnENC to clear related channel's enable. The waveform will keep the last wave configuration.

38.5.2 DMA update mode

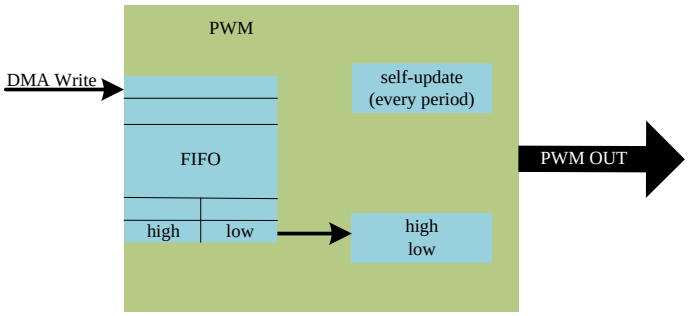
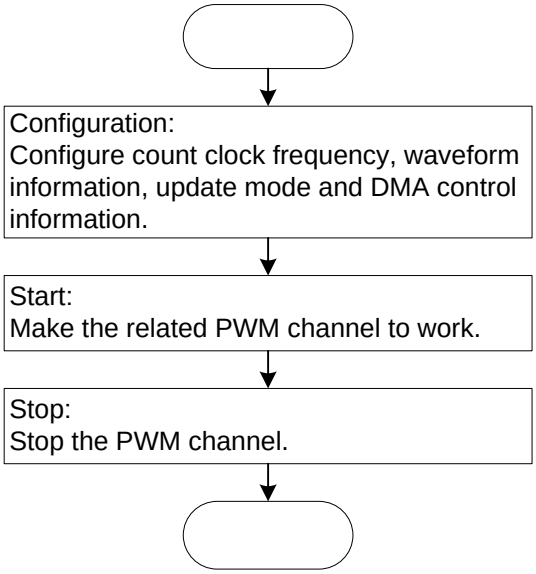


Figure 38-3 DMA update mode



1. Configuration.
   a) Write PWMCCFG to set related channel count clock frequency.(PWMCCFG cannot change after related channel is enabled, count clk must not less than AHB2 clk).
   b) Write PWMLVL to set the related PWM channel's waveform.
   c) Write 1 to PWMDCR0.CHn_DMA_MODE to select the DMA update mode.
   d) If you want channel n to loop the DMA transfer, set the PWMDCR1.CHn_DMA_LOOP bit to 1 (DMA_LOOP will not trigger DMA transfer end).
      If you want channel n to report interrupt to INTC, set the PWMDINTC.DMA_INT_MASK bit to 0 (default 1), and PWMDCR1.CHn_DMA_LOOP bit can't be setted 1.
   e) Write PWMnDMADDR and PWMnDTLR to set the DMA memory address and DMA transfer length.(DMA transfer length must 4 word align).
2. Start
   a) Wait PWMDFSM.CHn_DFSM bit to 0.
   b) Set the PWMDES.PWMDESn bit to 1 to enable the related PWM channels DMA.
   c) Set the PWMDTRIG.DMA_START to start DMA transfer.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

d) If multiple waveforms are required to be output simultaneously, wait for the PWMDFER.CHn_DFE of these channels to be 0 before PWMENS.PWMENSn setting

e) Set the PWMENS.PWMENSn bit to 1 to enable the related PWM channels.

3. Stop

a) If you want to configure the output waveform to complete output and then stop, you should wait for the PWMDSR.DMA_ENDn and then wait for PWMDFER.CHn_DFE to 1. Otherwise, directly perform the following steps.

b) Set the PWMDEC.PWMDECn bit to 1 to disable the related PWM channels DMA.

c) Set the PWMENC.PWMENCn bit to 1 to disable the related PWM channels.

4. Interrupt

Set PWMDSCR.END_CLRn bit to 1 to disable the channel n interrupt.

Set PWMDTRIG.CHn_DMA_START bit to 1 will restart DMA transfer, if you want to change wave configure , exec step 1 before Set PWMDTRIG.DMA_START.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

39 Digital True Random Number Generator （DTRNG）

39.1 Overview

DTRNG(Digital True Random Number Generator) is used to provide true random number encryption seed for system.

39.2 Features

- Pure digital logic circuits
- True random number
- APB bus configure Register
- Interrupt mode and no interrupt mode

39.3 Block Diagram

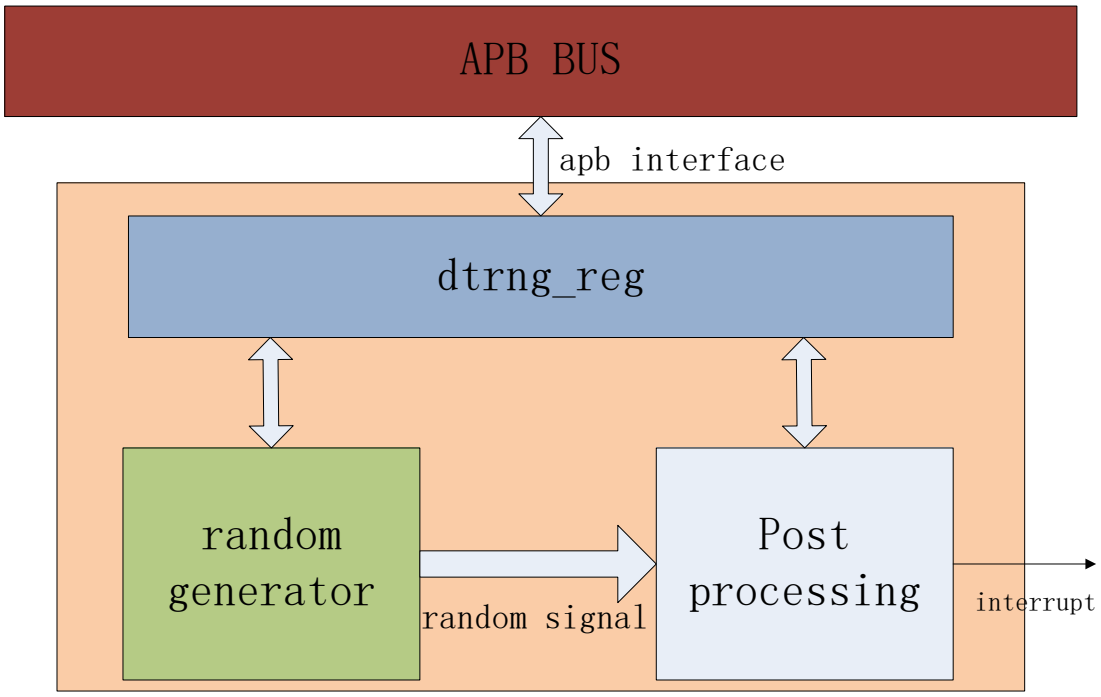


Figure 39-1 DTRNG Block Diagram

39.4 Register Description

Following chapter will describe the functions of all software accessible registers.

Conventions:

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

1. Register Address = Base + Address offset
2. Register read/write attribute
   R- Read only
   W- Write only
   RW- Read and Write
   RCW- Read and Write, but Clear to 0 by Read
   RSW- Read and Write, but Set to 1 by Read
   RWC- Read and Write, Clear to 0 by Write 1, Write 0 has no effect
   RWS- Read and Write, Set to 1 by Write 1, Write 0 has no effect
   RC- Read only, and Clear to 0 by read
   RS- Read only, and Set to 1 by read
3. Reset Value
   1 - reset to 1
   0 - reset to 0
   ? - value unknown after reset

39.4.1 Register Memory Map

Table 39-1 Registers Memory Map Base Address

Name	Base	Description
DTRNG	0x10072000	DTRNG

Table 39-2 DTRNG Registers Map

Name	RW	Reset Value	Address Offset	Access Size
DTRNG_CFG	RW	0x03ff0000	0x00	32
DTRNG_RANDOMNUM	RW	0x00000000	0x04	32
DTRNG_STAT	RW	0x00000000	0x08	32

39.4.2 Register and Fields Description

39.4.2.1 DTRNG CONFIG Register（DTRNG_CFG,0x00）

	TRNG_CFG																													0x0000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						line9_en	line8_en	line7_en	line6_en	line5_en	line4_en	line3_en	line2_en	line1_en	line0_en	Reserved			rdy_clr	int_mask	div_num										gen_en
RST	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

Bits	Name	Description	RW
31:26	Reserved	Writing has no effect. Read as zero.	R
25	line9_en	The enable of inverter9 1:enable the inverter 0: Disable the inverter	RW
24	line8_en	The enable of inverter8 1:enable the inverter 0: Disable the inverter	RW
23	line7_en	The enable of inverter7 1:enable the inverter 0: Disable the inverter	RW
22	line6_en	The enable of inverter6 1:enable the inverter 0: Disable the inverter	RW
21	line5_en	The enable of inverter5 1:enable the inverter 0: Disable the inverter	RW
20	line4_en	The enable of inverter4 1:enable the inverter 0: Disable the inverter	RW
19	line3_en	The enable of inverter3 1:enable the inverter 0: Disable the inverter	RW
18	line2_en	The enable of inverter2 1:enable the inverter 0: Disable the inverter	RW
17	line1_en	The enable of inverter1 1:enable the inverter 0: Disable the inverter	RW
16	line0_en	The enable of inverter0 1:enable the inverter 0:Disable the inverter	RW
15:13	Reserved	Writing has no effect. Read as zero.	R
12	rdy_clr	Ready clear signal: 1.Clear the interrupt 0.Normal work	RW
11	int_mask	The DTRNG interupt mask signal 1:mask the interupt 0:not mask the interupt	RW
10:1	div_num	The divder of pclk	RW

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

		The f(clk)=f(pclk)/(div_num+1) ;	
0	gen_en	The enable signal of DTRNG 1:enable the DTRNG 0:disable the DTRNG	RW

39.4.2.2 DTRNG RANDOM NUMBER REGISTER(DTRNG_RANDOMNUM,0x04)

	TRNG_RANDOMNUM																														0x0004
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	random_num																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	random_num	The random from DTRNG	R

39.4.2.3 DTRNG STATUS REGISTER(DTRNG_STAT,0x08)

	TRNG_STATUS																														0x0008
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																															random_rdy
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:1	Reserved	Writing has no effect. Read as zero.	R
0	random_rdy	The random data generate ready signal When READ: 1.The random data generate ready; 2.No random data generate ready;	R

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

39.5 Operation Flow

Interrupt mode:

1.configure　DTRNG_CFG.div_num, the f(dtrng_clk) = f(pclk)/(1+div_num);

2.Enable the DTRNG, configure DTRNG_CFG.gen_en to‘1’;

3.Wait interupt;

4.Read the random data from DTRNG_RANDOMNUM register

5.Clear the interupt, set DTRNG_CFG.rdy_clr to‘1’, then clear DTRNG_CFG.rdy_clr to‘0’;

Cpu mode:

1.configure　DTRNG_CFG.div_num, the f(dtrng_clk) = f(pclk)/(1+div_num);

2.Enable the DTRNG, configure DTRNG_CFG.gen_en to‘1’;

3.Read DTRNG_STAT.random_rdy until DTRNG_STAT.random_rdy is '1'

4.Read the random data from DTRNG_RANDOMNUM register

5.Clear the ramdom_rdy, set DTRNG_CFG.rdy_clr to‘1’, the clear DTRNG_CFG.rdy_clr to‘0’;

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Section 8

BOOT

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

40 XBurst Boot ROM Specification

The X2000 contains an internal 16KB boot ROM. The CPU boots from the boot ROM after reset.

40.1 Boot Select

The boot sequence of the X2000 is controlled by boot_sel [2:0]. The configuration is shown as follow:

Table 40-1 Boot Configuration of X2000

boot_sel[2:0]	Boot method
0 0 0	SFC@PE_3.3V
0 0 1	MSC2@PE_3.3V
0 1 0/1 1 0	USB
0 1 1	NOR
1 0 0	SFC@PD_1.8V
1 0 1	MSC0@PD
1 1 1	MSC2@PE_1.8V

40.2 Boot Procedure

After reset, the boot program on the internal boot ROM executes as follows:

Disable all interrupts, prepare the program running environment.

Read and save efuse values, the values to determine whether to improve system clock frequency, set MSC 4bit transmission data, gpio HI-Z, USB eye diagram.

Initialize clock and read boot_sel[2:0] to determine the boot method.

If it is boot from MMC/SD card at MSC0/MSC2, the boot program loads the 24KB data from MMC/SD card to SRAM and jump to it. The clock EXTCLK/122 is used initially. When reading data, the clock EXTCLK/4 is used. If the msc_bus_width_4 efuse value is set to 1, the function pins MSC_D0,MSC_D1,MSC_D2,MSC_D3 are initialized for 4bit data transmission, otherwise, only the MSC_D0 data bus is used.

If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in tcsm. Then branch to this area in tcsm.

If it is boot from SPI nor/nand at SFC, its function pins SFC_CLK,SFC_CE,SFC_DR,SFC_DT, SFC_WP, SFC_HOL are initialized, the boot program loads the spl size bytes code from nor/nand to SRAM and jump to it.

NOTE: The X2000's SRAM is 32KB, its address is from 0xB2400000 to 0xB2408000.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

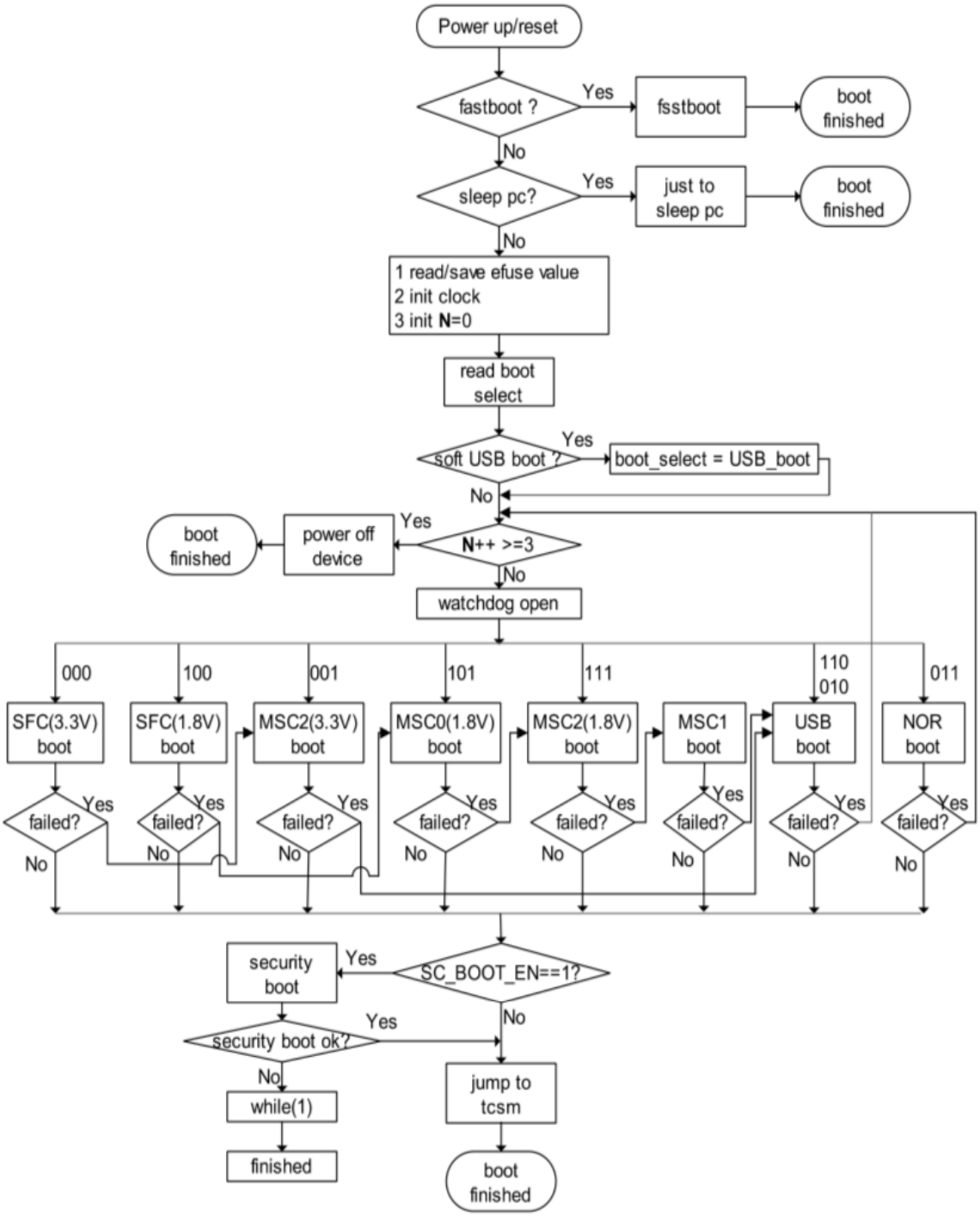
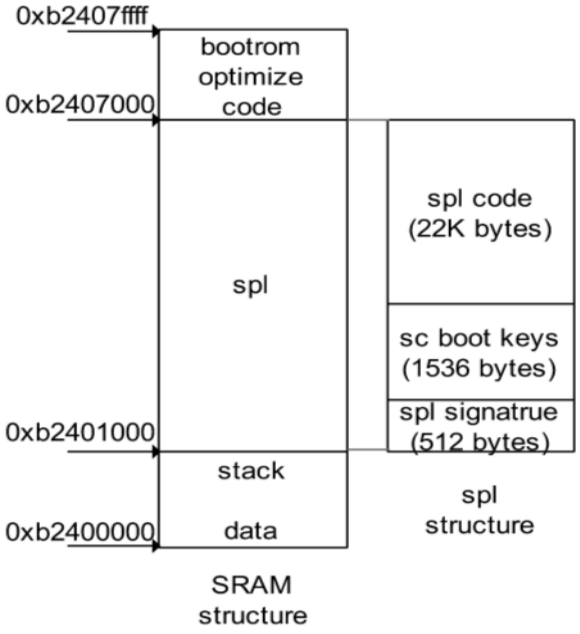


Figure 40-1 Boot sequence diagram of X2000

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

40.3 SPL Structure

For some special requirement, SPL(Second Program Loader) data needs to contain different



information according to the different boot modes. The basic structure as shown below. SC_Boot KEY (1.5K) use for security boot, SPL signature is used to store some information for kinds of boot (512B), and SPL.text (not more than22K,and 512 byte aligned) is real code segment. The first 4k bytes of SRAM address space is used for stack and data space. all the boot model must jump to 0xb2401000 to execute SPL code and all the boot model contains the SPL structure show as Figure 40-2. Every boot model has its unique SPL signature,Introduces the SPL signature structure behind.

Figure 40-2 The basic SPL structure

40.4 SPL Paramaters

In order to support variable length of SPL size and increase the loading speed by changing the clock frequency. The SPL parameter is created to accomplish this function. This mechanism is only used for SFC/SD/MMC boot, and this mechanism is optional.

Parameters in a storage space in a certain structure is placed, and the size is 256 bytes .When sd card boot, the parameters will be placed at 17K + 256 space

Table 40-2 SPL parameters structure

Offset	0x1 : 0x0	0x3 : 0x2	0x7 : 0x4	0xb : 0x8	0xf : 0xc
0x00	INGE		SPL length	CPU freq	Reserved
0x10	NAND Timing[0]		NAND Timing[1]	NAND Timing[2]	NAND Timing[3]
0x20	Desc[0].saddr	Desc[0].paddr	Desc[0].value	Desc[0].poll_h	Desc[0].poll_l
0x30	Desc[1].saddr	Desc[1].paddr	Desc[1].value	Desc[1].poll_h	Desc[1].poll_l
0x40	Desc[2].saddr	Desc[2].paddr	Desc[2].value	Desc[2].poll_h	Desc[2].poll_l
…	…	…	…	…	…
0xf0	Desc[13].saddr	Desc[13].paddr	Desc[13].value	Desc[13].poll_h	Desc[13].poll_l

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Domain in SPL parameter structure:

INGE：

SPL Params ID，must store ‘I’ ‘N’ ‘G’ ‘E’, if this area is not store “INGE”,bootrom will use default params to boot.

SPL length：

The length of SPL in bytes, and must be 512 byte aligned. the size of SPL must be not more than 24K.

CPU freq：

Cpu frequency conversion value in HZ.

NAND Timing[0~3]：

After frequency conversion, the timing parameters of NAND.

```
struct {
        unsigned set_rw:8;
        unsigned wait_rw:8;
        unsigned hold_rw:8;
        unsigned set_cs:8;
        unsigned wait_cs:8;
        unsigned trr:8;
        unsigned tedo:8;
        unsigned trpre:8;
        unsigned twpre:8;
        unsigned tds:8;
        unsigned tdh:8;
        unsigned twpst:8;
        unsigned tdqsre:8;
        unsigned trhw:8;
        unsigned t1:8;
        unsigned t2:8;
    };
```

Descriptor：

A maximum of 14 groups descriptor, each descriptor is used to configure an cpm register.

The content of descriptor definition is as follows:

Saddr: Set Value Addr(This is lower 16 bits address , th higher 16bit address is 0xb000).

paddr: Polling Value Addr(This is lower 16 bits address , th higher 16bit address is 0xb000).

value: The configuration value of the “saddr” register

poll_h: Polling high bit mask(32bit).

poll_l: Polling low bit mask(32bit).

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

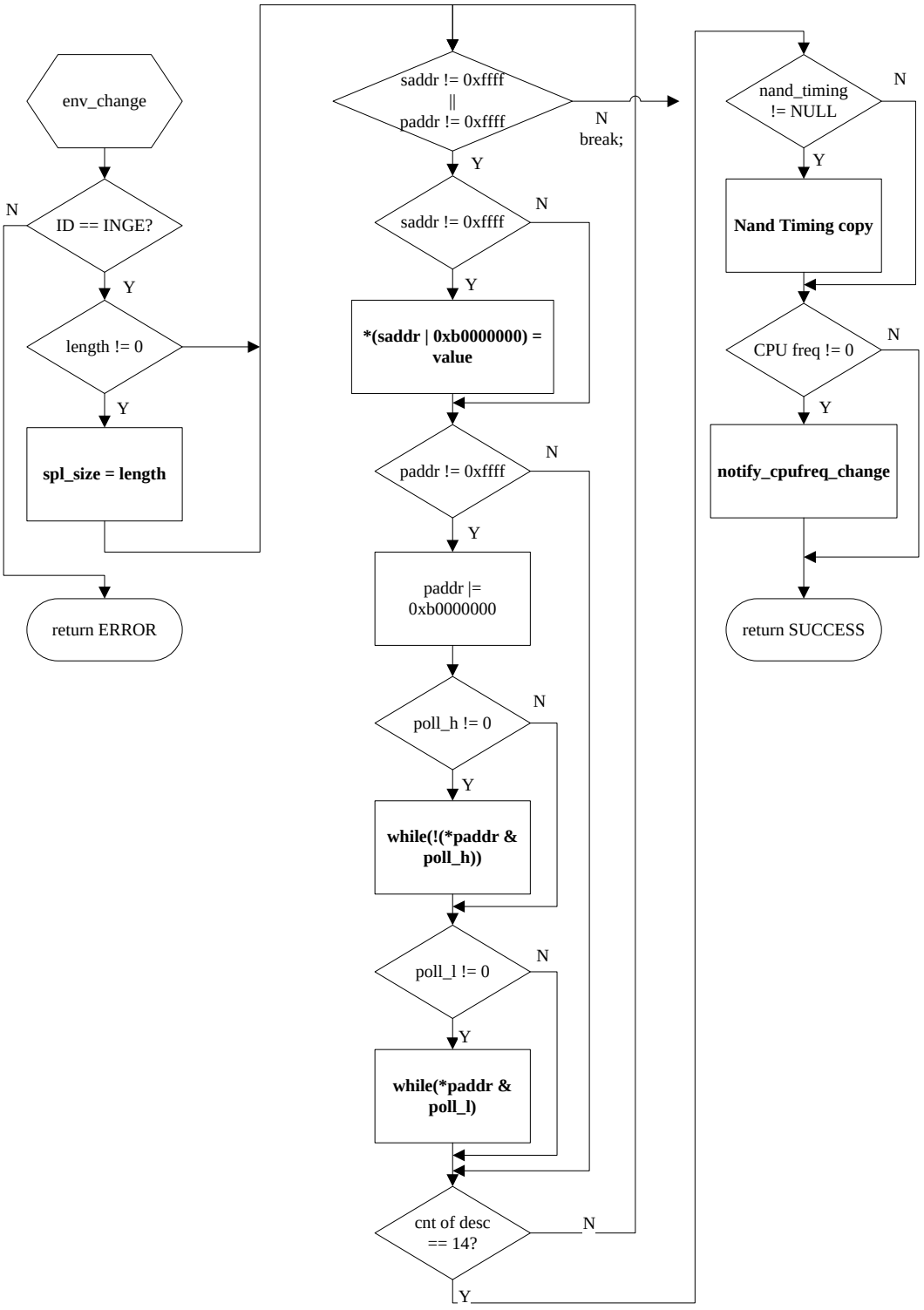


Figure 40-3 SPL configuration change Procedure

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

40.5 MSC Boot Specification

The MSC boot program will load 24KB code starting at address 0x4400 from MMC/SD card to SRAM. First the boot determine data transfer width through the efuse value, if 1 bit width initializes MSC_D0, MSC_CLK, MSC_CMD as function pins, if 4 bits width initializes MSC_D0, MSC_D1, MSC_D2, MSC_D3, MSC_CLK, MSC_CMD as function pins. Then the boot program sends CMD55 to test if it's SD or MMC card and initializes the card. At last it loads 24KB code from the card to cpu SRAM and branches to execute the code.

When initializing the card, the clock of EXTCLK/122 is used. And when reading data, the clock of EXTCLK/4 is used.

The procedure of the X2000 MMC/SD boot is shown as follow:

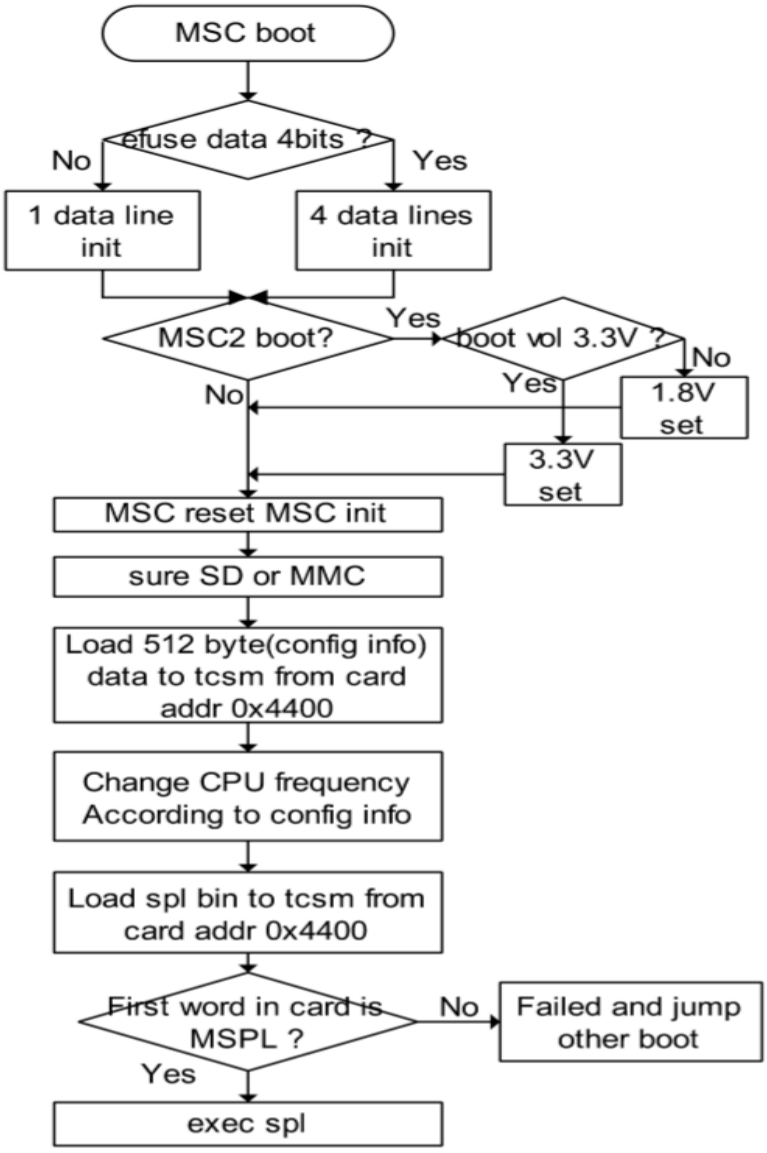


Figure 40-4 Typical Procedure of MSC0/MSC1/MSC2 boot

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

40.6 SFC boot Specification

When boot_sel[2:0] is selected as SFC boot, CPU will goes into SFC boot, AT first cpu fetch a 16 bytes flag information table(The first 16 bytes in SPL signature)from the SPI device. CPU check the flag table to decide the SPI address length , SPI device type(NOR flash or NAND flash), receive code length and the crc7 check data. SFC_boot detailed process shown “SFC Boot Procedure”

Note: Any irregularity in boot steps, SPI_boot will disable SFC controller and jump to MSC boot.

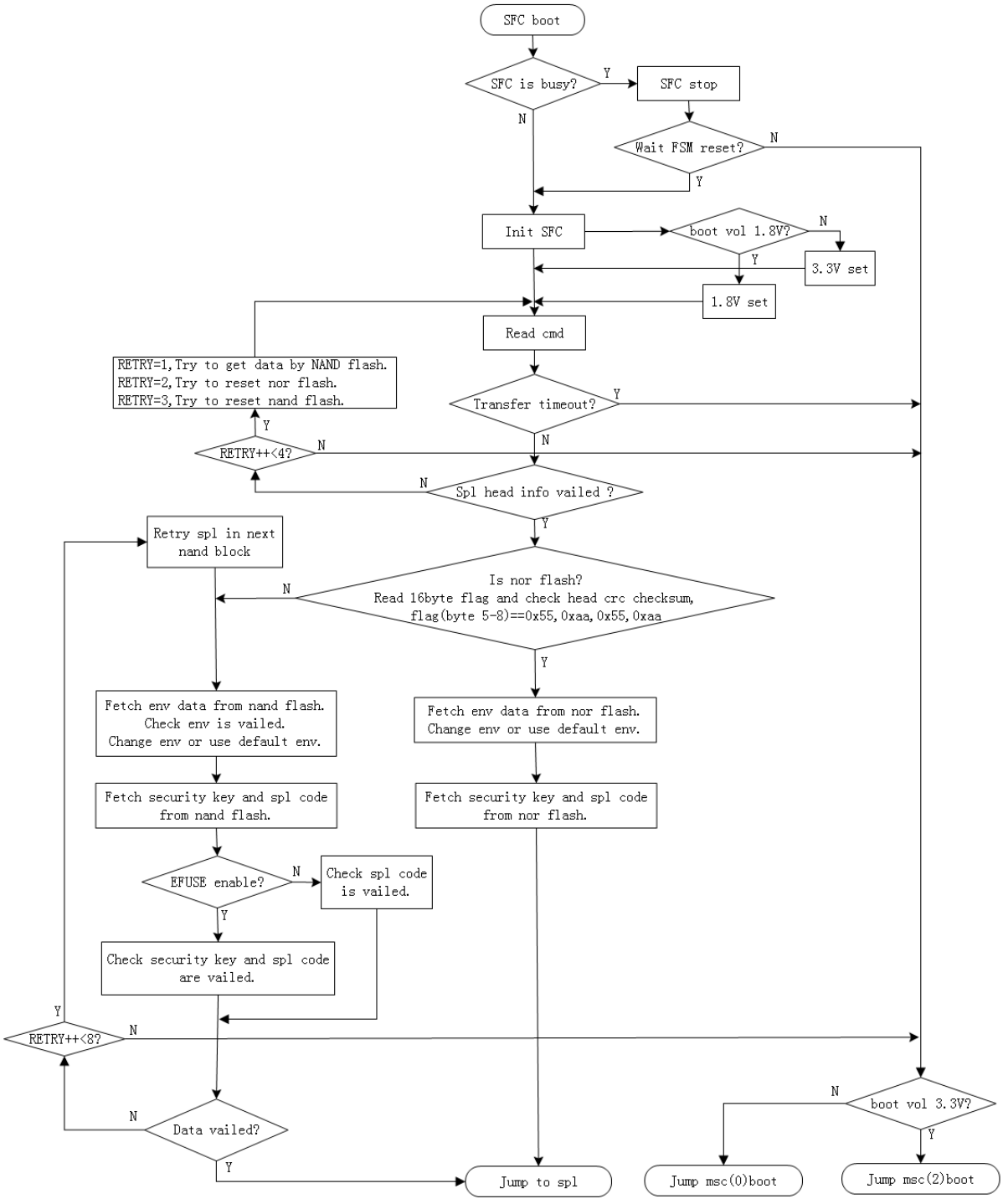


Figure 40-5 SFC Boot Procedure

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

SPI-NOR BOOT:

When SPI NOR flash by General-Purpose I/O Port-A 1,2,3,4 pin. In SPI NOR flash address 0x0~0xF, this space will store 16 bytes that agreed SPI boot flag.

The SPI boot flag information table and procedure of the X2000 SPI NOR boot is shown as follow:

Table 40-3 SPI NOR flash boot flag informations（in spl signature）

Addr	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
Detail	0x06	0x05	0x04	0x03	0x02	0x55	0xaa	0x55
Addr	0x8	0x9	0xa	0xb	0xc	0xd	0xe	0xf
Detail	0xaa	0x00	0x00	0x00	Len(LSB)	Len(MSB)	0x00	0x00

Explain:

0x00~0x04 :Must store 0x06,0x05,0x04,0x03,0x02
These part is used for cpu to decide the spi address length

0X05~0X08 :Must not be 0x55,0xAA,0x55,0xAA.
Magic code，device use this code decided whether is spi-nor flash boot

0x09~0x0b :Don't care.

0x0C~0x0D :The length of copy data.

0x0E~0X0F :Don't care.

SPI-NAND BOOT:

When SPI NAND flash by General-Purpose I/O Port-A 1,2,3,4 pin. Like spi nor flash, in spi NAND flash address 0x0~0xF, this space will store 16 bytes that agreed SPI_boot flag.

The SPI_boot flag information table and procedure of the X2000 SPI NAND boot is shown as follow:

Table 40-4 SPI NAND flash boot flag informations（in spl signature）

Addr	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
Detail	0x06	0x05	0x04	0x03	0x02	0x55	0xaa	0x55
Addr	0x8	0x9	0xa	0xb	0xc	0xd	0xe	0xf
Detail	0x00	Crc7	ppb	bpp	Len(LSB)	Len(MSB)	Env_crc	Head_crc

Explain:

0x00~0x04 :Must store 0x06,0x05,0x04,0x03,0x02
These part is used for cpu to decide the spi address length

0X05~0X08 :Must not be 0x55,0xAA,0x55,0x00.
Magic code，device use this code decided whether is spi-nand flash boot

0x09 :The copy code’s crc7 value .

0x0a :The pages per block of SPI Nand, the value is X/32, for example, the pages per block is 64, then ppb is 64/32=2.

0x0B :The bytes per page of SPI Nand, the value is X/1024, for example, the bytes per page is 2048, then bpp is 2048/1024=2.

0x0C~0x0D :The length of copy data.

0x0E :The env data code’s crc7 value .

0X0F :The first fifteen byte flags code’s crc7 value .

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

40.7 USB Boot Specification

When boot_sel[2:0] is selected as USB boot, the internal boot ROM downloads user program from the USB port to internal SRAM and branches to the internal SRAM to execute the program.

X2000 supports the external main crystal whose frequency is 24MHz.
The boot program supports both high-speed (480MHz) and full-speed (12MHz) transfer modes. The boot program uses the following two transfer types.

Table 40-5 Transfer Types Used by the Boot Program

Transfer Type	Description
Control Transfer	Used for transmitting standard requests and vendor requests.
Bulk Transfer	Used for responding to vendor requests and transmitting a user program.

The following figure shows an overview of the USB communication flow.

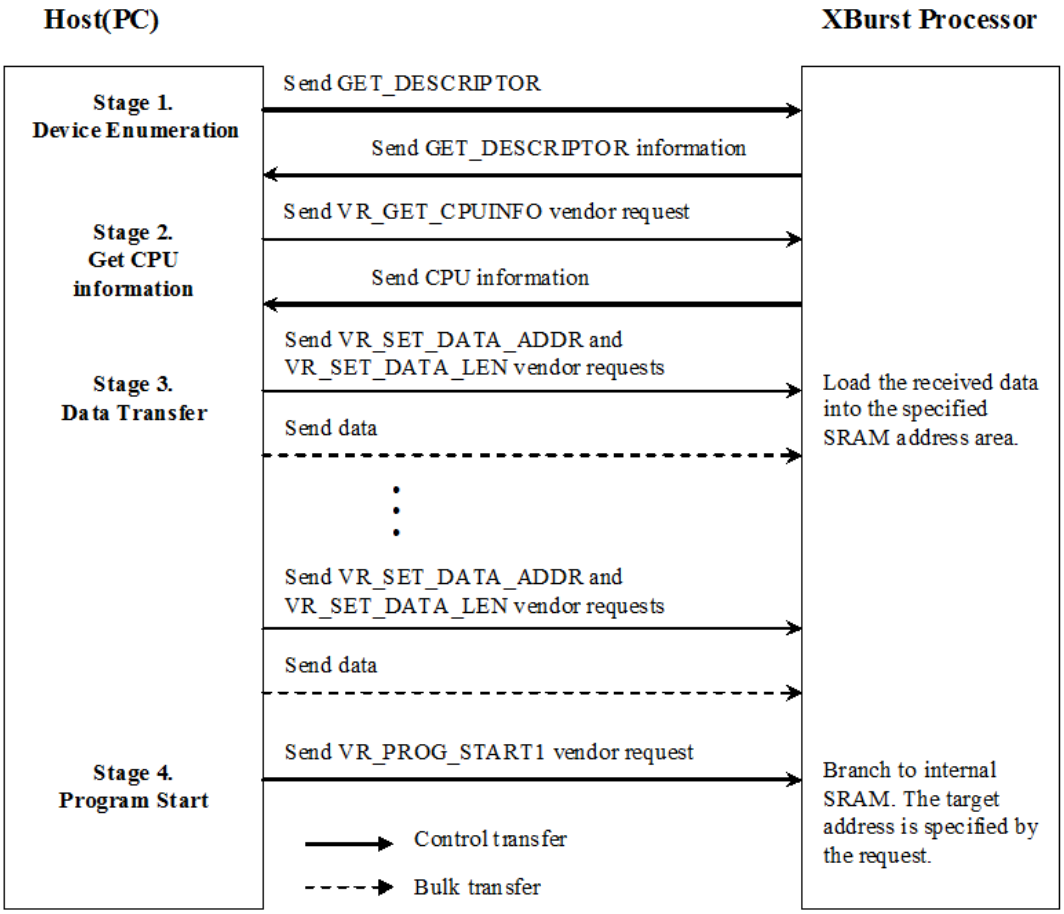


Figure 40-6 USB Communication Flow

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

The vendor ID and product ID for the USB boot device are 0xa108 and 0xEAEF respectively. The Configuration for USB is for Control Endpoint 0 with Max Packet Size equals 64 bytes, Bulk IN at Endpoint 1 with Max Packet Size equals 512 bytes in high-speed and 64 bytes in full-speed, Bulk OUT at Endpoint 1 with Max Packet Size equals 512 bytes in high-speed and 64 bytes in full-speed.

The USB boot program provides six vendor requests through control endpoint for user to download/upload data to/from device, and to branch to a target address to execute user program. The six vendor requests are VR_GET_CPU_INFO (0x00), VR_SET_DATA_ADDRESS (0x01), VR_SET_DATA_LENGTH (0x02), VR_FLUSH_CACHES (0x03), VR_PROGRAM_START1 (0x04) and VR_PROGRAM_START2 (0x05). User program is transferred through Bulk IN or Bulk OUT endpoint.

When X2000 is reset with boot_sel[2:0] equals 110b or 010b ,the internal boot ROM will switch to USB boot mode and wait for USB requests from host. After connecting the USB device port to host, host will recognize the connection of a USB device, and start device enumeration. After finishing the device enumeration, user can send VR_GET_CPU_INFO (0x00) to query the device CPU information. If user wants to download/upload a program to/from device, two vendor requests VR_SET_DATA_ADDRESS (0x01) and VR_SET_DATA_LENGTH (0x02) should be sent first to tell the device the address and length in byte of the subsequent transferring data. Then data can be transferred through bulk-out/bulk-in endpoint. After this first stage program has been transferred to device, user can send vendor request VR_PROGRAM_START1 (0x04) to let the CPU to execute the program. This first stage program must not greater than 20KB and is normally used to init GPIO and SDRAM of the target board. At the end of the first stage program, it can return back to the internal boot ROM by jumping to ra ($31) register. Thus user can download a new program to the SDRAM of the target board like the first stage, and send vendor request VR_FLUSH_CACHES (0x03) and VR_PROGRAM_START2 (0x05) to let the CPU to execute the new program. Next figure is the typical procedure of USB boot.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

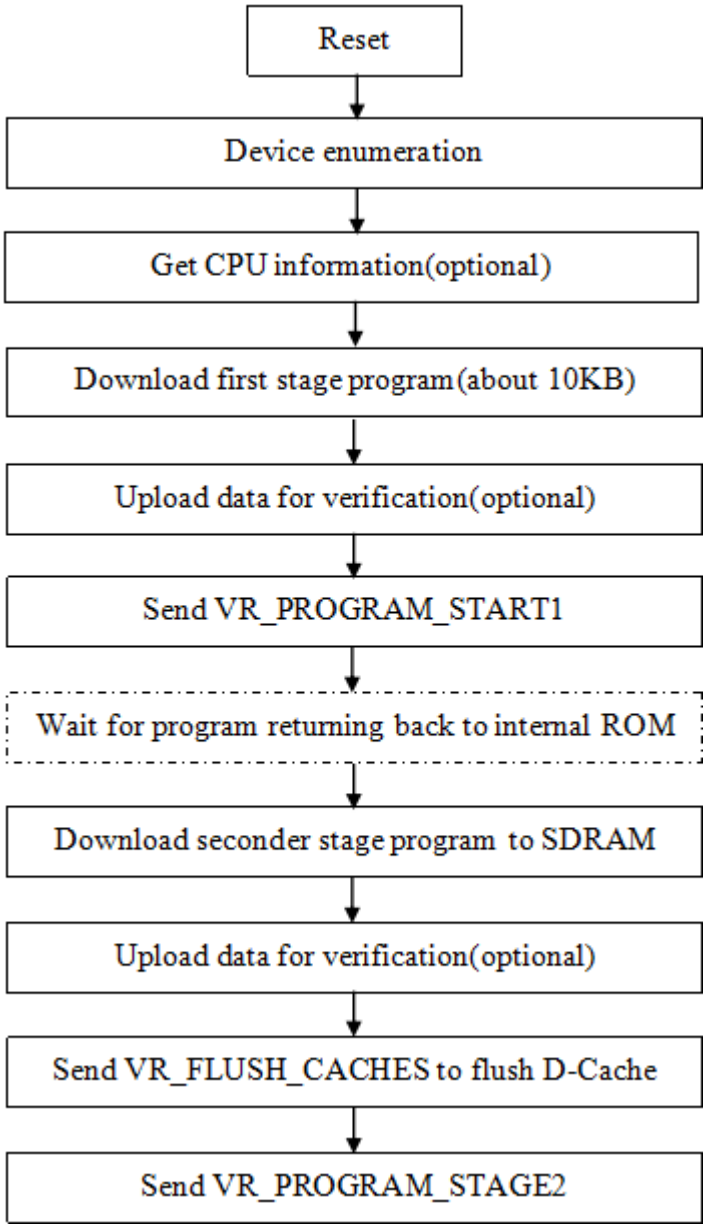


Figure 40-7 Typical Procedure of USB Boot

Following tables list all the vendor requests that USB boot program supports:

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.

Table 40-6 Vendor Request 0 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	00H	VR_GET_CPU_INFO: get CPU information.
2	wValue	2	0000H	Not in used.
4	wIndex	2	0000H	Not in used.
6	wLength	2	0008H	8 bytes.

Table 40-7 Vendor Request 1 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	01H	VR_SET_DATA_ADDRESS: set address for next bulk-in/bulk-out transfer.
2	wValue	2	xxxxH	MSB (bit[31:16]) of the data address.
4	wIndex	2	xxxxH	LSB (bit[15:0]) of the data address.
6	wLength	2	0000H	Not in used.

Table 40-8 Vendor Request 2 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	02H	VR_SET_DATA_LENGTH: set length in byte for next bulk-in/bulk-out transfer.
2	wValue	2	xxxxH	MSB (bit[31:16]) of the data length.
4	wIndex	2	xxxxH	LSB (bit[15:0]) of the data length.
6	wLength	2	0000H	Not in used.

Table 40-9 Vendor Request 3 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.

Copyright © 2005-2020 Ingenic Semiconductor Co., Ltd. All rights reserved.

1	bRequest	1	03H	VR_FLUSH_CACHES: flush I-Cache and D-Cache.
2	wValue	2	0000H	Not in used.
4	wIndex	2	0000H	Not in used.
6	wLength	2	0000H	Not in used.

Table 40-10 Vendor Request 4 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	04H	VR_PROGRAM_START1: transfer data from D-Cache to I-Cache and branch to address in I-Cache. **NOTE:** After downloading program from host to device for the first time, you can only use this request to start the program. Since the USB boot program will download data to D-Cache after reset. This request will transfer data from D-Cache to I-Cache and execute the program in I-Cache.
2	wValue	2	xxxxH	MSB (bit[31:16]) of the program entry point.
4	wIndex	2	xxxxH	LSB (bit[15:0]) of the program entry point.
6	wLength	2	0000H	Not in used.

Table 40-11 Vendor Request 5 Setup Command Data Structure

Offset	Field	Size	Value	Description
0	bmRequestType	1	40H	D7 0: Host to Device. D6-D5 2: Vendor. D4-D0 0: Device.
1	bRequest	1	05H	VR_PROGRAM_START2: branch to target address directly.
2	wValue	2	xxxxH	MSB (bit[31:16]) of the program entry point.
4	WIndex	2	xxxxH	LSB (bit[15:0]) of the program entry point.
6	WLength	2	0000H	Not in used.

Copyright © 2005-2019 Ingenic Semiconductor Co., Ltd. All rights reserved.