Serial Flash Secured OTP Area Introduction

1. Introduction

Macronix Serial Flash provides an additional 512 bits or 4K bits of secured OTP (One Time Programmable) memory that resides outside the main memory array. This OTP memory area provides a “one time program” function to permanently store information. The OTP area can be programmed and locked by the factory before shipping or programmed and locked by the customer later. This application note will explain how the customer can use this OTP area as extra memory.

2. Factory Locked and Customer Locked

Normally, serial flash are shipped from the factory with the OTP area unprogrammed (all FFh) and unlocked. Through “Special Order”, customers can request that the factory program an ESN (Electronic Serial Number) into the OTP area and then lock the OTP area so that it cannot be altered.

2-1. Factory Locked

In a Factory Locked device, the factory pre-programs a 128-bit ESN into the OTP area and locks the entire OTP area before shipping. Bit0 (Secured OTP indicator bit) of the Security Register will also be set to ‘1’ indicating that the device was factory locked. Since this bit cannot be set by the customer, cloning a factory locked device would be extremely difficult and provides a higher level of security. To order factory locked devices, please contact Macronix sales directly. Tables 2-1 and 2-2 show the Secured OTP structure and usage for factory and customer locked devices. To determine the Secured OTP memory size of a serial flash device, refer to its datasheet or Table 7-1.

Table 2-1: 512-bit Secured OTP Format

Address range	Size	Standard Factory Lock	Customer Lock
xxxx00~xxxx0F	128 bits	ESN (electronic serial number)	Determined by customer
xxxx10~xxxx3F	384 bits	N/A	

Table 2-2: 4K-bit Secured OTP Format

Address range	Size	Standard Factory Lock	Customer Lock
xxxx00~xxxx0F	128 bits	ESN (electronic serial number)	Determined by customer
xxxx10~xxx1FF	3968 bits	N/A	

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2-2. Customer Locked

In a Customer Locked device, bit0 of the Security Register remains set to '0', indicating that the Secured OTP memory has not been programmed or protected at the factory. In this state, the Secured OTP area is available for use as extra OTP memory space. The bits of the OTP memory area can be programmed to '0', but there is no means to change a '0' bit back to a '1'. If the user wants to protect the OTP from further updates, the Secured OTP area can be permanently locked-down by setting bit1 (LDSO) of the Security Register to '1'. The LDSO bit is OTP. Once it has been set to '1', the Secured OTP area becomes permanently locked and can no longer be programmed. Table 2-3 shows the Security Register bit definitions. Users should refer to the datasheet for more detailed information about setting the Security Register values.

Table 2-3: Security Register Bit Definitions

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WPSEL	E_FAIL	P_FAIL	Continuously Program	x	x	LDSO (lock-down OTP)	Secured OTP indicator bit
1 = individual WP mode	1 = erase fail	1 = program fail	1= CP mode	reserved	reserved	1 = lock-down	1 = factory lock
non-volatile bit	volatile bit	volatile bit	volatile bit	reserved	reserved	non-volatile bit	non-volatile bit
OTP	read only	read only	read only	reserved	reserved	OTP	read only

Note:

1. Some serial flash part numbers only define bit0 and bit1 and reserve the other bits for future use.

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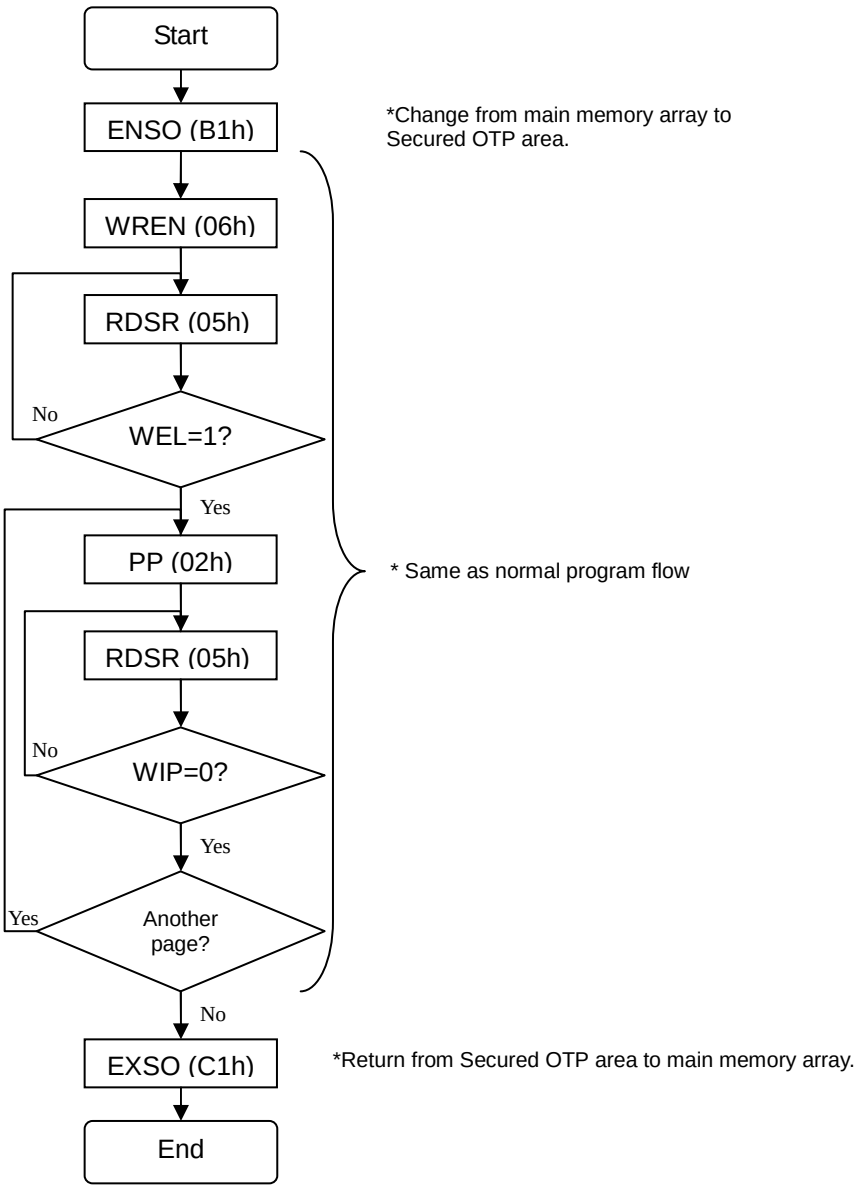
3. Programming Secured OTP Area

If the Secured OTP area has not been factory locked, the Secured OTP area provides either 512 bits or 4K bits of extra OTP memory space. To program the extra memory space, the device must enter the OTP region using the ENSO command (B1h). After entering the OTP region, the normal program flow may be used to program OTP data. The system may check bit0 of the Status Register to determine when the Program operation has completed. Finally, the EXSO command (C1h) is used to exit the OTP region and return to the main memory array. Figure 3-1 shows this flow.

Figure 3-1: Secured OTP Area Program Flow



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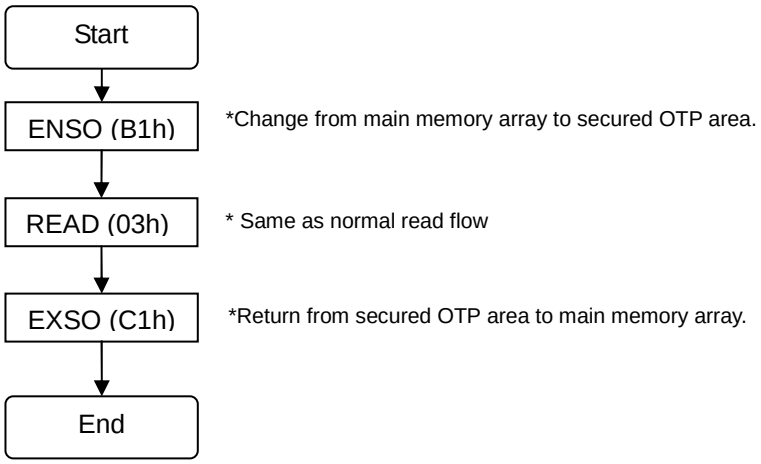
4. Reading Secured OTP Area

To read the Secured OTP area, the ENSO (B1h) command must be executed first to enter the OTP area. The system may use the normal READ (03h) command to read the Secured OTP memory. While in the OTP area, the main array is not accessible. When finished, the EXSO (C1h) command is used to exit the OTP area and return to the main memory array. Figure 4-1 shows the flow.

Figure 4-1: Secured OTP Area Read Flow



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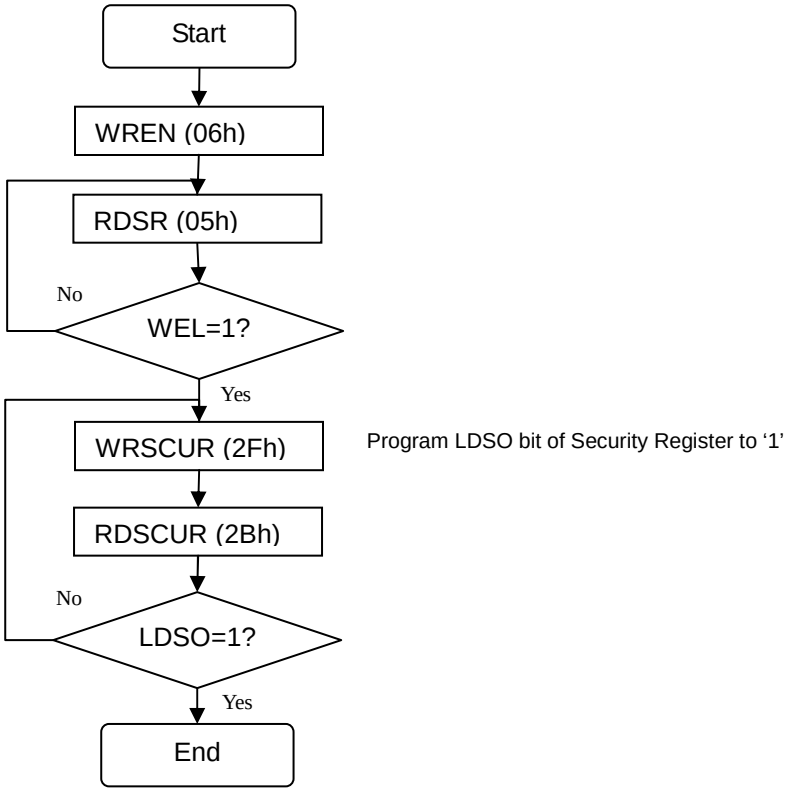
5. Lock Down of Secured OTP Area

Once the user is finished programming the OTP area and wishes that no further updates be allowed, the OTP area can be permanently locked. This is accomplished by issuing the WRSCUR (2Fh) command to set bit1 (LDSO) of the Security Register to '1'. LDSO is an OTP bit. After it has been set to '1', the OTP area is permanently write-protected and can no longer be programmed. Figure 5-1 shows the flow.

Figure 5-1: Secured OTP Area Lock Down Flow



6. Summary

The Secured OTP area provides an extra OTP memory space. It can be programmed and locked by the factory before shipping or programmed and locked by the customer later. If not locked by the factory, the Secured OTP area can be used by the application for data storage.

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7. Macronix Parallel Flash with Security OTP Region

The following Macronix serial flash devices support the Secured OTP area.

Table 7-1: Secured OTP Area Support List

Density	Voltage	Macronix Device	OTP size
2Mb	1.8V	MX25U2033E	4Kbit
4Mb	2.5V	MX25V4035	512bit
	1.8V	MX25U4033E	4Kbit
8Mb	3V	MX25L8006E	512bit
		MX25L8035E/36E/73E/75E	4Kbit
	2.5V	MX25V8006E/35	512bit
	1.8V	MX25U8033E/35E	4Kbit
16Mb	3V	MX25L1606E/33E/73E/75E	512bit
		MX25L1635E/36E	4Kbit
	1.8V	MX25U1635E/35F	4Kbit
32Mb	3V	MX25L3206E	512bit
		MX25L3235E/39E/73E/75E	4Kbit
	1.8V	MX25U3235E/35F	4Kbit
64Mb	3V	MX25L6406E	512bit
		MX25L6435E/39E/73E/75E	4Kbit
	1.8V	MX25U6435F	4Kbit
128Mb	3V	MX25L12835F	
		MX25L12839F	
		MX25L12873F	
		MX25L12875F	
	1.8V	MX25U12835F	4Kbit
256Mb	3V	MX25L25635F	4Kbit
		MX25L25639F	
		MX25L25735F	
	1.8V	MX25U25635F	4Kbit
512Mb	3V	MX66L51235F	4Kbit

8. References

Table 8-1 shows the datasheet versions used for comparison in this application note. For the most current, detailed specification, please refer to the Macronix website.

Table 8-1: Datasheet Version

Datasheet	Location	Data Issued	Version
MX25U2033E	Website	JAN. 04, 2013	Rev. 1.2
MX25U4033E	Website	JAN. 04, 2013	Rev. 1.4
MX25V4035/8035	Website	JUL. 23, 2010	Rev. 1.2.
MX25L8006E	Website	FEB. 10, 2012	Rev. 1.2
MX25L8035E	Website	DEC. 12, 2012	Rev. 1.2
MX25L8036E	Website	JUN. 13, 2012	Rev. 1.1

MX25L8073E	Website	NOV. 13, 2012	Rev. 0.00
MX25L8075E	Website	NOV. 30, 2012	Rev. 1.1
MX25V8006E	Website	FEB. 10, 2012	Rev. 1.2
MX25U8033E	Website	MAR. 20, 2012	Rev. 1.2
MX25U8035E	Website	DEC. 24, 2012	Rev. 1.3
MX25L1606E	Website	FEB. 23, 2012	Rev. 1.4
MX25L1633E	Website	JAN. 09, 2013	Rev. 1.7
MX25L1635E	Website	DEC. 12, 2012	Rev. 1.6
MX25L1636E	Website	JUN. 13, 2012	Rev. 1.3
MX25L1673E	Website	JAN. 02, 2013	Rev. 1.0
MX25L1675E	Website	OCT. 18, 2012	Rev. 1.1
MX25U1635F	Website	DEC. 04, 2012	Rev. 0.00
Mx25U1635E/3235E	Website	DEC. 12, 2012	Rev. 1.7
MX25L3206E	Website	FEB. 23, 2012	Rev. 1.4
MX25L3235E	Website	SEP. 24, 2012	Rev. 1.2
MX25L3239E	Website	JUN. 29, 2012	Rev. 1.0
MX25L3273E	Website	DEC. 25, 2012	Rev. 1.0
Mx25L3275E	Website	SEP. 24, 2012	Rev. 1.1
MX25U3235F/6435F	Website	FEB. 03, 2012	Rev. 1.0
MX25L6406E	Website	JUN. 13, 2012	Rev. 1.5
MX25L6435E	Website	SEP. 06, 2012	Rev. 1.0
MX25L6439E	Website	OCT. 09, 2012	Rev. 1.0
MX25L6473E	Website	DEC 25, 2012	Rev. 1.0
MX25L6475E	Website	SEP. 06, 2012	Rev. 1.0
MX25L12835F	Website	DEC. 26, 2012	Rev. 1.1
MX25L12839F	Website	AUG. 10, 2012	Rev. 0.00
MX25L12873F	Website	NOV. 14, 2012	Rev. 0.00
MX25L12875F	Website	JUL. 11, 2012	Rev. 0.00
MX25U12835F	Website	DEC. 17, 2012	Rev. 1.2
MX25L25635F	Website	DEC. 26, 2012	Rev. 1.1
MX25L25639F	Website	SEP. 05, 2012	Rev. 0.01
MX25L25735F	Website	OCT. 30, 2012	Rev. 1.0
MX25U25635F	Website	DEC. 14, 2012	Rev. 1.0
MX66L51235F	Website	AUG. 08, 2012	Rev. 0.00

9. Revision

Table 9-1: Revision History

Revision	Description	Date Issued
Rev. 1.0	Initial Release	Feb. 25, 2012

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For the contact and order information, please visit Macronix's Web site at: http://www.macronix.com